JoSIM and InductEx Integration into XIC

Quick Start Guide

Version SU1.2

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1 Introduction

The JoSIM and InductEx integration was developed under IARPA contract SuperTools(via the U.S. Army Research Office grant W911NF-17-1-0120). The XIC integration is split into two components, JoSIM and InductEx integration. This adds both JoSIM and InductEx circuit simulation functionality to XIC.

The JoSIM integration for XIC enables users to simulate a circuit with the JoSIM circuit simulator as well as the WRspice circuit simulator. JoSIM uses the .cir file generated from a schematic captured with XIC to simulate the circuit. JoSIM then outputs a file that can be used by the plot function of WRspice. The output of both JoSIM and WRSpice can be plotted together to allow for easy comparison between the two simulation methods.

The InductEx integration for XIC enables users to extract parameter values for a circuit layout using InductEx from the XIC layout environment. The the physical and electrical layer is converted into a format used by InductEx. The whole process executes in a separate terminal window.

2 Prerequisites

InductEx and JoSIM will be required to make use of the added functionality added to XIC. The install locations of each is indicated below:

2.1 JoSIM Install Location

XIC will search for JoSIM in the environment path as "josim".If the environment PATH is not set, the JoSIM executable ("josim") will be searched for in *usr/local/bin* as default. JoSIM is available at *https://github.com/JoeyDelp/JoSIM*

2.2 InductEx install Location

XIC will search for InductEx in the environment path as "inductex". If the environment PATH is not set, the InductEx executable will be searched for in the recommended default location: *usr/local/bin* . InductEx is available at *www.inductex.info*

3 Installing XIC

The XIC version with the integrated JoSIM and InductEx functionality can be installed using the precompiled CentOS 7 packages or from source.

3.1 CentOS 7 Packages

The precompiled packages for CentOS 7 are available on Github. Download the folder containing all the precompiled packages and run the installer as follows:

$ sudo ./wr_install all

Thereafter, XIC will be executable using the following command:

$ /usr/local/xictools/xic/bin/xic

3.2 Source Code

The source code is available at: **https://github.com/bernardventer/xictools.git** Follow the instructions on the **README** page for installation instructions.

4 Example Instructions

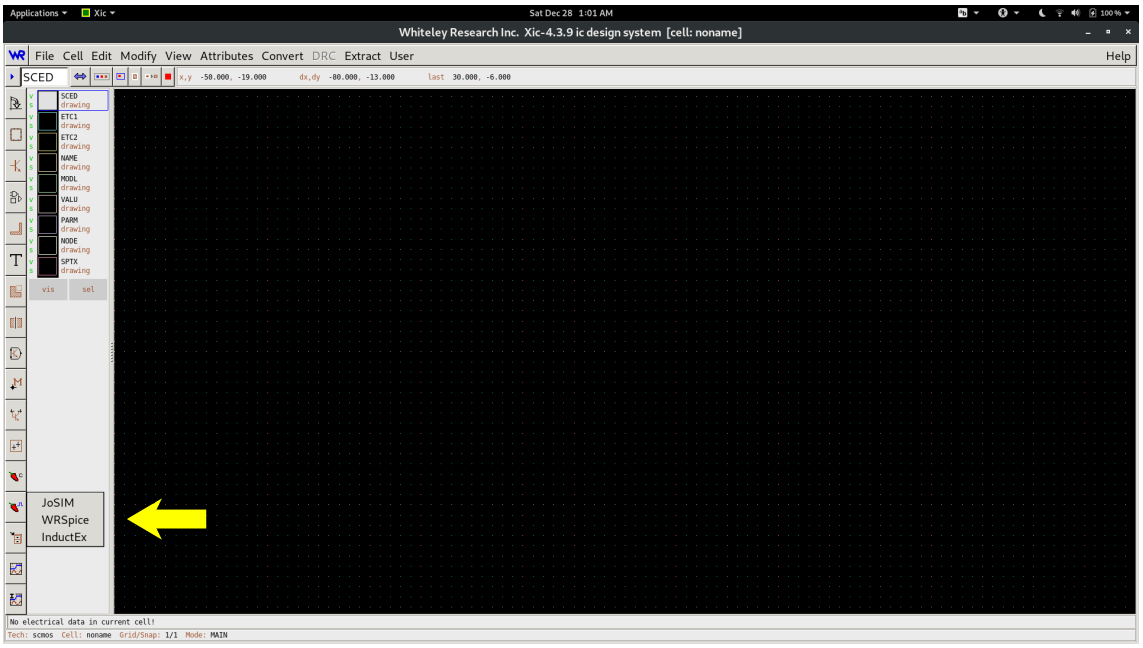

Figure 1: The Run command visible in the Electrical View of XIC. JoSIM, WRspice and InductEx is executed from the Run command.

4.1 JoSIM

1. Open XIC and select File → Open → New.
2. From the Pop-up Window, change the current working directory to the folder containing the circuits (File → new CWD).
3. Load the circuit to be simulated (eg .gds).
4. Switch to the Electrical view by clicking on View → Electrical.
5. **It is recommended to use the WRspice method first**. Run WRspice using using run → WRspice on the side menu and follow the instructions. Figure 1 shows the Run command.
6. Plot the results using plot command and select the nodes to be plotted.
7. Keep the Plot window open for comparison.
8. Run JoSIM using run → JoSIM on the side menu.
9. Enter the analysis command that will be used to simulate the circuit in JoSIM in the prompt box below and press enter.
10. If the JoSIM executable is not in the default location, the file has to be selected through the pop-up file select.

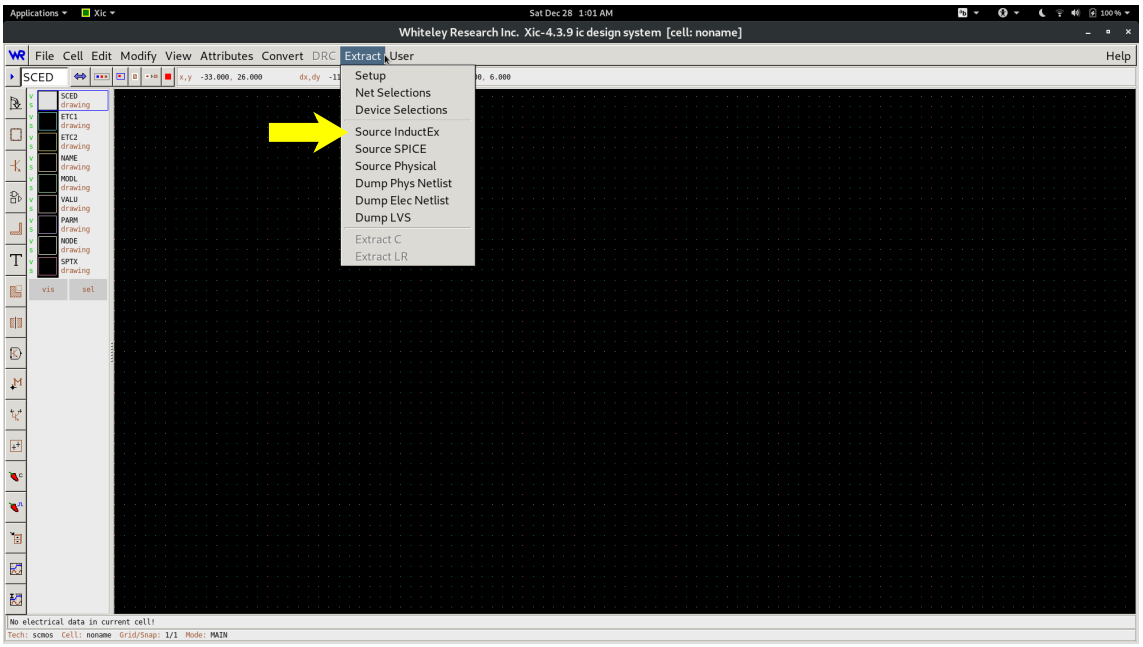

Figure 2: The values extracted from InductEx is back annotated to the XIC environment using the Extract → Source InductEx.

11. Plot the output as for WRspice.

4.2 InductEx

1. Open XIC and select File → Open → New.
2. From the Pop-up Window, change the current working directory to the folder containing the circuits (File → new CWD).
3. Load the circuit to be simulated (eg .gds).
4. Switch to the Electrical view by clicking on View → Electrical.
5. Run InductEx using run → InductEx on the side menu. Figure 1 shows the Run command.
6. Enter the analysis command that will be used to simulate the circuit in InductEx in the prompt box below and press enter.
7. Select the LDF file that will be used for the circuit in the file select menu.
8. Choose which numerical engine to make use of. Type f for FFH and t for TH.
9. The InductEx simulation of the circuit is executed in the terminal window.
10. The output of the simulation can be found in the current working directory of XIC.

4.3 Back Annotate

1. InductEx outputs the extracted impedance values into a circuit netlist file (**IDXout.elecnet**).
2. The extracted impedance values are back annotated by selecting Extract → Source InductEx. Figure 2 shows the InductEx back annotated command.
3. The component values are replaced with the extracted values.
4. The circuit with the updated values are simulated using JoSIM and WRspice.

4.4 Plotting Nodes

Select the desired nodes first using the plot command **This must be done before using the JoSIM command.** This allows the desired nodal values to be loaded into JoSIM for analysis. The nodal values can then be plotted using the plot command again after JoSIM was executed.

5 Output Data

5.1 JoSIM

The data output generated by JoSIM will be dumped in the current working directory. The output data file contains the values of the nodes at each time step. The output file is generated in a format that can be used by the plotting function used by XIC.

5.2 InductEx

The solution files generated by InductEx is found in the current working directory as specified by the user. The extracted inductance from the circuits is outputted as a circuit netlist file called IDXout.elecnet. The IDXout.elecnet file contains the extracted values compatible with XIC.

Appendices

A Recommended Design Rules

The recommended design rules for the electrical and physical layer is given below. These rules ensure the correct ports are generated for the InductEx input file.

A.1 Port Names

1. The Ports for the input and output nodes may have any name **but must start with a P**. The ports will match the names given to the nodes. **Example:** node (internal): v(PIN) will match the input Port PIN in the physical region and node (internal): v(PX1) will match to the Port PX1 in the physical region.
2. **PB** label for the port replacing the current source.
3. **PR** label for the port replacing the resistor connected to ground.

A.2 Naming Convention

1. Rename the JJ to the **B** component label to match that of the port assigned to it. The same as seen on the circuit diagram designed. Ex B1 must be used for J1 port, B10 for J10 etc.
2. Use the **IB** label for the current sources and match the numbering to that of the PB label. Ex. IB3 for port PB3 etc.
3. **RP** is used for the resistors connected to ground that will become ports. Keep the numbering constant. EX RP1 for PR1
4. **RB** for JJ resistor
5. **LRB** for JJ inductor
6. **LP** for inductor connecting the - JJ port to ground.
7. **L** for regular inductors
8. **LB** for current source inductors.