LAB 3

Datapath

LABWORK

Design a circuit with:

4 of 8 bit Register (Flipflop)

1 of 8 bit adder

3 of 8 bit 4 optional MUX

4 of 8 bit 2 optional MUX

1 of 8 bit Unidirectional Tri-BUS

and necessary controller signals and inputs/outputs to do add operation.

Timeline:

T: load data to Register A (A0 Hex)

T+1: load data to Register B (0B Hex)

T+2: add the data in register A and register B to Register C

T+3: Show output of register C

T+4: load data to Register D (06Hex)

T+5: add the data in register C and register D to register C

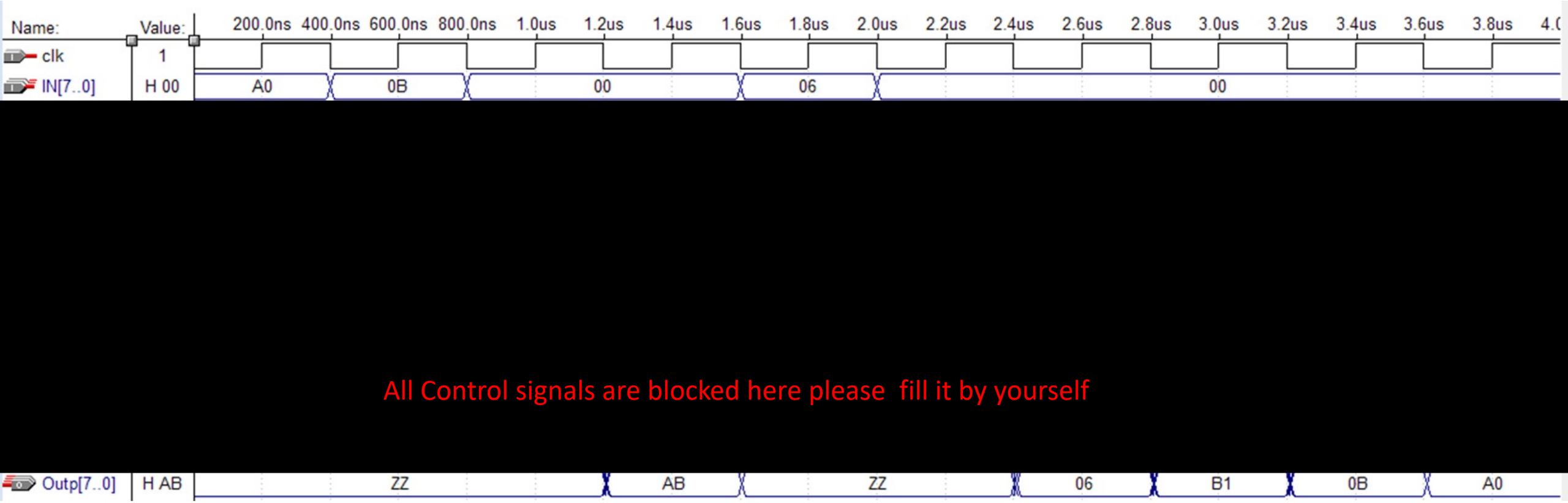
T+6: Show output of register D

T+7: Show output of register C

T+8: Show output of register B

T+9: Show output of register A

Example output



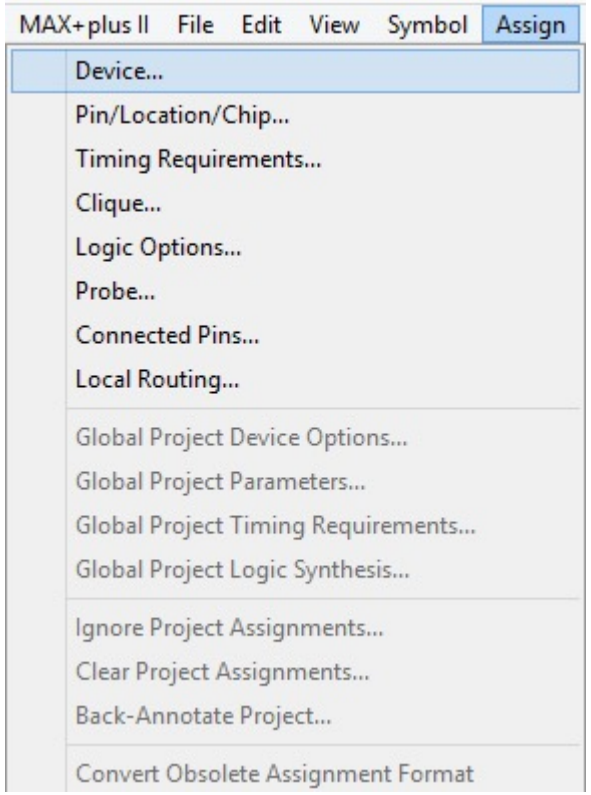
Set End time to 4us.(File-> End Time)

Grid size to 200ns
(Options->Grid Size)

Possible Errors Part 1

- Your project may not be fit in device so you should do those steps:
- Select
- Assign

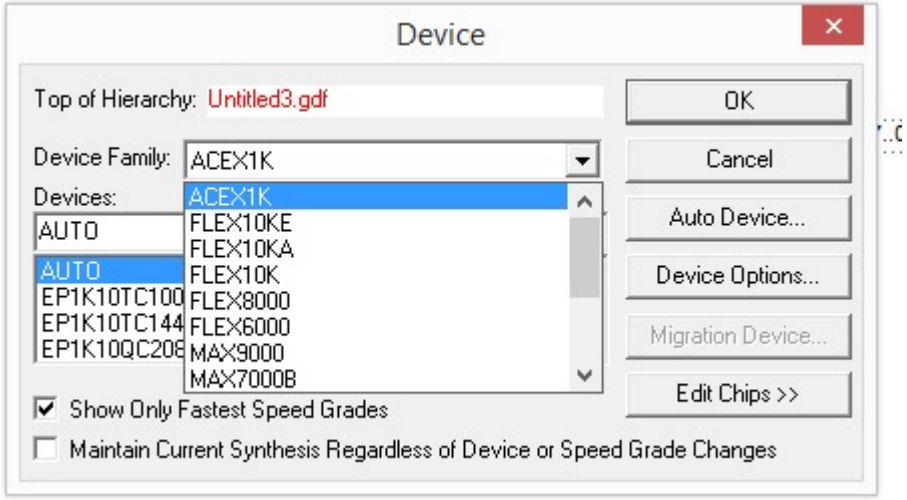
1. Devi



Select

Device Family

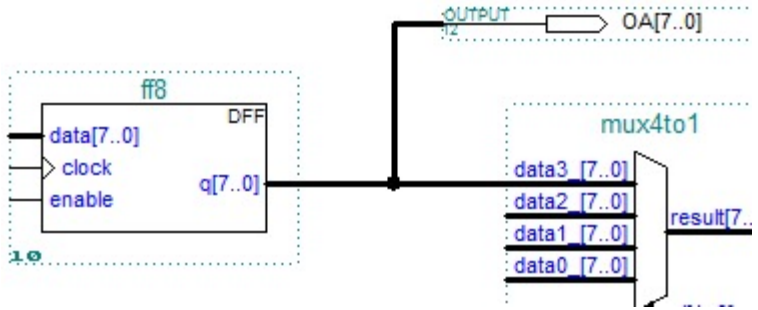
ACEX1K



Possible Errors Part 2

- You may get an error like this

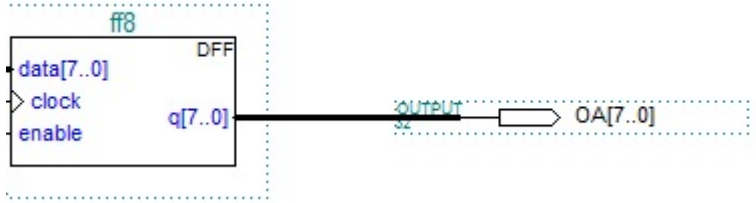
- Please add 4 outputs for 4 flip flops. Ie:



Possible Errors Part 3

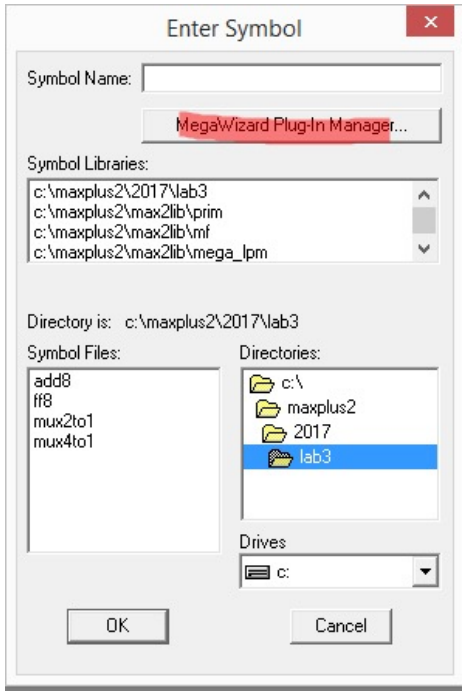
If you put a 1 bit output for an 8 bit output it will give this error when you click save and check

You have to change line to bold and write the necessary bit value to end of the output/signal

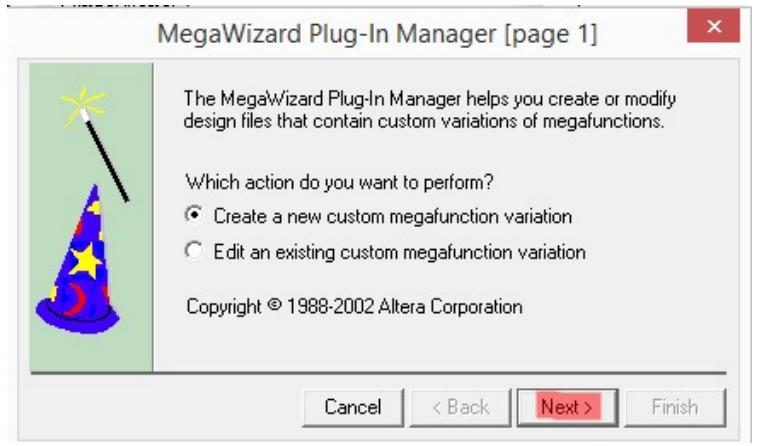


Hint 1 Adding a Component : 8 Bit Register: Part 1

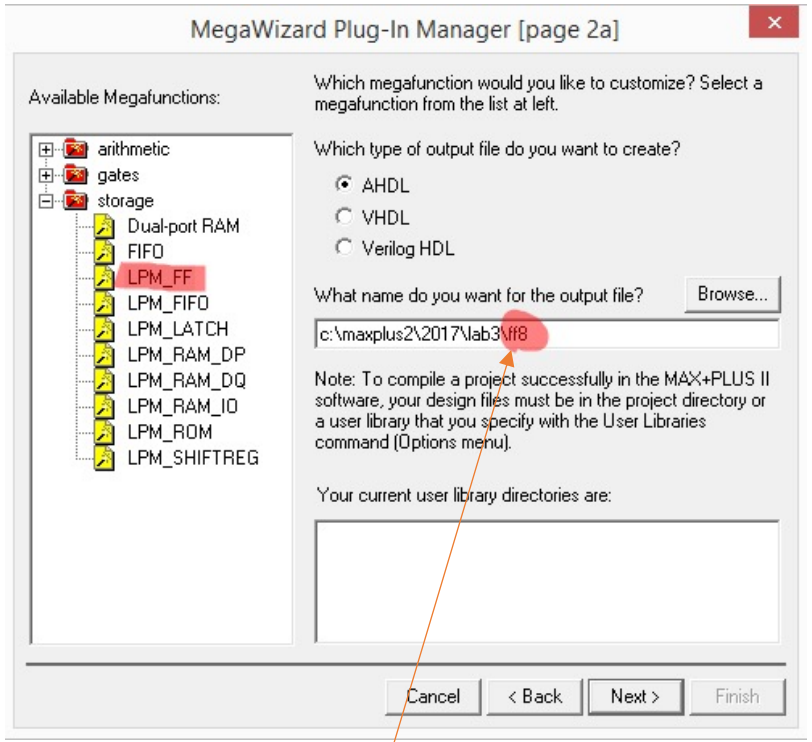
1



2



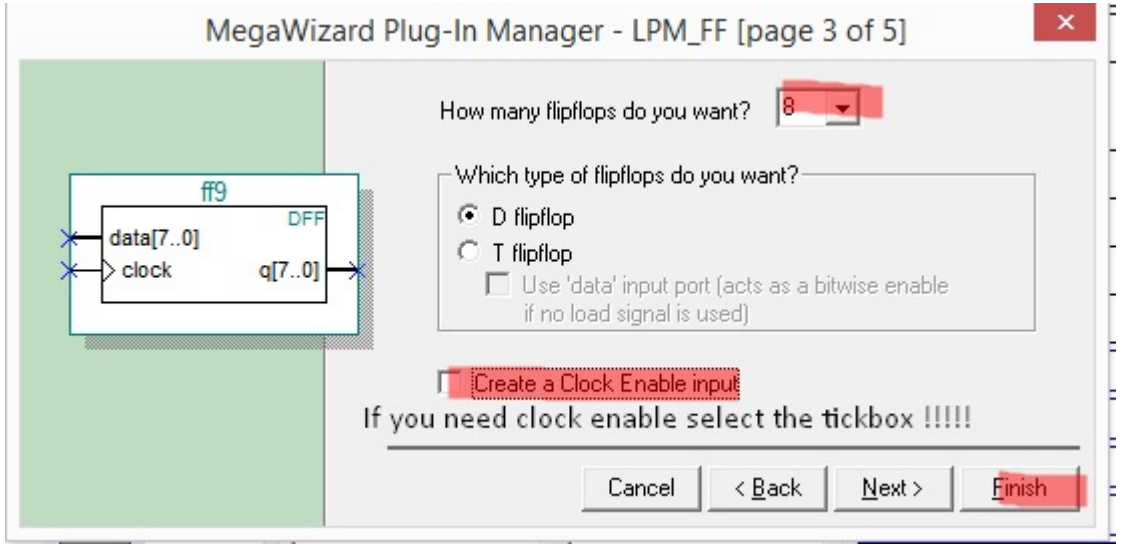
3



Please enter the path of your project file here

How to add 8 Bit Register: Part 2

4



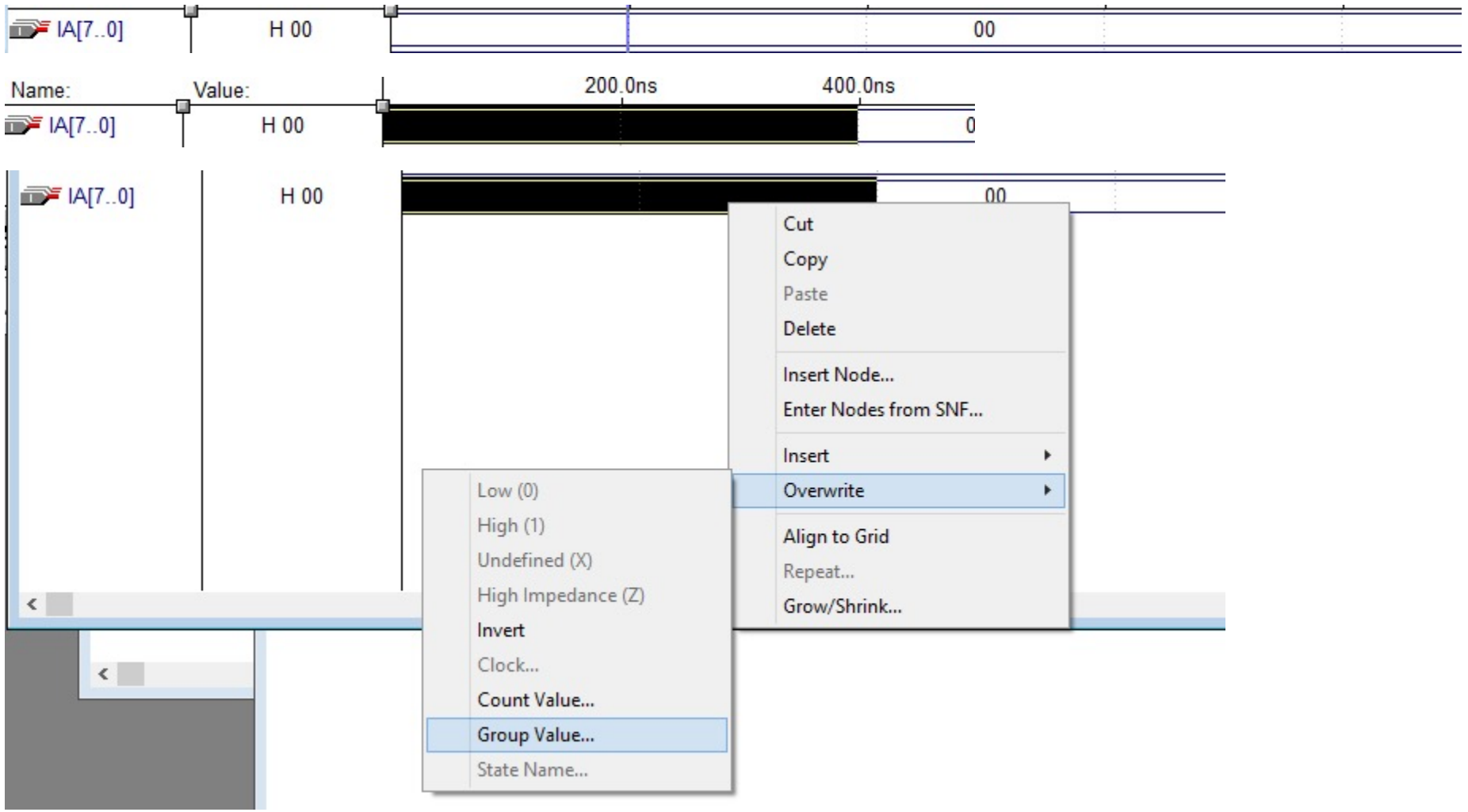
- Add the other necessary components. Please read all the options in component window Carefully
- !!!!!!!!!

Hint 2: Giving a value to signal simulation file Part 1

1

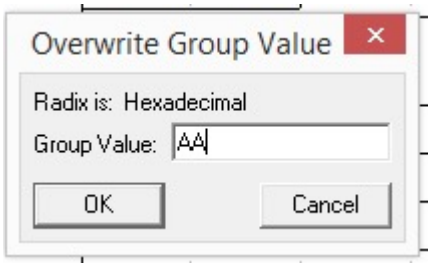
2

3



Hint 2: Giving a value to signal simulation file Part 2

4



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