KA49522A
Application Notes

Battery Monitoring IC (BMIC)
for Industrial Application

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Contents

Chapter 1 Overview

1.1 Description

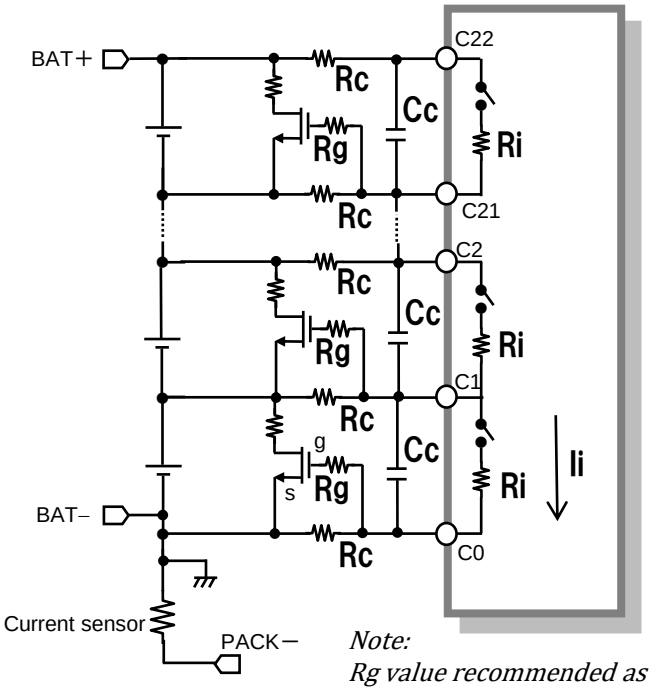
This is the application note for using KA49522A, which is a battery monitoring IC with protection function.

All the materials in this application notes are provided as design references only and not mass production guaranteed.

Sufficient evaluation and verification is required prior to mass production.

Chapter 2 Input RC and components setting for Cell Balance operation

2.1 RC external Cell Balancing



Note:
Rg value recommended as 1kohm for hotplug solution

Fig.2.1.1 Parameter for external cell balance

1) *Calculate Rc*

$$Vgs = \frac{Vcell * Rc}{2Rc + Ri} \qquad Ri = 20ohm$$

$Vgs \geq Vth(in\ order\ to\ turn\ on\ FET)$

$Suppose\ Vth = 1.5V$ Vcell = 3.7V

$$Rc \geq Ri * \frac{Vth}{Vcell - 2Vth} = 43ohm$$

$and\ Rc < 5kohm\ (for\ input\ impedance\ limitation)$

$Rc = 1kohm{\sim}4kohm\ is\ recommended$

2) *Calculate Cc*

$$fc = \frac{1}{2\pi * 2Rc * Cc} \leq \frac{fs}{2}$$

$fc\ depends\ on\ the\ sampling\ time\ of\ our\ system$

$$\left(MAX(fc) = \left(\frac{fs}{2}\right) = \frac{1}{50us * 2} = 10KHz\right)$$

$eg.when\ fs = 20KHz, Rc = 1kohm$

$$Cc \geq \frac{1}{fs * \pi * 2Rc} = 0.008\text{uF}$$

$Using\ 10 * Cc\ \ is\ recommended$

2.2 RC internal Cell Balancing

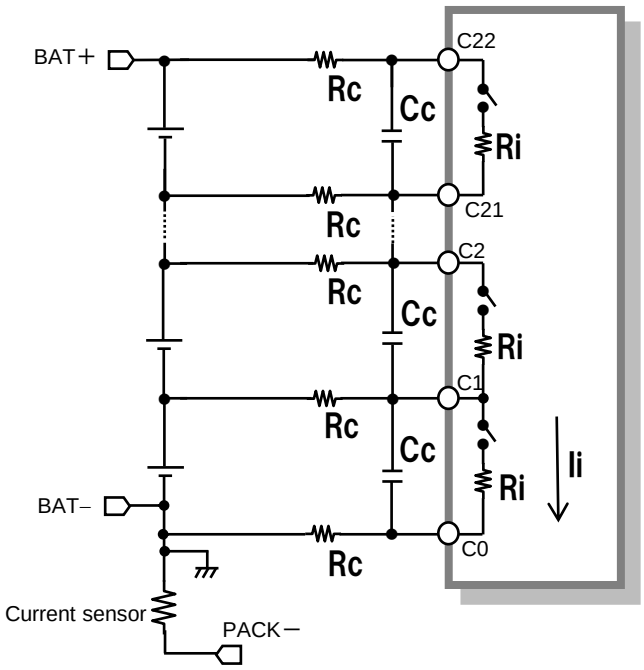


Fig.2.2.1 Parameter for internal cell balance

1) *Calculate Rc*

$$Ii = \frac{Vcell}{2Rc + Ri}$$

$Ii\ depends\ on\ the\ design\ target\ of\ your\ system$
$(Max(Ii) = 50mA)$

$Suppose\ Vcell = 4.2V\ \ Ii = 50\text{mA}$

$$Rc \geq \frac{1}{2} * \left(\frac{Vcell}{Ii} - Ri\right) = 32ohm$$

2) *Calculate Cc*

$$fc = \frac{1}{2\pi * 2Rc * Cc} \leq \frac{fs}{2}$$

$fc\ depends\ on\ the\ sampling\ time\ of\ our\ system$
$(MAX(fc) = \left(\frac{fs}{2}\right) = \frac{1}{50us*2} = 10KHz)$

$eg.when\ fs = 20KHz, Rc = 40ohm$

$$Cc \geq \frac{1}{fs * \pi * 2Rc} = 0.2\text{uF}$$

$Using\ 10 * Cc\ \ is\ recommended$

Chapter 2 Input RC and components setting for Cell Balance operation

2.3 NMOS for external cell balancing

When applying VBAT, high voltage may occur transiently between the external FET pins for cell balance because normally there is RC filter at VBAT line.

External Cell balance FET with high voltage tolerance is highly recommended to withstand this transient spike.

In case high voltage tolerance FET cannot be used in the system, user can consider to separate VBAT from C17 as shown in Fig.2.3.2.

Battery cells connection sequence is documented on page 20

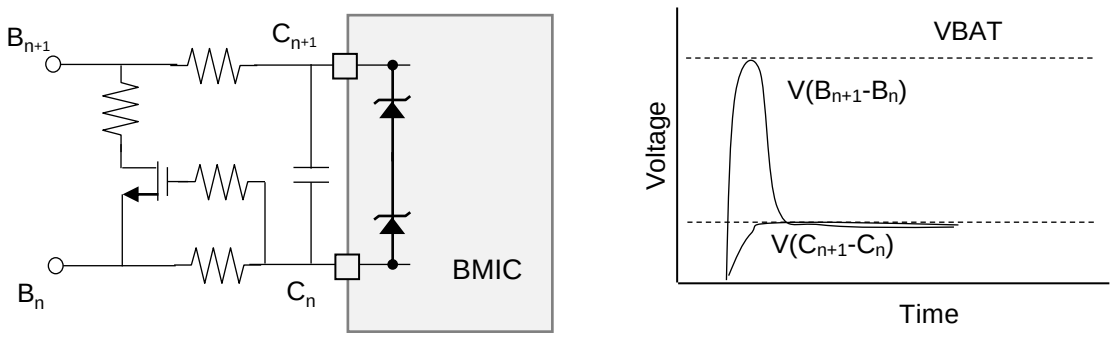


Fig. 2.3.1 Transient High Voltage

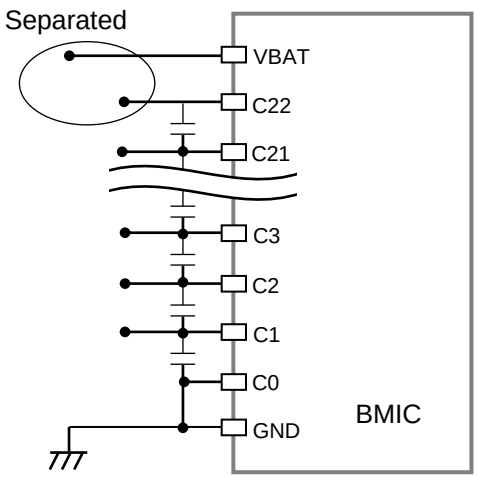


Fig. 2.3.2 Separated VBAT

Chapter 2 Input RC and components setting for Cell Balance operation

2.4 BJT for external cell balancing

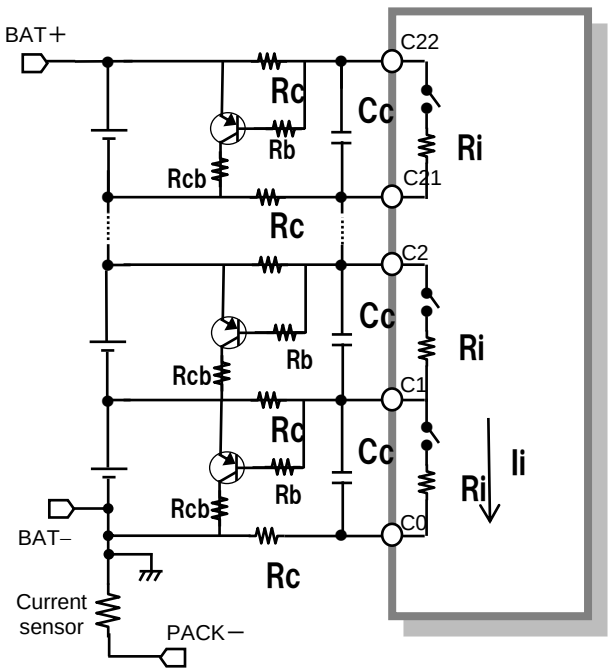


Fig. 2.4.1 Cell balance PNP

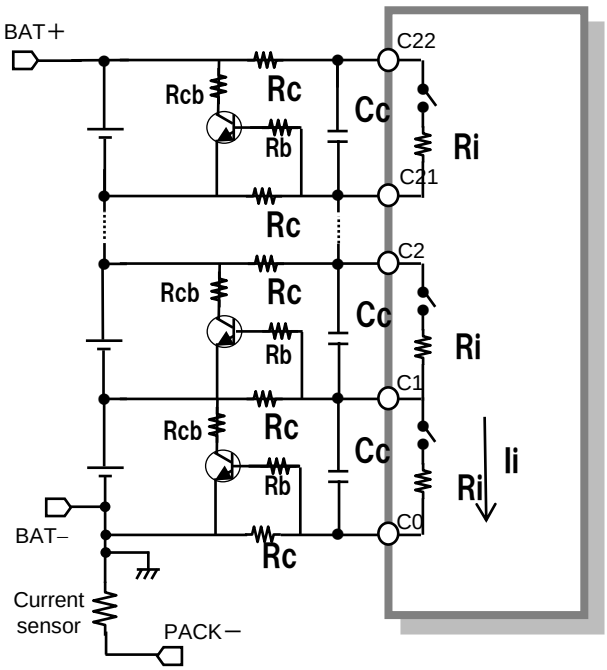


Fig. 2.4.2 Cell balance NPN

Example for parameter selection :

Rc=1kohm, Rcb =75ohm, Rb=100ohm

PNP BJT BC856 (Veb = 0.8V, Vce(sat)= -0.1V)

Icb = (Vcell - Vce(sat)) / Rcb = 48mA when Vcell = 3.7V

Chapter 3 High-Side Switch and Charge Pump components setting

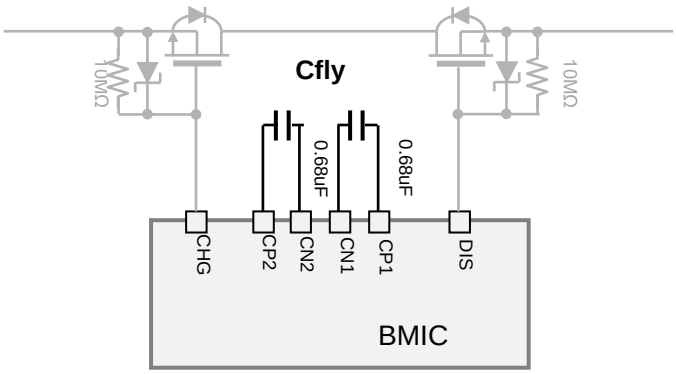
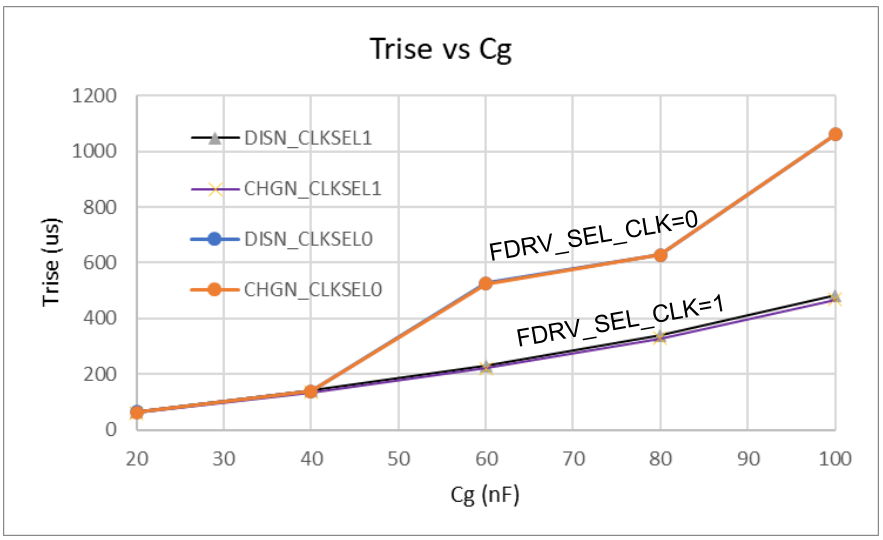


Fig. 3.0 Flying Capacitor & FET Gate Capacitance

Flying capacitor (Cfly) is the capacitor connected across CP1/CN1 or CP2/CN2. The voltage across this capacitor is charged to 11V(typ) internally. FET Gate capacitance (Cg) is the total capacitance at the gate terminal of the external NFET switch. During operation, charge from Cfly is transferred to Cg periodically to turn on the external NFET switch. The value of Cfly & Cg will affect both FET driver turn on rise time (Trise) & turn off fall time (Tfall).

3.1 Cg affecting FET Driver Rise Time

The internal charge pump is operating with a default clock of 2kHz. In application when large Cg is used, the FET driver turn on rise time might be longer than the clock period. The internal clock frequency can be slowed down to 500Hz, by setting FDRV_SEL_CLK (0x04[11]) to “1”.
Fig 3.1.1 shows the FET driver turn on rise time versus Cg capacitance when FDRV_SEL_CLK=1/0. This register function should be set before turning on the FET. After the FET is turned on, reset the charge pump to operate at default 2kHz.



Note:
Cfly = 680nF,
Trise = 10% to 90% delay

Fig. 3.1.1 FET Driver Rise Time

Chapter 3 High-Side Switch and Charge Pump components setting

3.2 Cg affecting FET Driver Fall time

Fig 3.2.1 shows FET Driver Fall Time versus Cg.
As Cg increases, longer fall time is expected to turn OFF the FET

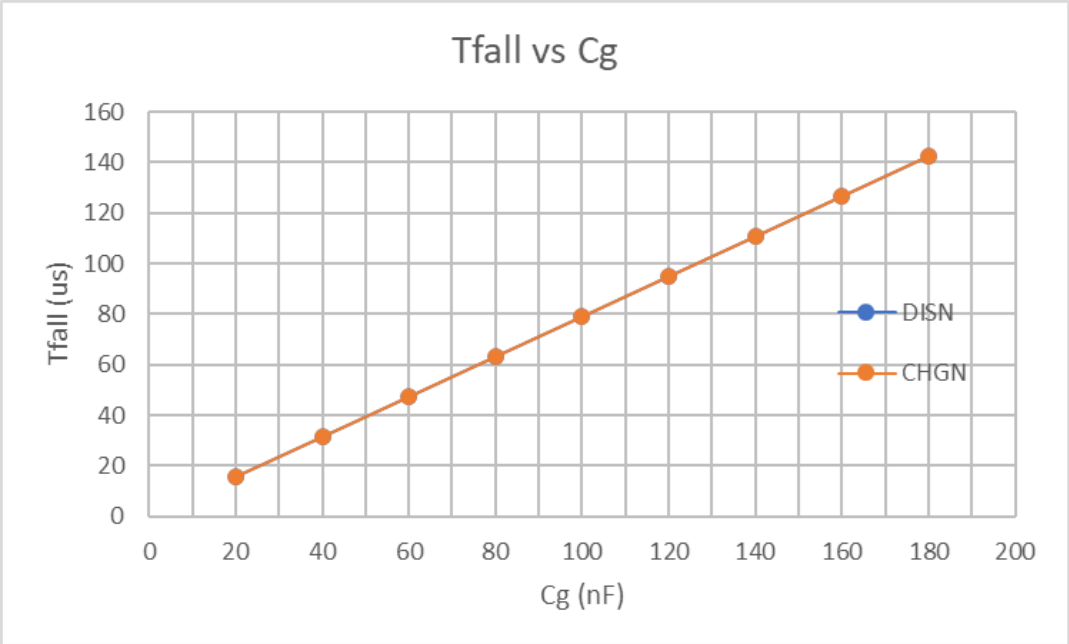


Fig. 3.2.1 FET Driver Fall Time

Note : Cfly = 680nF, Tfall = 90% to 10% delay

Chapter 3 High-Side Switch and Charge Pump components setting

3.3 Cfly affecting FET Driver Rise time

During FET 1st turn on, a portion of Cfly charge is transferred to Cg resulting in a transient voltage drop.

If this drop is more than 10%, Trise will take more than 1 charge pump clock cycle to reach 90% of its steady state.

Fig 3.3.1 shows FET Driver Rise Time versus Cfly.

When Cfly is not sufficiently larger than Cg, FET turn on rise time increases

Fig. 3.3.1 FET Driver Rise Time

Note : Cg = 200nF, Trise = 10% to 90% delay, FDRV_CLK_SEL = 1

Chapter 3 High-Side Switch and Charge Pump components setting

3.4 Effective FET gate capacitance (Cg) estimation

Fig 3.4.1 shows a typical VGS vs Qg graphs in a FET specification.
In this example, the FET has the following characteristics :

1) At V_{DD}=50V and I_D=180A,
2) ~175nC need to be discharge to get Vgs back from 10V to 0V,
3) Hence, the effective Cg = Qg/Vgs =17.5nF.

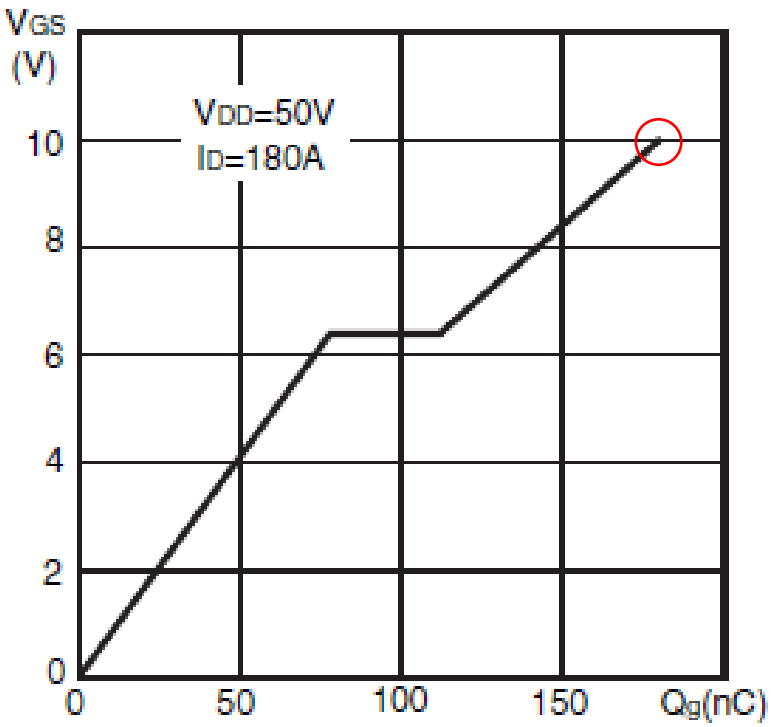


Fig. 3.4.1 Gate charge vs gate-source voltage

Note 1 :
When using power MOS FET in parallel, it is recommended to insert resistor around 50-100ohm (tuned the value by evaluation) between each gate of FET.
This may reduce abnormal voltage vibration during high current on off operation.

Chapter 3 High-Side Switch and Charge Pump components setting

3.5 High-side PMOS driving by GPOH pins

GPOH1/2 are driven by open-drain FET, so the Cg need not to be taken too much care of.

However, a resistor bigger than 100kohm is needed to limit the current flowing from Gate into GPOH pin.

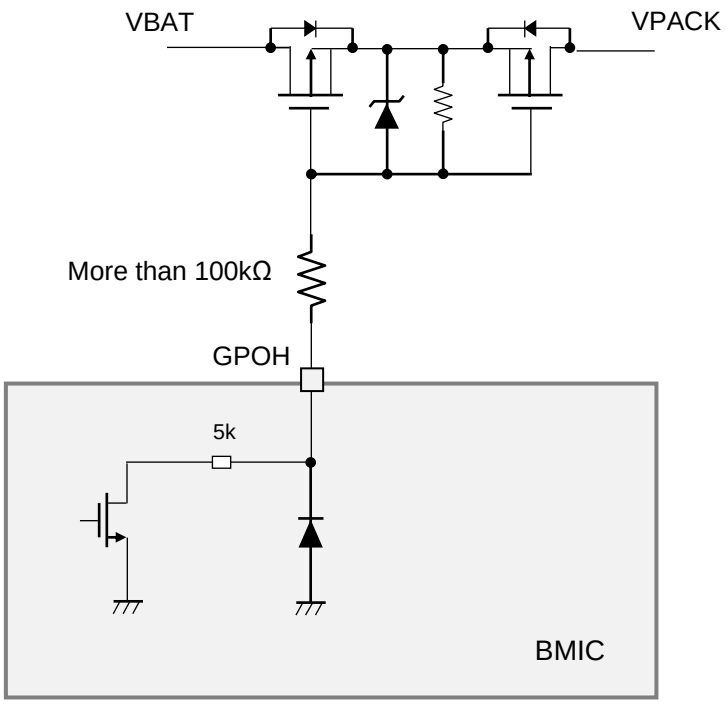


Fig. 3.5.1 Circuit example when using GPOH

Chapter 4 REG55 Components and Registers setting

4.1 REG55 RC and BJT components

VDD55 BJT and RC devices must be connected as shown in Fig .4.1.1.

C_{REGB}, R_{REGB}, C_{VDD55}, R_{VDD55} should be selected according to the loop characteristic of the regulator design with the select NPN BJT. The recommended RC values with the accompany BJT devices are shown in Table.4.1.2 below. These devices are to be used together with the recommended NPN BJT to ensure the best stability and load transient performance for VDD55 regulator. In case NPN BJT is changed from the recommended list, it is necessary to perform enough evaluation check and optimize the RC value again.

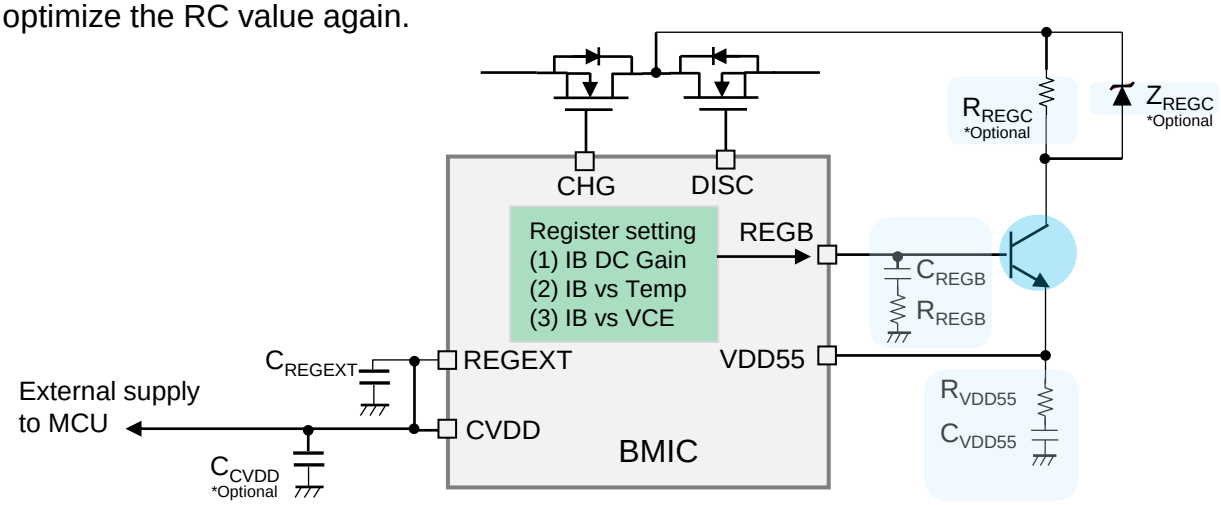


Fig. 4.1.1 VDD55 circuit

Component \ NPN	Recommended Component Value		Remark
	MJD340 (Diodes) MJD47 (ON Semi) MJD340 (ON Semi)	DXT696BK (Diodes)	
C_{REGB}	22nF	68nF	<±50% for stability.
R_{REGB}	18kΩ	1kΩ	
C_{VDD55}	10uF	22uF	<±30% for stability.
R_{VDD55}	0.1Ω	0.1Ω	
R_{REGC}	Depends on thermal performance of NPN and operating condition.		
Z_{REGC}	—	Depends on minimum VBAT level.	Use with R_{REGC} to bypass transient current.
C_{REGEXT}	1uF	1uF	
C_{VDD55} / (C_{REGEXT}+C_{CVDD}) Ratio	> 5	< 5 (Limited by 5ms startup time)	Meet ratio requirement in tolerance condition.

Table. 4.1.2 Recommended BOM for VDD55 regulator

Chapter 4 REG55 Components and Registers setting

VDD55 BJT and RC devices must be connected as shown in Fig .4.1.1.

When selecting the NPN BJT, it is recommended to consider the following key factor as listed in Table 4.1.3 below. Recommended BJT are listed in Table 4.1.2

BJT Parameters	Minimum	Maximum	Notes.
DC current gain (h_{FE})	Depends on output current needed	Depends on stability of regulator.	$h_{FE} = I_C / I_B$ (I_B is base current from REGB pin. I_C is output collector current.)
Continuous collector current (I_C)	Internal IC loading (10mA) + REGEXT loading needed (max 50mA)	Depend on NPN current rating as well as thermal performance	REGEXT can be used as power supply for CVDD pin and external circuit. OCP of REGEXT is up to 200mA. In case $I_{VDD55} < I_{REGEXT}$, due to the use of lower beta NPN like MDJ340 from diodes, it is necessary to keep 5 times ratio of $C_{VDD55}/(C_{REGEXT}+C_{CVDD})$ to ensure stability. If 5 times ratio cannot be met, it is recommended to design $I_{VDD55} > I_{REGEXT}$ by using higher Beta NPN like the DXT696BK from diodes.
Collector emitter voltage (V_{CEO})	> Charger input or >$VBAT_{max}$ with sufficient margin	--	Maximum battery level $VBAT_{max}$ or charger input voltage will be seen at V_{CE} of the NPN. It is necessary for selected NPN to be able to withstand this voltage applied to it with sufficient margin being considered.
Thermal	$Tj = (Pd \times \theta_{j-a}) + Ta$	--	(1) Tj ≦Tjmax BJT; (2) θ_{j-a} : Junction to ambient thermal Coefficient (It is recommended to have enough evaluation with the final PCB to determine actual θ_{j-a} and Tj of the NPN) (3) Ta=Ambient Temperature (4) Pd= ($VBAT_{max}$-5.5V) x I_{Cmax}

Table. 4.1.3 VDD55 BJT selection consideration

Chapter 4 REG55 Components and Registers setting

4.2 REG55 Registers selection

As shown in Fig .4.1.1. there are 3 registers setting inside IC to ensure collector output current remains relatively constant given the parameters variation of BJT device.

In a typical BJT device, the DC current gain h_{FE} tends to drift vs Temperature and V_{CE} voltage. This will result in a wide variation of output collector current.

By setting the 3 available registers setting, it is possible to reduce this variation.

(1) Output base current I_B setting.

The first setting is to determine the required output base current (I_B). I_B can be adjusted between the range of 0.7mA ~ 2.65mA as shown in Table 4.2.1 below. Depending on the selected NPN h_{FE}, suitable I_B can be set by this R55GAIN[2:0] registers at address 56h[9:7] to achieve the required collector current I_C.

Some of the recommended NPN R55GAIN selection with the required collector current I_C is shown in table 4.2.1 below.

R55GAIN [2]	R55GAIN [1]	R55GAIN [0]	I_B (mA)	hfe	I_C (mA)	NPN
1	0	0	2.467	60		
1	0	1	1.860	80	150	MJD47 (ON Semi)
1	1	0	1.445	100		
1	1	1	1.204	120		
0	0	0	0.950	150	150	MJD340 (Diodes)
0	0	1	0.833	170		
0	1	0	0.730	190		
0	1	1	0.655	215	150	MJD340 (ON Semi)
				415	300	DXT696BK (Diodes)

Table. 4.2.1 VDD55 Base current output range (for VBAT=81.4V)

Chapter 4 REG55 Components and Registers setting

(2) Output base current I_B vs Temperature compensation setting.

In NPN device product specs, Gain value (h_{FE}) vs temperature profile can be obtained. This information can be used to decide I_B vs temperature compensation.

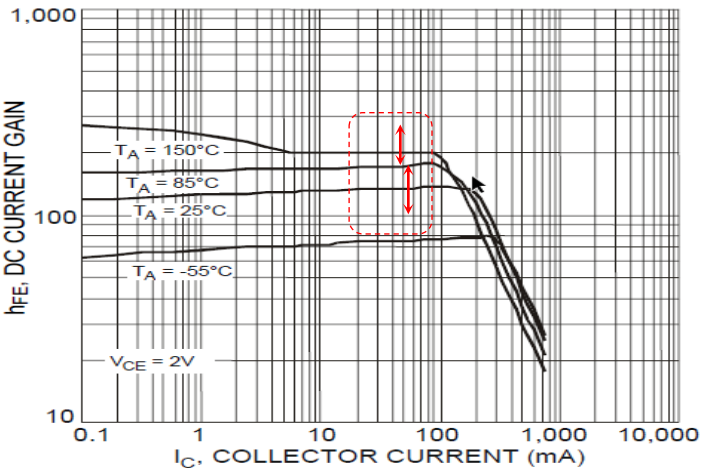


Figure. 4.2.2 Typical NPN hFE vs Ic vs Temperature graphs

Figure 4.2.2 shows a typical NPN h_{FE} vs collector current I_C with temperature trend. From the graph, we can tell the NPN h_{FE} variation vs temperature

BIT	[100]	[101]	[110]	[111]	[000]	[001]	[010]	[011]
Temp(°C)	IB(mA)							
-25	1.923	1.839	1.764	1.681	1.596	1.513	1.437	1.352
25	1.334	1.31	1.295	1.272	1.247	1.22	1.205	1.182
85	0.912	0.931	0.955	0.975	0.99	1.011	1.037	1.058
From 25 to -25 (%△)	44.2	40.4	36.2	32.2	28.0	24.0	19.3	14.4
From 25 to 125°C (%△)	-31.6	-28.9	-26.3	-23.4	-20.6	-17.1	-13.9	-10.5

Figure. 4.2.3 R55TC selection register settings for base current

Figure 4.2.3 shows R55TC register selection range. (Address 56h[6:4])
There are 8 selection level with different temperature gradient.
User should select the most suitable base current temperature curve to cancel out the NPN temperature characteristic

BIT	[100]	[101]	[110]	[111]	[000]	[001]	[010]	[011]
Temp(°C)	IC(mA)							
-25	123	117	115	113	111	109	106	103
25	105	104	103	102	101	100	99	98
85	96	97	98	100	98	102	104	106
From 25 to -25 (%△)	17.1	12.5	11.7	10.8	9.9	9.0	7.1	5.1
From 25 to 125 (%△)	-8.6	-6.7	-4.9	-2.0	-3.0	2.0	5.1	8.2

Figure. 4.2.4 collector current Temperature trend after compensation

From Figure 4.2.4, we can obtain a temperature flat collector current as shown by selecting [001] I_B selection in this example.

Chapter 4 REG55 Components and Registers setting

(3) Output base current I_B vs Supply (or V_{CE}) compensation setting.

h_{FE} vs NPN V_{CE} voltage characteristic is normally not provided in a typical NPN specs. This characteristic can be obtained by makers of the NPN. Alternatively, this characteristic can be obtained through bench test.

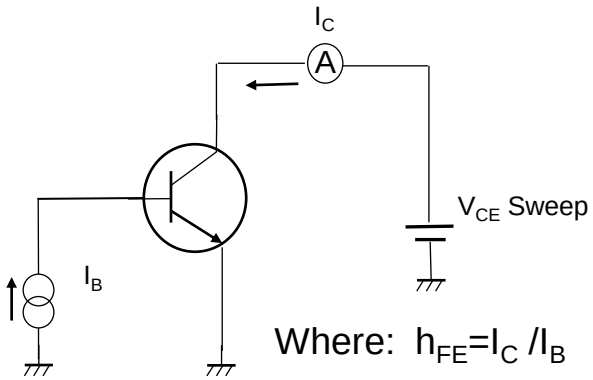


Figure 4.2.5 shows a typical setup to measure NPN h_{FE} vs V_{CE} profile. By this measurement, user can know how much hFE can be varied within a certain V_{CE} or battery supply voltage

Figure. 4.2.5 Typical NPN hFE vs Ic vs VCE evaluation

BIT	[100]	[101]	[110]	[111]	[000]	[001]	[010]	[011]
VCE(V)	IB(mA)							
30	1.281	1.269	1.256	1.243	1.232	1.218	1.206	1.191
81.4	1.235	1.166	1.098	1.028	0.984	0.916	0.845	0.778
110	1.205	1.104	1.004	0.902	0.845	0.741	0.637	0.531
From 30 to 81.4 (% △)	-3.7	-8.8	-14.4	-20.9	-25.2	-32.9	-42.7	-53.1
From 81.4 to 110 (% △)	-2.4	-5.3	-8.6	-12.3	-14.1	-19.1	-24.6	-31.8

Figure. 4.2.6 R55VC selection register settings for base current

Figure 4.2.6 shows R55VC register selection range. (Address 56h[3:1])
There are 8 selection level with different V_{CE} gradient.
User should select the most suitable base current V_{CE} gradient to cancel out the NPN V_{CE} gradient measured on the bench

BIT	[100]	[101]	[110]	[111]	[000]	[001]	[010]	[011]
VCE(V)	IC(mA)							
30	118	116	114	112	110	108	106	104
81.4	119	117	112	108	106	102	96	90
110	96	86	80	74	70	67	62	56
From 30 to 81.4 (% △)	+0.8	+0.9	-1.80	-3.7	-3.8	-5.9	-10.4	-15.6
From 81.4 to 110 (% △)	-19.3	-26.5	-28.6	-31.5	-34.0	-34.3	-35.4	-37.8

Figure. 4.2.7 collector current VCE(Supply) trend after compensation

From Figure 4.2.7, we can obtain a flat collector current vs V_{CE} trend as shown by selecting [100] selection in this example.

Chapter 4 REG55 Components and Registers setting

(4) Selected register setting for selected NPN

Table 4.2.8 below shows a summary of three selected NPN and its respective R55GAIN, R55TC and R55VC register setting after bench testing.

NPN	R55GAIN 56h[9:7]	R55TC 56h[6:4]	R55VC 56h[3:1]
MJD340(Diodes)	000	001	100
MJD340(ON Semi)	011	011	000
MJD47(ON Semi)	101	011	000
DXT696BK(Diodes)	011	011	100

Table. 4.2.8 VDD55 register setting with select NPN devices

Chapter 5 Unused pins setting

5.1 Unused Cell Pins:

1) For lower cells count system, the unused battery cells pins (C3~C20) should be connected as shown in Fig 5.1.2 / 5.1.3 / 5.1.4
2) Fig.5.1.4 is an example for 4-cell solution, the cells can be added from lower to upper (C3,C4…) for the solution which need more cells.

Fig.5.1.1
Example of
20 Cell System

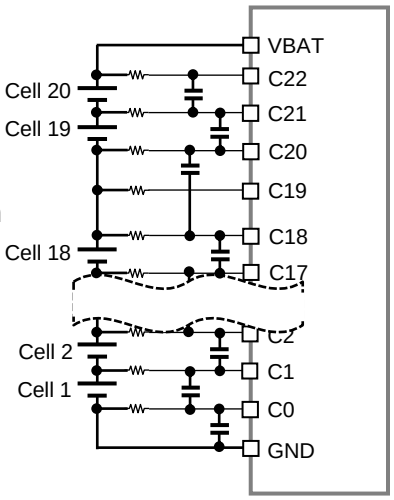


Fig.5.1.2
Example of
18 Cell System

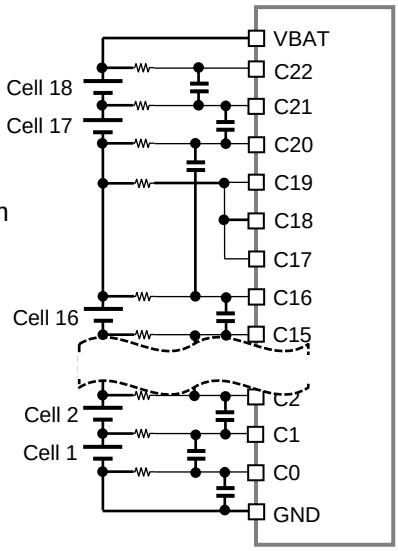


Fig.5.1.3
Example of
16 Cell System

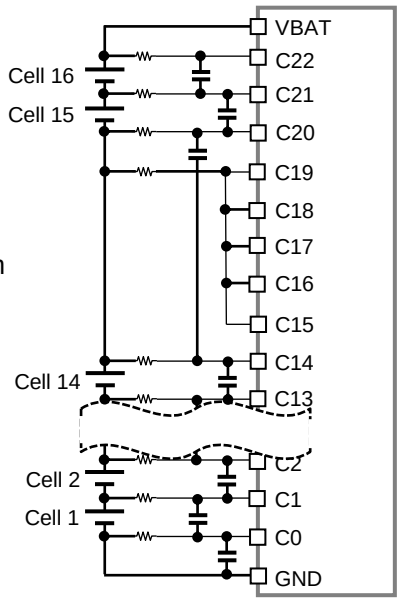
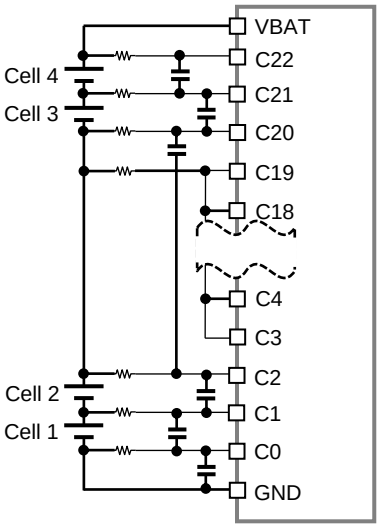


Fig.5.1.4
Example of
4 Cell System



Chapter 5 Unused pins setting

5.2 Other unused pins:

Table.5.2.1 is a list for unused function pins and its recommended connection method when not used.

Function	Pin	Connection
Temperature	TMONIn (n=1~5)	Open
Nch FET	CHG, CP2, CN2 DIS, CP1, CN1	Open
Pch FET	GPOH1,GPOH2	Open
Function pin	ALARM1	Open
	FETOFF	Ground
	SHDN	Ground
	REG_SEL	Open or Ground
	LDM	Open
MCU communication	SDO, NRST	Open
	SDI, SCL, SEN	Open
Current	SRP/SRN	Open or Ground
GPIO	GPIOn (n=1~3)	Open*1

Table.5.2.1 Connection Example for unused function pins

*1 Enabling the pull-down resistor by software is needed

Chapter 6 Battery Cell inputs connection sequence

6.1 Recommendation

Customer should strongly follow the below recommended Battery Cells connection sequence :

Connect the GND pin first, then followed by VBAT pin.

After that, connect lower cells in turn to upper cells.

GND → VBAT → Cell between C0-C1 → Cell between C1-C2 → Cell between…

6.2 Special case

If the recommended sequence can not be followed, but random connection or partial random connection sequence is required. Please use input resistors bigger than 100ohm for a fully random connection sequence.

For input resistors smaller than 100ohm, connect GND and VBAT first and than random connection for others cell voltage pin.

Note: Connection sequence for special case is verified by simulation with limited numbers of IC test, it seems no risks.

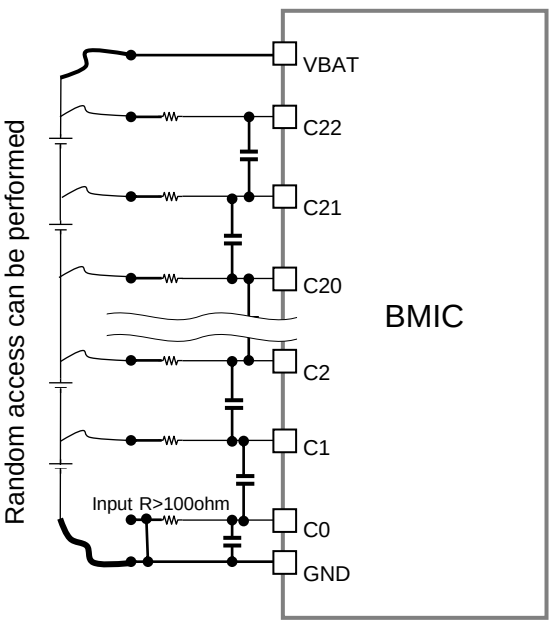


Fig. 6.2.1 Input Resistor bigger than 100ohm

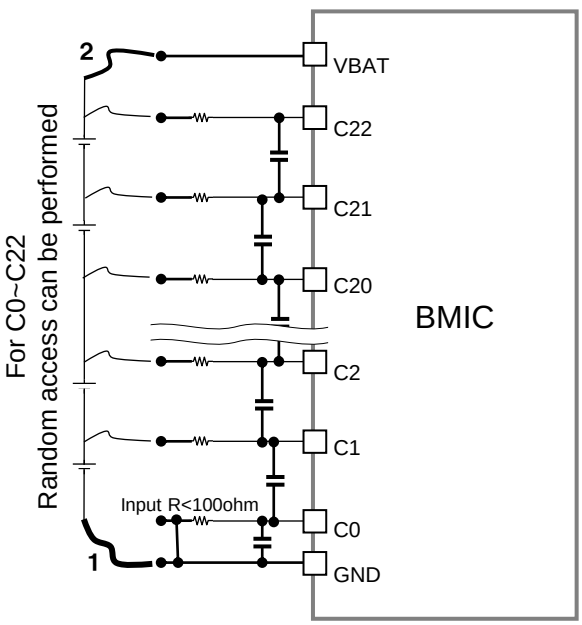


Fig. 6.2.2 Input Resistor smaller than 100ohm

Chapter 7 High-Side FET connection

7.1 Examples for high-side FET connection

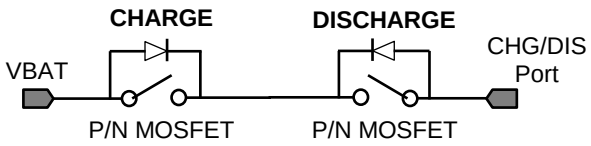


Figure 7.1.1 Single Port

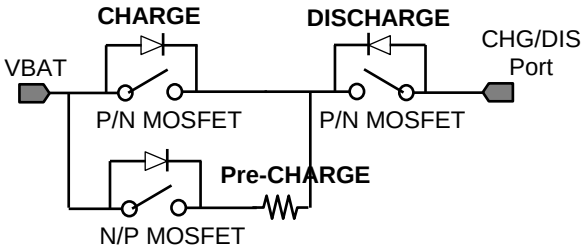


Figure 7.1.2 Single Port with Pre-charge

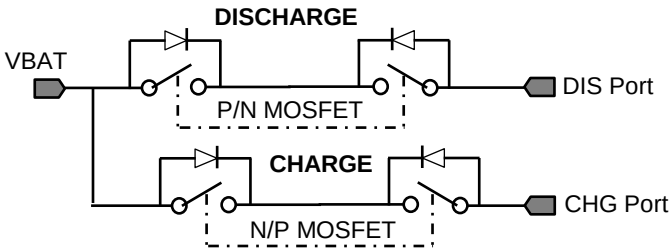


Figure 7.1.3 Separated port

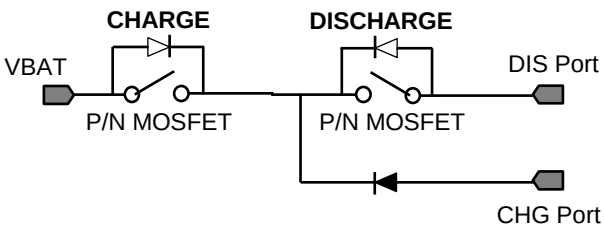


Figure 7.1.4.a Separated port (Low cost)

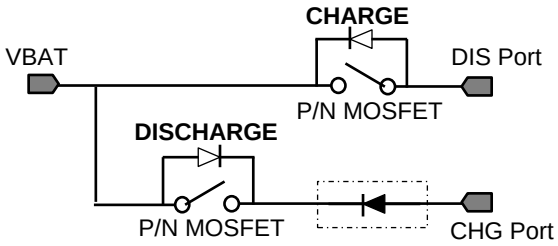


Figure 7.1.4.b Separated port (Low cost)

7.2 System example for UPS System (Use battery only at emergency)

For certain system such as UPS, the Batteries only need to be used when the external power supply failed. Open or close the FET(Power Loss) by using CHG pin, according to the monitored voltage of External Power by VPACK pin. Make sure the judgement voltage for the switching process is correctly set so that BMIC to get power from VBAT first before losing External Power. Subsequently, the FET of CHG(P) and DIS(P) can be controlled by GPOH pins.

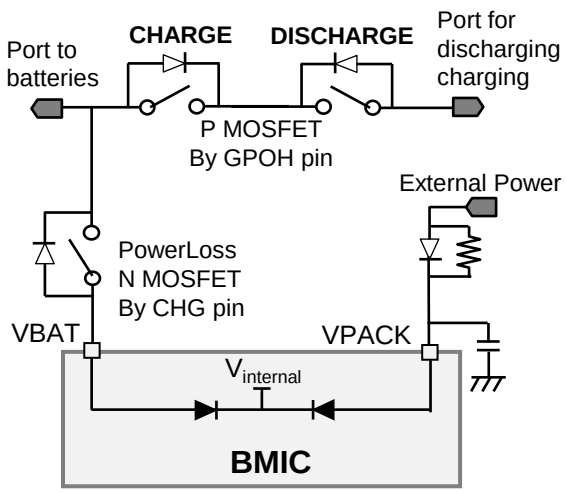


Figure 7.2.1 Switch Power by GPOH

Chapter 8 Low-Side FET connection

In case users want to use Low-Side FET system, pins GPOH1 and GPOH2 can be used together with external driver to control the FET.

The GPOH1 and GPOH2 state condition are controlled by registers setting.

The following push-pull driver is used to drive big or multiple FET for fast turning On and Off operation.

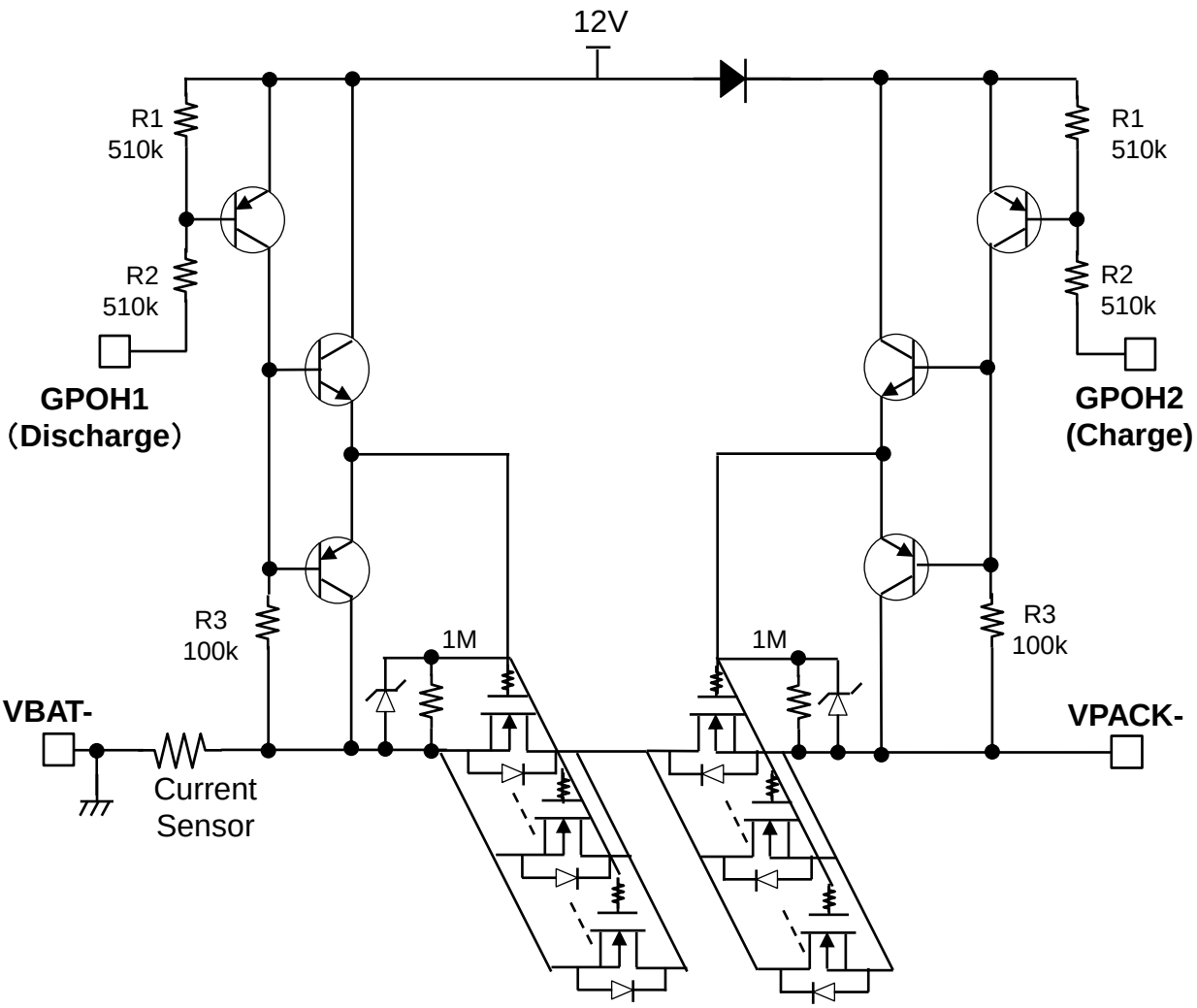
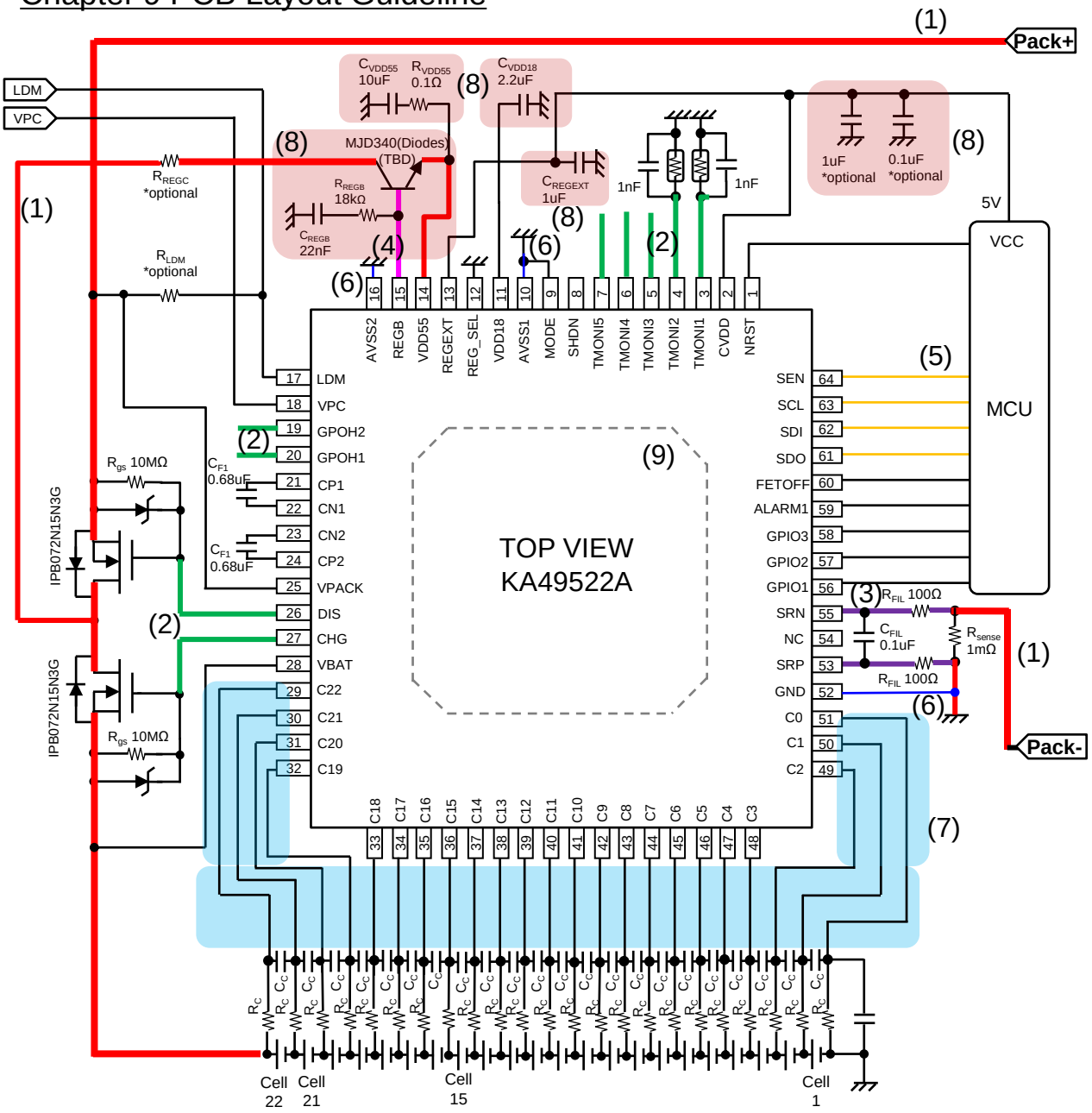


Figure 8.1.1 Low-side FET example (push pull structure)

Note 1 :
When using power MOS FET in parallel, it is recommended to insert resistor around 50-100ohm (tuned the value by evaluation) between each gate of FET.
This may reduce abnormal voltage vibration during high current on off operation.

Note 2:
Bipolar transistor hfe can affect the turn on and off speed of the Low side FETs. User can select high beta Bipolar transistors which have hfe in the range of a few hundreds, for faster switching operation.
Please note that resistor R1, R2 & R3 can be adjusted to a lower value in order to have a faster turn on and off speed. However, this will increase the total consumption current of this circuitry. User will have to adjust and decide the final suitable value to be used to suit their system requirement.

Chapter 9 PCB Layout Guideline



(1) Wide line width to be drawn based on the desired Current.

(2) Away from signals lines

(3) Differential Pair routing which have to be as short as possible and closely identical.
Route both lines on same layer as RC filter. Avoid to be parallel with high current and noisy lines.
For 1 piece Rsense case: Connect both lines directly to the center inner part of Rsense pads.
For multiple Rsense case: All Rsense must be put near together. Connect both lines to the center of this group of Rsense. Evaluate the actual measured current value, adjust the lines connection location or firmware parameter in order to get accurate current reading.

(4) Route lines as short as possible

(5) Insert capacitor if necessary, at communication lines according to your noise test
Draw all the SPI lines as short as possible and with same length to avoid propagation.
Draw all the SPI lines side by side and within the same layer.
Keep noisy lines and high voltage switching lines away from SPI lines.

(6) Connect all ground pins (AVSS1, AVSS2, GND) together and routed use copper plane under the IC

(7) Route these lines with the similar shape as much as possible since they are differential signals

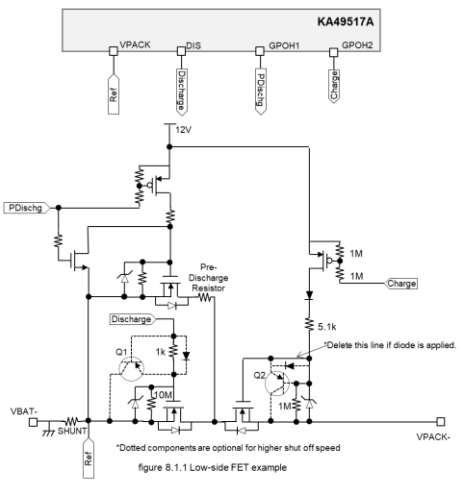
(8) Devices to be placed close to IC pin

(9) User can choose to float the bottom heat pad or connect it to GND plane for best heat dissipation

Important Notice

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board),
   it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins.
   In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.

Revision History

Control number	Revision date	Page	Item	Before revision	After revision
Ver.1.0	2021.1.28	29		Preliminary release	
Ver.1.1	2021.02.04	24		Optional CVDD cap=10uF	Optional CVDD cap=1uF
		25		Include	Remove
		26		Include	Remove
Ver.1.2	2021.03.18	12			Update VDD55 circuit Diagram. Add new BJT - DXT696BK
		13	I_C		Additional notes
		13	Thermal	$\theta_{j\text{-}PCB}$	$\theta_{j\text{-}a}$: Update to common coefficient in product spec of BJT
		14			Add new BJT - DXT696BK
		17			Add new BJT - DXT696BK
Ver.1.3	2021.06.1	4,5			Added Rg resistor in diagrams
Ver 1.4	2021.10.1	22		Chapter 8 Low-side FET connection 8.1 Examples for low-side FET connection GPIO1/2 can be used to output digital signal(0,5V) for control of FET, Relay etc. If the 5V is not enough for your FET and you do not want to implement an extra driver, The following diagram may be your solution.  figure 8.1.1 Low-side FET example Note1:Can not achieve short turn off Time for charge FET if Q2 is not applied. Note2:Charge FET may not be able fully turned on when Pre-discharge Current * Pre-discharge resistor is too large. Note3:Please check specification for turning off timing of GPOH when hardware protection is on.	Deleted, it was suggested for 1 specific customer but finally was not used.
		New 22			Updated explanation
		10			Improved Note text
		21			Improved section 7.1 drawings text Improved section 7.2 text
		18			Updated 5.1 explanation
Ver 1.5	2022.1.10	22			Added Note 2
		23			Expanded point 3
					Added point 9
Ver 2.5	2022 Dec	6		Note : Once open circuit detection is on, current (max. 80uA, typ.40uA) will be drawn though Rc. Please make sure Rc* I is smaller than On threshold of BJT.	Deleted. No more INR

Revision History

Control number	Revision date	Page	Item	Before revision	After revision
Ver.2.5	2022 JAN	14			Rectified Table 4.2.1 IB value
		15			Rectified Figure 4.2.3 value
		15			Rectified Figure 4.2.4 value
		16			Rectified Figure 4.2.6 value
		16			Rectified Figure 4.2.7 value

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.