Radio Controlled (RC) Computer Clock

The serial interface for Radio Controlled (RC) Computer Clock

1. Introduction to the serial interface for Radio Controlled (RC) Computer Clock

The serial interface consists of one data input line and one data output line.

The data traffic speed of the serial interface is 300 bps. Because of the limited resources of the RC Computer Clock micro-controller only an easy software protocol can be used.

There are no hand shake lines. Synchronising to the host is by means of the character echo.

2. Voltage supply of the serial interface

The RC Computer Clock is a battery operated RC clock which is powered by two 1.5V cells. This ensures a battery life of approximately two years. The voltage supply of the serial interface is independent of these batteries. The RS232 serial standard interface consists not only of the serial input (RxD) and output (TxD) lines but also some additional lines which are used in some applications for handshaking purposes, the RC Computer Clock uses these additional lines to supply its internal serial interface circuit with the required electrical voltage. These additional lines are not needed for data exchange.

The RC Computer Clock requires both a positive and a negative voltage out of the PC's serial interface. The positive voltage is supplied by the DTR line.

There are two ways of providing the negative voltage:

a) The PC "communicates" with the RC Computer Clock by sending ASCII characters to the RC Computer Clock as described below (see 5.). This allows the negative voltage to be provided by the TxD line. When the PC sends characters this line is toggled between a positive and negative voltage level. If the PC is waiting for the RC Computer Clock to reply the TxD line is always low at a negative voltage. The RC Computer Clock does not need the TxD negative voltage while receiving characters only while sending.

b) The RC Computer Clock can be triggered to transmit the time/date information by pulling the data input line to high voltage level as described below (see 3.3). This line must be held high until the data transmission out of the RC Computer Clock has begun. Therefore it cannot supply the negative voltage. The possibility exists to supply the negative voltage out of the RTS line. This line must be set to low level by the programmer who wants to cause the RC Computer Clock to transmit the time/date information by holding TxD at high voltage level.

3. Data word format

3.1 Data transmitted to the Radio controlled Computer Clock

Interface parameters

- Speed: 300 bps
- Data Bit Count: 7
- Parity: even, odd, mark, space (not checked by the PC Radio Clock)
- Stop Bit Count: 2

Function of data input

The RC Computer Clock accepts commands of up to three characters, including its parameters. The character carriage return (hex 0d) causes the RC Computer Clock to execute the command. Only the four lower bits of each command and parameter character are used. For instance the characters "?", "O" and "o" have the same effect. The exception is the final carriage return which is decoded by considering the seven lower bits (completely decoded).

3.2 Replies of the Radio controlled Computer Clock

Interface parameters

- Speed: 300 bps
- Data Bit Count: 7
- Parity: even
- Stop Bit Count: 2

Function of data input

The reply of the RC Computer Clock consists of a sequence of ASCII characters terminated by a final carriage return character cr. The character set used by the RC Computer Clock is limited to the numbers 0 ... 9 and the characters : ; = ?. The information is contained within the four lower bits.

The bits 4 and 5 of every reply character are binary ones, the bit 6 is binary zero and the bit 7 contains the even parity bit. This results in the sixteen different characters transmitted by the RC Computer Clock, as described above. the serial output of the RC Computer Clock can not be interrupted during its reply. Therefore all characters must be taken by the host computer immediately.

3.3 Support of a simplified data exchange

A simplified data exchange is possible.

The time/date information transmit command ((o cr) see below 5 .1.) is not the only way to initiate a sequence of ASCII characters. A simpler method is to pull the TxD (TxD of the PC) voltage level high. Normally TxD voltage level is low (inactive). If the TxD line is high at the start of a second then the RC Computer Clock will transmit its time/date information. This can takes up to one second because the first start bit of the time/date information sets the beginning of a second. If the TxD line is held high continually then the RC Computer Clock will transmit the time date information every second. But care must be taken: The current consumption of the RC Computer Clock increases during the time/date information output (duration approximately. 600 ms) up to 200 �A.

4. Handshaking

Every character received by the RC Computer Clock is echoed. The next character must not be transmitted to the RC Computer Clock before the echo of the preceding character and an additional duration of 10 ms.

Recognising input characters is by checking the correct appearance both of the start bit and the two stop bits. The eight echoed data bits remain unchanged under all circumstances, regardless whether or not parity is even or odd.

5. Description of commands

5.1 Transmit time/date information

syntax ASCII: o cr Character "o" may be replaced if necessary by a character whose code contains the lowest four bits f(hex), e.g. also / ? O _

syntax binary: xxxx1111 00001101

The RC Computer Clock replies to this command with a sequence of 15 characters which contain the complete time information and a final cr. Making 16 characters in total.

The RC Computer Clock will not reply immediately to this command because the start bit edge of the first reply character marks the beginning of the second. So the RC Computer Clock will reply to this command at the start of the next second.

The characters have the following meaning:

- 1. hours tens
- 2. hours units
- 3. minutes tens
- 4. minutes units

- 5. seconds tens
- 6. seconds units
- 7. day of week 1 (Monday) ... 7 (Sunday)
- 8. day of month tens
- 9. day of month units
- 10. month tens
- 11. month units
- 12. year tens
- 13. year units
- 14. BST/UTC status
- bit7 parity
- bit6 always 0
- bit5 always 1
- bit4 always 1
- bit3 always 0
- bit2 =1 if UTC is in effect, complementary to the BST bit
- bit1 =1 if BST is in effect, according to the BST bit
- bit0 BST/UTC change impending bit =1 in case of change impending
- 15. status
- bit7 parity
- bit6 always 0
- bit5 always 1
- bit4 always 1
- bit3 =1 if low battery voltage is detected
- bit2 =1 if the very last reception attempt failed and a valid time information already exists (bit0 = 1)
- bit2 =0 if the very last reception attempt was successful
- bit1 =1 if at least one reception attempt since 2:30 am was successful
- bit1 =0 if no reception attempt since 2:30 am was successful
- bit0 =1 if the RC Computer Clock contains a valid time information
- This bit is zero after reset and one after the first successful reception attempt.

5.2 Transmit reception status

syntax ASCII: g cr

Character "g" may be replaced by a character whose code contains the lowest four bits 7, e.g. also ' 7 G W w

syntax binary: xxxx0111 00001101

The reply to this command consists of two characters and the final cr.

The characters have the following meaning:

1. Status of reception and line

- bit7 parity
- bit6 always 0
- bit5 always 1
- bit4 always 1
- bit3 always 0
- bit2 always 0
- bit1 always 1
- bit0 =0 if no reception attempt takes place at the moment
- bit0 =1 if a reception attempt takes place at the moment

2. reception quality characterising number from 0 to 5

- 5 indicates a good reception without any disturbances
- 0 indicates very poor reception conditions

If the number is in the range from 0 to 2 no successful reception is to be expected normally.

During reception pauses this number is always 0.

5.3 Start reception attempt including time comparison

syntax ASCII: h cr

Character "h" may be replaced any other characters whose code contains the lowest four bits 8, e.g. also (8 H X x syntax binary: xxxx1000 00001101

This command causes the RC Computer Clock to activate the receiver IC and to start a reception attempt which includes input of the complete MSF time information and synchronising the RC Computer Clocks internal time according to the MSF second pulses. The accuracy is better than 20 ms. If this attempt ends unsuccessfully from 2:00 am to 3:00 am bit 1 of the 15th time/date information character will be reset (see 5.1.). This bit is always set after ending the reception attempt successfully.

5.4 Start reception attempt without time comparison

syntax ASCII: i cr

Character "i" may be replaced by all other characters which code contains the lowest four bits 9, e.g. also) 9 I Y y syntax binary: xxxx1001 00001101

This command causes the RC Computer Clock to activate the receiver IC and to start a reception attempt. Only the internal seconds timing will be synchronised according to the MSF seconds pulses. The accuracy is better than 20 ms. Setting of status bits is in accordance to 5.3.

Attention: If the preceding reception attempt was unsuccessful or if this command appears from 12:00 am to 3:00 am it will cause a reception attempt which includes complete time comparison (see 5.3.)