Super Quick Architecture Review
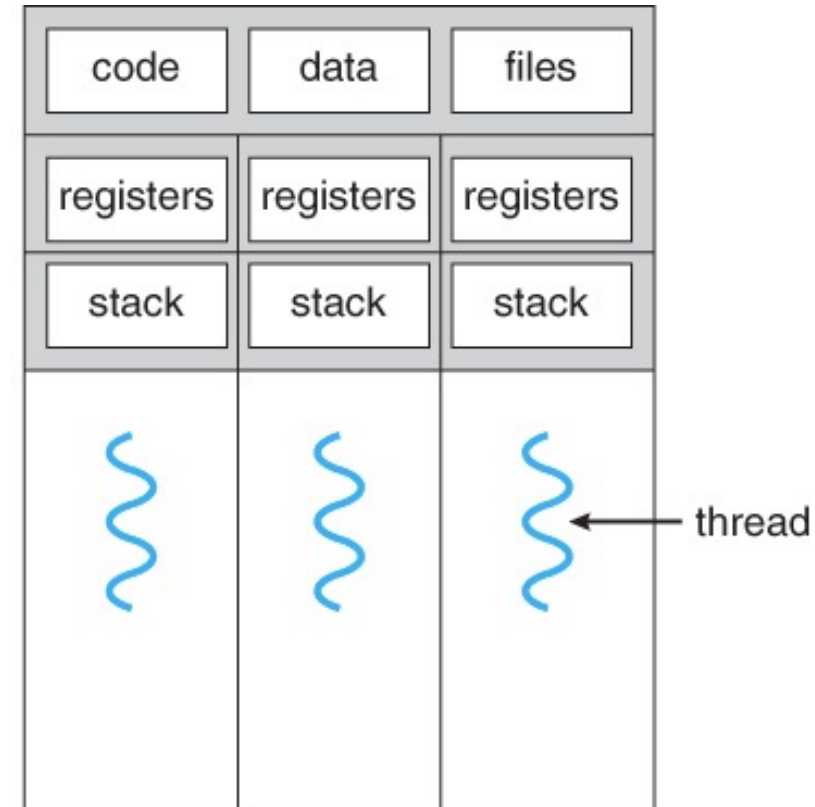
Software-Hardware stack

Credit:: Mark Redekopp, USC
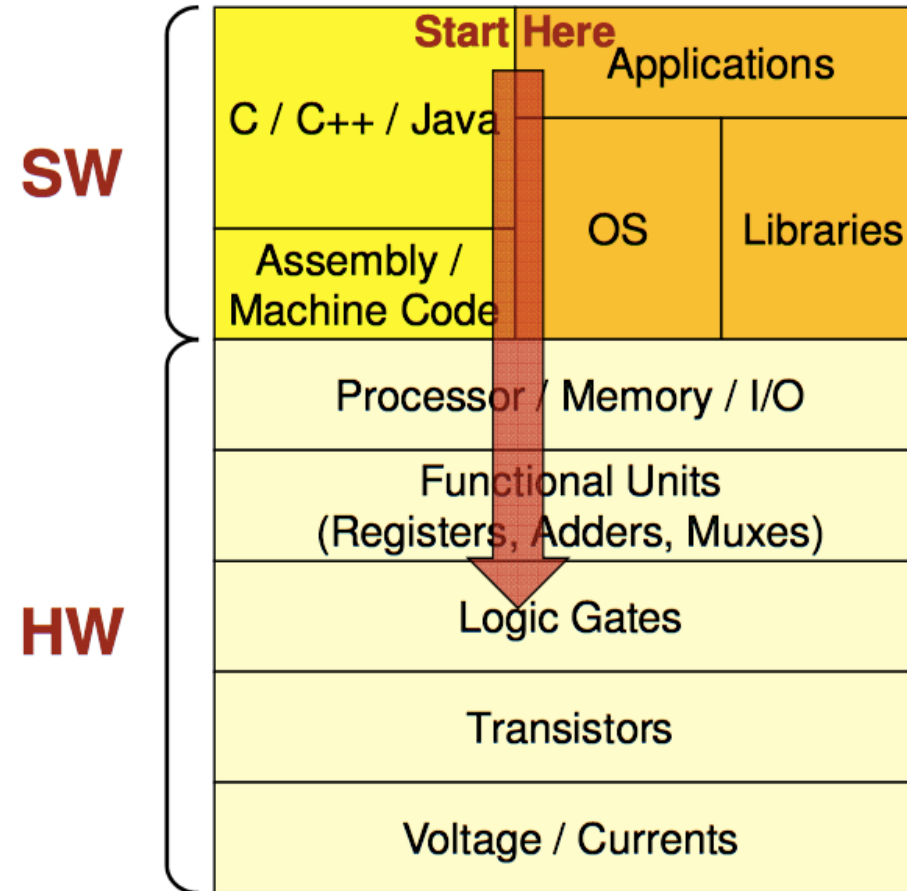
Process vs Thread
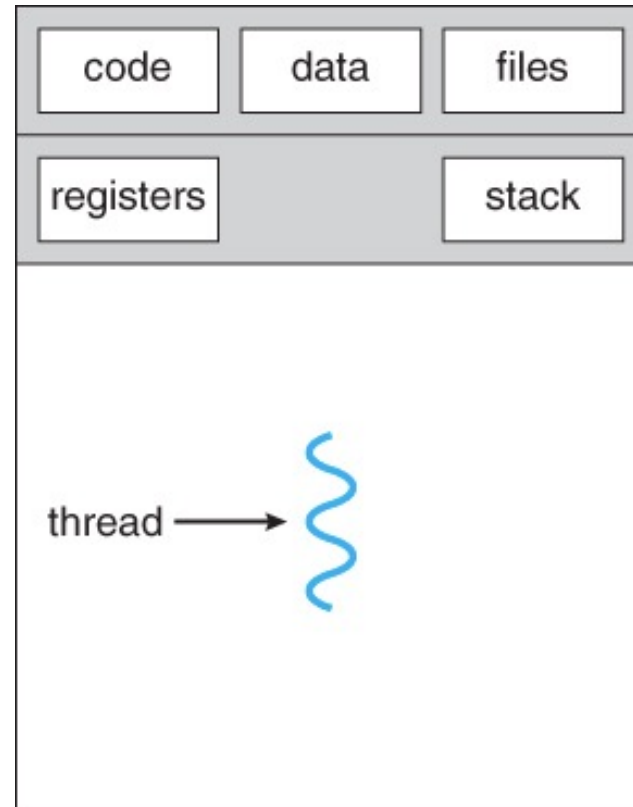
single-threaded process

multithreaded process

ISA example - MIPS R-format Instructions

op	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

- Instruction fields
  - op: operation code (opcode)
  - rs: first source register number
  - rt: second source register number
  - rd: destination register number
  - shamt: shift amount (00000 for now)
  - funct: function code (extends opcode)
- Used only for ALU instructions

R-format Example

op	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

add $r8, $r17, $r18

special	$r17	$r18	$r8	0	add

0	17	18	8	0	32

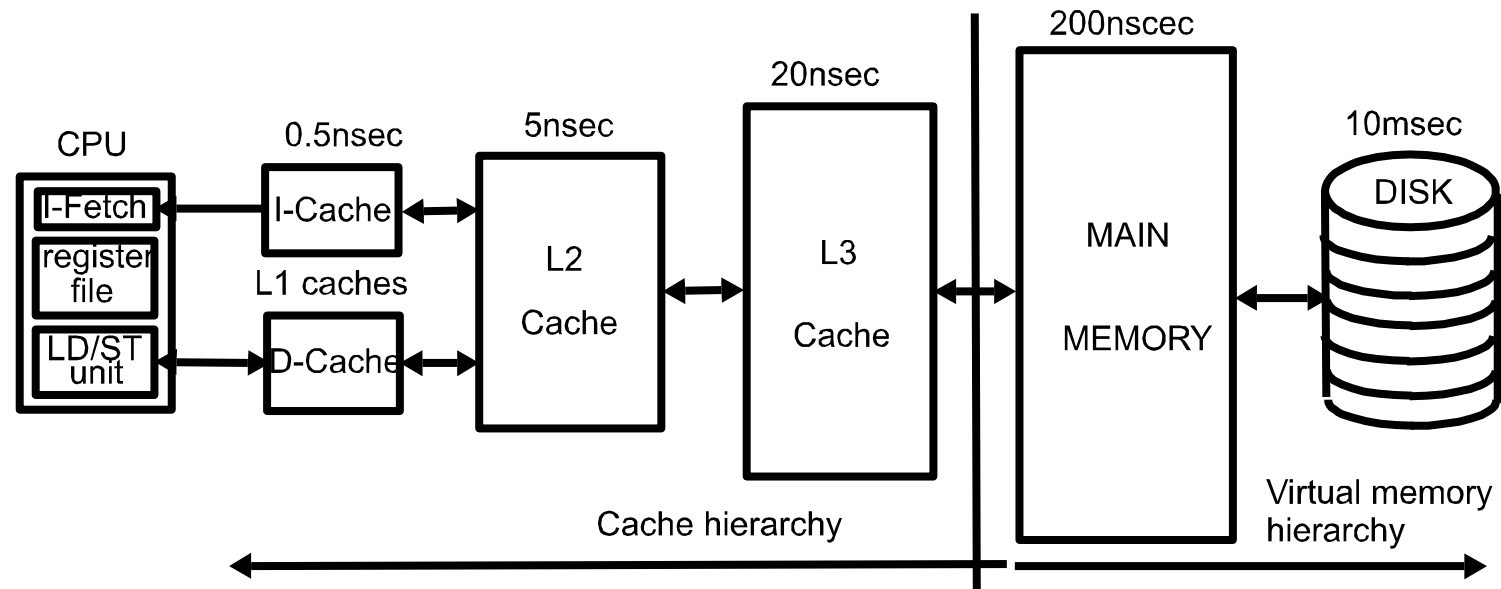| 000000	10001	10010	01000	00000	100000

$$00000010001100100100000000100000_2 = 02324020_{16}$$

5-stage pipeline
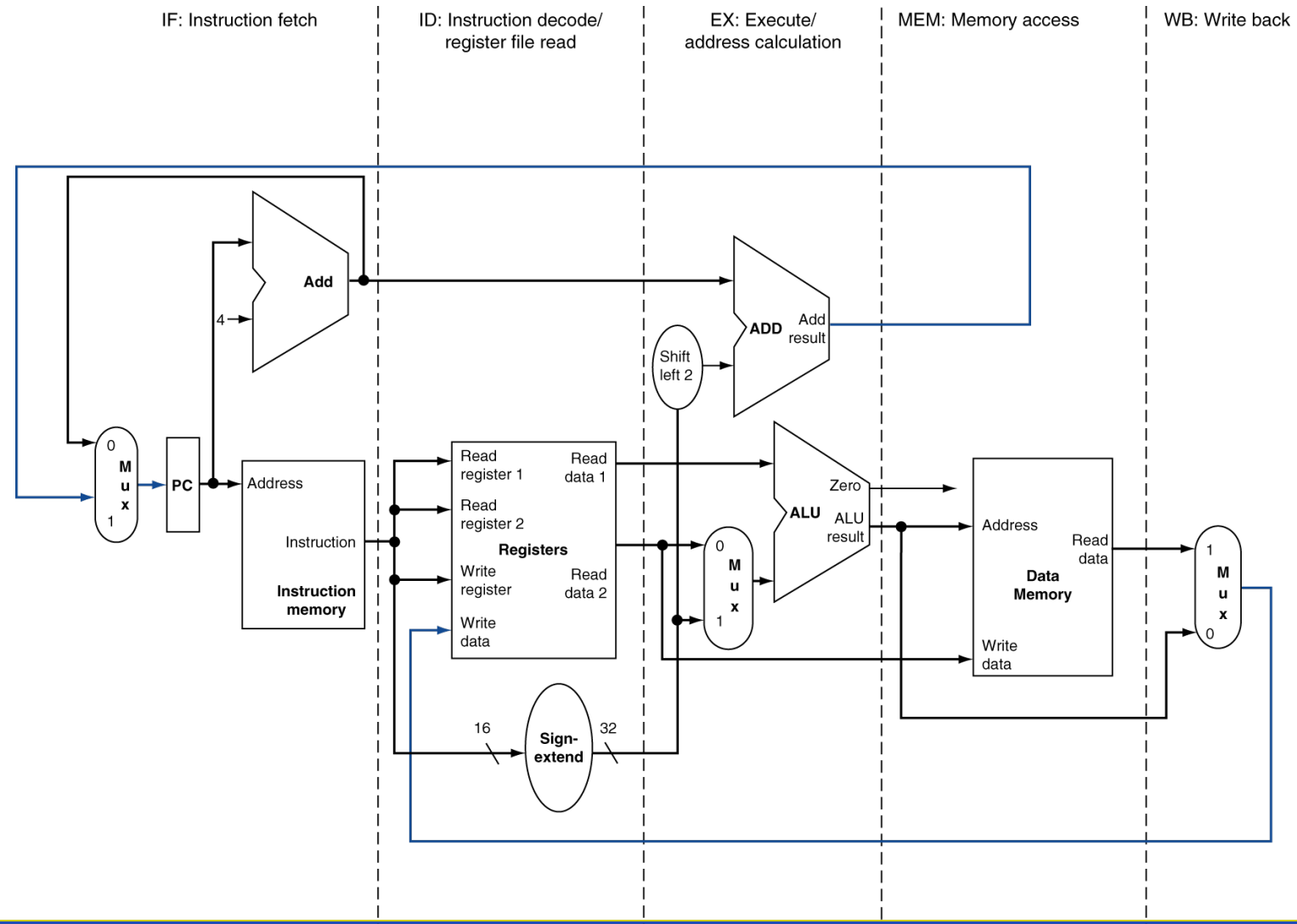
Abstracted CPU
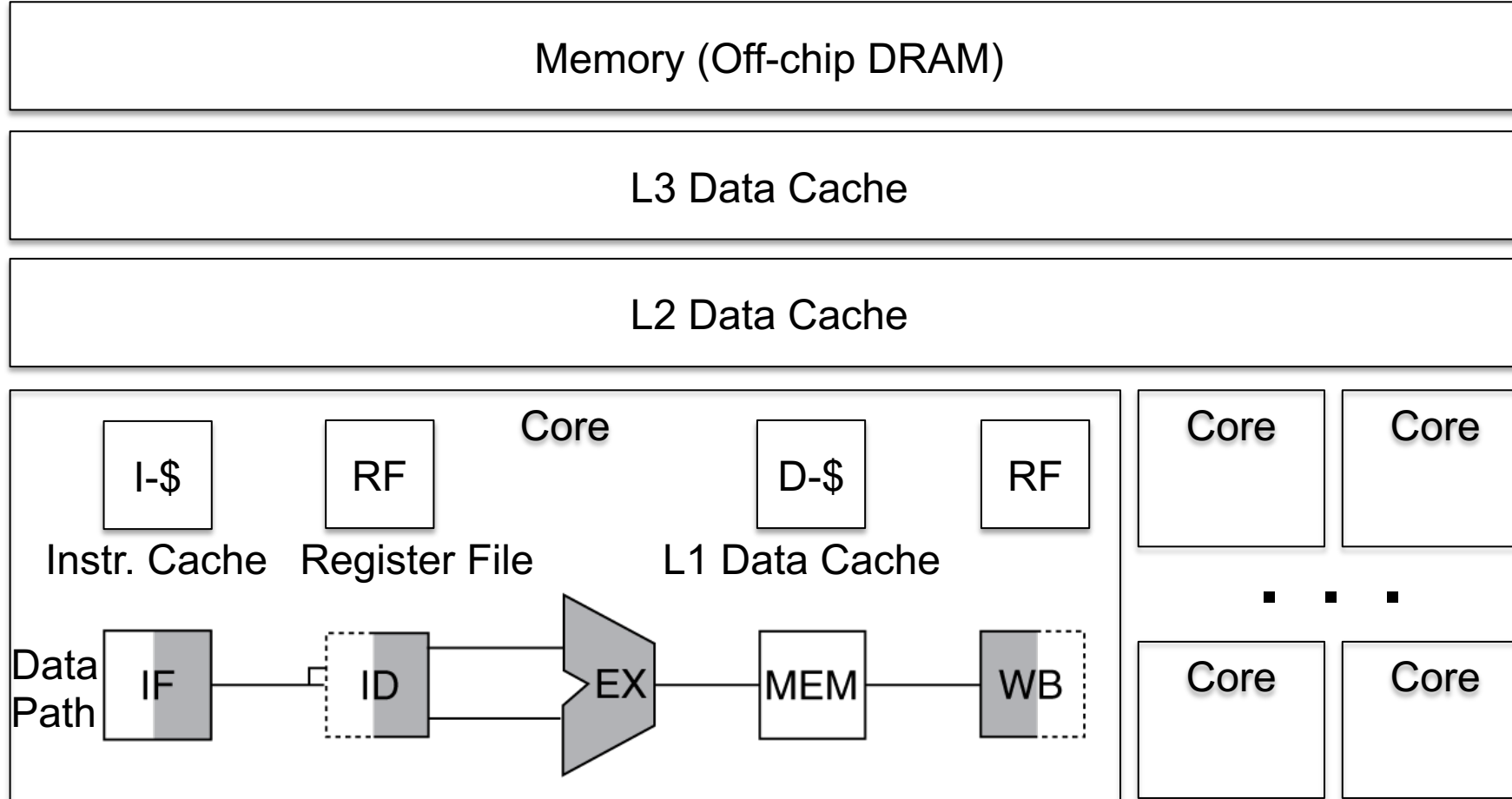
Memory Hierarchy

Virtual Memory

> Divide memory into equal sized "chunks" or pages (typically 4KB each)

> Any chunk of Virtual Memory can be assigned to any chunk of Physical Memory

Physical Memory

1GB

0

Virtual Memory

∞^{*}

Stack

Heap

Static

Code

0

Page Table

*256TB
(2^{48} B)

Single Process