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| Bertrand A. Maher  Curriculum Vitae | 20 Descanso Dr. Apt. 1233  San Jose, CA 95134  Phone: 214-226-7019  Email: [bertmaher@gmail.com](mailto:bertmaher@gmail.com)  http://www.cs.utexas.edu/users/bmaher/ |

Research Interests

I am interested in the problem of programming parallel machines. My interests include the language and compilation technology that allow a programmer to write correct concurrent programs, and the underlying architecture that supports efficient parallel execution.

Education

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| 9/2004–9/2010 | **University of Texas at Austin**  Ph.D. in Computer Science  Dissertation title: *Atomic Block Formation for Explicit Data Graph Execution Architectures*  Advisors: Doug Burger and Kathryn McKinley |
| 9/2004–5/2007 | **University of Texas at Austin**  M.S. in Computer Sciences. GPA: 3.93. |
| 9/2000–5/2004 | **Yale University**  B.S. in Electrical Engineering and Computer Science magna cum laude, with distinction in the major. GPA: 3.83. |

Honors

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| 3/2009 | Best Paper Award at ASPLOS-XIV for “An Evaluation of the TRIPS Computer System” |
| 9/2004 | Microelectronics and Computer Development (MCD) Fellowship |
| 9/2004 | Dean’s Excellence Award, College of Natural Sciences, UT Austin |
| 1/2004 | Elected to Tau Beta Pi Engineering Honors Society |
| 9/2002 | Society of American Military Engineers Scholarship |
| 5/2000 | National Merit Scholar |
| 5/2000 | United States Presidential Scholar Semifinalist |

Work Experience

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| 10/2010–present | **Software engineer, Intel Corp.**  Worked on hardware-software techniques for x86 binary translation. Designed and implemented optimizations and new functionality for the virtual machine, including the translator and runtime systems. Co-developed hardware features with a team of microarchitects. Carried out extensive power/performance analysis and tuning. |
| 6/2009–9/2009 | **Software engineering intern, Sun Microsystems Labs**  Developed part of a JIT compiler for dynamically translating x86 machine code to a different, native instruction set architecture. Researched testing techniques and developed a framework for assuring coverage of ISA corner cases. |
| 6/2008–9/2008 | **Software engineering intern, Intel Corp.**  Developed tools for Pin, a dynamic binary instrumentation system, for findingdifferences between executions of programs with nondeterministic behavior, and for finding implementation differences between simulation tools and hardware. |
| 6/1999–9/2004 (summers) | **Software developer, Innovative Managed Care Systems, Ltd.**  Worked during summers as a software developer, designing data acquisition soft- ware using Perl and web applications for modeling insurance contract changes using Visual Basic. |

Research Experience

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| 9/2004–9/2010 | **Research assistant, UT-Austin.**  Advisors: Doug Burger and Kathryn McKinley Researched compilation techniques for the TRIPS prototype processor. Implemented convergent hyperblock formation, which resolves phase ordering problems among hyperblock formation, loop unrolling, and scalar optimizations by iteratively growing and optimizing hyperblocks. |
| 9/2003–5/2004 | **Senior thesis, Yale University.**  Advisor: Brian Scassellati Designed, built, and programmed a microcontroller-based device to test the listening preferences of autistic children, in collaboration with faculty at the Yale Child Studies Center. |

Teaching Experience

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| 1/2008–5/2009 | **Teaching assistant, UT-Austin.**  Led discussion sections of 20-30 students and prepared and graded homework assignments for an introductory computer architecture and assembly language class. |
| 9/2002–12/2002 | **Teaching assistant, Yale University.**  Helped lead a sophomore level circuits laboratory of 20-30 students. |

Professional Service

**Program Committee Member**, International Symposium on Code Generation and Optimization (CGO), 2012.

**Reviewer**, ACM Transactions on Architecture and Code Optimization (TACO), 2012.

**Student member**, UTCS Faculty Recruiting Committee, Spring 2008.

**Representative**, Graduate Representative Association of Computer Sciences, 9/2005–5/2006.

**Reviewer**, IEEE International Symposium on Workload Characterization (IISWC) 2006.

Conference Publications

1. M. Gebhart, **B.A. Maher**, K.E. Coons, J. Diamond, P. Gratz, M. Marino, N. Ranganathan, B. Robatmili, A. Smith, J. Burrill, S.W. Keckler, D. Burger, K.S. McKinley. “An Evaluation of the TRIPS Computer System,”14th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March, 2009. **Best Paper Award.**
2. K.E. Coons, B. Robatmili, M.E. Taylor, **B.A. Maher**, D. Burger, K.S. McKinley. “Feature selection and policy optimization for distributed instruction placement using reinforcementlearning,”17th International Conferenceon Parallel Architectures and Compilation Techniques (PACT), October, 2008.
3. **B.A. Maher**, A. Smith, D.C. Burger, and K.S. McKinley. “Merging Head and Tail Duplication for Convergent Hyperblock Formation,” 39th International Symposium on Microarchitecture (MICRO), December, 2006.
4. A. Smith, J. Burrill, J. Gibson, **B.A. Maher**, B. Yoder, D. Burger, and K.S. McKinley. “Compiling for EDGE Architectures,” 4th International Symposium on Code Generation and Optimization (CGO), March, 2006.

Workshop Publications

1. **B.A. Maher**, K.E. Coons, K.S. McKinley, D. Burger. “The Good Block: Hardware/Software Design for Composable, Block-Atomic Processors,” 2011 Workshop on Interaction Between Compilers and Computer Architectures (INTERACT), February, 2011.
2. B. Yoder, J. Burrill, R. McDonald, K. Bush, K. Coons, M. Gebhart, S. Govindan, **B.A. Maher**, R. Nagarajan, B. Robatmili, K. Sankaralingam, S. Sharif, A. Smith, D. Burger, S.W. Keckler, and K.S. McKinley. “Software Infrastructure and Tools for the TRIPS Prototype,” 3rd Annual Workshop on Modeling, Benchmarking and Simulation (MoBS), June, 2007.
3. K. Bush, M. Gebhart, E. Wei, N. Yudin, **B.A. Maher**, N. Nethercote, D. Burger, and S.W. Keckler. “Evaluation and Optimization of Signal Processing Kernels on the TRIPS Architec- ture,”Proceedings of the Annual Workshop on Optimizations for DSP and Embedded Systems (ODES), March, 2006.

References

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| **Doug Burger**  Professor  University of Texas at Austin [dburger@cs.utexas.edu](mailto:dburger@cs.utexas.edu)  1 University Station C0500  Austin, TX 78712  512-471-9795 | **Kathryn S. McKinley**  Professor  University of Texas at Austin [mckinley@cs.utexas.edu](mailto:mckinley@cs.utexas.edu)  1 University Station C0500 Austin, TX 78712  512-232-7467 | **Stephen W. Keckler**  Professor  University of Texas at Austin [skeckler@cs.utexas.edu](mailto:skeckler@cs.utexas.edu)  1 University Station C0500 Austin, TX 78712  512-471-9763 |