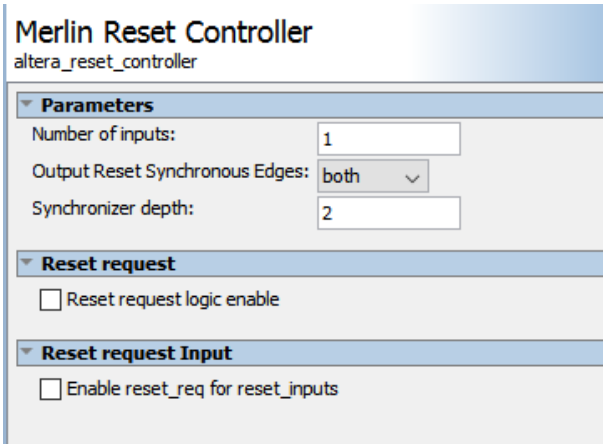
ECE 423 Lab 1 Reset Fix

In the provided prefab Qsys design, we used the input of the reset pushbutton to reset the system. However, there was a synchronization problem that caused instability when resetting the system. To fix this, you need to do these changes to your Qsys System:

1- Add **Reset Controller** component (*reset_controller_0*) to your design with the following parameters:



2- Disconnect (*clk_reset*) output of clock (*clk_125*) from all the reset connections in the system.
3- Connect (*clk_reset*) output of the clock (*clk_125*) to (*reset_in0*) input of (*reset_controller_0*).
4- Connect (*reset_out*) output of (reset_controller_0) to all the resets in the system except (*global_reset*) of (*lpddr2*).
5- Export (*global_reset*) of (*lpddr2*) as (*lpddr2_global_reset*).
6- A screenshot of the system after the modifications is provided in the next page.
7- In the top level file of the system (*ECE423_C5G.v*), add the following connection to (*lpddr2_global_reset*) in (ECE423_QSYS u0) component:

```
ECE423_QSYS u0 (
  .clk_125_clk                          (CLOCK_125_p),
  .clk_50_clk                           (CLOCK_50_B7A),
  .reset_reset_n                        (CPU_RESET_n),

  .lpddr2_mem_ca                        (DDR2LP_CA),
  .lpddr2_mem_ck                        (DDR2LP_CK_p),
  .lpddr2_mem_ck_n                      (DDR2LP_CK_n),
  .lpddr2_mem_cke                       (DDR2LP_CKE),
  .lpddr2_mem_cs_n                      (DDR2LP_CS_n),
  .lpddr2_mem_dm                        (DDR2LP_DM),
  .lpddr2_mem_dq                        (DDR2LP_DQ),
  .lpddr2_mem_dqs                       (DDR2LP_DQS_p),
  .lpddr2_mem_dqs_n                     (DDR2LP_DQS_n),
  .lpddr2_oct_rzqin                     (DDR2LP_OCT_RZQ),

  .lpddr2_pll_ref_clk_clk               (CLOCK_50_B5B),
  .lpddr2_status_local_init_done        (lpddr2_local_init_done),
  .lpddr2_status_local_cal_success      (lpddr2_local_cal_success),
  .lpddr2_status_local_cal_fail         (lpddr2_local_cal_fail),
  .lpddr2_global_reset_reset_n          (1'b1),
```

Qsys - ECE423_QSYS.qsys (C:\CycloneV\VMFiles\ECE423_C5G_Lab1\ECE423_QSYS.qsys)

File Edit System Generate View Tools Help

System Contents | Address Map | Interconnect Requirements

System: ECE423_QSYS **Path:** reset_controller_0.reset_out

Use	Connections	Name	Description	Export	Clock	Base	End	IRQ
☑		**clk_125**	Clock Source					
		clk_in	Clock Input	**clk_125**	***exported***			
		clk_in_reset	Reset Input	**reset**				
		clk	Clock Output	*Double-click to export*	clk_125			
		clk_reset	Reset Output	*Double-click to export*				
☑		**reset_controller_0**	Merlin Reset Controller					
		reset_in0	Reset Input	*Double-click to export*				
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset_out	Reset Output	*Double-click to export*	[clk]			
☑		**clk_50**	Clock Bridge					
		in_clk	Clock Input	**clk_50**	***exported***			
		out_clk	Clock Output	*Double-click to export*	clk_50_out_clk			
☑		**cpu**	Nios II Processor					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		data_master	Avalon Memory Mapped Master	*Double-click to export*	[clk]			
		instruction_master	Avalon Memory Mapped Master	*Double-click to export*	[clk]			
		irq	Interrupt Receiver	*Double-click to export*	[clk]		IRQ 0	IRQ 31
		debug_reset_request	Reset Output	*Double-click to export*	[clk]			
		debug_mem_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_0800	0x2010_0fff	
		custom_instruction_m...	Custom Instruction Master	*Double-click to export*				
☑		**sysid**	System ID Peripheral					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		control_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_1500	0x2010_1507	
☑		**timer_1**	Interval Timer					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_1400	0x2010_143f	
		irq	Interrupt Sender	*Double-click to export*	[clk]			
☑		**timer_0**	Interval Timer					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_14a0	0x2010_14bf	
		irq	Interrupt Sender	*Double-click to export*	[clk]			
☑		**jtag_uart**	JTAG UART					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		avalon_jtag_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_1508	0x2010_150f	
		irq	Interrupt Sender	*Double-click to export*	[clk]			
☑		**lpddr2**	LPDDR2 SDRAM Controller with UniPHY					
		pll_ref_clk	Clock Input	**lpddr2_pll_ref_clk**	***exported***			
		global_reset	Reset Input	**lpddr2_global_reset**				
		soft_reset	Reset Input	*Double-click to export*				
		afi_clk	Clock Output	*Double-click to export*	lpddr2_afi_clk			
		afi_half_clk	Clock Output	*Double-click to export*	lpddr2_afi_h...			
		afi_reset	Reset Output	*Double-click to export*				
		afi_reset_export	Reset Output	*Double-click to export*				
		memory	Conduit	**lpddr2**				
		avl_0	Avalon Memory Mapped Slave	*Double-click to export*	[mp_cmd_cl...	0x0000_0000	0x1fff_ffff	
		avl_1	Avalon Memory Mapped Slave	*Double-click to export*	[mp_cmd_cl...	0x0000_0000	0x1fff_ffff	
		mp_cmd_clk_0	Clock Input	*Double-click to export*	**clk_125**			
		mp_cmd_reset_n_0	Reset Input	*Double-click to export*				
		mp_cmd_clk_1	Clock Input	*Double-click to export*	**clk_125**			
		mp_cmd_reset_n_1	Reset Input	*Double-click to export*				
		mp_rfifo_clk_0	Clock Input	*Double-click to export*	**clk_125**			
		mp_rfifo_reset_n_0	Reset Input	*Double-click to export*				
		mp_wfifo_clk_0	Clock Input	*Double-click to export*	**clk_125**			
		mp_wfifo_reset_n_0	Reset Input	*Double-click to export*				
		mp_rfifo_clk_1	Clock Input	*Double-click to export*	**clk_125**			
		mp_rfifo_reset_n_1	Reset Input	*Double-click to export*				
		status	Conduit	**lpddr2_status**				
		oct	Conduit	**lpddr2_oct**				
		pll_sharing	Conduit	**lpddr2_pll_sharing**				
☑		**key**	PIO (Parallel I/O)					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_14f0	0x2010_14ff	
		external_connection	Conduit	**key**				
		irq	Interrupt Sender	*Double-click to export*	[clk]			
☑		**sram**	Generic Tri-State Controller					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		uas	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2008_0000	0x200f_ffff	
		tcm	Tristate Conduit Master	*Double-click to export*	[clk]			
☑		**sram_sharer**	Tri-State Conduit Pin Sharer					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		tcm	Tristate Conduit Master	*Double-click to export*	[clk]			
		tcs0	Tristate Conduit Slave	*Double-click to export*	[clk]			
☑		**sram_bridge**	Tri-State Conduit Bridge					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		tcs	Tristate Conduit Slave	*Double-click to export*	[clk]			
		out	Conduit	**sram_bridge_out**				
☑		**ledr**	PIO (Parallel I/O)					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_1460	0x2010_147f	
		external_connection	Conduit	**ledr**				
☑		**ledg**	PIO (Parallel I/O)					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_1480	0x2010_149f	
		external_connection	Conduit	**ledg**				
☑		**video_pll**	Altera PLL					
		refclk	Clock Input	*Double-click to export*	**clk_50_out...**			
		reset	Reset Input	*Double-click to export*				
		outclk0	Clock Output	*Double-click to export*	video_pll_ou...			
☑		**video_clk**	Clock Bridge					
		in_clk	Clock Input	*Double-click to export*	**video_pll_...**			
		out_clk	Clock Output	**video_clk**	video_clk_o...			
☑		**video_dma**	Modular Scatter-Gather DMA					
		mm_read	Avalon Memory Mapped Master	*Double-click to export*	[clock]			
		clock	Clock Input	*Double-click to export*	**clk_125**			
		reset_n	Reset Input	*Double-click to export*	[clock]			
		csr	Avalon Memory Mapped Slave	*Double-click to export*	[clock]	0x2010_1440	0x2010_145f	
		descriptor_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clock]	0x2010_14e0	0x2010_14ef	
		csr_irq	Interrupt Sender	*Double-click to export*	[clock]			
		st_source	Avalon Streaming Source	*Double-click to export*	[clock]			
☑		**video_fifo**	Avalon FIFO Memory					
		clk_in	Clock Input	*Double-click to export*	**clk_125**			
		reset_in	Reset Input	*Double-click to export*	[clk_in]			
		clk_out	Clock Input	*Double-click to export*	**video_pll_...**			
		reset_out	Reset Input	*Double-click to export*	[clk_out]			
		in	Avalon Streaming Sink	*Double-click to export*	[clk_in]			
		out	Avalon Streaming Source	*Double-click to export*	[clk_out]			
☑		**Pixel_Conv**	Pixel Converter					
		clk	Clock Input	*Double-click to export*	**video_pll_...**			
		clk_reset	Reset Input	*Double-click to export*	[clk]			
		in	Avalon Streaming Sink	*Double-click to export*	[clk]			
		out	Avalon Streaming Source	*Double-click to export*	[clk]			
☑		**video**	Video Sync Generator					
		clk	Clock Input	*Double-click to export*	**video_pll_...**			
		clk_reset	Reset Input	*Double-click to export*	[clk]			
		in	Avalon Streaming Sink	*Double-click to export*	[clk]			
		sync	Conduit	**video**				
☑		**i2c_scl**	PIO (Parallel I/O)					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_14d0	0x2010_14df	
		external_connection	Conduit	**i2c_scl**				
☑		**i2c_sda**	PIO (Parallel I/O)					
		clk	Clock Input	*Double-click to export*	**clk_125**			
		reset	Reset Input	*Double-click to export*	[clk]			
		s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]	0x2010_14c0	0x2010_14cf	
		external_connection	Conduit	**i2c_sda**				
☑		**sd_cont**	SD Controller					
		clock	Clock Input	*Double-click to export*	**clk_50_out...**			
		reset	Reset Input	*Double-click to export*	[clock]			
		slave	Avalon Memory Mapped Slave	*Double-click to export*	[clock]	0x2010_1000	0x2010_13ff	
		master	Avalon Memory Mapped Master	*Double-click to export*	[clock]			
		sd	Conduit	**sd**	[clock]			
		sd_clk	Clock Input	*Double-click to export*	**clk_50_out...**			

Current filter:

0 Errors, 5 Warnings

Generate HDL... Finish