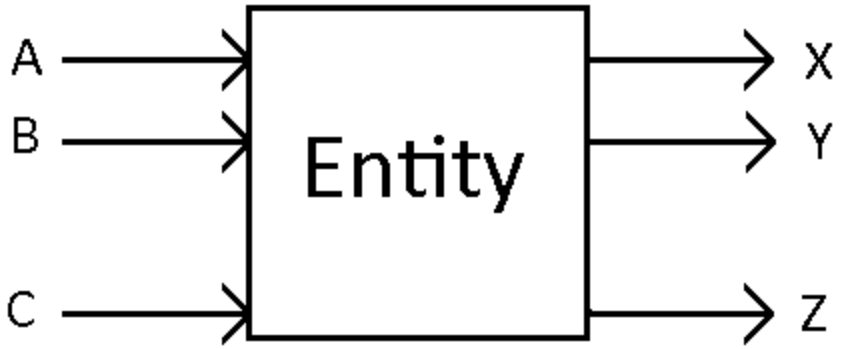
VHDL: V Hardware Description Language

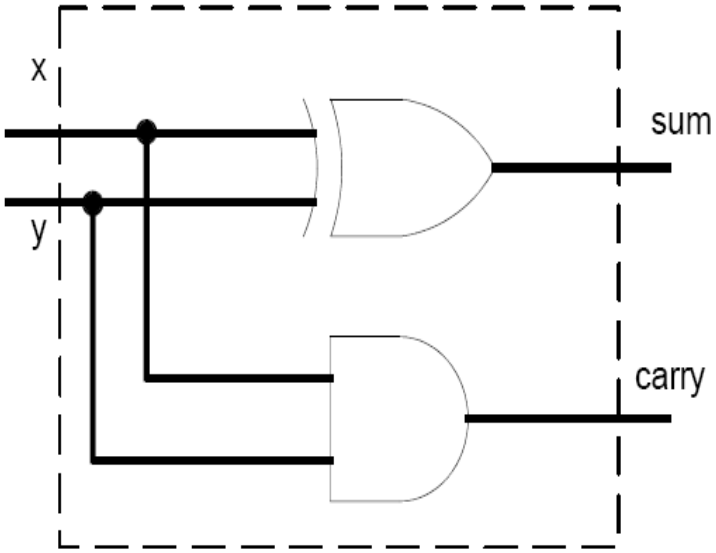
VHSIC: Very High Speed Integrated Circuit

Two main statements: Entity & Architecture

Entity	Declares ports (interface to outside world)
Architecture	Describes connections inside the entity



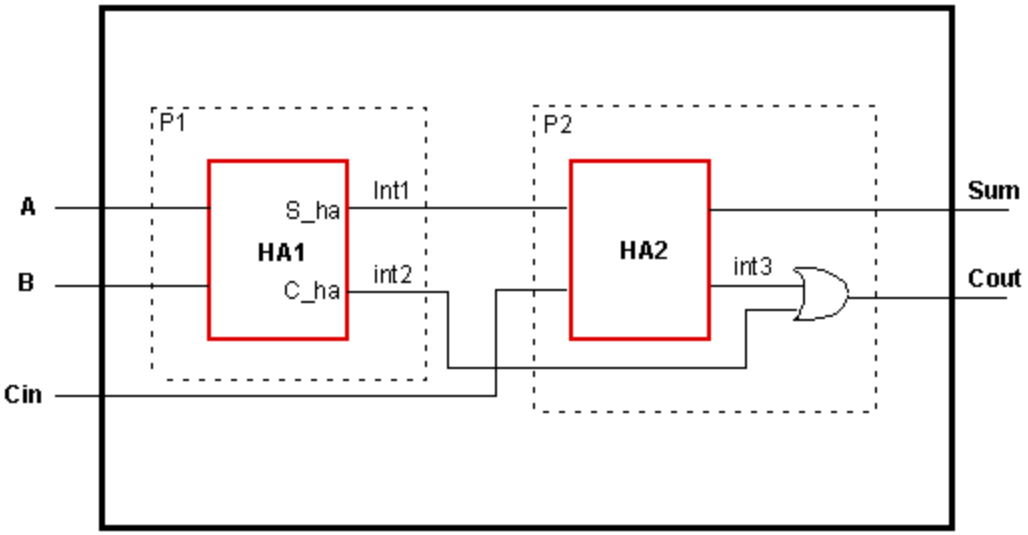

```
entity first_circuit is
      port (  A:          in          std_logic;
              B:          in          std_logic_vector(3 downto 0);
              C:          in          std_logic;
              X:          out         std_logic_vector(6 downto 0);
              Y:          out         std_logic;
              Z:          out         std_logic ) ;
end entity ;
```




```
library ieee;
use  ieee.std_logic_1164.all;

entity half_adder is
port(
            x,y: in std_logic;
            sum, carry: out std_logic);
end entity;

architecture myadd of half_adder is
        begin
                sum <= x xor y;
                carry <= x and y;
End architecture;
```

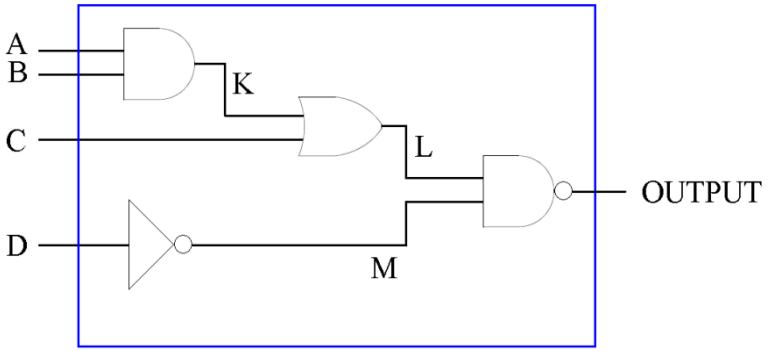


- Int1, Int2, and Int3 are declared as SIGNAL

```
architecture main of full_adder is
Signal Int1, Int3: std_logic  ;
Signal Int2: std_logic: ‘1’ ;
            begin
                        …

End architecture;
```

- Inside the body of the architecture, all statements run concurrently.




```
1   ARCHITECTURE MAIN OF MY_ENTITY IS
2   SIGNAL K, L, M : std_logic ;
3   BEGIN
4       K = A and B ;
5       L = K or C ;
6       M = not D ;
7       Output = L nand M ;
8   END MAIN ;
9
10
11
12  ARCHITECTURE MAIN OF MY_ENTITY IS
13  SIGNAL K, L, M : std_logic ;
14  BEGIN
15      Output = L nand M ;
16      L = K or C ;
17      K = A and B ;
18      M = not D ;
19  END MAIN ;
20
21
```