Separate bus for connecting to CPU

cache $\xrightarrow{\text{word}}$ CPU

memory $\xrightarrow{\text{line}}$ cache

Memory partitioned in M blocks, each containing K words

A cache contains C lines (blocks) $\rightarrow$ $C \ll M$

several words transmitted at a time

each line has tag to identify the block it refers to, and valid bit

hit ratio $H = C/M$