1. Description

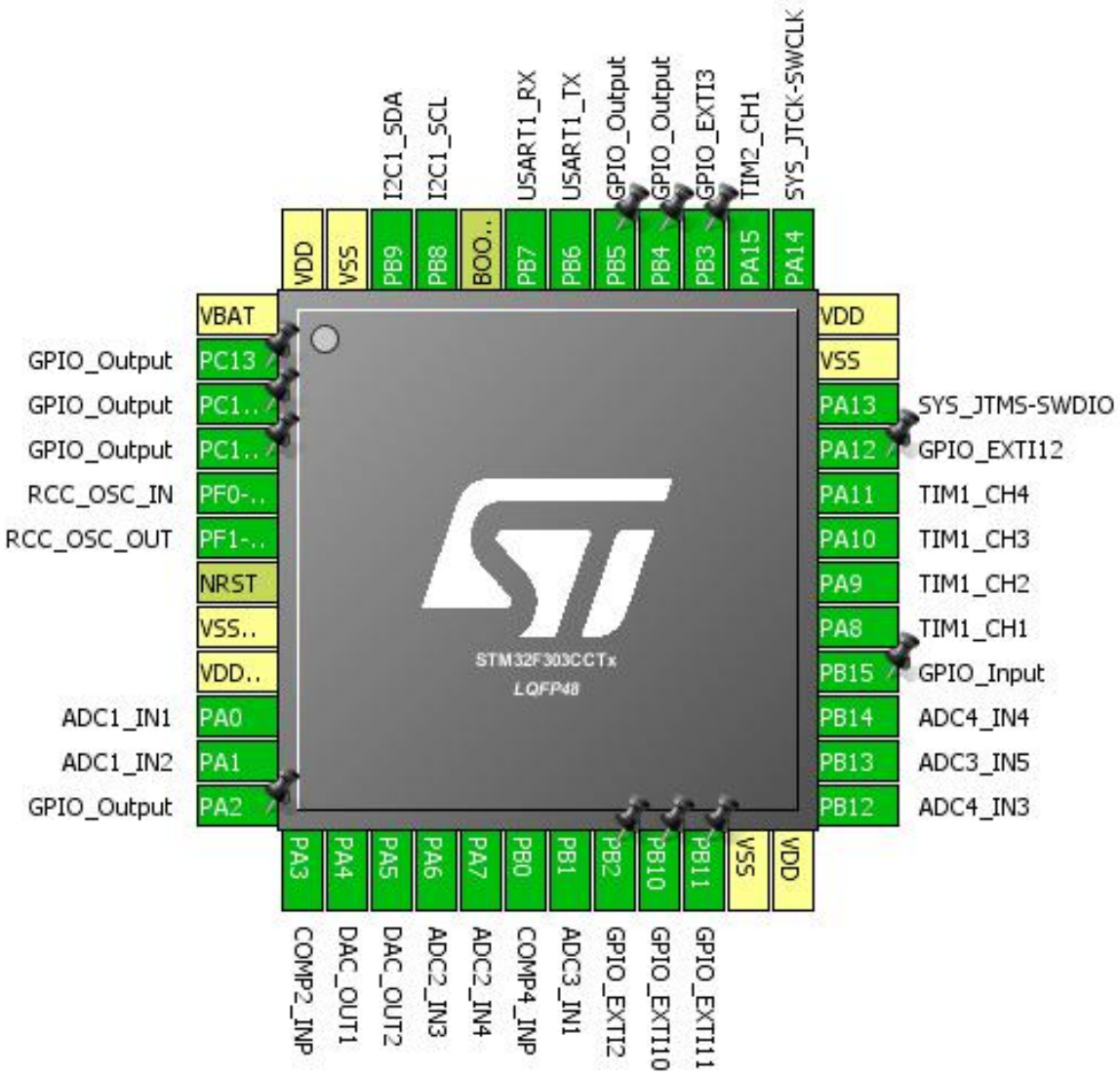
1.1. Project

Project Name	Driver_rev3
Board Name	Driver_rev3.0
Generated with:	STM32CubeMX 4.21.0
Date	05/18/2017

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303CCTx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration



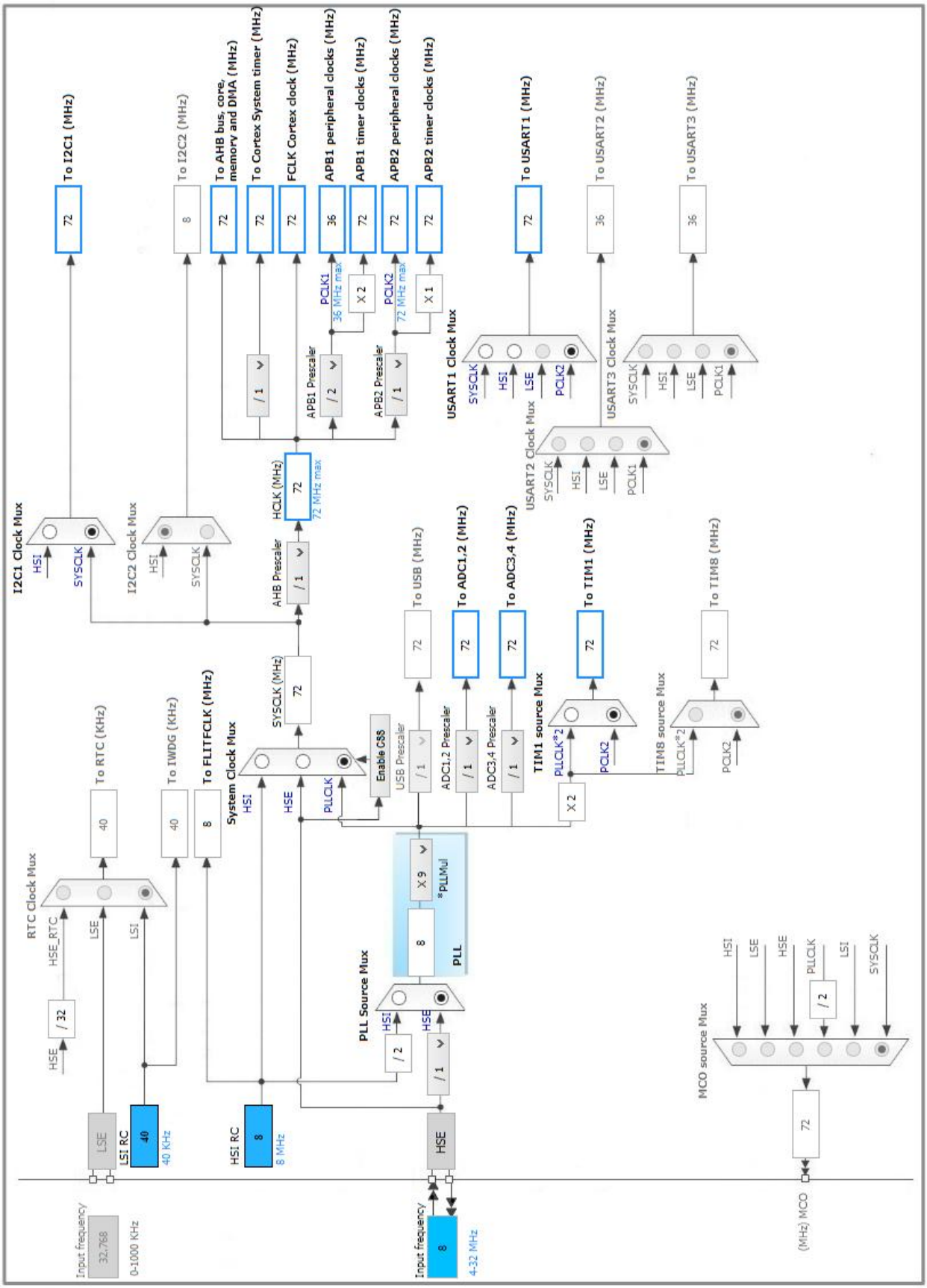
3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Output	
3	PC14-OSC32_IN *	I/O	GPIO_Output	
4	PC15-OSC32_OUT *	I/O	GPIO_Output	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	ADC1_IN1	
11	PA1	I/O	ADC1_IN2	
12	PA2 *	I/O	GPIO_Output	
13	PA3	I/O	COMP2_INP	
14	PA4	I/O	DAC_OUT1	
15	PA5	I/O	DAC_OUT2	
16	PA6	I/O	ADC2_IN3	
17	PA7	I/O	ADC2_IN4	
18	PB0	I/O	COMP4_INP	
19	PB1	I/O	ADC3_IN1	
20	PB2	I/O	GPIO_EXTI2	
21	PB10	I/O	GPIO_EXTI10	
22	PB11	I/O	GPIO_EXTI11	
23	VSS	Power		
24	VDD	Power		
25	PB12	I/O	ADC4_IN3	
26	PB13	I/O	ADC3_IN5	
27	PB14	I/O	ADC4_IN4	
28	PB15 *	I/O	GPIO_Input	
29	PA8	I/O	TIM1_CH1	
30	PA9	I/O	TIM1_CH2	
31	PA10	I/O	TIM1_CH3	
32	PA11	I/O	TIM1_CH4	
33	PA12	I/O	GPIO_EXTI12	
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
37	PA14	I/O	SYS_JTCK-SWCLK	
38	PA15	I/O	TIM2_CH1	
39	PB3	I/O	GPIO_EXTI3	
40	PB4 *	I/O	GPIO_Output	
41	PB5 *	I/O	GPIO_Output	
42	PB6	I/O	USART1_TX	
43	PB7	I/O	USART1_RX	
44	BOOT0	Boot		
45	PB8	I/O	I2C1_SCL	
46	PB9	I/O	I2C1_SDA	
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. ADC2

IN3: IN3 Single-ended
mode: IN4

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.3. ADC3

IN1: IN1 Single-ended

mode: IN5

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.4. ADC4

IN3: IN3 Single-ended

IN4: IN4 Single-ended

5.4.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 3
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.5. COMP2

Input [+]: INP

Input [-]: DAC OUT1

5.5.1. Parameter Settings:

Basic Parameters:

Speed / Power Mode	High Speed / Full Power
Interrupt Trigger Mode	None
Hysteresis Level	None
Blanking Source	None

Output Parameters:

Output Polarity	Not Inverted
Output Internal Selection	None

5.6. COMP4

Input [+]: INP

Input [-]: DAC OUT2

5.6.1. Parameter Settings:

Basic Parameters:

Speed / Power Mode	High Speed / Full Power
Interrupt Trigger Mode	None
Hysteresis Level	None
Blanking Source	None

Output Parameters:

Output Polarity	Not Inverted
Output Internal Selection	None

5.7. DAC

mode: OUT1 Configuration
mode: OUT2 Configuration

5.7.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	None

5.8. I2C1

I2C: I2C

5.8.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x10808DD3 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.9. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.9.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.10. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.11. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable

BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.12. TIM2

Clock Source : Internal Clock

Channel1: Input Capture direct mode

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.13. USART1

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	38400
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable

RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	
ADC2	PA6	ADC2_IN3	Analog mode	No pull up pull down	n/a	
	PA7	ADC2_IN4	Analog mode	No pull up pull down	n/a	
ADC3	PB1	ADC3_IN1	Analog mode	No pull up pull down	n/a	
	PB13	ADC3_IN5	Analog mode	No pull up pull down	n/a	
ADC4	PB12	ADC4_IN3	Analog mode	No pull up pull down	n/a	
	PB14	ADC4_IN4	Analog mode	No pull up pull down	n/a	
COMP2	PA3	COMP2_INP	Analog mode	No pull up pull down	n/a	
COMP4	PB0	COMP4_INP	Analog mode	No pull up pull down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull up pull down	n/a	
	PA5	DAC_OUT2	Analog mode	No pull up pull down	n/a	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull up	**High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull up	**High ***	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull up pull down	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull up pull down	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull up pull down	Low	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull up pull down	Low	
USART1	PB6	USART1_TX	Alternate Function Push Pull	Pull up	**High ***	
	PB7	USART1_RX	Alternate Function Push Pull	Pull up	**High ***	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PC14-OSC32_IN	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PC15-OSC32_OU	GPIO_Output	Output Push Pull	No pull up pull down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	T					
	PA2	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PB10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PB11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PB15	GPIO_Input	Input mode	No pull up pull down	n/a	
	PA12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PB3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PB4	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB5	GPIO_Output	Output Push Pull	No pull up pull down	Low	

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line2 and Touch Sense controller	unused		
EXTI line3 interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger, commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
I2C1 event global interrupt / I2C1 wake-up interrupt through EXTI line 23	unused		
I2C1 error interrupt	unused		
USART1 global interrupt / USART1 wake-up interrupt through EXTI line 25	unused		
EXTI line[15:10] interrupts	unused		
ADC3 global interrupt	unused		
Timer 6 interrupt and DAC underrun interrupts	unused		
ADC4 interrupt	unused		
COMP1, COMP2 and COMP3 interrupts through EXTI lines 21, 22 and 29	unused		
COMP4, COMP5 and COMP6 interrupts through EXTI lines 30, 31 and 32	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303CCTx
Datasheet	023353_Rev13

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Driver_rev3.0
Project Folder	D:\tmp\Driver_rev3.0
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F3 V1.8.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No