DARPA CRAFT Preliminary Packaging Guidelines for TSMC 16FFC Process

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This preliminary guidelines is for CRAFT users who wish to use the standard MOSIS Flip Chip Ball Grid Array (FCBGA) packaging. We are still fine tuning some of packaging requirements for future CRAFT MPW runs. So, some of information may be changed in the next revision.

(1) Packaging for 2.5 mm x 2.5 mm die size

Our packaging plan for 2.5 mm x 2.5 mm die size is to use the same package we had developed for CRAFT MPW1 run in 2016.

Below is the bonding diagram:

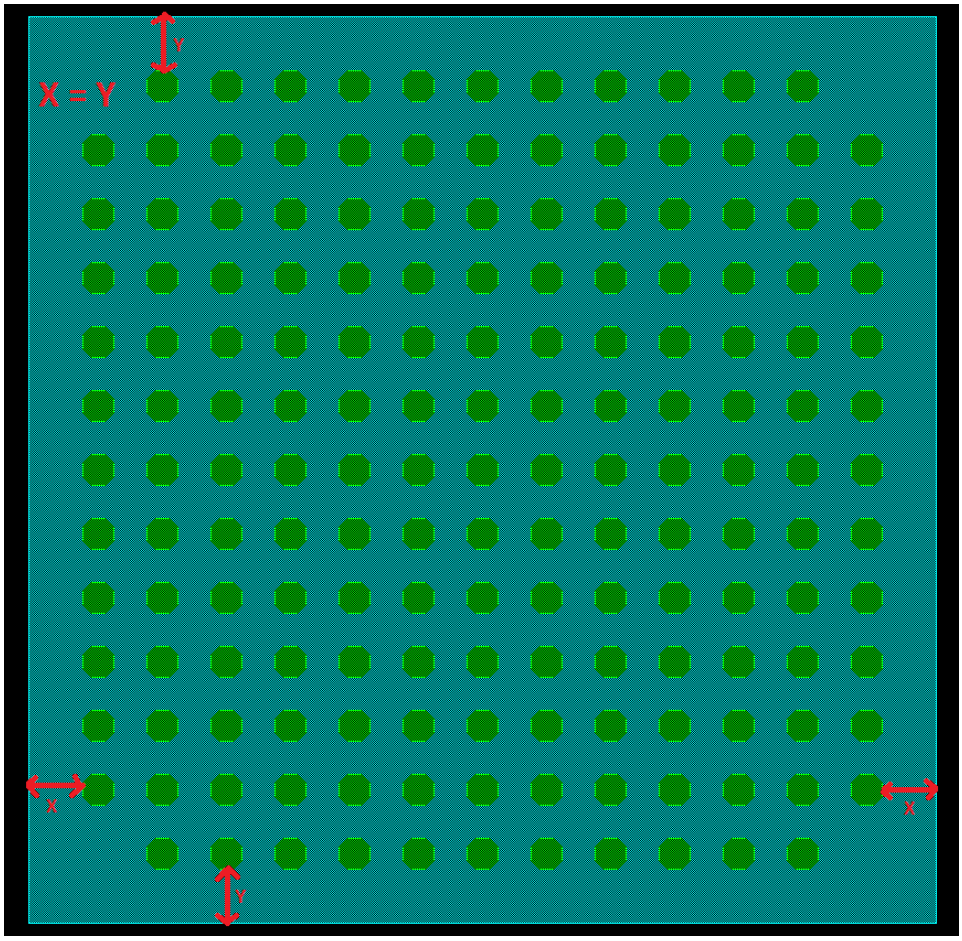
- 2.5 mm x 2.5 mm die area (pre-shrink size, 2500.8 microns x 2500.8 microns)
- 13 x 13 Flip Chip Ball Grid Array (FCBGA) with 170 µm bump pitch (post-shrink size)
- Netlist is shown in die/bump face up view
- Bump composition – Sn1.8Ag
- FCBGA Package body size – 15 X 15
- Solder ball pitch – 1 mm
- Solder ball size – 0.6 mm
- No bumps are allowed in four corners (A13, A1, N13, N1) and L7 (shown in black box)

	13	12	11	10	9	8	7	6	5	4	3	2	1
A		SIGNAL1	SIGNAL2	SIGNAL3	SIGNAL4	SIGNAL5	SIGNAL6	SIGNAL7	SIGNAL8	SIGNAL9	SIGNAL10	SIGNAL11	
B	SIGNAL12	SIGNAL13	SIGNAL14	SIGNAL15	SIGNAL16	SIGNAL17	SIGNAL18	SIGNAL19	SIGNAL20	SIGNAL21	SIGNAL22	SIGNAL23	SIGNAL24
C	SIGNAL25	SIGNAL26	GND	VDD1	GND	VDD2	GND	VDD3	GND	VDD4	GND	SIGNAL27	SIGNAL28
D	SIGNAL29	SIGNAL30	VDD5	VDD6	VDD7	VDD8	GND	VDD9	VDD10	VDD11	VDD12	SIGNAL31	SIGNAL32
E	SIGNAL33	SIGNAL34	GND	VDD13	GND	VDD14	GND	VDD15	GND	VDD16	GND	SIGNAL35	SIGNAL36
F	SIGNAL37	SIGNAL38	VDD17	VDD18	VDD19	GND	VDD20	GND	VDD21	VDD22	VDD23	SIGNAL39	SIGNAL40
G	SIGNAL41	SIGNAL42	GND	GND	GND	VDD24	GND	VDD25	GND	GND	GND	SIGNAL43	SIGNAL44
H	SIGNAL45	SIGNAL46	VDD26	VDD27	VDD28	GND	VDD29	GND	VDD30	VDD31	VDD32	SIGNAL47	SIGNAL48
J	SIGNAL49	SIGNAL50	GND	VDD33	GND	VDD34	GND	VDD35	GND	VDD36	GND	SIGNAL51	SIGNAL52
K	SIGNAL53	SIGNAL54	VDD37	VDD38	VDD39	VDD40	GND	VDD41	VDD42	VDD43	VDD44	SIGNAL55	SIGNAL56
L	SIGNAL57	SIGNAL58	GND	VDD45	GND	VDD46		VDD47	GND	VDD48	GND	SIGNAL59	SIGNAL60
M	SIGNAL61	SIGNAL62	SIGNAL63	SIGNAL64	SIGNAL65	SIGNAL66	SIGNAL67	SIGNAL68	SIGNAL69	SIGNAL70	SIGNAL71	SIGNAL72	SIGNAL73
N		SIGNAL74	SIGNAL75	SIGNAL76	SIGNAL77	SIGNAL78	SIGNAL79	SIGNAL80	SIGNAL81	SIGNAL82	SIGNAL83	SIGNAL84	

All 16FFC users need to use the MOSIS provided seal ring, which is 2.5 mm x 2.5 mm (pre-shrink size, 2500.8 microns x 2500.8 microns). Please notice that there is no pad in each of the four corners, this is a strict requirement from TSMC flip chip design rules (T-N16-BP-DR-001). This

FCBGA packaging has total 164 bumps, which are distributed to 84 signals, 32 grounds, and 48 VDD pins. All signal and VDD pins are individually routed. All GND pins are tied to a single ground.

The pad array in your design must be perfectly symmetrical inside of the seal ring. This means that the distance from UBM to ChipBoundary on all 4 sides must be equal. See diagram below:



The pads must have a 170 µm pitch (post-shrink dimension) for all 16FFC designs. For 16FFC, please use a UBM width of 85 µm with a 173.47 µm bump pitch, if you are using TSMC's provided pads (library name: tpbn16v). You need to use pad cell "**PAD85APB_LF_BU**" from the "**tpbn16v**" TSMC pad library. If you are making your own pads, you need to ensure the following layers are present in your pad layout:

CBD or RV*
AP
CB2_FC
PM
UBM

*: For more details, please refer to table 4.1.1 in document T-N16-BP-DR-001.

(2) Packaging for 5 mm x 5 mm die size

Our packaging plan for 5 mm x 5 mm die size is preliminary. A preliminary 5 mm x 5 mm FCBGA package is extrapolated from the 2.5 mm x 2.5 mm (pre-shrink size) FCBGA package. All 16FFC users need to use the MOSIS provided seal ring, which is 5mm x 5mm (pre-shrink size, 5001.6 microns x 5001.6 microns). This seal ring is posted in the TSMC 16FFC document folder. Please notice that there is no pad in each of the four corners, this is a strict requirement from TSMC flip chip design rules (T-N16-BP-DR-001). The pad array in your design must be perfectly symmetrical inside of the seal ring. This means that the distance from UBM to ChipBoundary on all 4 sides must be equal (X=Y). Please see the diagram provided in section (1) above.

A preliminary bump pattern diagram is shown below. This suggested FCBGA packaging has 26 x 26 array of bumps. The pads must have a 170 µm pitch (post-shrink dimension) for all 16FFC designs. For 16FFC, please use a UBM width of 85 µm with a 173.47 µm bump pitch, if you are using TSMC's provided pads (library name: tpbn16v). You need to use pad cell "**PAD85APB_LF_BU**" from the "**tpbn16v**" TSMC pad library. After 98% shrink, the final UBM width size and bump pitch will be 83.3 µm and 170 µm.

Also, here is a short summary of preliminary information for CRAFT MPW2 FCBGA package for 5 mm x 5 mm die (pre-shrink size, 5001.6 microns x 5001.6 microns).

- Bump composition - Sn1.8Ag
- FCBGA Package body size – 27 X 27
- Solder ball pitch – 1 mm
- Solder ball size – 0.6 mm
- Solder ball matrix – 26 X 26
- No bumps are allowed in four corners (A26, A1, AF26, AF1) and AF24 (shown in below bump pattern diagram as black box)

- Preliminary 5 mm x 5 mm die area: 26 x 26 Flip Chip Ball Grid Array (FCBGA) with 170 µm bump pitch (post-shrink size). The pin numbers are shown as it is for bump facing up (die face up) and the solder ball (BGA) assignment will be mirrored.

	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A		VCP	S1	S2	VSS	VIO	S3	VCP	S4	VSS	DP1	DP2	VSS	VSS	DP3	DP4	VSS	S5	VCP	S6	VIO	VSS	S7	S8	VCP	
B	VCP	VIO	VSS	S9	S10	S11	S12	S13	S14	S15	VSS	VSS	S16	S17	VSS	VSS	S18	S19	S20	S21	S22	S23	S24	VSS	VIO	VCP
C	S25	VSS	VIO	S26	S27	VCP	VSS	S28	S29	S30	VIO	VIO	VCP	VCP	VIO	VIO	S31	S32	S33	VSS	VCP	S34	S35	VIO	VSS	S36
D	S37	S38	S39	VSS	S40	S41	S42	S43	VSS	S44	S45	S46	S47	S48	S49	S50	S51	VSS	S52	S53	S54	S55	VSS	S56	S57	S58
E	VSS	S59	S60	S61	VSS	S62	S63	S64	S65	S66	VCP	S67	S68	S69	S70	VCP	S71	S72	S73	S74	S75	VSS	S76	S77	S78	VSS
F	VIO	S79	VCP	S80	S81	GVD	GVD	IVD1	IVD1	IVD1	IVD2	IVD2	IVD2	IVD2	IVD2	IVD2	IVD3	IVD3	IVD3	GVD	GVD	S82	S83	VCP	S84	VIO
G	S85	S86	VSS	S87	S88	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	S89	S90	VSS	S91	S92
H	VCP	S93	S94	S95	S96	IVD1	IVD1	IVD1	IVD1	IVD1	GVD	GVD	IVD2	IVD2	GVD	GVD	IVD3	IVD3	IVD3	IVD3	IVD3	S97	S98	S99	S100	VCP
J	S101	S102	S103	VSS	S104	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	S105	VSS	S106	S107	S108
K	VSS	S109	S110	S111	S112	GVD	GVD	IVD1	IVD1	IVD1	IVD2	IVD2	IVD2	IVD2	IVD2	IVD2	IVD3	IVD3	IVD3	GVD	GVD	S113	S114	S115	S116	VSS
L	DP5	VSS	VIO	S117	VCP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCP	S118	VIO	VSS	DP6
M	DP7	VSS	VIO	S119	S120	IVD1	IVD1	IVD1	IVD1	IVD1	GVD	GVD	IVD2	IVD2	GVD	GVD	IVD3	IVD3	IVD3	IVD3	IVD3	S121	S122	VIO	VSS	DP8
N	VSS	S123	VCP	S124	S125	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	S126	S127	VCP	S128	VSS
P	VSS	S129	VCP	S130	S131	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	S132	S133	VCP	S134	VSS
R	DP9	VSS	VIO	S135	S136	IVD4	IVD4	IVD4	IVD4	IVD4	GVD	GVD	IVD5	IVD5	GVD	GVD	IVD6	IVD6	IVD6	IVD6	IVD6	S137	S138	VIO	VSS	DP10
T	DP11	VSS	VIO	S139	VCP	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCP	S140	VIO	VSS	DP12
U	VSS	S141	S142	S143	S144	GVD	GVD	IVD4	IVD4	IVD4	IVD5	IVD5	IVD5	IVD5	IVD5	IVD5	IVD6	IVD6	IVD6	GVD	GVD	S145	S146	S147	S148	VSS
V	S149	S150	S151	VSS	S152	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	S153	VSS	S154	S155	S156
W	VCP	S157	S158	S159	S160	IVD4	IVD4	IVD4	IVD4	IVD4	GVD	GVD	IVD5	IVD5	GVD	GVD	IVD6	IVD6	IVD6	IVD6	IVD6	S161	S162	S163	S164	VCP
Y	S165	S166	VSS	S167	S168	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	S169	S170	VSS	S171	S172
AA	VIO	S173	VCP	S174	S175	GVD	GVD	IVD4	IVD4	IVD4	IVD5	IVD5	IVD5	IVD5	IVD5	IVD5	IVD6	IVD6	IVD6	GVD	GVD	S176	S177	VCP	S178	VIO
AB	VSS	S179	S180	S181	VSS	S182	S183	S184	S185	S186	VCP	S187	S188	S189	S190	VCP	S191	S192	S193	S194	S195	VSS	S196	S197	S198	VSS
AC	S199	S200	S201	VSS	S202	S203	S204	S205	VSS	S206	S207	S208	S209	S210	S211	S212	S213	VSS	S214	S215	S216	S217	VSS	S218	S219	S220
AD	S221	VSS	VIO	S222	S223	VCP	VSS	S224	S225	S226	VIO	VIO	VCP	VCP	VIO	VIO	S227	S228	S229	VSS	VCP	S230	S231	VIO	VSS	S232
AE	VCP	VIO	VSS	S233	S234	S235	S236	S237	S238	S239	VSS	VSS	S240	S241	VSS	VSS	S242	S243	S244	S245	S246	S247	S248	VSS	VIO	VCP
AF		VCP		S249	VSS	VIO	S250	VCP	S251	VSS	DP13	DP14	VSS	VSS	DP15	DP16	VSS	S252	VCP	S253	VIO	VSS	S254	S255	VCP	

- Legends for preliminary 5 mm x 5 mm die package bump patterns:

	Net	Net Short Name	# Bumps	Tied together on package?
	VSS	VSS	200	Yes
	VIO	VIO	32	Yes
	VDD Core Periph	VCP	40	Yes
1	Internal VDD1	IVD1	16	Yes
2	Internal VDD2	IVD2	16	Yes
3	Internal VDD3	IVD3	16	Yes
4	Internal VDD4	IVD4	16	Yes
5	Internal VDD5	IVD5	16	Yes
6	Internal VDD6	IVD6	16	Yes
	Global VDD	GVD	32	Yes
	Diff Pairs	DP	16	No (DP1 ~ DP16)
	Regular signals	S	255	No (S1 ~ S255)
	No Bump		5	No Bump

- 415 peripheral bumps
  - Bumps routed to IO cells in the peripheral pad ring
  - 32 VDDIO
  - 40 VDDCORE
  - 72 VSS
  - 271 Signal bumps
    - Includes 8 diff pairs (16)
    - Can be allocated to low-noise supply for PLLs etc.

- 256 Internal power bumps (16x16 internal bump array)
  - Not routed to the peripheral pad ring, but connected directly to package power planes
  - 128 VSS bumps
  - 32 Global VDD bumps
  - 16 VDD bumps/segment (96 total)