The RF MOSFET Line

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

• Typical 2-carrier W-CDMA Performance for $V_{DD}=28$ Volts, $I_{DQ}=500$ mA, f1 = 2135 MHz, f2 = 2145 MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels measured over 3.84 MHz Bandwidth at f1 -5 MHz and f2 +5 MHz, Distortion Products measured over a 3.84 MHz Bandwidth at f1 -10 MHz and f2 +10 MHz, Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.

Output Power — 10 Watts Avg.

Efficiency — 23.5%

Gain — 15 dB

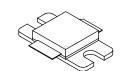
IM3 — -37.5 dBc

ACPR — -41 dBc

- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads, 40μ" Nominal.
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

MRF21045LR3 MRF21045LSR3

2170 MHz, 45 W, 28 V LATERAL N-CHANNEL RF POWER MOSFETs



CASE 465E-04, STYLE 1 NI-400 MRF21045LR3



CASE 465F-04, STYLE 1 NI-400S MRF21045LSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	105 0.60	Watts W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Operating Junction Temperature	TJ	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

THERMAL CHARACTERISTICS

Characteristic		Max	Unit
Thermal Resistance, Junction to Case		1.65	°C/W

NOTE - <u>CAUTION</u> - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.





Characteristic	Symbol	Min	Тур	Max	Unit
DFF CHARACTERISTICS					I
Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 100 μAdc)	V _{(BR)DSS}	65	_	_	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	_	_	10	μAdc
Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	_	_	1	μAdc
ON CHARACTERISTICS (DC)					
Gate Threshold Voltage $(V_{DS} = 10 \text{ Vdc}, I_D = 100 \mu\text{Adc})$	V _{GS(th)}	2	_	4	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 500 mAdc)	V _{GS(Q)}	3	3.9	5	Vdc
Drain-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 1 Adc)	V _{DS(on)}	_	0.19	0.21	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 1 Adc)	9fs	_	3	_	S
YNAMIC CHARACTERISTICS (1)			•		1
Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz)	C _{rss}	_	1.8	_	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2-carrier on CCDF.	W-CDMA. Pe	ak/Avg. ratio	= 8.3 dB @	0.01% Proba	ability
Common-Source Amplifier Power Gain $(V_{DD}=28\ Vdc,\ P_{out}=10\ W\ Avg.,\ I_{DQ}=500\ mA,\ f1=2112.5\ MHz,\ f2=2122.5\ MHz\ and\ f1=2157.5\ MHz,\ f2=2167.5\ MHz)$	G _{ps}	13.5	15	_	dB
Drain Efficiency $(V_{DD} = 28 \text{ Vdc}, P_{out} = 10 \text{ W Avg.}, I_{DQ} = 500 \text{ mA}, f1 = 2112.5 \text{ MHz}, f2 = 2122.5 \text{ MHz} and f1 = 2157.5 \text{ MHz}, f2 = 2167.5 \text{ MHz})$	η	21	23.5	_	%
Third Order Intermodulation Distortion ($V_{DD}=28~Vdc,~P_{out}=10~W~Avg.,~I_{DQ}=500~mA,~f1=2112.5~MHz,~f2=2122.5~MHz~and~f1=2157.5~MHz,~f2=2167.5~MHz;~IM3~measured~over~3.84~MHz~Bandwidth~at~f1~-10~MHz~and~f2~+10~MHz.)$	IM3	_	-37.5	-35	dBc
Adjacent Channel Power Ratio $(V_{DD}=28\ Vdc,\ P_{out}=10\ W\ Avg.,\ I_{DQ}=500\ mA,\ f1=2112.5\ MHz,\ f2=2122.5\ MHz\ and\ f1=2157.5\ MHz,\ f2=2167.5\ MHz;\ ACPR$ measured over 3.84 MHz Bandwidth at f1 -5 MHz and f2+5 MHz.)	ACPR	_	-41	-38	dBc
Input Return Loss $(V_{DD}=28\ Vdc,\ P_{out}=10\ W\ Avg.,\ I_{DQ}=500\ mA,\ f1=2112.5\ MHz,\ f2=2122.5\ MHz\ and\ f1=2157.5\ MHz,\ f2=2167.5\ MHz)$	IRL	_	-12	-9	dB
Output Mismatch Stress (V _{DD} = 28 Vdc, P _{out} = 45 W CW, I _{DQ} = 500 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No	Degradation Before and	In Output Po After Test	wer

⁽¹⁾ Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) — continu	FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) — continued				
Two-Tone Common-Source Amplifier Power Gain $(V_{DD}=28~Vdc,~P_{out}=45~W~PEP,~I_{DQ}=500~mA, f1=2110~MHz,~f2=2120~MHz~and~f1=2160~MHz,~f2=2170~MHz)$	G _{ps}	_	14.9		dB
Two-Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	η	_	36	_	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IMD	_	-30	_	dBc
Two-Tone Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IRL	_	-12	_	dB
P_{out} , 1 dB Compression Point (V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f = 2170 MHz)	P1dB	_	50		W

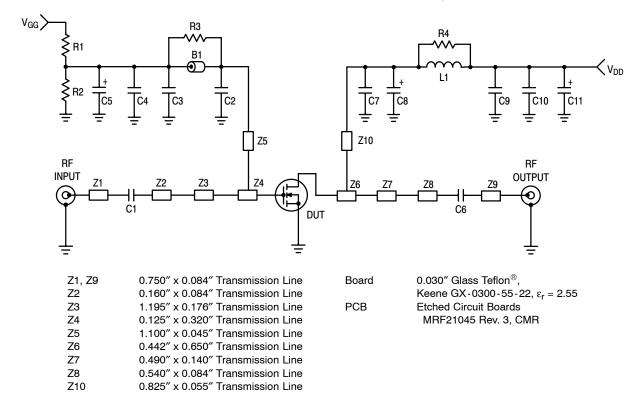


Figure 1. MRF21045LR3(LSR3) Test Circuit Schematic

Table 1. MRF21045LR3(LSR3) Component Designations and Values

Designators	Description	
B1	Short Ferrite Bead, Fair Rite, #2743019447	
C1, C2, C6	43 pF Chip Capacitors, ATC #100B430JCA500X	
C7	5.6 pF Chip Capacitor, ATC #100B5R6JCA500X	
C3, C9	1000 pF Chip Capacitors, ATC #100B102JCA500X	
C4, C10	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS	
C5	1.0 μF Tantalum Chip Capacitor, Kemet #T491C105M050	
C8	10 μF Tantalum Chip Capacitor, Kemet #T495X106K035AS4394	
C11	22 μF Tantalum Chip Capacitor, Kemet #T491X226K035AS4394	
L1	1 Turn, #20 AWG, 0.100" ID, Motorola	
N1, N2	Type N Flange Mounts, Omni Spectra #3052-1648-10	
R1	1.0 kΩ, 1/8 W Chip Resistor	
R2	180 kΩ, 1/8 W Chip Resistor	
R3, R4	10 Ω, 1/8 W Chip Resistors	

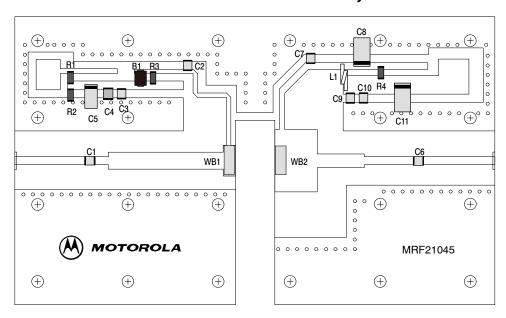


Figure 2. MRF21045LR3(LSR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

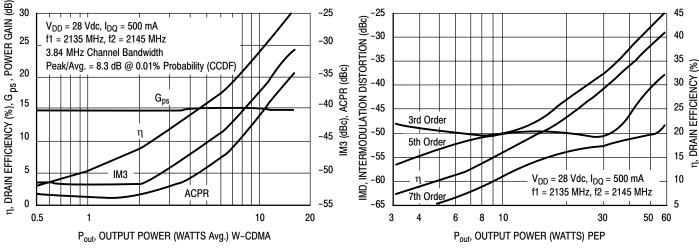


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

Figure 4. Intermodulation Distortion Products versus Output Power

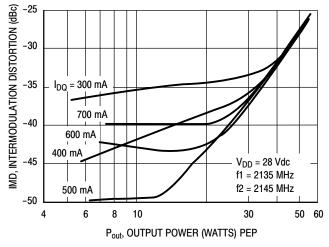


Figure 5. Intermodulation Distortion versus Output Power

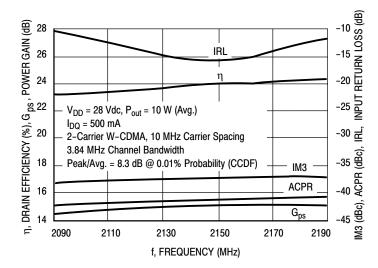


Figure 6. 2-Carrier W-CDMA Broadband Performance

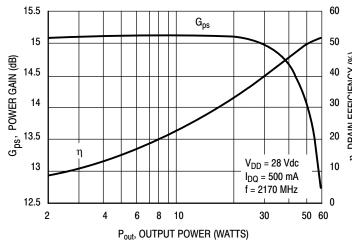


Figure 7. CW Performance

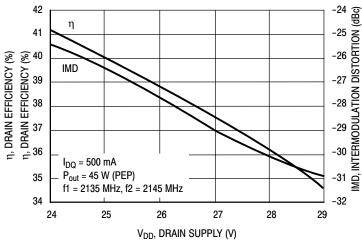


Figure 8. Two-Tone Intermodulation
Distortion and Drain Efficiency versus Drain
Supply

TYPICAL CHARACTERISTICS

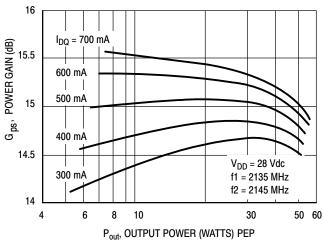


Figure 9. Two-Tone Power Gain versus
Output Power

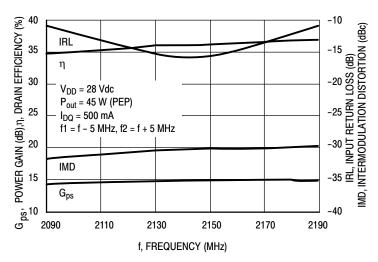


Figure 10. Two-Tone Broadband Performance

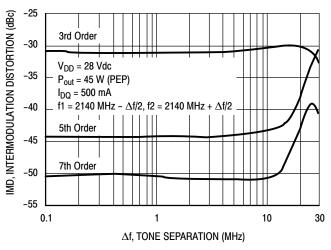


Figure 11. Intermodulation Distortion Products versus Two-Tone Spacing

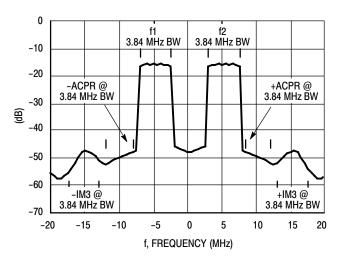
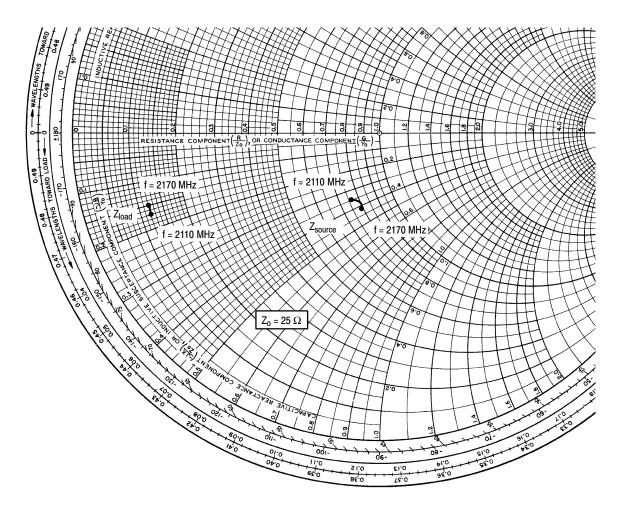


Figure 12. 2-Carrier W-CDMA Spectrum



 V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 10 W Avg.

f MHz	$\mathbf{Z_{source}}_{\Omega}$	$oldsymbol{Z_{load}}{\Omega}$
2110	18.88 - j8.86	3.11 - j4.18
2140	19.80 - j9.93	3.09 - j3.87
2170	19.68 - j10.44	3.12 - j3.72

Test circuit impedance as measured from $Z_{source} =$ gate to ground.

 $Z_{load} \\$ Test circuit impedance as measured from drain to ground.

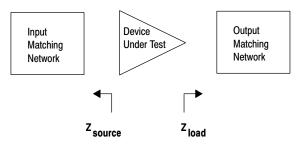
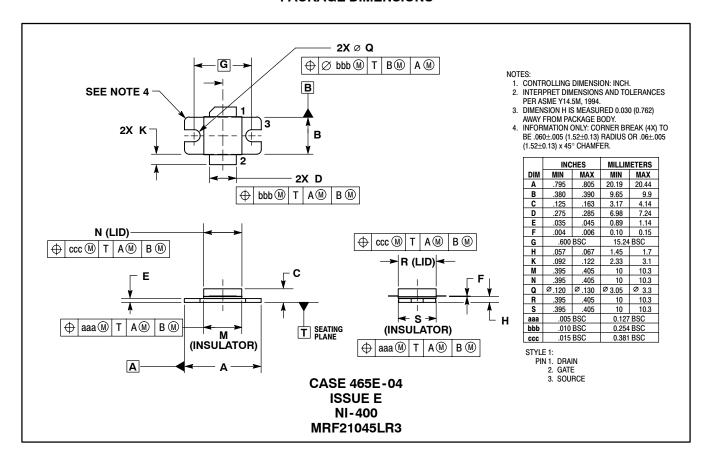
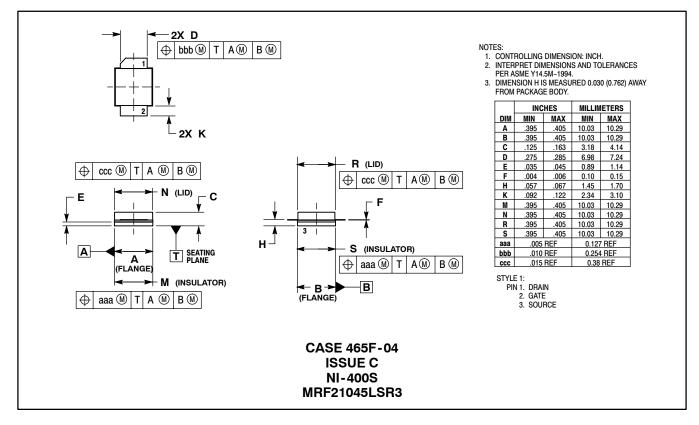


Figure 13. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS





Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

MOTOROLA and the Stylized M Logo are registered in the US Patent and Trademark Office. All other product or service names are the property of their respective owners. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© Motorola Inc. 2004

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED: Motorola Literature Distribution P.O. Box 5405, Denver, Colorado 80217 1-800-521-6274 or 480-768-2130 JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573, Japan 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong 852-26668334

HOME PAGE: http://motorola.com/semiconductors

