Gebze Technical University Computer Engineering

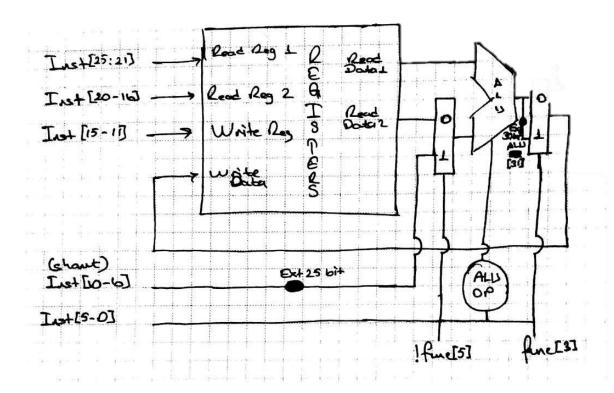
CSE 331 - 2018 Fall

ASSIGNMENT 3 REPORT

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Making of Single Cycle Datapath of a mips processor

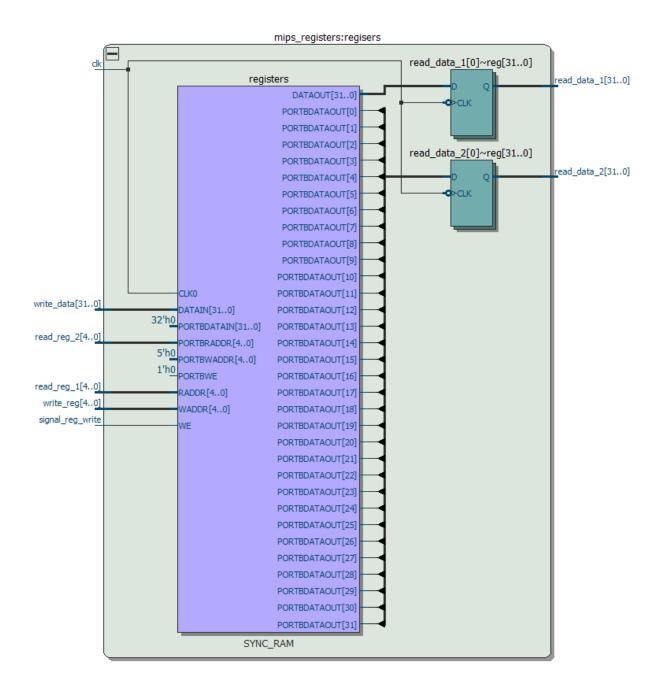
To make the required datapath I used following schema.



Main Mips32 Module(Explained)

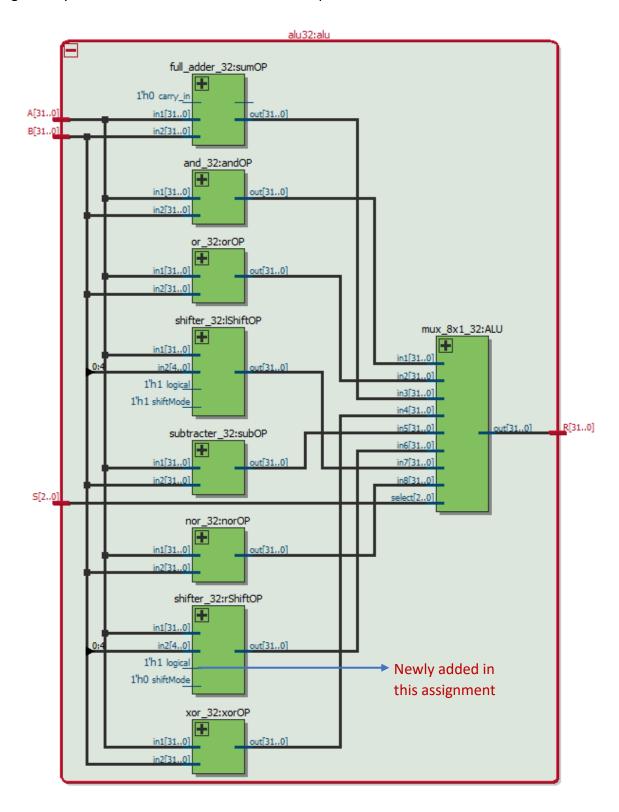
Registers (Mips_register module)

I used an external clock to determine to write or read in a single cycle. In positive edge it always writes and in negative edge it always reads.



Alu (From previous assignment)

I used previous alu unit with slight modifications to shifter to work both in arithmetic and logical way. To do that I added another control input to shifter module in alu.

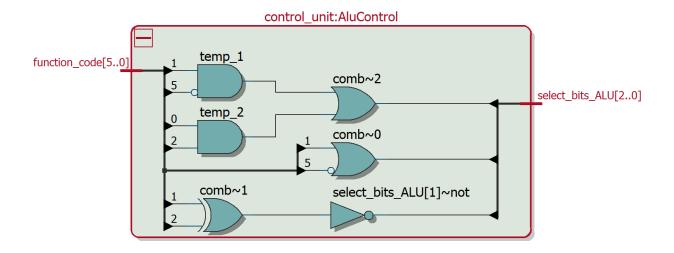


Alu Control Unit

I created a truth table for given function what to expect from Alu select bits. And after that used simplification and Karnaugh map methods to create simplest logic out of it.

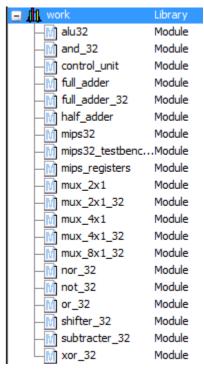
P7 F4 F3 F2 F1 F0	52 31 SO	ALU OP HOUNE
100000	010	
100001	010	S2 = Total F5 +F
100100	000	
100111	1 1 1	SL= FZ=1+FZ=1 (XNOV)
00101	001	
01011	100	SO = 1371 + 7270
00000	110	
00000	101	
00010	100	
00011	100	

Note: I used an online Karnaugh map solver for given input and outputs to take the most efficient logic.



ModelSim Results

All modules



Simulation Results

```
# rs = 10010, rt = 10001, rd = 10100, func = 000010, shamt =
                         # rs = 10000, rt = 10001, rd = 10101, func = 100001, shamt =
# rs = 10000, rt = 10001, rd = 00000, func = 100100, shamt =
                         # rs = 10000, rt = 10001, rd = 00001, func = 100111, shamt =
# rs = 10000, rt = 10001, rd = 00011, func = 101011, shamt =
                         # rs = 10001, rt = 10000, rd = 10100, func = 100010, shamt =
                         # rs = 10001, rt = 10000, rd = 10101, func = 100011, shamt =
```

