計算機結構
(數位邏輯基礎)

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第 4 章
Logic Functions and Gates

Computer Organization and Design Fundamental

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投影片製作者：陳鍾誠

4.1 Logic Gate Basics

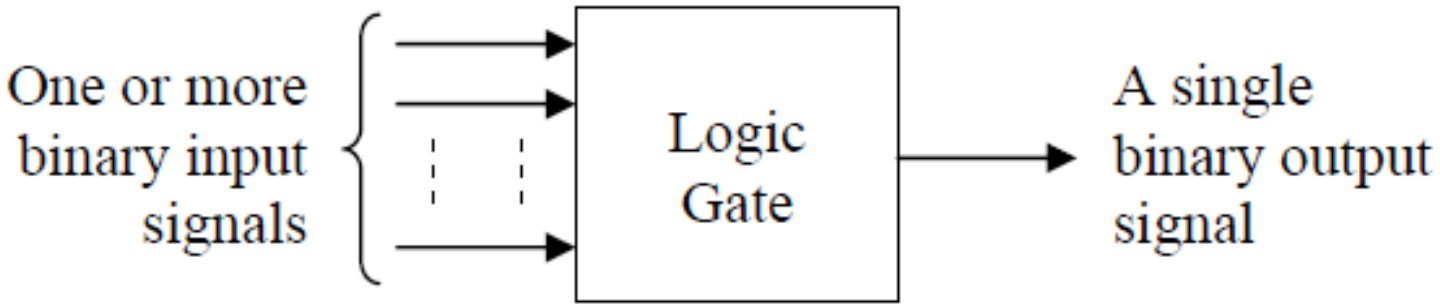


Figure 4-1 Basic Format of a Logic Gate

4 種基本邏輯閘

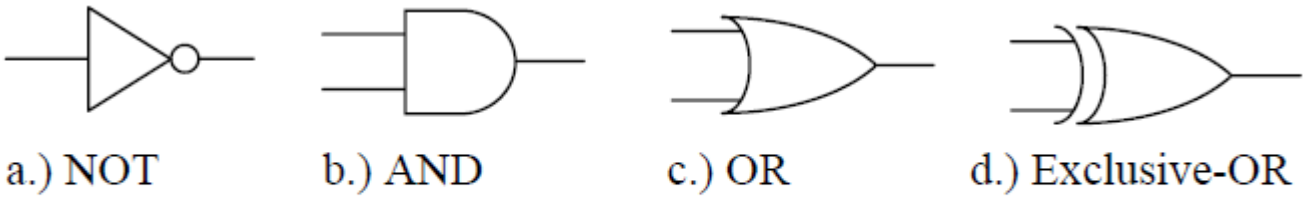


Figure 4-2 Basic Logic Symbols

4.1.1 NOT Gate (反閘)

Figure 4-3 Operation of the NOT Gate

A	X
0	1
1	0

Figure 4-9 Inverter Truth Table

4.1.2 AND Gate

Figure 4-4 Operation of a Two-Input AND Gate

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Figure 4-10 Two-Input AND Gate Truth Table

4.1.3 OR Gate

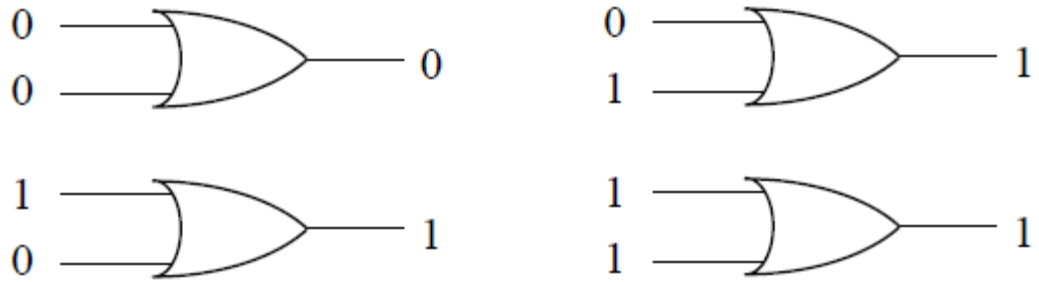


Figure 4-5 Operation of a Two-Input OR Gate

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

Figure 4-11 Two-Input OR Gate Truth Table

4.1.4 Exclusive-OR (XOR) Gate

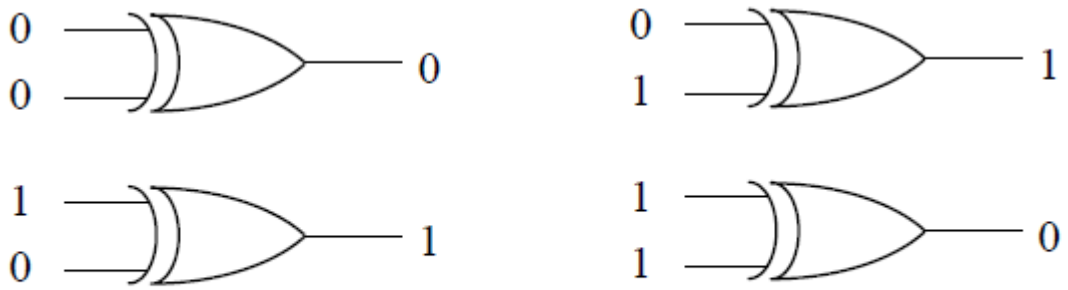


Figure 4-6 Operation of a Two-Input XOR Gate

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

Figure 4-12 Two-Input XOR Gate Truth Table

4.2 Truth Tables (真值表)

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Figure 4-7 Sample Three-Input Truth Table

真值表輸入的完整列舉

A	B	C	D	X
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Figure 4-8 Listing All Bit Patterns for a Four-Input Truth Table

有 Don’t care 的真值表

- X : Don’t care, 可以是 0 或 1

A	B	C	X
0	X	X	0
X	0	X	0
X	X	0	0
1	1	1	1

Figure 4-13 Three-Input AND Gate Truth Table With Don't Cares

4.3 Timing Diagrams for Gates

4.3 Timing Diagrams for Gates

三輸入 And 閘的時序圖

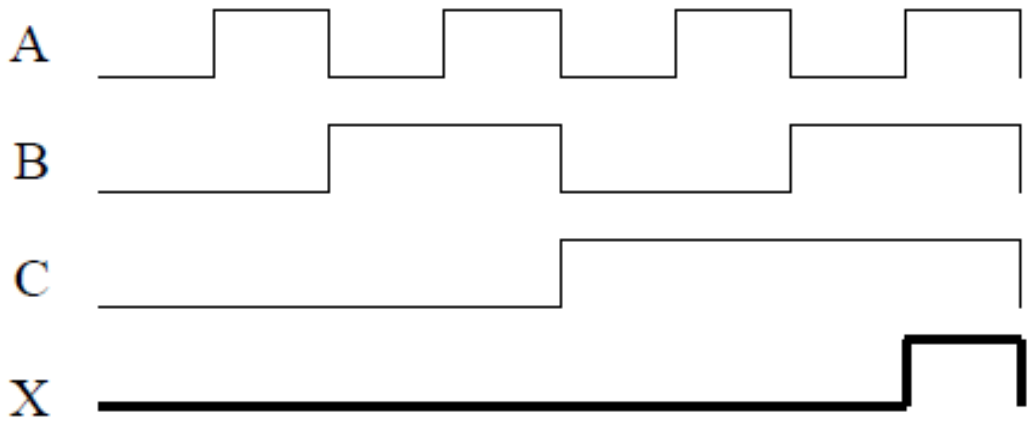


Figure 4-14 Sample Timing Diagram for a Three-Input AND Gate

三輸入 OR 閘的時序圖

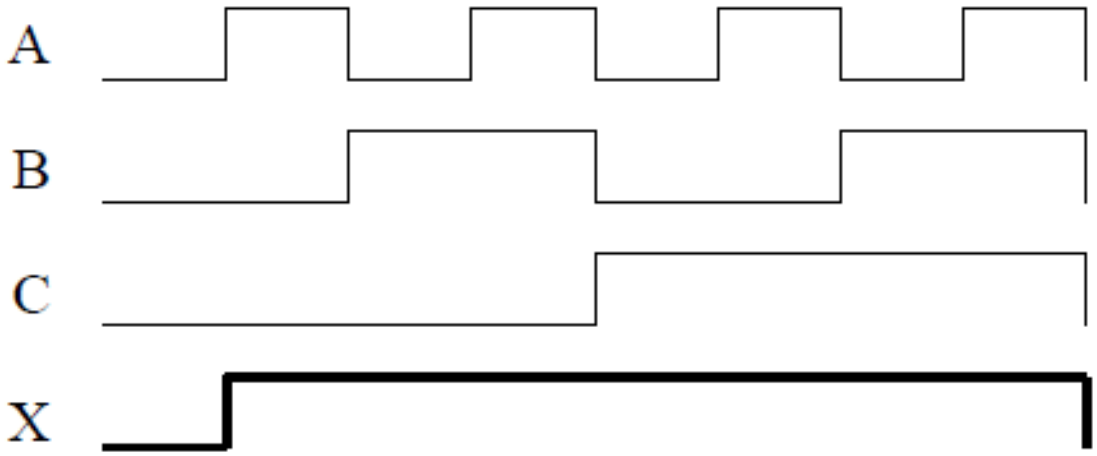


Figure 4-15 Sample Timing Diagram for a Three-Input OR Gate

三輸入 XOR 閘的時序圖

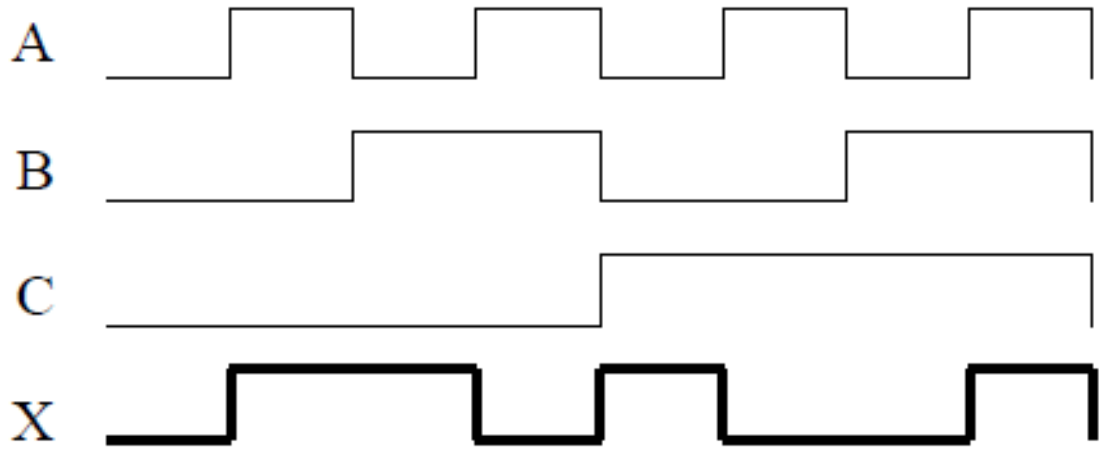


Figure 4-16 Sample Timing Diagram for a Three-Input XOR Gate

4.4 Combinational Logic

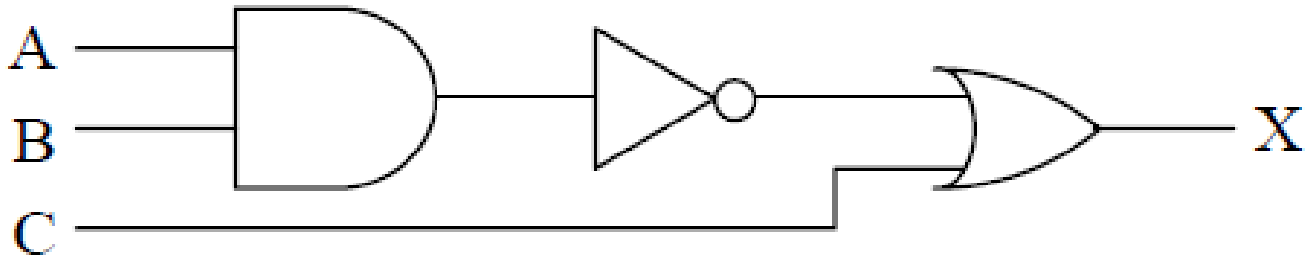
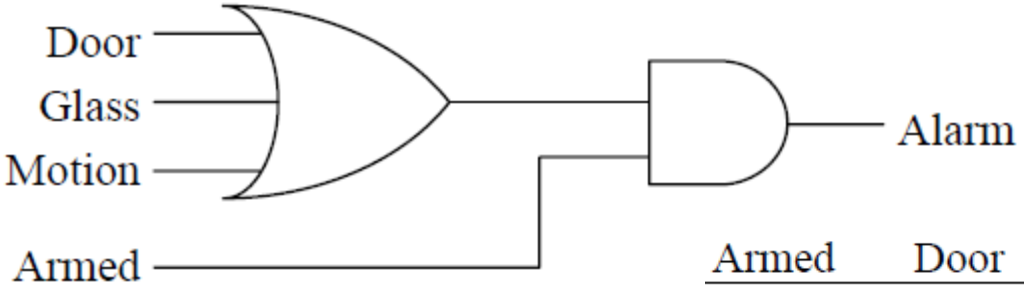


Figure 4-17 Sample Combinational Logic

防盜系統電路



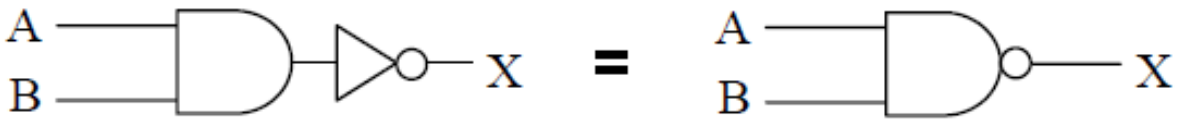
armed

KK [ɑrmd] DJ [ɑ:md] 即時發音

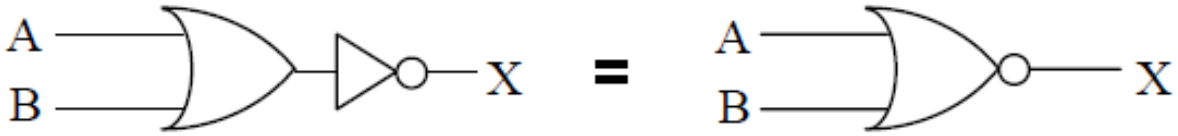
1. 武裝的, 裝甲的

Armed	Door	Glass	Motion	Alarm
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

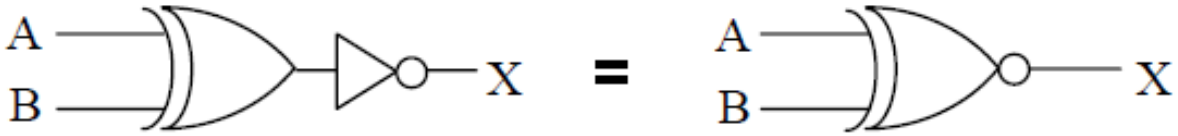
包含 not 的基本電路符號



a) AND gate + NOT gate = NAND gate



b) OR gate + NOT gate = NOR gate



c) Exclusive-OR gate + NOT gate = Exclusive NOR gate

Figure 4-20 "NOT" Circuits

包含 not 的簡化電路圖

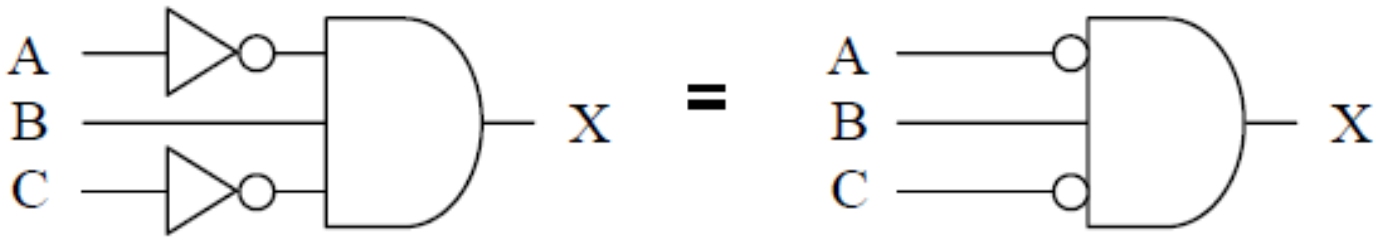


Figure 4-21 Schematic "Short-Hand" for Inverted Inputs

4.5 Truth Tables for Combinational Logic

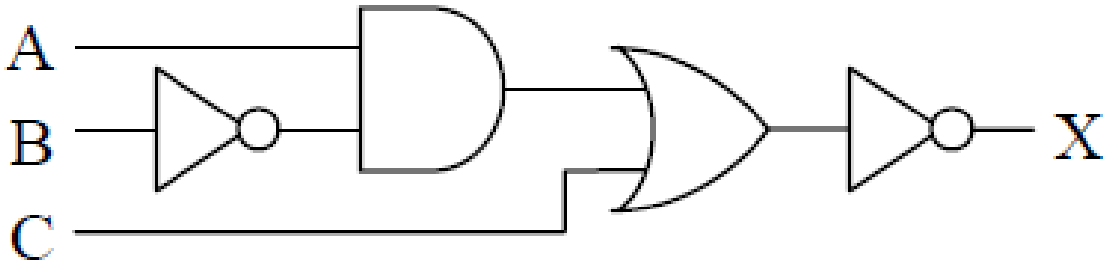


Figure 4-22 Sample of Multi-Level Combinational Logic

如何計算電路的輸出值（單一輸入）

a.) A 0 is input to the first inverter which outputs a 1.

b.) The 1 coming from the inverter is combined with a 0 in the AND gate to output a 0.

c.) The OR gate receives a 0 from the AND and a 0 from the inputs which makes it output a 0.

d.) The 0 output from the OR gate passes through the inverter output a 1.

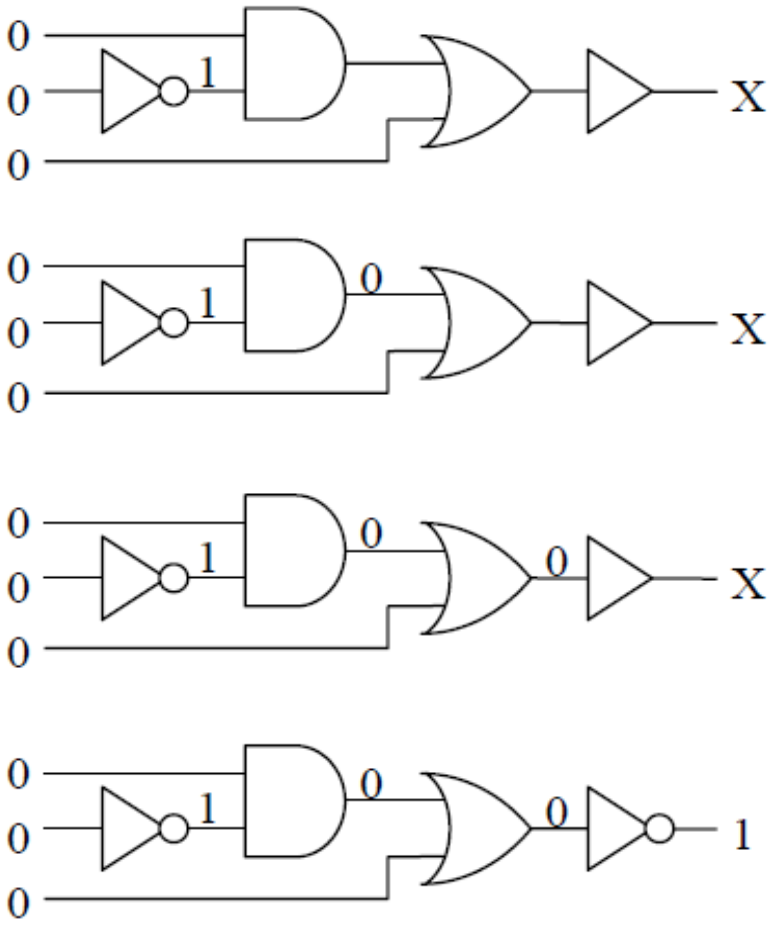
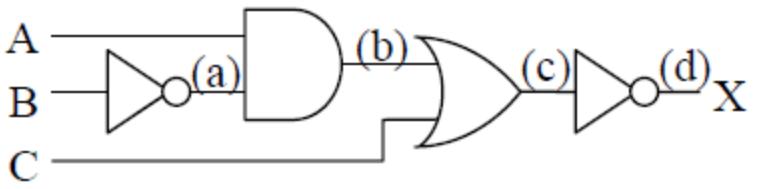


Figure 4-23 Process of Passing Inputs Through Combinational Logic

如何計算電路的輸出值（所有輸入）



計算 (a)

A	B	C	(a) = NOT of B
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

計算 (b)

A	B	C	(a)	(b)	(c) = (b) OR C
0	0	0	1	0	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	1	0	0	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	0	1

計算 (c)

A	B	C	(a)	(b) = (a) AND A
0	0	0	1	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	0	0
1	1	1	0	0

計算 (d)

A	B	C	(a)	(b)	(c)	X = (d) = NOT of (c)
0	0	0	1	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	1	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	0	1
1	1	1	0	0	1	0

計算機結構 – 組合電路

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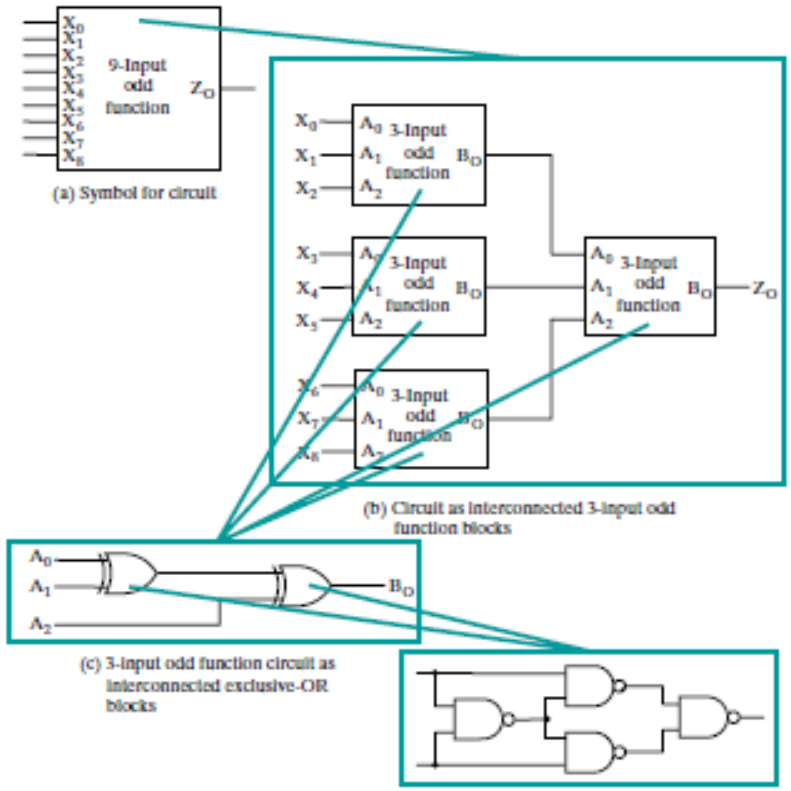
同位檢查 (Parity Check) 電路

Hierarchy for Parity Tree Example



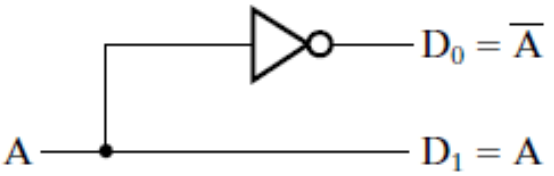
解碼器

Decoder Examples

- **1-to-2-Line Decoder**

A	D_0	D_1
0	1	0
1	0	1

(a)

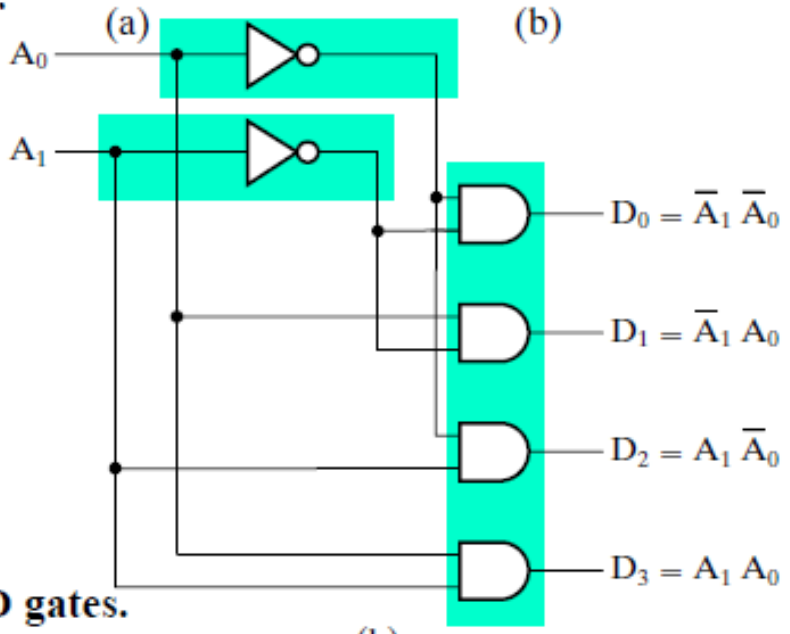


(b)

- **2-to-4-Line Decoder**

A_1	A_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

(a)



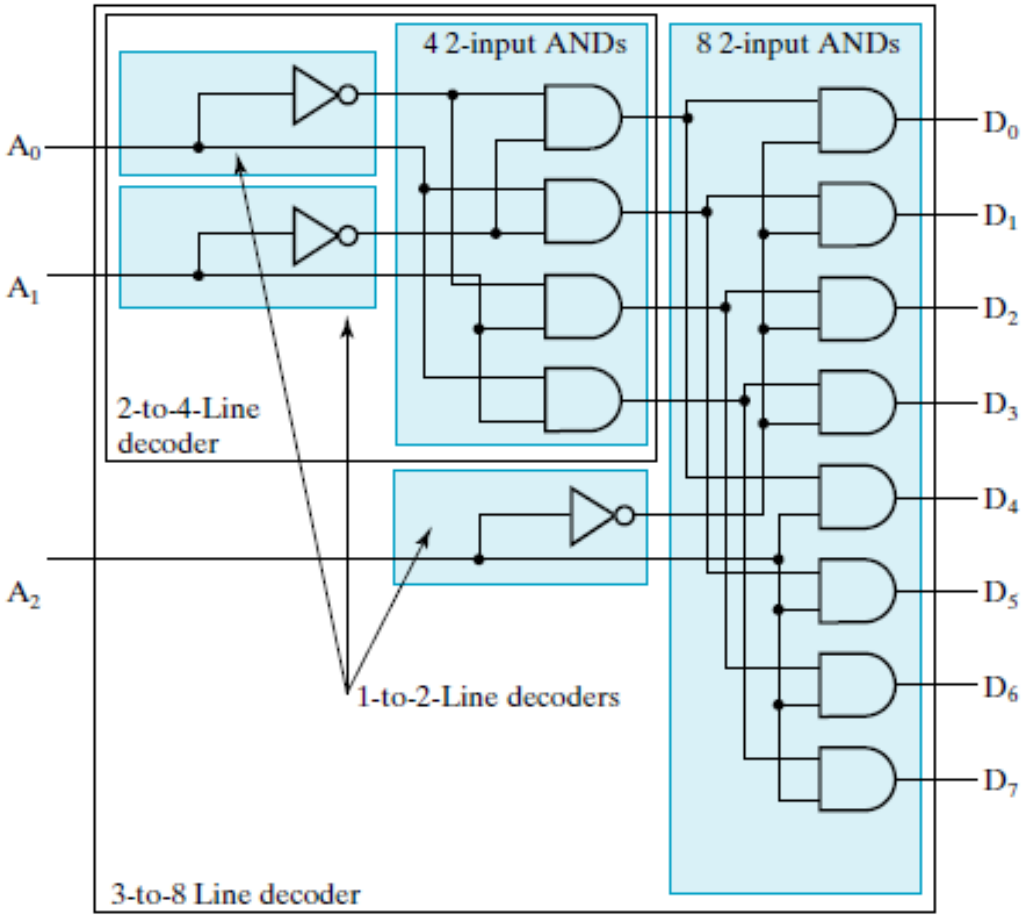
(b)

- **Note that the 2-4-line made up of 2 1-to-2-line decoders and 4 AND gates.**

解碼器的擴展

Decoder Expansion - Example 1

- **Result**



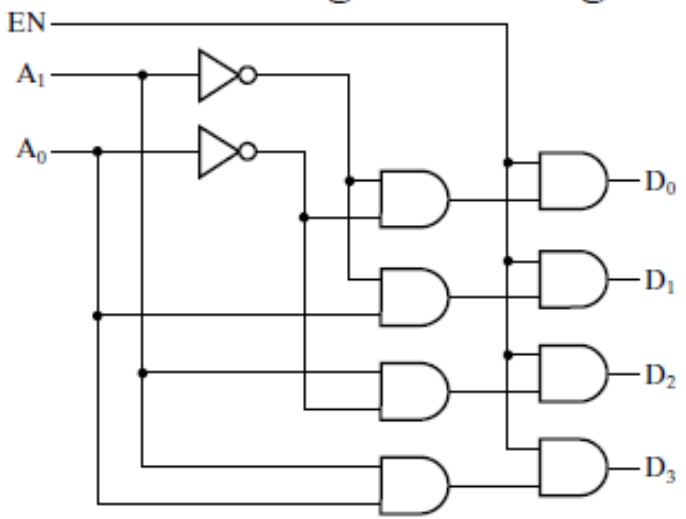
有 Enable 的解碼器

Decoder with Enable

- In general, attach *m*-enabling circuits to the outputs
- See truth table below for function
  - Note use of X's to denote both 0 and 1
  - Combination containing two X's represent four binary combinations
- Alternatively, can be viewed as distributing value of signal EN to 1 of 4 outputs
- In this case, called a *demultiplexer*

EN	A_1	A_0	D_0	D_1	D_2	D_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

(a)



(b)

Priority Encoder Example

- Priority encoder with 5 inputs (D_4, D_3, D_2, D_1, D_0) - highest priority to most significant 1 present - Code outputs A2, A1, A0 and V where V indicates at least one 1 present.

No. of Min-terms/Row	Inputs					Outputs			
	D4	D3	D2	D1	D0	A2	A1	A0	V
1	0	0	0	0	0	X	X	X	0
1	0	0	0	0	1	0	0	0	1
2	0	0	0	1	X	0	0	1	1
4	0	0	1	X	X	0	1	0	1
8	0	1	X	X	X	0	1	1	1
16	1	X	X	X	X	1	0	0	1

- Xs in input part of table represent 0 or 1; thus table entries correspond to product terms instead of minterms. The column on the left shows that all 32 minterms are present in the product terms in the table

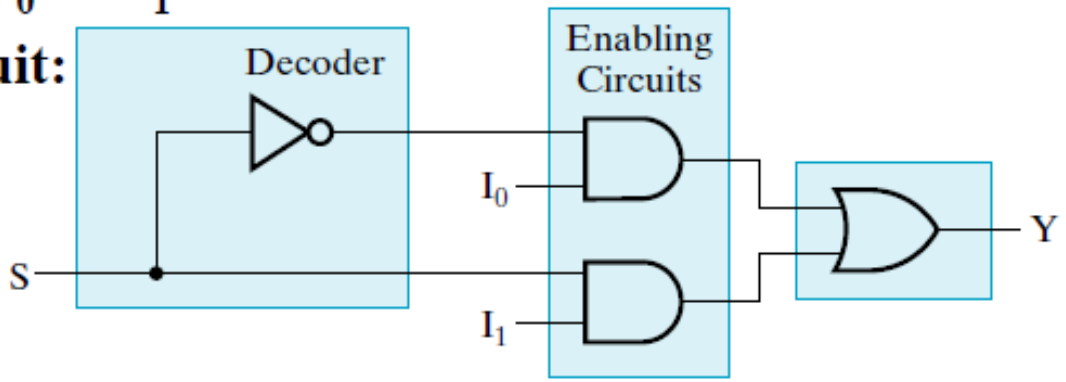
2 對 1 多工器

2-to-1-Line Multiplexer

- Since $2 = 2^1$, $n = 1$
- The single selection variable S has two values:
  - S = 0 selects input I_0
  - S = 1 selects input I_1
- The equation:

$$Y = \overline{S}I_0 + SI_1$$

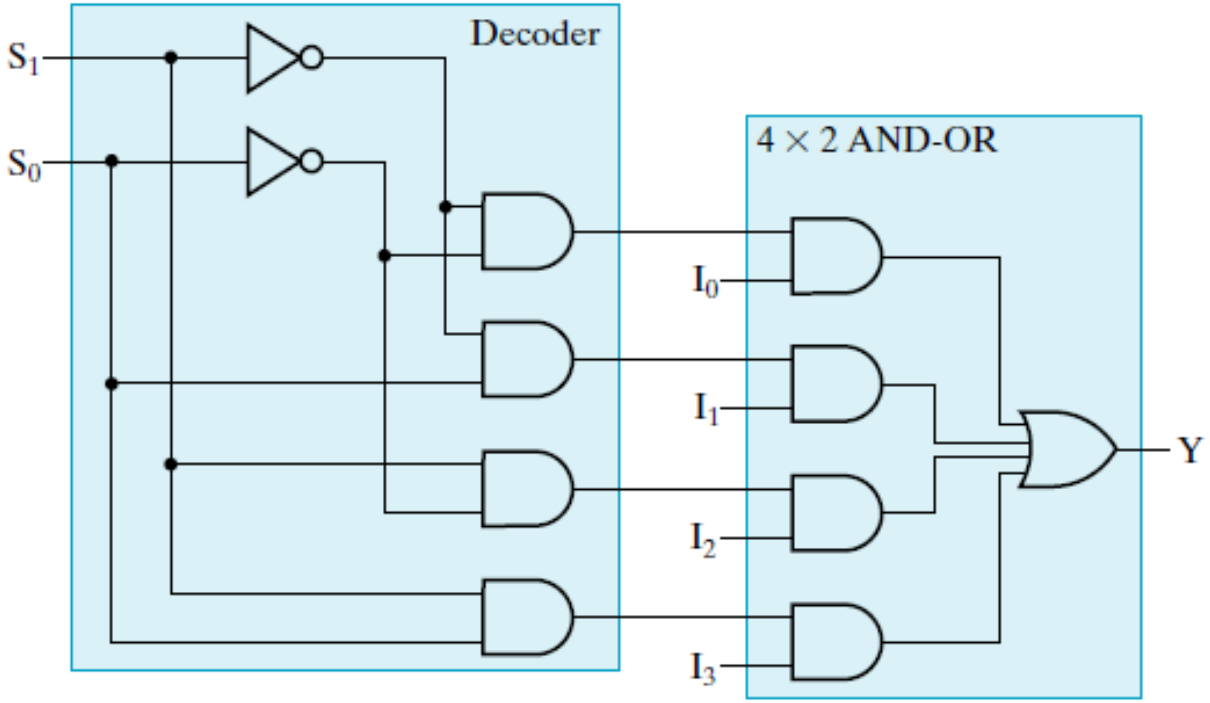
- The circuit:



4 對 1 多工器

Example: 4-to-1-line Multiplexer

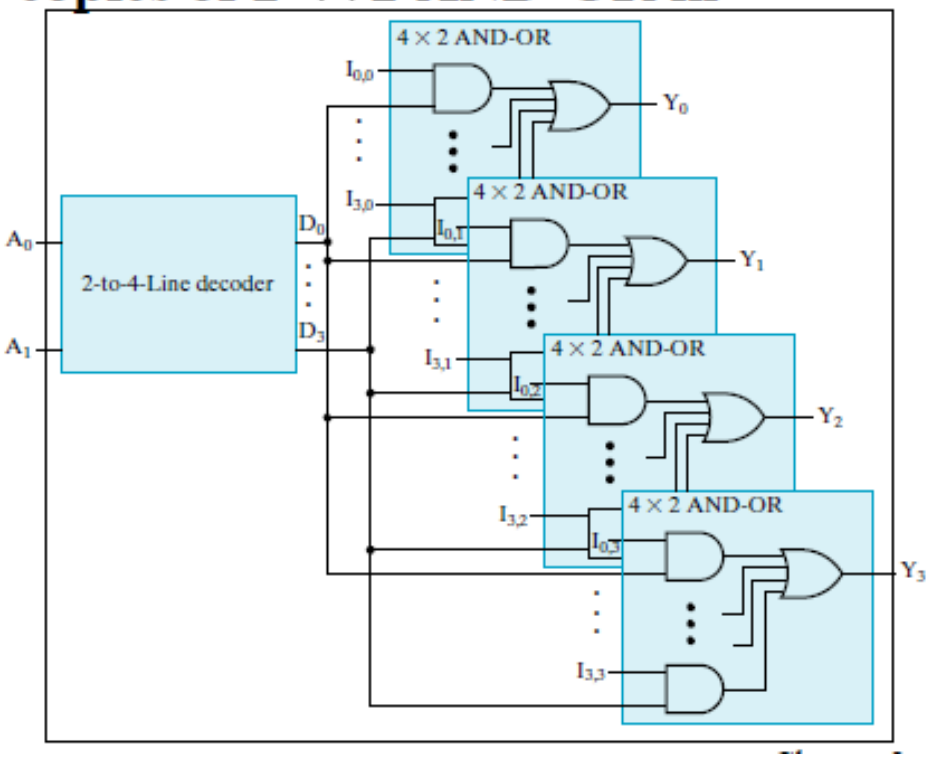
- 2-to-2^2-line decoder
- $2^2 \times 2$ AND-OR



多工器的擴展

Multiplexer Width Expansion

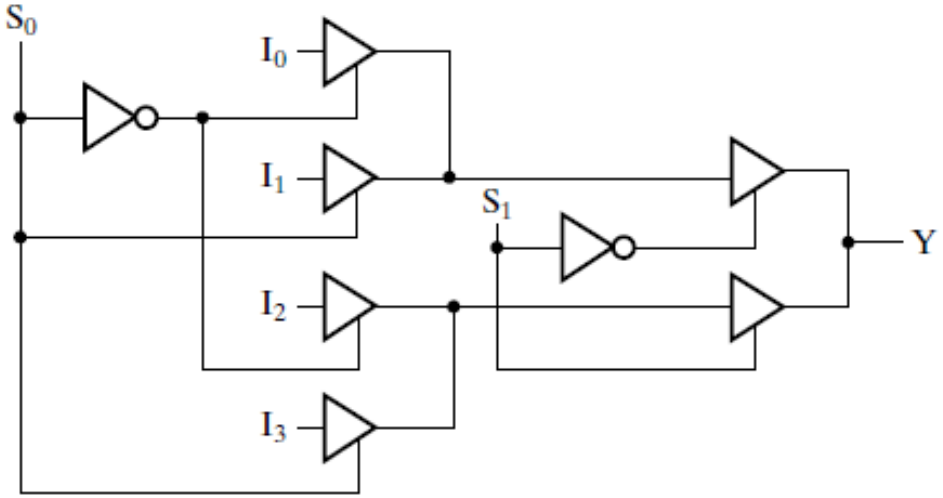
- Select "vectors of bits" instead of "bits"
- Use multiple copies of $2^n \times 2$ AND-OR in parallel
- Example: 4-to-1-line quad multi-plexer



使用三態緩衝器實作

Other Selection Implementations

- **Three-state logic in place of AND-OR**



(b)

- **Gate input cost = 14 compared to 22 (or 18) for gate implementation**

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