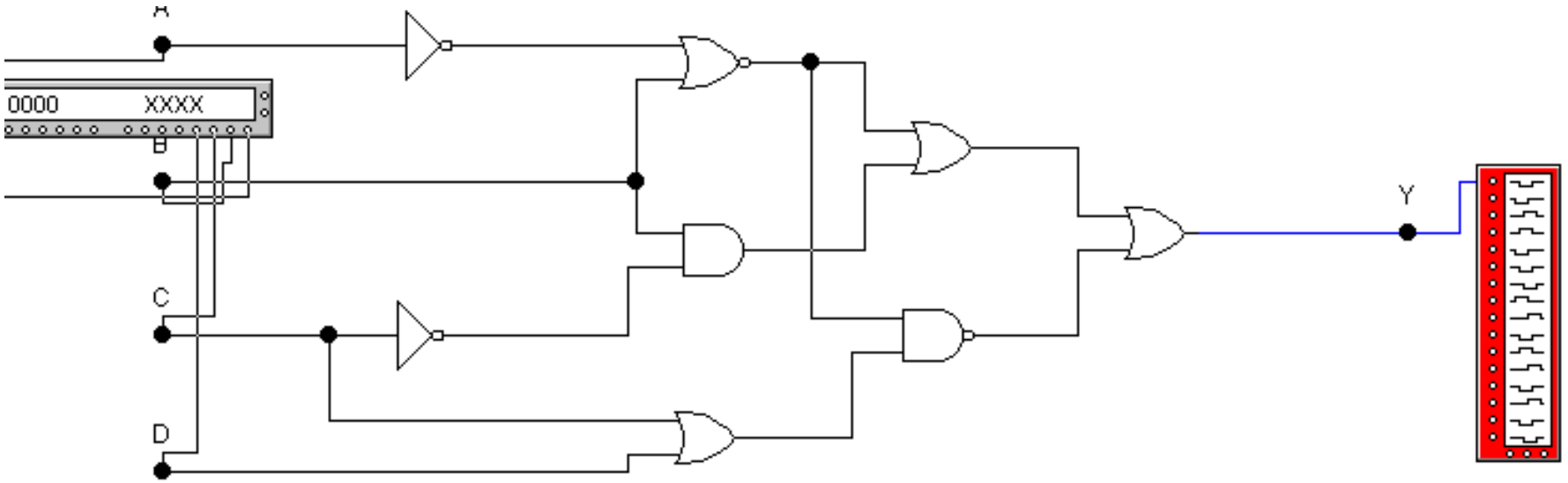
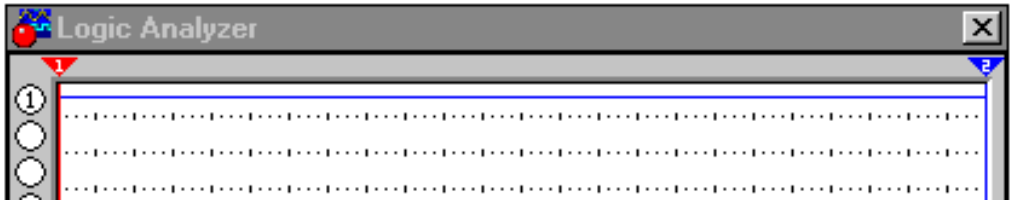
計算機結構
（數位邏輯與電子學）

陳鍾誠 於金門大學

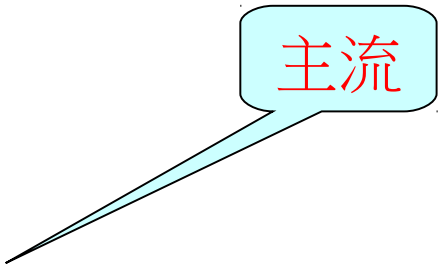
邏輯閘





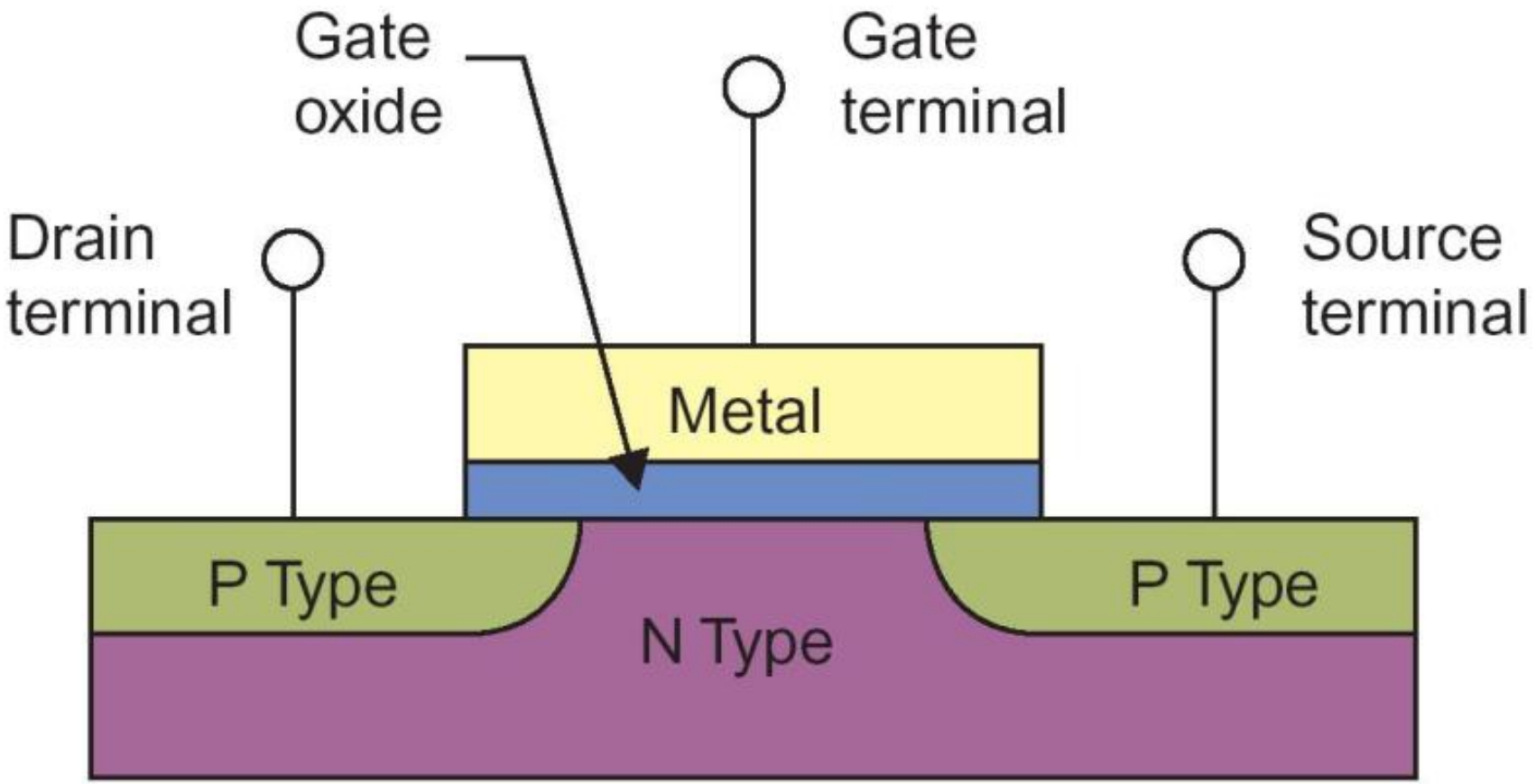
邏輯閘是由電晶體所組成的

- 電晶體
  - 類型
    - 雙極接面電晶體 （TTL 、 ECL）
    - 金氧半導體場效電晶體 （MOSFET）

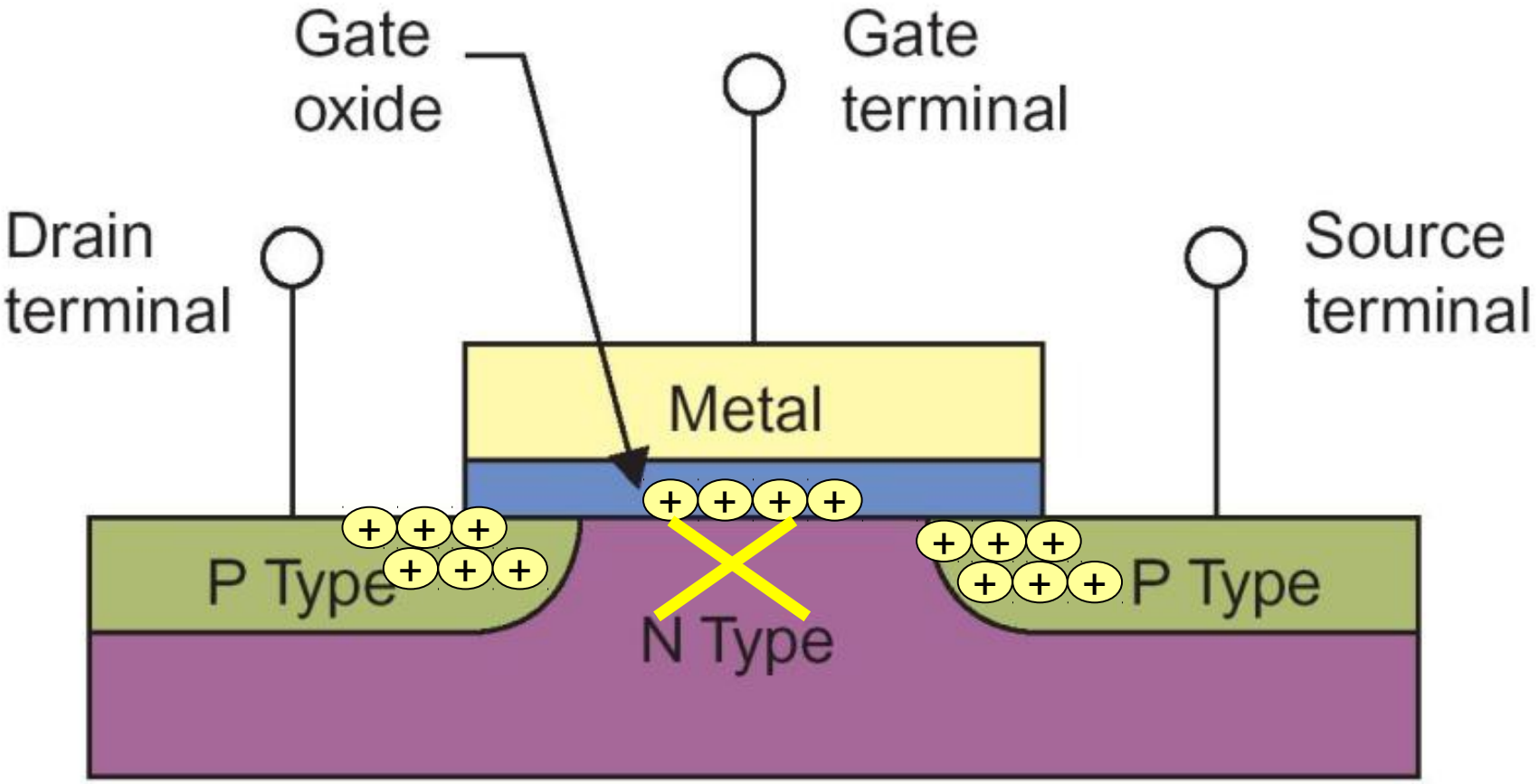


  - 特徵
    - 某些狀況下、電會流過、某些狀況下不會。
      - 穿遂效應。

MOSFET

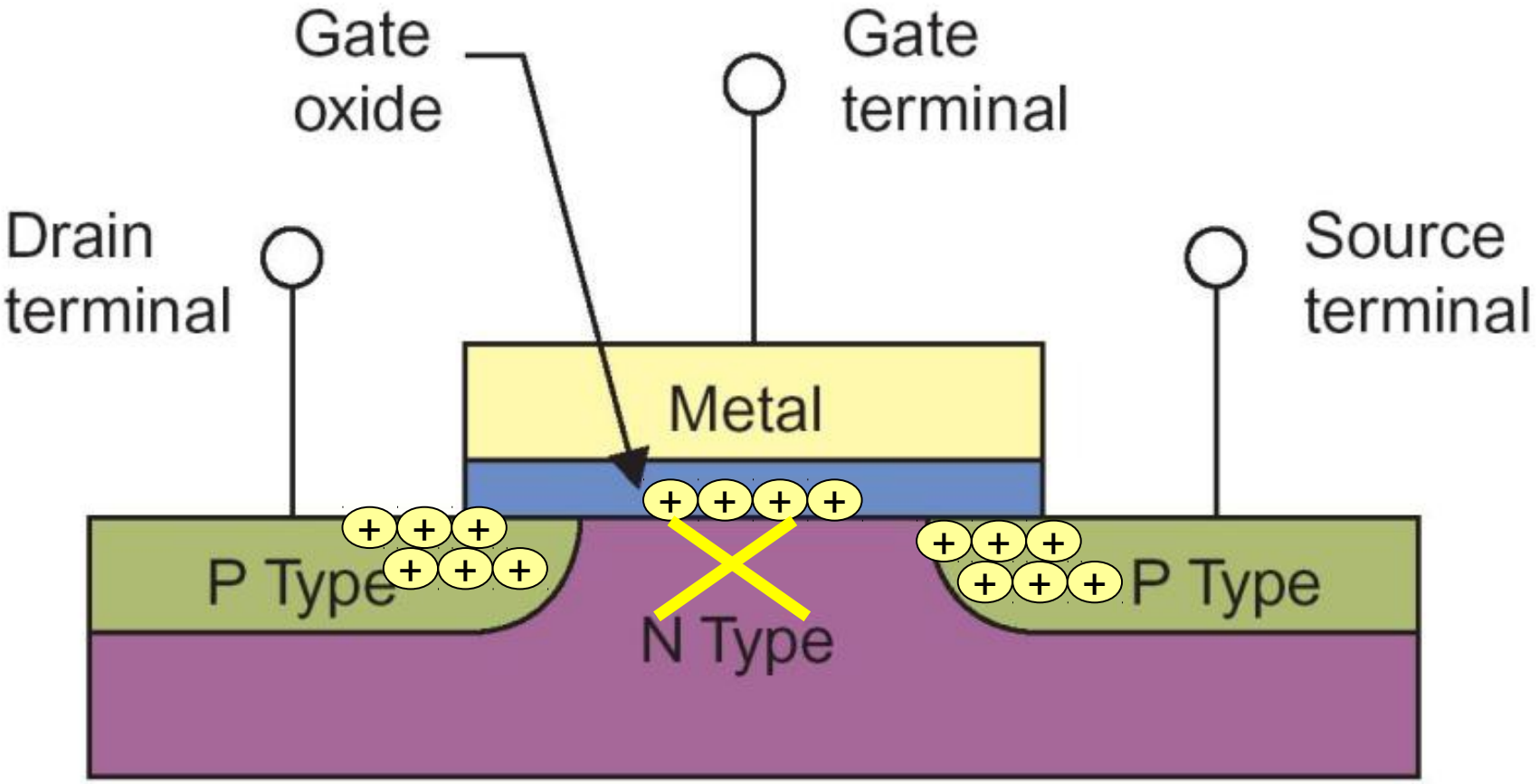

Gate
oxide
Gate
terminal
Drain
terminal
Source
terminal
Metal
P Type
P Type
N Type

P-Channel MOSFET ： 斷路狀態



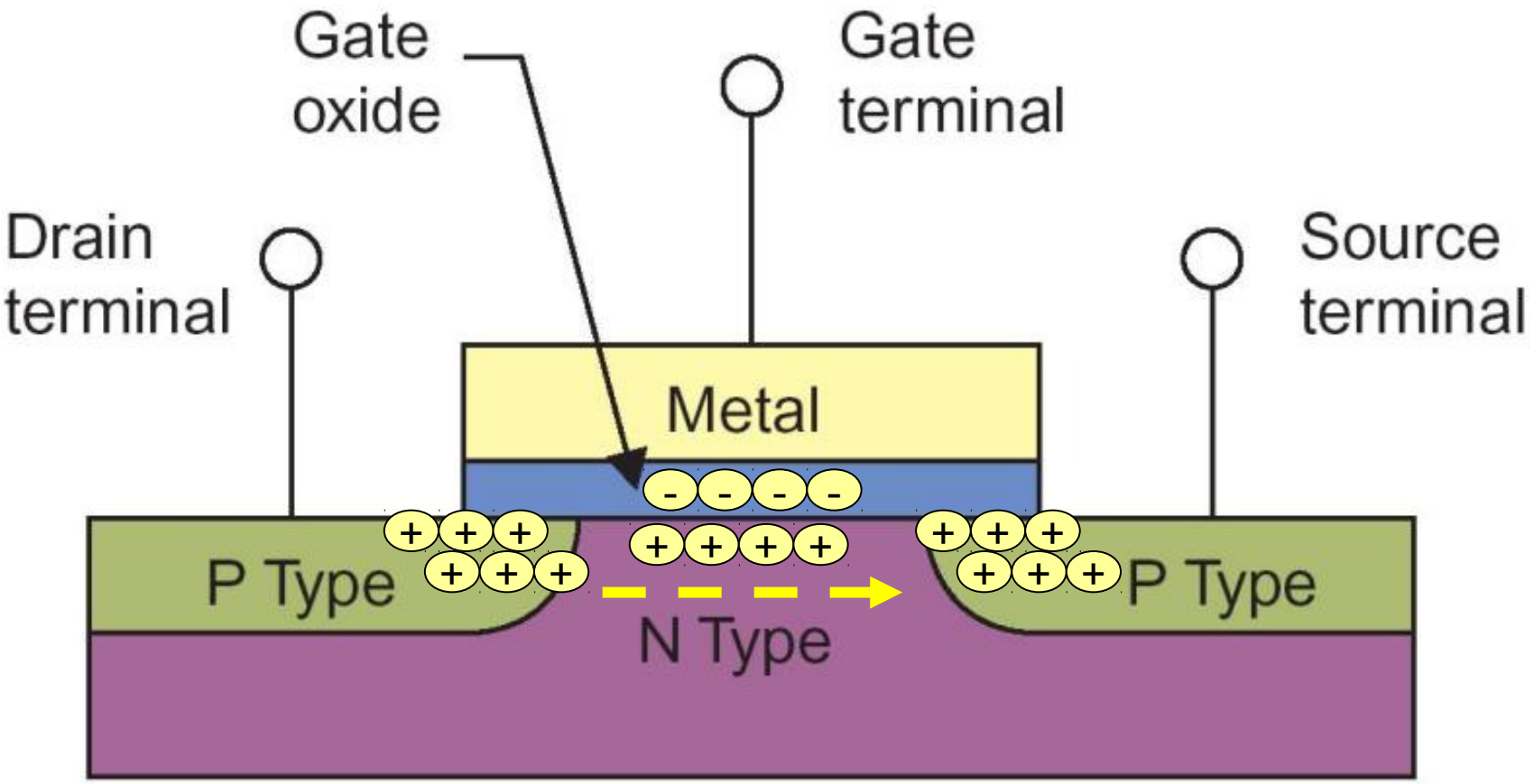
因為正電對正電排斥，正電進不來 ，因此不通。

P-Channel MOSFET ： 斷路狀態



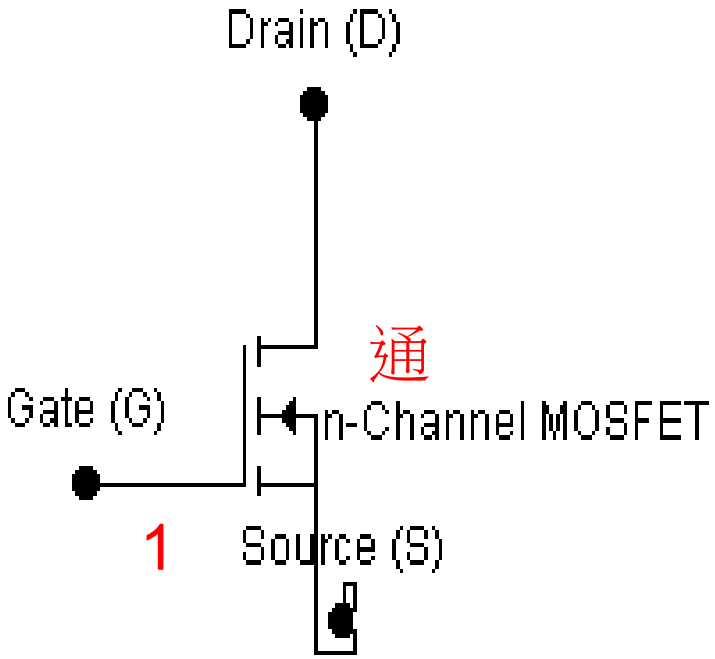
因為正電對正電排斥，正電進不來 ，因此不通。

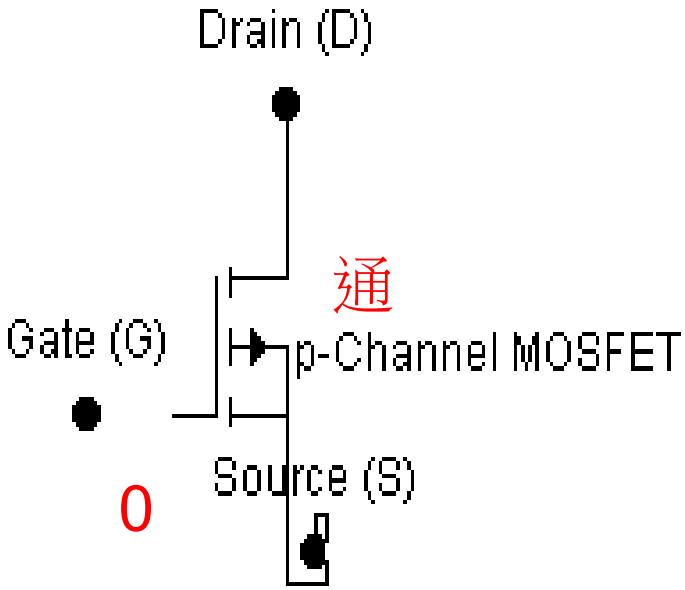
P-Channel MOSFET ： 通路狀態



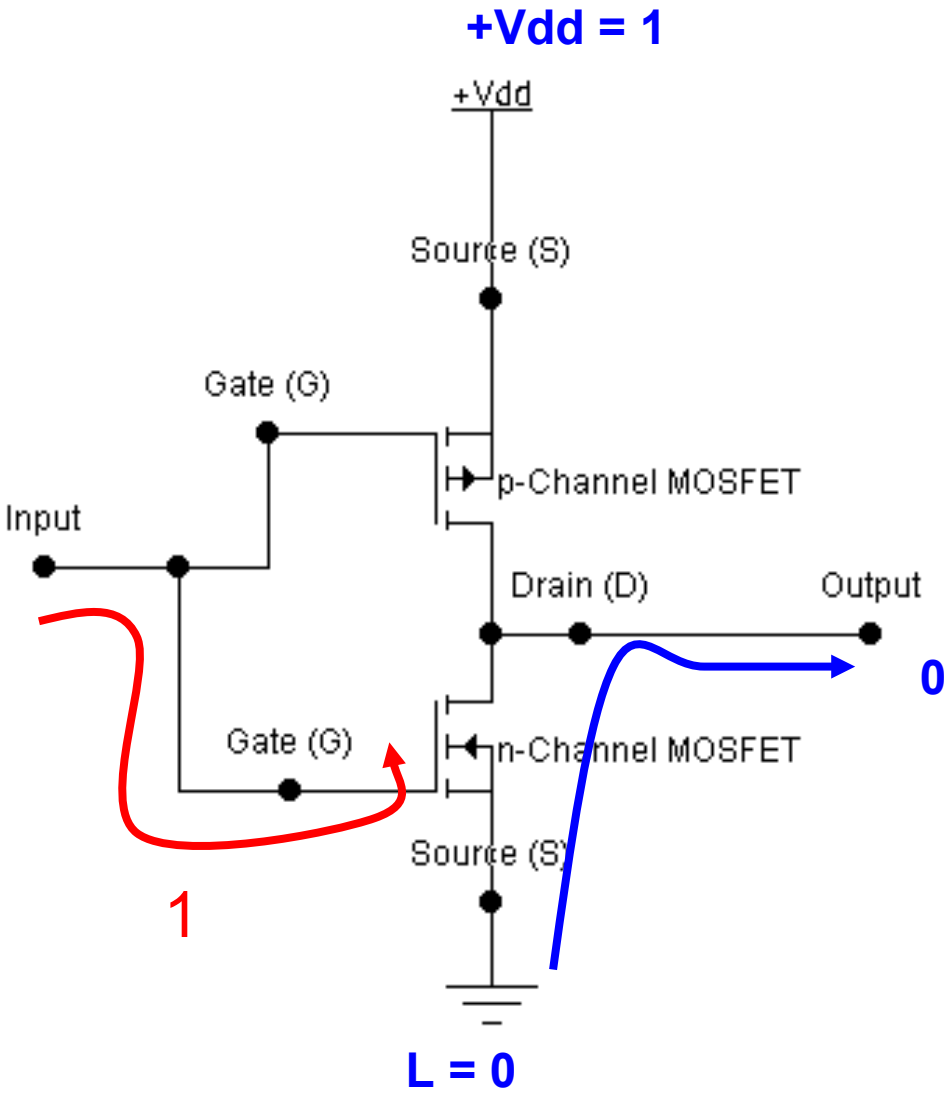
因為負電吸引下，正電穿過 N 型矽，通了，稱為穿隧效應。

P-Channel v.s. N-Channel

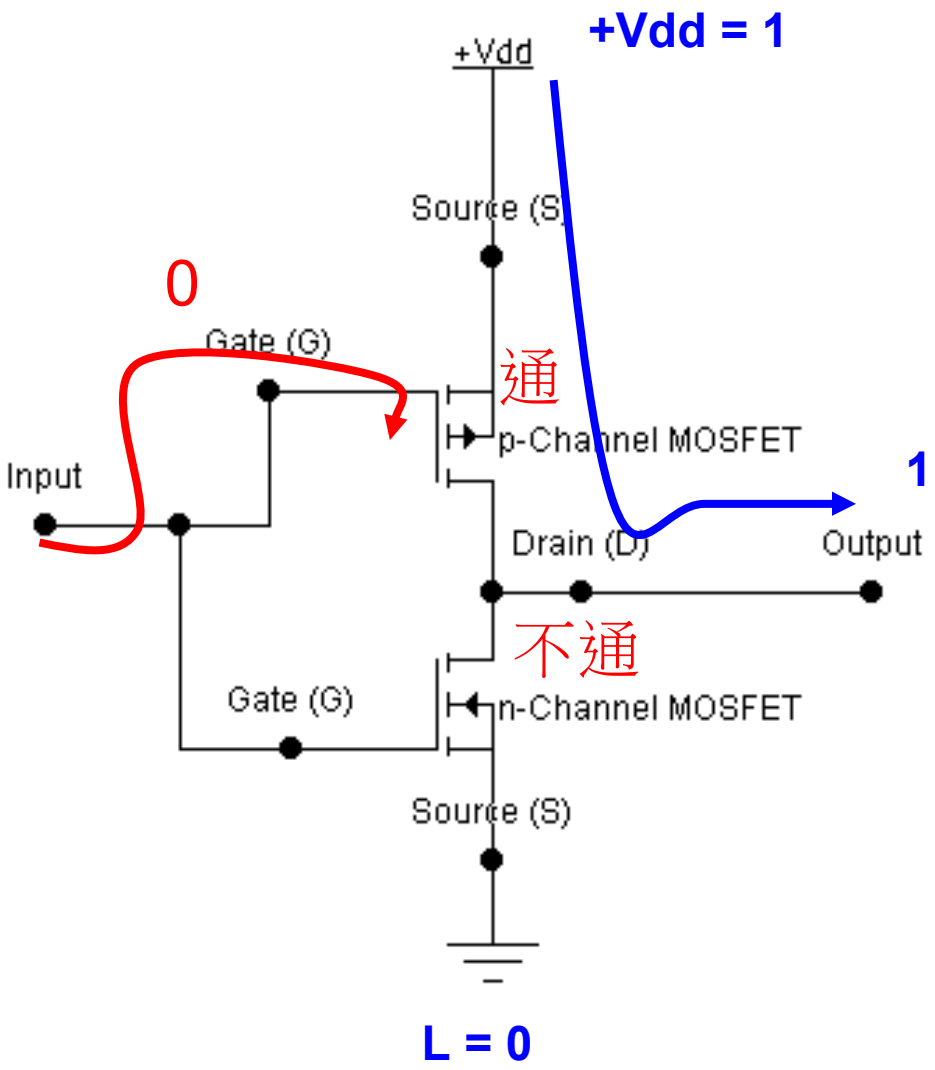




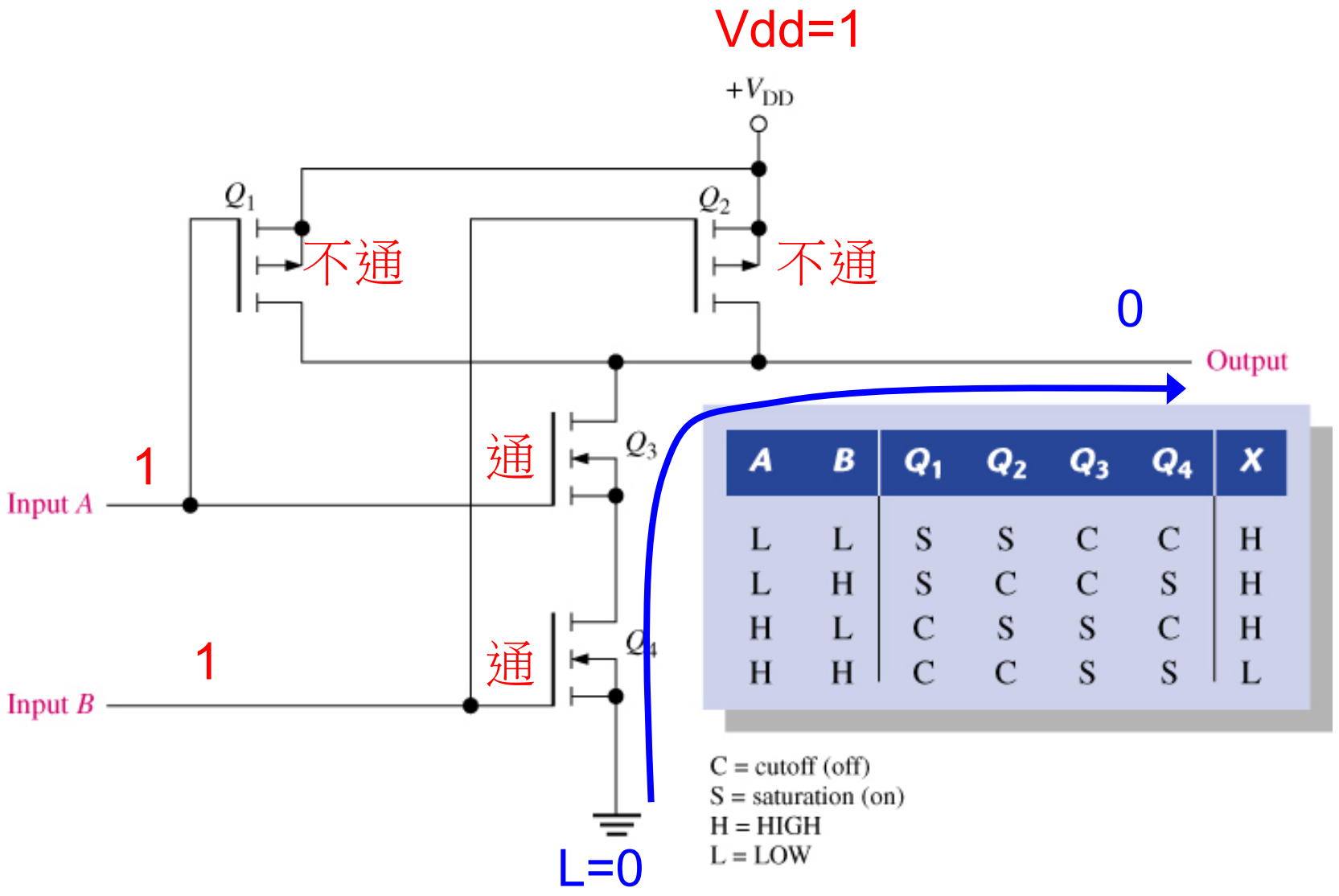
CMOS Inverter (not)



CMOS Inverter (not)



CMOS NAND

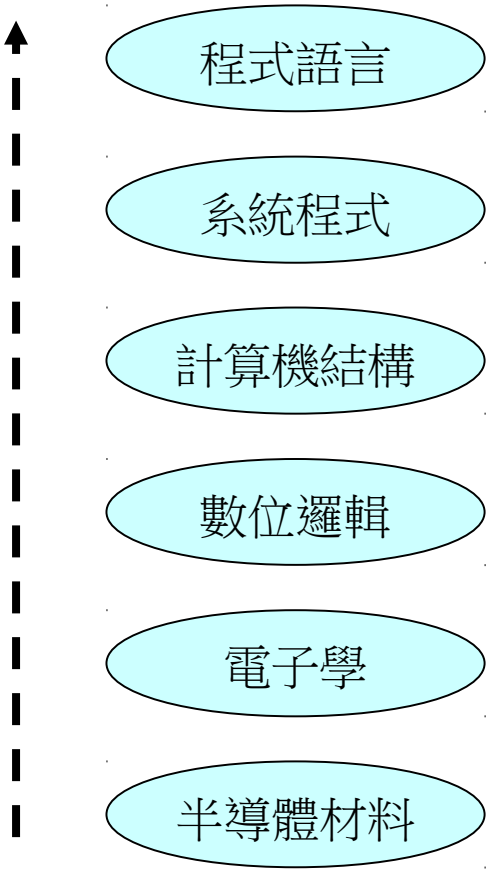


A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	H
H	L	C	S	S	C	H
H	H	C	C	S	S	L

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

結語

- 資工系的硬體課程都學完了
- 對硬體有興趣的同學請到電子系修電子學與計算機結構！
- 對系統軟體有興趣的同學請修系統程式與作業系統 ！



計算機結構 – 邏輯電路的背後

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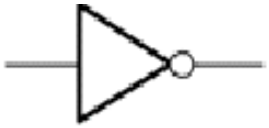
邏輯閘

- AND

- OR

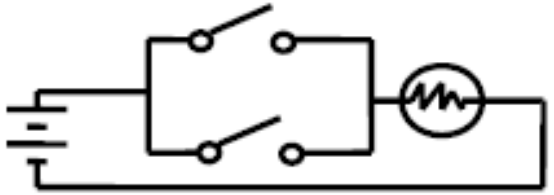
- NOT



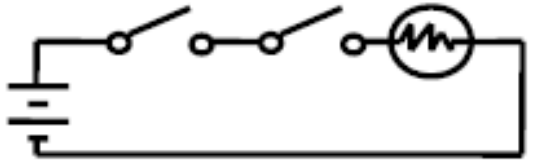
Logic Function Implementation

- **Using Switches**
  - For inputs:
    - logic 1 is switch closed
    - logic 0 is switch open
  - For outputs:
    - logic 1 is light on
    - logic 0 is light off.
  - NOT uses a switch such that:
    - logic 1 is switch open
    - logic 0 is switch closed

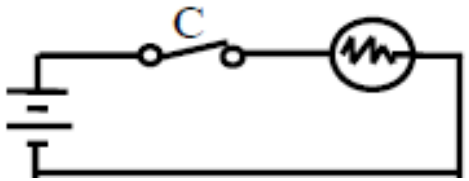
Switches in parallel => OR



Switches in series => AND

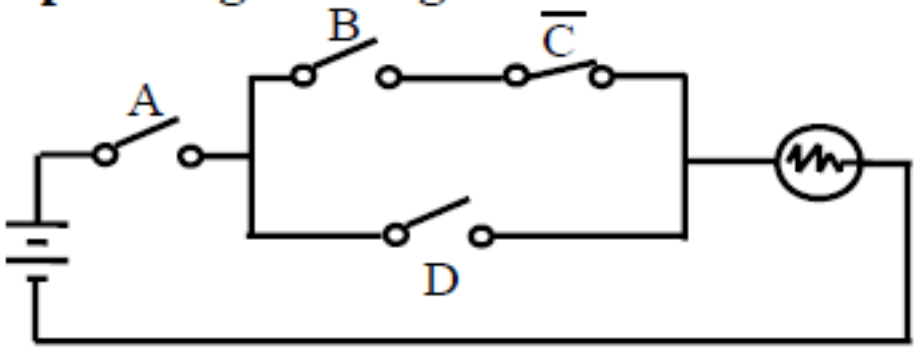


Normally-closed switch => NOT



Logic Function Implementation (Continued)

- **Example: Logic Using Switches**



- **Light is on (L = 1) for**

  L(A, B, C, D) =

  and off (L = 0), otherwise.

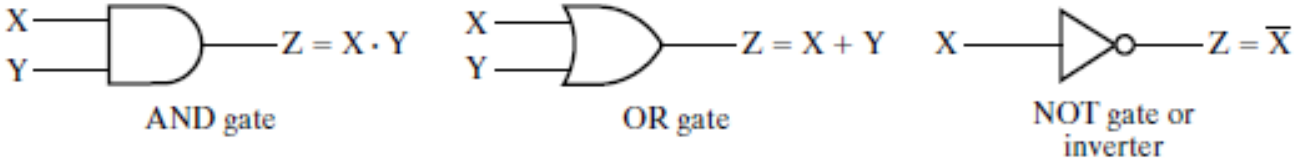
- **Useful model for relay circuits and for CMOS gate circuits, the foundation of current digital logic technology**

Logic Gates

- In the earliest computers, switches were opened and closed by magnetic fields produced by energizing coils in *relays*. The switches in turn opened and closed the current paths.
- Later, *vacuum tubes* that open and close current paths electronically replaced relays.
- Today, *transistors* are used as electronic switches that open and close current paths.
- Optional: Chapter 6 – Part 1: The Design Space

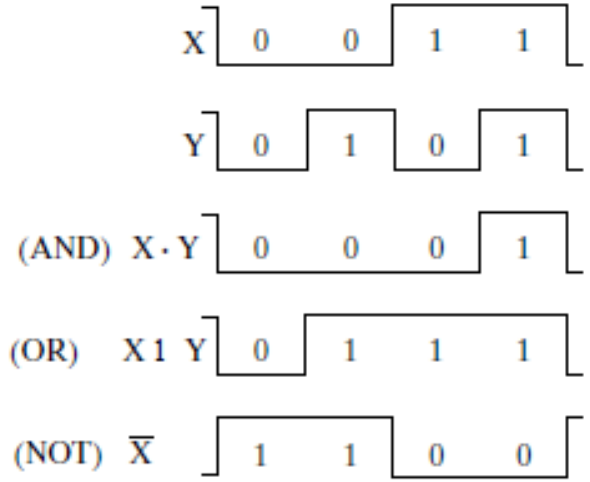
Logic Gate Symbols and Behavior

- **Logic gates have special symbols:**



(a) Graphic symbols

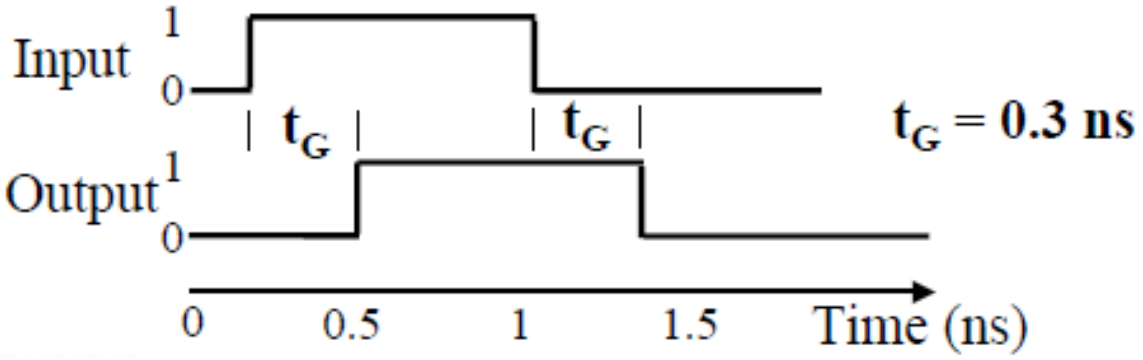
- **And waveform behavior in time as follows:**



(b) Timing diagram

Gate Delay

- In actual physical gates, if one or more input changes causes the output to change, the output change does not occur instantaneously.
- The delay between an input change(s) and the resulting output change is the *gate delay* denoted by t_G:



Logic Diagrams and Expressions

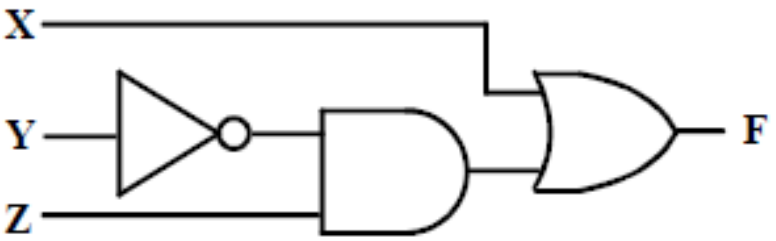
Truth Table

X Y Z	$F = X + \overline{Y} \cdot Z$
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

Equation

$$F = X + \overline{Y}\,Z$$

Logic Diagram



- **Boolean equations, truth tables and logic diagrams describe the same function!**
- **Truth tables are unique; expressions and logic diagrams are not. This gives flexibility in implementing functions.**

Boolean Algebra

- **An algebraic structure defined on a set of at least two elements, B, together with three binary operators (denoted +, · and ¯) that satisfies the following basic identities:**

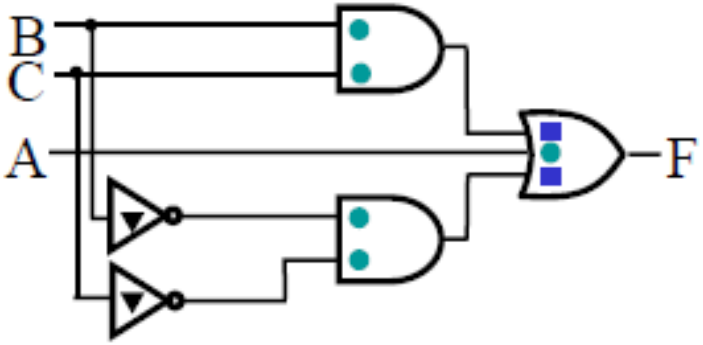
1.	$X + 0 = X$	2.	$X \cdot 1 = X$
3.	$X + 1 = 1$	4.	$X \cdot 0 = 0$
5.	$X + X = X$	6.	$X \cdot X = X$
7.	$X + \overline{X} = 1$	8.	$X \cdot \overline{X} = 0$
9.	$\overline{\overline{X}} = X$		

10.	$X + Y = Y + X$	11.	$XY = YX$	Commutative
12.	$(X + Y) + Z = X + (Y + Z)$	13.	$(XY)Z = X(YZ)$	Associative
14.	$X(Y + Z) = XY + XZ$	15.	$X + YZ = (X + Y)(X + Z)$	Distributive
16.	$\overline{X + Y} = \overline{X} \cdot \overline{Y}$	17.	$\overline{X \cdot Y} = \overline{X} + \overline{Y}$	DeMorgan's

Cost Criteria (continued)

- Example 1:
- $F = A + BC + \overline{B}\,\overline{C}$

GN = G + 2 = 9
L = 5
G = L + 2 = 7



- L (literal count) counts the AND inputs and the single literal OR input.
- G (gate input count) adds the remaining OR gate inputs
- GN(gate input count with NOTs) adds the inverter inputs

Cost Criteria (continued)

- Example 2:
- $F = A\,B\,C + \bar{A}\bar{B}\,\bar{C}$
- L = 6 G = 8 GN = 11
- $F = (A + \bar{C})(\bar{B} + C)(\bar{A} + B)$
- L = 6 G = 9 GN = 12
- Same function and same literal cost
- But first circuit has better gate input count and better gate input count with NOTs
- Select it!