



Process and Device Specification

XT018 - 0.18 µm HV SOI CMOS

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1. Introduction

1. Introduction

1.1 Related documents

Note: The specification documents listed in the table below do not contain information which is additional to that available in the SpecXplorer.

Description	Document number
Design Rule Specification XT018 - 0.18 µm HV SOI CMOS	DR_018_06
PCM Acceptance Specification XT018 - 0.18 µm HV SOI CMOS	PAS_018_06
Process Reliability Specification XT018 - 0.18 µm HV SOI CMOS	PR_018_06

Note: Additional available specifications:

Design Rule Specification 0.18µm MIM Antenna Rules DR_018_10

Note: Note that additional documents and application notes related to this process family can be found in the relevant document container at "my X-FAB", under "[Process Selection Documents](#)" and "[Technical Documents](#)"

Note: Users may also wish to use the RelXplorer interactive application. This can provide information about device and layer reliability according to application specific mission profiles. For access to this see <https://relxplorer.xfab.com/>

1.2 General notes

The specification describes parameters of the wafer process and of the available primitive devices. Data is provided for information to assist integrated circuit product development, especially for circuit design. This data can be seen in the columns Low/Typ/High.

Dispositional pass/fail parameters, which are used in the PCM test to check wafer electrical conformance prior to shipment, are also shown, in the columns LSL/USL.

Characteristic curves of the primitive devices showing measurement results of a typical wafer in comparison to the SPICE model simulations are available in the [Device Characteristics Documentation](#) (formerly Model Guides) on "my X-FAB".

The specification values have been obtained during the pre-production phase of the processes.

This specification is valid excluding a process specific area around the wafer edge of 5mm width. In the affected area, the function, parameters and reliability of the structures are not guaranteed.

1.3 Support

Technical questions should be directed to:

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email:	hotline@xfab.com	fax:	+49 361 427-6631

1.4 SpecXplorer

All of the data in this specification document is also available online via the SpecXplorer website. For access to this, see <http://specxplorer.xfab.com>.

2. General

2. General

2.1 Process modules

For the process family, two main modules exist. One of the main modules must be chosen. This can then be combined with one or more additional modules. Please also refer to the tables showing the required and forbidden modules, because:

- some modules are only available in combination with other modules,
- some modules are not available in combination with other modules.

For a complete list of available metal layer combinations, refer to the table below:

Metal Options

number of metals	Available Metal Layer Combinations	Module name (main=LP5MOS or MOS5)
3	MET1-MET2-METTP	main+METMID
4	MET1-MET2-MET3-METTP	main+MET3+METMID
4	MET1-MET2-MET3-METTPL	main+MET3+METTHK
4	MET1-MET2-METTP-METTPL	main+METMID+METTHK
5	MET1-MET2-MET3-MET4-METTP	main+MET3+MET4+METMID
5	MET1-MET2-MET3-MET4-METTPL	main+MET3+MET4+METTHK
5	MET1-MET2-MET3-METTP-METTPL	main+MET3+METMID+METTHK
5	MET1-MET2-MET3-METTP-METCOP	main+MET3+METMID+THKCOP
5	MET1-MET2-MET3-METTPL-METCOP	main+MET3+METTHK+THKCOP
6	MET1-MET2-MET3-METTP-METTPL-METCOP	main+MET3+METMID+METTHK+THKCOP
6	MET1-MET2-MET3-MET4-MET5-METTP	main+MET3+MET4+MET5+METMID
6	MET1-MET2-MET3-MET4-MET5-METTPL	main+MET3+MET4+MET5+METTHK
6	MET1-MET2-MET3-MET4-METTP-METTPL	main+MET3+MET4+METMID+METTHK

2.1.1 Main modules

Name	No. of masks	Description	Typical devices, applications
LP5MOS	19	1.8V / 5.0V low power CMOS module, single polysilicon, metal 1, metal 2	1.8V low power NMOS/ PMOS, 5.0V low power NMOS/ PMOS, well, polysilicon and metal resistors
MOS5	14	5.0V low power CMOS module, single polysilicon, metal 1, metal 2	5.0V low power NMOS/PMOS, well, polysilicon and metal resistors

Module restrictions for main modules

Name	Required modules	Forbidden modules
LP5MOS	METMID or (MET3 and METTHK)	MOS5
MOS5	METMID or (MET3 and METTHK)	LP5MOS

2.1.2 Additional modules for LP5MOS main module

Name	No. of masks	Description	Typical devices, applications
MET3	2	3-metal module, additional via2/metal 3 layers	more complex wiring



2. General → 2.1 Process modules→ 2.1.2 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
MET4	2	4-metal module, additional via3/metal 4 layers	more complex wiring
MET5	2	5-metal module, additional via4/metal 5 layers	more complex wiring
METMID	2	top metal module, additional top metal & via layers	more complex wiring
METTHK	2	thick metal module, additional thick metal and thick via layers	power distribution
THKCOP	1	thick copper module	thick copper redistribution layer
	Note: Halogen free mold compound is strongly recommended to avoid the surface leakage. Only full wafer thickness is acceptable for THKCOP module (i.e. grinding has to be done afterwards). No ink dots is allowed, probe marks on chips are not recommended.		
HRPOLY	1	high resistance polysilicon module	lightly N-doped Polysilicon resistor
	Note: When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.		
MRPOLY	1	medium resistance polysilicon module	lightly P-doped Polysilicon resistor
DTI	1	deep trench isolation module	complete dielectric isolation for high and low side operation, 10V drain extension NMOS/ PMOS and well resistor
PSUB	1	sub block module	1.8V / 5.0V PNP bipolar transistors
LVT	2	1.8V low Vt module	1.8V low Vt NMOS and PMOS
SVT	2	1.8V medium Vt module	1.8V medium Vt NMOS and PMOS
BJTA	1	bipolar module	5V / 25V PNP bipolar transistor
BJTC	1	bipolar module	5V / 25V NPN bipolar transistor
DEPL	1	depletion module	5.0V / 20V / 32V / 40V depletion NMOS and Low Ron 40V depletion NMOS
HVDEPL	1	High voltage depletion module	85V / 125V depletion NMOS
1XN	1	Gen1 super-junction NDMOS module	100V / 140V / 200V SJNP HV NMOS and SJNP diode
1XP	1	Gen1 super-junction PDMOS module	100V / 140V / 200V SJPN HV PMOS
2XP	2	Gen2 Low Ron super-junction high voltage PMOS module	115V / 140V / 155V / 195V / 235V SJ2XP HV PMOS
DNC	1	DNC module	6.0V/7.0V P-Type protection diode, additional NWELL1 implant into NWELL2
	Note: When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.		
DPC	1	DPC module	7.0V N-type protection diode, additional PWELL1 implant into PWELL2
	Note: When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.		
HVN	1	Deep n-well module	1.8V/ 5.0V trench isolated PMOS, 5.0V schottky diode, 6.0V/7.0V P-type protection diode and 5.0V rectifier p+/n diode, additional HVNWELL implant for SJ MOS
HVP	1	Deep p-well module	additional HVPWELL implant for SJ MOS
HWC	1	handle wafer contact module	top side handle wafer contact
NBUF	1	n-buffer module	200V SJNP NIGBT
NBUR	1	n-buried handle wafer diode module	high voltage handle wafer diodes
NHVA	2	high voltage NMOS module	40V / 60V NMOS, Low Ron 40V NMOS and 40V / 60V rectifier diode
	Note: When this module is chosen in combination with DIODEA or NHVR module, the combined additional mask count is reduced by one.		



2. General → 2.1 Process modules→ 2.1.2 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
NHVR	3	high voltage NMOS module	40V / 60V / 70V / 85V / 100V / 125V NMOS and 70V / 85V / 100V / 125V rectifier diode
	Note: When this module is chosen in combination with PHVR module, the combined additional mask count is reduced by one.		
	Note: When this module is chosen in combination with DIODEA or NHVA module, the combined additional mask count is reduced by one.		
NMV	2	mid voltage NMOS module	12V / 15V / 20V / 25V / 32V NMOS and 12V / 15V / 20V rectifier diode
PHVA	1	high voltage PMOS module	40V / 60V PMOS and Low Ron 40V PMOS
PHVR	2	high voltage PMOS module	40V / 60V / 70V / 85V / 100V / 125V PMOS
	Note: When this module is chosen in combination with NHVR module, the combined additional mask count is reduced by one.		
PMV	1	mid voltage PMOS module	12V / 18V / 25V / 32V PMOS
SJHVL	0	Gen2 super-junction modules <120V	45V / 72V / 95V / 115V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode, 2XP HV PMOS
SJHVM	0	Gen2 super-junction modules ≥120V and <250V	140V / 155V / 195V / 235V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode, 2XP HV PMOS
SJHVU	0	Gen2 super-junction modules >250V	290V / 375V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode
SJ1XN	1	Gen2 super-junction high voltage NMOS module	45V / 72V / 95V / 115V / 140V / 155V / 195V / 235V / 290V / 375V SJ1XN HV NMOS and diode
SJ1XP	1	Gen2 super-junction high voltage PMOS module	72V / 95V / 115V / 140V / 155V / 195V / 235V / 290V / 375V SJ1XP HV PMOS
DIODEA	1	diode a module	8V N-type protection diode
	Note: When this module is chosen in combination with NHVA or NHVR module, the combined additional mask count is reduced by one.		
DIODEB	1	diode b module	5.3V Zener diode
DIODEC	1	diode c module	5.3V Zener diode (DTI)
MIM	1	MIM capacitor module	MIM capacitor between metal top and metal layer underneath
MIM23	1	MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIM34	1	MIM capacitor module	MIM capacitor between metal 3 and metal 4
MIM45	1	MIM capacitor module	MIM capacitor between metal 4 and metal 5
DMIM	1	double MIM capacitor module	double MIM capacitor
DMIM3	1	double MIM capacitor module	double MIM capacitor between metal 3 and (metal 5 or metal top)
TMIM	1	triple MIM capacitor module	triple MIM capacitor
MIMH	1	single high capacitance MIM capacitor module	single high capacitance MIM capacitor
MIMH23	1	single high capacitance MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIMH34	1	high capacitance MIM capacitor module	MIM capacitor between metal 3 and metal 4
MIMH45	1	high capacitance MIM capacitor module	MIM capacitor between metal 4 and metal 5
DMIMH	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor
DMIMH3	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor between metal 3 and (metal 5 or metal top)

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2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	No. of masks	Description	Typical devices, applications
TMIMH	1	triple high capacitance MIM capacitor module	triple high capacitance MIM capacitor
CSP5L	0	MOM capacitor module	MOM capacitor >250V
CEEPROM	0	EEPROM memory module	ready to use EEPROM memory blocks
Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.			
NVM	4	non volatile memory module (SONOS based)	ready-to-use FLASH and EEPROM blocks
Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.			
OTP5	0	One-Time Programmable memory module	ready to use OTP memory blocks
Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.			
BOTDIE	1	bottom dielectric	stress relief between copper and X-Fab's passivation, required for chip size >2mm*2mm or passivation topography >0.5µm
FLATPV	0	Flat passivation	Flat passivation, post process
SMALLPAD	0	Smaller passivation opening	Smaller passivation opening for bumping process
PIMIDE	1	polyimide module, resilient barrier layer on top of passivation	wafer overcoat for stress relief and passivation protection

Module restrictions for LP5MOS main module

Name	Required modules	Forbidden modules
MET3	-	-
MET4	MET3	THKCOP
MET5	MET4	(METMID and METTHK) or THKCOP
METMID	-	-
METTHK	MET3 or METMID	FLATPV
THKCOP	MET3 and BOTDIE	PIMIDE or MET4 or MET5 or SMALLPAD
HRPOLY	-	-
MRPOLY	-	-
DTI	-	-
PSUB	-	-
LVT	-	-
SVT	-	-
BJTA	DTI and PSUB	-
BJTC	DTI and PSUB	-
DEPL	-	-
HVDEPL	DTI and PSUB and NHVR	-
1XN	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR	-
1XP	DTI and PSUB and DNC and HVN and HVP and HWC and NBUR	-
2XP	DTI and PSUB and DNC and HVN and HWC and NBUR and (SJHVL or SJHVM)	-
DNC	-	-
DPC	-	-



2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	Required modules	Forbidden modules
HVN	DTI and PSUB	-
HVP	PSUB	-
HWC	DTI	-
NBUF	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR and 1XN	-
NBUR	HWC and DTI and HVN and PSUB	-
NHVA	DTI and PSUB	-
NHVR	DTI and PSUB	-
NMV	DTI	-
PHVA	DTI and PSUB	-
PHVR	DTI and PSUB	-
PMV	DTI and PSUB	-
SJHVL	SJ1XP or 2XP or SJ1XN or NBUR	-
SJHVM	SJ1XP or 2XP or SJ1XN or NBUR	-
SJHVU	SJ1XP or SJ1XN or NBUR	-
SJ1XN	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR and (SJHVL or SJHVM or SJHVU)	-
SJ1XP	DTI and PSUB and HVN and HWC and NBUR and DNC and (SJHVL or SJHVM or SJHVU)	-
DIODEA	PSUB	-
DIODEB	PSUB	-
DIODEC	DTI and PSUB	-
MIM	METMID	MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM23	MET3	MIM or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM34	MET4	MIM or MIM23 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM45	MET5	MIM or MIM23 or MIM34 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIM	MET4 or (MET3 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIM3	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
TMIM	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH	METMID or METTHK	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH23	MET3	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH

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2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	Required modules	Forbidden modules
MIMH34	MET4	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH45	MET5	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or DMIMH or DMIMH3 or TMIMH
DMIMH	MET4 or (MET3 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or TMIMH
DMIMH3	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or TMIMH
TMIMH	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3
CSP5L	MET4 and METMID and METTHK and NBUR	MET5
EEPROM	-	-
NVM	-	-
OTP5	-	-
BOTDIE	THKCOP	-
FLATPV	METMID	METTHK
SMALLPAD	-	PIMIDE or THKCOP
PIMIDE	-	THKCOP or SMALLPAD

2.1.3 Additional modules for MOS5 main module

Name	No. of masks	Description	Typical devices, applications
MET3	2	3-metal module, additional via2/metal 3 layers	more complex wiring
MET4	2	4-metal module, additional via3/metal 4 layers	more complex wiring
MET5	2	5-metal module, additional via4/metal 5 layers	more complex wiring
METMID	2	top metal module, additional top metal & via layers	more complex wiring
METTHK	2	thick metal module, additional thick metal and thick via layers	power distribution
THKCOP	1	thick copper module	thick copper redistribution layer
	Note: Halogen free mold compound is strongly recommended to avoid the surface leakage. Only full wafer thickness is acceptable for THKCOP module (i.e. grinding has to be done afterwards). No ink dots is allowed, probe marks on chips are not recommended.		
HRPOLY	1	high resistance polysilicon module	lightly N-doped Polysilicon resistor
	Note: When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.		
MRPOLY	1	medium resistance polysilicon module	lightly P-doped Polysilicon resistor
DTI	1	deep trench isolation module	complete dielectric isolation for high and low side operation, 10V drain extension NMOS/PMOS and well resistor
PSUB	1	sub block module	1.8V / 5.0V PNP bipolar transistors
BJTA	1	bipolar module	5V / 25V PNP bipolar transistor
BJTC	1	bipolar module	5V / 25V NPN bipolar transistor



2. General → 2.1 Process modules→ 2.1.3 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
DEPL	1	depletion module	5.0V / 20V / 32V / 40V depletion NMOS and Low Ron 40V depletion NMOS
HVDEPL	1	High voltage depletion module	85V / 125V depletion NMOS
1XN	1	Gen1 super-junction NDMOS module	100V / 140V / 200V SJNP HV NMOS and SJNP diode
1XP	1	Gen1 super-junction PDMOS module	100V / 140V / 200V SJPN HV PMOS
2XP	2	Gen2 Low Ron super-junction high voltage PMOS module	115V / 140V / 155V / 195V / 235V SJ2XP HV PMOS
DNC	1	DNC module	6.0V/7.0V P-Type protection diode, additional NWELL1 implant into NWELL2
Note: When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.			
DPC	1	DPC module	7.0V N-type protection diode, additional PWELL1 implant into PWELL2
Note: When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.			
HVN	1	Deep n-well module	1.8V/ 5.0V trench isolated PMOS, 5.0V schottky diode, 6.0V/7.0V P-type protection diode and 5.0V rectifier p+/n diode, additional HVNWELL implant for SJ MOS
HVP	1	Deep p-well module	additional HVPWELL implant for SJ MOS
HWC	1	handle wafer contact module	top side handle wafer contact
NBUF	1	n-buffer module	200V SJNP NIGBT
NBUR	1	n-buried handle wafer diode module	high voltage handle wafer diodes
NHVA	2	high voltage NMOS module	40V / 60V NMOS, Low Ron 40V NMOS and 40V / 60V rectifier diode
Note: When this module is chosen in combination with DIODEA or NHVR module, the combined additional mask count is reduced by one.			
NHVR	3	high voltage NMOS module	40V / 60V / 70V / 85V / 100V / 125V NMOS and 70V / 85V / 100V / 125V rectifier diode
Note: When this module is chosen in combination with PHVR module, the combined additional mask count is reduced by one.			
Note: When this module is chosen in combination with DIODEA or NHVA module, the combined additional mask count is reduced by one.			
NMV	2	mid voltage NMOS module	12V / 15V / 20V / 25V / 32V NMOS and 12V / 15V / 20V rectifier diode
PHVA	1	high voltage PMOS module	40V / 60V PMOS and Low Ron 40V PMOS
PHVR	2	high voltage PMOS module	40V / 60V / 70V / 85V / 100V / 125V PMOS
Note: When this module is chosen in combination with NHVR module, the combined additional mask count is reduced by one.			
PMV	1	mid voltage PMOS module	12V / 18V / 25V / 32V PMOS
SJHVL	0	Gen2 super-junction modules <120V	45V / 72V / 95V / 115V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode, 2XP HV PMOS
SJHVM	0	Gen2 super-junction modules ≥120V and <250V	140V / 155V / 195V / 235V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode, 2XP HV PMOS
SJHVU	0	Gen2 super-junction modules >250V	290V / 375V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode



2. General → 2.1 Process modules→ 2.1.3 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
SJ1XN	1	Gen2 super-junction high voltage NMOS module	45V / 72V / 95V / 115V / 140V / 155V / 195V / 235V / 290V / 375V SJ1XN HV NMOS and diode
SJ1XP	1	Gen2 super-junction high voltage PMOS module	72V / 95V / 115V / 140V / 155V / 195V / 235V / 290V / 375V SJ1XP HV PMOS
DIODEA	1	diode a module	8V N-type protection diode
		Note: When this module is chosen in combination with NHVA or NHVR module, the combined additional mask count is reduced by one.	
DIODEB	1	diode b module	5.3V Zener diode
DIODEC	1	diode c module	5.3V Zener diode (DTI)
MIM	1	MIM capacitor module	MIM capacitor between metal top and metal layer underneath
MIM23	1	MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIM34	1	MIM capacitor module	MIM capacitor between metal 3 and metal 4
MIM45	1	MIM capacitor module	MIM capacitor between metal 4 and metal 5
DMIM	1	double MIM capacitor module	double MIM capacitor
DMIM3	1	double MIM capacitor module	double MIM capacitor between metal 3 and (metal 5 or metal top)
TMIM	1	triple MIM capacitor module	triple MIM capacitor
MIMH	1	single high capacitance MIM capacitor module	single high capacitance MIM capacitor
MIMH23	1	single high capacitance MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIMH34	1	high capacitance MIM capacitor module	MIM capacitor between metal 3 and metal 4
MIMH45	1	high capacitance MIM capacitor module	MIM capacitor between metal 4 and metal 5
DMIMH	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor
DMIMH3	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor between metal 3 and (metal 5 or metal top)
TMIMH	1	triple high capacitance MIM capacitor module	triple high capacitance MIM capacitor
CSP5L	0	MOM capacitor module	MOM capacitor >250V
CEEPROM	0	EEPROM memory module	ready to use EEPROM memory blocks
		Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.	
OTP5	0	One-Time Programmable memory module	ready to use OTP memory blocks
		Note: For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.	
BOTDIE	1	bottom dielectric	stress relief between copper and X-Fab's passivation, required for chip size >2mm*2mm or passivation topography >0.5µm
FLATPV	0	Flat passivation	Flat passivation, post process
SMALLPAD	0	Smaller passivation opening	Smaller passivation opening for bumping process
PIMIDE	1	polyimide module, resilient barrier layer on top of passivation	wafer overcoat for stress relief and passivation protection

2. General → 2.1 Process modules → 2.1.3 Additional modules f... → Module restrictions ...

Module restrictions for MOS5 main module

Name	Required modules	Forbidden modules
MET3	-	-
MET4	MET3	THKCOP
MET5	MET4	(METMID and METTHK) or THKCOP
METMID	-	-
METTHK	MET3 or METMID	FLATPV
THKCOP	MET3 and BOTDIE	PIMIDE or MET4 or MET5 or SMALLPAD
HRPOLY	-	-
MRPOLY	-	-
DTI	-	-
PSUB	-	-
BJTA	DTI and PSUB	-
BJTC	DTI and PSUB	-
DEPL	-	-
HVDEPL	DTI and PSUB and NHVR	-
1XN	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR	-
1XP	DTI and PSUB and DNC and HVN and HVP and HWC and NBUR	-
2XP	DTI and PSUB and DNC and HVN and HWC and NBUR and (SJHVL or SJHVM)	-
DNC	-	-
DPC	-	-
HVN	DTI and PSUB	-
HVP	PSUB	-
HWC	DTI	-
NBUF	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR and 1XN	-
NBUR	HWC and DTI and HVN and PSUB	-
NHVA	DTI and PSUB	-
NHVR	DTI and PSUB	-
NMV	DTI	-
PHVA	DTI and PSUB	-
PHVR	DTI and PSUB	-
PMV	DTI and PSUB	-
SJHVL	SJ1XP or 2XP or SJ1XN or NBUR	-
SJHVM	SJ1XP or 2XP or SJ1XN or NBUR	-
SJHVU	SJ1XP or SJ1XN or NBUR	-
SJ1XN	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR and (SJHVL or SJHVM or SJHVU)	-
SJ1XP	DTI and PSUB and HVN and HWC and NBUR and DNC and (SJHVL or SJHVM or SJHVU)	-
DIODEA	PSUB	-
DIODEB	PSUB	-



2. General → 2.1 Process modules → 2.1.3 Additional modules f... → Module restrictions ...

Name	Required modules	Forbidden modules
DIODEC	DTI and PSUB	-
MIM	METMID	MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM23	MET3	MIM or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM34	MET4	MIM or MIM23 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM45	MET5	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIM	MET4 or (MET3 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIM3	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
TMIM	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH	METMID or METTHK	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH23	MET3	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH34	MET4	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH45	MET5	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or DMIMH or DMIMH3 or TMIMH
DMIMH	MET4 or (MET3 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIMH3	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or TMIMH
TMIMH	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3
CSP5L	MET4 and METMID and METTHK and NBUR	MET5
CEEPROM	-	-
OTP5	-	-
BOTDIE	THKCOP	-
FLATPV	METMID	METTHK
SMALLPAD	-	PIMIDE or THKCOP
PIMIDE	-	THKCOP or SMALLPAD

2. General → 2.2 Process flows

2.2 Process flows

2.2.1 for LP5MOS main module

WIP reference	Process step	Process modules
WAFERSTART	wafer start	LP5MOS
HWC	Handle Wafer Contact	HWC
NBUR	N-buried implant	NBUR
EPI	epitaxy	LP5MOS
ACTIVE	active	LP5MOS
DTI	Deep Trench Isolation	DTI
SUB	SUB implant	LP5MOS
DFN	N-type drift implant	NHVR, PHVR
PDD	P-type drift implant	NHVR
DFP	P-type drift implant	PHVR
NDFMV	N-drift extension implant	NMV
PDFMV	P-drift extension implant	PMV
HVPW	HVPWELL	HVP
SJNP	SJNP implant	1XN
ESDMV	ESD implant for medium voltage	NMV
HVNW	HVNWELL	HVN
2XP	2X SJPN implant	2XP
SJPN	SJPN implant	1XP
NTOP	NTOP Implant	2XP
SJ1XN	1X SJNP implant	SJ1XN
SJ1XP	1X SJPN implant	SJ1XP
NBUF	NBUF implant	NBUF
NDF	N-drain extension implant	NHVA
PDF	P-drain extension implant	PHVA
NVM	non volatile memory	NVM
NPN	PBASE implant	BJTC
PNP	NBASE implant	BJTA
WELL2	5.0V wells	LP5MOS
PZN	PZENER implant	DIODEB
NZN	NZENER Implant	DIODEC
PW4	n DMOS pwell	NHVA, NHVR, DIODEA
WELL1	1.8V wells	LP5MOS
HVDEPL	HV depletion implant	HVDEPL
DEPL	depletion implant	DEPL
LVT	1.8V low Vt wells	LVT
SVT	1.8V medium Vt wells	SVT
GOX	1.8V gate oxide	LP5MOS
MVGOX	5.0V gate oxide	LP5MOS
POLY	poly silicon gate	LP5MOS
NLDD1	1.8V NMOS LDD	LP5MOS



2. General → 2.2 Process flows→ 2.2.1 for LP5MOS main mod...

WIP reference	Process step	Process modules
PLDD1	1.8V PMOS LDD	LP5MOS
NLDD2	5.0V NMOS LDD	LP5MOS
PLDD2	5.0V PMOS LDD	LP5MOS
SD	source/ drain implants	LP5MOS
MRPOLY	MRPOLY implant	MRPOLY
SALICIDE	salicidation	LP5MOS
CONTACT	contact	LP5MOS
METAL1	metal1	LP5MOS
VIA1	via1	LP5MOS
METAL2	metal2	LP5MOS
MIM23/MIMH23	MIM capacitor	MIM23, MIMH23
DMIM1/DMIMH1	double MIM capacitor	DMIM, DMIMH
TMIM1/TMIMH1	triple MIM capacitor	TMIM, TMIMH
VIA2	via2	MET3
METAL3	metal3	MET3
MIM34/ MIMH34	single MIM capacitor	MIM34, MIMH34
DMIM2/DMIMH2	double MIM capacitor	DMIM, DMIMH
DMIM31/DMIMH31	double MIM capacitor module	DMIM3, DMIMH3
TMIM2/TMIMH2	triple MIM capacitor	TMIM, TMIMH
VIA3	via3	MET4
METAL4	metal4	MET4
MIM45/ MIMH45	single MIM capacitor	MIM45, MIMH45
DMIM32/DMIMH32	double MIM capacitor module	DMIM3, DMIMH3
TMIM3/TMIMH3	triple MIM capacitor	TMIM, TMIMH
VIA4	via4	MET5
METAL5	metal5	MET5
MIM/ MIMH	MIM capacitor	MIM, MIMH
VIATP	top via	METMID
METALTP	top metal	METMID
VIATPL	thick via	METTHK
MTPL	thick metal	METTHK
FLATPV	planarized passivation	FLATPV
SMALLPAD	small passivation opening	SMALLPAD
PAD	passivation	LP5MOS
PIMIDE	polyimide	PIMIDE
BOTDIE	bottom dielectric	BOTDIE
METCOP	thick copper metal	THKCOP

2.2.2 for MOS5 main module

WIP reference	Process step	Process modules
WAFERSTART	wafer start	MOS5
HWC	Handle Wafer Contact	HWC
NBUR	N-buried implant	NBUR



2. General → 2.2 Process flows→ 2.2.2 for MOS5 main modul...

WIP reference	Process step	Process modules
EPI	epitaxy	MOS5
ACTIVE	active	MOS5
DTI	Deep Trench Isolation	DTI
SUB	SUB implant	MOS5
DFN	N-type drift implant	NHVR, PHVR
PDD	P-type drift implant	NHVR
DFP	P-type drift implant	PHVR
NDFMV	N-drift extension implant	NMV
PDFMV	P-drift extension implant	PMV
HVPW	HVPWELL	HVP
SJNP	SJNP implant	1XN
ESDMV	ESD implant for medium voltage	NMV
HVNW	HVNWELL	HVN
2XP	2X SJPN implant	2XP
SJPN	SJPN implant	1XP
NBUF	NBUF implant	NBUF
NDF	N-drain extension implant	NHVA
PDF	P-drain extension implant	PHVA
NPN	PBASE implant	BJTC
PNP	NBASE implant	BJTA
SJ1XN	1X SJNP implant	SJ1XN
WELL2	5.0V wells	MOS5
SJ1XP	1X SJPN implant	SJ1XP
PZN	PZENER implant	DIODEB
NZN	NZENER Implant	DIODEC
WELL1	1.8V wells	DNC, DPC
HVDEPL	HV depletion implant	HVDEPL
DEPL	depletion implant	DEPL
MVGOX	5.0V gate oxide	MOS5
POLY	poly silicon gate	MOS5
LDN	Additional HRPOLY implant	HRPOLY
NLDD2	5.0V NMOS LDD	MOS5
PLDD2	5.0V PMOS LDD	MOS5
SD	source/ drain implants	MOS5
MRPOLY	MRPOLY implant	MRPOLY
SALICIDE	salicidation	MOS5
CONTACT	contact	MOS5
METAL1	metal1	MOS5
VIA1	via1	MOS5
METAL2	metal2	MOS5
MIM23/MIMH23	MIM capacitor	MIM23, MIMH23
DMIM1/DMIMH1	double MIM capacitor	DMIM, DMIMH
TMIM1/TMIMH1	triple MIM capacitor	TMIM, TMIMH



2. General → 2.2 Process flows→ 2.2.2 for MOS5 main modul...

WIP reference	Process step	Process modules
VIA2	via2	MET3
METAL3	metal3	MET3
MIM34/ MIMH34	single MIM capacitor	MIM34, MIMH34
DMIM2/DMIMH2	double MIM capacitor	DMIM, DMIMH
DMIM31/DMIMH31	double MIM capacitor module	DMIM3
TMIM2/TMIMH2	triple MIM capacitor	TMIM, TMIMH
VIA3	via3	MET4
METAL4	metal4	MET4
MIM45/ MIMH45	single MIM capacitor	MIM45, MIMH45
DMIM32/DMIMH32	double MIM capacitor module	DMIM3
TMIM3/TMIMH3	triple MIM capacitor	TMIM, TMIMH
VIA4	via4	MET5
METAL5	metal5	MET5
MIM/ MIMH	MIM capacitor	MIM, MIMH
VIATP	top via	METMID
METALTP	top metal	METMID
VIATPL	thick via	METTHK
MTPL	thick metal	METTHK
FLATPV	planarized passivation	FLATPV
SMALLPAD	small passivation opening	SMALLPAD
PAD	passivation	MOS5
PIMIDE	polyimide	PIMIDE
BOTDIE	bottom dielectric	BOTDIE
METCOP	thick copper metal	THKCOP

2. General → 2.3 Wafer cross-section

2.3 Wafer cross-section

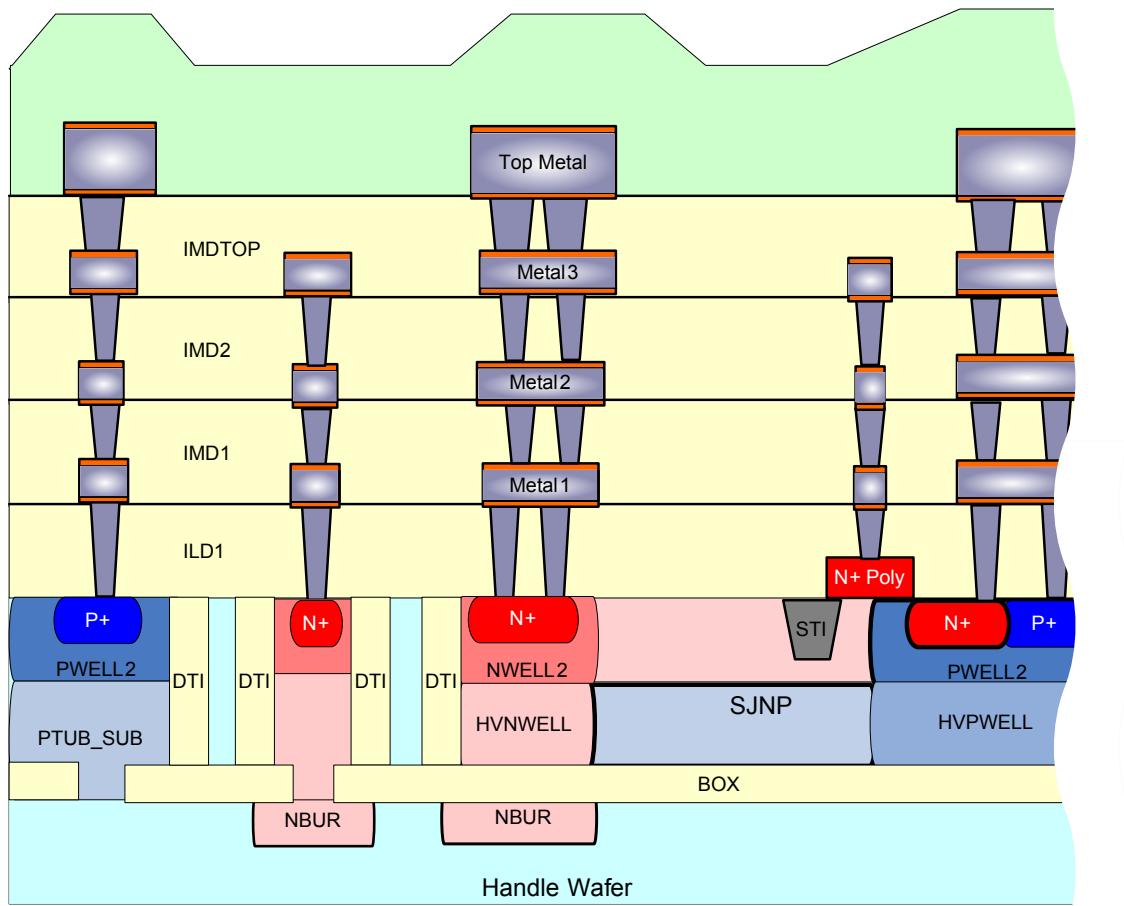
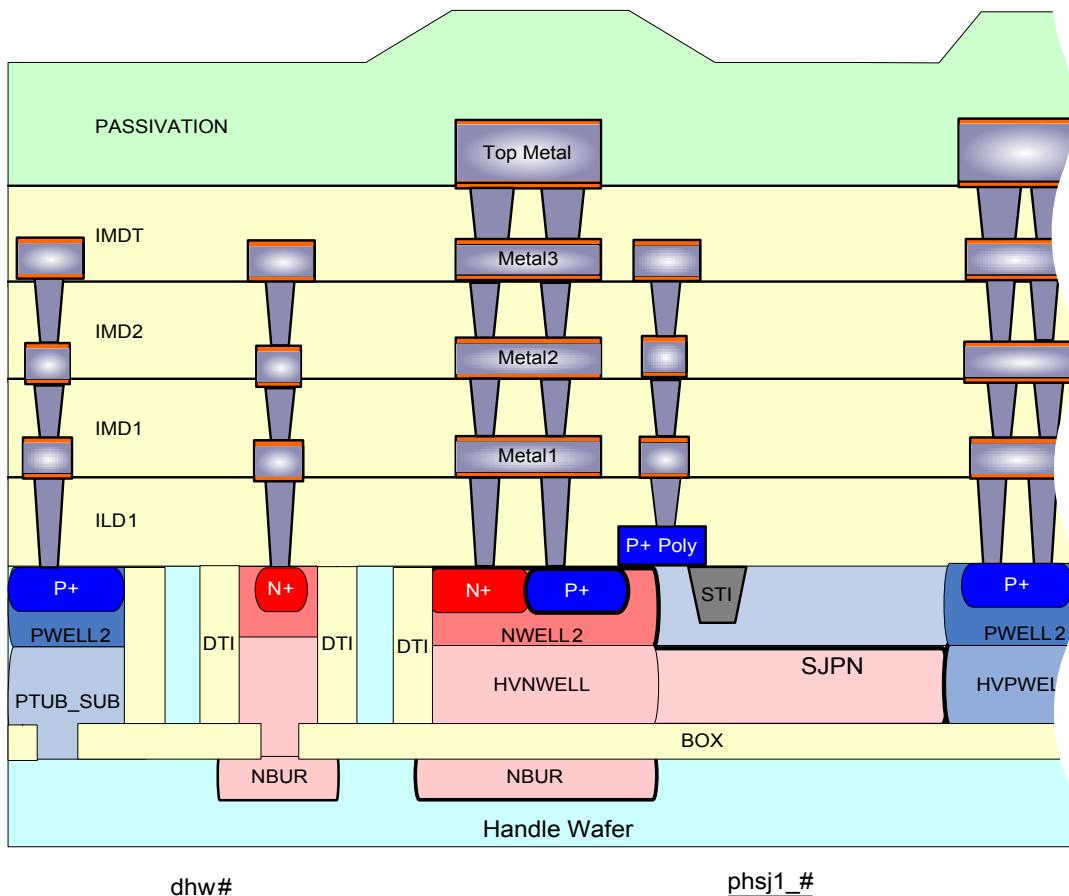
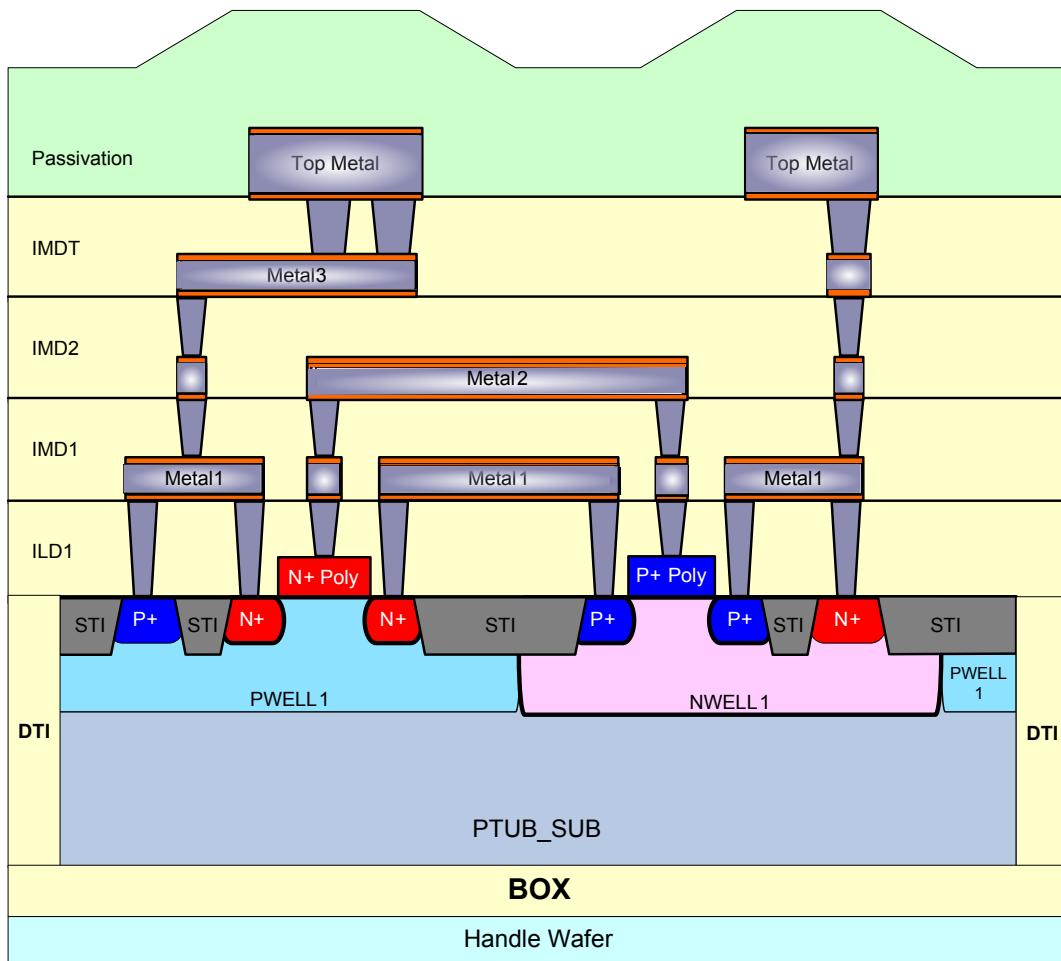


Figure 2.1 Cross-section showing devices **dhw#** and **nhsj1_#**

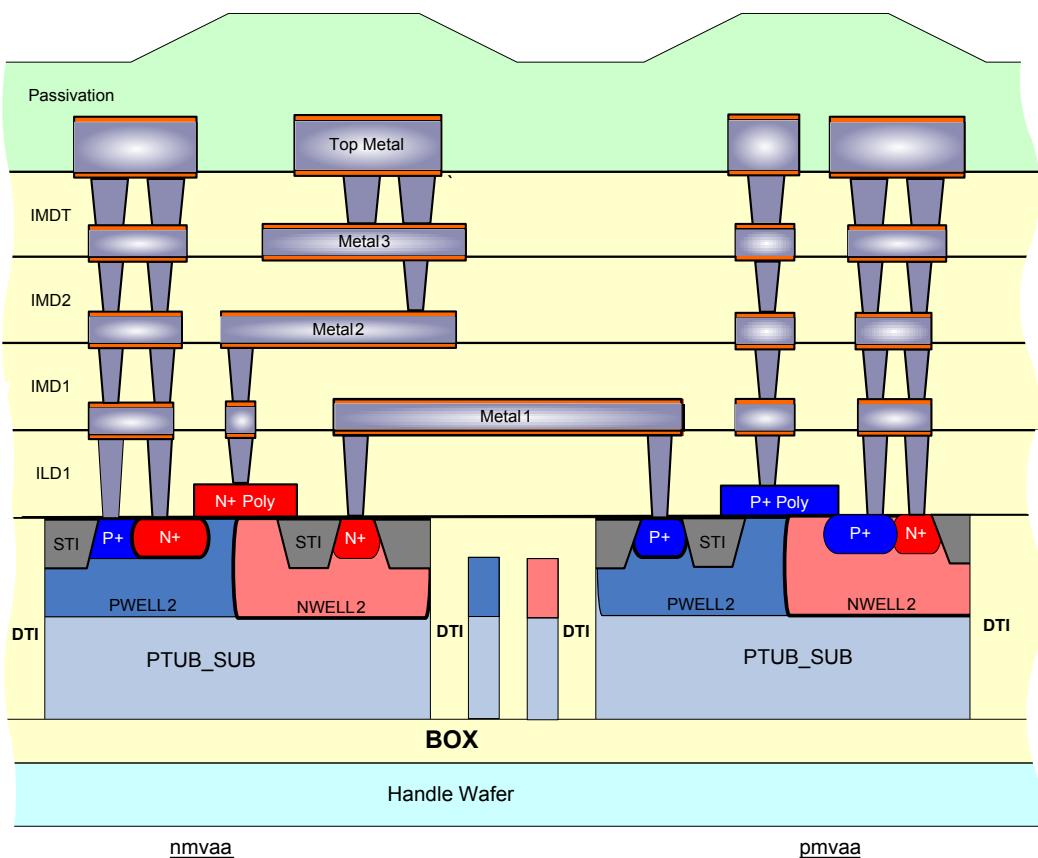
2. General → 2.3 Wafer cross-section

**Figure 2.2** Cross-section showing devices dhw# and phsj1_#

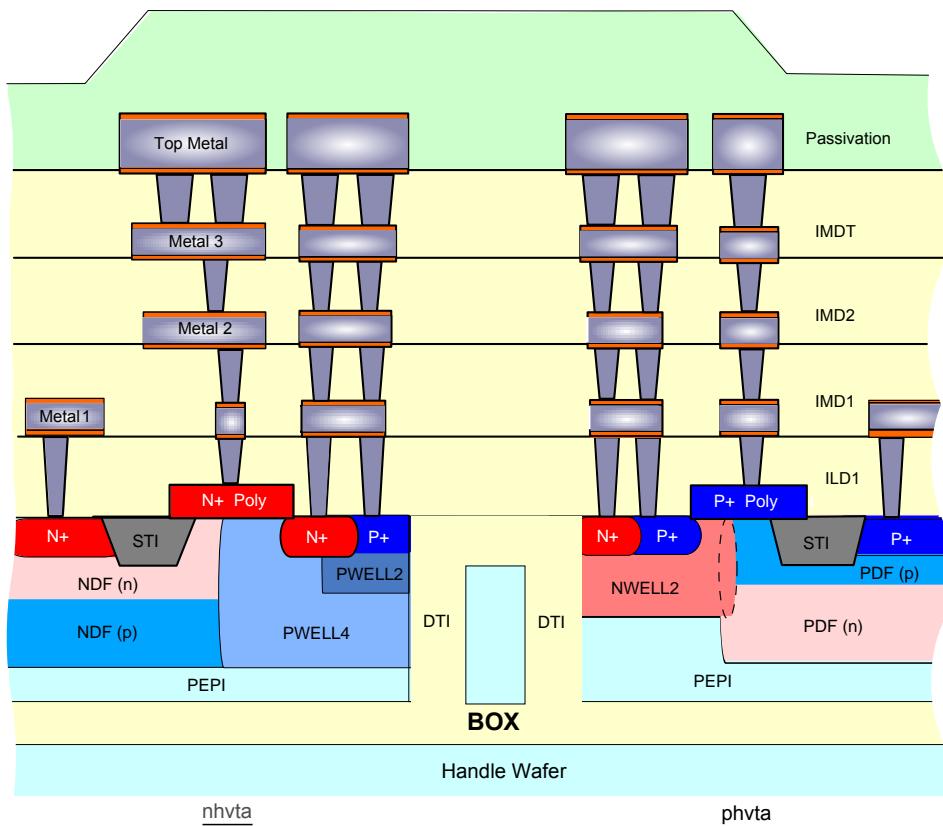
2. General → 2.3 Wafer cross-section

**Figure 2.3** Cross-section showing devices ne and pe

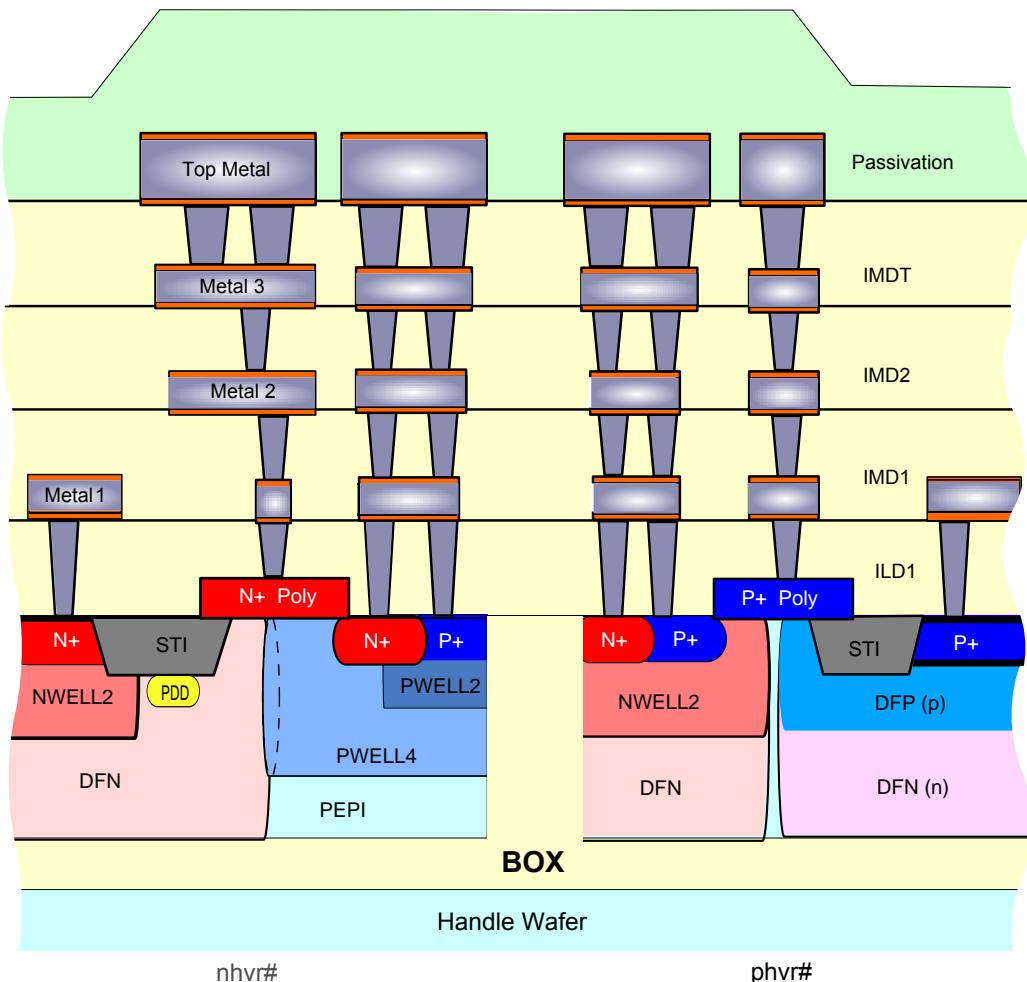
2. General → 2.3 Wafer cross-section

**Figure 2.4** Cross-section showing devices nmvaa pmvaa

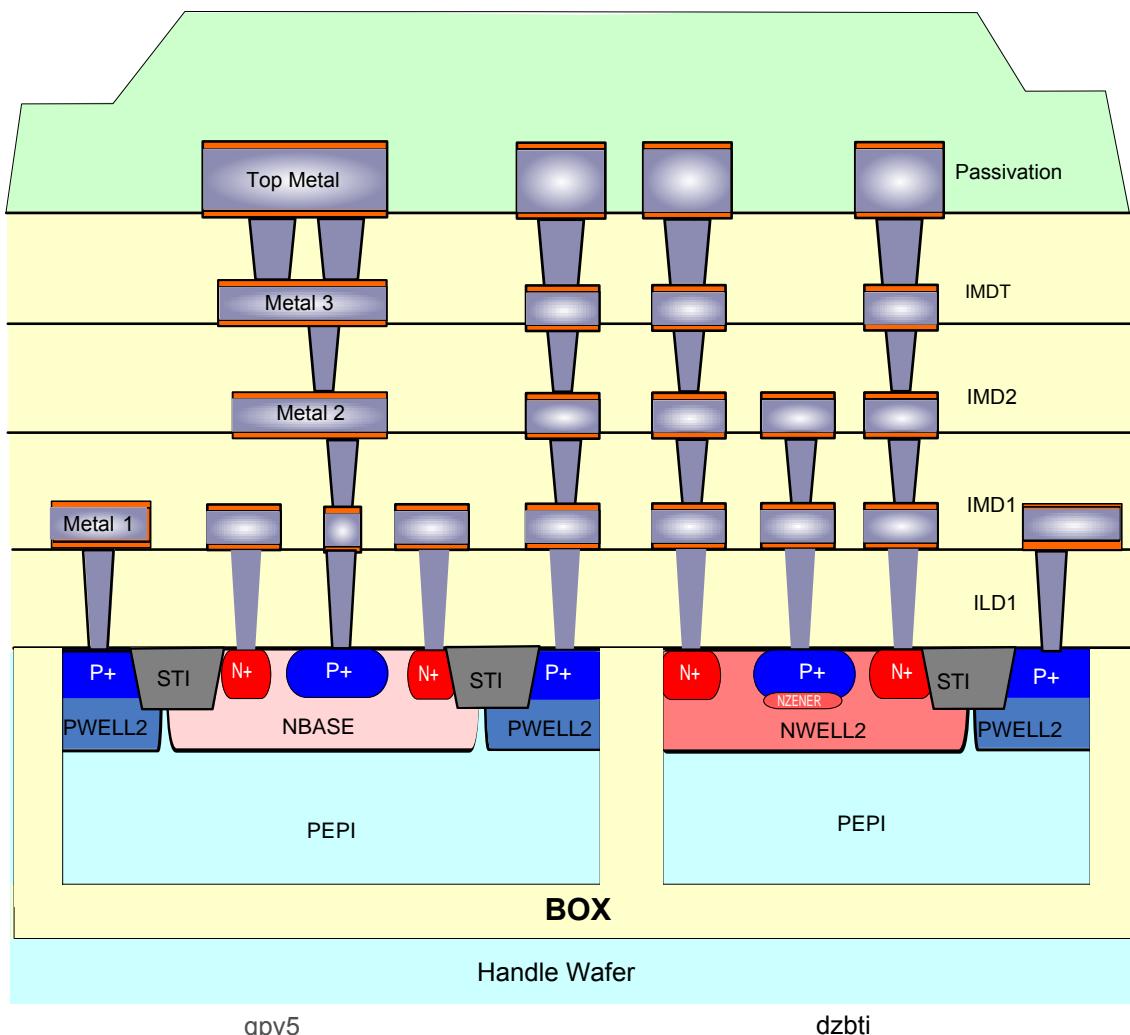
2. General → 2.3 Wafer cross-section

**Figure 2.5** Cross-section showing devices nhvta and phvta

2. General → 2.3 Wafer cross-section

**Figure 2.6** Cross-section showing devices nhvr# and phvr#

2. General → 2.3 Wafer cross-section

**Figure 2.7** Cross-section showing devices qpv5 and dzbti

2. General → 2.4 Bond pad structure

2.4 Bond pad structure

2.4.1 3 Metal METMID Bond Pad

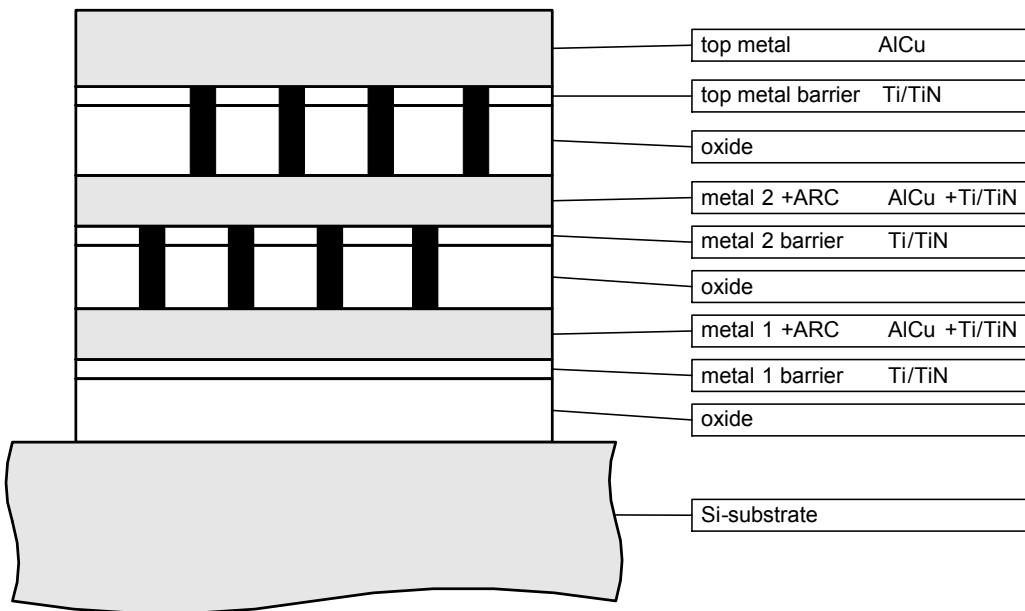


Figure 2.8 Principle of vertical structure of bond pads for three layer metal
(only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)
-----------	-----------------------

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.2 4 Metal METMID + MET...

2.4.2 4 Metal METMID + METTHK Bond Pad

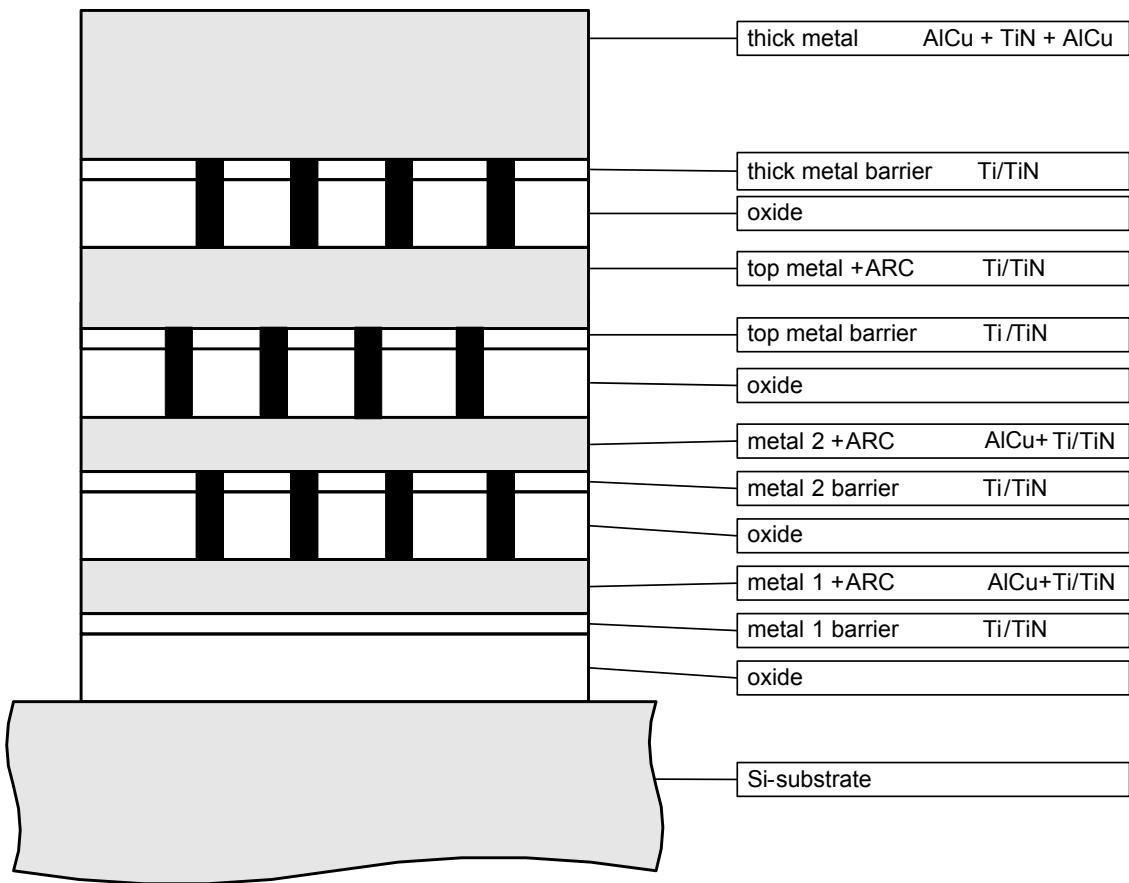


Figure 2.9 Principle of vertical structure of bond pads for four layers of metal
(only valid for the bond pad described by the Design Rule Specification):

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.3 4 Metal METMID Bond ...

2.4.3 4 Metal METMID Bond Pad

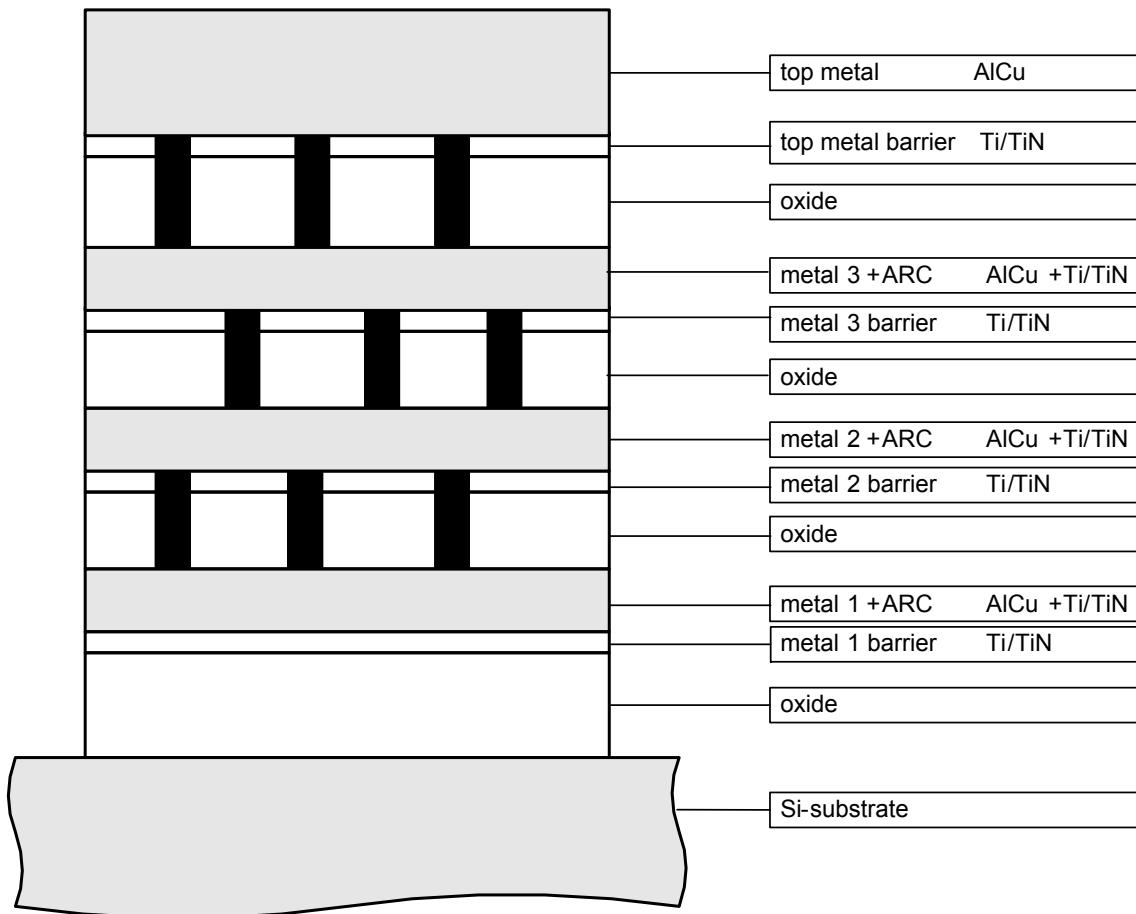


Figure 2.10 Principle of vertical structure of bond pads for four layer metal
(only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)
-----------	-----------------------

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.4 5 Metal METMID + MET...

2.4.4 5 Metal METMID + METTHK Bond Pad

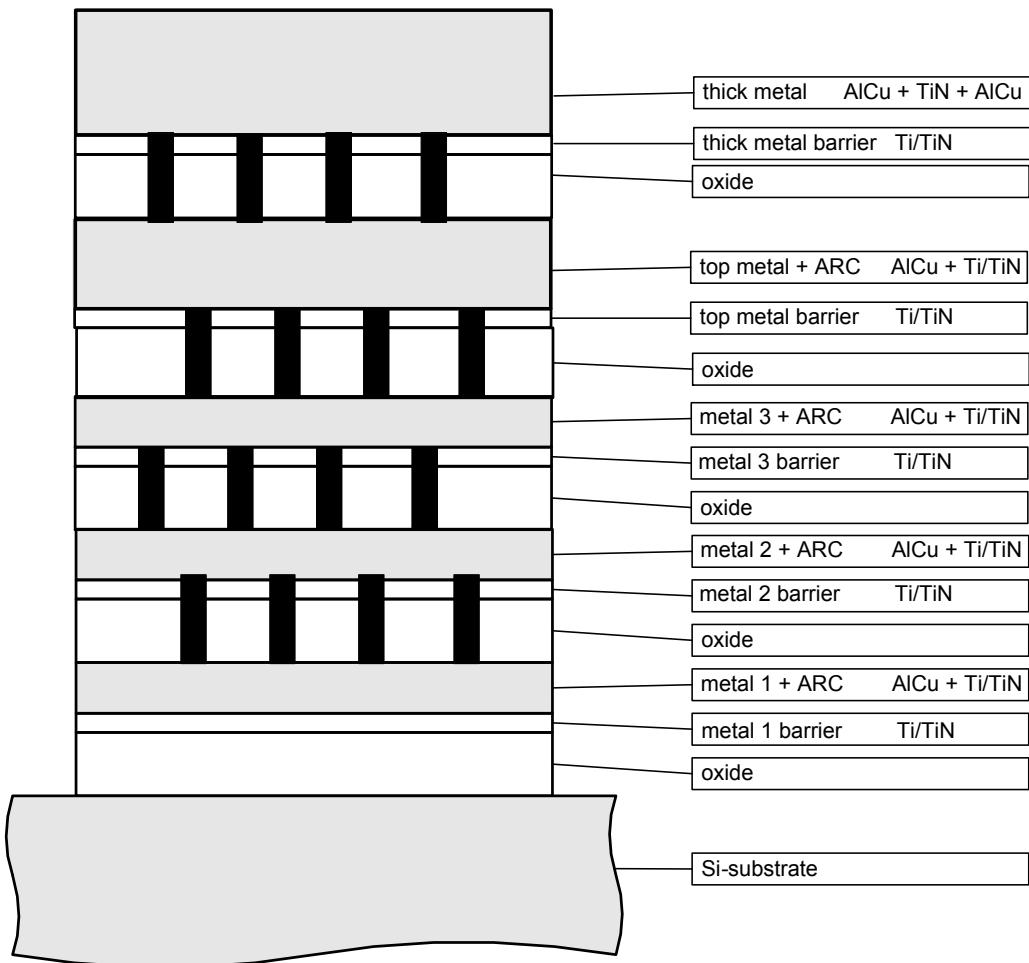


Figure 2.11 Principle of vertical structure of bond pads for five layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.5 5 Metal METMID Bond ...

2.4.5 5 Metal METMID Bond Pad

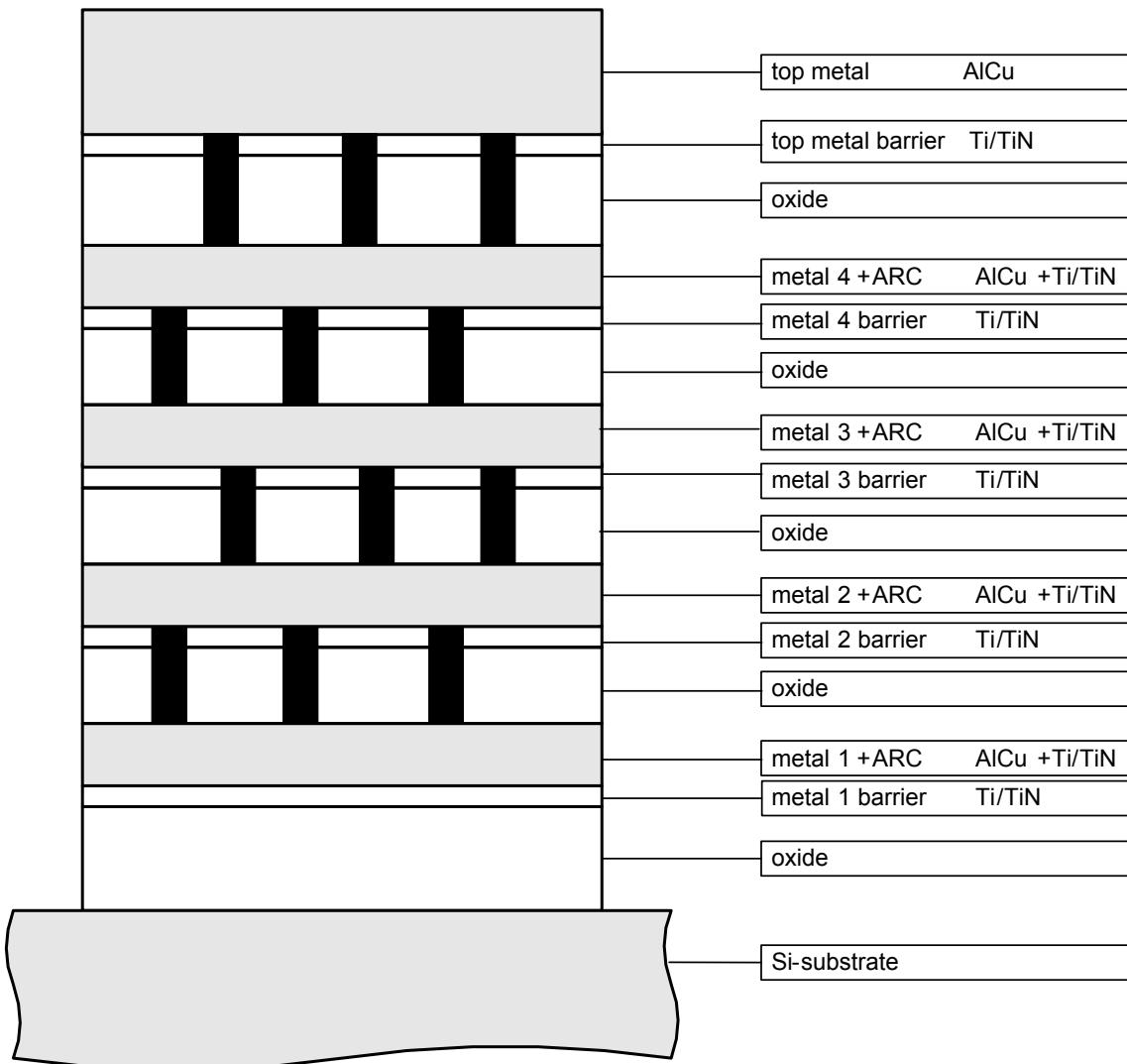


Figure 2.12 Principle of vertical structure of bond pads for five layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)
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It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.6 6 Metal METMID + MET...

2.4.6 6 Metal METMID + METTHK Bond Pad

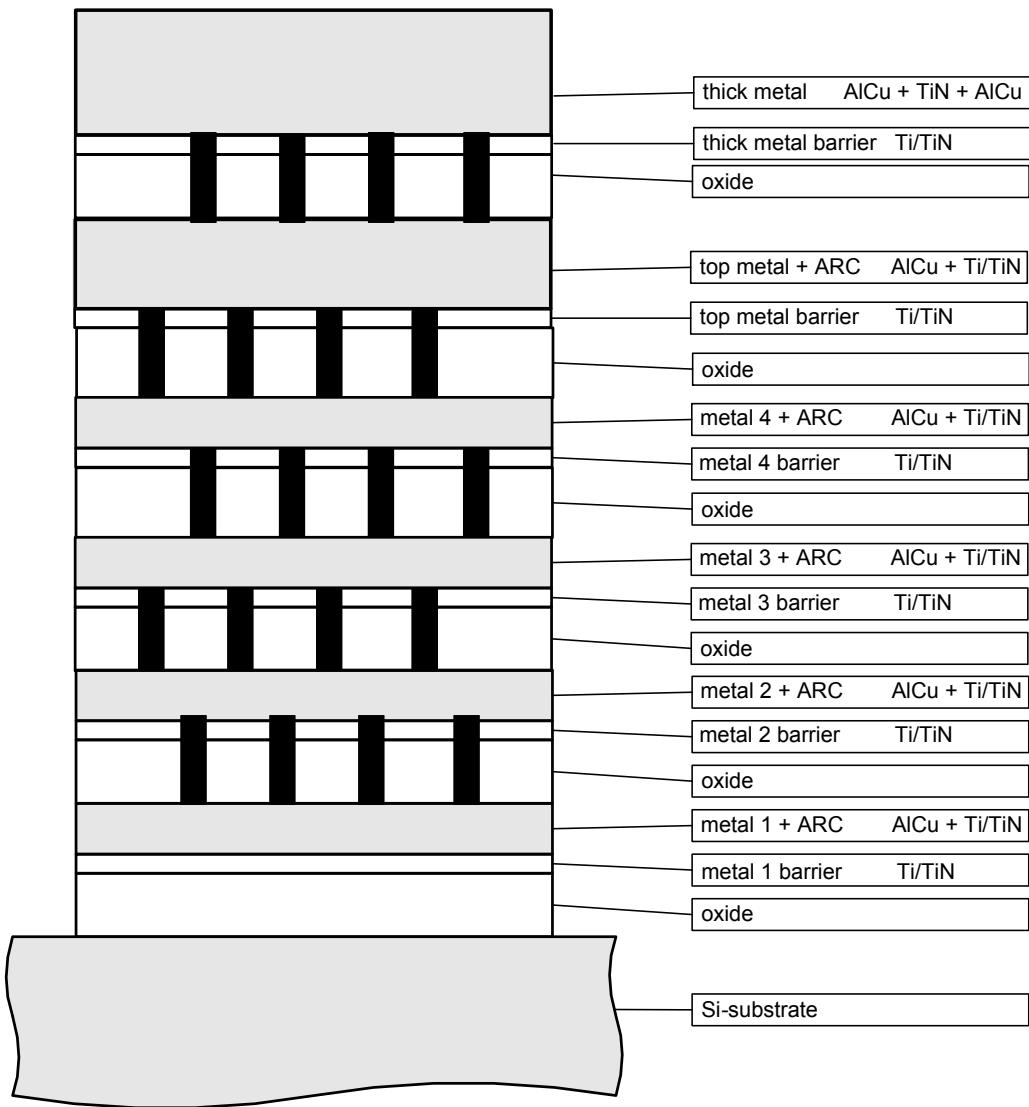


Figure 2.13 Principle of vertical structure of bond pads for six layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.7 6 Metal METMID Bond ...

2.4.7 6 Metal METMID Bond Pad

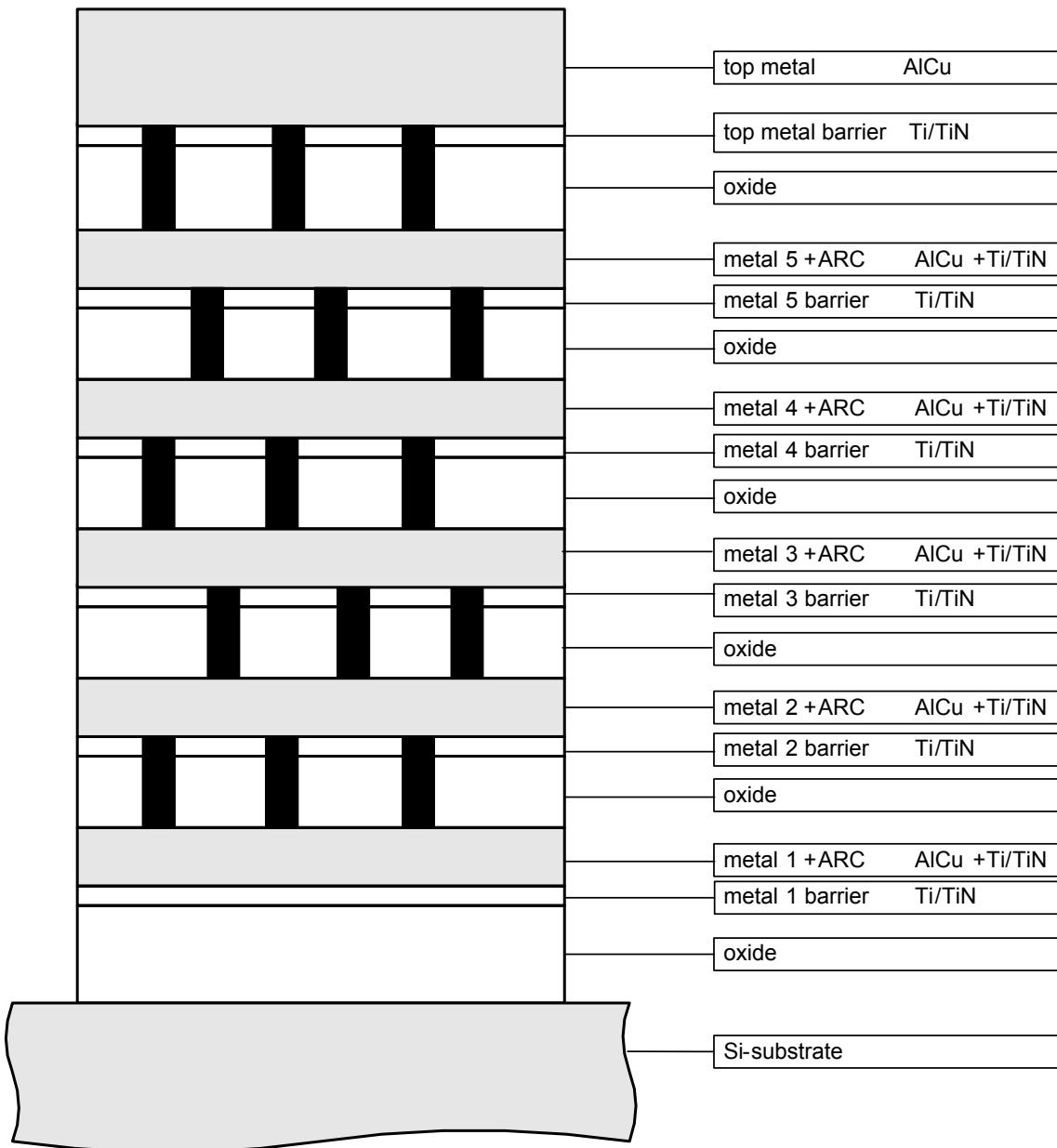


Figure 2.14 Principle of vertical structure of bond pads for six layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)
-----------	-----------------------

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure→ 2.4.8 4 Metal METTHK Bond ...

2.4.8 4 Metal METTHK Bond Pad

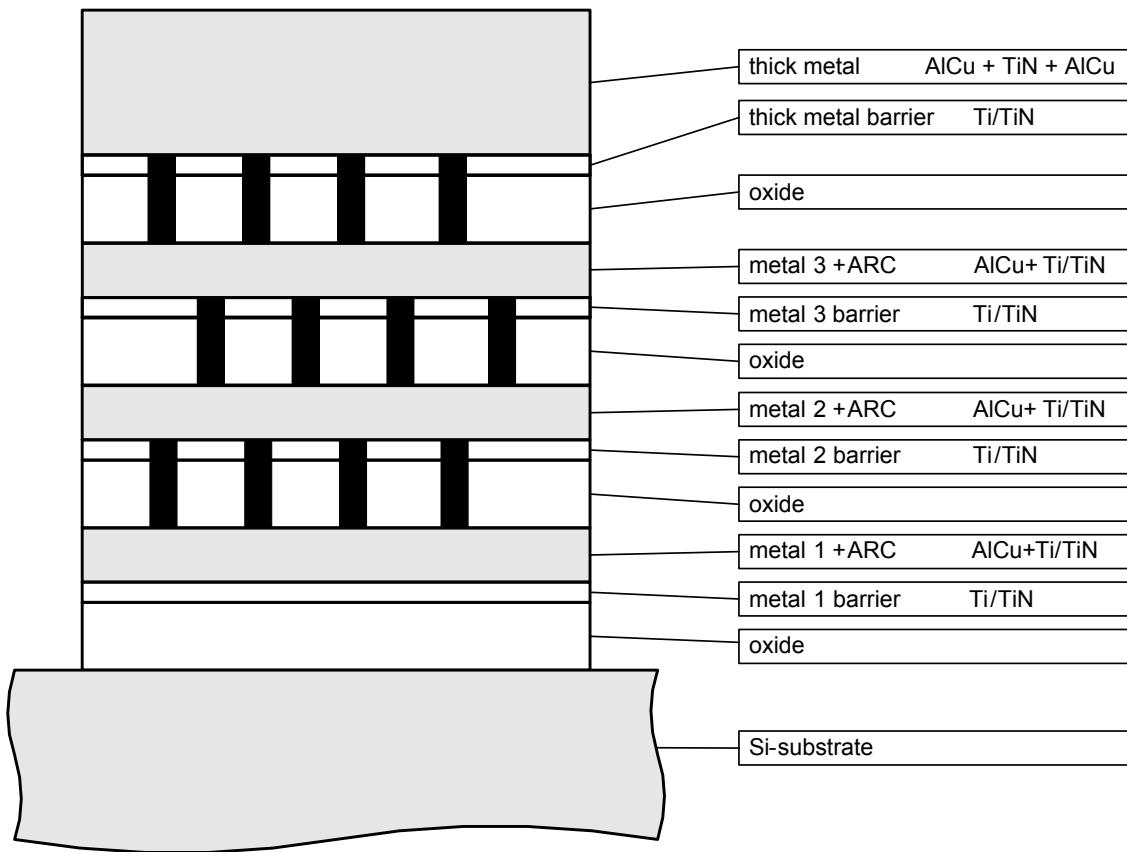


Figure 2.15 Principle of vertical structure of bond pads for four layers of metal (only valid for the bond pad described by the Design Rule Specification):

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.9 5 Metal METTHK Bond ...

2.4.9 5 Metal METTHK Bond Pad

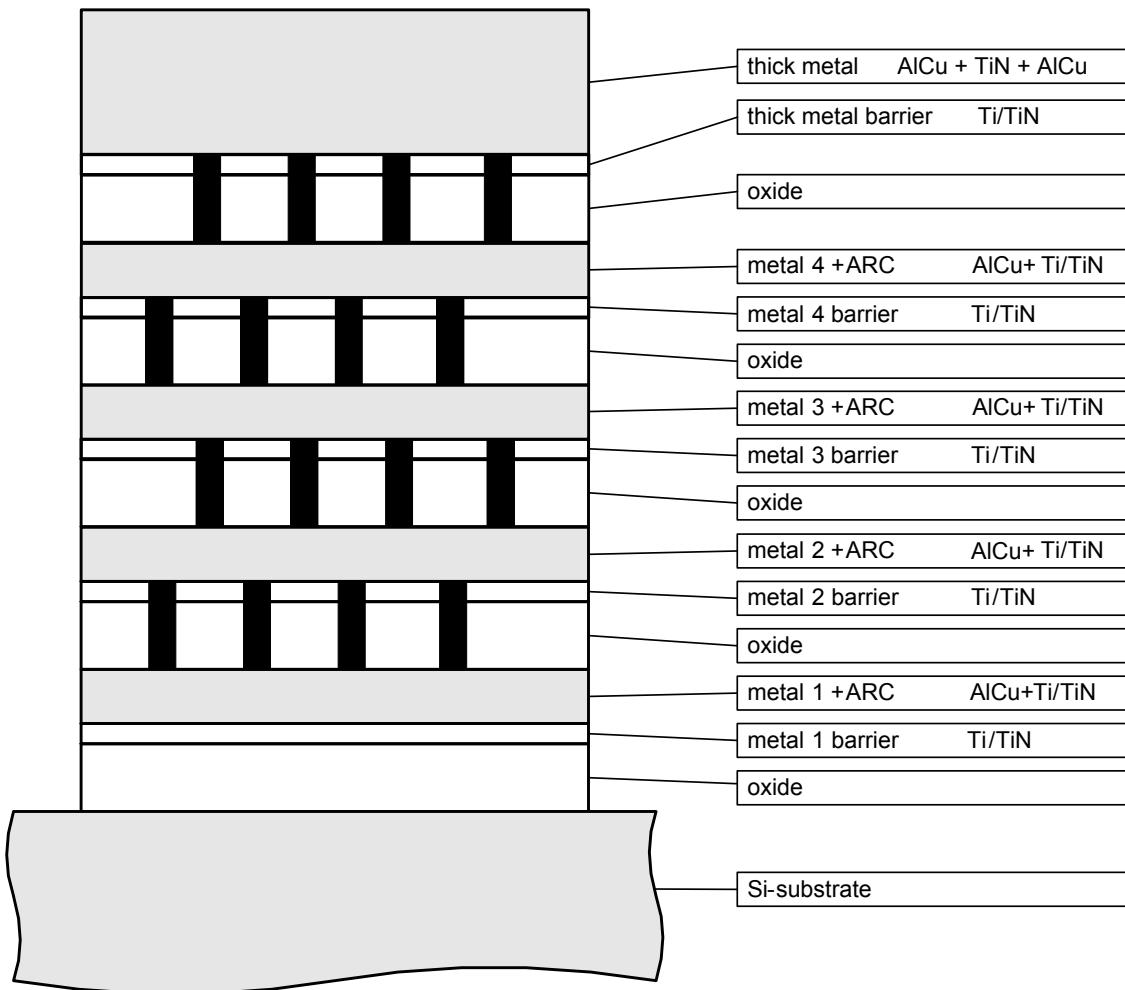


Figure 2.16 Principle of vertical structure of bond pads for five layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.10 6 Metal METTHK Bond ...

2.4.10 6 Metal METTHK Bond Pad

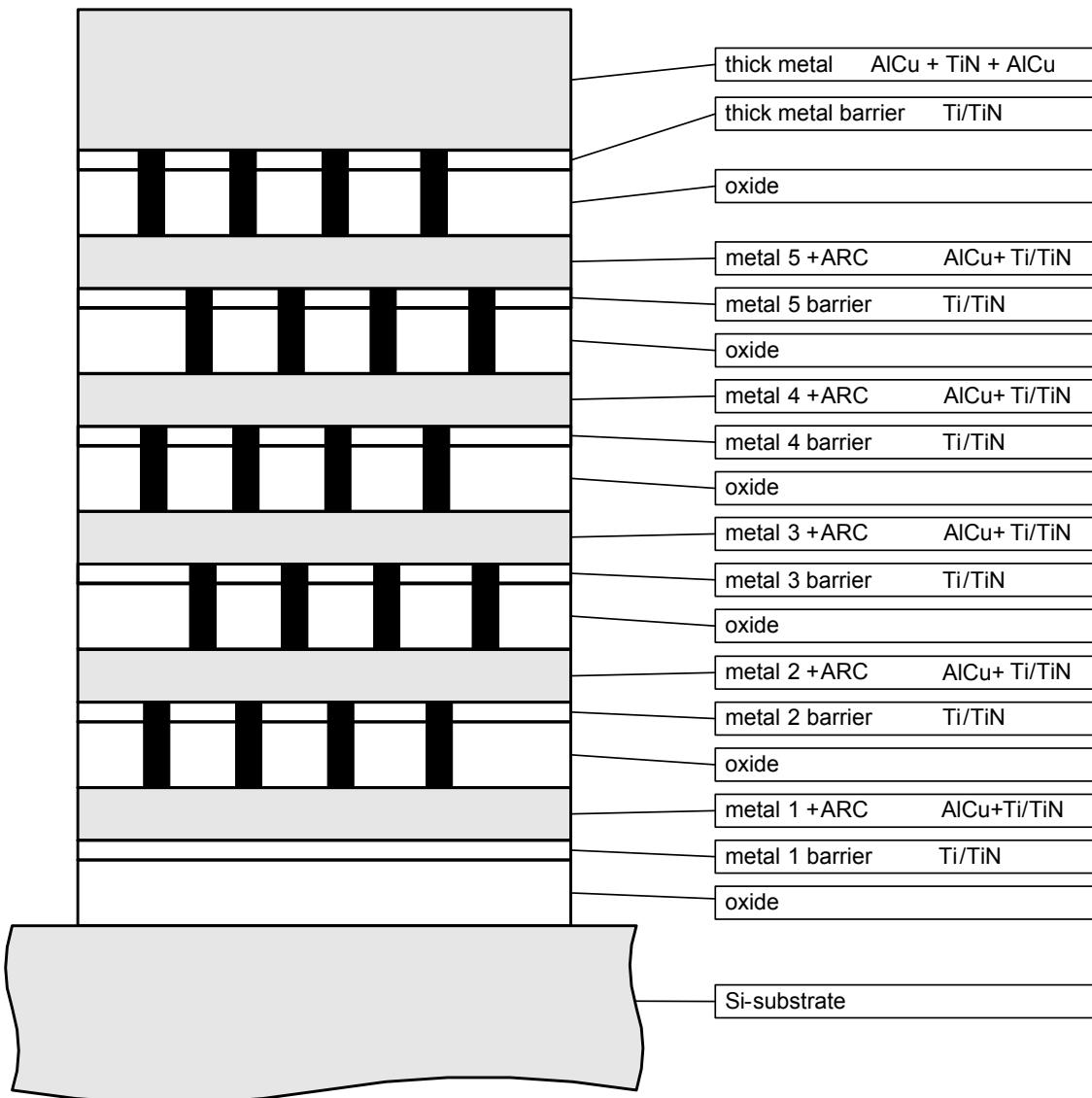


Figure 2.17 Principle of vertical structure of bond pads for six layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure→ 2.4.11 4 Metal METMID + MET...

2.4.11 4 Metal METMID + METTHK Circuit-Under-Pad Bond Pad

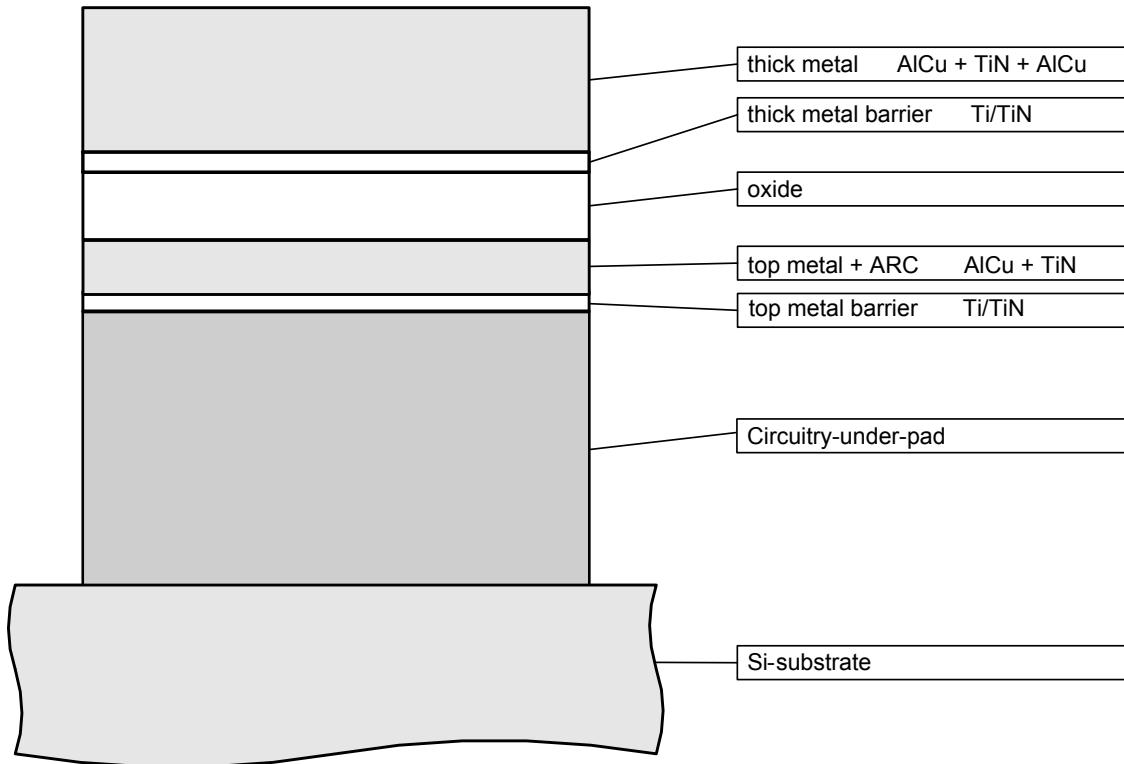


Figure 2.18 Principle of vertical structure of Circuit-Under-Pad Bond Pads for four layers of metal (only valid for the bond pad described by the Design Rule Specification):

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure→ 2.4.12 4 Metal METMID Circu...

2.4.12 4 Metal METMID Circuit-Under-Pad Bond Pad

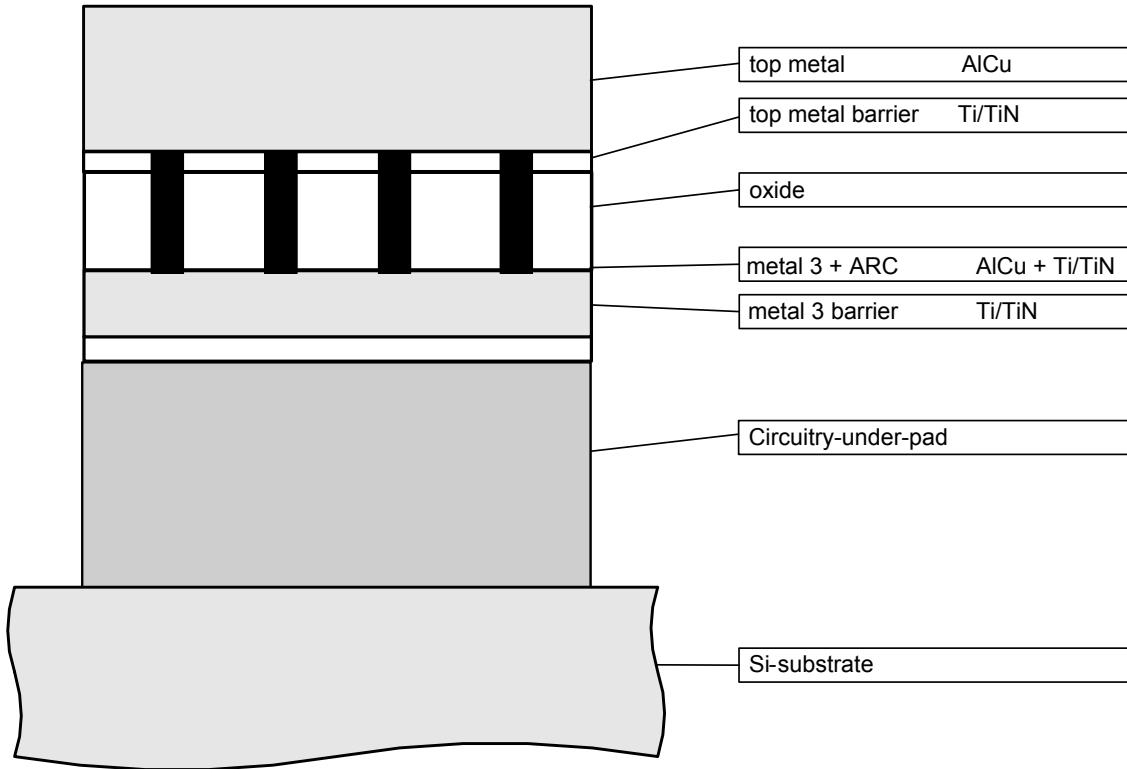


Figure 2.19 Principle of vertical structure of Circuit-Under-Pad Bond Pads for four layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)
-----------	-----------------------

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure→ 2.4.13 4 Metal METTHK Circu...

2.4.13 4 Metal METTHK Circuit-Under-Pad Bond Pad

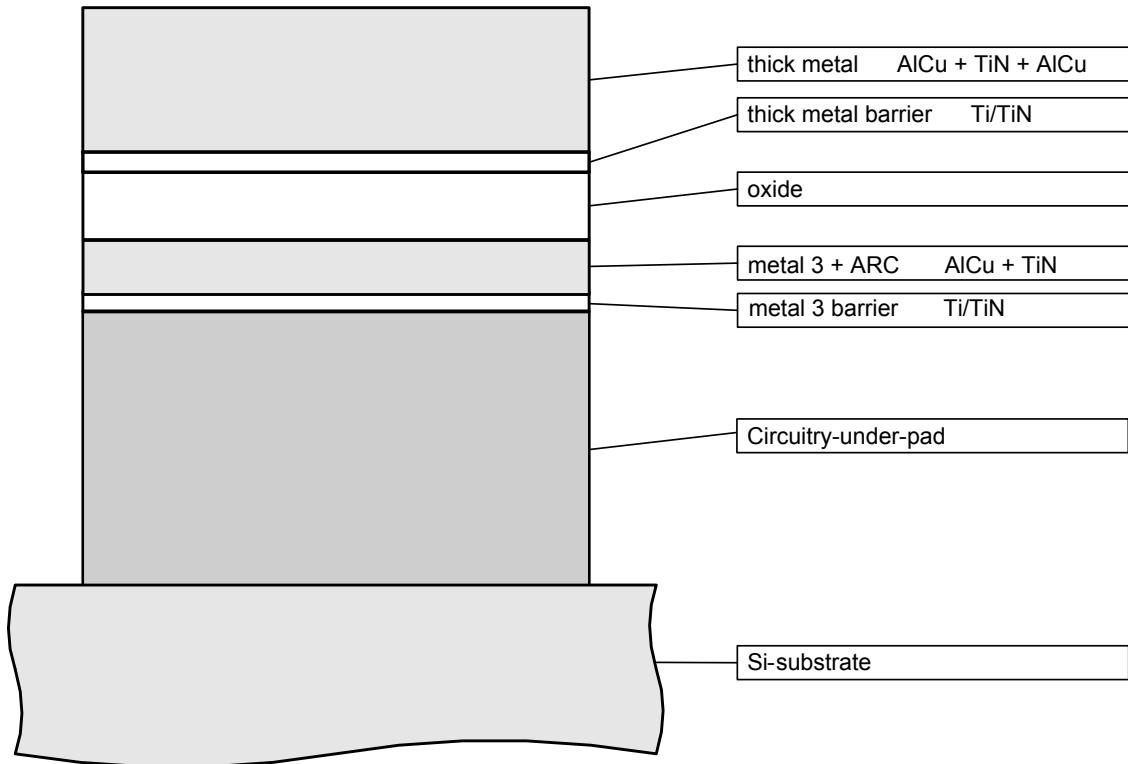


Figure 2.20 Principle of vertical structure of Circuit-Under-Pad Bond Pads for four layers of metal (only valid for the bond pad described by the Design Rule Specification):

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.14 5 Metal METMID + MET...

2.4.14 5 Metal METMID + METTHK Circuit-Under-Pad Bond Pad

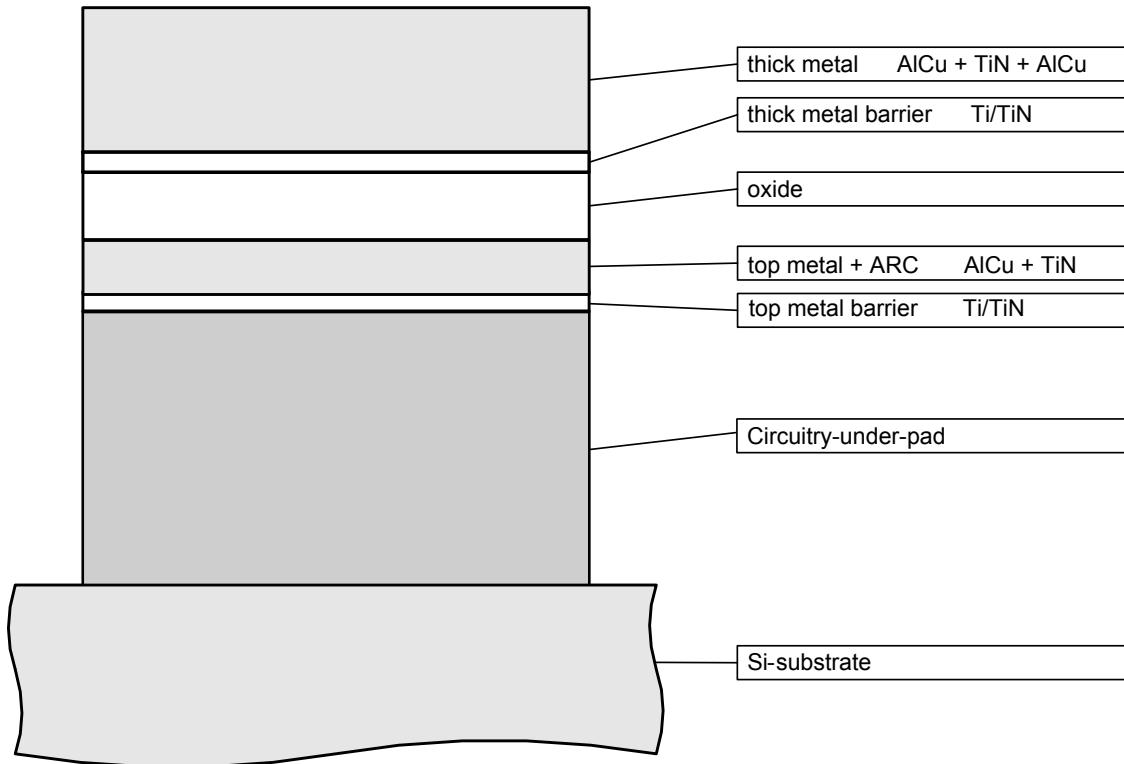


Figure 2.21 Principle of vertical structure of Circuit-Under-Pad Bond Pads for five layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure→ 2.4.15 5 Metal METMID Circu...

2.4.15 5 Metal METMID Circuit-Under-Pad Bond Pad

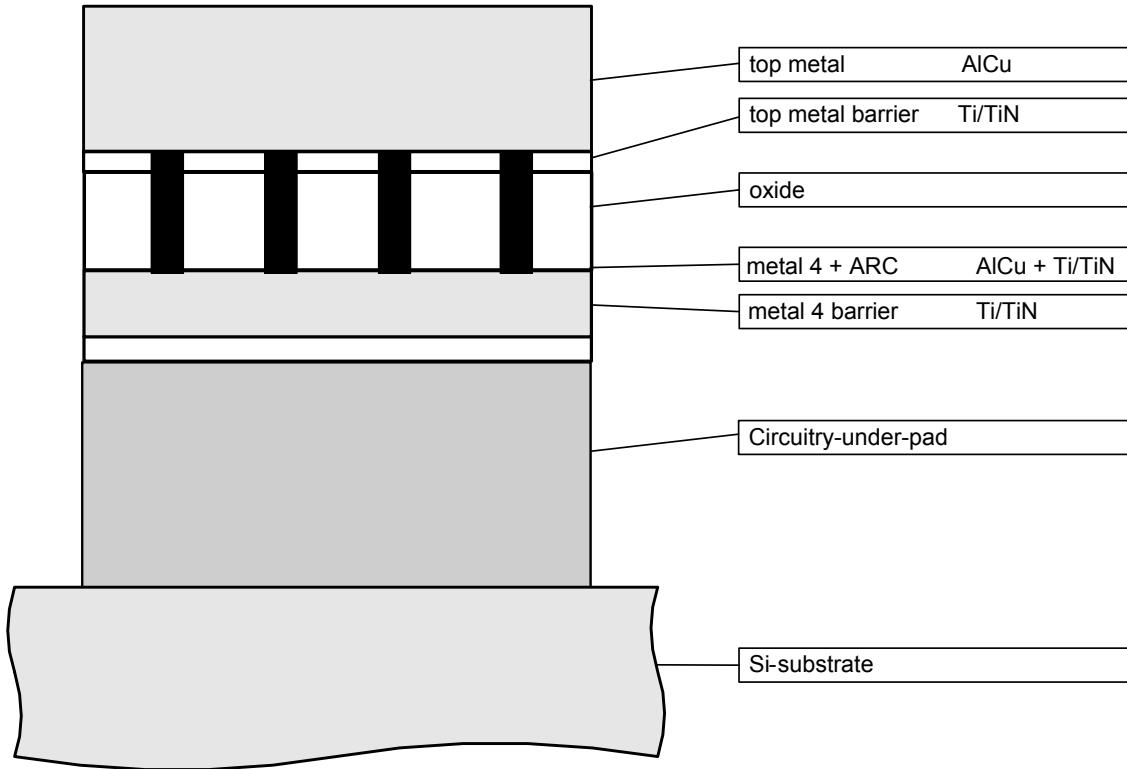


Figure 2.22 Principle of vertical structure of Circuit-Under-Pad Bond Pads for five layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)
-----------	-----------------------

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure→ 2.4.16 5 Metal METTHK Circu...

2.4.16 5 Metal METTHK Circuit-Under-Pad Bond Pad

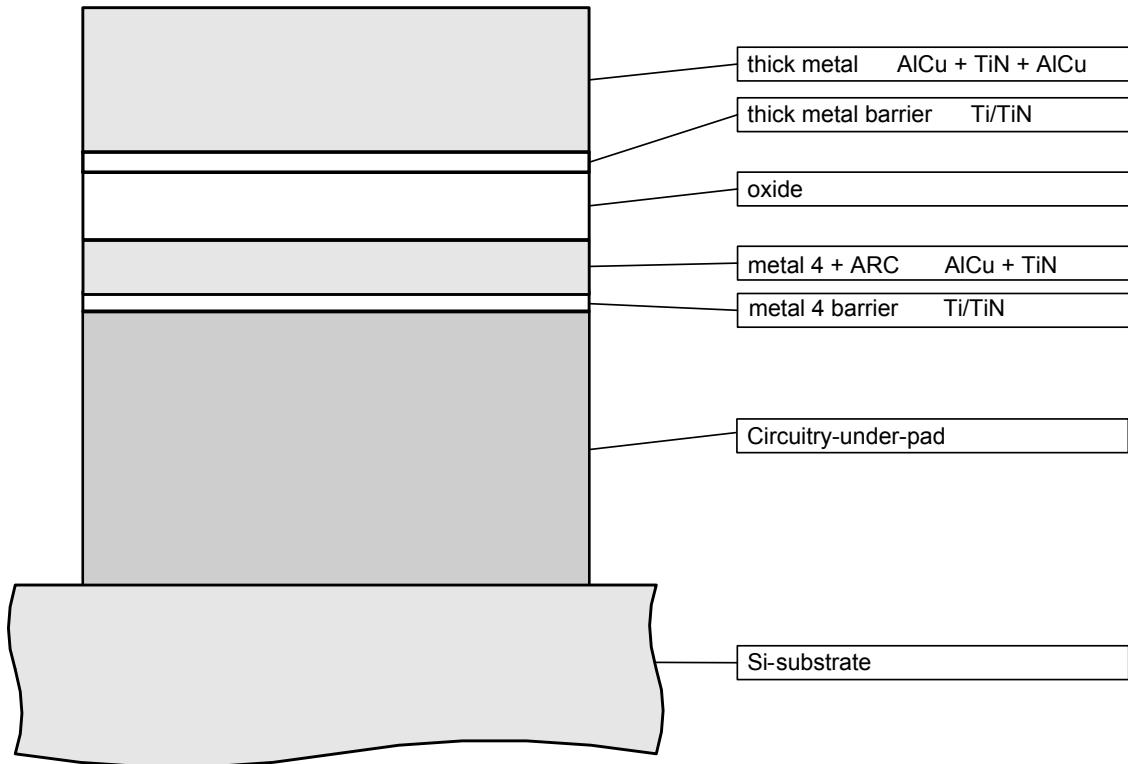


Figure 2.23 Principle of vertical structure of Circuit-Under-Pad Bond Pads for five layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.17 6 Metal METMID + MET...

2.4.17 6 Metal METMID + METTHK Circuit-Under-Pad Bond Pad

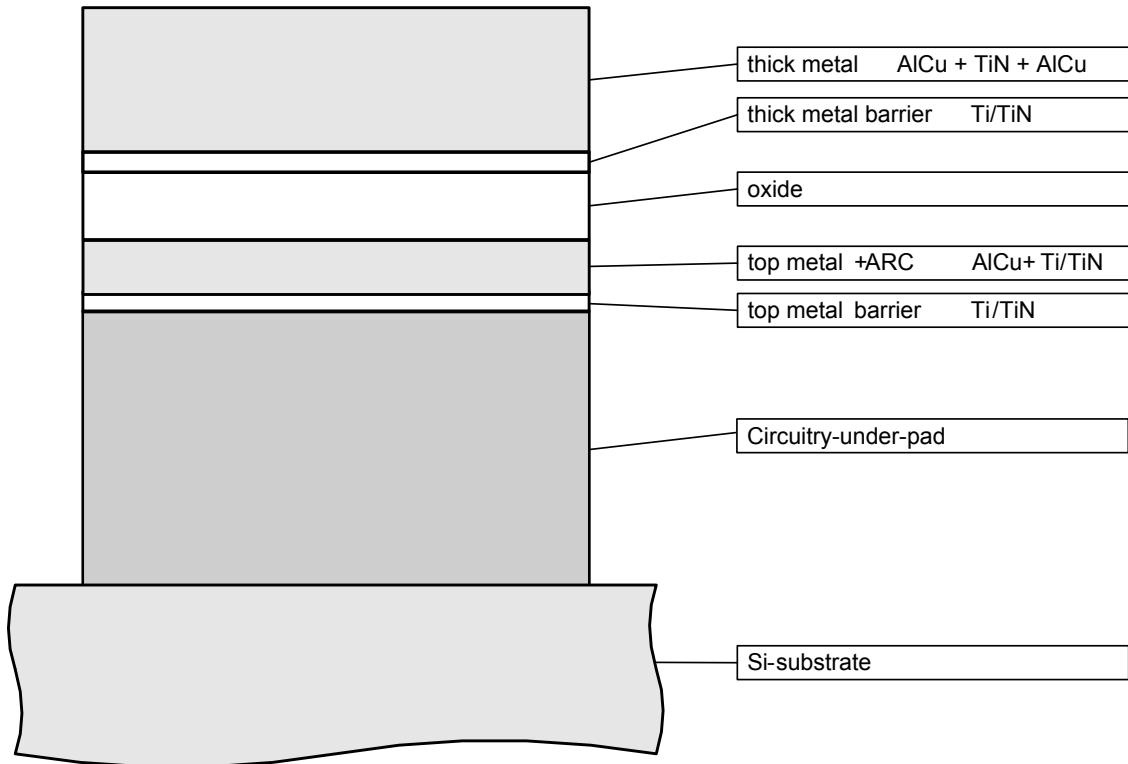


Figure 2.24 Principle of vertical structure of Circuit-Under-Pad Bond Pads for six layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure→ 2.4.18 6 Metal METMID Circu...

2.4.18 6 Metal METMID Circuit-Under-Pad Bond Pad

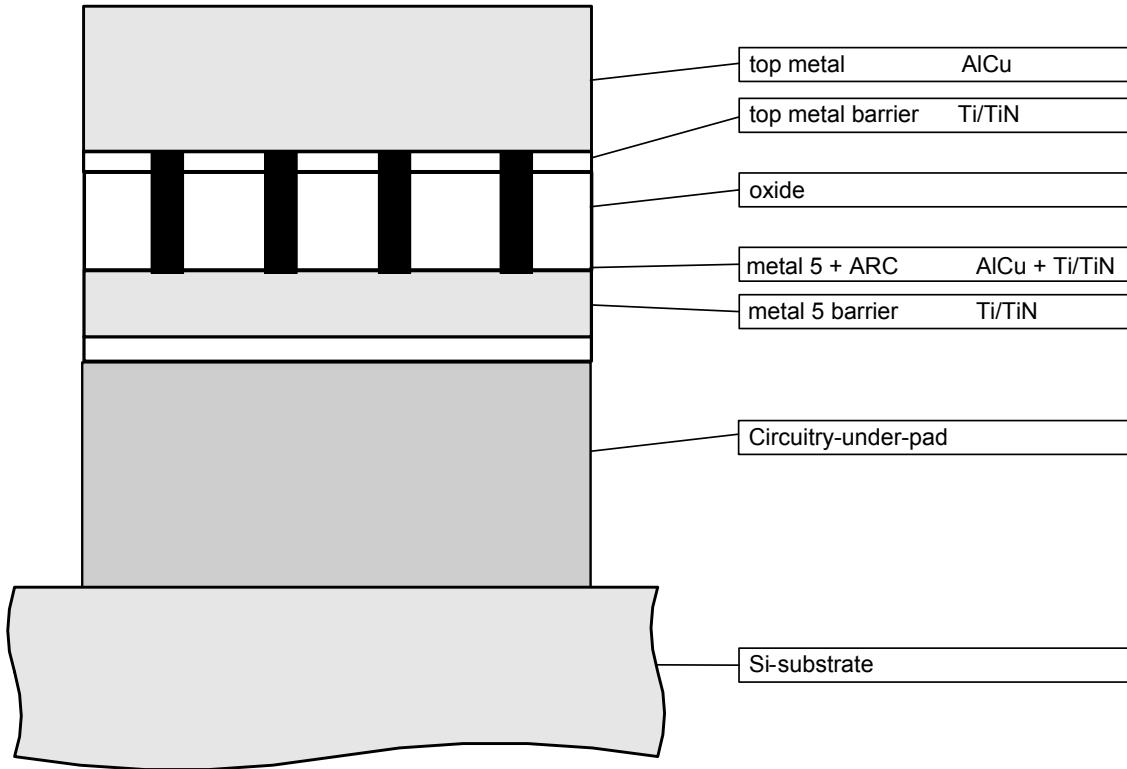


Figure 2.25 Principle of vertical structure of Circuit-Under-Pad Bond Pads for six layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

top metal	880 nm AlCu (0.5% Cu)
-----------	-----------------------

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.4 Bond pad structure → 2.4.19 6 Metal METTHK Circu...

2.4.19 6 Metal METTHK Circuit-Under-Pad Bond Pad

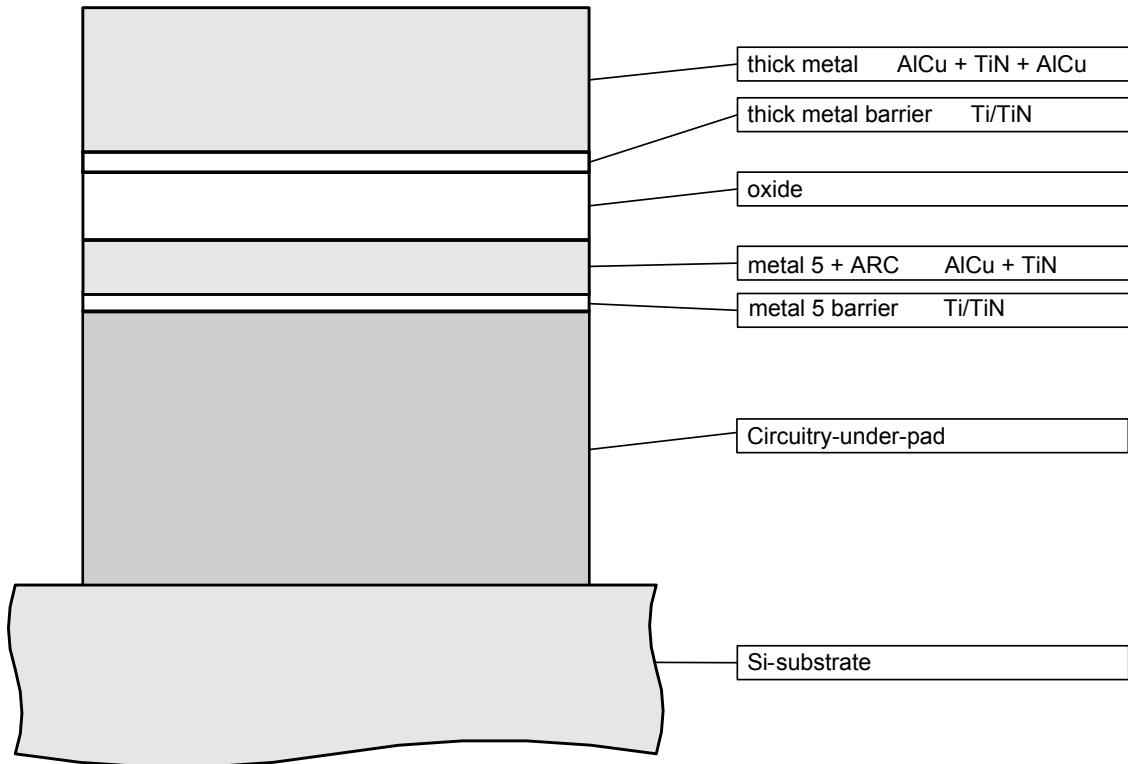


Figure 2.26 Principle of vertical structure of Circuit-Under-Pad Bond Pads for six layers of metal (only valid for the bond pad described by the Design Rule Specification)

Note: Top metal thickness at Bond Pad (typical value):

thick metal	1480 nm AlCu (0.5% Cu) + 40 nm TiN + 1480 nm AlCu (0.5% Cu)
-------------	---

It is completely under customer's responsibility to communicate the bond pad structure as described above towards the assembly house to achieve a maximum of assembly performance by optimized assembly process parameters.

2. General → 2.5 Acronyms for operating conditions

2.5 Acronyms for operating conditions

Name	Description
VGS	Gate to source voltage
VGB	Gate to bulk voltage
VGD	Gate to drain voltage
VDS	Drain to source voltage
VDB	Drain to bulk voltage
VSB	Source to bulk voltage
VBpsub	Bulk to p-substrate voltage
VBptub	Bulk to p-tub voltage
VCE	Collector to emitter voltage
VEB	Emitter to base voltage
VBC	Base to collector voltage
VGE	Gate to emitter voltage
VGC	Gate to collector voltage
Vterm-bulk	Terminal to bulk voltage
Vterm-HW	Terminal to handle wafer voltage
Vterm-NB	Terminal to buried-N voltage
Vterm1-Vterm2	Terminal to terminal voltage
Vtub-handle wafer	Tub to Handle wafer voltage
Vanode-Vcathode	Anode to cathode voltage
Vcathode-Vpsub	Cathode to p-substrate voltage
Vcathode-Vpepi	Cathode to pepi voltage
VA-HW	Anode to handle wafer voltage
VB-HW	Bulk to handle wafer voltage
Vcathode-HW	Cathode to handle wafer voltage
VD-HW	Drain to handle wafer voltage
VC-HW	Collector to handle wafer voltage
VPT-HW	PTUB to handle wafer voltage
VB-NB	Bulk to buried-N voltage
VC-NB	Collector to buried-N voltage
VD-NB	Drain to buried-N voltage
Vcathode-NB	Cathode to buried-N voltage
If	Forward current
Ifp	Forward pulse current
Ibr	Breakdown current
Ibr1000	Breakdown current for 1000 seconds
JDL	Current density per width
JVI	Current density per via
JMax_CT_DC	Current density per contact, DC
JMax_DC	Current density per width, DC
JMax_N_DC	Current density per width for narrow tracks, DC
JMax_VI_DC	Current density per via, DC
JMax_CT_AC	Current density per contact, AC



2. General → 2.5 Acronyms for operating conditions

Name	Description
JMax_AC	Current density per width, AC
JMax_N_AC	Current density per width for narrow tracks, AC
JMax_VI_AC	Current density per via, AC
T_Factor_1e4	Temperature correction factor, for 1E+04h lifetime
T_Factor_1e5	Temperature correction factor, for 1E+05h lifetime
E	Electric field

2. General → 2.6 Acronyms for measurement conditions

2.6 Acronyms for measurement conditions

Name	Description
VGS	Gate to source voltage
VDS	Drain to source voltage
VCE	Collector to emitter voltage
Ibr	Breakdown current
Irev	Diode reverse current
Vterm	Terminal voltage
Vlow	Lower voltage in measurement range
Vhigh	Upper voltage in measurement range
Vbias	Bias voltage
VG	Voltage potential on gate terminal.
VD	Voltage potential on drain terminal.
Vhw	Handle wafer voltage
VC	Voltage potential on collector terminal.
VPTUB	Voltage potential n substrate terminal
VL	Given voltage for leakage current measurement
VG-VT	Gate overdrive
Vrev	Reverse voltage
Isupply	Hall sensor supply current
Ic	Collector current
le	Emitter current
Ib	Base current
Id	Drain current
Idio	Diode current
Jfwd	Forward current density
f	Frequency
T	temperature
Tnom	Nominal temperature
Er	Relative permittivity of the dielectric
Dcyc	Duty cycle
Pwid	Pulse width
L	Device length
W	Device width
Pitch	Device pitch
LE	Emitter length
Ngates	Number of gates
NF	Number of finger
WF	Finger width

2. General → 2.7 Primitive devices

2.7 Primitive devices

The primitive device list does not include all the required module combinations for the stated modules. Refer also to the Module restrictions tables.

In addition to the capacitors stated in the primitive device list, it is also possible to use the capacitors built by the different gate oxides. These capacitors can be simulated by using the model of a transistor which has the respective oxide: for instance the ne and pe models in case of the 1.8V gate oxide. The operating conditions of the relating transistors are valid as well for these capacitors.

Minor changes of the simulation models might be generated due to continuous improvement of device and circuit simulation. Minor changes of models are described within the actual model data files. Please refer to further information within the current model path.

The qualification status of single devices can be checked in the Application Note "Primitive device release status" at "my X-FAB".

In addition to the listed primitive devices, non-volatile memory blocks are also available; please refer to the applicable process module details.

The following devices are available for design:

2.7.1 LP5MOS main module

MOS transistors

Name	Description	Required modules	Model rev.
ne	1.8V low power NMOS	-	10.0
nn	1.8V native Vt NMOS	-	10.0
pe	1.8V low power PMOS	-	10.0
pe_5 ⁽¹⁾	1.8V low power PMOS, 5 terminals	-	10.0
nel	1.8V low VT NMOS	LVT	10.0
pel	1.8V low VT PMOS	LVT	10.0
pel_5 ⁽¹⁾	1.8V low VT PMOS, 5 terminals	LVT	10.0
nesvt	1.8V medium VT NMOS	SVT	10.0
pesvt	1.8V medium VT PMOS 4 terminals	SVT	12.0
pesvt_5 ⁽¹⁾	1.8V medium VT PMOS 5 terminals	SVT	12.0
ne5	5.0V NMOS	-	12.0
nn5	5.0V native Vt NMOS	-	10.0
pe5	5.0V PMOS	-	12.0
pe5_5 ⁽¹⁾	5.0V PMOS, 5 terminals	-	12.0
peti	1.8V PMOS (NTUB)	DTI and HVN	12.0
pe5ti	5.0V PMOS (NTUB)	DTI and HVN	12.0
nd5	5.0V depletion NMOS	DEPL	10.0
nmva ⁽²⁾⁽³⁾	10V drain extension NMOS	DTI	
nmvaa ⁽³⁾	10V drain extension NMOS	DTI	12.0
nmvab ⁽³⁾	10V drain extension NMOS, with drain ballast resistor	DTI	12.0
nmvb	12V NMOS	DTI and NMV	11.0
nmvc	15V NMOS	DTI and NMV	11.0
nmvd	20V NMOS	DTI and NMV	11.0
nmve	25V NMOS	DTI and NMV	11.0
nmvf	32V NMOS	DTI and NMV	11.0
ndmvd	20V depletion NMOS	DTI and DEPL and NMV	11.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ MOS transistors

Name	Description	Required modules	Model rev.
ndmvf	32V depletion NMOS	DTI and DEPL and NMV	11.0
pmva ⁽⁴⁾⁽³⁾	10V drain extension PMOS	DTI	
pmvaa ⁽³⁾	10V drain extension PMOS	DTI	12.0
pmvab ⁽³⁾	10V drain extension PMOS, with drain ballast resistor	DTI	12.0
pmvb	12V PMOS	DTI and PSUB and PMV	11.0
pmvd	18V PMOS	DTI and PSUB and PMV	11.0
pmve	25V PMOS	DTI and PSUB and PMV	11.0
pmvf	32V PMOS	DTI and PSUB and PMV	11.0
nhvta ⁽⁵⁾	Low Ron 40V NMOS	DTI and PSUB and NHVA	11.0
nhvtaa ⁽⁶⁾⁽⁵⁾	Low Ron 40V NMOS	DTI and PSUB and NHVA	11.0
nhvtb ⁽⁵⁾	40V NMOS	DTI and PSUB and NHVA	11.0
nhvu ⁽⁵⁾	60V NMOS	DTI and PSUB and NHVA	11.0
ndhv ⁽⁵⁾	40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
ndhvta ⁽⁵⁾	Low Ron 40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
ndhvtaa ⁽⁷⁾⁽⁵⁾	Low Ron 40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
phvta	Low Ron 40V PMOS	DTI and PSUB and PHVA	11.1
phvtb	40V PMOS	DTI and PSUB and PHVA	11.1
phvu	60V PMOS	DTI and PSUB and PHVA	11.1
nhvra ⁽⁸⁾	40V NMOS	DTI and PSUB and NHVR	10.0
nhvrb ⁽⁸⁾	60V NMOS	DTI and PSUB and NHVR	10.0
nhvrc ⁽⁸⁾	70V NMOS	DTI and PSUB and NHVR	10.0
nhvrd ⁽⁸⁾	85V NMOS	DTI and PSUB and NHVR	10.0
nhvre ⁽⁸⁾	100V NMOS	DTI and PSUB and NHVR	10.0
nhvrf ⁽⁹⁾	125V NMOS	DTI and PSUB and NHVR	10.0
ndhvrd ⁽⁸⁾	85V depletion NMOS	DTI and PSUB and NHVR and HVDEPL	10.0
ndhvrf ⁽⁹⁾	125V depletion NMOS	DTI and PSUB and NHVR and HVDEPL	10.0
phvra ⁽⁸⁾	40V PMOS	DTI and PSUB and PHVR	10.0
phvrb ⁽⁸⁾	60V PMOS	DTI and PSUB and PHVR	10.0
phvrc ⁽⁸⁾	70V PMOS	DTI and PSUB and PHVR	10.0
phvrd ⁽⁸⁾	85V PMOS	DTI and PSUB and PHVR	10.0
phvre ⁽⁸⁾	100V PMOS	DTI and PSUB and PHVR	10.0
phvrf ⁽⁹⁾	125V PMOS	DTI and PSUB and PHVR	10.0
nhsj1_7	100V Gen1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1_10	140V Gen 1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1_16c	200V Gen1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1b_2	45V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ MOS transistors

Name	Description	Required modules	Model rev.
nhsj1b_4	72V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_5	95V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_7	115V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_8	140V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1b_10	155V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_13	195V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_16	235V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_20	290V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVU	12.0
nhsj1a_28	375V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVU	12.0
phsj1_7	100V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj1_10	140V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj1_16c	200V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj2b_7	115V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
phsj2b_8	140V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_10	155V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_13	195V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_16	235V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_4	72V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_5	95V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_7	115V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_8	140V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_10	155V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ MOS transistors

Name	Description	Required modules	Model rev.
phsj1a_13	195V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_16	235V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_20	290V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	12.0
phsj1a_31	375V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	12.0

Note 1 This device is a variant of the corresponding basic device with connections to the underlying wells. Parameters of this device are identical to the corresponding basic device.

Note 2 The device nmva is superseded by nmvaa. nmvaa must not be used for any new designs.

Note 3 Please also refer to the "[xt018-ApplicationNote-10V_MOSFET](#)" available on "my X-FAB".

Note 4 The device pmva is superseded by pmvaa. pmvaa must not be used for any new designs.

Note 5 Please also refer to the "[xt018-ApplicationNote-NHVA_Module_HV_Transistors](#)" available on "my X-FAB".

Note 6 nhvtaa provides better avalanche robustness than nhvta

Note 7 ndhvtaa provides better avalanche robustness than ndhvta

Note 8 The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Note 9 This device is intended to enhance the ESD design window for 100V applications. The ESD design window may not be suitable for applications up to 125V.

Bipolar transistors

Name	Description	Required modules	Model rev.
qpva	1.8V vertical PNP bipolar transistor in PEPI; emitter area = 2µm x 2µm	PSUB	5.0
qpvb	1.8V vertical PNP bipolar transistor in PEPI; emitter area = 5µm x 5µm	PSUB	5.0
qpvc	1.8V vertical PNP bipolar transistor in PEPI; emitter area = 10µm x 10µm	PSUB	5.0
qpve	1.8V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 2µm x 2µm	-	5.0
qpvf	1.8V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 5µm x 5µm	-	5.0
qpvg	1.8V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 10µm x 10µm	-	5.0
qpva5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 2 µm x 2 µm	PSUB	5.0
qpvb5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 5 µm x 5 µm	PSUB	5.0
qpvc5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 10 µm x 10 µm	PSUB	5.0
qpve5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 2 µm x 2 µm	-	5.0
qpvf5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 5 µm x 5 µm	-	5.0
qpvg5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 10 µm x 10 µm	-	5.0
qnv5	5V high gain NPN bipolar transistor	DTI and PSUB and BJTC	5.0



2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ Bipolar transistors

Name	Description	Required modules	Model rev.
qpv5	5V high gain PNP bipolar transistor	DTI and PSUB and BJTA	5.0
qnvha	25V high gain NPN bipolar transistor	DTI and PSUB and BJTC	10.0
qpvha	25V high gain PNP bipolar transistor	DTI and PSUB and BJTA	10.0

Resistors

Name	Description	Required modules	Model rev.
rdn	1.8V NDIFF / PWELL1 resistor (non salicided)	-	6.0
rdp	1.8V PDIFF / NWELL1 resistor (non salicided)	-	6.0
rnw	1.8V NWELL1 / PSUB resistor (STI terminated)	-	10.0
rxw2ti	NWELL Resistor under active (DTI)	DTI and PSUB	10.0
rdn5	5.0V NDIFF / PWELL2 resistor (non salicided)	-	6.0
rdp5	5.0V PDIFF / NWELL2 resistor (non salicided)	-	10.0
rnw5	5.0V NWELL2 / PSUB resistor (STI terminated)	-	10.0
rnp1 ⁽¹⁾	N-doped POLY1 resistor (non salicided), 2 terminals	-	12.0
rnp1_3 ⁽²⁾	N-doped POLY1 resistor (non-salicided, underlying NWELL/PWELL2), 3 terminals	-	12.0
rnp1a_3 ⁽²⁾	N-doped POLY1 resistor (non-salicided, underlying PWELL1/PWELL3/PWELL5), 3 terminals	-	12.0
rpp1 ⁽¹⁾	P-doped POLY1 resistor (non-salicided), 2 terminals	-	12.0
rpp1_3 ⁽²⁾	P-doped POLY1 resistor (non-salicided, underlying PWELL), 3 terminals	-	12.0
rpp1nw_3 ⁽²⁾	P-doped POLY1 resistor (non-salicided, underlying NWELL), 3 terminals	-	12.0
rpp1s	salicided P-doped POLY1 resistor, 2 terminals	-	10.0
rpp1s_3 ⁽³⁾	salicided P-doped POLY1 resistor, 3 terminals	-	10.0
rnp1h	high ohmic N-doped POLY1 resistor (non salicided), 2 terminals	HRPOLY	10.0
rnp1h_3 ⁽³⁾	high ohmic N-doped POLY1 resistor (non salicided), 3 terminals	HRPOLY	10.0
rpp1k1	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.0
rpp1k1_3 ⁽³⁾	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.0
rpp1k1a	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.0
rpp1k1a_3 ⁽³⁾	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.0
rm1	metal 1 resistor	-	6.0
rm2	metal 2 resistor	-	6.0
rm3	metal 3 resistor	MET3	6.0
rm4	metal 4 resistor	MET4	6.0
rm5	metal 5 resistor	MET5	6.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ Resistors

Name	Description	Required modules	Model rev.
rmtpl	top metal resistor	METMID	6.0
rmtpl	thick metal resistor	METTHK	6.0
rmdl	thick copper redistribution resistor	THKCOP	4.1

Note 1 The 2-terminal poly resistor devices do not consider the underlying wells. As a result of this simplification, the models are less accurate than their 3-terminal counterparts, which do account for the underlying well configuration.

Note 2 These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency.

Note 3 These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency. Parameters of these devices are identical to the corresponding basic device.

Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
mosvc	1.8V N-type Varactor	-	-	5.0
mosvc5	5V N-type Varactor	-	-	5.0
mosvcti	1.8V P-type Varactor (DTI)	DTI	-	5.0
mosvc5ti	5V P-type Varactor (DTI)	DTI	-	5.0
csandwt3	POLY1 / metal1/ metal2/ metal3 capacitor	MET3	-	6.0
csandwt4	POLY1 / metal1/ metal2/ metal3/ metal4 capacitor	MET4	-	6.0
csandwt5	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 capacitor	MET5	-	6.0
csp5tl_3	300V active/ metal 1/ metal 2/ metal 3/ metal 4/ top metal/ thick metal capacitor, 3 terminals	CSP5L	MET5	12.0
csp5tla_3	400V active/ metal 2/ metal 4/ thick metal capacitor, 3 terminals	CSP5L	MET5	12.0
cif3	100V metal1/metal2/metal3 fringe capacitor	MET3	-	8.0
cif4	100V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	8.0
cif5	100V metal1/metal2/metal3/metal4/ metal5 fringe capacitor	MET5	-	8.0
cift4	100V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	9.0
cift5	100V metal1/metal2/metal3/metal4/ metaltop fringe capacitor	MET4 and METMID	MET5	9.0
cift6	100V metal1/metal2/metal3/metal4/ metal5/metaltop fringe capacitor	MET5 and METMID	-	9.0
csf2p	POLY1/metal1/metal2 fringe capacitor	-	-	6.1
csf3p	POLY1/metal1/metal2/metal3 fringe capacitor	MET3	-	6.1
cif3a	30V metal1/metal2/metal3 fringe capacitor	MET3	-	12.0
csf3	10V metal1/metal2/metal3 fringe capacitor	MET3	-	6.0
csf3a	60V metal1/metal2/metal3 fringe capacitor	MET3	-	6.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cif4a	30V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	12.0
csf4	10V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	6.0
csf4a	60V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	6.0
cif5a	30V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	12.0
csf5	10V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	6.0
csf5a	60V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	6.0
cift4a ⁽¹⁾	30V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	12.0
csft4	10V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	6.0
csft4a	60V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	6.0
cift5a ⁽¹⁾	30V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	12.0
csft5	10V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	6.0
csft5a	60V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	6.0
cift6a ⁽¹⁾	30V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	12.0
csft6	10V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	6.0
csft6a	60V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	6.0
cmm3	single MIM capacitor between metal2 and metal3	MET3 and MIM23	-	7.0
cmm4	single MIM capacitor between metal3 and metal4	MET4 and MIM34	-	6.0
cmm5	single MIM capacitor between metal4 and metal5	MET5 and MIM45	-	7.0
cmm3t	single MIM capacitor between metal 2 and metaltop	METMID and MIM	MET3	6.0
cmm4t	single MIM capacitor between metal3 and metaltop	MET3 and METMID and MIM	MET4	6.0
cmm5t	single MIM capacitor between metal4 and metaltop	MET4 and METMID and MIM	MET5	6.0
cmm6t	single MIM capacitor between metal5 and metaltop	MET5 and METMID and MIM	-	6.0
cmmh3	single MIM capacitor (high capacitance) between metal2 and metal3	MET3 and MIMH23	-	7.0
cmmh4	single MIM capacitor (high capacitance) between metal3 and metal4	MET4 and MIMH34	-	7.0
cmmh5	single MIM capacitor (high capacitance) between metal4 and metal5	MET5 and MIMH45	-	7.0



2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cmmh3t	single MIM capacitor (high capacitance) between metal2 and metaltop	METMID and MIMH	MET3	6.0
cmmh4t	single MIM capacitor (high capacitance) between metal3 and metaltop	MET3 and METMID and MIMH	MET4	6.0
cmmh5t	single MIM capacitor (high capacitance) between metal4 and metaltop	MET4 and METMID and MIMH	MET5	6.0
cmmh6t	single MIM capacitor (high capacitance) between metal5 and metaltop	MET5 and METMID and MIMH	-	6.0
cdmm4	double MIM capacitor between metal2, metal3 and metal4	MET4 and DMIM	-	6.0
cdmm4t	double MIM capacitor between metal2, metal3 and metaltop	MET3 and METMID and DMIM	MET4	6.0
cdmmh4	double MIM capacitor (high capacitance) between metal2, metal3 and metal4	MET4 and DMIMH	-	6.0
cdmmh4t	double MIM capacitor (high capacitance) between metal2, metal3 and metaltop	MET3 and METMID and DMIMH	MET4	6.0
cdmm5	double MIM capacitor between metal3, metal4 and metal5	MET5 and DMIM3	-	7.0
cdmm5t	double MIM capacitor between metal3, metal4 and metaltop	MET4 and METMID and DMIM3	MET5	7.0
ctmm5	triple MIM capacitor between metal2, metal3, metal4 and metal5	MET5 and TMIM	-	6.0
cdmmh5	double MIM capacitor (high capacitance) between metal3, metal4 and metal5	MET5 and DMIMH3	-	7.0
ctmm5t	triple MIM capacitor between metal2, metal3, metal4 and metaltop	MET4 and METMID and TMIM	MET5	6.0
cdmmh5t	double MIM capacitor (high capacitance) between metal3, metal4 and metaltop	MET4 and METMID and DMIMH3	MET5	7.0
ctmmh5	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metal5	MET5 and TMIMH	-	6.0
ctmmh5t	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metaltop	MET4 and METMID and TMIMH	MET5	6.0
cmmh4l	single MIM capacitor (high capacitance) between metal3 and metal thick	MIMH and MET3 and METTHK	MET4 or METMID	6.0
cmmh5l	single MIM capacitor (high capacitance) between metal4 and metal thick	MIMH and MET4 and METTHK	MET5 or METMID	6.0
cmmh6l	single MIM capacitor (high capacitance) between metal5 and metal thick	MIMH and MET5 and METTHK	METMID	6.0

Note 1 This device is under development. All values represent the status which have been obtained during the development phase and are subject to change.

Diodes

Name	Description	Required modules	Model rev.
dn	diode NDIFF / PWELL1,3,5 (1.8V)	-	7.0

2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ Diodes

Name	Description	Required modules	Model rev.
dnn ⁽¹⁾	diode NDIFF / PTUB_SUB (1.8V)	-	7.0
dp	diode PDIFF / NWELL1,3,5 (1.8V)	-	7.0
dnw	diode NWELL1,3,5 / PWELL1 (1.8V)	-	7.0
dn5	diode NDIFF / PWELL2 (5.0V)	-	7.0
dnn5 ⁽¹⁾	diode NDIFF / PTUB_SUB (5.0V)	-	7.0
dp5	diode PDIFF / NWELL2 (5.0V)	-	7.0
dnw5	diode NWELL2 / PWELL2 (5.0V)	-	7.0
dfwdpa	5.0V rectifier p+/n diode	DTI and PSUB and HVN and DNC	7.0
dfwdn5	6.0V rectifier n+/p diode	DTI and PSUB	10.0
dfwdnb	12V rectifier diode	DTI and NMV	9.0
dfwdnc	15V rectifier diode	DTI and NMV	9.0
dfwdnd	20V rectifier diode	DTI and NMV	9.0
dfwdnt	40V rectifier diode	DTI and PSUB and NHVA	10.0
dfwdnu	60V rectifier diode	DTI and PSUB and NHVA	10.0
dfwdnhc	70V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhd	85V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhe	100V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhf	125V rectifier diode	DTI and PSUB and NHVR	9.0
dfwnsj1_7	100V Gen 1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1_10	140V Gen 1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1_16c	200V Gen1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1b_2	45V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_4	72V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_5	95V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_7	115V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_8	140V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1b_10	155V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_13	195V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_16	235V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_20	290V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	12.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ Diodes

Name	Description	Required modules	Model rev.
dfwnsj1a_28	375V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHUV	12.0
dhw2a	100V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw2	140V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw3	200V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw2b	115V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw2c	160V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw3c	235V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw4c	280V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVM	11.0
dhw4d	360V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHUV	11.0
dhw5d	420V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHUV	11.0
ds5a	5V Schottky diode	HVN and DTI	12.0
ds5b ⁽²⁾	5V Schottky diode	PSUB and DTI	12.0
dpp6	6V P-type protection diode (DTI)	HVN and DNC and DTI	10.0
dnp7	7V N-type protection diode (DTI)	DPC and DTI	12.0
dpp7	7V P-type protection diode (DTI)	HVN and DNC and DTI	10.0
dnpa	8V N-type protection diode	PSUB and (DIODEA or NHVA or NHVR)	11.0
dnpati	8V N-type protection diode (DTI)	DTI and PSUB and (DIODEA or NHVA or NHVR)	11.0
dza ⁽³⁾	5.3V Zener diode, 2 terminals	PSUB and DIODEB	10.0
dzati ⁽³⁾	5.3V Zener diode (DTI), 2 terminals	DTI and PSUB and DIODEB	11.1
dzbt1 ⁽³⁾	5.3V Zener diode (DTI), 3 terminals	DTI and PSUB and DIODEC	7.0
dzcti ⁽⁴⁾⁽³⁾	5.3V Zener diode (DTI), 2 terminals	DTI and PSUB and DIODEC	12.0
dfwdnha ⁽⁵⁾	diode drain / bulk for nhvra	DTI and PSUB and NHVR	8.0
dfwdnhb ⁽⁵⁾	diode drain / bulk for nhvrb	DTI and PSUB and NHVR	8.0
dfwdpta ⁽⁵⁾	diode drain / bulk for phvta	DTI and PSUB and PHVA	10.0
dfwdptb ⁽⁵⁾	diode drain / bulk for phvtb	DTI and PSUB and PHVA	10.0
dfwdpdu ⁽⁵⁾	diode drain / bulk for phvu	DTI and PSUB and PHVA	10.0
dfwdgne ⁽⁵⁾	diode drain / bulk for nmve	DTI and NMV	9.0
dfwddnf ⁽⁵⁾	diode drain / bulk for nmvf	DTI and NMV	9.0
dfwdpaa ⁽⁵⁾	diode drain / bulk for pmvaa	DTI	12.0
dfwdpab ⁽⁵⁾	diode drain / bulk for pmvab	DTI	12.0
dfwdpbb ⁽⁵⁾	diode drain / bulk for pmvb	DTI and PSUB and PMV	11.0
dfwdpd ⁽⁵⁾	diode drain / bulk for pmvd	DTI and PSUB and PMV	10.0
dfwdpe ⁽⁵⁾	diode drain / bulk for pmve	DTI and PSUB and PMV	8.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ Diodes

Name	Description	Required modules	Model rev.
dfwdpf ⁽⁵⁾	diode drain / bulk for pmvf	DTI and PSUB and PMV	8.0
dfwdpha ⁽⁵⁾	diode drain / bulk for phvra	DTI and PSUB and PHVR	8.0
dfwdphb ⁽⁵⁾	diode drain / bulk for phvrb	DTI and PSUB and PHVR	8.0
dfwdphc ⁽⁵⁾	diode drain / bulk for phvrc	DTI and PSUB and PHVR	8.0
dfwdphd ⁽⁵⁾	diode drain / bulk for phvrd	DTI and PSUB and PHVR	9.0
dfwdphe ⁽⁵⁾	diode drain / bulk for phvre	DTI and PSUB and PHVR	9.0
dfwdphf ⁽⁵⁾	diode drain / bulk for phvrf	DTI and PSUB and PHVR	8.1
dfwpsj1_7 ⁽⁵⁾	diode drain / bulk for phsj1_7	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj1_10 ⁽⁵⁾	diode drain / bulk for phsj1_10	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj1_16c ⁽⁵⁾	diode drain / bulk for phsj1_16c	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj2b_7 ⁽⁵⁾	diode drain / bulk for phsj2b_7	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj2b_8 ⁽⁵⁾	diode drain / bulk for phsj2b_8	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_10 ⁽⁵⁾	diode drain / bulk for phsj2b_10	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_13 ⁽⁵⁾	diode drain / bulk for phsj2b_13	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_16 ⁽⁵⁾	diode drain / bulk for phsj2b_16	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_4 ⁽⁵⁾	diode drain / bulk for phsj1a_4	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_5 ⁽⁵⁾	diode drain / bulk for phsj1a_5	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_7 ⁽⁵⁾	diode drain / bulk for phsj1a_7	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_8 ⁽⁵⁾	diode drain / bulk for phsj1a_8	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_10 ⁽⁵⁾	diode drain / bulk for phsj1a_10	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_13 ⁽⁵⁾	diode drain / bulk for phsj1a_13	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_16 ⁽⁵⁾	diode drain / bulk for phsj1a_16	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_20 ⁽⁵⁾	diode drain / bulk for phsj1a_20	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	11.0
dfwpsj1a_31 ⁽⁵⁾	diode drain / bulk for phsj1a_31	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	11.0
dfwdnaa ⁽⁵⁾	diode drain / bulk for nmvaa	DTI	12.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ Diodes

Name	Description	Required modules	Model rev.
dfwdnab ⁽⁵⁾	diode drain / bulk for nmvab	DTI	12.0

Note 1 This diode is only available along with the corresponding transistor where it is used as source/drain**Note 2** ds5b provides a similar device to ds5a but with a lower mask count**Note 3** Please also refer to the "[xt018-ApplicationNote-Zener_Diodes](#)" available in "my X-FAB".**Note 4** dzcti provides a similar device to dzbt1 but with a smaller pitch**Note 5** This device can only be used as a parasitic diode of the transistor noted in the description**Memories**

Name	Description	Required modules	Model rev.
pfuse	polysilicon fuse	-	5.0

IGBTs

Name	Description	Required modules	Model rev.
nisj1_16	200V Gen1 SJ NIGBT	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and NBUF and DPC	12.0

Virtual devices

Name	Description	Required modules	Model rev.
tag_m400v ⁽¹⁾	defines voltage class for net < -300V	-	11.0
tag_m300v ⁽¹⁾	defines voltage class for net \geq -300V < -200V	-	11.0
tag_m200v ⁽¹⁾	defines voltage class for net \geq -200V < -100V	-	7.0
tag_m100v ⁽¹⁾	defines voltage class for net \geq -100V < -60V	-	7.0
tag_m60v ⁽¹⁾	defines voltage class for net \geq -60V < -25V	-	7.0
tag_m25v ⁽¹⁾	defines voltage class for net \geq -25V < 0V	-	7.0
tag_25v ⁽¹⁾	defines voltage class for net \geq 0V \leq 25V	-	7.0
tag_60v ⁽¹⁾	defines voltage class for net >25V \leq 60V	-	7.0
tag_100v ⁽¹⁾	defines voltage class for net >60V \leq 100V	-	7.0
tag_200v ⁽¹⁾	defines voltage class for net >100V \leq 200V	-	7.0
tag_300v ⁽¹⁾	defines voltage class for net > 200V \leq 300V	-	11.0
tag_400v ⁽¹⁾	defines voltage class for net > 300V	-	11.0

Note 1 These devices are not fabricated on silicon; they are available for DRC and LVS voltage class checks only. For further information, please refer to the design related guideline "Voltage class definitions".**ESD devices**

Name	Description	Required modules	Model rev.
rdn5_dpc ⁽¹⁾	NDIFF drain ballast resistor of ESD NMOS (DPC in PWELL2)	DPC	6.0
rdn5_pw4 ⁽¹⁾	NDIFF drain ballast resistor of ESD NMOS (PWELL4 in PWELL2)	NHVA or DIODEA or NHVR	6.0

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2. General → 2.7 Primitive devices→ 2.7.1 LP5MOS main module→ ESD devices

Name	Description	Required modules	Model rev.
rnw_scr ⁽¹⁾	1.8V LV NMOS triggered SCR dio/res network resistor	-	10.0
rnw5_scr ⁽¹⁾	5V LV NMOS triggered SCR dio/res network resistor	-	10.0

Note 1 These devices are only allowed to be used for ESD protection.
 Please refer to ESD documentation on "my X-FAB":
["XT018-DesignGuideline-ESD_and_LU"](#)
["XT018 TLP Characteristics"](#)
["XT018 Technical Report MOS TLP Characteristics"](#)
["XT018 Technical Report UHV TLP Characteristics"](#)

2.7.2 MOS5 main module

MOS transistors

Name	Description	Required modules	Model rev.
ne5	5.0V NMOS	-	12.0
nn5	5.0V native Vt NMOS	-	10.0
pe5	5.0V PMOS	-	12.0
pe5_5 ⁽¹⁾	5.0V PMOS, 5 terminals	-	12.0
pe5ti	5.0V PMOS (NTUB)	DTI and HVN	12.0
nd5	5.0V depletion NMOS	DEPL	10.0
nmva ⁽²⁾⁽³⁾	10V drain extension NMOS	DTI	
nmvaa ⁽³⁾	10V drain extension NMOS	DTI	12.0
nmvab ⁽³⁾	10V drain extension NMOS, with drain ballast resistor	DTI	12.0
nmvb	12V NMOS	DTI and NMV	11.0
nmvc	15V NMOS	DTI and NMV	11.0
nmvd	20V NMOS	DTI and NMV	11.0
nmve	25V NMOS	DTI and NMV	11.0
nmvf	32V NMOS	DTI and NMV	11.0
ndmvd	20V depletion NMOS	DTI and DEPL and NMV	11.0
ndmvf	32V depletion NMOS	DTI and DEPL and NMV	11.0
pmva ⁽⁴⁾⁽³⁾	10V drain extension PMOS	DTI	
pmvaa ⁽³⁾	10V drain extension PMOS	DTI	12.0
pmvab ⁽³⁾	10V drain extension PMOS, with drain ballast resistor	DTI	12.0
pmvb	12V PMOS	DTI and PSUB and PMV	11.0
pmvd	18V PMOS	DTI and PSUB and PMV	11.0
pmve	25V PMOS	DTI and PSUB and PMV	11.0
pmvf	32V PMOS	DTI and PSUB and PMV	11.0
nhvta ⁽⁵⁾	Low Ron 40V NMOS	DTI and PSUB and NHVA	11.0
nhvtaa ⁽⁶⁾⁽⁵⁾	Low Ron 40V NMOS	DTI and PSUB and NHVA	11.0
nhvtb ⁽⁵⁾	40V NMOS	DTI and PSUB and NHVA	11.0
nhvu ⁽⁵⁾	60V NMOS	DTI and PSUB and NHVA	11.0
ndhvt ⁽⁵⁾	40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1



2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ MOS transistors

Name	Description	Required modules	Model rev.
ndhvta ⁽⁵⁾	Low Ron 40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
ndhvtaa ⁽⁷⁾⁽⁵⁾	Low Ron 40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
phvta	Low Ron 40V PMOS	DTI and PSUB and PHVA	11.1
phvtb	40V PMOS	DTI and PSUB and PHVA	11.1
phvu	60V PMOS	DTI and PSUB and PHVA	11.1
nhvra ⁽⁸⁾	40V NMOS	DTI and PSUB and NHVR	10.0
nhvrb ⁽⁸⁾	60V NMOS	DTI and PSUB and NHVR	10.0
nhvrc ⁽⁸⁾	70V NMOS	DTI and PSUB and NHVR	10.0
nhvrd ⁽⁸⁾	85V NMOS	DTI and PSUB and NHVR	10.0
nhvre ⁽⁸⁾	100V NMOS	DTI and PSUB and NHVR	10.0
nhvrf ⁽⁹⁾	125V NMOS	DTI and PSUB and NHVR	10.0
ndhvrdd ⁽⁸⁾	85V depletion NMOS	DTI and PSUB and NHVR and HVDEPL	10.0
ndhvrdf ⁽⁹⁾	125V depletion NMOS	DTI and PSUB and NHVR and HVDEPL	10.0
phvra ⁽⁸⁾	40V PMOS	DTI and PSUB and PHVR	10.0
phvrb ⁽⁸⁾	60V PMOS	DTI and PSUB and PHVR	10.0
phvrc ⁽⁸⁾	70V PMOS	DTI and PSUB and PHVR	10.0
phvrd ⁽⁸⁾	85V PMOS	DTI and PSUB and PHVR	10.0
phvre ⁽⁸⁾	100V PMOS	DTI and PSUB and PHVR	10.0
phvrf ⁽⁹⁾	125V PMOS	DTI and PSUB and PHVR	10.0
nhsj1_7	100V Gen1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1_10	140V Gen 1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1_16c	200V Gen1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1b_2	45V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_4	72V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_5	95V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_7	115V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_8	140V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1b_10	155V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_13	195V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0

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2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ MOS transistors

Name	Description	Required modules	Model rev.
nhsj1a_16	235V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_20	290V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVU	12.0
nhsj1a_28	375V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVU	12.0
phsj1_7	100V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj1_10	140V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj1_16c	200V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj2b_7	115V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
phsj2b_8	140V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_10	155V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_13	195V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_16	235V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_4	72V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_5	95V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_7	115V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_8	140V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_10	155V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_13	195V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_16	235V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_20	290V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	12.0

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2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ MOS transistors

Name	Description	Required modules	Model rev.
phsj1a_31	375V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHUV	12.0

- Note 1** This device is a variant of the corresponding basic device with connections to the underlying wells. Parameters of this device are identical to the corresponding basic device.
- Note 2** The device nmva is superseded by nmvaa. nmva must not be used for any new designs.
- Note 3** Please also refer to the "[xt018-ApplicationNote-10V_MOSFET](#)" available on "my X-FAB".
- Note 4** The device pmva is superseded by pmvaa. pmva must not be used for any new designs.
- Note 5** Please also refer to the "[xt018-ApplicationNote-NHVA_Module_HV_Transistors](#)" available on "my X-FAB".
- Note 6** nhvtaa provides better avalanche robustness than nhvta
- Note 7** ndhvtaa provides better avalanche robustness than ndhvta
- Note 8** The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.
- Note 9** This device is intended to enhance the ESD design window for 100V applications. The ESD design window may not be suitable for applications up to 125V.

Bipolar transistors

Name	Description	Required modules	Model rev.
qpva5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 2 μm x 2 μm	PSUB	5.0
qpvb5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 5 μm x 5 μm	PSUB	5.0
qpvc5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 10 μm x 10 μm	PSUB	5.0
qpve5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 2 μm x 2 μm	-	5.0
qpvf5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 5 μm x 5 μm	-	5.0
qpgv5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 10 μm x 10 μm	-	5.0
qnv5	5V high gain NPN bipolar transistor	DTI and PSUB and BJTC	5.0
qpv5	5V high gain PNP bipolar transistor	DTI and PSUB and BJTA	5.0
qnvhha	25V high gain NPN bipolar transistor	DTI and PSUB and BJTC	10.0
qpvha	25V high gain PNP bipolar transistor	DTI and PSUB and BJTA	10.0

Resistors

Name	Description	Required modules	Model rev.
rxw2ti	NWELL Resistor under active (DTI)	DTI and PSUB	10.0
rdn5	5.0V NDIFF / PWELL2 resistor (non salicided)	-	6.0
rdp5	5.0V PDIFF / NWELL2 resistor (non salicided)	-	10.0
rnw5	5.0V NWELL2 / PSUB resistor (STI terminated)	-	10.0
rnp1 ⁽¹⁾	N-doped POLY1 resistor (non salicided), 2 terminals	-	12.0
rnp1_3 ⁽²⁾	N-doped POLY1 resistor (non-salicided, underlying NWELL/PWELL2), 3 terminals	-	12.0

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2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ Resistors

Name	Description	Required modules	Model rev.
rpp1 ⁽¹⁾	P-doped POLY1 resistor (non-salicided), 2 terminals	-	12.0
rpp1_3 ⁽²⁾	P-doped POLY1 resistor (non-salicided, underlying PWELL), 3 terminals	-	12.0
rpp1nw_3 ⁽²⁾	P-doped POLY1 resistor (non-salicided, underlying NWELL), 3 terminals	-	12.0
rpp1s	salicided P-doped POLY1 resistor, 2 terminals	-	10.0
rpp1s_3 ⁽³⁾	salicided P-doped POLY1 resistor, 3 terminals	-	10.0
rnp1h	high ohmic N-doped POLY1 resistor (non salicided), 2 terminals	HRPOLY	10.0
rnp1h_3 ⁽³⁾	high ohmic N-doped POLY1 resistor (non salicided), 3 terminals	HRPOLY	10.0
rpp1k1	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.0
rpp1k1_3 ⁽³⁾	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.0
rpp1k1a	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.0
rpp1k1a_3 ⁽³⁾	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.0
rm1	metal 1 resistor	-	6.0
rm2	metal 2 resistor	-	6.0
rm3	metal 3 resistor	MET3	6.0
rm4	metal 4 resistor	MET4	6.0
rm5	metal 5 resistor	MET5	6.0
rmtpl	top metal resistor	METMID	6.0
rmtpl	thick metal resistor	METTHK	6.0
rnrld	thick copper redistribution resistor	THKCOP	4.1

Note 1 The 2-terminal poly resistor devices do not consider the underlying wells. As a result of this simplification, the models are less accurate than their 3-terminal counterparts, which do account for the underlying well configuration.

Note 2 These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency.

Note 3 These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency. Parameters of these devices are identical to the corresponding basic device.

Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
mosvc5	5V N-type Varactor	-	-	5.0
mosvc5ti	5V P-type Varactor (DTI)	DTI	-	5.0
csandwt3	POLY1 / metal1/ metal2/ metal3 capacitor	MET3	-	6.0
csandwt4	POLY1 / metal1/ metal2/ metal3/ metal4 capacitor	MET4	-	6.0
csandwt5	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 capacitor	MET5	-	6.0



2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
csp5tl_3	300V active/ metal 1/ metal 2/ metal 3/ metal 4/ top metal/ thick metal capacitor, 3 terminals	CSP5L	MET5	12.0
csp5tla_3	400V active/ metal 2/ metal 4/ thick metal capacitor, 3 terminals	CSP5L	MET5	12.0
cif3	100V metal1/metal2/metal3 fringe capacitor	MET3	-	8.0
cif4	100V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	8.0
cif5	100V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	8.0
cift4	100V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	9.0
cift5	100V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	9.0
cift6	100V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	9.0
csf2p	POLY1/metal1/metal2 fringe capacitor	-	-	6.1
csf3p	POLY1/metal1/metal2/metal3 fringe capacitor	MET3	-	6.1
cif3a	30V metal1/metal2/metal3 fringe capacitor	MET3	-	12.0
csf3	10V metal1/metal2/metal3 fringe capacitor	MET3	-	6.0
csf3a	60V metal1/metal2/metal3 fringe capacitor	MET3	-	6.0
cif4a	30V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	12.0
csf4	10V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	6.0
csf4a	60V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	6.0
cif5a	30V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	12.0
csf5	10V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	6.0
csf5a	60V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	6.0
cift4a ⁽¹⁾	30V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	12.0
csft4	10V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	6.0
csft4a	60V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	6.0
cift5a ⁽¹⁾	30V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	12.0
csft5	10V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	6.0
csft5a	60V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	6.0

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2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cift6a ⁽¹⁾	30V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	12.0
csft6	10V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	6.0
csft6a	60V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	6.0
cmm3	single MIM capacitor between metal2 and metal3	MET3 and MIM23	-	7.0
cmm4	single MIM capacitor between metal3 and metal4	MET4 and MIM34	-	6.0
cmm5	single MIM capacitor between metal4 and metal5	MET5 and MIM45	-	7.0
cmm3t	single MIM capacitor between metal 2 and metaltop	METMID and MIM	MET3	6.0
cmm4t	single MIM capacitor between metal3 and metaltop	MET3 and METMID and MIM	MET4	6.0
cmm5t	single MIM capacitor between metal4 and metaltop	MET4 and METMID and MIM	MET5	6.0
cmm6t	single MIM capacitor between metal5 and metaltop	MET5 and METMID and MIM	-	6.0
cmmh3	single MIM capacitor (high capacitance) between metal2 and metal3	MET3 and MIMH23	-	7.0
cmmh4	single MIM capacitor (high capacitance) between metal3 and metal4	MET4 and MIMH34	-	7.0
cmmh5	single MIM capacitor (high capacitance) between metal4 and metal5	MET5 and MIMH45	-	7.0
cmmh3t	single MIM capacitor (high capacitance) between metal2 and metaltop	METMID and MIMH	MET3	6.0
cmmh4t	single MIM capacitor (high capacitance) between metal3 and metaltop	MET3 and METMID and MIMH	MET4	6.0
cmmh5t	single MIM capacitor (high capacitance) between metal4 and metaltop	MET4 and METMID and MIMH	MET5	6.0
cmmh6t	single MIM capacitor (high capacitance) between metal5 and metaltop	MET5 and METMID and MIMH	-	6.0
cdmm4	double MIM capacitor between metal2, metal3 and metal4	MET4 and DMIM	-	6.0
cdmm4t	double MIM capacitor between metal2, metal3 and metaltop	MET3 and METMID and DMIM	MET4	6.0
cdmmh4	double MIM capacitor (high capacitance) between metal2, metal3 and metal4	MET4 and DMIMH	-	6.0
cdmmh4t	double MIM capacitor (high capacitance) between metal2, metal3 and metaltop	MET3 and METMID and DMIMH	MET4	6.0
cdmm5	double MIM capacitor between metal3, metal4 and metal5	MET5 and DMIM3	-	7.0
cdmm5t	double MIM capacitor between metal3, metal4 and metaltop	MET4 and METMID and DMIM3	MET5	7.0
ctmm5	triple MIM capacitor between metal2, metal3, metal4 and metal5	MET5 and TMIM	-	6.0



2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cdmmh5	double MIM capacitor (high capacitance) between metal3, metal4 and metal5	MET5 and DMIMH3	-	7.0
ctmm5t	triple MIM capacitor between metal2, metal3, metal4 and metatop	MET4 and METMID and TMIM	MET5	6.0
cdmmh5t	double MIM capacitor (high capacitance) between metal3, metal4 and metatop	MET4 and METMID and DMIMH3	MET5	7.0
ctmmh5	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metal5	MET5 and TMIMH	-	6.0
ctmmh5t	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metatop	MET4 and METMID and TMIMH	MET5	6.0
cmmh4l	single MIM capacitor (high capacitance) between metal3 and metal thick	MIMH and MET3 and METTHK	MET4 or METMID	6.0
cmmh5l	single MIM capacitor (high capacitance) between metal4 and metal thick	MIMH and MET4 and METTHK	MET5 or METMID	6.0
cmmh6l	single MIM capacitor (high capacitance) between metal5 and metal thick	MIMH and MET5 and METTHK	METMID	6.0

Note 1 This device is under development. All values represent the status which have been obtained during the development phase and are subject to change.

Diodes

Name	Description	Required modules	Model rev.
dn5	diode NDIFF / PWELL2 (5.0V)	-	7.0
dnn5 ⁽¹⁾	diode NDIFF / PTUB_SUB (5.0V)	-	7.0
dp5	diode PDIFF / NWELL2 (5.0V)	-	7.0
dnw5	diode NWELL2 / PWELL2 (5.0V)	-	7.0
dfwdpa	5.0V rectifier p+/n diode	DTI and PSUB and HVN and DNC	7.0
dfwdn5	6.0V rectifier n+/p diode	DTI and PSUB	10.0
dfwdnb	12V rectifier diode	DTI and NMV	9.0
dfwdnc	15V rectifier diode	DTI and NMV	9.0
dfwdnd	20V rectifier diode	DTI and NMV	9.0
dfwdnt	40V rectifier diode	DTI and PSUB and NHVA	10.0
dfwdnu	60V rectifier diode	DTI and PSUB and NHVA	10.0
dfwdnhc	70V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhd	85V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhe	100V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhf	125V rectifier diode	DTI and PSUB and NHVR	9.0
dfwnsj1_7	100V Gen 1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1_10	140V Gen 1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1_16c	200V Gen1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0



2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ Diodes

Name	Description	Required modules	Model rev.
dfwnsj1b_2	45V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_4	72V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_5	95V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_7	115V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_8	140V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1b_10	155V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_13	195V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_16	235V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_20	290V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	12.0
dfwnsj1a_28	375V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	12.0
dhw2a	100V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw2	140V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw3	200V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw2b	115V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw2c	160V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw3c	235V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw4c	280V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVM	11.0
dhw4d	360V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVM	11.0
dhw5d	420V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVM	11.0
ds5a	5V Schottky diode	HVN and DTI	12.0
ds5b ⁽²⁾	5V Schottky diode	PSUB and DTI	12.0
dpp6	6V P-type protection diode (DTI)	HVN and DNC and DTI	10.0
dnp7	7V N-type protection diode (DTI)	DPC and DTI	12.0
dpp7	7V P-type protection diode (DTI)	HVN and DNC and DTI	10.0
dnpa	8V N-type protection diode	PSUB and (DIODEA or NHVA or NHVR)	11.0

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2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ Diodes

Name	Description	Required modules	Model rev.
dnpati	8V N-type protection diode (DTI)	DTI and PSUB and (DIODEA or NHVA or NHVR)	11.0
dza ⁽³⁾	5.3V Zener diode, 2 terminals	PSUB and DIODEB	10.0
dzati ⁽³⁾	5.3V Zener diode (DTI), 2 terminals	DTI and PSUB and DIODEB	11.1
dzbt ⁽³⁾	5.3V Zener diode (DTI), 3 terminals	DTI and PSUB and DIODEC	7.0
dzct ⁽⁴⁾⁽³⁾	5.3V Zener diode (DTI), 2 terminals	DTI and PSUB and DIODEC	12.0
dfwdnha ⁽⁵⁾	diode drain / bulk for nhvra	DTI and PSUB and NHVR	8.0
dfwdnhb ⁽⁵⁾	diode drain / bulk for nhvrb	DTI and PSUB and NHVR	8.0
dfwdpta ⁽⁵⁾	diode drain / bulk for phvta	DTI and PSUB and PHVA	10.0
dfwdptb ⁽⁵⁾	diode drain / bulk for phvtb	DTI and PSUB and PHVA	10.0
dfwdpdu ⁽⁵⁾	diode drain / bulk for phvu	DTI and PSUB and PHVA	10.0
dfwdgne ⁽⁵⁾	diode drain / bulk for nmve	DTI and NMV	9.0
dfwdnfv ⁽⁵⁾	diode drain / bulk for nmvf	DTI and NMV	9.0
dfwdpaa ⁽⁵⁾	diode drain / bulk for pmvaa	DTI	12.0
dfwdpab ⁽⁵⁾	diode drain / bulk for pmvab	DTI	12.0
dfwdpb ⁽⁵⁾	diode drain / bulk for pmvb	DTI and PSUB and PMV	11.0
dfwdpd ⁽⁵⁾	diode drain / bulk for pmvd	DTI and PSUB and PMV	10.0
dfwdpe ⁽⁵⁾	diode drain / bulk for pmve	DTI and PSUB and PMV	8.0
dfwdpf ⁽⁵⁾	diode drain / bulk for pmvf	DTI and PSUB and PMV	8.0
dfwdpha ⁽⁵⁾	diode drain / bulk for phvra	DTI and PSUB and PHVR	8.0
dfwdphb ⁽⁵⁾	diode drain / bulk for phvrb	DTI and PSUB and PHVR	8.0
dfwdphc ⁽⁵⁾	diode drain / bulk for phvrc	DTI and PSUB and PHVR	8.0
dfwdphd ⁽⁵⁾	diode drain / bulk for phvrd	DTI and PSUB and PHVR	9.0
dfwdphe ⁽⁵⁾	diode drain / bulk for phvre	DTI and PSUB and PHVR	9.0
dfwdphf ⁽⁵⁾	diode drain / bulk for phvrf	DTI and PSUB and PHVR	8.1
dfwpsj1_7 ⁽⁵⁾	diode drain / bulk for phsj1_7	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj1_10 ⁽⁵⁾	diode drain / bulk for phsj1_10	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj1_16c ⁽⁵⁾	diode drain / bulk for phsj1_16c	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj2b_7 ⁽⁵⁾	diode drain / bulk for phsj2b_7	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj2b_8 ⁽⁵⁾	diode drain / bulk for phsj2b_8	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_10 ⁽⁵⁾	diode drain / bulk for phsj2b_10	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_13 ⁽⁵⁾	diode drain / bulk for phsj2b_13	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_16 ⁽⁵⁾	diode drain / bulk for phsj2b_16	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_4 ⁽⁵⁾	diode drain / bulk for phsj1a_4	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0

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2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ Diodes

Name	Description	Required modules	Model rev.
dfwpsj1a_5 ⁽⁵⁾	diode drain / bulk for phsj1a_5	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_7 ⁽⁵⁾	diode drain / bulk for phsj1a_7	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_8 ⁽⁵⁾	diode drain / bulk for phsj1a_8	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_10 ⁽⁵⁾	diode drain / bulk for phsj1a_10	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_13 ⁽⁵⁾	diode drain / bulk for phsj1a_13	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_16 ⁽⁵⁾	diode drain / bulk for phsj1a_16	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_20 ⁽⁵⁾	diode drain / bulk for phsj1a_20	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_31 ⁽⁵⁾	diode drain / bulk for phsj1a_31	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwdnaa ⁽⁵⁾	diode drain / bulk for nmvaa	DTI	12.0
dfwdnab ⁽⁵⁾	diode drain / bulk for nmvab	DTI	12.0

Note 1 This diode is only available along with the corresponding transistor where it is used as source/drain

Note 2 ds5b provides a similar device to ds5a but with a lower mask count

Note 3 Please also refer to the "[xt018-ApplicationNote-Zener_Diodes](#)" available in "my X-FAB".

Note 4 dzcti provides a similar device to dzbt1 but with a smaller pitch

Note 5 This device can only be used as a parasitic diode of the transistor noted in the description

Memories

Name	Description	Required modules	Model rev.
pfuse	polysilicon fuse	-	5.0

IGBTs

Name	Description	Required modules	Model rev.
nisj1_16	200V Gen1 SJ NIGBT	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and NBUF and DPC	12.0

Virtual devices

Name	Description	Required modules	Model rev.
tag_m400v ⁽¹⁾	defines voltage class for net < -300V	-	11.0
tag_m300v ⁽¹⁾	defines voltage class for net \geq -300V < -200V	-	11.0
tag_m200v ⁽¹⁾	defines voltage class for net \geq -200V < -100V	-	7.0
tag_m100v ⁽¹⁾	defines voltage class for net \geq -100V < -60V	-	7.0
tag_m60v ⁽¹⁾	defines voltage class for net \geq -60V < -25V	-	7.0
tag_m25v ⁽¹⁾	defines voltage class for net \geq -25V < 0V	-	7.0



2. General → 2.7 Primitive devices→ 2.7.2 MOS5 main module→ Virtual devices

Name	Description	Required modules	Model rev.
tag_25v ⁽¹⁾	defines voltage class for net $\geq 0V \leq 25V$	-	7.0
tag_60v ⁽¹⁾	defines voltage class for net $>25V \leq 60V$	-	7.0
tag_100v ⁽¹⁾	defines voltage class for net $>60V \leq 100V$	-	7.0
tag_200v ⁽¹⁾	defines voltage class for net $>100V \leq 200V$	-	7.0
tag_300v ⁽¹⁾	defines voltage class for net $> 200V \leq 300V$	-	11.0
tag_400v ⁽¹⁾	defines voltage class for net $> 300V$	-	11.0

Note 1 These devices are not fabricated on silicon; they are available for DRC and LVS voltage class checks only. For further information, please refer to the design related guideline "Voltage class definitions".

ESD devices

Name	Description	Required modules	Model rev.
rdn5_dpc ⁽¹⁾	NDIFF drain ballast resistor of ESD NMOS (DPC in PWELL2)	DPC	6.0
rdn5_pw4 ⁽¹⁾	NDIFF drain ballast resistor of ESD NMOS (PWELL4 in PWELL2)	NHVA or DIODEA or NHVR	6.0
rnw5_scr ⁽¹⁾	5V LV NMOS triggered SCR dio/res network resistor	-	10.0

Note 1 These devices are only allowed to be used for ESD protection.
Please refer to ESD documentation on "my X-FAB":
["XT018-DesignGuideline-ESD_and_LU"](#)
["XT018 TLP Characteristics"](#)
["XT018 Technical Report MOS TLP Characteristics"](#)
["XT018 Technical Report UHV TLP Characteristics"](#)

3. Parameters

This section contains geometrical and electrical parameters that have been extracted primarily from measurements within the fabrication process or from special process monitor structures placed along the scribe lane.

Parameters which describe temperature dependence have been extracted in the temperature range $27^{\circ}\text{C} < T < 175^{\circ}\text{C}$. All the other measurements have been done at $T_0 = 27^{\circ}\text{C}$, unless otherwise stated.

The specified limits of the dispositional pass/fail process parameters:

LSL Lower Specification Limit
USL Upper Specification Limit

describe the parameter ranges of the delivered wafer quality. These parameter ranges are based on the 6 sigma values of the parameter distribution. These specification limits are the basis for Cp and Cpk evaluations.

For the following process parameters, the LSL and USL limits do not reflect the statistics of the process but merely represent that the value(s) pass(es) the particular limit:

- Parameters marked by a corresponding note

The stated LSL or USL limits of those parameters are selection limits only and are not allowed for Cp and Cpk evaluations.

For process parameters having a normal distribution, the Low and High values are the 3 sigma values of the parameter distribution.

For process parameters having a non-normal distribution, the Low and High values encompass the same fraction of the distribution as a +/- 3 sigma range would include for a normal distribution.

Designers may use the Low and High values to understand circuit sensitivities, but for more robust designs the wider parameter ranges available in the LSL and USL values should be used. Note that all of these values are also available in the simulation models.

For the following process parameters, the Low and High values (where quoted) do not reflect process statistics:

- Breakdown voltages having Low value only
- Punch-through voltages,
- Structural and geometrical parameters except gate oxide thickness,
- Wafer material parameters,
- Field threshold voltage parameters,
- Parasitic capacitance parameters,
- Junction diode capacitance parameters,
- Off-state leakage parameters
- Temperature coefficient parameters,
- Parameters which are marked by a corresponding note;

The device parameters must not be used for circuit simulation purposes. They are extracted from simplified model equations in order to increase the speed of the measurements. Special circuit simulation device parameters are related to the Process Related Guideline "Simulation Models". These are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. Therefore, device parameters may differ from their corresponding circuit simulation device parameters.

The breakdown voltage parameters within this section do not describe the allowed operating voltages of the devices. For maximum operating voltages required for reliable device operation, please refer to device operating conditions.

Only a subset of the parameters is measured regularly. The complete set of parameters is only available for wafers with updated process control monitor test structures.

Characteristic curves of the primitive devices showing measurement results of a typical wafer in comparison to the SPICE model simulations are available in the [Device Characteristics Documentation](#) (formerly Model Guides) on my X-FAB.

Operating Conditions

Functional operation of the device at conditions between maximum operating conditions and absolute maximum (or between minimum and absolute minimum) is not implied. Exposure to these conditions for extended periods may affect device reliability (e.g. hot carrier degradation, oxide breakdown). Applying conditions beyond absolute values may be destructive to the devices.



3. Parameters → 3.1 LP5MOS main module

In addition to the stated operating conditions, the process reliability parameters must also be considered. These include lifetimes and detailed SOA descriptions.

Parasitics have the same maximum operating voltage as the primitive device they exist within.

Junction Temperature

The junction temperature range is defined as:

Operating Conditions: $T_j = -40^{\circ}\text{C} \dots +175^{\circ}\text{C}$

Absolute maximum ratings: $T_j = -55^{\circ}\text{C} / +185^{\circ}\text{C}$

3.1 LP5MOS main module

3.1.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_ILD1	metal 1 / substrate equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
EPS_IMD1	metal 1 / metal 2 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
RSWAFDL	SOI wafer: device layer resistivity	66	100	134	Ωcm
RSWAFHW	SOI wafer: handle wafer resistivity	70	100	130	Ωcm
THD_ILD1	metal 1 - active dielectric thickness	840	990	1140	nm
THD_IMD1	metal 2 - metal 1 dielectric thickness	765	850	935	nm
THD_M1P1	metal 1 - poly 1 dielectric thickness	640	790	940	nm
THD_M1STI	metal 1 field dielectric thickness	1240	1390	1540	nm
THGN	1.8V gate oxide thickness (measured on NMOS capacitor)	3.9	4.1	4.3	nm
THGN5	5.0V gate oxide thickness (measured on NMOS capacitor)	12.2	12.7	13.2	nm
THGP	1.8V gate oxide thickness (measured on PMOS capacitor)	3.7	3.9	4.1	nm
THGP5	5.0V gate oxide thickness(measured on PMOS capacitor)	12.2	12.7	13.2	nm
THOBOX	SOI wafer: buried oxide thickness	950	1000	1050	nm
	Note: The thickness is given in reference to wafer supplier specification				
THV	passivation thickness	1570	1750	1930	nm
	Note: Passivation is composed from the following stack (bottom to top): silicon oxide/silicon nitride.				
THV_THK	passivation thickness with METTHK module	1920	2200	2480	nm
	Note: Passivation is composed from the following stack (bottom to top): silicon oxide/silicon nitride.				
TH_DL	SOI wafer: device layer thickness	3435	3500	3565	nm
	Note: The thickness is given in reference to wafer supplier specification				
TH_M1	metal 1 thickness	505	565	625	nm
TH_M2	metal 2 thickness	505	565	625	nm
TH_P1	poly 1 thickness	180	200	220	nm
TH_WAF	wafer thickness	710	725	740	μm
	Note: The thickness is given in reference to wafer supplier specification				
XJ_N	N+ source/ drain junction depth	-	0.2	-	μm
XJ_NW1	NWELL1 junction depth	-	1.5	-	μm

3. Parameters → 3.1 LP5MOS main module → 3.1.1 Device independent p... → Structural and geom...

Name	Description	Low	Typ	High	Unit
XJ_NW2	NWELL2 junction depth	-	1.5	-	µm
XJ_P	P+ source/ drain junction depth	-	0.2	-	µm
XT_STI	STI depth	360	400	440	nm

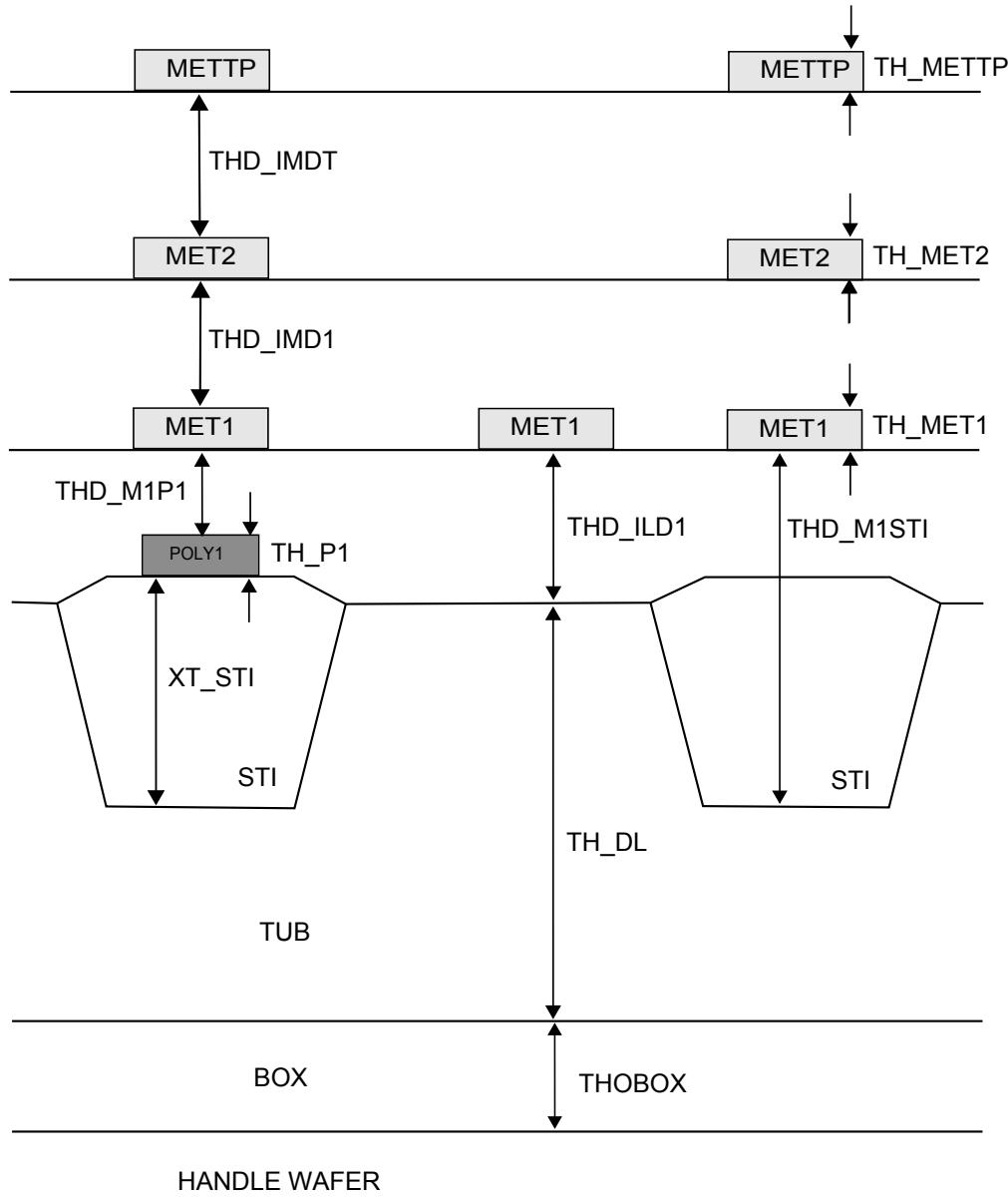


Figure 3.1 Cross-Sectional diagram showing layer thickness values

Parasitic field parameters

Name	Description	Low	Typ	High	Unit
VTFNM1PW1	n-channel threshold voltage metal 1 on field over PWELL1 @ VD=1.8V, Id=1µA, L=0.28µm, W=210µm	40	-	-	V
VTFNM1PW2	n-channel threshold voltage metal 1 on field over PWELL2 @ VD=5V, Id=1µA, L=0.28µm, W=210µm	40	-	-	V
VTFNP1PW1	n-channel threshold voltage poly 1 on field over PWELL1 @ VD=1.8V, Id=1µA, L=0.28µm, W=210µm	8	-	-	V
VTFNP1PW2	n-channel threshold voltage poly 1 on field over PWELL2, @ VD=5V, Id=1µA, L=0.28µm, W=210µm	8	-	-	V

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3. Parameters → 3.1 LP5MOS main module→ 3.1.1 Device independent p...→ Parasitic field para...

Name	Description	Low	Typ	High	Unit
VTFPM1NW1	p-channel threshold voltage metal 1 on field over NWELL1, @ VD=-1.8V, Id=-1µA, L=0.28µm, W=210µm	-	-	-40	V
VTFPM1NW2	p-channel threshold voltage metal 1 on field over NWELL2 @ VD=-5V, Id=-1µA, L=0.28µm, W=210µm	-	-	-40	V
VTFPP1NW1	p-channel threshold voltage poly 1 on field over NWELL1 @ VD=-1.8V, Id=-1µA, L=0.28µm, W=210µm	-	-	-8	V
VTFPP1NW2	p-channel threshold voltage poly 1 on field over NWELL2 @ VD=-5V, Id=-1µA, L=0.28µm, W=210µm	-	-	-8	V

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RCTNDM	metal 1 - N+ contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RCTNMP1	metal 1 - N+ poly 1 contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RCTPDM	metal 1 - P+ contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RCTPMP1	metal 1 - P+ poly 1 contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RSENP1ASB	N+ poly 1 silicide block edge resistance per terminal (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	65	-	-	Ωµm
RSENP1SB	N+ poly 1 silicide block edge resistance per terminal (2 terminals)	-	-	65	-	-	Ωµm
RSENP1_3SB	N+ poly 1 silicide block edge resistance per terminal (underlying NWELL/PWELL2, 3 terminals)	-	-	65	-	-	Ωµm
RSEPP1PWSB	P+ poly 1 silicide block edge resistance per terminal (underlying PWELL, 3 terminals)	-	-	70	-	-	Ωµm
RSEPP1SB	P+ poly 1 silicide block edge resistance per terminal (2 terminals)	-	-	70	-	-	Ωµm
RSRNNS	NDIFF (salicided) sheet resistance	-	-	6.4	7.9	9.4	Ω/□
RSRNP1	N+ poly 1 sheet resistance (2 terminals)	-	225	315	405	-	Ω/□
RSRNP1A	N+ poly 1 sheet resistance (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	200	245	290	335	380	Ω/□
RSRNP1S	N+ poly 1 (salicided) sheet resistance	-	-	7.5	-	-	Ω/□
RSRNP1_3	N+ poly 1 sheet resistance (underlying NWELL/PWELL2, 3 terminals)	220	280	340	400	460	Ω/□
RSRNW1	NWELL1 sheet resistance (STI terminated)	840	930	1020	1110	1200	Ω/□
RSRNW2	NWELL2 sheet resistance (STI terminated)	840	1020	1200	1380	1560	Ω/□
RSRPP1	P+ poly 1 sheet resistance (2 terminals)	-	230	275	320	-	Ω/□
RSRPP1NW	P+ poly 1 sheet resistance (underlying NWELL, 3 terminals)	210	240	270	300	330	Ω/□
RSRPP1PW	P+ poly 1 sheet resistance (underlying PWELL, 3 terminals)	225	255	285	315	345	Ω/□

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3. Parameters → 3.1 LP5MOS main module→ 3.1.1 Device independent p...→ Sheet and contact re...

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRPP1S	P+ poly 1 sheet resistance (salicided)	5.2	6.3	7.5	8.7	9.8	Ω/□
RSRPPS	PDIFF (salicided) sheet resistance	-	-	7.1	8.6	10.1	Ω/□
RSR_M1	metal 1 sheet resistance	61	69	77	85	93	mΩ/□
RSR_M2	metal 2 sheet resistance	58	66	74	82	90	mΩ/□
RSSPTUB	PTUB_SUB sheet resistance	-	-	3500	-	-	Ω/□
RVI_V1	VIA1 resistance	-	3	4.5	6.75	9	Ω/via
TC1NP1	N+ poly 1 temperature coefficient 1 (2 terminals)	-	-1.73	-1.47	-1.22	-	1e-03/K
TC1NP1A	N+ poly 1 temperature coefficient 1 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-1.53	-1.4	-1.27	-	1e-03/K
TC1NP1ARSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	-1.4	-	-	1e-03/K
TC1NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (2 terminals)	-	-	-1.4	-	-	1e-03/K
TC1NP1_3	N+ poly 1 temperature coefficient 1 (underlying NWELL/PWELL2, 3 terminals)	-	-1.71	-1.54	-1.37	-	1e-03/K
TC1NP1_3RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying NWELL/PWELL2, 3 terminals)	-	-	-1.4	-	-	1e-03/K
TC1PP1	P+ poly 1 temperature coefficient 1 (2 terminals)	-	-0.17	-0.08	0.01	-	1e-03/K
TC1PP1PW	P+ poly 1 temperature coefficient 1 (underlying PWELL, 3 terminals)	-	-0.16	-0.1	-0.04	-	1e-03/K
TC1PP1PWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying PWELL, 3 terminals)	-	-	-1.2	-	-	1e-03/K
TC1PP1RSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (2 terminals)	-	-	-1.2	-	-	1e-03/K
TC1PP1S	P+ poly 1 temperature coefficient 1	-	2.74	3.1	3.46	-	1e-03/K
TC1_CT	contact resistance temperature coefficient 1	-	-	2.15	-	-	1e-03/K
TC1_V1	VIA1 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2NP1	N+ poly 1 temperature coefficient 2 (2 terminals)	-	1.85	2.75	3.65	-	1e-06/K ²
TC2NP1A	N+ poly 1 temperature coefficient 2 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	2.05	2.5	2.95	-	1e-06/K ²
TC2NP1ARSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	0.3	-	-	1e-06/K ²
TC2NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (2 terminals)	-	-	0.3	-	-	1e-06/K ²



3. Parameters → 3.1 LP5MOS main module → 3.1.1 Device independent p... → Sheet and contact re...

Name	Description	LSL	Low	Typ	High	USL	Unit
TC2NP1_3	N+ poly 1 temperature coefficient 2 (underlying NWELL/PWELL2, 3 terminals)	-	2.4	3	3.6	-	1e-06/K ²
TC2NP1_3RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying NWELL/PWELL2, 3 terminals)	-	-	0.3	-	-	1e-06/K ²
TC2PP1	P+ poly 1 temperature coefficient 2 (2 terminals)	-	0.3	0.75	1.2	-	1e-06/K ²
TC2PP1PW	P+ poly 1 temperature coefficient 2 (underlying PWELL, 3 terminals)	-	0.55	0.85	1.15	-	1e-06/K ²
TC2PP1PWRSE	P + poly 1 silicide block edge resistance temperature coefficient 2 (underlying PWELL, 3 terminals)	-	-	0.2	-	-	1e-06/K ²
TC2PP1RSE	P + poly 1 silicide block edge resistance temperature coefficient 2 (2 terminals)	-	-	0.2	-	-	1e-06/K ²
TC2PP1S	P+ poly 1 temperature coefficient 2	-	-1.12	0.08	1.28	-	1e-06/K ²
TC2_CT	contact resistance temperature coefficient 2	-	-	0	-	-	1e-06/K ²
TC2_V1	VIA1 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WERNNS	NDIFF (salicided) effective width @ W=0.42µm	-	0.42	0.48	0.54	-	µm
WERPPS	PDIFF (salicided) effective width @ W=0.42µm	-	0.4	0.46	0.52	-	µm

Note: The values of the sheet resistances (except for the metals) depend on the used operating conditions. For detailed information, refer to the simulation models.

Gate oxide parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDON	1.8V NMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm ²	4.5	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BDON5	5.0V NMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm ²	11	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BDOP	1.8V PMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm ²	4.1	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BDOP5	5.0V PMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm ²	11	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CGAN	1.8V NMOS gate oxide area capacitance @ Vbias=1.8V	-	8.06	8.46	8.91	-	fF/µm ²
CGAN5	5.0V NMOS gate oxide area capacitance @ Vbias=5.5V	-	2.62	2.71	2.83	-	fF/µm ²
CGAP	1.8V PMOS gate oxide area capacitance @ Vbias=-1.8V	8.05	8.46	8.91	9.4	9.95	fF/µm ²
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

3. Parameters → 3.1 LP5MOS main module → 3.1.1 Device independent p... → Gate oxide parameter...

Name	Description	LSL	Low	Typ	High	USL	Unit
CGAP5	5.0V PMOS gate oxide area capacitance @ Vbias=-5.5V	2.5	2.62	2.71	2.83	2.94	fF/ μm^2
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGON	1.8V NMOS gate – source/drain overlap	-	-	0.33	-	-	fF/ μm
CGON5	5.0V NMOS gate – source/drain overlap	-	-	0.11	-	-	fF/ μm
CGOP	1.8V PMOS gate – source/drain overlap	-	-	0.32	-	-	fF/ μm
CGOP5	5.0V PMOS gate – source/drain overlap	-	-	0.13	-	-	fF/ μm

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances.

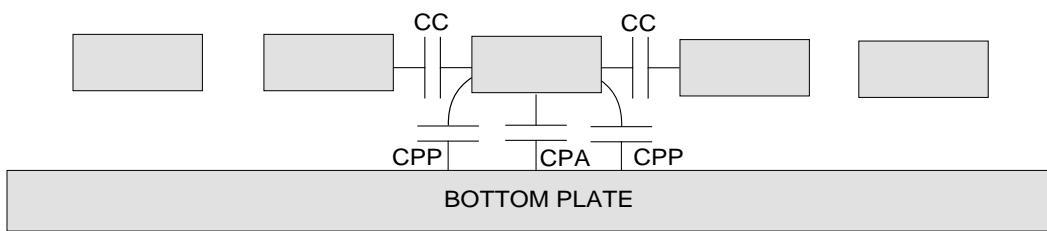


Figure 3.2 Parasitic capacitance structure

Name	Description	Typ	Unit
CC_M1M1	coupling capacitance metal 1 – metal 1	113	aF/ μm
CC_M2M2	coupling capacitance metal 2 – metal 2	97	aF/ μm
CC_P1P1	coupling capacitance poly 1 – poly 1	56	aF/ μm
CPAM1DIFF	metal 1 – active area capacitance	35.9	aF/ μm^2
CPAM1P1	metal 1 – poly 1 area capacitance	45.4	aF/ μm^2
CPAM1STI	metal 1 – field area (STI) area capacitance	25.6	aF/ μm^2
CPAM2DIFF	metal 2 – active area capacitance	14.6	aF/ μm^2
CPAM2M1	metal 2 – metal 1 area capacitance	41.5	aF/ μm^2
CPAM2P1	metal 2 – poly 1 area capacitance	16	aF/ μm^2
CPAM2STI	metal 2 – field area (STI) area capacitance	12.5	aF/ μm^2
CPASTI	poly 1 – field area (STI) area capacitance	88.5	aF/ μm^2
CPATUB	tub-handle wafer area capacitance	0.0345	fF/ μm^2
CPPM1DIFF	metal 1 – active perimeter capacitance	10.3	aF/ μm
CPPM1P1	metal 1 – poly 1 perimeter capacitance	7.8	aF/ μm
CPPM1STI	metal 1 – field area (STI) perimeter capacitance	9.2	aF/ μm
CPPM2DIFF	metal 2 – active perimeter capacitance	7.9	aF/ μm
CPPM2M1	metal 2 – metal 1 perimeter capacitance	8.3	aF/ μm
CPPM2P1	metal 2 – poly 1 perimeter capacitance	5	aF/ μm
CPPM2STI	metal 2 – field area (STI) perimeter capacitance	7.6	aF/ μm
CPPSTI	poly 1 – field area (STI) perimeter capacitance	15.1	aF/ μm

3. Parameters → 3.1 LP5MOS main module → 3.1.1 Device independent p... → Physical layer opera...

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_CT_DC ⁽¹⁾	Contact	-40°C to 175°C	-	-	0.53	-	mA/cnt
JMax_DC ⁽²⁾⁽¹⁾	Poly 1	-40°C to 175°C	-	-	1	-	mA/µm
JMax_DC ⁽³⁾⁽¹⁾	Metal 1	-40°C to 175°C	-	-	1	20	mA/µm
JMax_DC ⁽³⁾⁽¹⁾	Metal 2	-40°C to 175°C	-	-	1	20	mA/µm
JMax_N_DC ⁽⁴⁾⁽¹⁾	Metal 1	-40°C to 175°C	-	-	0.5	20	mA/µm
JMax_N_DC ⁽⁴⁾⁽¹⁾	Metal 2	-40°C to 175°C	-	-	0.5	20	mA/µm
JMax_VI_DC ⁽¹⁾	Via 1	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_CT_AC ⁽⁵⁾	Contact	-40°C to 175°C	-	-	2.4	-	mA/cnt
JMax_AC ⁽³⁾⁽⁵⁾	Metal 1	-40°C to 175°C	-	-	4.5	20	mA/µm
JMax_AC ⁽³⁾⁽⁵⁾	Metal 2	-40°C to 175°C	-	-	4.5	20	mA/µm
JMax_N_AC ⁽⁴⁾⁽⁵⁾	Metal 1	-40°C to 175°C	-	-	2.2	20	mA/µm
JMax_N_AC ⁽⁴⁾⁽⁵⁾	Metal 2	-40°C to 175°C	-	-	2.2	20	mA/µm
JMax_VI_AC ⁽⁵⁾	Via 1	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4 ⁽⁶⁾⁽⁷⁾	Contact	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁷⁾	Metal 1	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁷⁾	Metal 2	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁷⁾	Via 1	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁶⁾	Contact	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁶⁾	Metal 1	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁶⁾	Metal 2	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁶⁾	Via 1	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁹⁾⁽⁶⁾	Contact	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e4 ⁽⁹⁾⁽⁶⁾	Metal 1	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4 ⁽⁹⁾⁽⁶⁾	Metal 2	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4 ⁽⁹⁾⁽⁶⁾	Via 1	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁷⁾	Contact	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁷⁾	Metal 1	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁷⁾	Metal 2	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁷⁾	Via 1	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁶⁾	Contact	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁶⁾	Metal 1	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁶⁾	Metal 2	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁶⁾	Via 1	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁹⁾⁽⁶⁾	Contact	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁹⁾⁽⁶⁾	Metal 1	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁹⁾⁽⁶⁾	Metal 2	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁹⁾⁽⁶⁾	Via 1	125°C to 175°C	-	0.1	-	-	-
E ⁽¹⁰⁾	Poly 1	-40°C to 175°C	-	-	150	-	V/µm

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3. Parameters → 3.1 LP5MOS main module → 3.1.1 Device independent p... → Physical layer opera...

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
E ⁽¹¹⁾	Metal 1	-40°C to 175°C	-	-	250	-	V/µm
E ⁽¹²⁾	Metal 2	-40°C to 175°C	-	-	250	-	V/µm

Note 1 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 2 The specified values are valid for salicidized polysilicon interconnects and salicidized polysilicon resistors.

Note 3 track width > 0.44µm.

Note 4 track width ≤ 0.44µm.

Note 5 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 6 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 7 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 9 The temperature correction factor is interpolated between given values for temperatures above 125°C

Note 10 lateral electric field between Poly 1 track

Note 11 lateral electric field between Metal 1 track

Note 12 lateral electric field between Metal 2 track

3.1.2 Device parameters

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Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PWELL1.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNES	drain-source breakdown @ VG=0V, Id=1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNE	mobility exponent	-	-	-1.7	-	-	-
FC_NE	corner frequency @ VD=1.8V, Id=1µA	-	-	2.1	-	-	kHz
GA_NE	body factor long channel @ L=10µm, W=10µm	-	-	0.7	-	-	√V
IDSNES	saturation current @ VG=1.8V, VD=1.8V, L=0.18µm, W=10µm	355	423	490	558	625	µA/µm
IOFNES	off-state leakage @ VD=1.8V, L=0.18µm, W=10µm	-	-	-	6	-	pA/µm
ISBNES	bulk current @ VD=1.8V, L=0.18µm	-	-	0.09	-	-	µA/µm



3. Parameters → 3.1 LP5MOS main module→ 3.1.2 Device parameters→ ne→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
KP_NE	gain factor long channel @ L=10µm, W=10µm	-	-	243	-	-	µA/V ²
LEFNE	effective channel length @ L=0.18µm	-	-	0.16	-	-	µm
NOINE	input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	15.6	-	-	µVµm/√(Hz)
STSNE	subthreshold slope @ VD=1.8V	-	-	11.5	-	-	decade/V
TC_VTXNE	threshold voltage temperature coefficient @ L=10µm, L=10µm, W=10µm, W=10µm	-	-	-0.89	-	-	mV/K
U0_NE	effective mobility	-	-	294	-	-	cm ² /(Vs)
VTINEL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.53	0.555	0.58	0.605	0.63	V
VTINES	threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	0.46	0.52	0.58	0.64	0.7	V
VTINESS	threshold voltage small channel @ VD=0.1V, L=0.18µm, W=0.22µm	-	-	0.47	-	-	V
VTXNES	extrapolated threshold voltage short channel @ VD=0.1V, L=0.18µm, W=10µm	-	-	0.68	-	-	V
WEFNE	effective channel width @ W=0.22µm	-	-	0.19	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE	pelgrom coefficient gain factor mismatch	0.81	%µm
AIDNE00	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0V	8.53	%µm
AIDNE01	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.1V	5.89	%µm
AIDNE02	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.2V	4.2	%µm
AIDNE04	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.4V	2.43	%µm
AIDNE06	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.6V	1.65	%µm
AIDNE08	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.8V	1.24	%µm
AIDNE10	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1V	1.01	%µm
AIDNE14	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1.4V	0.76	%µm
AVTNE	pelgrom coefficient threshold voltage mismatch	6.56	mVµm
DLTNE	transistor delta length	0.02	µm
DWTNE	transistor delta width	0.03	µm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → ne → Matching parameters

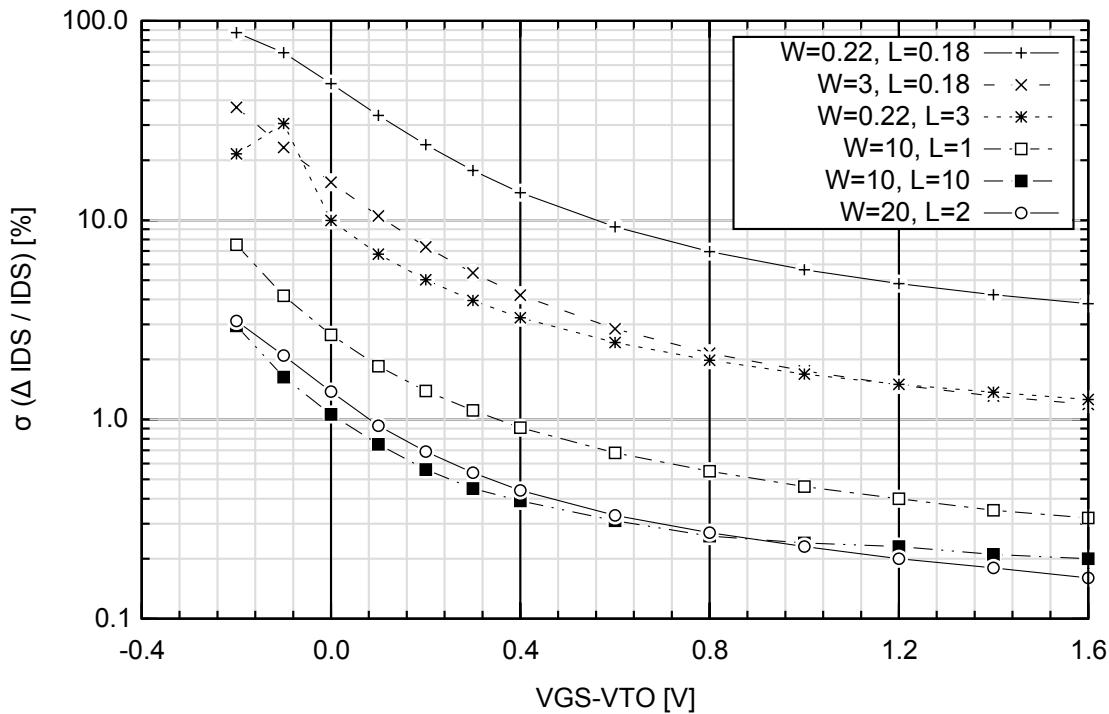


Figure 3.3 Device ne: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nn

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PTUB_SUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
FC_NN	corner frequency @ VD=1.8V, Id=1µA	-	-	0.58	-	-	kHz
IDSNNSS	saturation current @ VG=1.8V, VD=1.8V, L=1µm, W=10µm	240	280	320	360	400	µA/µm
IDSNNSS2	saturation current @ VG=1.8V, VD=1.8V, L=2µm, W=10µm	-	-	206	-	-	µA/µm
IOF2NNSS2	off-state leakage @ VG=-0.5V, VD=1.8V, L=1µm, W=10µm	-	-	-	25	-	nA/µm
IOFNNS2	off-state leakage @ VG=-0.5V, VD=1.8V, L=2µm, W=10µm	-	-	1	-	-	pA/µm
KP_NN	gain factor @ L=10µm, W=10µm	-	-	345	-	-	µA/V ²

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3. Parameters → 3.1 LP5MOS main module→ 3.1.2 Device parameters→ nn→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
LEFNN	effective channel length @ L=1μm	-	-	1.25	-	-	μm
NOINN	input referred noise @ VD=1.8V, Id=1μA, f=1Hz, L=10μm, W=10μm	-	-	4.8	-	-	μVμm/√(Hz)
VTXNNL	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=10μm	-0.18	-0.15	-0.12	-0.09	-0.06	V
VTXNNS	extrapolated threshold voltage short channel @ VD=0.1V, L=1μm, W=10μm	-0.23	-0.2	-0.17	-0.14	-0.11	V
VTXNNS2	extrapolated threshold voltage short channel @ VD=0.1V, L=2μm, W=10μm	-	-	-0.14	-	-	V
WEFNN	effective channel width @ W=1μm	-	-	0.95	-	-	μm

Note: It is strongly recommended to use a channel length of $\geq 2\mu\text{m}$ when the nn and nn5 is operated in the sub-threshold region.

Matching parameters

Name	Description	Typ	Unit
ABTNN	pelgrom coefficient gain factor mismatch	1	%μm
AIDNN00	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0V	6.91	%μm
AIDNN01	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.1V	3.33	%μm
AIDNN02	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.2V	1.92	%μm
AIDNN04	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.4V	1.19	%μm
AIDNN06	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.6V	1.03	%μm
AIDNN08	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.8V	0.98	%μm
AIDNN10	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1V	0.96	%μm
AIDNN14	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1.4V	0.94	%μm
AVTNN	pelgrom coefficient threshold voltage mismatch	1.95	mVμm
DLTNN	transistor delta length	-0.25	μm
DWTNN	transistor delta width	0.05	μm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → nn → Matching parameters

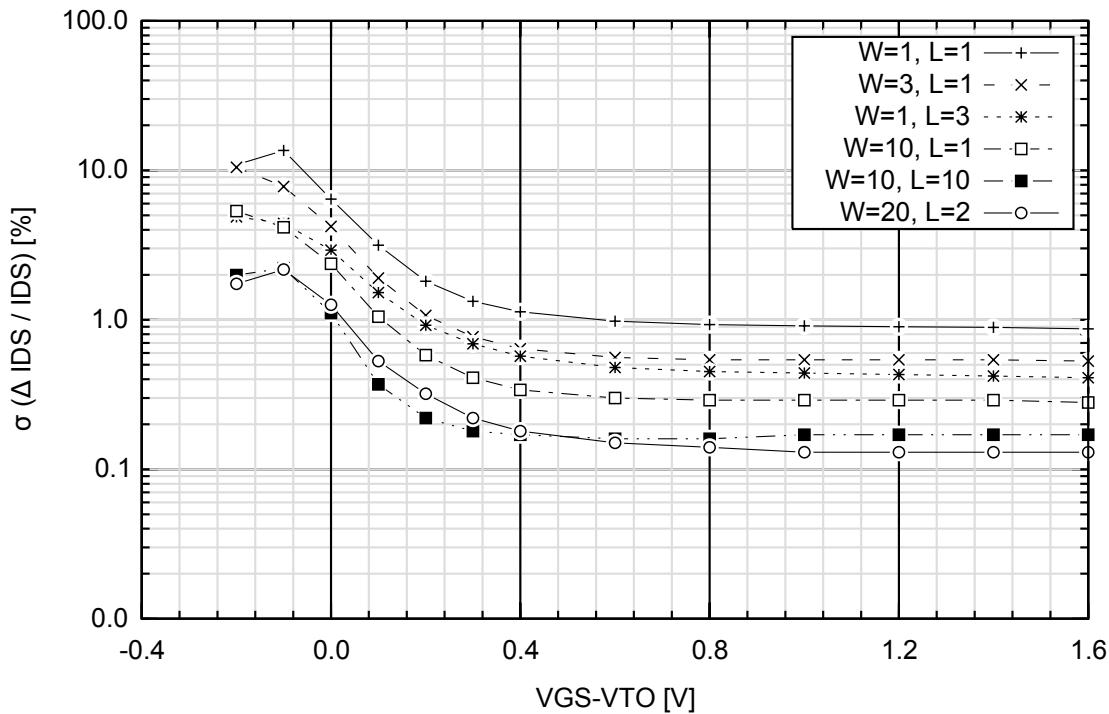


Figure 3.4 Device nn: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe, pe_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBptub	-40°C to 175°C	-0.5	0	1.98	2.3	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL1.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPEs	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEXPE	mobility exponent	-	-	-1	-	-	-
FC_PE	corner frequency @ VD=-1.8V, Id=-1µA	-	-	0.43	-	-	kHz
GA_PE	body factor long channel @ L=10µm, W=10µm	-	-	0.9	-	-	√V
IDSPEs	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	130	160	190	220	250	µA/µm

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3. Parameters → 3.1 LP5MOS main module→ 3.1.2 Device parameters→ pe, pe_5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPES	off-state leakage @ VD=-1.8V, L=0.18μm, W=10μm	-	-	-	1.5	-	pA/μm
ISBPES	bulk current @ VD=-1.8V, L=0.18μm	-	-	0.2	-	-	nA/μm
KP_PE	gain factor long channel @ L=10μm, W=10μm	-	-	53.5	-	-	μA/V ²
LEFPE	effective channel length @ L=0.18μm	-	-	0.12	-	-	μm
NOIPE	input referred noise @ VD=-1.8V, Id=-1μA, f=1Hz, L=10μm, W=10μm	-	-	13.3	-	-	μVμm/√(Hz)
STSPE	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPE	threshold voltage temperature coefficient @ L=10μm, L=10μm, W=10μm, W=10μm	-	-	0.91	-	-	mV/K
U0_PE	effective mobility	-	-	65	-	-	cm ² /(Vs)
VTIPEL	threshold voltage long channel @ VD=-0.1V, L=10μm, W=10μm	-0.76	-0.72	-0.68	-0.64	-0.6	V
VTIPES	threshold voltage short channel @ VD=-0.1V, L=0.18μm, W=10μm	-0.74	-0.69	-0.64	-0.59	-0.54	V
VTIPESS	threshold voltage small channel @ VD=-0.1V, L=0.18μm, W=0.22μm	-	-	-0.6	-	-	V
VTXPES	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18μm, W=10μm	-	-	-0.65	-	-	V
WEFPE	effective channel width @ W=0.22μm	-	-	0.25	-	-	μm

Matching parameters

Name	Description	Typ	Unit
ABTPE	pelgrom coefficient gain factor mismatch	0.93	%μm
AIDPE00	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0V	7.9	%μm
AIDPE01	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.1V	5.49	%μm
AIDPE02	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.2V	3.83	%μm
AIDPE04	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.4V	2.3	%μm
AIDPE06	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.6V	1.55	%μm
AIDPE08	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.8V	1.22	%μm
AIDPE10	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1V	1	%μm
AIDPE14	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1.4V	0.78	%μm
AVTPE	pelgrom coefficient threshold voltage mismatch	5.04	mVμm
DLTPE	transistor delta length	0.06	μm
DWTPE	transistor delta width	-0.03	μm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → pe, pe_5 → Matching parameters

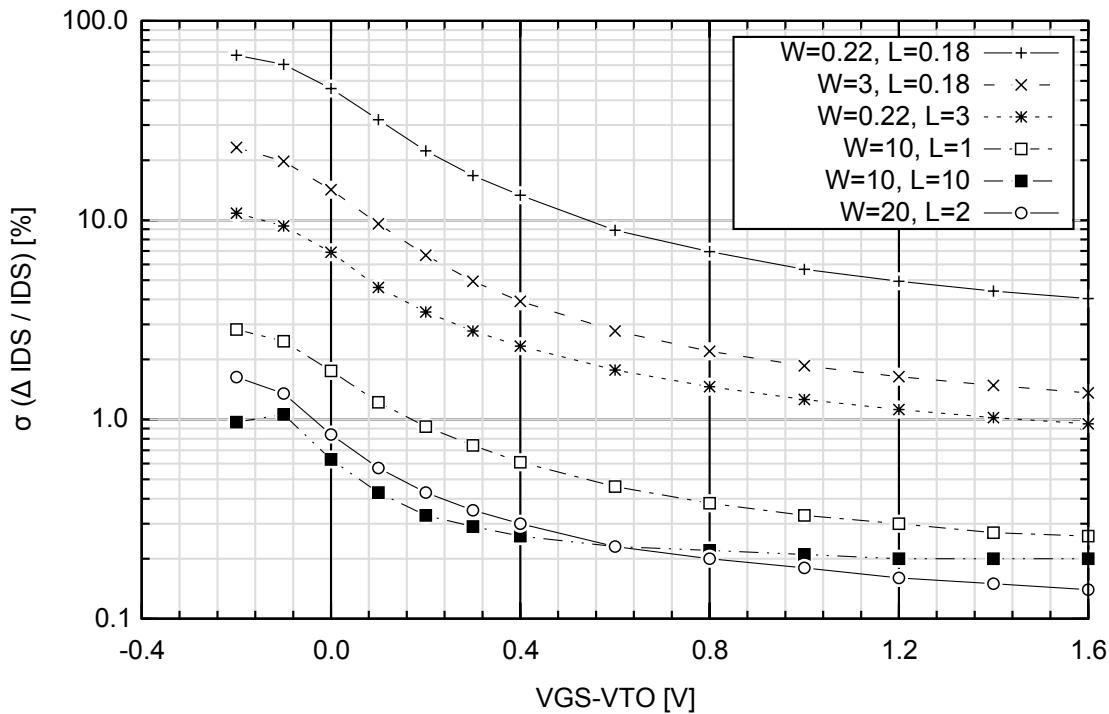


Figure 3.5 Device pe: drain current matching vs. VGS-VTO (typical values, drawn W and L)

ne5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	5.5	7	V
VDS	-40°C to 175°C	-7	-5.5	5.5	7	V
VDB	-40°C to 175°C	-0.5	0	5.5	7	V
VSB	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE5S	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEXNE5	mobility exponent	-	-	-1.7	-	-	-
FC_NE5	corner frequency @ VD=5V, Id=1µA	-	-	5.44	-	-	kHz
GA_NE5	body factor long channel @ L=10µm, W=10µm	-	-	0.9	-	-	√V
IDSNE5S	saturation current @ VG=5V, VD=5V, L=0.5µm, W=10µm	470	498	525	552	580	µA/µm
IOFNE5S	off-state leakage @ VD=5V, L=0.5µm, W=10µm	-	-	-	0.5	-	pA/µm

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3. Parameters → 3.1 LP5MOS main module→ 3.1.2 Device parameters→ ne5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ISBNE5S	bulk current @ VD=5V, L=0.5μm	-	-	5.8	-	-	μA/μm
KP_NE5	gain factor @ L=10μm, W=10μm	-	-	111	-	-	μA/V ²
LEFNE5	effective channel length @ L=0.5μm	-	-	0.45	-	-	μm
NOINE5	input referred noise @ VD=5V, Id=1μA, f=1Hz, L=10μm, W=10μm	-	-	32.1	-	-	μVμm/√(Hz)
STSNE5	subthreshold slope @ VD=5V	-	-	10	-	-	decade/V
TC_VTXNE5	threshold voltage temperature coefficient @ L=10μm, W=10μm	-	-	-1.4	-	-	mV/K
U0_NE5	effective mobility	-	-	400	-	-	cm ² /(Vs)
VTINE5L	threshold voltage long channel @ VD=0.1V, L=10μm, W=10μm	0.62	0.66	0.7	0.74	0.78	V
VTINE5S	threshold voltage short channel @ VD=0.1V, L=0.5μm, W=10μm	0.61	0.685	0.76	0.835	0.91	V
VTXNE5S	extrapolated threshold voltage short channel @ VD=0.1V, L=0.5μm, W=10μm	-	-	0.82	-	-	V
WEFNE5	effective channel width @ W=0.22μm	-	-	0.19	-	-	μm

Matching parameters

Name	Description	Typ	Unit
ABTNE5	pelgrom coefficient gain factor mismatch	1.72	%μm
AIDNE500	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	15.6	%μm
AIDNE502	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	7.91	%μm
AIDNE504	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	4.71	%μm
AIDNE506	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	3.21	%μm
AIDNE510	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	1.88	%μm
AIDNE520	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.91	%μm
AIDNE530	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.63	%μm
AIDNE550	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.43	%μm
AVTNE5	pelgrom coefficient threshold voltage mismatch	13.8	mVμm
DLTNE5	transistor delta length	0.05	μm
DWTNE5	transistor delta width	0.03	μm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → ne5 → Matching parameters

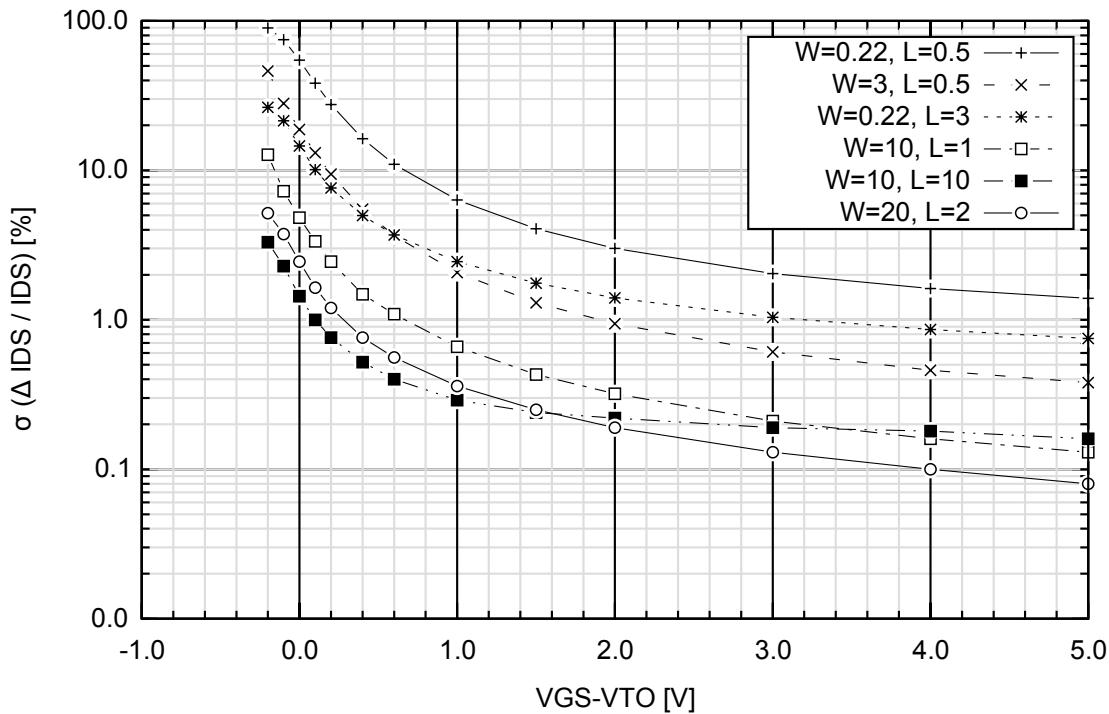


Figure 3.6 Device ne5: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	5.5	7	V
VDS	-40°C to 175°C	-7	-5.5	5.5	7	V
VDB	-40°C to 175°C	-0.5	0	5.5	7	V
VSB	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PTUB_SUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
FC_NN5	corner frequency @ VD=5V, Id=1µA	-	-	1.58	-	-	kHz
IDSNN5S	saturation current @ VG=5V, VD=5V, L=1µm, W=10µm	478	514	550	585	622	µA/µm
IDSNN5S2	saturation current @ VG=5V, VD=5V, L=2µm, W=10µm	-	-	388	-	-	µA/µm
IOF2NN5S2	off-state leakage @ VG=-0.5V, VD=5V, L=1µm, W=10µm	-	-	-	300	-	nA/µm
IOFNN5S2	off-state leakage @ VG=-0.5V, VD=5V, L=2µm, W=10µm	-	-	3	-	-	pA/µm
KP_NN5	gain factor @ L=10µm, W=10µm	-	-	150	-	-	µA/V ²
LEFNN5	effective channel length @ L=1µm	-	-	1.13	-	-	µm

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3. Parameters → 3.1 LP5MOS main module→ 3.1.2 Device parameters→ nn5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
NOINN5	input referred noise @ VD=5V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	11.6	-	-	µVµm/√(Hz)
VTXNN5L	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	-0.185	-0.145	-0.105	-0.065	-0.025	V
VTXNN5S	extrapolated threshold voltage short channel @ VD=0.1V, L=1µm, W=10µm	-0.24	-0.2	-0.16	-0.12	-0.08	V
VTXNN5S2	extrapolated threshold voltage short channel @ VD=0.1V, L=2µm, W=10µm	-	-	-0.13	-	-	V
WEFNN5	effective channel width @ W=1µm	-	-	1	-	-	µm

Note: It is strongly recommended to use a channel length of $\geq 2\mu\text{m}$ when the nn and nn5 is operated in the sub-threshold region.

Matching parameters

Name	Description	Typ	Unit
ABTNN5	pelgrom coefficient gain factor mismatch	0.83	%µm
AIDNN500	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	8.95	%µm
AIDNN502	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	2.99	%µm
AIDNN504	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	1.63	%µm
AIDNN506	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	1.15	%µm
AIDNN510	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	0.8	%µm
AIDNN520	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.58	%µm
AIDNN530	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.51	%µm
AIDNN550	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.45	%µm
AVTNN5	pelgrom coefficient threshold voltage mismatch	3.43	mVµm
DLTNN5	transistor delta length	-0.13	µm
DWTNN5	transistor delta width	0	µm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → nn5 → Matching parameters

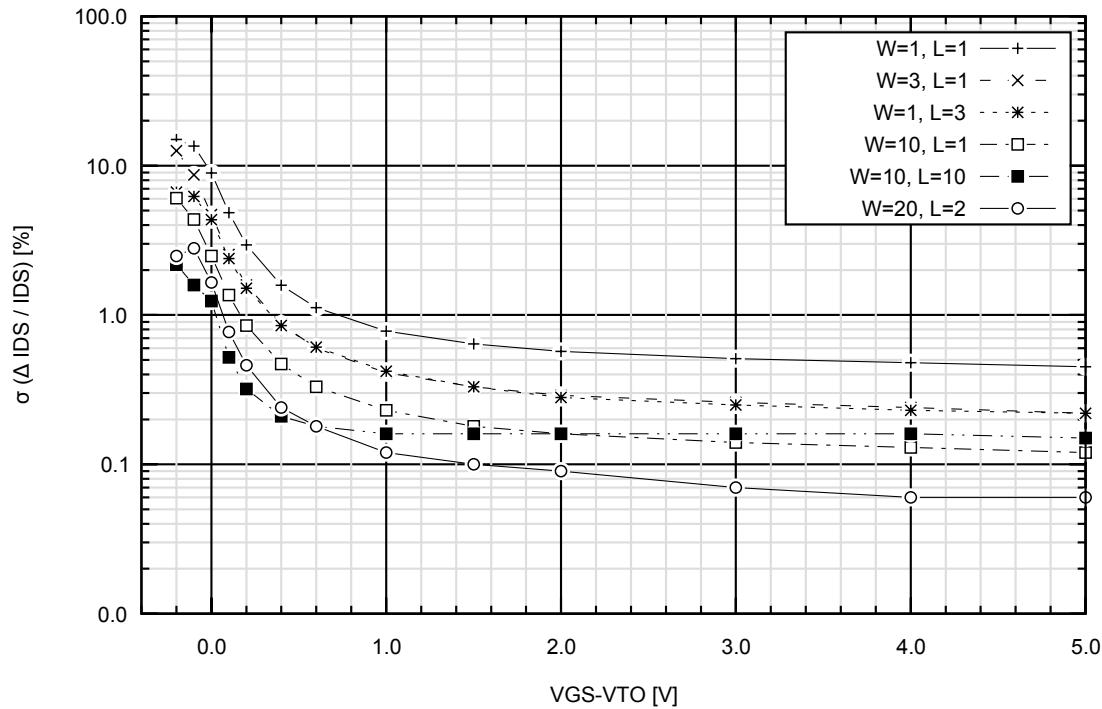


Figure 3.7 Device nn5: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe5, pe5_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	5.5	7	V
VDS	-40°C to 175°C	-7	-5.5	5.5	7	V
VDB	-40°C to 175°C	-7	-5.5	0	0.5	V
VSB	-40°C to 175°C	-7	-5.5	0	0.5	V
VBptub	-40°C to 175°C	-0.5	0	5.5	7	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE5S	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	7.5	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEXPE5	mobility exponent	-	-	-1.2	-	-	-
FC_PE5	corner frequency @ VD=-5V, Id=-1µA	-	-	0.43	-	-	kHz
GA_PE5	body factor long channel @ L=10µm, W=10µm	-	-	1.1	-	-	√V
IDSPE5S	saturation current @ VG=-5V, VD=-5V, L=0.5µm, W=10µm	225	245	265	285	305	µA/µm

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3. Parameters → 3.1 LP5MOS main module→ 3.1.2 Device parameters→ pe5, pe5_5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPE5S	off-state leakage @ VD=-5V, L=0.5μm, W=10μm	-	-	-	1	-	pA/μm
KP_PE5	gain factor @ L=10μm, W=10μm	-	-	28	-	-	μA/V ²
LEFPE5	effective channel length @ L=0.5μm	-	-	0.36	-	-	μm
NOIPE5	input referred noise @ VD=-5V, Id=-1μA, f=1Hz, L=10μm, W=10μm	-	-	20.2	-	-	μVμm/√(Hz)
STSPE5	subthreshold slope @ VD=-5V	-	-	10	-	-	decade/V
TC_VTXPE5	threshold voltage temperature coefficient @ L=10μm, W=10μm	-	-	1.1	-	-	mV/K
U0_PE5	effective mobility	-	-	102	-	-	cm ² /(Vs)
VTIPE5L	threshold voltage long channel @ VD=-0.1V, L=10μm, W=10μm	-0.94	-0.9	-0.86	-0.82	-0.78	V
VTIPE5S	threshold voltage short channel @ VD=-0.1V, L=0.5μm, W=10μm	-0.93	-0.885	-0.84	-0.795	-0.75	V
VTXPE5S	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5μm, W=10μm	-	-	-0.79	-	-	V
WEFPE5	effective channel width @ W=0.22μm	-	-	0.22	-	-	μm

Matching parameters

Name	Description	Typ	Unit
ABTPE5	pelgrom coefficient gain factor mismatch	0.78	%μm
AIDPE500	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	11.1	%μm
AIDPE502	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	5.03	%μm
AIDPE504	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	2.92	%μm
AIDPE506	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	2.02	%μm
AIDPE510	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	1.26	%μm
AIDPE520	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.7	%μm
AIDPE530	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.52	%μm
AIDPE550	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.39	%μm
AVTPE5	pelgrom coefficient threshold voltage mismatch	6.72	mVμm
DLTPE5	transistor delta length	0.14	μm
DWTPE5	transistor delta width	0	μm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → pe5, pe5_5 → Matching parameters

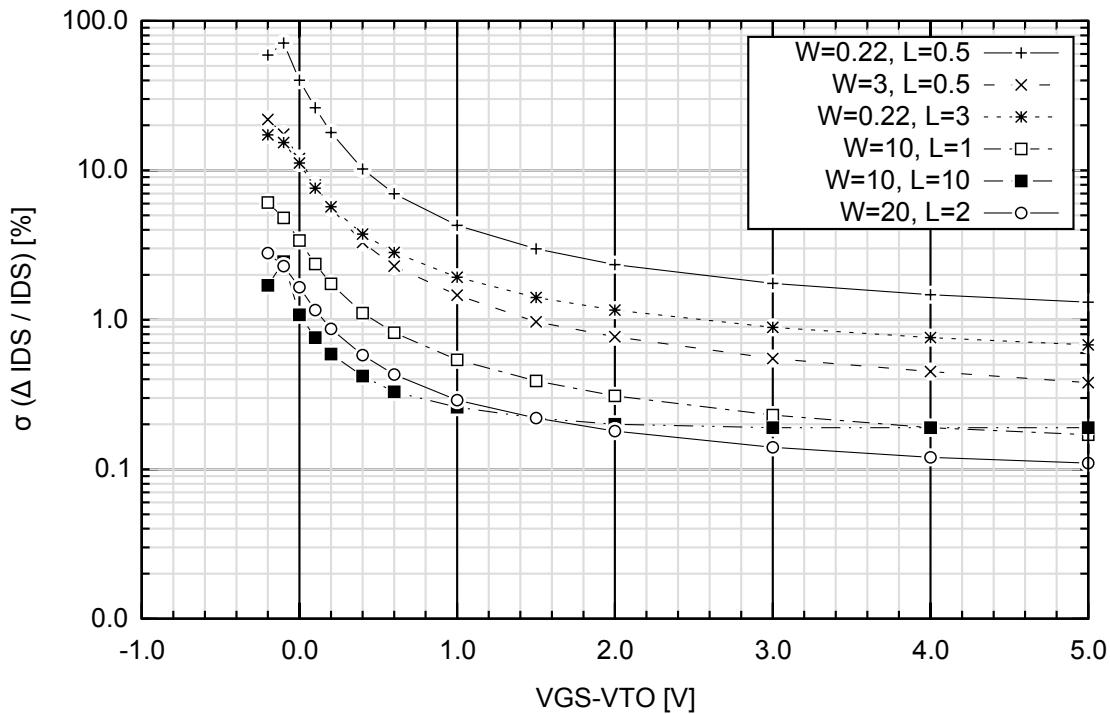


Figure 3.8 Device pe5: drain current matching vs. VGS-VTO (typical values, drawn W and L)

qpve

emitter area: $2 \times 2 \mu\text{m}^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	Low	Typ	High	Unit
EVFPE	early voltage forward @ $I_b = 1 \mu\text{A}$	100	-	-	V
HF_PE	forward current gain @ $I_e = 1 \mu\text{A}$	-	2.6	-	-
VBEPE	base-emitter voltage @ $I_e = 1 \mu\text{A}$	-	708	-	mV

Matching parameters

Name	Description	Typ	Unit
SIBPE1	standard deviation base current mismatch @ $I_c = 100 \text{nA}$	1.76	%
	Note: Preliminary		
SIBPE2	standard deviation base current mismatch @ $I_c = 10 \mu\text{A}$	1.76	%
	Note: Preliminary		
SICPE1	standard deviation collector current mismatch @ $I_c = 100 \text{nA}$	0.29	%
	Note: Preliminary		

⇒

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → qpve → Matching parameters

Name	Description	Typ	Unit
SICPE2	standard deviation collector current mismatch @ $I_c=10\mu A$ Note: Preliminary	0.24	%
SVBPE1	standard deviation base emitter voltage mismatch @ $I_e=100nA$ Note: Preliminary	0.24	mV
SVBPE2	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$ Note: Preliminary	0.2	mV

qpvf

emitter area: $5 \times 5 \mu m^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
EVFPF	early voltage forward @ $I_b=-1\mu A$	-	100	-	-	-	V
HF_PF	forward current gain @ $I_e=1\mu A$	-	-	2.7	-	-	-
VBEFP	base-emitter voltage @ $I_e=1\mu A$	659	664	669	674	679	mV

Matching parameters

Name	Description	Typ	Unit
SIBPF1	standard deviation base current mismatch @ $I_c=100nA$ Note: Preliminary	0.7	%
SIBPF2	standard deviation base current mismatch @ $I_c=10\mu A$ Note: Preliminary	0.65	%
SICPF1	standard deviation collector current mismatch @ $I_c=100nA$ Note: Preliminary	0.18	%
SICPF2	standard deviation collector current mismatch @ $I_c=10\mu A$ Note: Preliminary	0.16	%
SVBPF1	standard deviation base emitter voltage mismatch @ $I_e=100nA$ Note: Preliminary	0.22	mV
SVBPF2	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$ Note: Preliminary	0.18	mV

qpvg

emitter area: $10 \times 10 \mu m^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → qpvg → Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	Low	Typ	High	Unit
EVFPG	early voltage forward @ Ib=-1µA	100	-	-	V
HF_PG	forward current gain @ Ie=1µA	-	2.9	-	-
VBEPEG	base-emitter voltage @ Ie=1µA	-	636	-	mV

Matching parameters

Name	Description	Typ	Unit
SIBPG1	standard deviation base current mismatch @ Ic=100nA	0.37	%
	Note: Preliminary		
SIBPG2	standard deviation base current mismatch @ Ic=10µA	0.36	%
	Note: Preliminary		
SICPG1	standard deviation collector current mismatch @ Ic=100nA	0.12	%
	Note: Preliminary		
SICPG2	standard deviation collector current mismatch @ Ic=10µA	0.12	%
	Note: Preliminary		
SVBPG1	standard deviation base emitter voltage mismatch @ Ie=100nA	0.21	mV
	Note: Preliminary		
SVBPG2	standard deviation base emitter voltage mismatch @ Ie=10µA	0.16	mV
	Note: Preliminary		

qpve5

emitter area: 2x2µm²

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	Low	Typ	High	Unit
EVFPE5	early voltage forward @ Ib=-1µA	100	-	-	V
HF_PE5	forward current gain @ Ie=1µA	-	1.95	-	-
VBEPE5	base-emitter voltage @ Ie=1µA	-	709	-	mV

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → qpve5 → Matching parameters

Matching parameters

Name	Description	Typ	Unit
SIBPE51	standard deviation base current mismatch @ $I_c=100nA$	1.79	%
	Note: Preliminary		
SIBPE52	standard deviation base current mismatch @ $I_c=10\mu A$	1.65	%
	Note: Preliminary		
SICPE51	standard deviation collector current mismatch @ $I_c=100nA$	0.35	%
	Note: Preliminary		
SICPE52	standard deviation collector current mismatch @ $I_c=10\mu A$	0.35	%
	Note: Preliminary		
SVBPE51	standard deviation base emitter voltage mismatch @ $I_e=100nA$	0.3	mV
	Note: Preliminary		
SVBPE52	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$	0.23	mV
	Note: Preliminary		

qpvf5

emitter area: $5 \times 5 \mu m^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
EVFPF5	early voltage forward @ $I_b=-1\mu A$	-	100	-	-	-	V
HF_PF5	forward current gain @ $I_e=1\mu A$	-	-	2.15	-	-	-
VBEFP5	base-emitter voltage @ $I_e=1\mu A$	659	664	669	674	679	mV

Matching parameters

Name	Description	Typ	Unit
SIBPF51	standard deviation base current mismatch @ $I_c=100nA$	0.56	%
	Note: Preliminary		
SIBPF52	standard deviation base current mismatch @ $I_c=10\mu A$	0.55	%
	Note: Preliminary		
SICPF51	standard deviation collector current mismatch @ $I_c=100nA$	0.19	%
	Note: Preliminary		
SICPF52	standard deviation collector current mismatch @ $I_c=10\mu A$	0.21	%
	Note: Preliminary		
SVBPF51	standard deviation base emitter voltage mismatch @ $I_e=100nA$	0.27	mV
	Note: Preliminary		

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → qpvg5 → Matching parameters

Name	Description	Typ	Unit
SVBPF52	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$	0.16	mV
	Note: Preliminary		

qpvg5

emitter area: $10 \times 10 \mu m^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	Low	Typ	High	Unit
EVFPG5	early voltage forward @ $I_b=-1\mu A$	100	-	-	V
HF_PG5	forward current gain @ $I_e=1\mu A$	-	2.25	-	-
VBEPG5	base-emitter voltage @ $I_e=1\mu A$	-	636	-	mV

Matching parameters

Name	Description	Typ	Unit
SIBPG51	standard deviation base current mismatch @ $I_c=100nA$	0.34	%
	Note: Preliminary		
SIBPG52	standard deviation base current mismatch @ $I_c=10\mu A$	0.26	%
	Note: Preliminary		
SICPG51	standard deviation collector current mismatch @ $I_c=100nA$	0.12	%
	Note: Preliminary		
SICPG52	standard deviation collector current mismatch @ $I_c=10\mu A$	0.15	%
	Note: Preliminary		
SVBPG51	standard deviation base emitter voltage mismatch @ $I_e=100nA$	0.22	mV
	Note: Preliminary		
SVBPG52	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$	0.15	mV
	Note: Preliminary		

rdn

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	1.98	2.3	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rdn → Operating conditions

Note: The node B (BULK) is PWELL1

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENNNSB	NDIFF silicide block edge resistance per terminal	-	-	12	-	-	Ωμm
RSRNN	NDIFF sheet resistance	49	55	61	67	73	Ω/□
TC1NN	NDIFF temperature coefficient 1	-	1.28	1.4	1.52	-	1e-03/K
TC1NNRSE	NDIFF silicide block edge resistance temperature coefficient 1	-	-	0.27	-	-	1e-03/K
TC2NN	NDIFF temperature coefficient 2	-	0.14	0.5	0.86	-	1e-06/K ²
TC2NNRSE	NDIFF silicide block edge resistance temperature coefficient 2	-	-	-1	-	-	1e-06/K ²
WERNN	NDIFF effective width @ W=0.42μm	-	0.34	0.4	0.46	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_NN	pelgrom coefficient resistor mismatch	1.2	%μm
DWRNN	resistor delta width	0.02	μm

rdp

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VBptub	-40°C to 175°C	-0.5	0	5.5	7	V
Vterm-bulk	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is NWELL1

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPPSB	PDIFF silicide block edge resistance per terminal	-	-	35	-	-	Ωμm
RSRPP	PDIFF sheet resistance	92	110	127	144	162	Ω/□
TC1PP	PDIFF temperature coefficient 1	-	1.18	1.3	1.42	-	1e-03/K
TC1PPRSE	PDIFF silicide block edge resistance temperature coefficient 1	-	-	-0.25	-	-	1e-03/K
TC2PP	PDIFF temperature coefficient 2	-	0.11	0.5	0.89	-	1e-06/K ²
TC2PPRSE	PDIFF silicide block edge resistance temperature coefficient 2	-	-	-2	-	-	1e-06/K ²
WERPP	PDIFF effective width @ W=0.42μm	-	0.3	0.36	0.42	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_PP	pelgrom coefficient resistor mismatch	1.2	%μm
DWRPP	resistor delta width	0.06	μm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rnw → Operating conditions

rnw

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PTUB_SUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRNW1	NWELL1 sheet resistance (STI terminated)	840	930	1020	1110	1200	Ω/□
TC1NW1	NWELL1 temperature coefficient 1	-	2.7	3	3.3	-	1e-03/K
TC2NW1	NWELL1 temperature coefficient 2	-	7	8.8	10.6	-	1e-06/K ²
WERNW1	NWELL1 effective width @ W=2μm	-	1.6	1.75	1.9	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_NW1	pelgrom coefficient resistor mismatch	1	%μm
DWRNW1	resistor delta width	0.25	μm

rdn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENN5SB	NDIFF5 silicide block edge resistance per terminal	-	-	12	-	-	Ωμm
RSRNN5	NDIFF5 sheet resistance (non salicided)	53	59	65	71	77	Ω/□
TC1NN5	NDIFF5 (non salicided) temperature coefficient 1	-	1.28	1.4	1.52	-	1e-03/K
TC1NN5RSE	NDIFF5 silicide block edge resistance temperature coefficient 1	-	-	0.12	-	-	1e-03/K
TC2NN5	NDIFF5 (non salicided) temperature coefficient 2	-	0.14	0.5	0.86	-	1e-06/K ²
TC2NN5RSE	NDIFF5 silicide block edge resistance temperature coefficient 2	-	-	-0.3	-	-	1e-06/K ²
WERNN5	NDIFF5 effective width @ W=0.42μm	-	0.34	0.4	0.46	-	μm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rdn5 → Matching parameters

Matching parameters

Name	Description	Typ	Unit
AR_NN5	pelgrom coefficient resistor mismatch	1.2	%μm
DWRNN5	resistor delta width	0.02	μm

rdp5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VBptub	-40°C to 175°C	-0.5	0	5.5	7	V
Vterm-bulk	-40°C to 175°C	-7	-5.5	0	0.5	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPP5SB	PDIFF5 silicide block edge resistance per terminal	-	-	35	-	-	Ωμm
RSRPP5	PDIFF5 sheet resistance (non salicided)	97	115	132	149	167	Ω/□
TC1PP5	PDIFF5 (non salicided) temperature coefficient 1	-	1.18	1.3	1.42	-	1e-03/K
TC1PP5RSE	PDIFF5 silicide block edge resistance temperature coefficient 1	-	-	-0.28	-	-	1e-03/K
TC2PP5	PDIFF5 (non salicided) temperature coefficient 2	-	0.11	0.5	0.89	-	1e-06/K ²
TC2PP5RSE	PDIFF5 silicide block edge resistance temperature coefficient 2	-	-	-3	-	-	1e-06/K ²
WERPP5	PDIFF5 effective width @ W=0.42μm	-	0.25	0.31	0.37	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_PP5	pelgrom coefficient resistor mismatch	1.3	%μm
DWRPP5	resistor delta width	0.11	μm

rnw5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Note: The node B (BULK) is: PTUB_SUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRNW2	NWELL2 sheet resistance (STI terminated)	840	1020	1200	1380	1560	Ω/□

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rnw5 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC1NW2	NWELL2 temperature coefficient 1	-	2.7	3	3.3	-	1e-03/K
TC2NW2	NWELL2 temperature coefficient 2	-	7	8.8	10.6	-	1e-06/K ²
WERNW2	NWELL2 effective width @ W=2µm	-	1.51	1.66	1.81	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NW2	pelgrom coefficient resistor mismatch	1.7	%µm
DWRNW2	resistor delta width	0.34	µm

rnp1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65µW/µm².

Process parameters

Name	Description	Low	Typ	High	Unit
RSENP1SB	N+ poly 1 silicide block edge resistance per terminal (2 terminals)	-	65	-	Ωµm
RSRNP1	N+ poly 1 sheet resistance (2 terminals)	225	315	405	Ω/□
TC1NP1	N+ poly 1 temperature coefficient 1 (2 terminals)	-1.73	-1.47	-1.22	1e-03/K
TC1NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (2 terminals)	-	-1.4	-	1e-03/K
TC2NP1	N+ poly 1 temperature coefficient 2 (2 terminals)	1.85	2.75	3.65	1e-06/K ²
TC2NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (2 terminals)	-	0.3	-	1e-06/K ²
WERNP1	N+ poly 1 effective width (2 terminals) @ W=0.42µm	0.285	0.36	0.435	µm

Matching parameters

Name	Description	Typ	Unit
AR_NP1	pelgrom coefficient resistor mismatch	4.9	%µm
DWRNP1	resistor delta width	0.06	µm

rnp1_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V



3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rnp1_3 → Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/μm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65μW/μm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENP1_3SB	N+ poly 1 silicide block edge resistance per terminal (underlying NWELL/PWELL2, 3 terminals)	-	-	65	-	-	Ωμm
RSRNP1_3	N+ poly 1 sheet resistance (underlying NWELL/PWELL2, 3 terminals)	220	280	340	400	460	Ω/□
TC1NP1_3	N+ poly 1 temperature coefficient 1 (underlying NWELL/PWELL2, 3 terminals)	-	-1.71	-1.54	-1.37	-	1e-03/K
TC1NP1_3RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying NWELL/PWELL2, 3 terminals)	-	-	-1.4	-	-	1e-03/K
TC2NP1_3	N+ poly 1 temperature coefficient 2 (underlying NWELL/PWELL2, 3 terminals)	-	2.4	3	3.6	-	1e-06/K ²
TC2NP1_3RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying NWELL/PWELL2, 3 terminals)	-	-	0.3	-	-	1e-06/K ²
VCBNP1_3	N+ poly 1 bulk voltage coefficient (underlying NWELL/PWELL2, 3 terminals)	-	-	0.08	-	-	1e-03/V
WERNP1_3	N+ poly 1 effective width (underlying NWELL/PWELL2, 3 terminals) @ W=0.42μm	-	0.31	0.37	0.43	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_NP1	pelgrom coefficient resistor mismatch	4.9	%μm
DWRNP1_3	resistor delta width	0.05	μm

rnp1a_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/μm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65μW/μm².

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rnp1a_3 → Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENP1ASB	N+ poly 1 silicide block edge resistance per terminal (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	65	-	-	Ωµm
RSRNP1A	N+ poly 1 sheet resistance (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	200	245	290	335	380	Ω/□
TC1NP1A	N+ poly 1 temperature coefficient 1 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-1.53	-1.4	-1.27	-	1e-03/K
TC1NP1ARSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	-1.4	-	-	1e-03/K
TC2NP1A	N+ poly 1 temperature coefficient 2 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	2.05	2.5	2.95	-	1e-06/K ²
TC2NP1ARSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	0.3	-	-	1e-06/K ²
VCBNP1A	N+ poly 1 bulk voltage coefficient (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	0.08	-	-	1e-03/V
WERNP1A	N+ poly 1 effective width (underlying PWELL1/PWELL3/PWELL5, 3 terminals) @ W=0.42µm	-	0.29	0.35	0.41	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NP1	pelgrom coefficient resistor mismatch	4.9	%µm
DWRNP1A	resistor delta width	0.07	µm

rpp1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65µW/µm².

Process parameters

Name	Description	Low	Typ	High	Unit
RSEPP1SB	P+ poly 1 silicide block edge resistance per terminal (2 terminals)	-	70	-	Ωµm
RSRPP1	P+ poly 1 sheet resistance (2 terminals)	230	275	320	Ω/□
TC1PP1	P+ poly 1 temperature coefficient 1 (2 terminals)	-0.17	-0.08	0.01	1e-03/K

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rpp1 → Process parameters

Name	Description	Low	Typ	High	Unit
TC1PP1RSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (2 terminals)	-	-1.2	-	1e-03/K
TC2PP1	P+ poly 1 temperature coefficient 2 (2 terminals)	0.3	0.75	1.2	1e-06/K ²
TC2PP1RSE	P + poly 1 silicide block edge resistance temperature coefficient 2 (2 terminals)	-	0.2	-	1e-06/K ²
WERPP1	P+ poly 1 effective width (2 terminals) @ W=0.42μm	0.305	0.365	0.425	μm

Matching parameters

Name	Description	Typ	Unit
AR_PP1	pelgrom coefficient resistor mismatch	1.7	%μm
DWRPP1	resistor delta width	0.055	μm

rpp1_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/μm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65μW/μm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPP1PWSB	P+ poly 1 silicide block edge resistance per terminal (underlying PWELL, 3 terminals)	-	-	70	-	-	Ωμm
RSRPP1PW	P+ poly 1 sheet resistance (underlying PWELL, 3 terminals)	225	255	285	315	345	Ω/□
TC1PP1PW	P+ poly 1 temperature coefficient 1 (underlying PWELL, 3 terminals)	-	-0.16	-0.1	-0.04	-	1e-03/K
TC1PP1PWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying PWELL, 3 terminals)	-	-	-1.2	-	-	1e-03/K
TC2PP1PW	P+ poly 1 temperature coefficient 2 (underlying PWELL, 3 terminals)	-	0.55	0.85	1.15	-	1e-06/K ²
TC2PP1PWRSE	P + poly 1 silicide block edge resistance temperature coefficient 2 (underlying PWELL, 3 terminals)	-	-	0.2	-	-	1e-06/K ²
VCBPP1PW	P+ poly 1 bulk voltage coefficient (underlying PWELL, 3 terminals)	-	-	-0.05	-	-	1e-03/V
WERPP1PW	P+ poly 1 effective width (underlying PWELL, 3 terminals) @ W=0.42μm	-	0.325	0.37	0.415	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_PP1	pelgrom coefficient resistor mismatch	1.7	%μm
DWRPP1PW	resistor delta width	0.05	μm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rpp1nw_3 → Operating conditions

rpp1nw_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/μm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65μW/μm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPP1NWSB	P+ poly 1 silicide block edge resistance per terminal (underlying NWELL, 3 terminals)	-	-	70	-	-	Ωμm
RSRPP1NW	P+ poly 1 sheet resistance (underlying NWELL, 3 terminals)	210	240	270	300	330	Ω/□
TC1PP1NW	P+ poly 1 temperature coefficient 1 (underlying NWELL, 3 terminals)	-	-0.13	-0.07	-0.01	-	1e-03/K
TC1PP1NWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying NWELL, 3 terminals)	-	-	-1.2	-	-	1e-03/K
TC2PP1NW	P+ poly 1 temperature coefficient 2 (underlying NWELL, 3 terminals)	-	0.4	0.7	1	-	1e-06/K ²
TC2PP1NWRSE	P + poly 1 silicide block edge resistance temperature coefficient 2 (underlying NWELL, 3 terminals)	-	-	0.2	-	-	1e-06/K ²
VCBPP1NW	P+ poly 1 bulk voltage coefficient (underlying NWELL, 3 terminals)	-	-	-0.05	-	-	1e-03/V
WERPP1NW	P+ poly 1 effective width (underlying NWELL, 3 terminals) @ W=0.42μm	-	0.315	0.36	0.405	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_PP1	pelgrom coefficient resistor mismatch	1.7	%μm
DWRPP1NW	resistor delta width	0.06	μm

rpp1s, rpp1s_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRPP1S	P+ poly 1 sheet resistance (salicided)	5.2	6.3	7.5	8.7	9.8	Ω/□
TC1PP1S	P+ poly 1 temperature coefficient 1	-	2.74	3.1	3.46	-	1e-03/K

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → rpp1s, rpp1s_3 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC2PP1S	P+ poly 1 temperature coefficient 2	-	-1.12	0.08	1.28	-	1e-06/K ²
WERPP1S	P+ poly 1 effective width (salicided) @ W=0.18µm	-	0.13	0.16	0.19	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_PP1S	pelgrom coefficient resistor mismatch	1.65	%µm
DWRPP1S	resistor delta width	0.02	µm

rm1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M1	metal 1 sheet resistance	61	69	77	85	93	mΩ/□
TC1_MET	metal 1 / metal 2 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_MET	metal 1 / metal 2 temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_M1B	metal 1 effective width @ W=0.23µm	-	0.18	0.21	0.24	-	µm

rm2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M2	metal 2 sheet resistance	58	66	74	82	90	mΩ/□
TC1_MET	metal 1 / metal 2 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_MET	metal 1 / metal 2 temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_M2	metal 2 effective width @ W=0.28µm	-	0.2	0.24	0.28	-	µm

mosvc

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VBpsub	-40°C to 175°C	-0.5	0	5.5	7	V

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → mosvc → Process parameters

Process parameters

Name	Description	Typ	Unit
CNV_MVC	varactor capacitance at negative voltage @ Vterm=-1.8V, f=100kHz	2.4	fF/ μm^2
CPV_MVC	varactor capacitance at positive voltage @ Vterm=1.8V, f=100kHz	8	fF/ μm^2
TUR_MVC	tuning range @ Vlow=-1.8V, Vhigh=1.8V, f=100kHz	70	%

mosvc5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB ⁽¹⁾	-40°C to 175°C	-7	-1.98	5.5	7	V
VBpsub	-40°C to 175°C	-0.5	0	5.5	7	V

Note 1 VGB Min operating condition means a model limit. Between VGB Min and VGB Abs.Min, the device will be very slow in terms of charge carriers because it works in deep depletion region. Only thermally generated charge carriers are available which lead to very large time constants at low temperatures. The C-V-curve will show memory effects when used between VGB=-1.98V...-7V. This effect can not be modeled.

Process parameters

Name	Description	Typ	Unit
CNV_MVC5	varactor capacitance at negative voltage @ Vterm=-1.8V, f=100kHz	0.9	fF/ μm^2
CPV_MVC5	varactor capacitance at positive voltage @ Vterm=5V, f=100kHz	2.5	fF/ μm^2
TUR_MVC5	tuning range @ Vlow=-1.8V, Vhigh=5V, f=100kHz	64	%

csf2p

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFP2	csf2p breakdown voltage @ Ibr=1 μA	15	-	-	V
CA_SFP2_B	csf2p capacitance per cell @ Vbias=0V, L=10.8 μm , W=4.48 μm	22.8	25.2	27.6	fF
IL_SFP2	csf2p leakage current @ VL=5.5V, L=10.8 μm , W=4.48 μm	-	-	50	fA/cell
	Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.				
TC1_SFP2	csf2p temperature coefficient 1 @ Tnom=27°C	-	0.25	-	1e-03/K
TC2_SFP2	csf2p temperature coefficient 2 @ Tnom=27°C	-	-1.2	-	1e-06/K ²
VC1_SFP2	csf2p capacitor voltage coefficient 1	-	81	-	ppm/V
VC2_SFP2	csf2p capacitor voltage coefficient 2	-	100	-	ppm/V ²

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → csf2p → Matching parameters

Matching parameters

Name	Description	Typ	Unit
AC_CSFP	pelgrom coefficient capacitor mismatch @ L=10.8µm, W=4.48µm	0.5	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

dn

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNPW1	breakdown voltage NDIFF / PWELL1 @ Irev=1µA, L=70µm, W=40µm	6	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CJANPW1	area junction capacitance	-	-	1.27	-	-	fF/µm ²
CJPNPW1	sidewall junction capacitance	-	-	0.35	-	-	fF/µm
ILA NPW1	diode area leakage current @ Vrev=1.98V, T=27°C	-	-	0.017	-	-	fA/µm ²
ILA NPW1 HT	diode area leakage current @ Vrev=1.98V, T=175°C	-	-	0.3	-	-	pA/µm ²
ILP NPW1	diode perimeter leakage current @ Vrev=1.98V, T=27°C	-	-	0.29	-	-	fA/µm
ILP NPW1 HT	diode perimeter leakage current @ Vrev=1.98V, T=175°C	-	-	1.17	-	-	pA/µm
MJANPW1	area grading coefficient	-	-	0.48	-	-	-
MJPNPW1	sidewall grading coefficient	-	-	0.25	-	-	-
PBANPW1	area junction potential	-	-	1.03	-	-	V
PBPNPW1	sidewall junction potential	-	-	0.74	-	-	V

Note: dn is also used as parasitic diode p_dn.

dnn

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	Typ	Unit
CJANN	area junction capacitance	0.18	fF/µm ²

3. Parameters → 3.1 LP5MOS main module→ 3.1.2 Device parameters→ dnn→ Process parameters

Name	Description	Typ	Unit
CJPNN	sidewall junction capacitance	0.3	fF/ μ m
ILANN	diode area leakage current @ Vrev=1.98V, T=27°C	0.002	fA/ μ m²
ILANNHT	diode area leakage current @ Vrev=1.98V, T=175°C	0.35	pA/ μ m²
ILPNN	diode perimeter leakage current @ Vrev=1.98V, T=27°C	0.095	fA/ μ m
ILPNNHT	diode perimeter leakage current @ Vrev=1.98V, T=175°C	0.78	pA/ μ m
MJANN	area grading coefficient	0.31	-
MJPNN	sidewall grading coefficient	0.05	-
PBANNN	area junction potential	0.68	V
PBPNN	sidewall junction potential	0.46	V

Note: dnn is also used as parasitic diode p_dnn.

dp**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-2.3	-1.98	0	0.5	V
Vcathode-Vpsub	-40°C to 175°C	-0.5	0	5.5	7	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPNW1	breakdown voltage PDIFF / NWELL1 @ Irev=1 μ A, L=70 μ m, W=40 μ m	6	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CJAPNW1	area junction capacitance	-	-	0.98	-	-	fF/ μ m²
CJPPNW1	sidewall junction capacitance	-	-	0.21	-	-	fF/ μ m
ILA PNW1	diode area leakage current @ Vrev=1.98V, T=27°C	-	-	0.002	-	-	fA/ μ m²
ILA PNW1HT	diode area leakage current @ Vrev=1.98V, T=175°C	-	-	330	-	-	fA/ μ m²
ILPPNW1	diode perimeter leakage current @ Vrev=1.98V, T=27°C	-	-	0.1	-	-	fA/ μ m
ILPPNW1HT	diode perimeter leakage current @ Vrev=1.98V, T=175°C	-	-	0.39	-	-	pA/ μ m
MJAPNW1	area grading coefficient	-	-	0.43	-	-	-
MJPPNW1	sidewall grading coefficient	-	-	0.09	-	-	-
PBAPNW1	area junction potential	-	-	0.93	-	-	V
PBPPNW1	sidewall junction potential	-	-	1.12	-	-	V

Note: dp is also used as parasitic diode p_dp.

dnw**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V

⇒

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → dnw → Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNW1	breakdown voltage NWELL1 / PSUB @ Irev=1µA, L=70µm, W=40µm	9	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANW1	area junction capacitance	-	-	0.21	-	-	fF/µm ²
CJPNW1	sidewall junction capacitance	-	-	0.48	-	-	fF/µm
ILA_NW1	diode area leakage current @ Vrev=5.5V, T=27°C	-	-	0.004	-	-	fA/µm ²
ILA_NW1HT	diode area leakage current @ Vrev=5.5V, T=175°C	-	-	0.97	-	-	pA/µm ²
ILPNW1	diode perimeter leakage current @ Vrev=5.5V, T=27°C	-	-	0.07	-	-	fA/µm
ILPNW1HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	-	-	0.24	-	-	pA/µm
MJANW1	area grading coefficient	-	-	0.35	-	-	-
MJPNW1	sidewall grading coefficient	-	-	0.29	-	-	-
PBANW1	area junction potential	-	-	0.46	-	-	V
PBPNW1	sidewall junction potential	-	-	0.86	-	-	V

Note: dnw is also used as parasitic diode p_dnw.

dn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNPW2	breakdown voltage NDIFF / PWELL2 @ Irev=1µA, L=70µm, W=40µm	8	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CJANPW2	area junction capacitance	-	-	1.02	-	-	fF/µm ²
CJPNPW2	sidewall junction capacitance	-	-	0.21	-	-	fF/µm
ILA_NPW2	diode area leakage current @ Vrev=5.5V, T=27°C	-	-	0.016	-	-	fA/µm ²
ILA_NPW2HT	diode area leakage current @ Vrev=5.5V, T=175°C	-	-	0.4	-	-	pA/µm ²
ILPNPW2	diode perimeter leakage current @ Vrev=5.5V, T=27°C	-	-	1.44	-	-	fA/µm
ILPNPW2HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	-	-	1.41	-	-	pA/µm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → dn5 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
MJANPW2	area grading coefficient	-	-	0.34	-	-	-
MJPNPW2	sidewall grading coefficient	-	-	0.05	-	-	-
PBANPW2	area junction potential	-	-	0.82	-	-	V
PBPNPW2	sidewall junction potential	-	-	1.2	-	-	V

dnn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	Typ	Unit
CJANN5	area junction capacitance	0.18	fF/μm ²
CJPNN5	sidewall junction capacitance	0.32	fF/μm
ILANN5	diode area leakage current @ Vrev=5.5V, T=27°C	0.012	fA/μm ²
ILANN5HT	diode area leakage current @ Vrev=5.5V, T=175°C	0.39	pA/μm ²
ILPNN5	diode perimeter leakage current @ Vrev=5.5V, T=27°C	0.31	fA/μm
ILPNN5HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	1.18	pA/μm
MJANN5	area grading coefficient	0.36	-
MJPNN5	sidewall grading coefficient	0.07	-
PBANN5	area junction potential	1.2	V
PBPNNN5	sidewall junction potential	0.46	V

Note: dnn5 is also used as parasitic diode p_dnn5.

dp5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V
Vcathode-Vpsub	-40°C to 175°C	-0.5	0	5.5	7	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPNW2	breakdown voltage PDIFF / NWELL2 @ Irev=1μA, L=70μm, W=40μm	7.5	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CJAPNW2	area junction capacitance	-	-	1.29	-	-	fF/μm ²
CJPPNW2	sidewall junction capacitance	-	-	0.22	-	-	fF/μm

3. Parameters → 3.1 LP5MOS main module → 3.1.2 Device parameters → dp5 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ILA PNW2	diode area leakage current @ Vrev=5.5V, T=27°C	-	-	0.13	-	-	fA/μm²
ILA PNW2HT	diode area leakage current @ Vrev=5.5V, T=175°C	-	-	0.9	-	-	pA/μm²
ILP PNW2	diode perimeter leakage current @ Vrev=5.5V, T=27°C	-	-	15.2	-	-	fA/μm
ILP PNW2HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	-	-	2.82	-	-	pA/μm
MJA PNW2	area grading coefficient	-	-	0.44	-	-	-
MJP PNW2	sidewall grading coefficient	-	-	0.05	-	-	-
PBA PNW2	area junction potential	-	-	1.04	-	-	V
PBP PNW2	sidewall junction potential	-	-	0.46	-	-	V

dnw5**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJ NW2	breakdown voltage NWELL2 / PWELL2 @ Irev=1μA, L=70μm, W=40μm	9	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CJA NW2	area junction capacitance	-	-	0.21	-	-	fF/μm²
CJP NW2	sidewall junction capacitance	-	-	0.47	-	-	fF/μm
ILA NW2	diode area leakage current @ Vrev=5.5V, T=27°C	-	-	0.005	-	-	fA/μm²
ILA NW2HT	diode area leakage current @ Vrev=5.5V, T=175°C	-	-	1.11	-	-	pA/μm²
ILP NW2	diode perimeter leakage current @ Vrev=5.5V, T=27°C	-	-	0.1	-	-	fA/μm
ILP NW2HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	-	-	0.18	-	-	pA/μm
MJA NW2	area grading coefficient	-	-	0.3	-	-	-
MJP NW2	sidewall grading coefficient	-	-	0.29	-	-	-
PBA NW2	area junction potential	-	-	0.46	-	-	V
PBP NW2	sidewall junction potential	-	-	0.51	-	-	V

pfuse**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm1-Vterm2 ⁽¹⁾	-40°C to 175°C	-0.2	-0.1	0.1	0.2	V

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3. Parameters → 3.1 LP5MOS main module→ 3.1.2 Device parameters→ pfuse→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm1-Vterm2 ⁽²⁾	-40°C to 175°C	-5	-3.6	3.6	5	V

Note 1 unprogrammed state

Note 2 programmed state

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RP_FUSE	programmed fuse resistance @ Vbias=3.3V	-	100	-	-	-	kΩ
	Note: The values of this parameter do not reflect the statistics of the process.						
RU_FUSE	unprogrammed fuse resistance @ Isupply=50µA	10	25	40	55	70	Ω

Note: For the primitive device pfuse, the programming conditions and further information are available in the "[Application Note – EasyFuse](#)" on "my X-FAB."

3. Parameters → 3.2 MOS5 main module

3.2 MOS5 main module

3.2.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_ILD1	metal 1 / substrate equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
EPS_IMD1	metal 1 / metal 2 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
RSWAFDL	SOI wafer: device layer resistivity	66	100	134	Ωcm
RSWAFHW	SOI wafer: handle wafer resistivity	70	100	130	Ωcm
THD_ILD1	metal 1 - active dielectric thickness	840	990	1140	nm
THD_IMD1	metal 2 - metal 1 dielectric thickness	765	850	935	nm
THD_M1P1	metal 1 - poly 1 dielectric thickness	640	790	940	nm
THD_M1STI	metal 1 field dielectric thickness	1240	1390	1540	nm
THGN5	5.0V gate oxide thickness (measured on NMOS capacitor)	12.2	12.7	13.2	nm
THGP5	5.0V gate oxide thickness(measured on PMOS capacitor)	12.2	12.7	13.2	nm
THOBOX	SOI wafer: buried oxide thickness	950	1000	1050	nm
	Note: The thickness is given in reference to wafer supplier specification				
THV	passivation thickness	1570	1750	1930	nm
	Note: Passivation is composed from the following stack (bottom to top): silicon oxide/silicon nitride.				
THV_THK	passivation thickness with METTHK module	1920	2200	2480	nm
	Note: Passivation is composed from the following stack (bottom to top): silicon oxide/silicon nitride.				
TH_DL	SOI wafer: device layer thickness	3435	3500	3565	nm
	Note: The thickness is given in reference to wafer supplier specification				
TH_M1	metal 1 thickness	505	565	625	nm
TH_M2	metal 2 thickness	505	565	625	nm
TH_P1	poly 1 thickness	180	200	220	nm
TH_WAF	wafer thickness	710	725	740	μm
	Note: The thickness is given in reference to wafer supplier specification				
XJ_N	N+ source/ drain junction depth	-	0.2	-	μm
XJ_NW2	NWELL2 junction depth	-	1.5	-	μm
XJ_P	P+ source/ drain junction depth	-	0.2	-	μm
XT_STI	STI depth	360	400	440	nm

3. Parameters → 3.2 MOS5 main module→ 3.2.1 Device independent p...→ Structural and geom...

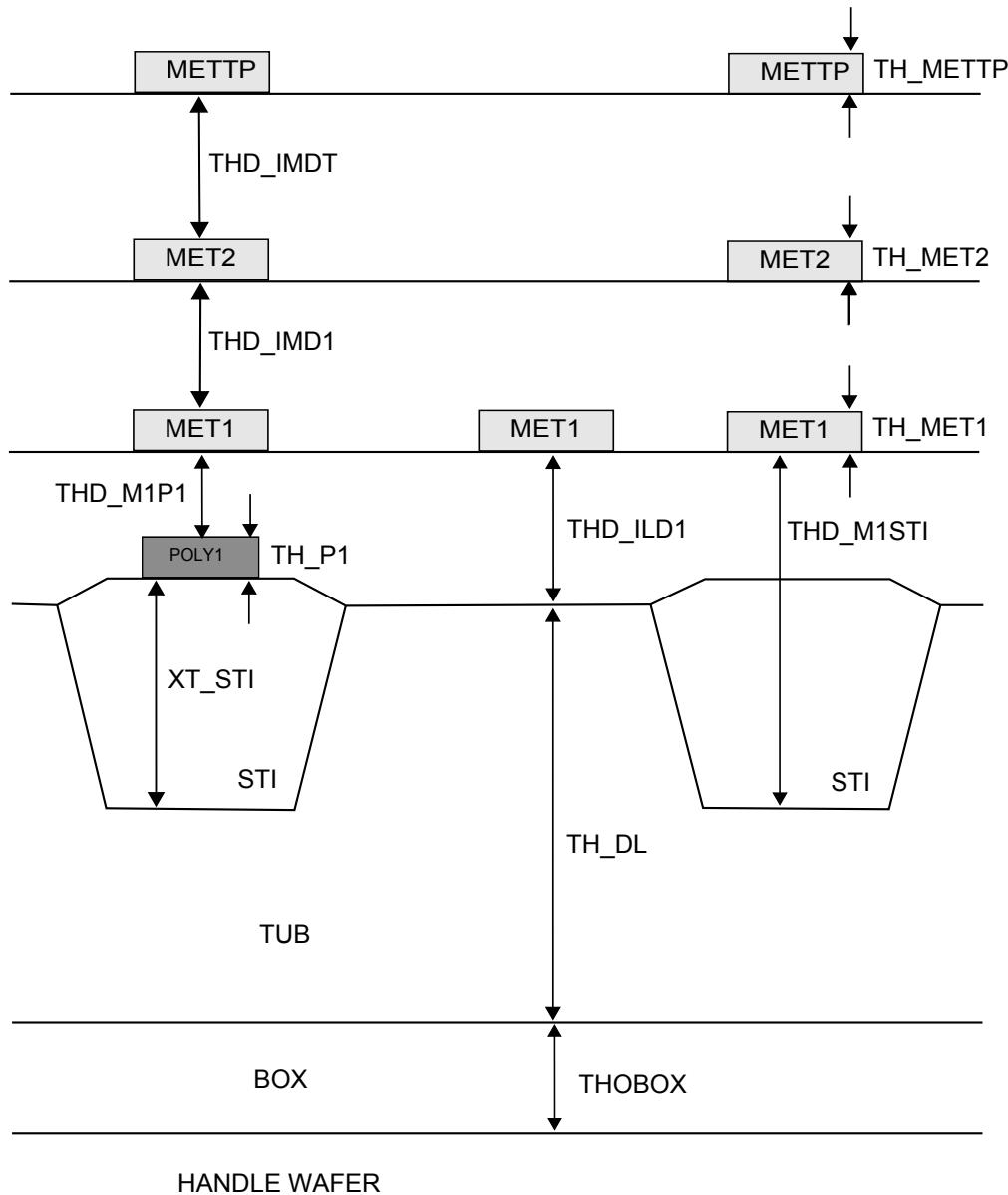


Figure 3.9 Cross-Sectional diagram showing layer thickness values

Parasitic field parameters

Name	Description	Low	Typ	High	Unit
VTFNM1PW2	n-channel threshold voltage metal 1 on field over PWELL2 @ VD=5V, Id=1µA, L=0.28µm, W=210µm	40	-	-	V
VTFNP1PW2	n-channel threshold voltage poly 1 on field over PWELL2, @ VD=5V, Id=1µA, L=0.28µm, W=210µm	8	-	-	V
VTFPM1NW2	p-channel threshold voltage metal 1 on field over NWELL2 @ VD=-5V, Id=-1µA, L=0.28µm, W=210µm	-	-	-40	V
VTFPP1NW2	p-channel threshold voltage poly 1 on field over NWELL2 @ VD=-5V, Id=-1µA, L=0.28µm, W=210µm	-	-	-8	V

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RCTNDM	metal 1 - N+ contact resistance	-	5.5	7.5	9.8	12	Ω/cnt

3. Parameters → 3.2 MOS5 main module→ 3.2.1 Device independent p...→ Sheet and contact re...

Name	Description	LSL	Low	Typ	High	USL	Unit
RCTNMP1	metal 1 - N+ poly 1 contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RCTPDM	metal 1 - P+ contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RCTPMP1	metal 1 - P+ poly 1 contact resistance	-	5.5	7.5	9.8	12	Ω/cnt
RSENP1ASB	N+ poly 1 silicide block edge resistance per terminal (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	65	-	-	Ωµm
RSENP1SB	N+ poly 1 silicide block edge resistance per terminal (2 terminals)	-	-	65	-	-	Ωµm
RSENP1_3SB	N+ poly 1 silicide block edge resistance per terminal (underlying NWELL/PWELL2, 3 terminals)	-	-	65	-	-	Ωµm
RSEPP1PWSB	P+ poly 1 silicide block edge resistance per terminal (underlying PWELL, 3 terminals)	-	-	70	-	-	Ωµm
RSEPP1SB	P+ poly 1 silicide block edge resistance per terminal (2 terminals)	-	-	70	-	-	Ωµm
RSRNNS	NDIFF (salicided) sheet resistance	-	-	6.4	7.9	9.4	Ω/□
RSRNP1	N+ poly 1 sheet resistance (2 terminals)	-	225	315	405	-	Ω/□
RSRNP1A	N+ poly 1 sheet resistance (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	200	245	290	335	380	Ω/□
RSRNP1S	N+ poly 1 (salicided) sheet resistance	-	-	7.5	-	-	Ω/□
RSRNP1_3	N+ poly 1 sheet resistance (underlying NWELL/PWELL2, 3 terminals)	220	280	340	400	460	Ω/□
RSRNW2	NWELL2 sheet resistance (STI terminated)	840	1020	1200	1380	1560	Ω/□
RSRPP1	P+ poly 1 sheet resistance (2 terminals)	-	230	275	320	-	Ω/□
RSRPP1NW	P+ poly 1 sheet resistance (underlying NWELL, 3 terminals)	210	240	270	300	330	Ω/□
RSRPP1PW	P+ poly 1 sheet resistance (underlying PWELL, 3 terminals)	225	255	285	315	345	Ω/□
RSRPP1S	P+ poly 1 sheet resistance (salicided)	5.2	6.3	7.5	8.7	9.8	Ω/□
RSRPPS	PDIFF (salicided) sheet resistance	-	-	7.1	8.6	10.1	Ω/□
RSR_M1	metal 1 sheet resistance	61	69	77	85	93	mΩ/□
RSR_M2	metal 2 sheet resistance	58	66	74	82	90	mΩ/□
RSSPTUB	PTUB_SUB sheet resistance	-	-	3500	-	-	Ω/□
RVI_V1	VIA1 resistance	-	3	4.5	6.75	9	Ω/via
TC1NP1	N+ poly 1 temperature coefficient 1 (2 terminals)	-	-1.73	-1.47	-1.22	-	1e-03/K
TC1NP1A	N+ poly 1 temperature coefficient 1 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-1.53	-1.4	-1.27	-	1e-03/K
TC1NP1ARSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	-1.4	-	-	1e-03/K

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3. Parameters → 3.2 MOS5 main module→ 3.2.1 Device independent p...→ Sheet and contact re...

Name	Description	LSL	Low	Typ	High	USL	Unit
TC1NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (2 terminals)	-	-	-1.4	-	-	1e-03/K
TC1NP1_3	N+ poly 1 temperature coefficient 1 (underlying NWELL/PWELL2, 3 terminals)	-	-1.71	-1.54	-1.37	-	1e-03/K
TC1NP1_3RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying NWELL/PWELL2, 3 terminals)	-	-	-1.4	-	-	1e-03/K
TC1PP1	P+ poly 1 temperature coefficient 1 (2 terminals)	-	-0.17	-0.08	0.01	-	1e-03/K
TC1PP1PW	P+ poly 1 temperature coefficient 1 (underlying PWELL, 3 terminals)	-	-0.16	-0.1	-0.04	-	1e-03/K
TC1PP1PWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying PWELL, 3 terminals)	-	-	-1.2	-	-	1e-03/K
TC1PP1RSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (2 terminals)	-	-	-1.2	-	-	1e-03/K
TC1PP1S	P+ poly 1 temperature coefficient 1	-	2.74	3.1	3.46	-	1e-03/K
TC1_CT	contact resistance temperature coefficient 1	-	-	2.15	-	-	1e-03/K
TC1_V1	VIA1 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2NP1	N+ poly 1 temperature coefficient 2 (2 terminals)	-	1.85	2.75	3.65	-	1e-06/K ²
TC2NP1A	N+ poly 1 temperature coefficient 2 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	2.05	2.5	2.95	-	1e-06/K ²
TC2NP1ARSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying PWELL1/PWELL3/PWELL5, 3 terminals)	-	-	0.3	-	-	1e-06/K ²
TC2NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (2 terminals)	-	-	0.3	-	-	1e-06/K ²
TC2NP1_3	N+ poly 1 temperature coefficient 2 (underlying NWELL/PWELL2, 3 terminals)	-	2.4	3	3.6	-	1e-06/K ²
TC2NP1_3RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying NWELL/PWELL2, 3 terminals)	-	-	0.3	-	-	1e-06/K ²
TC2PP1	P+ poly 1 temperature coefficient 2 (2 terminals)	-	0.3	0.75	1.2	-	1e-06/K ²
TC2PP1PW	P+ poly 1 temperature coefficient 2 (underlying PWELL, 3 terminals)	-	0.55	0.85	1.15	-	1e-06/K ²
TC2PP1PWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying PWELL, 3 terminals)	-	-	0.2	-	-	1e-06/K ²
TC2PP1RSE	P+ poly 1 silicide block edge resistance temperature coefficient 2 (2 terminals)	-	-	0.2	-	-	1e-06/K ²



3. Parameters → 3.2 MOS5 main module→ 3.2.1 Device independent p...→ Sheet and contact re...

Name	Description	LSL	Low	Typ	High	USL	Unit
TC2PP1S	P+ poly 1 temperature coefficient 2	-	-1.12	0.08	1.28	-	1e-06/K ²
TC2_CT	contact resistance temperature coefficient 2	-	-	0	-	-	1e-06/K ²
TC2_V1	VIA1 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WERNNS	NDIFF (salicided) effective width @ W=0.42µm	-	0.42	0.48	0.54	-	µm
WERPPS	PDIFF (salicided) effective width @ W=0.42µm	-	0.4	0.46	0.52	-	µm

Gate oxide parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDON5	5.0V NMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm ²	11	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BDOP5	5.0V PMOS gate oxide breakdown voltage @ Ibr=0.1nA/µm ²	11	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGAN5	5.0V NMOS gate oxide area capacitance @ Vbias=5.5V	-	2.62	2.71	2.83	-	fF/µm ²
CGAP5	5.0V PMOS gate oxide area capacitance @ Vbias=-5.5V	2.5	2.62	2.71	2.83	2.94	fF/µm ²
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CGON5	5.0V NMOS gate – source/drain overlap	-	-	0.11	-	-	fF/µm
CGOP5	5.0V PMOS gate – source/drain overlap	-	-	0.13	-	-	fF/µm

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances.

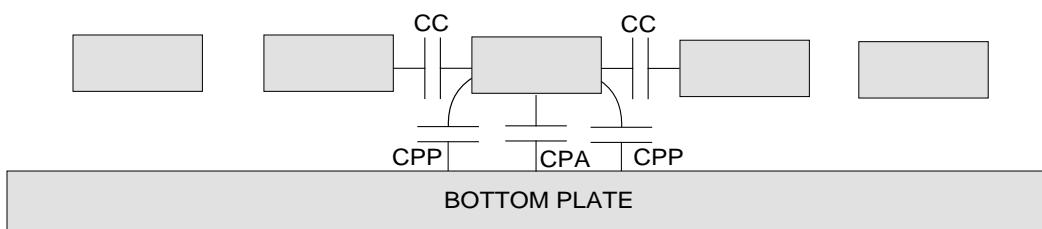


Figure 3.10 Parasitic capacitance structure

Name	Description	Typ	Unit
CC_M1M1	coupling capacitance metal 1 – metal 1	113	aF/µm
CC_M2M2	coupling capacitance metal 2 – metal 2	97	aF/µm
CC_P1P1	coupling capacitance poly 1 – poly 1	56	aF/µm
CPAM1DIFF	metal 1 – active area capacitance	35.9	aF/µm ²
CPAM1P1	metal 1 – poly 1 area capacitance	45.4	aF/µm ²
CPAM1STI	metal 1 – field area (STI) area capacitance	25.6	aF/µm ²
CPAM2DIFF	metal 2 – active area capacitance	14.6	aF/µm ²

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3. Parameters → 3.2 MOS5 main module→ 3.2.1 Device independent p...→ Parasitic capacitanc...

Name	Description	Typ	Unit
CPAM2M1	metal 2 – metal 1 area capacitance	41.5	aF/ μm^2
CPAM2P1	metal 2 – poly 1 area capacitance	16	aF/ μm^2
CPAM2STI	metal 2 – field area (STI) area capacitance	12.5	aF/ μm^2
CPASTI	poly 1 – field area (STI) area capacitance	88.5	aF/ μm^2
CPATUB	tub-handle wafer area capacitance	0.0345	fF/ μm^2
CPPM1DIFF	metal 1 – active perimeter capacitance	10.3	aF/ μm
CPPM1P1	metal 1 – poly 1 perimeter capacitance	7.8	aF/ μm
CPPM1STI	metal 1 – field area (STI) perimeter capacitance	9.2	aF/ μm
CPPM2DIFF	metal 2 – active perimeter capacitance	7.9	aF/ μm
CPPM2M1	metal 2 – metal 1 perimeter capacitance	8.3	aF/ μm
CPPM2P1	metal 2 – poly 1 perimeter capacitance	5	aF/ μm
CPPM2STI	metal 2 – field area (STI) perimeter capacitance	7.6	aF/ μm
CPPSTI	poly 1 – field area (STI) perimeter capacitance	15.1	aF/ μm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_CT_DC ⁽¹⁾	Contact	-40°C to 175°C	-	-	0.53	-	mA/cnt
JMax_DC ⁽²⁾⁽¹⁾	Poly 1	-40°C to 175°C	-	-	1	-	mA/ μm
JMax_DC ⁽³⁾⁽¹⁾	Metal 1	-40°C to 175°C	-	-	1	20	mA/ μm
JMax_DC ⁽³⁾⁽¹⁾	Metal 2	-40°C to 175°C	-	-	1	20	mA/ μm
JMax_N_DC ⁽⁴⁾⁽¹⁾	Metal 1	-40°C to 175°C	-	-	0.5	20	mA/ μm
JMax_N_DC ⁽⁴⁾⁽¹⁾	Metal 2	-40°C to 175°C	-	-	0.5	20	mA/ μm
JMax_VI_DC ⁽¹⁾	Via 1	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_CT_AC ⁽⁵⁾	Contact	-40°C to 175°C	-	-	2.4	-	mA/cnt
JMax_AC ⁽³⁾⁽⁵⁾	Metal 1	-40°C to 175°C	-	-	4.5	20	mA/ μm
JMax_AC ⁽³⁾⁽⁵⁾	Metal 2	-40°C to 175°C	-	-	4.5	20	mA/ μm
JMax_N_AC ⁽⁴⁾⁽⁵⁾	Metal 1	-40°C to 175°C	-	-	2.2	20	mA/ μm
JMax_N_AC ⁽⁴⁾⁽⁵⁾	Metal 2	-40°C to 175°C	-	-	2.2	20	mA/ μm
JMax_VI_AC ⁽⁵⁾	Via 1	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4 ⁽⁶⁾⁽⁷⁾	Contact	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁷⁾	Metal 1	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁷⁾	Metal 2	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁷⁾	Via 1	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁶⁾	Contact	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁶⁾	Metal 1	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁶⁾	Metal 2	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁶⁾	Via 1	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁹⁾⁽⁶⁾	Contact	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e4 ⁽⁹⁾⁽⁶⁾	Metal 1	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4 ⁽⁹⁾⁽⁶⁾	Metal 2	125°C to 175°C	-	0.32	-	-	-

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3. Parameters → 3.2 MOS5 main module→ 3.2.1 Device independent p...→ Physical layer opera...

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
T_Factor_1e4 ⁽⁹⁾⁽⁶⁾	Via 1	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁷⁾	Contact	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁷⁾	Metal 1	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁷⁾	Metal 2	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁷⁾	Via 1	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁶⁾	Contact	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁶⁾	Metal 1	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁶⁾	Metal 2	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁶⁾	Via 1	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁹⁾⁽⁶⁾	Contact	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁹⁾⁽⁶⁾	Metal 1	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁹⁾⁽⁶⁾	Metal 2	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁹⁾⁽⁶⁾	Via 1	125°C to 175°C	-	0.1	-	-	-
E ⁽¹⁰⁾	Poly 1	-40°C to 175°C	-	-	150	-	V/μm
E ⁽¹¹⁾	Metal 1	-40°C to 175°C	-	-	250	-	V/μm
E ⁽¹²⁾	Metal 2	-40°C to 175°C	-	-	250	-	V/μm

Note 1 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 2 The specified values are valid for salicided polysilicon interconnects and salicided polysilicon resistors.

Note 3 track width > 0.44μm.

Note 4 track width ≤ 0.44μm.

Note 5 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 6 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 7 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 9 The temperature correction factor is interpolated between given values for temperatures above 125°C

Note 10 lateral electric field between Poly 1 track

Note 11 lateral electric field between Metal 1 track

Note 12 lateral electric field between Metal 2 track

3.2.2 Device parameters

ne5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	5.5	7	V
VDS	-40°C to 175°C	-7	-5.5	5.5	7	V
VDB	-40°C to 175°C	-0.5	0	5.5	7	V
VSB	-40°C to 175°C	-0.5	0	5.5	7	V



3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ ne5→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNE5S	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEXNE5	mobility exponent	-	-	-1.7	-	-	-
FC_NE5	corner frequency @ VD=5V, Id=1µA	-	-	5.44	-	-	kHz
GA_NE5	body factor long channel @ L=10µm, W=10µm	-	-	0.9	-	-	√V
IDSNE5S	saturation current @ VG=5V, VD=5V, L=0.5µm, W=10µm	470	498	525	552	580	µA/µm
IOFNE5S	off-state leakage @ VD=5V, L=0.5µm, W=10µm	-	-	-	0.5	-	pA/µm
ISBNE5S	bulk current @ VD=5V, L=0.5µm	-	-	5.8	-	-	µA/µm
KP_NE5	gain factor @ L=10µm, W=10µm	-	-	111	-	-	µA/V ²
LEFNE5	effective channel length @ L=0.5µm	-	-	0.45	-	-	µm
NOINE5	input referred noise @ VD=5V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	32.1	-	-	µVµm/√(Hz)
STSNE5	subthreshold slope @ VD=5V	-	-	10	-	-	decade/V
TC_VTXNE5	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-1.4	-	-	mV/K
U0_NE5	effective mobility	-	-	400	-	-	cm ² /(Vs)
VTINE5L	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.62	0.66	0.7	0.74	0.78	V
VTINE5S	threshold voltage short channel @ VD=0.1V, L=0.5µm, W=10µm	0.61	0.685	0.76	0.835	0.91	V
VTXNE5S	extrapolated threshold voltage short channel @ VD=0.1V, L=0.5µm, W=10µm	-	-	0.82	-	-	V
WEFNE5	effective channel width @ W=0.22µm	-	-	0.19	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNE5	pelgrom coefficient gain factor mismatch	1.72	%µm
AIDNE500	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	15.6	%µm
AIDNE502	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	7.91	%µm
AIDNE504	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	4.71	%µm
AIDNE506	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	3.21	%µm
AIDNE510	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	1.88	%µm
AIDNE520	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.91	%µm
AIDNE530	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.63	%µm
AIDNE550	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.43	%µm
AVTNE5	pelgrom coefficient threshold voltage mismatch	13.8	mVµm

⇒

3. Parameters → 3.2 MOS5 main module → 3.2.2 Device parameters → ne5 → Matching parameters

Name	Description	Typ	Unit
DLTNE5	transistor delta length	0.05	μm
DWTNE5	transistor delta width	0.03	μm

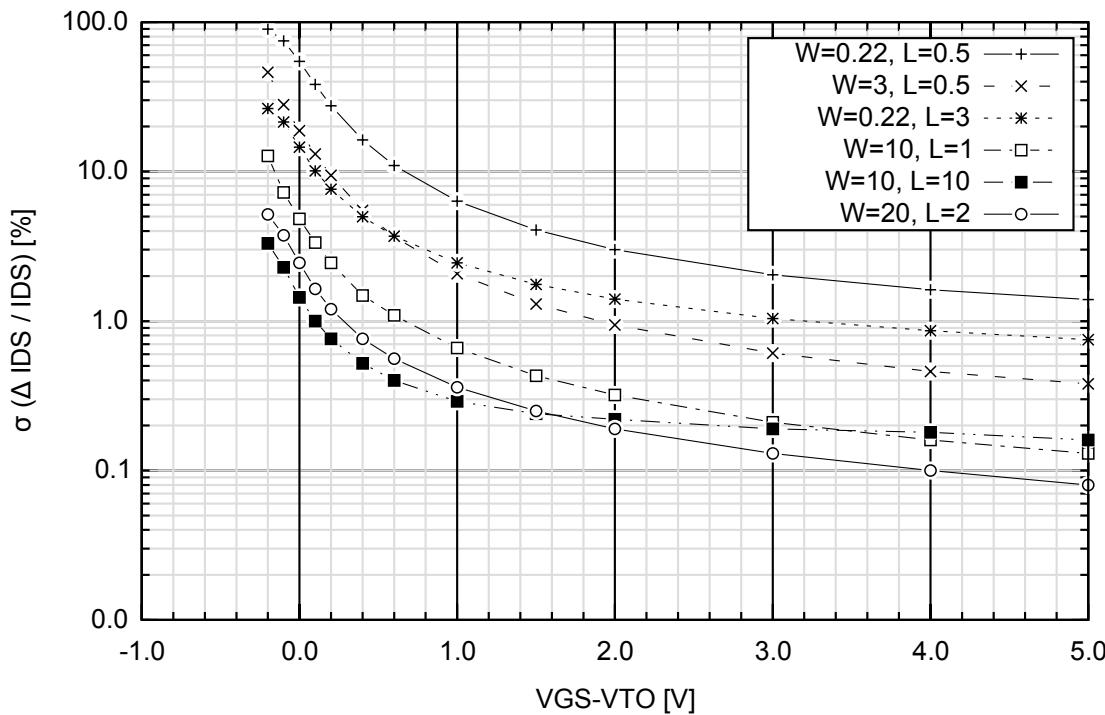


Figure 3.11 Device ne5: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	5.5	7	V
VDS	-40°C to 175°C	-7	-5.5	5.5	7	V
VDB	-40°C to 175°C	-0.5	0	5.5	7	V
VSB	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PTUB_SUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
FC_NN5	corner frequency @ VD=5V, Id=1μA	-	-	1.58	-	-	kHz
IDSNN5S	saturation current @ VG=5V, VD=5V, L=1μm, W=10μm	478	514	550	585	622	μA/μm
IDSNN5S2	saturation current @ VG=5V, VD=5V, L=2μm, W=10μm	-	-	388	-	-	μA/μm
IOF2NN5S2	off-state leakage @ VG=-0.5V, VD=5V, L=1μm, W=10μm	-	-	-	300	-	nA/μm

⇒

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ nn5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IOFNN5S2	off-state leakage @ VG=-0.5V, VD=5V, L=2μm, W=10μm	-	-	3	-	-	pA/μm
KP_NN5	gain factor @ L=10μm, W=10μm	-	-	150	-	-	μA/V ²
LEFNN5	effective channel length @ L=1μm	-	-	1.13	-	-	μm
NOINN5	input referred noise @ VD=5V, Id=1μA, f=1Hz, L=10μm, W=10μm	-	-	11.6	-	-	μVμm/√(Hz)
VTXNN5L	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=10μm	-0.185	-0.145	-0.105	-0.065	-0.025	V
VTXNN5S	extrapolated threshold voltage short channel @ VD=0.1V, L=1μm, W=10μm	-0.24	-0.2	-0.16	-0.12	-0.08	V
VTXNN5S2	extrapolated threshold voltage short channel @ VD=0.1V, L=2μm, W=10μm	-	-	-0.13	-	-	V
WEFNN5	effective channel width @ W=1μm	-	-	1	-	-	μm

Note: It is strongly recommended to use a channel length of $\geq 2\mu\text{m}$ when the nn and nn5 is operated in the sub-threshold region.

Matching parameters

Name	Description	Typ	Unit
ABTNN5	pelgrom coefficient gain factor mismatch	0.83	%μm
AIDNN500	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	8.95	%μm
AIDNN502	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	2.99	%μm
AIDNN504	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	1.63	%μm
AIDNN506	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	1.15	%μm
AIDNN510	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	0.8	%μm
AIDNN520	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.58	%μm
AIDNN530	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.51	%μm
AIDNN550	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.45	%μm
AVTNN5	pelgrom coefficient threshold voltage mismatch	3.43	mVμm
DLTNN5	transistor delta length	-0.13	μm
DWTNN5	transistor delta width	0	μm

3. Parameters → 3.2 MOS5 main module → 3.2.2 Device parameters → nn5 → Matching parameters

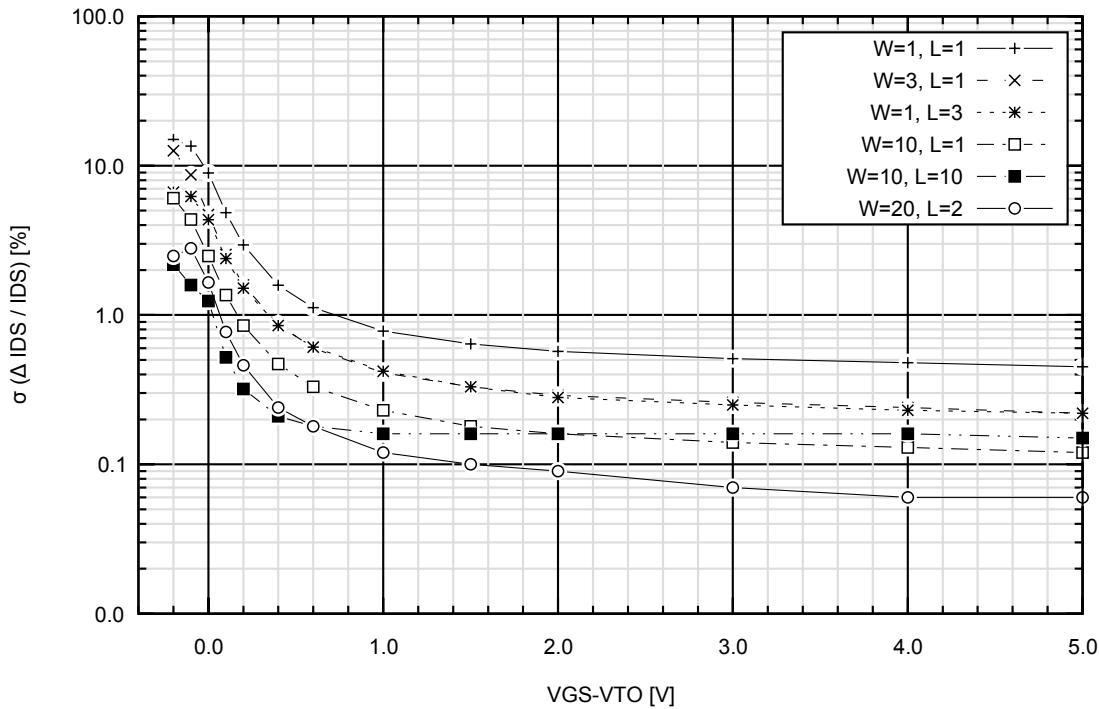


Figure 3.12 Device nn5: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pe5, pe5_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	5.5	7	V
VDS	-40°C to 175°C	-7	-5.5	5.5	7	V
VDB	-40°C to 175°C	-7	-5.5	0	0.5	V
VSB	-40°C to 175°C	-7	-5.5	0	0.5	V
VBptub	-40°C to 175°C	-0.5	0	5.5	7	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE5S	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	7.5	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEXPE5	mobility exponent	-	-	-1.2	-	-	-
FC_PE5	corner frequency @ VD=-5V, Id=-1µA	-	-	0.43	-	-	kHz
GA_PE5	body factor long channel @ L=10µm, W=10µm	-	-	1.1	-	-	√V
IDSPE5S	saturation current @ VG=-5V, VD=-5V, L=0.5µm, W=10µm	225	245	265	285	305	µA/µm

⇒

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ pe5, pe5_5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPE5S	off-state leakage @ VD=-5V, L=0.5μm, W=10μm	-	-	-	1	-	pA/μm
KP_PE5	gain factor @ L=10μm, W=10μm	-	-	28	-	-	μA/V ²
LEFPE5	effective channel length @ L=0.5μm	-	-	0.36	-	-	μm
NOIPE5	input referred noise @ VD=-5V, Id=-1μA, f=1Hz, L=10μm, W=10μm	-	-	20.2	-	-	μVμm/√(Hz)
STSPE5	subthreshold slope @ VD=-5V	-	-	10	-	-	decade/V
TC_VTXPE5	threshold voltage temperature coefficient @ L=10μm, W=10μm	-	-	1.1	-	-	mV/K
U0_PE5	effective mobility	-	-	102	-	-	cm ² /(Vs)
VTIPE5L	threshold voltage long channel @ VD=-0.1V, L=10μm, W=10μm	-0.94	-0.9	-0.86	-0.82	-0.78	V
VTIPE5S	threshold voltage short channel @ VD=-0.1V, L=0.5μm, W=10μm	-0.93	-0.885	-0.84	-0.795	-0.75	V
VTXPE5S	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5μm, W=10μm	-	-	-0.79	-	-	V
WEFPE5	effective channel width @ W=0.22μm	-	-	0.22	-	-	μm

Matching parameters

Name	Description	Typ	Unit
ABTPE5	pelgrom coefficient gain factor mismatch	0.78	%μm
AIDPE500	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	11.1	%μm
AIDPE502	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	5.03	%μm
AIDPE504	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	2.92	%μm
AIDPE506	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	2.02	%μm
AIDPE510	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	1.26	%μm
AIDPE520	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.7	%μm
AIDPE530	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.52	%μm
AIDPE550	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.39	%μm
AVTPE5	pelgrom coefficient threshold voltage mismatch	6.72	mVμm
DLTPE5	transistor delta length	0.14	μm
DWTPE5	transistor delta width	0	μm

3. Parameters → 3.2 MOS5 main module → 3.2.2 Device parameters → pe5, pe5_5 → Matching parameters

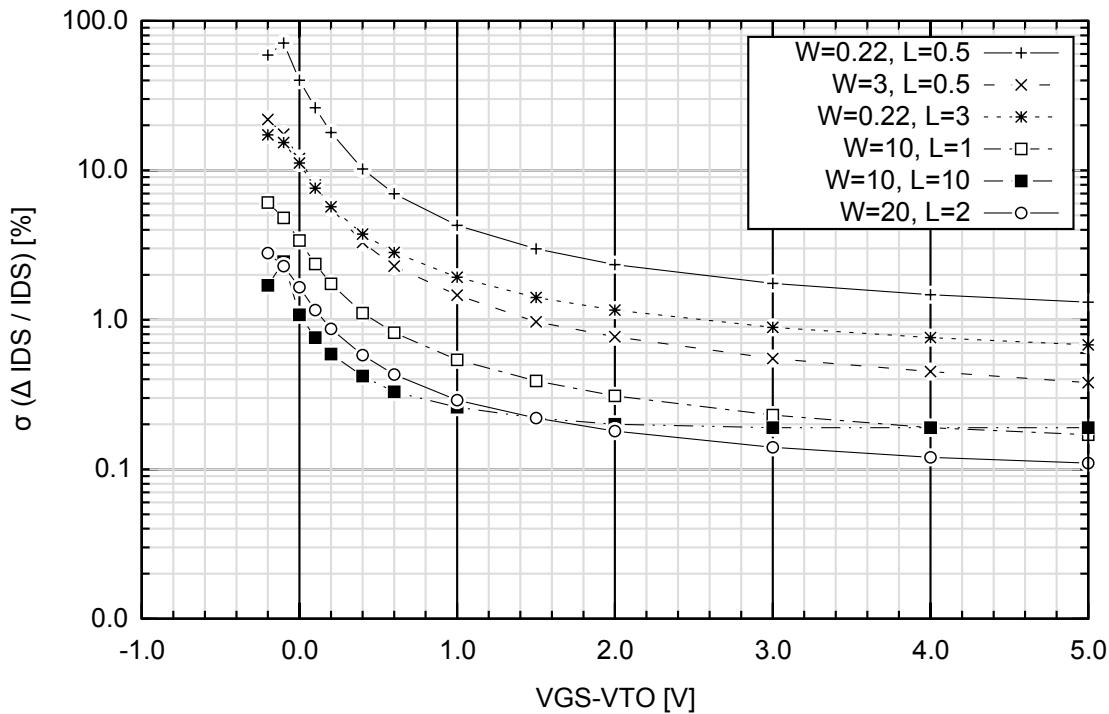


Figure 3.13 Device pe5: drain current matching vs. VGS-VTO (typical values, drawn W and L)

qpve5

emitter area: $2 \times 2 \mu\text{m}^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	Low	Typ	High	Unit
EVFPE5	early voltage forward @ $I_b=1\mu\text{A}$	100	-	-	V
HF_PE5	forward current gain @ $I_e=1\mu\text{A}$	-	1.95	-	-
VBEPE5	base-emitter voltage @ $I_e=1\mu\text{A}$	-	709	-	mV

Matching parameters

Name	Description	Typ	Unit
SIBPE51	standard deviation base current mismatch @ $I_c=100\text{nA}$	1.79	%
	Note: Preliminary		
SIBPE52	standard deviation base current mismatch @ $I_c=10\mu\text{A}$	1.65	%
	Note: Preliminary		
SICPE51	standard deviation collector current mismatch @ $I_c=100\text{nA}$	0.35	%
	Note: Preliminary		

⇒

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ qpve5→ Matching parameters

Name	Description	Typ	Unit
SICPE52	standard deviation collector current mismatch @ $I_c=10\mu A$ Note: Preliminary	0.35	%
SVBPE51	standard deviation base emitter voltage mismatch @ $I_e=100nA$ Note: Preliminary	0.3	mV
SVBPE52	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$ Note: Preliminary	0.23	mV

qpvf5

emitter area: $5 \times 5 \mu m^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
EVFPF5	early voltage forward @ $I_b=-1\mu A$	-	100	-	-	-	V
HF_PF5	forward current gain @ $I_e=1\mu A$	-	-	2.15	-	-	-
VBEFP5	base-emitter voltage @ $I_e=1\mu A$	659	664	669	674	679	mV

Matching parameters

Name	Description	Typ	Unit
SIBPF51	standard deviation base current mismatch @ $I_c=100nA$ Note: Preliminary	0.56	%
SIBPF52	standard deviation base current mismatch @ $I_c=10\mu A$ Note: Preliminary	0.55	%
SICPF51	standard deviation collector current mismatch @ $I_c=100nA$ Note: Preliminary	0.19	%
SICPF52	standard deviation collector current mismatch @ $I_c=10\mu A$ Note: Preliminary	0.21	%
SVBPF51	standard deviation base emitter voltage mismatch @ $I_e=100nA$ Note: Preliminary	0.27	mV
SVBPF52	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$ Note: Preliminary	0.16	mV

qpvg5

emitter area: $10 \times 10 \mu m^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ qpvg5→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-220	-200	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	Low	Typ	High	Unit
EVFPG5	early voltage forward @ Ib=-1µA	100	-	-	V
HF_PG5	forward current gain @ Ie=1µA	-	2.25	-	-
VBEPG5	base-emitter voltage @ Ie=1µA	-	636	-	mV

Matching parameters

Name	Description	Typ	Unit
SIBPG51	standard deviation base current mismatch @ Ic=100nA Note: Preliminary	0.34	%
SIBPG52	standard deviation base current mismatch @ Ic=10µA Note: Preliminary	0.26	%
SICPG51	standard deviation collector current mismatch @ Ic=100nA Note: Preliminary	0.12	%
SICPG52	standard deviation collector current mismatch @ Ic=10µA Note: Preliminary	0.15	%
SVBPG51	standard deviation base emitter voltage mismatch @ Ie=100nA Note: Preliminary	0.22	mV
SVBPG52	standard deviation base emitter voltage mismatch @ Ie=10µA Note: Preliminary	0.15	mV

rdn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Note: The node B (BULK) is: PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENN5SB	NDIFF5 silicide block edge resistance per terminal	-	-	12	-	-	Ωµm
RSRNN5	NDIFF5 sheet resistance (non salicided)	53	59	65	71	77	Ω/□
TC1NN5	NDIFF5 (non salicided) temperature coefficient 1	-	1.28	1.4	1.52	-	1e-03/K
TC1NN5RSE	NDIFF5 silicide block edge resistance temperature coefficient 1	-	-	0.12	-	-	1e-03/K
TC2NN5	NDIFF5 (non salicided) temperature coefficient 2	-	0.14	0.5	0.86	-	1e-06/K ²

⇒

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ rdn5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC2NN5RSE	NDIFF5 silicide block edge resistance temperature coefficient 2	-	-	-0.3	-	-	1e-06/K ²
WERNN5	NDIFF5 effective width @ W=0.42μm	-	0.34	0.4	0.46	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_NN5	pelgrom coefficient resistor mismatch	1.2	%μm
DWRNN5	resistor delta width	0.02	μm

rdp5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VBptub	-40°C to 175°C	-0.5	0	5.5	7	V
Vterm-bulk	-40°C to 175°C	-7	-5.5	0	0.5	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPP5SB	PDIFF5 silicide block edge resistance per terminal	-	-	35	-	-	Ωμm
RSRPP5	PDIFF5 sheet resistance (non salicided)	97	115	132	149	167	Ω/□
TC1PP5	PDIFF5 (non salicided) temperature coefficient 1	-	1.18	1.3	1.42	-	1e-03/K
TC1PP5RSE	PDIFF5 silicide block edge resistance temperature coefficient 1	-	-	-0.28	-	-	1e-03/K
TC2PP5	PDIFF5 (non salicided) temperature coefficient 2	-	0.11	0.5	0.89	-	1e-06/K ²
TC2PP5RSE	PDIFF5 silicide block edge resistance temperature coefficient 2	-	-	-3	-	-	1e-06/K ²
WERPP5	PDIFF5 effective width @ W=0.42μm	-	0.25	0.31	0.37	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_PP5	pelgrom coefficient resistor mismatch	1.3	%μm
DWRPP5	resistor delta width	0.11	μm

rnw5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

3. Parameters → 3.2 MOS5 main module → 3.2.2 Device parameters → rnw5 → Operating conditions

Note: The node B (BULK) is: PTUB_SUB

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRNW2	NWELL2 sheet resistance (STI terminated)	840	1020	1200	1380	1560	Ω/□
TC1NW2	NWELL2 temperature coefficient 1	-	2.7	3	3.3	-	1e-03/K
TC2NW2	NWELL2 temperature coefficient 2	-	7	8.8	10.6	-	1e-06/K ²
WERNW2	NWELL2 effective width @ W=2μm	-	1.51	1.66	1.81	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_NW2	pelgrom coefficient resistor mismatch	1.7	%μm
DWRNW2	resistor delta width	0.34	μm

rnp1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/μm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65μW/μm².

Process parameters

Name	Description	Low	Typ	High	Unit
RSENP1SB	N+ poly 1 silicide block edge resistance per terminal (2 terminals)	-	65	-	Ωμm
RSRNP1	N+ poly 1 sheet resistance (2 terminals)	225	315	405	Ω/□
TC1NP1	N+ poly 1 temperature coefficient 1 (2 terminals)	-1.73	-1.47	-1.22	1e-03/K
TC1NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (2 terminals)	-	-1.4	-	1e-03/K
TC2NP1	N+ poly 1 temperature coefficient 2 (2 terminals)	1.85	2.75	3.65	1e-06/K ²
TC2NP1RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (2 terminals)	-	0.3	-	1e-06/K ²
WERNP1	N+ poly 1 effective width (2 terminals) @ W=0.42μm	0.285	0.36	0.435	μm

Matching parameters

Name	Description	Typ	Unit
AR_NP1	pelgrom coefficient resistor mismatch	4.9	%μm
DWRNP1	resistor delta width	0.06	μm

rnp1_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ rnp1_3→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65µW/µm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSENP1_3SB	N+ poly 1 silicide block edge resistance per terminal (underlying NWELL/PWELL2, 3 terminals)	-	-	65	-	-	Ωµm
RSRNP1_3	N+ poly 1 sheet resistance (underlying NWELL/PWELL2, 3 terminals)	220	280	340	400	460	Ω/□
TC1NP1_3	N+ poly 1 temperature coefficient 1 (underlying NWELL/PWELL2, 3 terminals)	-	-1.71	-1.54	-1.37	-	1e-03/K
TC1NP1_3RSE	N+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying NWELL/PWELL2, 3 terminals)	-	-	-1.4	-	-	1e-03/K
TC2NP1_3	N+ poly 1 temperature coefficient 2 (underlying NWELL/PWELL2, 3 terminals)	-	2.4	3	3.6	-	1e-06/K ²
TC2NP1_3RSE	N+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying NWELL/PWELL2, 3 terminals)	-	-	0.3	-	-	1e-06/K ²
VCBNP1_3	N+ poly 1 bulk voltage coefficient (underlying NWELL/PWELL2, 3 terminals)	-	-	0.08	-	-	1e-03/V
WERNP1_3	N+ poly 1 effective width (underlying NWELL/PWELL2, 3 terminals) @ W=0.42µm	-	0.31	0.37	0.43	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_NP1	pelgrom coefficient resistor mismatch	4.9	%µm
DWRNP1_3	resistor delta width	0.05	µm

rpp1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65µW/µm².

3. Parameters → 3.2 MOS5 main module → 3.2.2 Device parameters → rpp1 → Process parameters

Process parameters

Name	Description	Low	Typ	High	Unit
RSEPP1SB	P+ poly 1 silicide block edge resistance per terminal (2 terminals)	-	70	-	Ωµm
RSRPP1	P+ poly 1 sheet resistance (2 terminals)	230	275	320	Ω/□
TC1PP1	P+ poly 1 temperature coefficient 1 (2 terminals)	-0.17	-0.08	0.01	1e-03/K
TC1PP1RSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (2 terminals)	-	-1.2	-	1e-03/K
TC2PP1	P+ poly 1 temperature coefficient 2 (2 terminals)	0.3	0.75	1.2	1e-06/K ²
TC2PP1RSE	P+ poly 1 silicide block edge resistance temperature coefficient 2 (2 terminals)	-	0.2	-	1e-06/K ²
WERPP1	P+ poly 1 effective width (2 terminals) @ W=0.42µm	0.305	0.365	0.425	µm

Matching parameters

Name	Description	Typ	Unit
AR_PP1	pelgrom coefficient resistor mismatch	1.7	%µm
DWRPP1	resistor delta width	0.055	µm

rpp1_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65µW/µm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPP1PWSB	P+ poly 1 silicide block edge resistance per terminal (underlying PWELL, 3 terminals)	-	-	70	-	-	Ωµm
RSRPP1PW	P+ poly 1 sheet resistance (underlying PWELL, 3 terminals)	225	255	285	315	345	Ω/□
TC1PP1PW	P+ poly 1 temperature coefficient 1 (underlying PWELL, 3 terminals)	-	-0.16	-0.1	-0.04	-	1e-03/K
TC1PP1PWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying PWELL, 3 terminals)	-	-	-1.2	-	-	1e-03/K
TC2PP1PW	P+ poly 1 temperature coefficient 2 (underlying PWELL, 3 terminals)	-	0.55	0.85	1.15	-	1e-06/K ²
TC2PP1PWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying PWELL, 3 terminals)	-	-	0.2	-	-	1e-06/K ²
VCPPP1PW	P+ poly 1 bulk voltage coefficient (underlying PWELL, 3 terminals)	-	-	-0.05	-	-	1e-03/V
WERPP1PW	P+ poly 1 effective width (underlying PWELL, 3 terminals) @ W=0.42µm	-	0.325	0.37	0.415	-	µm

3. Parameters → 3.2 MOS5 main module → 3.2.2 Device parameters → rpp1_3 → Matching parameters

Matching parameters

Name	Description	Typ	Unit
AR_PP1	pelgrom coefficient resistor mismatch	1.7	%μm
DWRPP1PW	resistor delta width	0.05	μm

rpp1nw_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.45	-	mA/μm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65μW/μm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSEPP1NWSB	P+ poly 1 silicide block edge resistance per terminal (underlying NWELL, 3 terminals)	-	-	70	-	-	Ωμm
RSRPP1NW	P+ poly 1 sheet resistance (underlying NWELL, 3 terminals)	210	240	270	300	330	Ω/□
TC1PP1NW	P+ poly 1 temperature coefficient 1 (underlying NWELL, 3 terminals)	-	-0.13	-0.07	-0.01	-	1e-03/K
TC1PP1NWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 1 (underlying NWELL, 3 terminals)	-	-	-1.2	-	-	1e-03/K
TC2PP1NW	P+ poly 1 temperature coefficient 2 (underlying NWELL, 3 terminals)	-	0.4	0.7	1	-	1e-06/K ²
TC2PP1NWRSE	P+ poly 1 silicide block edge resistance temperature coefficient 2 (underlying NWELL, 3 terminals)	-	-	0.2	-	-	1e-06/K ²
VCBPP1NW	P+ poly 1 bulk voltage coefficient (underlying NWELL, 3 terminals)	-	-	-0.05	-	-	1e-03/V
WERPP1NW	P+ poly 1 effective width (underlying NWELL, 3 terminals) @ W=0.42μm	-	0.315	0.36	0.405	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_PP1	pelgrom coefficient resistor mismatch	1.7	%μm
DWRPP1NW	resistor delta width	0.06	μm

rpp1s, rpp1s_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

3. Parameters → 3.2 MOS5 main module → 3.2.2 Device parameters → rpp1s, rpp1s_3 → Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRPP1S	P+ poly 1 sheet resistance (salicided)	5.2	6.3	7.5	8.7	9.8	Ω/□
TC1PP1S	P+ poly 1 temperature coefficient 1	-	2.74	3.1	3.46	-	1e-03/K
TC2PP1S	P+ poly 1 temperature coefficient 2	-	-1.12	0.08	1.28	-	1e-06/K ²
WERPP1S	P+ poly 1 effective width (salicided) @ W=0.18μm	-	0.13	0.16	0.19	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_PP1S	pelgrom coefficient resistor mismatch	1.65	%μm
DWRPP1S	resistor delta width	0.02	μm

rm1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M1	metal 1 sheet resistance	61	69	77	85	93	mΩ/□
TC1_MET	metal 1 / metal 2 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_MET	metal 1 / metal 2 temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_M1B	metal 1 effective width @ W=0.23μm	-	0.18	0.21	0.24	-	μm

rm2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M2	metal 2 sheet resistance	58	66	74	82	90	mΩ/□
TC1_MET	metal 1 / metal 2 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_MET	metal 1 / metal 2 temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_M2	metal 2 effective width @ W=0.28μm	-	0.2	0.24	0.28	-	μm

mosvc5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB ⁽¹⁾	-40°C to 175°C	-7	-1.98	5.5	7	V

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ mosvc5→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VBsub	-40°C to 175°C	-0.5	0	5.5	7	V

Note 1 VGB Min operating condition means a model limit. Between VGB Min and VGB Abs.Min, the device will be very slow in terms of charge carriers because it works in deep depletion region. Only thermally generated charge carriers are available which lead to very large time constants at low temperatures. The C-V-curve will show memory effects when used between VGB=-1.98V...-7V. This effect can not be modeled.

Process parameters

Name	Description	Typ	Unit
CNV_MVC5	varactor capacitance at negative voltage @ Vterm=-1.8V, f=100kHz	0.9	fF/μm ²
CPV_MVC5	varactor capacitance at positive voltage @ Vterm=5V, f=100kHz	2.5	fF/μm ²
TUR_MVC5	tuning range @ Vlow=-1.8V, Vhigh=5V, f=100kHz	64	%

csf2p

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFP2	csf2p breakdown voltage @ Ibr=1μA	15	-	-	V
CA_SFP2_B	csf2p capacitance per cell @ Vbias=0V, L=10.8μm, W=4.48μm	22.8	25.2	27.6	fF
IL_SFP2	csf2p leakage current @ VL=5.5V, L=10.8μm, W=4.48μm	-	-	50	fA/cell
Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.					
TC1_SFP2	csf2p temperature coefficient 1 @ Tnom=27°C	-	0.25	-	1e-03/K
TC2_SFP2	csf2p temperature coefficient 2 @ Tnom=27°C	-	-1.2	-	1e-06/K ²
VC1_SFP2	csf2p capacitor voltage coefficient 1	-	81	-	ppm/V
VC2_SFP2	csf2p capacitor voltage coefficient 2	-	100	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_CSFP	pelgrom coefficient capacitor mismatch @ L=10.8μm, W=4.48μm	0.5	%μm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

dn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

3. Parameters → 3.2 MOS5 main module → 3.2.2 Device parameters → dn5 → Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNPW2	breakdown voltage NDIFF / PWELL2 @ Irev=1µA, L=70µm, W=40µm	8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CJANPW2	area junction capacitance	-	-	1.02	-	-	fF/µm ²
CJPNPW2	sidewall junction capacitance	-	-	0.21	-	-	fF/µm
ILA NPW2	diode area leakage current @ Vrev=5.5V, T=27°C	-	-	0.016	-	-	fA/µm ²
ILA NPW2HT	diode area leakage current @ Vrev=5.5V, T=175°C	-	-	0.4	-	-	pA/µm ²
ILPNPW2	diode perimeter leakage current @ Vrev=5.5V, T=27°C	-	-	1.44	-	-	fA/µm
ILPNPW2HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	-	-	1.41	-	-	pA/µm
MJANPW2	area grading coefficient	-	-	0.34	-	-	-
MJPNPW2	sidewall grading coefficient	-	-	0.05	-	-	-
PBANPW2	area junction potential	-	-	0.82	-	-	V
PBPNPW2	sidewall junction potential	-	-	1.2	-	-	V

dnn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	Typ	Unit
CJANN5	area junction capacitance	0.18	fF/µm ²
CJPNN5	sidewall junction capacitance	0.32	fF/µm
ILANN5	diode area leakage current @ Vrev=5.5V, T=27°C	0.012	fA/µm ²
ILANN5HT	diode area leakage current @ Vrev=5.5V, T=175°C	0.39	pA/µm ²
ILPNN5	diode perimeter leakage current @ Vrev=5.5V, T=27°C	0.31	fA/µm
ILPNN5HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	1.18	pA/µm
MJANN5	area grading coefficient	0.36	-
MJPNN5	sidewall grading coefficient	0.07	-
PBANN5	area junction potential	1.2	V
PBPNNN5	sidewall junction potential	0.46	V

Note: dnn5 is also used as parasitic diode p_dnn5.

dp5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V
Vcathode-Vpsub	-40°C to 175°C	-0.5	0	5.5	7	V

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ dp5→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VPT-HW ¹	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJPNW2	breakdown voltage PDIFF / NWELL2 @ Irev=1µA, L=70µm, W=40µm	7.5	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CJAPNW2	area junction capacitance	-	-	1.29	-	-	fF/µm ²
CJPPNW2	sidewall junction capacitance	-	-	0.22	-	-	fF/µm
ILA PNW2	diode area leakage current @ Vrev=5.5V, T=27°C	-	-	0.13	-	-	fA/µm ²
ILA PNW2HT	diode area leakage current @ Vrev=5.5V, T=175°C	-	-	0.9	-	-	pA/µm ²
ILPPNW2	diode perimeter leakage current @ Vrev=5.5V, T=27°C	-	-	15.2	-	-	fA/µm
ILPPNW2HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	-	-	2.82	-	-	pA/µm
MJA PNW2	area grading coefficient	-	-	0.44	-	-	-
MJPPNW2	sidewall grading coefficient	-	-	0.05	-	-	-
PBA PNW2	area junction potential	-	-	1.04	-	-	V
PBPPNW2	sidewall junction potential	-	-	0.46	-	-	V

dnw5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	0	0.5	V
VA-HW ¹	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVJNW2	breakdown voltage NWELL2 / PWELL2 @ Irev=1µA, L=70µm, W=40µm	9	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CJANW2	area junction capacitance	-	-	0.21	-	-	fF/µm ²
CJPNW2	sidewall junction capacitance	-	-	0.47	-	-	fF/µm
ILA NW2	diode area leakage current @ Vrev=5.5V, T=27°C	-	-	0.005	-	-	fA/µm ²
ILA NW2HT	diode area leakage current @ Vrev=5.5V, T=175°C	-	-	1.11	-	-	pA/µm ²
ILPNW2	diode perimeter leakage current @ Vrev=5.5V, T=27°C	-	-	0.1	-	-	fA/µm
ILPNW2HT	diode perimeter leakage current @ Vrev=5.5V, T=175°C	-	-	0.18	-	-	pA/µm

3. Parameters → 3.2 MOS5 main module→ 3.2.2 Device parameters→ dnw5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
MJANW2	area grading coefficient	-	-	0.3	-	-	-
MJPNW2	sidewall grading coefficient	-	-	0.29	-	-	-
PBANW2	area junction potential	-	-	0.46	-	-	V
PBPNW2	sidewall junction potential	-	-	0.51	-	-	V

pfuse

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm1-Vterm2 ⁽¹⁾	-40°C to 175°C	-0.2	-0.1	0.1	0.2	V
Vterm1-Vterm2 ⁽²⁾	-40°C to 175°C	-5	-3.6	3.6	5	V

Note 1 unprogrammed state

Note 2 programmed state

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RP_FUSE	programmed fuse resistance @ Vbias=3.3V	-	100	-	-	-	kΩ
Note: The values of this parameter do not reflect the statistics of the process.							
RU_FUSE	unprogrammed fuse resistance @ Isupply=50µA	10	25	40	55	70	Ω

Note: For the primitive device pfuse, the programming conditions and further information are available in the "[Application Note – EasyFuse](#)" on "my X-FAB."

3. Parameters → 3.3 MET3 module

3.3 MET3 module

3.3.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMD2	metal 2 / metal 3 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMD2	metal 3 – metal 2 dielectric thickness	765	850	935	nm
TH_M3	metal 3 thickness	505	565	625	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M3	metal 3 sheet resistance	58	66	74	82	90	mΩ/□
RVI_V2	VIA2 resistance	-	3	4.5	6.75	9	Ω/via
TC1_V234	VIA2,3,4 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2_V234	VIA2,3,4 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K ²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances.

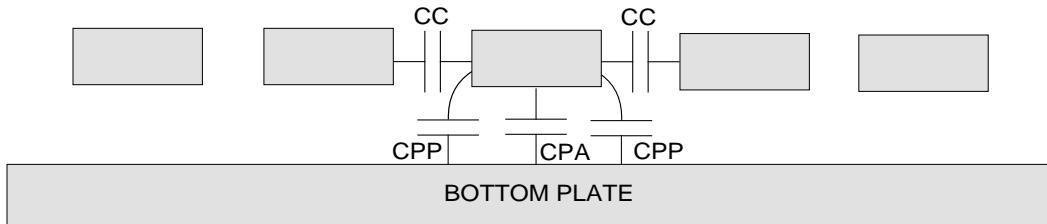


Figure 3.14 Parasitic capacitance structure

Name	Description	Typ	Unit
CC_M3M3	coupling capacitance metal 3 – metal 3	98	aF/µm
CPAM3DIFF	metal 3 – active area capacitance	9.2	aF/µm ²
CPAM3M1	metal 3 – metal 1 area capacitance	15.5	aF/µm ²
CPAM3M2	metal 3 – metal 2 area capacitance	41.5	aF/µm ²
CPAM3P1	metal 3 – poly 1 area capacitance	9.5	aF/µm ²
CPAM3STI	metal 3 – field area (STI) area capacitance	8.3	aF/µm ²
CPPM3DIFF	metal 3 – active perimeter capacitance	7.2	aF/µm
CPPM3M1	metal 3 – metal 1 perimeter capacitance	5	aF/µm
CPPM3M2	metal 3 – metal 2 perimeter capacitance	8.3	aF/µm
CPPM3P1	metal 3 – poly 1 perimeter capacitance	4.1	aF/µm
CPPM3STI	metal 3 – field area (STI) perimeter capacitance	7	aF/µm

3. Parameters → 3.3 MET3 module → 3.3.1 Device independent p... → Physical layer opera...

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC ⁽¹⁾⁽²⁾	Metal 3	-40°C to 175°C	-	-	1	20	mA/µm
JMax_N_DC ⁽³⁾⁽²⁾	Metal 3	-40°C to 175°C	-	-	0.5	20	mA/µm
JMax_VI_DC ⁽²⁾	Via 2	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_AC ⁽¹⁾⁽⁴⁾	Metal 3	-40°C to 175°C	-	-	4.5	20	mA/µm
JMax_N_AC ⁽³⁾⁽⁴⁾	Metal 3	-40°C to 175°C	-	-	2.2	20	mA/µm
JMax_VI_AC ⁽⁴⁾	Via 2	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4 ⁽⁵⁾⁽⁶⁾	Metal 3	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁵⁾⁽⁶⁾	Via 2	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁵⁾	Metal 3	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁵⁾	Via 2	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁵⁾	Metal 3	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁵⁾	Via 2	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5 ⁽⁵⁾⁽⁶⁾	Metal 3	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁵⁾⁽⁶⁾	Via 2	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁵⁾	Metal 3	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁵⁾	Via 2	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁵⁾	Metal 3	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁵⁾	Via 2	125°C to 175°C	-	0.1	-	-	-
E ⁽⁹⁾	Metal 3	-40°C to 175°C	-	-	250	-	V/µm

Note 1 track width > 0.44µm.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 track width ≤ 0.44µm.

Note 4 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 5 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 6 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 125°C

Note 9 lateral electric field between Metal 3 track

3.3.2 Device parameters

rm3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M3	metal 3 sheet resistance	58	66	74	82	90	mΩ/□

3. Parameters → 3.3 MET3 module→ 3.3.2 Device parameters→ rm3→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC1_M3	metal 3 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_M3	metal 3 temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_M3	metal 3 effective width @ W=0.28µm	-	0.2	0.24	0.28	-	µm

csandwt3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V
Vterm1-Vterm2	-40°C to 175°C	-220	-200	200	220	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
CAA_SANDW3B	POLY1 / metal1/ metal2/ metal3 sandwich area capacitance @ Vbias=0V	0.125	0.155	0.185	fF/µm ²
CAP_SANDW3	POLY1 / metal1/ metal2/ metal3 sandwich perimeter capacitance	-	0.055	-	fF/µm

Matching parameters

Name	Description	Typ	Unit
AC_SANDW3	pelgrom coefficient capacitor mismatch	0.65	%µm

Note: Valid for interleaved structures. Side by side structures may exhibit greater mismatch!

cif3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-110	-100	100	110	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIF3	cif3 breakdown voltage @ Ibr=1µA	140	-	-	V
CA_CIF3	cif3 capacitance per cell @ Vbias=0V, L=25µm, W=7.04µm	34.6	39.3	44	fF
IL_CIF3	cif3 leakage current @ VL=100V	-	-	20	fA/cell
TC1_CIF3	cif3 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K
VC1_CIF3	cif3 capacitor voltage coefficient 1	-	0.35	-	ppm/V
VC2_CIF3	cif3 capacitor voltage coefficient 2	-	-0.19	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_CIF	pelgrom coefficient capacitor mismatch @ L=25µm, W=7.04µm	0.95	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

3. Parameters → 3.3 MET3 module→ 3.3.2 Device parameters→ csf3p→ Operating conditions

csf3p

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFP3	csf3p breakdown voltage @ Ibr=1µA	15	-	-	V
CA_SFP3_B	csf3p capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	33.2	36.8	40.4	fF
IL_SFP3	csf3p leakage current @ VL=5.5V, L=10.8µm, W=4.48µm	-	-	50	fA/cell
	Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.				
TC1_SFP3	csf3p temperature coefficient 1 @ Tnom=27°C	-	0.155	-	1e-03/K
TC2_SFP3	csf3p temperature coefficient 2 @ Tnom=27°C	-	-0.83	-	1e-06/K ²
VC1_SFP3	csf3p capacitor voltage coefficient 1	-	80	-	ppm/V
VC2_SFP3	csf3p capacitor voltage coefficient 2	-	68	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_CSFP	pelgrom coefficient capacitor mismatch @ L=10.8µm, W=4.48µm	0.5	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

cif3a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-33	-30	30	33	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIF3A	cif3a breakdown voltage @ Ibr=1µA	50	-	-	V
CA_CIF3A	cif3a capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	20.9	23.7	26.5	fF
IL_CIF3A	cif3a leakage current @ VL=30V, L=10.8µm, W=4.48µm	-	-	30	fA/cell
TC1_CIF3A	cif3a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

3. Parameters → 3.3 MET3 module→ 3.3.2 Device parameters→ cif3a→ Matching parameters

Matching parameters

Name	Description	Typ	Unit
AC_CIFA	pelgrom coefficient capacitor mismatch @ L=10.8µm, W=4.48µm	0.5	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csf3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF3	csf3 breakdown voltage @ Ibr=1µA	35	-	-	V
CA_SF3_B	csf3 capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	30.2	32.9	35.6	fF
IL_SF3	csf3 leakage current @ VL=10V, L=10.8µm, W=4.48µm	-	-	30	fA/cell
Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.					
TC1_SF3	csf3 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
AC_CSF	pelgrom coefficient capacitor mismatch @ L=10.8µm, W=4.48µm	0.5	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csf3a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-66	-60	60	66	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF3A	csf3a breakdown voltage @ Ibr=1µA	70	-	-	V
CA_SF3A_B	csf3a capacitance per cell @ Vbias=0V, L=11.1µm, W=5.76µm	21.6	23.9	26.2	fF
IL_SF3A	csf3a leakage current @ VL=60V, L=11.1µm, W=5.76µm	-	-	35	fA/cell
Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.					
TC1_SF3A	csf3a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

3. Parameters → 3.3 MET3 module→ 3.3.2 Device parameters→ csf3a→ Matching parameters

Matching parameters

Name	Description	Typ	Unit
AC_CSFA	pelgrom coefficient capacitor mismatch @ L=11.1µm, W=5.76µm	0.6	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

3. Parameters → 3.4 MET4 module

3.4 MET4 module

3.4.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMD3	metal 3 / metal 4 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMD3	metal 4 - metal 3 dielectric thickness	765	850	935	nm
TH_M4	metal 4 thickness	505	565	625	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M4	metal 4 sheet resistance	58	66	74	82	90	mΩ/□
RVI_V3	VIA3 resistance	-	3	4.5	6.75	9	Ω/via
TC1_V234	VIA2,3,4 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2_V234	VIA2,3,4 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances.

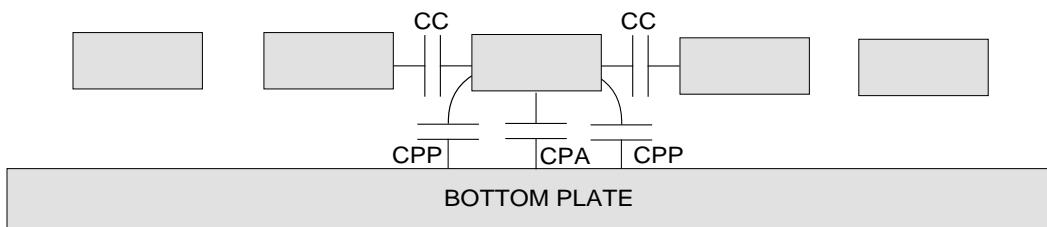


Figure 3.15 Parasitic capacitance structure

Name	Description	Typ	Unit
CC_M4M4	coupling capacitance metal 4 – metal 4	99	aF/µm
CPAM4DIFF	metal 4 – active area capacitance	6.6	aF/µm²
CPAM4M1	metal 4 – metal 1 area capacitance	9.5	aF/µm²
CPAM4M2	metal 4 – metal 2 area capacitance	15.5	aF/µm²
CPAM4M3	metal 4 – metal 3 area capacitance	41.5	aF/µm²
CPAM4P1	metal 4 – poly 1 area capacitance	6.8	aF/µm²
CPAM4STI	metal 4 – field area (STI) area capacitance	6.2	aF/µm²
CPPM4DIFF	metal 4 – active perimeter capacitance	6.8	aF/µm
CPPM4M1	metal 4 – metal 1 perimeter capacitance	4.1	aF/µm
CPPM4M2	metal 4 – metal 2 perimeter capacitance	5	aF/µm
CPPM4M3	metal 4 – metal 3 perimeter capacitance	8.3	aF/µm
CPPM4P1	metal 4 – poly 1 perimeter capacitance	3.7	aF/µm
CPPM4STI	metal 4 – field area (STI) perimeter capacitance	6.7	aF/µm

3. Parameters → 3.4 MET4 module → 3.4.1 Device independent p... → Physical layer opera...

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC ⁽¹⁾⁽²⁾	Metal 4	-40°C to 175°C	-	-	1	20	mA/μm
JMax_N_DC ⁽³⁾⁽²⁾	Metal 4	-40°C to 175°C	-	-	0.5	20	mA/μm
JMax_VI_DC ⁽²⁾	Via 3	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_AC ⁽¹⁾⁽⁴⁾	Metal 4	-40°C to 175°C	-	-	4.5	20	mA/μm
JMax_N_AC ⁽³⁾⁽⁴⁾	Metal 4	-40°C to 175°C	-	-	2.2	20	mA/μm
JMax_VI_AC ⁽⁴⁾	Via 3	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4 ⁽⁵⁾⁽⁶⁾	Metal 4	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁵⁾⁽⁶⁾	Via 3	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁵⁾	Metal 4	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁵⁾	Via 3	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁵⁾	Metal 4	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁵⁾	Via 3	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5 ⁽⁵⁾⁽⁶⁾	Metal 4	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁵⁾⁽⁶⁾	Via 3	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁵⁾	Metal 4	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁵⁾	Via 3	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁵⁾	Metal 4	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁵⁾	Via 3	125°C to 175°C	-	0.1	-	-	-
E ⁽⁹⁾	Metal 4	-40°C to 175°C	-	-	250	-	V/μm

Note 1 track width > 0.44μm.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 track width ≤ 0.44μm.

Note 4 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 5 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 6 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 125°C

Note 9 lateral electric field between Metal 4 track

3.4.2 Device parameters

rm4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M4	metal 4 sheet resistance	58	66	74	82	90	mΩ/□

3. Parameters → 3.4 MET4 module→ 3.4.2 Device parameters→ rm4→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC1_M4	metal 4 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_M4	metal 4 temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_M4	metal 4 effective width @ W=0.28µm	-	0.2	0.24	0.28	-	µm

csandwt4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V
Vterm1-Vterm2	-40°C to 175°C	-220	-200	200	220	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
CAA_SANDW4B	POLY1 / metal1/ metal2/ metal3/ metal4 sandwich area capacitance @ Vbias=0V	0.16	0.2	0.24	fF/µm ²
CAP_SANDW4	POLY1 / metal1/ metal2/ metal3/ metal4 sandwich perimeter capacitance	-	0.085	-	fF/µm

Matching parameters

Name	Description	Typ	Unit
AC_SANDW4	pelgrom coefficient capacitor mismatch	0.46	%µm

Note: Valid for interleaved structures. Side by side structures may exhibit greater mismatch!

cif4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-110	-100	100	110	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIF4	cif4 breakdown voltage @ Ibr=1µA	140	-	-	V
CA_CIF4	cif4 capacitance per cell @ Vbias=0V, L=25µm, W=7.04µm	46.9	53.3	59.7	fF
IL_CIF4	cif4 leakage current @ VL=100V	-	-	20	fA/cell
TC1_CIF4	cif4 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K
VC1_CIF4	cif4 capacitor voltage coefficient 1	-	0.35	-	ppm/V
VC2_CIF4	cif4 capacitor voltage coefficient 2	-	-0.19	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_CIF	pelgrom coefficient capacitor mismatch @ L=25µm, W=7.04µm	0.95	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

3. Parameters → 3.4 MET4 module→ 3.4.2 Device parameters→ cif4a→ Operating conditions

cif4a**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-33	-30	30	33	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIF4A	cif4a breakdown voltage @ lbr=1µA	50	-	-	V
CA_CIF4A	cif4a capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	27.8	31.6	35.4	fF
IL_CIF4A	cif4a leakage current @ VL=30V, L=10.8µm, W=4.48µm	-	-	30	fA/cell
TC1_CIF4A	cif4a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
AC_CIFA	pelgrom coefficient capacitor mismatch @ L=10.8µm, W=4.48µm	0.5	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csf4**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF4	csf4 breakdown voltage @ lbr=1µA	35	-	-	V
CA_SF4_B	csf4 capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	41.3	45	48.7	fF
IL_SF4	csf4 leakage current @ VL=10V, L=10.8µm, W=4.48µm	-	-	30	fA/cell
TC1_SF4	csf4 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
AC_CSF	pelgrom coefficient capacitor mismatch @ L=10.8µm, W=4.48µm	0.5	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csf4a**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V

3. Parameters → 3.4 MET4 module→ 3.4.2 Device parameters→ csf4a→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm1-Vterm2	-40°C to 175°C	-66	-60	60	66	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF4A	csf4a breakdown voltage @ Ibr=1µA	70	-	-	V
CA_SF4A_B	csf4a capacitance per cell @ Vbias=0V, L=11.1µm, W=5.76µm	30.2	32.9	35.6	fF
IL_SF4A	csf4a leakage current @ VL=60V, L=11.1µm, W=5.76µm	-	-	35	fA/cell
TC1_SF4A	csf4a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
	pelgrom coefficient capacitor mismatch @ L=11.1µm, W=5.76µm	0.6	%µm
AC_CSFA	Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."		

3. Parameters → 3.5 MET5 module

3.5 MET5 module

3.5.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMD4	metal 4 / metal 5 equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMD4	metal 5 - metal 4 dielectric thickness	765	850	935	nm
TH_M5	metal 5 thickness	505	565	625	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M5	metal 5 sheet resistance	58	66	74	82	90	mΩ/□
RVI_V4	VIA4 resistance	-	3	4.5	6.75	9	Ω/via
TC1_V234	VIA2,3,4 resistance temperature coefficient 1	-	-	1.1	-	-	1e-03/K
TC2_M5	metal 5 temperature coefficient 2	-	-	0	-	-	1e-06/K ²
TC2_V234	VIA2,3,4 resistance temperature coefficient 2	-	-	0	-	-	1e-06/K ²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances.

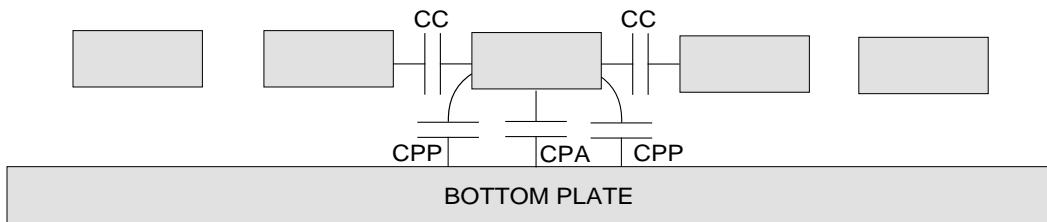


Figure 3.16 Parasitic capacitance structure

Name	Description	Typ	Unit
CC_M5M5	coupling capacitance metal 5 – metal 5	99	aF/µm
CPAM5DIFF	metal 5 – active area capacitance	5.2	aF/µm ²
CPAM5M1	metal 5 – metal 1 area capacitance	6.8	aF/µm ²
CPAM5M2	metal 5 – metal 2 area capacitance	9.5	aF/µm ²
CPAM5M3	metal 5 – metal 3 area capacitance	15.5	aF/µm ²
CPAM5M4	metal 5 – metal 4 area capacitance	41.5	aF/µm ²
CPAM5P1	metal 5 – poly 1 area capacitance	5.3	aF/µm ²
CPAM5STI	metal 5 – field area (STI) area capacitance	4.9	aF/µm ²
CPPM5DIFF	metal 5 – active perimeter capacitance	6.6	aF/µm
CPPM5M1	metal 5 – metal 1 perimeter capacitance	3.7	aF/µm
CPPM5M2	metal 5 – metal 2 perimeter capacitance	4.1	aF/µm
CPPM5M3	metal 5 – metal 3 perimeter capacitance	5	aF/µm
CPPM5M4	metal 5 – metal 4 perimeter capacitance	8.3	aF/µm

3. Parameters → 3.5 MET5 module → 3.5.1 Device independent p... → Parasitic capacitanc...

Name	Description	Typ	Unit
CPPM5P1	metal 5 – poly 1 perimeter capacitance	3.5	aF/ μ m
CPPM5STI	metal 5 – field area (STI) perimeter capacitance	6.5	aF/ μ m

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC ⁽¹⁾⁽²⁾	Metal 5	-40°C to 175°C	-	-	1	20	mA/ μ m
JMax_N_DC ⁽³⁾⁽²⁾	Metal 5	-40°C to 175°C	-	-	0.5	20	mA/ μ m
JMax_VI_DC ⁽²⁾	Via 4	-40°C to 175°C	-	-	0.28	20	mA/via
JMax_AC ⁽¹⁾⁽⁴⁾	Metal 5	-40°C to 175°C	-	-	4.5	20	mA/ μ m
JMax_N_AC ⁽³⁾⁽⁴⁾	Metal 5	-40°C to 175°C	-	-	2.2	20	mA/ μ m
JMax_VI_AC ⁽⁴⁾	Via 4	-40°C to 175°C	-	-	1.3	20	mA/via
T_Factor_1e4 ⁽⁵⁾⁽⁶⁾	Metal 5	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁵⁾⁽⁶⁾	Via 4	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁵⁾	Metal 5	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁵⁾	Via 4	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁵⁾	Metal 5	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4 ⁽⁸⁾⁽⁵⁾	Via 4	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5 ⁽⁵⁾⁽⁶⁾	Metal 5	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁵⁾⁽⁶⁾	Via 4	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁵⁾	Metal 5	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁵⁾	Via 4	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁵⁾	Metal 5	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁸⁾⁽⁵⁾	Via 4	125°C to 175°C	-	0.1	-	-	-
E ⁽⁹⁾	Metal 5	-40°C to 175°C	-	-	250	-	V/ μ m

Note 1 track width > 0.44 μ m.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 track width ≤ 0.44 μ m.

Note 4 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 5 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 6 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 8 The temperature correction factor is interpolated between given values for temperatures above 125°C

Note 9 lateral electric field between Metal 5 track

3.5.2 Device parameters

rm5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V

3. Parameters → 3.5 MET5 module→ 3.5.2 Device parameters→ rm5→ Operating conditions

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_M5	metal 5 sheet resistance	58	66	74	82	90	mΩ/□
TC1_M5	metal 5 temperature coefficient 1	-	-	3.4	-	-	1e-03/K
TC2_M5	metal 5 temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_M5	metal 5 effective width @ W=0.28μm	-	0.2	0.24	0.28	-	μm

csandwt5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V
Vterm1-Vterm2	-40°C to 175°C	-220	-200	200	220	V

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Process parameters

Name	Description	Low	Typ	High	Unit
CAA_SANDW5B	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 sandwich area capacitance @ Vbias=0V	0.2	0.25	0.3	fF/μm ²
CAP_SANDW5	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 sandwich perimeter capacitance	-	0.145	-	fF/μm

Matching parameters

Name	Description	Typ	Unit
AC_SANDW5	pelgrom coefficient capacitor mismatch	0.39	%μm

Note: Valid for interleaved structures. Side by side structures may exhibit greater mismatch!

cif5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-110	-100	100	110	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIF5	cif5 breakdown voltage @ Ibr=1μA	140	-	-	V
CA_CIF5	cif5 capacitance per cell @ Vbias=0V, L=25μm, W=7.04μm	59.2	67.3	75.4	fF
IL_CIF5	cif5 leakage current @ VL=100V	-	-	20	fA/cell
TC1_CIF5	cif5 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K
VC1_CIF5	cif5 capacitor voltage coefficient 1	-	0.35	-	ppm/V
VC2_CIF5	cif5 capacitor voltage coefficient 2	-	-0.19	-	ppm/V ²

3. Parameters → 3.5 MET5 module→ 3.5.2 Device parameters→ cif5→ Matching parameters

Matching parameters

Name	Description	Typ	Unit
AC_CIF	pelgrom coefficient capacitor mismatch @ L=25µm, W=7.04µm	0.95	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

cif5a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-33	-30	30	33	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIF5A	cif5a breakdown voltage @ Ibr=1µA	50	-	-	V
CA_CIF5A	cif5a capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	34.8	39.5	44.2	fF
IL_CIF5A	cif5a leakage current @ VL=30V, L=10.8µm, W=4.48µm	-	-	30	fA/cell
TC1_CIF5A	cif5a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
AC_CIFA	pelgrom coefficient capacitor mismatch @ L=10.8µm, W=4.48µm	0.5	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csf5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF5	csf5 breakdown voltage @ Ibr=1µA	35	-	-	V
CA_SF5_B	csf5 capacitance per cell @ Vbias=0V, L=10.8µm, W=4.48µm	52.3	57.1	61.9	fF
IL_SF5	csf5 leakage current @ VL=10V, L=10.8µm, W=4.48µm	-	-	30	fA/cell
Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.					
TC1_SF5	csf5 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

3. Parameters → 3.5 MET5 module→ 3.5.2 Device parameters→ csf5→ Matching parameters

Matching parameters

Name	Description	Typ	Unit
AC_CSF	pelgrom coefficient capacitor mismatch @ L=10.8μm, W=4.48μm	0.5	%μm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csf5a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-66	-60	60	66	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SF5A	csf5a breakdown voltage @ Ibr=1μA	70	-	-	V
CA_SF5A_B	csf5a capacitance per cell @ Vbias=0V, L=11.1μm, W=5.76μm	37.8	41.8	45.8	fF
IL_SF5A	csf5a leakage current @ VL=60V, L=11.1μm, W=5.76μm	-	-	35	fA/cell
Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.					
TC1_SF5A	csf5a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
AC_CSFA	pelgrom coefficient capacitor mismatch @ L=11.1μm, W=5.76μm	0.6	%μm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

3. Parameters → 3.6 METMID module

3.6 METMID module

3.6.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMDTP	metal underneath top metal / top metal equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMDT	top metal – metal underneath top metal dielectric thickness	885	1000	1115	nm
TH_MTP	top metal thickness	885	985	1085	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MTPB	top metal sheet resistance	22	26.5	31	35.5	40	mΩ/□
RVI_VTP	VIATP resistance	-	1.6	2	3.2	4.4	Ω/via
TC1_MTP	top metal temperature coefficient 1	-	-	3.2	-	-	1e-03/K
TC1_VTP	VIATP resistance temperature coefficient 1	-	-	1.35	-	-	1e-03/K
TC2_MTP	top metal temperature coefficient 2	-	-	0	-	-	1e-06/K²
TC2_VTP	VIATP resistance temperature coefficient 2	-	-	0	-	-	1e-06/K²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances.

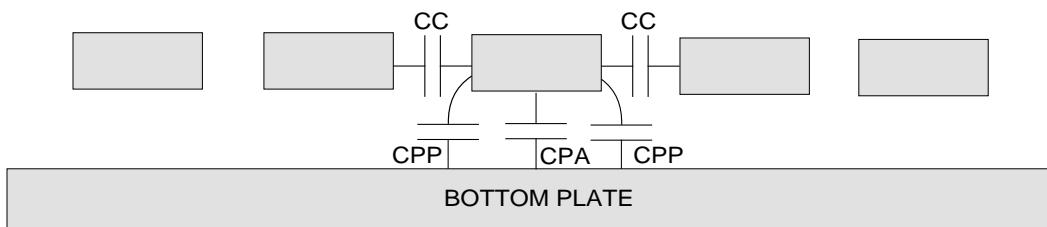


Figure 3.17 Parasitic capacitance structure

Name	Description	Typ	Unit
CC_MTPMTP3	coupling capacitance top metal – top metal (3 metal layers)	94	aF/µm
CC_MTPMTP4	coupling capacitance top metal – top metal (4 metal layers)	94	aF/µm
CC_MTPMTP5	coupling capacitance top metal – top metal (5 metal layers)	94	aF/µm
CC_MTPMTP6	coupling capacitance top metal – top metal (6 metal layers)	94	aF/µm
CPAMTPDIF3	top metal – active area capacitance	8.8	aF/µm²
CPAMTPDIF4	top metal – active area capacitance (4 metal layers)	6.5	aF/µm²
CPAMTPDIF5	top metal – active area capacitance (5 metal layers)	5.1	aF/µm²
CPAMTPDIF6	top metal – active area capacitance (6 metal layers)	4.2	aF/µm²
CPAMTPM1_3	top metal – metal 1 area capacitance area	14.5	aF/µm²
CPAMTPM1_4	top metal – metal 1 area capacitance (4 metal layers)	9.1	aF/µm²

⇒

3. Parameters → 3.6 METMID module→ 3.6.1 Device independent p...→ Parasitic capacitanc...

Name	Description	Typ	Unit
CPAMTPM1_5	top metal – metal 1 area capacitance (5 metal layers)	6.6	aF/ μm^2
CPAMTPM1_6	top metal – metal 1 area capacitance (6 metal layers)	5.2	aF/ μm^2
CPAMTPM2_3	top metal – metal 2 area capacitance	35.3	aF/ μm^2
CPAMTPM2_4	top metal – metal 2 area capacitance (4 metal layers)	14.5	aF/ μm^2
CPAMTPM2_5	top metal – metal 2 area capacitance (5 metal layers)	9.1	aF/ μm^2
CPAMTPM2_6	top metal – metal 2 area capacitance (6 metal layers)	6.6	aF/ μm^2
CPAMTPM3_4	top metal – metal 3 area capacitance (4 metal layers)	35.3	aF/ μm^2
CPAMTPM3_5	top metal – metal 3 area capacitance (5 metal layers)	14.5	aF/ μm^2
CPAMTPM3_6	top metal – metal 3 area capacitance (6 metal layers)	9.1	aF/ μm^2
CPAMTPM4_5	top metal – metal 4 area capacitance (5 metal layers)	35.3	aF/ μm^2
CPAMTPM4_6	top metal – metal 4 area capacitance (6 metal layers)	14.5	aF/ μm^2
CPAMTPM5_6	top metal – metal 5 area capacitance (6 metal layers)	35.3	aF/ μm^2
CPAMTPP1_3	top metal – poly 1 area capacitance area	9.3	aF/ μm^2
CPAMTPP1_4	top metal – poly 1 area capacitance (4 metal layers)	6.7	aF/ μm^2
CPAMTPP1_5	top metal – poly 1 area capacitance (5 metal layers)	5.2	aF/ μm^2
CPAMTPP1_6	top metal – poly 1 area capacitance (6 metal layers)	4.3	aF/ μm^2
CPAMTPSTI3	top metal – field area (STI) area capacitance area	8	aF/ μm^2
CPAMTPSTI4	top metal – field area (STI) area capacitance (4 metal layers)	6	aF/ μm^2
CPAMTPSTI5	top metal – field area (STI) area capacitance (5 metal layers)	4.8	aF/ μm^2
CPAMTPSTI6	top metal – field area (STI) area capacitance (6 metal layers)	4	aF/ μm^2
CPPMTPDIF3	top metal – active perimeter	7.2	aF/ μm
CPPMTPDIF4	top metal – active perimeter capacitance (4 metal layers)	6.7	aF/ μm
CPPMTPDIF5	top metal – active perimeter capacitance (5 metal layers)	6.5	aF/ μm
CPPMTPDIF6	top metal – active perimeter capacitance (6 metal layers)	6.2	aF/ μm
CPPMTPM1_3	Top metal – metal 1 perimeter	5.5	aF/ μm
CPPMTPM1_4	top metal – metal 1 perimeter capacitance (4 metal layers)	4.4	aF/ μm
CPPMTPM1_5	top metal – metal 1 perimeter capacitance (5 metal layers)	3.9	aF/ μm
CPPMTPM1_6	top metal – metal 1 perimeter capacitance (6 metal layers)	3.6	aF/ μm
CPPMTPM2_3	top metal – metal 2 perimeter	9.5	aF/ μm
CPPMTPM2_4	top metal – metal 2 perimeter capacitance (4 metal layers)	5.5	aF/ μm
CPPMTPM2_5	top metal – metal 2 perimeter capacitance (5 metal layers)	4.4	aF/ μm
CPPMTPM2_6	top metal – metal 2 perimeter capacitance (6 metal layers)	3.9	aF/ μm
CPPMTPM3_4	top metal – metal 3 perimeter capacitance (4 metal layers)	9.5	aF/ μm
CPPMTPM3_5	top metal – metal 3 perimeter capacitance (5 metal layers)	5.5	aF/ μm
CPPMTPM3_6	top metal – metal 3 perimeter capacitance (6 metal layers)	4.4	aF/ μm
CPPMTPM4_5	top metal – metal 4 perimeter capacitance (5 metal layers)	9.5	aF/ μm
CPPMTPM4_6	top metal – metal 4 perimeter capacitance (6 metal layers)	5.5	aF/ μm
CPPMTPM5_6	top metal – metal 5 perimeter capacitance (6 metal layers)	9.5	aF/ μm
CPPMTPP1_3	top metal – poly 1 perimeter	4.4	aF/ μm
CPPMTPP1_4	top metal – poly 1 perimeter capacitance (4 metal layers)	3.9	aF/ μm
CPPMTPP1_5	top metal – poly 1 perimeter capacitance (5 metal layers)	3.6	aF/ μm
CPPMTPP1_6	top metal – poly 1 perimeter capacitance (6 metal layers)	3.4	aF/ μm
CPPMTPSTI3	top metal – field area (STI) perimeter	7	aF/ μm

⇒

3. Parameters → 3.6 METMID module → 3.6.1 Device independent p... → Parasitic capacitanc...

Name	Description	Typ	Unit
CPPMTPSTI4	top metal – field area (STI) perimeter capacitance (4 metal layers)	6.6	aF/ μ m
CPPMTPSTI5	top metal – field area (STI) perimeter capacitance (5 metal layers)	6.4	aF/ μ m
CPPMTPSTI6	top metal – field area (STI) perimeter capacitance (6 metal layers)	6.1	aF/ μ m

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC ⁽¹⁾⁽²⁾	Top metal	-40°C to 175°C	-	-	1.6	32	mA/ μ m
JMax_VI_DC ⁽²⁾	Top Via	-40°C to 175°C	-	-	0.7	32	mA/via
JMax_AC ⁽¹⁾⁽³⁾	Top metal	-40°C to 175°C	-	-	7.2	32	mA/ μ m
JMax_VI_AC ⁽³⁾	Top Via	-40°C to 175°C	-	-	3.1	32	mA/via
T_Factor_1e4 ⁽⁴⁾⁽⁵⁾	Top metal	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁴⁾⁽⁵⁾	Top Via	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁴⁾	Top metal	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁴⁾	Top Via	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁴⁾	Top metal	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁴⁾	Top Via	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e5 ⁽⁴⁾⁽⁵⁾	Top metal	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁴⁾⁽⁵⁾	Top Via	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁴⁾	Top metal	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁴⁾	Top Via	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁴⁾	Top metal	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁴⁾	Top Via	125°C to 175°C	-	0.1	-	-	-
E ⁽⁸⁾	Top metal	-40°C to 175°C	-	-	250	-	V/ μ m

Note 1 Valid for all widths.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 4 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 5 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 6 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 125°C

Note 8 lateral electric field between Top Metal track

3.6.2 Device parameters

rmtp

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V

3. Parameters → 3.6 METMID module → 3.6.2 Device parameters → rmtt → Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MTPB	top metal sheet resistance	22	26.5	31	35.5	40	mΩ/□
TC1_MTP	top metal temperature coefficient 1	-	-	3.2	-	-	1e-03/K
TC2_MTP	top metal temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_MTP	top metal effective width @ W=0.44μm	-	0.26	0.32	0.38	-	μm

cift4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-110	-100	100	110	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIFT4	cift4 breakdown voltage @ Ibr=1μA	140	-	-	V
CA_CIFT4	cift4 capacitance per cell @ Vbias=0V, L=25μm, W=7.04μm	43.8	49.8	55.8	fF
IL_CIFT4	cift4 leakage current @ VL=100V	-	-	20	fA/cell
TC1_CIFT4	cift4 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K
VC1_CIFT4	cift4 capacitor voltage coefficient 1	-	0.35	-	ppm/V
VC2_CIFT4	cift4 capacitor voltage coefficient 2	-	-0.19	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
	pelgrom coefficient capacitor mismatch @ L=25.84μm, W=7.04μm	0.95	%μm
AC_CIFT	Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."		

cift5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-110	-100	100	110	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIFT5	cift5 breakdown voltage @ Ibr=1μA	140	-	-	V
CA_CIFT5	cift5 capacitance per cell @ Vbias=0V, L=25μm, W=7.04μm	55.8	63.4	71	fF
IL_CIFT5	cift5 leakage current @ VL=100V	-	-	20	fA/cell
TC1_CIFT5	cift5 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K
VC1_CIFT5	cift5 capacitor voltage coefficient 1	-	0.35	-	ppm/V

3. Parameters → 3.6 METMID module→ 3.6.2 Device parameters→ cift5→ Process parameters

Name	Description	Low	Typ	High	Unit
VC2_CIFT5	cift5 capacitor voltage coefficient 2	-	-0.19	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
	pelgrom coefficient capacitor mismatch @ L=25.84μm, W=7.04μm	0.95	%μm
AC_CIFT	Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."		

cift6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-110	-100	100	110	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIFT6	cift6 breakdown voltage @ Ibr=1μA	140	-	-	V
CA_CIFT6	cift6 capacitance per cell @ Vbias=0V, L=25μm, W=7.04μm	67.3	76.5	85.7	fF
IL_CIFT6	cift6 leakage current @ VL=100V	-	-	20	fA/cell
TC1_CIFT6	cift6 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K
VC1_CIFT6	cift6 capacitor voltage coefficient 1	-	0.35	-	ppm/V
VC2_CIFT6	cift6 capacitor voltage coefficient 2	-	-0.19	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
	pelgrom coefficient capacitor mismatch @ L=25.84μm, W=7.04μm	0.95	%μm
AC_CIFT	Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."		

cift4a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-33	-30	30	33	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIFT4A	cift4a breakdown voltage @ Ibr=1μA	50	-	-	V
CA_CIFT4A	cift4a capacitance per cell @ Vbias=0V, L=11.04μm, W=4.48μm	24.2	27.5	30.8	fF
IL_CIFT4A	cift4a leakage current @ VL=30V, L=11.04μm, W=4.48μm	-	-	30	fA/cell

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3. Parameters → 3.6 METMID module→ 3.6.2 Device parameters→ cift4a→ Process parameters

Name	Description	Low	Typ	High	Unit
TC1_CIFT4A	cift4a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
pelgrom coefficient capacitor mismatch @ L=11.04μm, W=4.48μm	0.5	%μm	
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csft4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT4	csft4 breakdown voltage @ Ibr=1μA	35	-	-	V
CA_SFT4_B	csft4 capacitance per cell @ Vbias=0V, L=10.8μm, W=4.48μm	33.4	36.5	39.6	fF
IL_SFT4	csft4 leakage current @ VL=10V, L=10.8μm, W=4.48μm	-	-	30	fA/cell
TC1_SFT4	csft4 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
pelgrom coefficient capacitor mismatch @ L=10.8μm, W=4.48μm	0.5	%μm	
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csft4a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-66	-60	60	66	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT4A	csft4a breakdown voltage @ Ibr=1μA	70	-	-	V
CA_SFT4A_B	csft4a capacitance per cell @ Vbias=0V, L=11.1μm, W=5.76μm	26	28.7	31.4	fF
IL_SFT4A	csft4a leakage current @ VL=60V, L=11.1μm, W=5.76μm	-	-	35	fA/cell
Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.					

3. Parameters → 3.6 METMID module→ 3.6.2 Device parameters→ csft4a→ Process parameters

Name	Description	Low	Typ	High	Unit
TC1_SFT4A	csft4a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
pelgrom coefficient capacitor mismatch @ L=11.1μm, W=5.76μm	0.6	%μm	
AC_CSFTA	Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."		

cift5a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-33	-30	30	33	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIFT5A	cift5a breakdown voltage @ Ibr=1μA	50	-	-	V
CA_CIFT5A	cift5a capacitance per cell @ Vbias=0V, L=11.04μm, W=4.48μm	31.2	35.4	39.6	fF
IL_CIFT5A	cift5a leakage current @ VL=30V, L=11.04μm, W=4.48μm	-	-	30	fA/cell
TC1_CIFT5A	cift5a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
pelgrom coefficient capacitor mismatch @ L=11.04μm, W=4.48μm	0.5	%μm	
AC_CIFTA	Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."		

csft5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT5	csft5 breakdown voltage @ Ibr=1μA	35	-	-	V
CA_SFT5_B	csft5 capacitance per cell @ Vbias=0V, L=10.8μm, W=4.48μm	45	49.1	53.2	fF
IL_SFT5	csft5 leakage current @ VL=10V, L=10.8μm, W=4.48μm	-	-	30	fA/cell
TC1_SFT5	Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.				
TC1_SFT5	csft5 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

3. Parameters → 3.6 METMID module → 3.6.2 Device parameters → csft5 → Matching parameters

Matching parameters

Name	Description	Typ	Unit
AC_CSFT	pelgrom coefficient capacitor mismatch @ L=10.8µm, W=4.48µm	0.5	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csft5a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-66	-60	60	66	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT5A	csft5a breakdown voltage @ Ibr=1µA	70	-	-	V
CA_SFT5A_B	csft5a capacitance per cell @ Vbias=0V, L=11.1µm, W=5.76µm	34.1	37.7	41.3	fF
IL_SFT5A	csft5a leakage current @ VL=60V, L=11.1µm, W=5.76µm	-	-	35	fA/cell
Note: The leakage current of an array of capacitors is measured and the leakage is quoted for a single cell.					
TC1_SFT5A	csft5a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
AC_CSFTA	pelgrom coefficient capacitor mismatch @ L=11.1µm, W=5.76µm	0.6	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

cift6a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-33	-30	30	33	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_CIFT6A	cift6a breakdown voltage @ Ibr=1µA	50	-	-	V
CA_CIFT6A	cift6a capacitance per cell @ Vbias=0V, L=11.04µm, W=4.48µm	38.1	43.3	48.5	fF
IL_CIFT6A	cift6a leakage current @ VL=30V, L=11.04µm, W=4.48µm	-	-	30	fA/cell
TC1_CIFT6A	cift6a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

3. Parameters → 3.6 METMID module→ 3.6.2 Device parameters→ cift6a→ Matching parameters

Matching parameters

Name	Description	Typ	Unit
AC_CIFTA	pelgrom coefficient capacitor mismatch @ L=11.04μm, W=4.48μm	0.5	%μm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csft6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT6	csft6 breakdown voltage @ Ibr=1μA	35	-	-	V
CA_SFT6_B	csft6 capacitance per cell @ Vbias=0V, L=10.8μm, W=4.48μm	56.4	61.5	66.6	fF
IL_SFT6	csft6 leakage current @ VL=10V, L=10.8μm, W=4.48μm	-	-	30	fA/cell
TC1_SFT6	csft6 temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

Matching parameters

Name	Description	Typ	Unit
AC_CSFT	pelgrom coefficient capacitor mismatch @ L=10.8μm, W=4.48μm	0.5	%μm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

csft6a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-220	-200	200	220	V
Vterm1-Vterm2	-40°C to 175°C	-66	-60	60	66	V

Process parameters

Name	Description	Low	Typ	High	Unit
BDO_SFT6A	csft6a breakdown voltage @ Ibr=1μA	70	-	-	V
CA_SFT6A_B	csft6a capacitance per cell @ Vbias=0V, L=11.1μm, W=5.76μm	42.1	46.6	51.1	fF
IL_SFT6A	csft6a leakage current @ VL=60V, L=11.1μm, W=5.76μm	-	-	35	fA/cell
TC1_SFT6A	csft6a temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

3. Parameters → 3.6 METMID module→ 3.6.2 Device parameters→ csft6a→ Matching parameters

Matching parameters

Name	Description	Typ	Unit
AC_CSFTA	pelgrom coefficient capacitor mismatch @ L=11.1µm, W=5.76µm	0.6	%µm
Note: In order to achieve the reported 'pelgrom-coefficient-like-behavior' a common-centroid layout with surrounding guard ring is necessary. Please also refer to the document Design Guidelines for Improved Device Matching , available on "my X-FAB."			

3. Parameters → 3.7 METTHK module

3.7 METTHK module

3.7.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
EPS_IMDTPL	metal underneath thick metal / thick metal equivalent dielectric constant	-	4	-	-
	Note: The values for dielectric permittivity are mean values only, because the dielectric consists of a stack of layers each with a different permittivity				
THD_IMDTPL	thick metal – top metal dielectric thickness	890	1000	1110	nm
TH_MTPL	thick metal thickness	2800	3110	3420	nm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MTPLB	thick metal sheet resistance	7.7	8.9	10.1	11.3	12.5	mΩ/□
RVI_VTPL	thick via resistance	-	0.9	1.2	1.8	2.4	Ω/via
TC1_MTPL	thick metal temperature coefficient 1	-	-	3.8	-	-	1e-03/K
TC1_VTPL	VIATPL resistance temperature coefficient 1	-	-	1.35	-	-	1e-03/K
TC2_MTPL	thick metal temperature coefficient 2	-	-	0	-	-	1e-06/K ²
TC2_VTPL	VIATPL resistance temperature coefficient 2	-	-	0	-	-	1e-06/K ²

Parasitic capacitance parameters

The following table provides a principal overview with respect to interconnect capacitances.

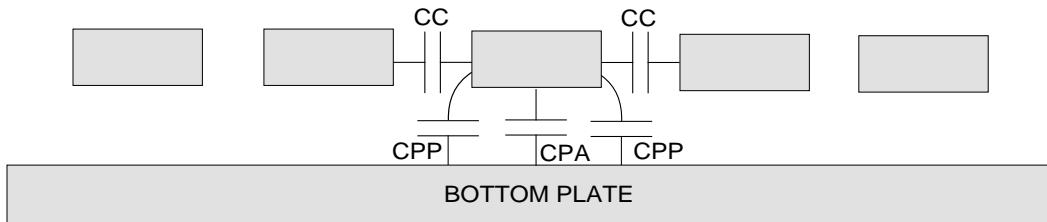


Figure 3.18 Parasitic capacitance structure

Name	Description	Typ	Unit
CC_MTLMTL	coupling capacitance thick metal – thick metal	78	aF/µm
CPAMTLDIFF4	thick metal – active area capacitance (4 metal layers with METTP and METTHK)	6	aF/µm ²
CPAMTLDIFF4L	thick metal – active area capacitance (4 metal layers with METTHK)	6.1	aF/µm ²
CPAMTLDIFF5	thick metal – active area capacitance (5 metal layers with METTP and METTHK)	4.8	aF/µm ²
CPAMTLDIFF5L	thick metal – active area capacitance (5 metal layers with METTHK)	4.9	aF/µm ²
CPAMTLDIFF6	thick metal – active area capacitance (6 metal layers with METTP and METTHK)	4.1	aF/µm ²
CPAMTLDIFF6L	thick metal – active area capacitance (6 metal layers with METTHK)	4.1	aF/µm ²
CPAMTLM14	thick metal – metal 1 area capacitance (4 metal layers with METTP and METTHK)	8	aF/µm ²

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3. Parameters → 3.7 METTHK module→ 3.7.1 Device independent p...→ Parasitic capacitanc...

Name	Description	Typ	Unit
CPAMTLM14L	thick metal – metal 1 area capacitance (4 metal layers with METTHK)	8.3	aF/ μm^2
CPAMTLM15	thick metal – metal 1 area capacitance (5 metal layers with METTP and METTHK)	6.1	aF/ μm^2
CPAMTLM15L	thick metal – metal 1 area capacitance (5 metal layers with METTHK)	6.3	aF/ μm^2
CPAMTLM16	thick metal – metal 1 area capacitance (6 metal layers with METTP and METTHK)	4.9	aF/ μm^2
CPAMTLM16L	thick metal – metal 1 area capacitance (6 metal layers with METTHK)	5	aF/ μm^2
CPAMTLM24	thick metal – metal 2 area capacitance (4 metal layers with METTP and METTHK)	11.8	aF/ μm^2
CPAMTLM24L	thick metal – metal 2 area capacitance (4 metal layers with METTHK)	12.5	aF/ μm^2
CPAMTLM25	thick metal – metal 2 area capacitance (5 metal layers with METTP and METTHK)	8	aF/ μm^2
CPAMTLM25L	thick metal – metal 2 area capacitance (5 metal layers with METTHK)	8.3	aF/ μm^2
CPAMTLM26	thick metal – metal 2 area capacitance (6 metal layers with METTP and METTHK)	6.1	aF/ μm^2
CPAMTLM26L	thick metal – metal 2 area capacitance (6 metal layers with METTHK)	6.3	aF/ μm^2
CPAMTLM34L	thick metal – metal 3 area capacitance (4 metal layers with METTHK)	24.9	aF/ μm^2
CPAMTLM35	thick metal – metal 3 area capacitance (5 metal layers with METTP and METTHK)	11.8	aF/ μm^2
CPAMTLM35L	thick metal – metal 3 area capacitance (5 metal layers with METTHK)	12.5	aF/ μm^2
CPAMTLM36	thick metal – metal 3 area capacitance (6 metal layers with METTP and METTHK)	8	aF/ μm^2
CPAMTLM36L	thick metal – metal 3 area capacitance (6 metal layers with METTHK)	8.3	aF/ μm^2
CPAMTLM45L	thick metal – metal 4 area capacitance (4 metal layers with METTHK)	24.9	aF/ μm^2
CPAMTLM46	thick metal – metal 4 area capacitance (6 metal layers with METTP and METTHK)	11.8	aF/ μm^2
CPAMTLM46L	thick metal – metal 4 area capacitance (6 metal layers with METTHK)	12.5	aF/ μm^2
CPAMTLM56L	thick metal – metal 5 area capacitance (6 metal layers with METTHK)	24.9	aF/ μm^2
CPAMTLMP4	thick metal – top metal area capacitance (4 metal layers with METTP and METTHK)	35.7	aF/ μm^2
CPAMTLMP5	thick metal – top metal area capacitance (5 metal layers with METTP and METTHK)	35.7	aF/ μm^2
CPAMTLMP6	thick metal – top metal area capacitance (6 metal layers with METTP and METTHK)	35.7	aF/ μm^2
CPAMTLP14	thick metal – poly 1 area capacitance (4 metal layers with METTP and METTHK)	6.1	aF/ μm^2
CPAMTLP14L	thick metal – poly 1 area capacitance (4 metal layers with METTHK)	6.3	aF/ μm^2
CPAMTLP15	thick metal – poly 1 area capacitance (5 metal layers with METTP and METTHK)	5	aF/ μm^2
CPAMTLP15L	thick metal – poly 1 area capacitance (5 metal layers with METTHK)	5.1	aF/ μm^2
CPAMTLP16	thick metal – poly 1 area capacitance (6 metal layers with METTP and METTHK)	4.1	aF/ μm^2
CPAMTLP16L	thick metal – poly 1 area capacitance (6 metal layers with METTHK)	4.2	aF/ μm^2
CPAMTLSTI4	thick metal – field area (STI) area capacitance (4 metal layers with METTP and METTHK)	5.6	aF/ μm^2
CPAMTLSTI4L	thick metal – field area (STI) area capacitance (4 metal layers with METTHK)	5.7	aF/ μm^2
CPAMTLSTI5	thick metal – field area (STI) area capacitance (5 metal layers with METTP and METTHK)	4.6	aF/ μm^2

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3. Parameters → 3.7 METTHK module→ 3.7.1 Device independent p...→ Parasitic capacitanc...

Name	Description	Typ	Unit
CPA _{MTLSTI5L}	thick metal – field area (STI) area capacitance (5 metal layers with METTHK)	4.7	aF/ μm^2
CPA _{MTLSTI6}	thick metal – field area (STI) area capacitance (6 metal layers with METTP and METTHK)	3.9	aF/ μm^2
CPA _{MTLSTI6L}	thick metal – field area (STI) area capacitance (6 metal layers with METTHK)	3.9	aF/ μm^2
CPP _{MTLDIFF4}	thick metal – active perimeter capacitance (4 metal layers with METTP and METTHK)	10	aF/ μm
CPP _{MTLDIFF4L}	thick metal – active perimeter capacitance (4 metal layers with METTHK)	10.2	aF/ μm
CPP _{MTLDIFF5}	thick metal – active perimeter capacitance (5 metal layers with METTP and METTHK)	8.8	aF/ μm
CPP _{MTLDIFF5L}	thick metal – active perimeter capacitance (5 metal layers with METTHK)	8.9	aF/ μm
CPP _{MTLDIFF6}	thick metal – active perimeter capacitance (6 metal layers with METTP and METTHK)	8	aF/ μm
CPP _{MTLDIFF6L}	thick metal – active perimeter capacitance (6 metal layers with METTHK)	8.1	aF/ μm
CPP _{MTLM14}	thick metal – metal 1 perimeter capacitance (4 metal layers with METTP and METTHK)	10.1	aF/ μm
CPP _{MTLM14L}	thick metal – metal 1 perimeter capacitance (4 metal layers with METTHK)	10.3	aF/ μm
CPP _{MTLM15}	thick metal – metal 1 perimeter capacitance (5 metal layers with METTP and METTHK)	8	aF/ μm
CPP _{MTLM15L}	thick metal – metal 1 perimeter capacitance (5 metal layers with METTHK)	8.2	aF/ μm
CPP _{MTLM16}	thick metal – metal 1 perimeter capacitance (6 metal layers with METTP and METTHK)	6.7	aF/ μm
CPP _{MTLM16L}	thick metal – metal 1 perimeter capacitance (6 metal layers with METTHK)	6.8	aF/ μm
CPP _{MTLM24}	thick metal – metal 2 perimeter capacitance (4 metal layers with METTP and METTHK)	13.9	aF/ μm
CPP _{MTLM24L}	thick metal – metal 2 perimeter capacitance (4 metal layers with METTHK)	14.5	aF/ μm
CPP _{MTLM25}	thick metal – metal 2 perimeter capacitance (5 metal layers with METTP and METTHK)	10.1	aF/ μm
CPP _{MTLM25L}	thick metal – metal 2 perimeter capacitance (5 metal layers with METTHK)	10.3	aF/ μm
CPP _{MTLM26}	thick metal – metal 2 perimeter capacitance (6 metal layers with METTP and METTHK)	8	aF/ μm
CPP _{MTLM26L}	thick metal – metal 2 perimeter capacitance (6 metal layers with METTHK)	8.2	aF/ μm
CPP _{MTLM34L}	thick metal – metal 3 perimeter capacitance (4 metal layers with METTHK)	24.5	aF/ μm
CPP _{MTLM35}	thick metal – metal 3 perimeter capacitance (5 metal layers with METTP and METTHK)	13.9	aF/ μm
CPP _{MTLM35L}	thick metal – metal 3 perimeter capacitance (5 metal layers with METTHK)	14.5	aF/ μm
CPP _{MTLM36}	thick metal – metal 3 perimeter capacitance (6 metal layers with METTP and METTHK)	10.1	aF/ μm
CPP _{MTLM36L}	thick metal – metal 3 perimeter capacitance (6 metal layers with METTHK)	10.3	aF/ μm
CPP _{MTLM45L}	thick metal – metal 4 perimeter capacitance (4 metal layers with METTHK)	24.5	aF/ μm
CPP _{MTLM46}	thick metal – metal 4 perimeter capacitance (6 metal layers with METTP and METTHK)	13.9	aF/ μm
CPP _{MTLM46L}	thick metal – metal 4 perimeter capacitance (6 metal layers with METTHK)	14.5	aF/ μm
CPP _{MTLM56L}	thick metal – metal 5 perimeter capacitance (6 metal layers with METTHK)	24.5	aF/ μm
CPP _{MTLMTP4}	thick metal – top metal perimeter capacitance (4 metal layers with METTP and METTHK)	31.1	aF/ μm
CPP _{MTLMTP5}	thick metal – top metal perimeter capacitance (5 metal layers with METTP and METTHK)	31.1	aF/ μm

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3. Parameters → 3.7 METTHK module→ 3.7.1 Device independent p...→ Parasitic capacitanc...

Name	Description	Typ	Unit
CPPMTLMTP6	thick metal – top metal perimeter capacitance (6 metal layers with METTP and METTHK)	31.1	aF/µm
CPPMTLP14	thick metal – poly 1 perimeter capacitance (4 metal layers with METTP and METTHK)	8.1	aF/µm
CPPMTLP14L	thick metal – poly 1 perimeter capacitance (4 metal layers with METTHK)	8.2	aF/µm
CPPMTLP15	thick metal – poly 1 perimeter capacitance (5 metal layers with METTP and METTHK)	6.7	aF/µm
CPPMTLP15L	thick metal – poly 1 perimeter capacitance (5 metal layers with METTHK)	6.8	aF/µm
CPPMTLP16	thick metal – poly 1 perimeter capacitance (6 metal layers with METTP and METTHK)	5.8	aF/µm
CPPMTLP16L	thick metal – poly 1 perimeter capacitance (6 metal layers with METTHK)	5.9	aF/µm
CPPMTLSTI4	thick metal – field perimeter (STI) perimeter capacitance (4 metal layers with METTP and METTHK)	9.6	aF/µm
CPPMTLSTI4L	thick metal – field perimeter (STI) perimeter capacitance (4 metal layers with METTHK)	9.8	aF/µm
CPPMTLSTI5	thick metal – field perimeter (STI) perimeter capacitance (5 metal layers with METTP and METTHK)	8.6	aF/µm
CPPMTLSTI5L	thick metal – field perimeter (STI) perimeter capacitance (5 metal layers with METTHK)	8.7	aF/µm
CPPMTLSTI6	thick metal – field perimeter (STI) perimeter capacitance (6 metal layers with METTP and METTHK)	7.9	aF/µm
CPPMTLSTI6L	thick metal – field perimeter (STI) perimeter capacitance (6 metal layers with METTHK)	7.9	aF/µm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JMax_DC ⁽¹⁾⁽²⁾	Thick Metal	-40°C to 175°C	-	-	6	32	mA/µm
JMax_VI_DC ⁽²⁾	Thick Via	-40°C to 175°C	-	-	1	32	mA/via
JMax_AC ⁽¹⁾⁽³⁾	Thick Metal	-40°C to 175°C	-	-	10	32	mA/µm
JMax_VI_AC ⁽³⁾	Thick Via	-40°C to 175°C	-	-	4.5	32	mA/via
T_Factor_1e4 ⁽⁴⁾⁽⁵⁾	Thick Via	-40°C to 85°C	-	4.25	-	-	-
T_Factor_1e4 ⁽⁴⁾⁽⁵⁾	Thick Metal	-40°C to 85°C	-	3.13	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁴⁾	Thick Via	85°C to 125°C	-	1.16	-	-	-
T_Factor_1e4 ⁽⁶⁾⁽⁴⁾	Thick Metal	85°C to 125°C	-	1	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁴⁾	Thick Via	125°C to 175°C	-	0.31	-	-	-
T_Factor_1e4 ⁽⁷⁾⁽⁴⁾	Thick Metal	125°C to 175°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁴⁾⁽⁵⁾	Thick Via	-40°C to 85°C	-	1.35	-	-	-
T_Factor_1e5 ⁽⁴⁾⁽⁵⁾	Thick Metal	-40°C to 85°C	-	1	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁴⁾	Thick Via	85°C to 125°C	-	0.37	-	-	-
T_Factor_1e5 ⁽⁶⁾⁽⁴⁾	Thick Metal	85°C to 125°C	-	0.32	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁴⁾	Thick Via	125°C to 175°C	-	0.1	-	-	-
T_Factor_1e5 ⁽⁷⁾⁽⁴⁾	Thick Metal	125°C to 175°C	-	0.1	-	-	-



3. Parameters → 3.7 METTHK module→ 3.7.1 Device independent p...→ Physical layer opera...

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
E ⁽⁸⁾	Thick Metal	-40 °C to 175 °C	-	-	250	-	V/µm

Note 1 Valid for all widths.

Note 2 Max values of JMAX*DC refer to rms/avg values. Abs. max values of JMAX*DC refer to peak values.

Note 3 Max values of JMAX*AC refer to rms values. Abs. max values of JMAX*AC refer to peak values.

Note 4 Temperature correction factors allow the scaling of the current density according to the required lifetime and temperature. For more detailed information, please refer to the Interconnect reliability sections of the SpecXplorer or Process Reliability Specification.

Note 5 The temperature correction factor remains constant at the stated value across the whole temperatures range.

Note 6 The temperature correction factor is interpolated between given values for temperatures above 85°C.

Note 7 The temperature correction factor is interpolated between given values for temperatures above 125°C

Note 8 lateral electric field between Thick Metal track

3.7.2 Device parameters

rmtpl

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40 °C to 175 °C	-460	-420	420	460	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MTPLB	thick metal sheet resistance	7.7	8.9	10.1	11.3	12.5	mΩ/□
TC1_MTPL	thick metal temperature coefficient 1	-	-	3.8	-	-	1e-03/K
TC2_MTPL	thick metal temperature coefficient 2	-	-	0	-	-	1e-06/K ²
WER_MTPLB	thick metal resistor effective width @ W=3µm	-	2.55	3	3.45	-	µm

3. Parameters → 3.8 THKCOP module

3.8 THKCOP module

3.8.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
TH_METCOPAU	gold metal thickness	0.35	0.5	0.65	µm
TH_METCOPCU	copper metal thickness	8	10	12	µm
TH_METCOPNI	nickel metal thickness	1.7	2	2.3	µm

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MCOP	copper metal sheet resistance	0.7	1.2	1.7	2.2	2.7	mΩ/□
RVI_VCOP	copper via resistance @ L=5µm, W=5µm	-	-	25	50	75	mΩ/via
TC1_METCOP	copper metal temperature coefficient 1	-	-	3.6	-	-	1e-03/K
TC2_METCOP	copper metal temperature coefficient 2	-	-	0.6	-	-	1e-06/K ²

Parasitic capacitance parameters

Name	Description	Typ	Unit
CC_MCOPMCOP5	coupling capacitance thick copper – thick copper (5 metal layers with METTP)	15	aF/µm
CC_MCOPMCOP6	coupling capacitance thick copper – thick copper (6 metal layers with METTHK)	15	aF/µm
CC_MCOPMTL	coupling capacitance thick copper – thick copper (6 metal layers with METTP & METTHK)	15	aF/µm
CPAMCOPDIFF5	thick copper – active area capacitance (5 metal layers with METTP)	2.7	aF/µm ²
CPAMCOPDIFF5L	thick copper – active area capacitance (5 metal layers with METTHK)	2.2	aF/µm ²
CPAMCOPDIFF6	thick copper – active area capacitance (6 metal layers with METTP and METTHK)	2	aF/µm ²
CPAMCOPM15	thick copper – metal 1 area capacitance (5 metal layers with METTP)	3.1	aF/µm ²
CPAMCOPM15L	thick copper – metal 1 area capacitance (5 metal layers with METTHK)	2.4	aF/µm ²
CPAMCOPM16	thick copper – metal 1 area capacitance (6 metal layers with METTP and METTHK)	2.2	aF/µm ²
CPAMCOPM25	thick copper – metal 2 area capacitance (5 metal layers with METTP)	3.6	aF/µm ²
CPAMCOPM25L	thick copper – metal 2 area capacitance (5 metal layers with METTHK)	2.7	aF/µm ²
CPAMCOPM26	thick copper – metal 2 area capacitance (6 metal layers with METTP and METTHK)	2.4	aF/µm ²
CPAMCOPM35	thick copper – metal 3 area capacitance (5 metal layers with METTP)	4.1	aF/µm ²
CPAMCOPM35L	thick copper – metal 3 area capacitance (5 metal layers with METTHK)	3	aF/µm ²
CPAMCOPM36	thick copper – metal 3 area capacitance (6 metal layers with METTP and METTHK)	2.7	aF/µm ²
CPAMCOPMTL5L	thick copper – thick metal area capacitance (5 metal layers with METTHK)	5	aF/µm ²
CPAMCOPMTL6	thick copper – thick metal area capacitance (6 metal layers with METTP and METTHK)	5	aF/µm ²
CPAMCOPMTP5	thick copper – top metal area capacitance (5 metal layers with METTHK)	4.7	aF/µm ²

⇒

3. Parameters → 3.8 THKCOP module→ 3.8.1 Device independent p...→ Parasitic capacitanc...

Name	Description	Typ	Unit
CPAMCOPMTP6	thick copper – top metal area capacitance (6 metal layers with METTP and METTHK)	3.1	aF/ μm^2
CPAMCOPP15	thick copper – poly 1 area capacitance (5 metal layers with METTP)	2.8	aF/ μm^2
CPAMCOPP15L	thick copper – poly 1 area capacitance (5 metal layers with METTHK)	2.2	aF/ μm^2
CPAMCOPP16	thick copper – poly 1 area capacitance (6 metal layers with METTP and METTHK)	2.2	aF/ μm^2
CPAMCOPSTI5	thick copper – field area (STI) area capacitance (5 metal layers with METTP)	2.7	aF/ μm^2
CPAMCOPSTI5L	thick copper – field area (STI) area capacitance (5 metal layers with METTHK)	2.1	aF/ μm^2
CPAMCOPSTI6	thick copper – field area (STI) area capacitance (6 metal layers with METTP and METTHK)	2	aF/ μm^2
CPPMCOPDIFF5	thick copper – active perimeter capacitance (5 metal layers with METTP)	10.9	aF/ μm
CPPMCOPDIFF5L	thick copper – active perimeter capacitance (5 metal layers with METTHK)	9.4	aF/ μm
CPPMCOPDIFF6	thick copper – active perimeter capacitance (6 metal layers with METTP and METTHK)	8.8	aF/ μm
CPPMCOPM15	thick copper – metal 1 perimeter capacitance (5 metal layers with METTP)	11.5	aF/ μm
CPPMCOPM15L	thick copper – metal 1 perimeter capacitance (5 metal layers with METTHK)	9.6	aF/ μm
CPPMCOPM16	thick copper – metal 1 perimeter capacitance (6 metal layers with METTP and METTHK)	8.9	aF/ μm
CPPMCOPM25	thick copper – metal 2 perimeter capacitance (5 metal layers with METTP)	12.4	aF/ μm
CPPMCOPM25L	thick copper – metal 2 perimeter capacitance (5 metal layers with METTHK)	10.3	aF/ μm
CPPMCOPM26	thick copper – metal 2 perimeter capacitance (6 metal layers with METTP and METTHK)	9.6	aF/ μm
CPPMCOPM35	thick copper – metal 3 perimeter capacitance (5 metal layers with METTP)	13.6	aF/ μm
CPPMCOPM35L	thick copper – metal 3 perimeter capacitance (5 metal layers with METTHK)	11.2	aF/ μm
CPPMCOPM36	thick copper – metal 3 perimeter capacitance (6 metal layers with METTP and METTHK)	10.3	aF/ μm
CPPMCOPMTL5	thick copper – thick top perimeter capacitance (5 metal layers with METTP)	14.5	aF/ μm
CPPMCOPMTL5L	thick copper – thick metal perimeter capacitance (5 metal layers with METTHK)	15	aF/ μm
CPPMCOPMTL6	thick copper – thick metal perimeter capacitance (6 metal layers with METTP and METTHK)	15	aF/ μm
CPPMCOPMTP6	thick copper – top metal perimeter capacitance (6 metal layers with METTP and METTHK)	13.2	aF/ μm
CPPMCOPP15	thick copper – poly 1 perimeter capacitance (5 metal layers with METTP)	10.6	aF/ μm
CPPMCOPP15L	thick copper – poly 1 perimeter capacitance (5 metal layers with METTHK)	9	aF/ μm
CPPMCOPP16	thick copper – poly 1 perimeter capacitance (6 metal layers with METTP and METTHK)	8.4	aF/ μm
CPPMCOPSTI5	thick copper – field area (STI) perimeter capacitance (5 metal layers with METTP)	10.7	aF/ μm
CPPMCOPSTI5L	thick copper – field area (STI) perimeter capacitance (5 metal layers with METTHK)	9.2	aF/ μm
CPPMCOPSTI6	thick copper – field area (STI) perimeter capacitance (6 metal layers with METTP and METTHK)	8.7	aF/ μm

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JDL	Thick copper	-40°C to 175°C	-	-	25	-	mA/ μm

3. Parameters → 3.8 THKCOP module→ 3.8.1 Device independent p...→ Physical layer opera...

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
JVI ⁽¹⁾ ⁽²⁾	Thick copper	-40°C to 175°C	-	-	400	-	mA/via
E ⁽³⁾	Thick copper	-40°C to 175°C	-	-	10	-	V/µm

Note 1 Defined by 50K Joule heating limit

Note 2 Total viacop structure limited by aluminum physical layer operating conditions

Note 3 Lateral electric field between METCOP tracks at room temperature

3.8.2 Device parameters

rmrdl

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSR_MCOP	copper metal sheet resistance	0.7	1.2	1.7	2.2	2.7	mΩ/□
TC1_METCOP	copper metal temperature coefficient 1	-	-	3.6	-	-	1e-03/K
TC2_METCOP	copper metal temperature coefficient 2	-	-	0.6	-	-	1e-06/K ²
WER_MCOP	copper metal effective width @ W=15µm	-	-	15.5	-	-	µm

3. Parameters → 3.9 HRPOLY module

3.9 HRPOLY module

3.9.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRNP1H	high-ohmic N doped poly 1 sheet resistance	4	5.15	6.3	7.45	8.6	kΩ/□
TC1NP1H	high-ohmic N doped poly 1 temperature coefficient 1	-	-5.8	-5.4	-5	-	1e-03/K
TC2NP1H	high-ohmic N doped poly 1 temperature coefficient 2	-	17.9	19.4	20.9	-	1e-06/K ²

3.9.2 Device parameters

rnp1h, rnp1h_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.1	-	mA/μm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65μW/μm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRNP1H	high-ohmic N doped poly 1 sheet resistance	4	5.15	6.3	7.45	8.6	kΩ/□
TC1NP1H	high-ohmic N doped poly 1 temperature coefficient 1	-	-5.8	-5.4	-5	-	1e-03/K
TC2NP1H	high-ohmic N doped poly 1 temperature coefficient 2	-	17.9	19.4	20.9	-	1e-06/K ²
VCBNP1H	high-ohmic N-doped poly 1 bulk voltage coefficient	-	-	0.35	-	-	1e-03/V
WERNP1H	high-ohmic N doped poly 1 effective width @ W=0.42μm	-	0.29	0.34	0.39	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_NP1H	pelgrom coefficient resistor mismatch	2.63	%μm
DWRNP1H	resistor delta width	0.08	μm

3. Parameters → 3.10 MRPOLY module

3.10 MRPOLY module

3.10.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSE_MRPSB	medium resistance poly 1 silicide block edge resistance per terminal	-	-	100	-	-	Ωµm
RSR_MRP	medium resistive poly 1 sheet resistance	800	900	1000	1100	1200	Ω/□
TC1MRP	medium resistive poly1 temperature coefficient 1	-	-0.95	-0.85	-0.75	-	1e-03/K
TC1MRPRSE	medium resistance poly 1 silicide block edge resistance temperature coefficient 1	-	-	-1.5	-	-	1e-03/K
TC2MRP	medium resistive poly1 temperature coefficient 2	-	1.3	1.6	1.9	-	1e-06/K ²
TC2MRPRSE	medium resistance poly 1 silicide block edge resistance temperature coefficient 2	-	-	3	-	-	1e-06/K ²
VCBMRP	medium resistive poly 1 bulk voltage coefficient	-	-	-0.122	-	-	1e-03/V

3.10.2 Device parameters

rpp1k1, rpp1k1_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-66	-60	60	66	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.25	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65µW/µm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSE_MRPSB	medium resistance poly 1 silicide block edge resistance per terminal	-	-	100	-	-	Ωµm
RSR_MRP	medium resistive poly 1 sheet resistance	800	900	1000	1100	1200	Ω/□
TC1MRP	medium resistive poly1 temperature coefficient 1	-	-0.95	-0.85	-0.75	-	1e-03/K
TC1MRPRSE	medium resistance poly 1 silicide block edge resistance temperature coefficient 1	-	-	-1.5	-	-	1e-03/K
TC2MRP	medium resistive poly1 temperature coefficient 2	-	1.3	1.6	1.9	-	1e-06/K ²
TC2MRPRSE	medium resistance poly 1 silicide block edge resistance temperature coefficient 2	-	-	3	-	-	1e-06/K ²

3. Parameters → 3.10 MRPOLY module → 3.10.2 Device parameters → rpp1k1, rpp1k1_3 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VCBMRP	medium resistive poly 1 bulk voltage coefficient	-	-	-0.122	-	-	1e-03/V
WERMRP	medium resistive poly 1 effective width @ W=0.42µm	-	0.29	0.35	0.41	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_MRP	pelgrom coefficient resistor mismatch	1.95	%µm
DWRMRP	resistor delta width	0.07	µm

rpp1k1a, rpp1k1a_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V
JDL ⁽²⁾	-40°C to 175°C	-	-	0.25	-	mA/µm

Note 1 An inversion layer is formed in the bulk underneath the poly if the terminal-to-bulk voltage exceeds the field threshold voltage. The field threshold voltages are specified in section "3. Parameters"

Note 2 The maximum current density is derived for a maximum resistance change of 0.1% over lifetime in the temperature range -40°C to 175°C. It is determined based on a maximum power/area density of 65µW/µm².

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSE_MRPSB	medium resistance poly 1 silicide block edge resistance per terminal	-	-	100	-	-	Ωµm
RSR_MRP	medium resistive poly 1 sheet resistance	800	900	1000	1100	1200	Ω/□
TC1MRP	medium resistive poly1 temperature coefficient 1	-	-0.95	-0.85	-0.75	-	1e-03/K
TC1MRPRSE	medium resistance poly 1 silicide block edge resistance temperature coefficient 1	-	-	-1.5	-	-	1e-03/K
TC2MRP	medium resistive poly1 temperature coefficient 2	-	1.3	1.6	1.9	-	1e-06/K ²
TC2MRPRSE	medium resistance poly 1 silicide block edge resistance temperature coefficient 2	-	-	3	-	-	1e-06/K ²
VCBMRP	medium resistive poly 1 bulk voltage coefficient	-	-	-0.122	-	-	1e-03/V
WERMRP	medium resistive poly 1 effective width @ W=0.42µm	-	0.29	0.35	0.41	-	µm

Matching parameters

Name	Description	Typ	Unit
AR_MRP	pelgrom coefficient resistor mismatch	1.95	%µm
DWRMRP	resistor delta width	0.07	µm

3. Parameters → 3.11 DTI module

3.11 DTI module

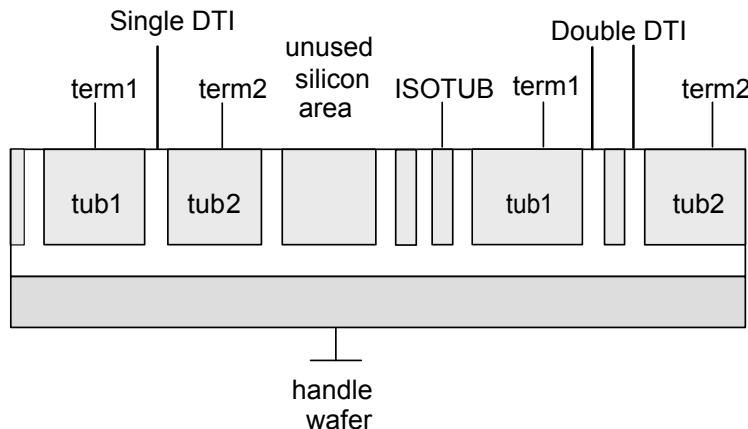


Figure 3.19 Cross-Sectional diagram showing DTI

The Handle Wafer can be biased by using the HWC module, by relying on large-area capacitive coupling through the BOX, or by backside metalisation/packaging.

Due to capacitive coupling effects, Tub should be biased at the defined potential and not left floating. An exception is that ISOTUBS between multiple DTI rings must be floating for higher voltage isolation and reduced parasitics.

3.11.1 Device independent parameters

Parasitic capacitance parameters

Name	Description	Typ	Unit
CC_TBTB	coupling capacitance tub – tub (Single DTI)	0.121	fF/ μ m
CPATUB	tub-handle wafer area capacitance	0.0345	fF/ μ m ²
CC_DTBTB	coupling capacitance tub – tub (Double DTI)	0.0605	fF/ μ m
Note: tub – tub coupling capacitance is reciprocal function of number of DTI			

Dielectric isolation electrical parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVTTR	Single DTI breakdown voltage	-	200	-	-	-	V
TLLDTR	Double DTI leakage per drawn length @ Vbias=250V	-	-	0.5	-	-	pA/ μ m
TLLTR	Single DTI leakage per drawn length @ Vbias=150V	-	-	-	-	50	pA/ μ m
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

Physical layer operating conditions

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm1-Vterm2	Single POLYDTI	-40°C to 175°C	-66	-60	60	66	V
Vterm1-Vterm2	Single DTI	-40°C to 175°C	-165	-150	150	165	V
Vterm1-Vterm2	Double DTI	-40°C to 175°C	-330	-300	300	330	V
Vterm1-Vterm2	Triple DTI	-40°C to 175°C	-495	-450	450	495	V

3. Parameters → 3.11 DTI module → 3.11.1 Device independent p... → Physical layer opera...

Name	Structure	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vtub-handle wafer	Single DTI, Single POLYDTI, Double DTI, Triple DTI	-40°C to 175°C	-440	-400	400	440	V

3.11.2 Device parameters

nmva

The device nmva is superseded by nmvaa. nmva must not be used for any new designs. The device model will not receive any further updates.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-11	-10	5.5	7	V
VDS	-40°C to 175°C	-0.5	0	10	11	V
VDB	-40°C to 175°C	-0.5	0	10	11	V
VD-HW ⁽¹⁾	-40°C to 175°C	-55	-50	200	220	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMVA	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	12	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDS _{NMVA}	saturation current @ VG=5V, VD=5V, L=0.5µm, W=10µm	360	405	450	495	540	µA/µm
VTX _{NMVA}	extrapolated threshold voltage @ VD=0.1V, L=0.5µm, W=10µm	0.48	0.61	0.73	0.85	0.98	V

nmvaa

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-11	-10	5.5	7	V
VDS	-40°C to 175°C	-	-1.5	10	11	V
VDB	-40°C to 175°C	-	-1.5	10	11	V
VD-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 This operating condition will not be checked by automatic check tools.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

3. Parameters → 3.11 DTI module→ 3.11.2 Device parameters→ nmvaa→ Process parameters

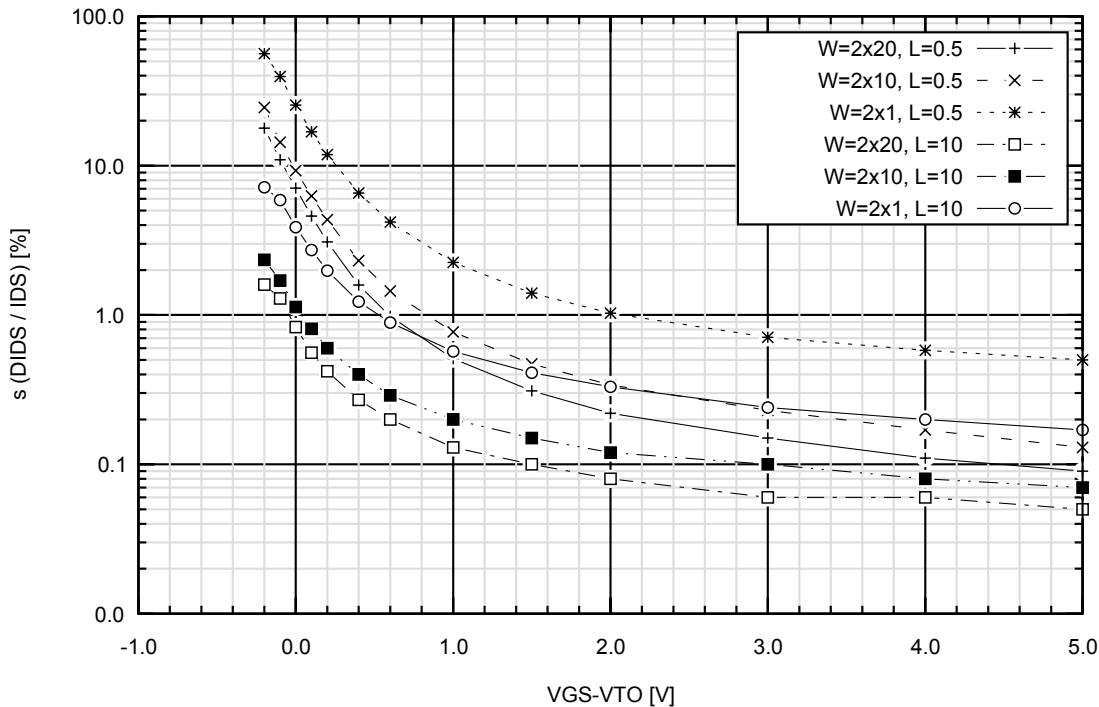
Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMVAA	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	12	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDPNMVAA	pulsed saturation current @ VG=5V, VD=5V, Dcyc=1%, Pwid=100ns, NF=2, WF=10µm	-	-	493	-	-	µA/µm
IDSNMVAA	saturation current @ VG=5V, VD=5V, L=0.5µm, W=20µm, NF=2, WF=10µm	325	355	385	415	445	µA/µm
KP_NMVAAL	gain factor long channel @ L=10µm, W=20µm	-	-	225	-	-	µA/V ²
ROANMVAA	area specific on-resistance @ VG=5V, VD=0.1V, L=0.5µm, W=20µm, Pitch=1.95µm, NF=2, WF=10µm	-	-	7.3	8.8	-	mΩmm ²
RO_NMVAA	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	2.4	3.1	3.8	4.5	5.2	kΩµm
TC_VTXNMVAA	threshold voltage temperature coefficient	-	-	-1.3	-	-	mV/K
VT1NMVAA	snap-back trigger voltage @ VGS=5V, Ngates=10, WF=50µm	-	-	24	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 Technical Report MOS TLP Characteristics" at "my X-FAB"						
VTXNMVAA	extrapolated threshold voltage short channel @ VD=0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	0.7	0.76	0.82	0.88	0.94	V
VTXNMVAAL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=20µm, NF=2, WF=10µm	-	-	0.74	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTNMVAA	pelgrom coefficient gain factor mismatch	1.78	%µm
AIDNMVAA00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	25.6	%µm
AIDNMVAA02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	11.93	%µm
AIDNMVAA04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.59	%µm
AIDNMVAA06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.22	%µm
AIDNMVAA10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.29	%µm
AIDNMVAA20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.05	%µm
AIDNMVAA30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.73	%µm
AIDNMVAA50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.5	%µm
AVTNMVAA	pelgrom coefficient threshold voltage mismatch	15.73	mVµm
DLTNMVAA	transistor delta length	0	µm
DWTNMVAA	transistor delta width	0	µm

3. Parameters → 3.11 DTI module→ 3.11.2 Device parameters→ nmvaa→ Matching parameters

**Figure 3.20** Device nmvaa: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nmvab****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-11	-10	5.5	7	V
VDS	-40°C to 175°C	-	-1.5	10	11	V
VDB	-40°C to 175°C	-	-1.5	10	11	V
VD-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 This operating condition will not be checked by automatic check tools.**Note 2** This forward current is allowed only for transistor's drain bulk junction**Note 3** Pulsed operation with negligible self-heating (<=100ns)**Note:** The node B (BULK) is: PWELL2**Process parameters**

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMVAB	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	12	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNMVAB	pulsed saturation current @ VG=5V, VD=5V, Dcyc=1%, Pwid=100ns, NF=2, WF=10µm	-	-	502	-	-	µA/µm

⇒

3. Parameters → 3.11 DTI module→ 3.11.2 Device parameters→ nmvab→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDS _{NMVAB}	saturation current @ VG=5V, VD=5V, L=0.5μm, W=20μm, NF=2, WF=10μm	330	360	390	420	450	μA/μm
KP _{NMVABL}	gain factor long channel @ L=10μm, W=20μm	-	-	225	-	-	μA/V ²
ROA _{NMVAB}	area specific on-resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, Pitch=2.57μm, NF=2, WF=10μm	-	-	9	10.5	-	mΩmm ²
RO _{NMVAB}	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	2.1	2.8	3.5	4.2	4.9	kΩμm
TC _{VTXNMVAB}	threshold voltage temperature coefficient	-	-	-1.3	-	-	mV/K
VT1 _{NMVAB}	snap-back trigger voltage @ VGS=5V, Ngates=10, WF=50μm	-	-	25	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report MOS TLP Characteristics " at "my X-FAB"							
VTX _{NMVAB}	extrapolated threshold voltage short channel @ VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	0.73	0.79	0.85	0.91	0.97	V
VTX _{NMVABL}	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=20μm, NF=2, WF=10μm	-	-	0.74	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABT _{NMVAB}	pelgrom coefficient gain factor mismatch	1.98	%μm
AID _{NMVAB00}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	25.17	%μm
AID _{NMVAB02}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	11.82	%μm
AID _{NMVAB04}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.56	%μm
AID _{NMVAB06}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.22	%μm
AID _{NMVAB10}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.32	%μm
AID _{NMVAB20}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.07	%μm
AID _{NMVAB30}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.74	%μm
AID _{NMVAB50}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVT _{NMVAB}	pelgrom coefficient threshold voltage mismatch	16.23	mVμm
DLT _{NMVAB}	transistor delta length	0	μm
DWT _{NMVAB}	transistor delta width	0	μm

3. Parameters → 3.11 DTI module→ 3.11.2 Device parameters→ nmvab→ Matching parameters

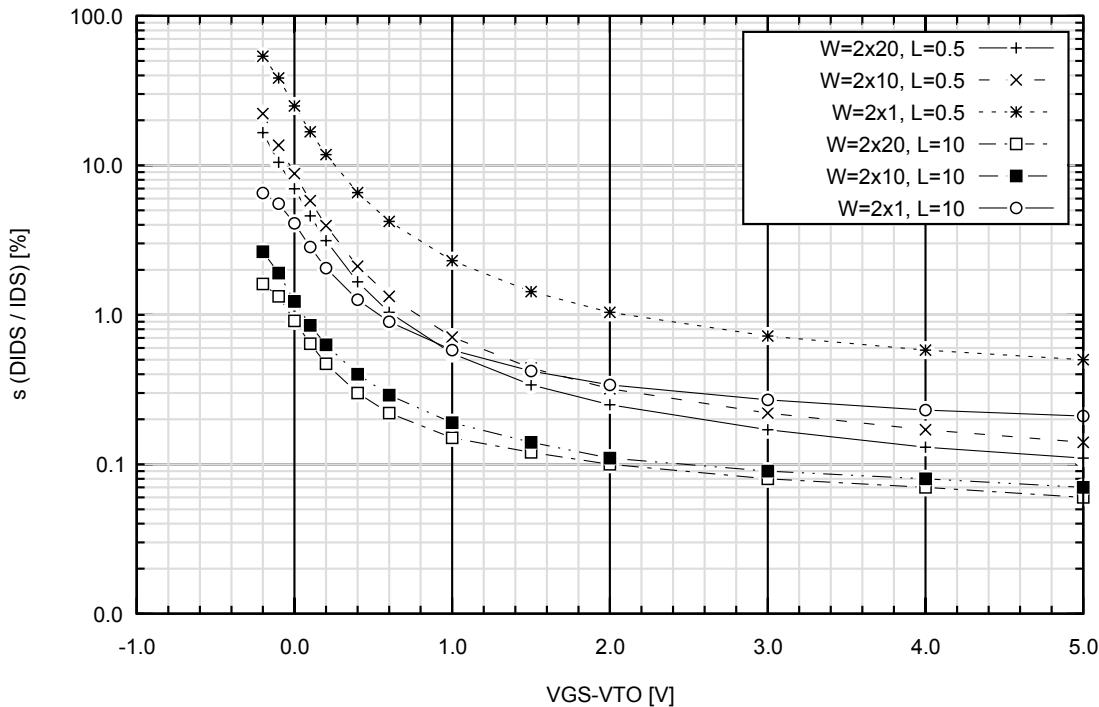


Figure 3.21 Device nmvab: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pmva

The device pmva is superseded by pmvaa. pmva must not be used for any new designs. The device model will not receive any further updates.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	10	11	V
VDS	-40°C to 175°C	-11	-10	0	0.5	V
VDB	-40°C to 175°C	-11	-10	0	0.5	V
VB-HW ⁽¹⁾	-40°C to 175°C	-55	-50	200	220	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMVA	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	12	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDSPMVA	saturation current @ VG=-5V, VD=-5V, L=0.5µm, W=10µm	160	198	235	273	310	µA/µm
VTXPMVA	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=10µm	-1.06	-0.93	-0.81	-0.69	-0.56	V

3. Parameters → 3.11 DTI module→ 3.11.2 Device parameters→ pmvaa→ Operating conditions

pmvaa

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	10	11	V
VDS	-40°C to 175°C	-11	-10	1.5	-	V
VDB	-40°C to 175°C	-11	-10	1.5	-	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 This operating condition will not be checked by automatic check tools.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMVAA	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	12	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPMVAA	pulsed saturation current @ VG=-5V, VD=-5V, Dcyc=1%, Pwid=100ns, NF=2, WF=10µm	-	-	243	-	-	µA/µm
IDS PMVAA	saturation current @ VG=-5V, VD=-5V, L=0.5µm, W=20µm, NF=2, WF=10µm	169	187	205	223	241	µA/µm
KP_PMVAA	gain factor @ L=10µm, W=20µm, NF=2, WF=10µm	-	-	57	-	-	µA/V ²
ROAPMVAA	area specific on-resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=1.95µm, NF=2, WF=10µm	-	-	19	22	-	mΩmm ²
RO_PMVAA	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	7.2	8.5	9.8	11.1	12.4	kΩµm
TC_VTXPMVAA	threshold voltage temperature coefficient	-	-	1.3	-	-	mV/K
VTXPMVAA	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.05	-0.99	-0.93	-0.87	-0.81	V
VTXPMVAAL	extrapolated threshold voltage @ VD=-0.1V, L=10µm, W=20µm, NF=2, WF=10µm	-	-	-0.86	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTPMVAA	pelgrom coefficient gain factor mismatch	1	%µm
AIDPMVAA00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	15.44	%µm
AIDPMVAA02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	7.46	%µm
AIDPMVAA04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	4.44	%µm

3. Parameters → 3.11 DTI module→ 3.11.2 Device parameters→ pmvaa→ Matching parameters

Name	Description	Typ	Unit
AIDPMVAA06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	3.04	%μm
AIDPMVAA10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	1.86	%μm
AIDPMVAA20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.97	%μm
AIDPMVAA30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.71	%μm
AIDPMVAA50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.46	%μm
AVTPMVAA	pelgrom coefficient threshold voltage mismatch	9.58	mVμm
DLTPMVAA	transistor delta length	0	μm
DWTPMVAA	transistor delta width	0	μm

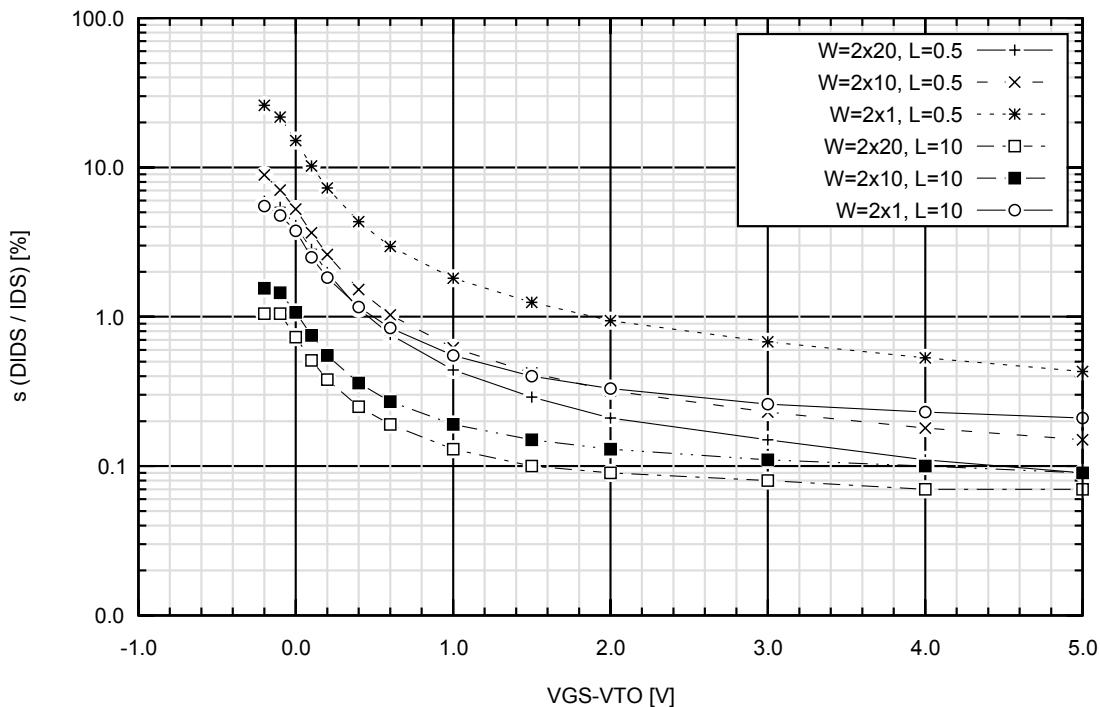


Figure 3.22 Device pmvaa: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pmvab**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	10	11	V
VDS	-40°C to 175°C	-11	-10	1.5	-	V
VDB	-40°C to 175°C	-11	-10	1.5	-	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 This operating condition will not be checked by automatic check tools.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: NWELL2

3. Parameters → 3.11 DTI module→ 3.11.2 Device parameters→ pmvab→ Process parameters

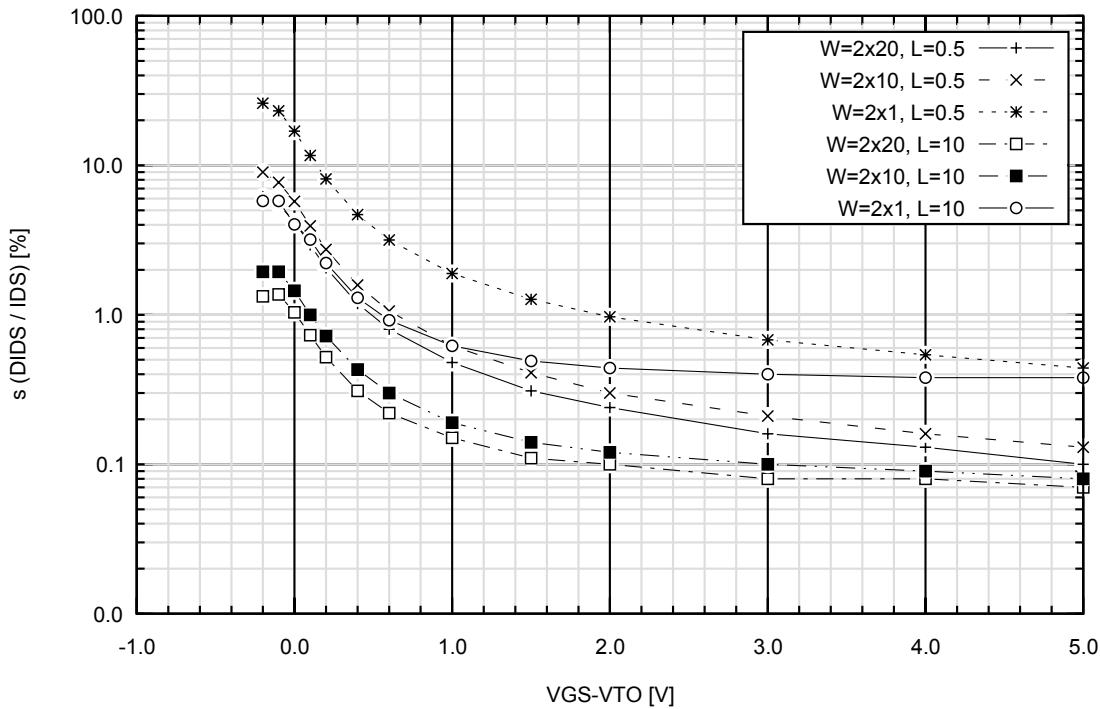
Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMVAB	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	12	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPMVAB	pulsed saturation current @ VG=-5V, VD=-5V, Dcyc=1%, Pwid=100ns, NF=2, WF=10µm	-	-	243	-	-	µA/µm
IDS PMVAB	saturation current @ VG=-5V, VD=-5V, L=0.5µm, W=20µm, NF=2, WF=10µm	169	187	205	223	241	µA/µm
KP_PMVABL	gain factor @ L=10µm, W=20µm, NF=2, WF=10µm	-	-	57	-	-	µA/V ²
ROAPMVAB	area specific on-resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=2.57µm, NF=2, WF=10µm	-	-	24.2	27.2	-	mΩmm ²
RO_PMVAB	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	6.8	8.1	9.4	10.7	12	kΩµm
TC_VTXPMVAB	threshold voltage temperature coefficient	-	-	1.3	-	-	mV/K
VTXPMVAB	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.08	-1.02	-0.96	-0.9	-0.84	V
VTXPMVABL	extrapolated threshold voltage @ VD=-0.1V, L=10µm, W=20µm, NF=2, WF=10µm	-	-	-0.86	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTPMVAB	pelgrom coefficient gain factor mismatch	1.16	%µm
AIDPMVAB00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	17.19	%µm
AIDPMVAB02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	8.28	%µm
AIDPMVAB04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	4.79	%µm
AIDPMVAB06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	3.25	%µm
AIDPMVAB10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	1.95	%µm
AIDPMVAB20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.02	%µm
AIDPMVAB30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.73	%µm
AIDPMVAB50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.5	%µm
AVTPMVAB	pelgrom coefficient threshold voltage mismatch	10.22	mVµm
DLTPMVAB	transistor delta length	0	µm
DWTPMVAB	transistor delta width	0	µm

3. Parameters → 3.11 DTI module→ 3.11.2 Device parameters→ pmvab→ Matching parameters

**Figure 3.23** Device pmvab: drain current matching vs. VGS-VTO (typical values, drawn W and L)**rxw2ti****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-0.5	0	5.5	7	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) : PEPI

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RSRXW2TI	NWELL under active sheet resistance	0.35	0.4	0.45	0.5	0.55	kΩ/□
TC_1XW2TI	NWELL temperature coefficient 1	-	3.3	3.6	3.9	-	1e-03/K
TC_2XW2TI	NWELL temperature coefficient 2	-	7.4	9.8	12.2	-	1e-06/K ²
WERXW2TI	NWELL under active effective @ W=2μm	-	1.66	1.81	1.96	-	μm

Matching parameters

Name	Description	Typ	Unit
AR_XW2TI	pelgrom coefficient resistor mismatch	1.7	%μm
DWRXW2TI	resistor delta width	0.19	μm

3. Parameters → 3.11 DTI module → 3.11.2 Device parameters → mosvcti → Operating conditions

mosvcti

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V

Process parameters

Name	Description	Typ	Unit
CNV_MVCTI	varactor capacitance at negative voltage @ Vterm=-1.8V, f=100kHz	8	fF/µm²
CPV_MVCTI	varactor capacitance at positive voltage @ Vterm=1.8V, f=100kHz	2	fF/µm²
TUR_MVCTI	tuning range @ Vlow=-1.8V, Vhigh=1.8V, f=100kHz	75	%

mosvc5ti

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGB ⁽¹⁾	-40°C to 175°C	-7	-5.5	1.98	7	V

Note 1 VGB Max operating condition means a model limit. Between VGB Max and VGB Abs.Max, the device will be very slow in terms of charge carriers because it works in deep depletion region. Only thermally generated charge carriers are available which lead to very large time constants at low temperatures. The C-V-curve will show memory effects when used between VGB=1.98V...7V. This effect can not be modeled.

Process parameters

Name	Description	Typ	Unit
CNV_MVC5TI	varactor capacitance at negative voltage @ Vterm=-5V, f=100kHz	2.6	fF/µm²
CPV_MVC5TI	varactor capacitance at positive voltage @ Vterm=1.8V, f=100kHz	0.8	fF/µm²
TUR_MVC5TI	tuning range @ Vlow=-5V, Vhigh=1.8V, f=100kHz	69	%

3. Parameters → 3.12 PSUB module

3.12 PSUB module

3.12.1 Device parameters

qpva

emitter area: $2 \times 2 \mu\text{m}^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V
VC-HW ⁽¹⁾	-40°C to 175°C	-2.3	-1.98	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

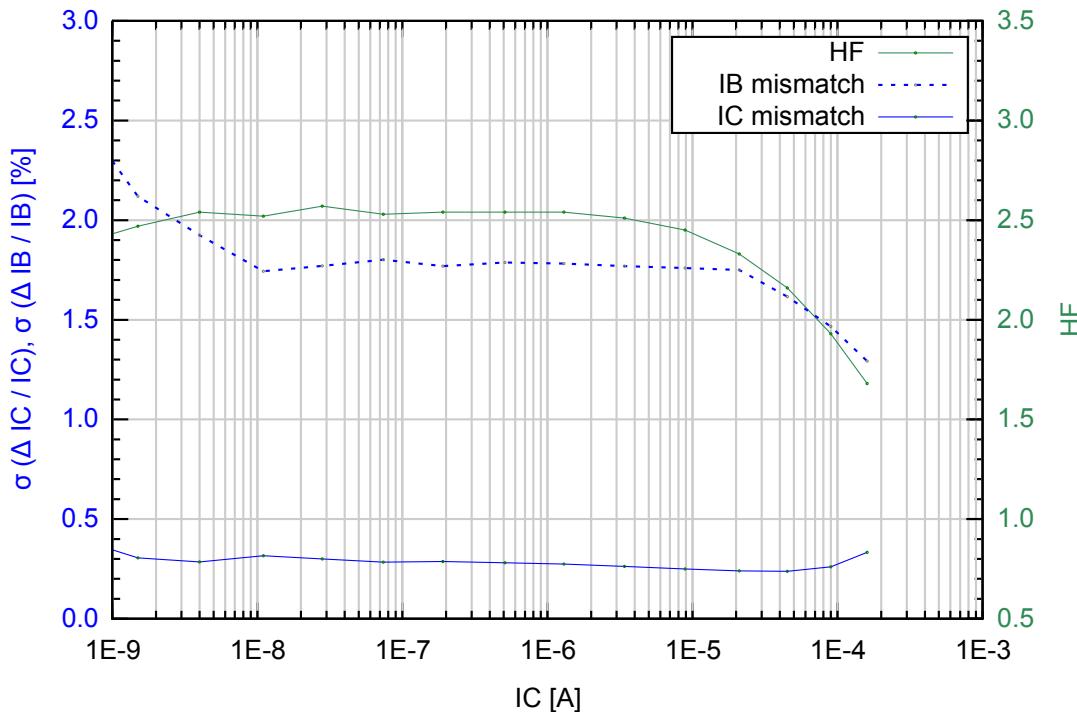
Process parameters

Name	Description	Low	Typ	High	Unit
EVFPA	Early voltage @ $I_b = -1 \mu\text{A}$	500	-	-	V
HF_PA	forward current gain @ $I_e = 1 \mu\text{A}$	-	2.7	-	-
VBEPA	base-emitter voltage @ $I_e = 1 \mu\text{A}$	-	708	-	mV

Matching parameters

Name	Description	Typ	Unit
SIBPA1	standard deviation base current mismatch @ $I_c = 100 \text{nA}$	1.76	%
SIBPA2	standard deviation base current mismatch @ $I_c = 10 \mu\text{A}$	1.76	%
SICPA1	standard deviation collector current mismatch @ $I_c = 100 \text{nA}$	0.29	%
SICPA2	standard deviation collector current mismatch @ $I_c = 10 \mu\text{A}$	0.24	%
SVBPA1	standard deviation base emitter voltage mismatch @ $I_e = 100 \text{nA}$	0.24	mV
SVBPA2	standard deviation base emitter voltage mismatch @ $I_e = 10 \mu\text{A}$	0.2	mV

3. Parameters → 3.12 PSUB module→ 3.12.1 Device parameters→ qpva→ Matching parameters

**Figure 3.24** Device qpva: IC matching and IB matching vs. IC (typical values)**qpvb**emitter area: $5 \times 5 \mu\text{m}^2$ **Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V
VC-HW ⁽¹⁾	-40°C to 175°C	-2.3	-1.98	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.**Process parameters**

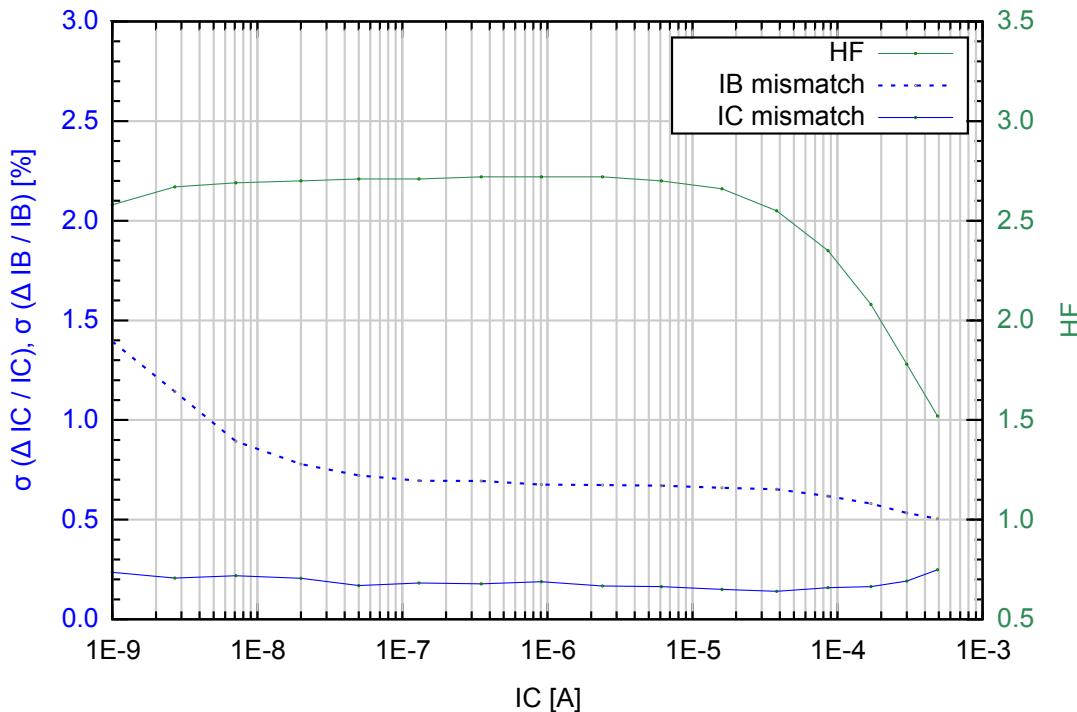
Name	Description	LSL	Low	Typ	High	USL	Unit
EVFPB	Early voltage @ Ib=-1μA	-	200	-	-	-	V
HF_PB	forward current gain @ Ie=1μA	-	-	2.8	-	-	-
VBEPB	base-emitter voltage @ Ie=1μA	659	664	669	674	679	mV

Matching parameters

Name	Description	Typ	Unit
SIBPB1	standard deviation base current mismatch @ Ic=100nA	0.7	%
SIBPB2	standard deviation base current mismatch @ Ic=10μA	0.65	%
SICPB1	standard deviation collector current mismatch @ Ic=100nA	0.18	%
SICPB2	standard deviation collector current mismatch @ Ic=10μA	0.16	%
SVBPB1	standard deviation base emitter voltage mismatch @ Ie=100nA	0.22	mV

3. Parameters → 3.12 PSUB module → 3.12.1 Device parameters → qpvb → Matching parameters

Name	Description	Typ	Unit
SVPB2	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$	0.18	mV

**Figure 3.25** Device qpvb: IC matching and IB matching vs. IC (typical values)**qpvc**emitter area: $10 \times 10 \mu m^2$ **Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VEB	-40°C to 175°C	-2.3	-1.98	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	1.98	2.3	V
VC-HW ⁽¹⁾	-40°C to 175°C	-2.3	-1.98	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.**Process parameters**

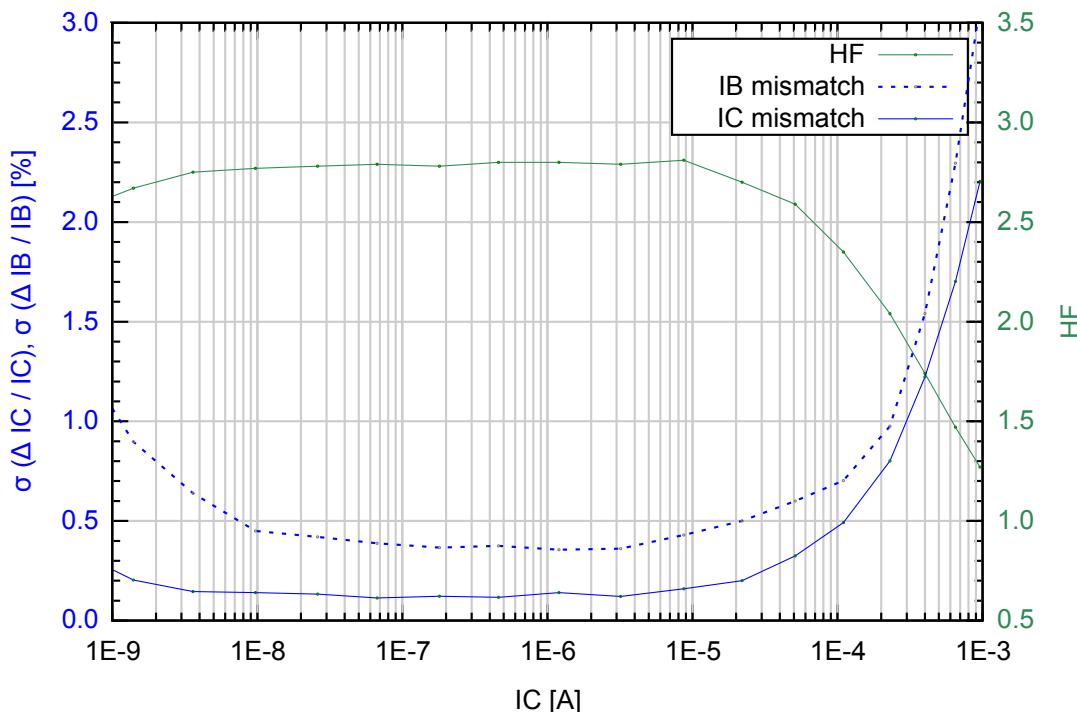
Name	Description	Low	Typ	High	Unit
EVFPC	Early voltage @ $I_b=-1\mu A$	100	-	-	V
HF_PC	forward current gain @ $I_e=1\mu A$	-	2.8	-	-
VBEPC	base-emitter voltage @ $I_e=1\mu A$	-	636	-	mV

Matching parameters

Name	Description	Typ	Unit
SIBPC1	standard deviation base current mismatch @ $I_c=100nA$	0.37	%
SIBPC2	standard deviation base current mismatch @ $I_c=10\mu A$	0.36	%
SICPC1	standard deviation collector current mismatch @ $I_c=100nA$	0.12	%

3. Parameters → 3.12 PSUB module → 3.12.1 Device parameters → qpvc → Matching parameters

Name	Description	Typ	Unit
SICPC2	standard deviation collector current mismatch @ $I_C=10\mu A$	0.12	%
SVBPC1	standard deviation base emitter voltage mismatch @ $I_E=100nA$	0.21	mV
SVBPC2	standard deviation base emitter voltage mismatch @ $I_E=10\mu A$	0.16	mV

**Figure 3.26** Device qpvc: IC matching and IB matching vs. IC (typical values)**qpva5**emitter area: $2 \times 2 \mu m^2$ **Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-7	-5.5	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.**Process parameters**

Name	Description	Low	Typ	High	Unit
EVFPA5	Early voltage @ $I_B=-1\mu A$	500	-	-	V
HF_PA5	forward current gain @ $I_E=1\mu A$	-	1.9	-	-
VBEPA5	base-emitter voltage @ $I_E=1\mu A$	-	709	-	mV

Matching parameters

Name	Description	Typ	Unit
SIBPA51	standard deviation base current mismatch @ $I_C=100nA$	1.79	%

3. Parameters → 3.12 PSUB module→ 3.12.1 Device parameters→ qpva5→ Matching parameters

Name	Description	Typ	Unit
SIBPA52	standard deviation base current mismatch @ $I_c=10\mu A$	1.65	%
SICPA51	standard deviation collector current mismatch @ $I_c=100nA$	0.35	%
SICPA52	standard deviation collector current mismatch @ $I_c=10\mu A$	0.35	%
SVBPA51	standard deviation base emitter voltage mismatch @ $I_e=100nA$	0.3	mV
SVBPA52	standard deviation base emitter voltage mismatch @ $I_e=10\mu A$	0.23	mV

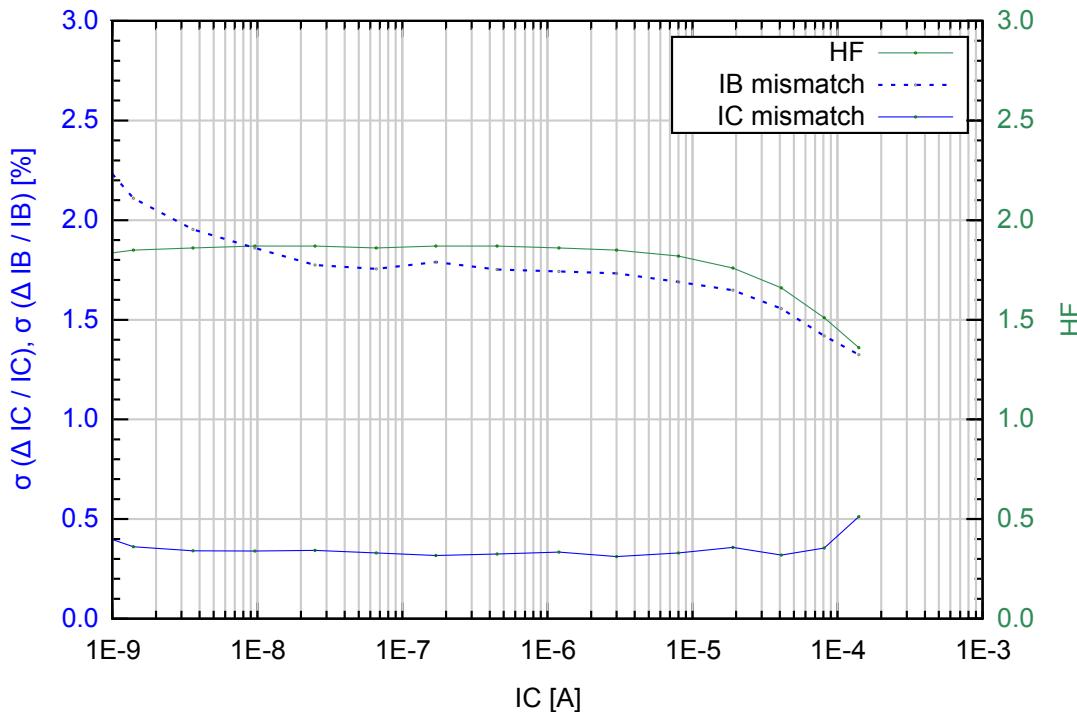


Figure 3.27 Device qpva5: IC matching and IB matching vs. IC (typical values)

qpvb5emitter area: $5 \times 5 \mu m^2$ **Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-7	-5.5	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.**Process parameters**

Name	Description	LSL	Low	Typ	High	USL	Unit
EVFPB5	Early voltage @ $I_b=1\mu A$	-	200	-	-	-	V
HF_PB5	forward current gain @ $I_e=1\mu A$	-	-	2.1	-	-	-
VBEPB5	base-emitter voltage @ $I_e=1\mu A$	660	665	670	675	680	mV

3. Parameters → 3.12 PSUB module → 3.12.1 Device parameters → qpvb5 → Matching parameters

Matching parameters

Name	Description	Typ	Unit
SIBPB51	standard deviation base current mismatch @ $I_c=100\text{nA}$	0.56	%
SIBPB52	standard deviation base current mismatch @ $I_c=10\mu\text{A}$	0.55	%
SICPB51	standard deviation collector current mismatch @ $I_c=100\text{nA}$	0.19	%
SICPB52	standard deviation collector current mismatch @ $I_c=10\mu\text{A}$	0.21	%
SVBPB51	standard deviation base emitter voltage mismatch @ $I_e=100\text{nA}$	0.27	mV
SVBPB52	standard deviation base emitter voltage mismatch @ $I_e=10\mu\text{A}$	0.16	mV

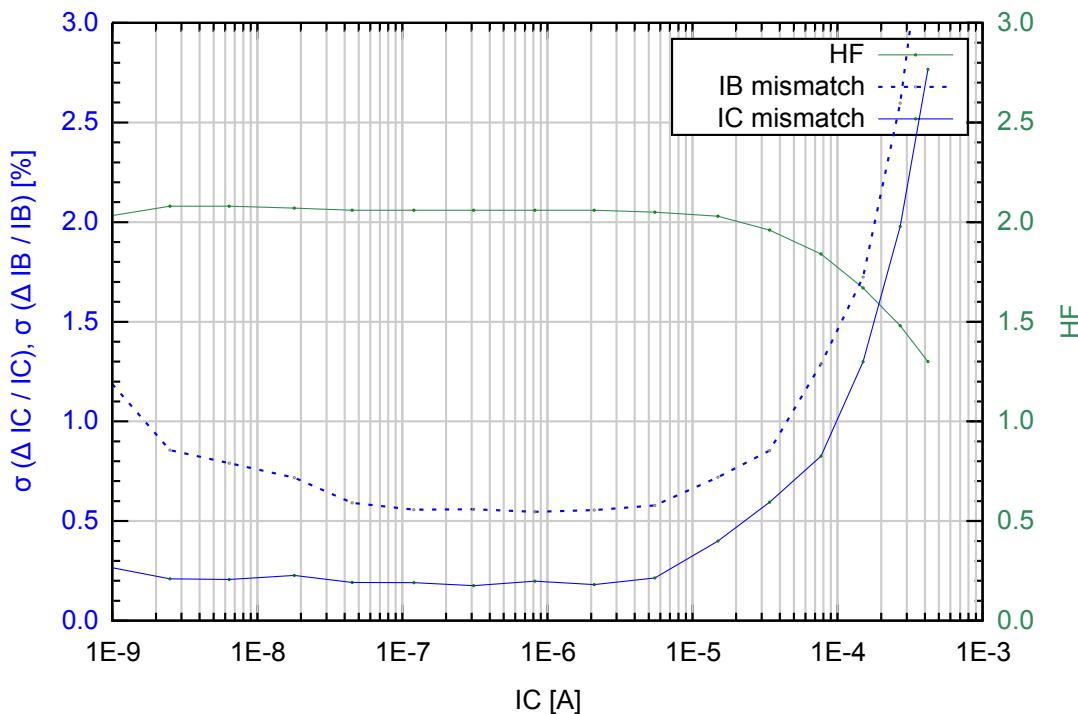


Figure 3.28 Device qpvb5: IC matching and IB matching vs. IC (typical values)

qpvc5

emitter area: $10 \times 10 \mu\text{m}^2$

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	0	0.5	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-7	-5.5	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	Low	Typ	High	Unit
EVFPC5	Early voltage @ $I_b=-1\mu\text{A}$	100	-	-	V
HF_PC5	forward current gain @ $I_e=1\mu\text{A}$	-	2.2	-	-
VBEPC5	base-emitter voltage @ $I_e=1\mu\text{A}$	-	636	-	mV

3. Parameters → 3.12 PSUB module → 3.12.1 Device parameters → qpvc5 → Matching parameters

Matching parameters

Name	Description	Typ	Unit
SIBPC51	standard deviation base current mismatch @ $I_c=100\text{nA}$	0.34	%
SIBPC52	standard deviation base current mismatch @ $I_c=10\mu\text{A}$	0.26	%
SICPC51	standard deviation collector current mismatch @ $I_c=100\text{nA}$	0.12	%
SICPC52	standard deviation collector current mismatch @ $I_c=10\mu\text{A}$	0.15	%
SVBPC51	standard deviation base emitter voltage mismatch @ $I_e=100\text{nA}$	0.22	mV
SVBPC52	standard deviation base emitter voltage mismatch @ $I_e=10\mu\text{A}$	0.15	mV

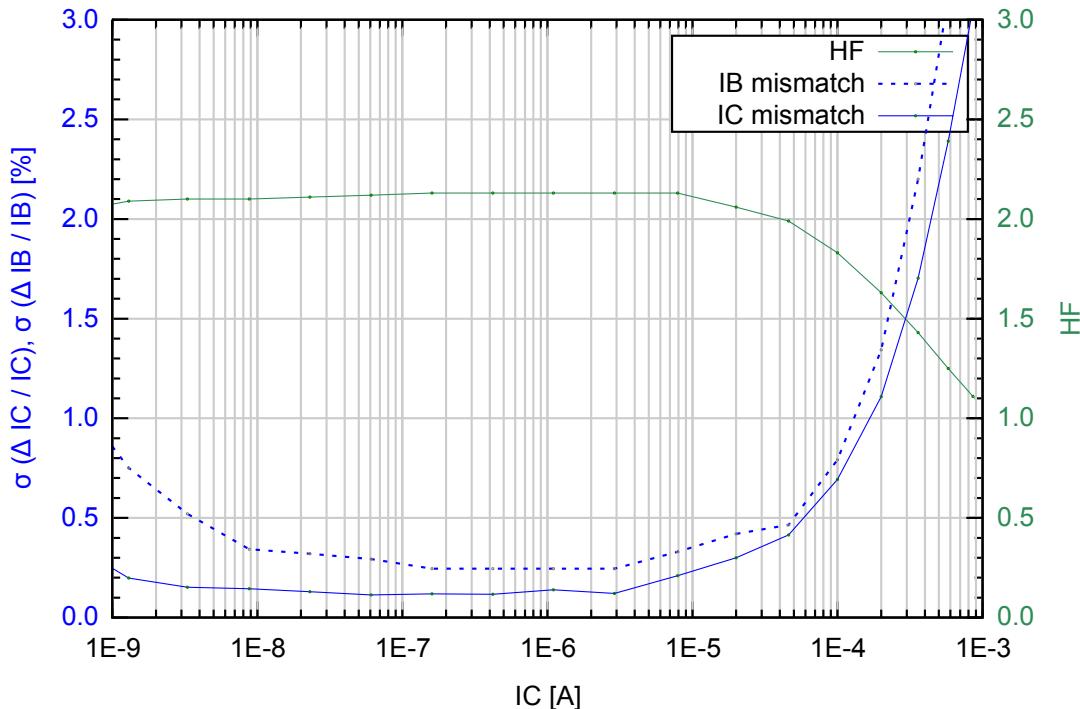


Figure 3.29 Device qpvc5: IC matching and IB matching vs. IC (typical values)

dfwdn5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-7	-6	1.5	-	V
VA-HW ⁽²⁾	-40°C to 175°C	-440	-400	400	440	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDN5	breakdown voltage @ $I_{rev}=1\mu\text{A}$, $L=1\mu\text{m}$, $W=10\mu\text{m}$	8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							



3. Parameters → 3.12 PSUB module→ 3.12.1 Device parameters→ dfwdn5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDFWDN5	forward voltage temperature coefficient	-	-	-1.8	-	-	mV/K
VDFDFWDN5	diode forward voltage @ Idio=1µA, L=1µm, W=10µm	0.699	0.704	0.709	0.714	0.719	V

ds5b**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	1.5	-	V
Vcathode-HW ⁽¹⁾	-40°C to 175°C	-	-1.5	200	220	V

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DS5BL	breakdown voltage @ Irev=1mA, L=0.94µm, W=50µm	7.3	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BV_DS5BS	breakdown voltage @ Irev=50µA, L=0.94µm, W=2.4µm	7.3	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDFDS5BL	diode forward current @ Vbias=0.6V, L=0.94µm, W=50µm	-	-	7000	-	-	µA
IDFDS5BS	diode forward current @ Vbias=0.6V, L=0.94µm, W=2.4µm	-	-	410	-	-	µA
IL_DS5BL2	leakage current @ VL=2V, L=0.94µm, W=50µm	-	-	100	-	-	nA
IL_DS5BL5	leakage current @ VL=5.5V, L=0.94µm, W=50µm	-	-	1150	-	300000	nA
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DS5BS2	leakage current @ VL=2V, L=0.94µm, W=2.4µm	-	-	4.8	-	-	nA
IL_DS5BS5	leakage current @ VL=5.5V, L=0.94µm, W=2.4µm	-	-	55	-	-	nA
TC_VDFDS5B	forward voltage temperature coefficient	-	-	-1.1	-	-	mV/K
VDFDS5BL	diode forward voltage @ Idio=200µA, L=0.94µm, W=50µm	-	-	0.37	-	-	V
VDFDS5BS	diode forward voltage @ Idio=10µA, L=0.94µm, W=2.4µm	0.31	0.345	0.38	0.415	0.45	V

3. Parameters → 3.13 LVT module

3.13 LVT module

3.13.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_NW3	NWELL3 junction depth	1.5	μm

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSRNW3	NWELL3 sheet resistance (STI terminated)	1050	Ω/□

3.13.2 Device parameters

nel

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PWELL3

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNELSA	drain-source breakdown @ VG=0V, Id=1μA, L=0.22μm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXNEL	mobility exponent	-	-	-1.83	-	-	-
FC_NEL	corner frequency @ VD=1.8V, Id=1μA	-	-	1.83	-	-	kHz
GAMNEL	body factor long channel @ L=10μm, W=10μm	-	-	0.505	-	-	√V
IDSNELSA	saturation current @ VG=1.8V, VD=1.8V, L=0.22μm, W=10μm	418	493	568	643	718	μA/μm
IOFNELSA	off-state leakage @ VD=1.8V, L=0.22μm, W=10μm	-	-	-	1.5	-	nA/μm
ISBNELSA	maximum substrate current @ VD=1.8V, L=0.22μm	-	-	0.07	-	-	μA/μm
KP_NELL	gain factor @ L=10μm, W=10μm	-	-	287	-	-	μA/V ²
LEFNELA	effective channel length @ L=0.22μm	-	-	0.2	-	-	μm
NOINEL	input referred noise @ VD=1.8V, Id=1μA, f=1Hz, L=10μm, W=10μm	-	-	13.2	-	-	μVμm/√(Hz)
STSNELSA	subthreshold slope @ VD=0.1V	-	-	11.9	-	-	decade/V

3. Parameters → 3.13 LVT module→ 3.13.2 Device parameters→ nel→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VTXNEL	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.8	-	-	mV/K
U0_NEL	effective mobility	-	-	345	-	-	cm ² /(Vs)
VTINELL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.27	0.3	0.33	0.36	0.39	V
VTINELSA	threshold voltage short channel @ VD=0.1V, L=0.22µm, W=10µm	0.25	0.29	0.34	0.39	0.43	V
VTINELSSA	threshold voltage small channel @ VD=0.1V, L=0.22µm, W=0.22µm	-	-	0.345	-	-	V
VTXNELSA	extrapolated threshold voltage short channel @ VD=0.1V, L=0.22µm, W=10µm	-	-	0.395	-	-	V
WEFNEL	effective channel width @ W=0.22µm	-	-	0.21	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTNEL	pelgrom coefficient gain factor mismatch	0.57	%µm
AIDNEL00	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0V	7.1	%µm
AIDNEL01	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.1V	4.49	%µm
AIDNEL02	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.2V	3.02	%µm
AIDNEL04	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.4V	1.69	%µm
AIDNEL06	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.6V	1.15	%µm
AIDNEL08	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.8V	0.87	%µm
AIDNEL10	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1V	0.72	%µm
AIDNEL14	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1.4V	0.55	%µm
AVTNEL	pelgrom coefficient threshold voltage mismatch	4.11	mVµm
DLTNEL	transistor delta length	0.02	µm
DWTNEL	transistor delta width	0.01	µm

3. Parameters → 3.13 LVT module → 3.13.2 Device parameters → nel → Matching parameters

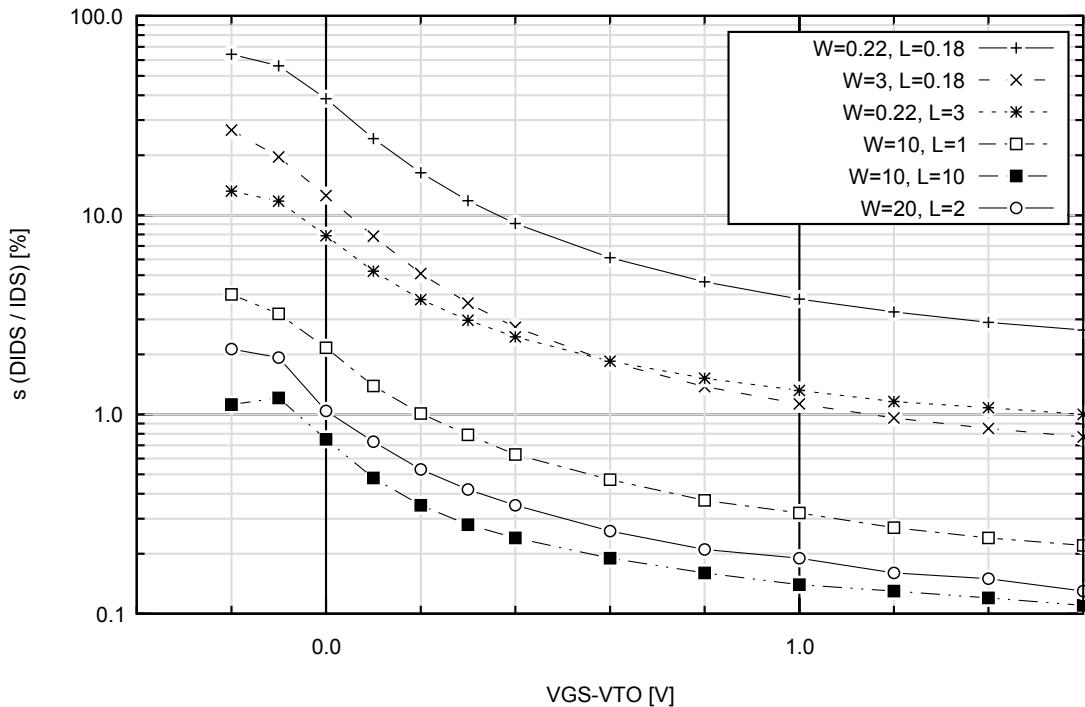


Figure 3.30 Device nel: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pel, pel_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBptub	-40°C to 175°C	-0.5	0	1.98	2.3	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL3

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPELSA	drain-source breakdown @ VG=0V, Id=-1µA, L=0.22µm	3.6	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEXPEL	mobility exponent	-	-	-1.15	-	-	-
FC_PEL	corner frequency @ VD=-1.8V, Id=-1µA	-	-	0.28	-	-	kHz
GAMPEL	body factor long channel @ L=10µm, W=10µm	-	-	0.432	-	-	√V
IDSPELSA	saturation current @ VG=-1.8V, VD=-1.8V, L=0.22µm, W=10µm	178	228	278	328	378	µA/µm

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3. Parameters → 3.13 LVT module→ 3.13.2 Device parameters→ pel, pel_5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IOFPELSA	off-state leakage @ VD=-1.8V, L=0.22μm, W=10μm	-	-	-	1.5	-	nA/μm
KP_PELL	gain factor @ L=10μm, W=10μm	-	-	69	-	-	μA/V ²
LEFPELA	effective channel length @ L=0.22μm	-	-	0.17	-	-	μm
NOIPEL	input referred noise @ VD=-1.8V, Id=-1μA, f=1Hz, L=10μm, W=10μm	-	-	13.6	-	-	μVμm/√(Hz)
STSPELSA	subthreshold slope @ VD=-0.1V	-	-	11.6	-	-	decade/V
TC_VTXPEL	threshold voltage temperature coefficient @ L=10μm, W=10μm	-	-	0.7	-	-	mV/K
U0_PEL	effective mobility	-	-	81	-	-	cm ² /(Vs)
VTIPELL	threshold voltage long channel @ VD=-0.1V, L=10μm, W=10μm	-0.41	-0.38	-0.35	-0.32	-0.29	V
VTIPELSA	threshold voltage short channel @ VD=-0.1V, L=0.22μm, W=10μm	-0.455	-0.395	-0.335	-0.275	-0.215	V
VTIPELSSA	threshold voltage small channel @ VD=-0.1V, L=0.22μm, W=0.22μm	-	-	-0.35	-	-	V
VTXPELSA	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.22μm, W=10μm	-	-	-0.336	-	-	V
WEFPEL	effective channel width @ W=0.22μm	-	-	0.255	-	-	μm

Matching parameters

Name	Description	Typ	Unit
ABTPEL	pelgrom coefficient gain factor mismatch	0.55	%μm
AIDPEL00	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0V	6.19	%μm
AIDPEL01	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.1V	3.75	%μm
AIDPEL02	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.2V	2.37	%μm
AIDPEL04	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.4V	1.32	%μm
AIDPEL06	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.6V	0.91	%μm
AIDPEL08	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.8V	0.72	%μm
AIDPEL10	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1V	0.63	%μm
AIDPEL14	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1.4V	0.49	%μm
AVTPEL	pelgrom coefficient threshold voltage mismatch	3.12	mVμm
DLTPEL	transistor delta length	0.05	μm
DWTPEL	transistor delta width	-0.035	μm

3. Parameters → 3.13 LVT module→ 3.13.2 Device parameters→ pel, pel_5→ Matching parameters

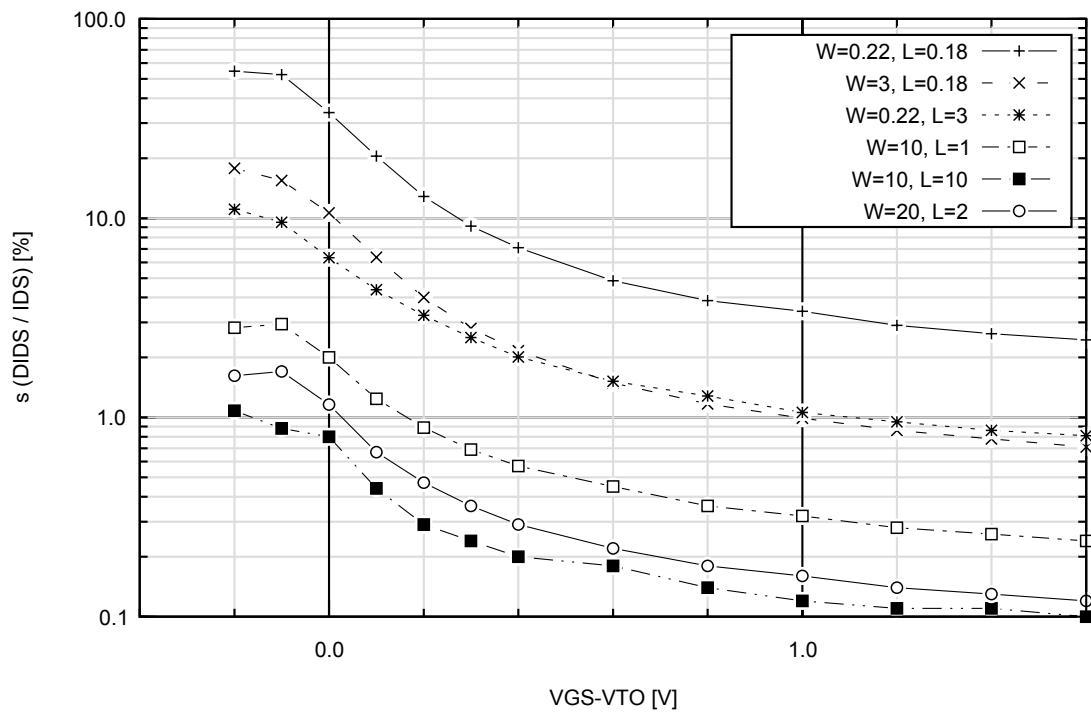


Figure 3.31 Device pel: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.14 SVT module

3.14 SVT module

3.14.1 Device parameters

nesvt

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VSB	-40°C to 175°C	-0.5	0	1.98	2.3	V
VB-HW	-40°C to 175°C	-440	-400	400	440	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS_NESVTS	drain-source breakdown @ VG=0V, Id=1µA, L=0.21µm	3.6	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEX_NESVT	mobility exponent	-	-	-1.84	-	-	-
FC_NESVT	corner frequency @ VD=1.8V, Id=1µA	-	-	4.1	-	-	kHz
GA_NESVT	body factor long channel @ L=10µm, W=10µm	-	-	0.58	-	-	√V
IDS_NESVTS	saturation current @ VG=1.8V, VD=1.8V, L=0.21µm, W=10µm	390	453	515	577	640	µA/µm
IOF_NESVTS	off-state leakage @ VD=1.8V, L=0.21µm, W=10µm	-	-	-	80	-	pA/µm
ISB_NESVTS	bulk current @ VD=1.8V, L=0.21µm	-	-	0.03	-	-	µA/µm
KP_NESVT	gain factor long channel @ L=10µm, W=10µm	-	-	265	-	-	µA/V²
LEF_NESVT	effective channel length @ L=0.21µm	-	-	0.2	-	-	µm
NOI_NESVT	input referred noise @ VD=1.8V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	12.7	-	-	µVµm/√(Hz)
STS_NESVT	subthreshold slope @ VD=1.8V	-	-	12.3	-	-	decade/V
TC_VTX_NESVT	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-0.92	-	-	mV/K
U0_NESVT	effective mobility	-	-	320	-	-	cm²/(Vs)
VTI_NESVTL	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	0.38	0.41	0.44	0.47	0.5	V
VTI_NESVTS	threshold voltage short channel @ VD=0.1V, L=0.21µm, W=10µm	0.34	0.4	0.46	0.52	0.58	V
VTI_NESVTSS	threshold voltage small channel @ VD=0.1V, L=0.21µm, W=0.22µm	-	-	0.38	-	-	V
VTX_NESVTS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.21µm, W=10µm	-	-	0.52	-	-	V
WEF_NESVT	effective channel width @ W=0.22µm	-	-	0.18	-	-	µm

3. Parameters → 3.14 SVT module → 3.14.1 Device parameters → nesvt → Matching parameters

Matching parameters

Name	Description	Typ	Unit
ABTNEVT	pelgrom coefficient gain factor mismatch	0.74	%μm
AIDNESVT00	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0V	9.57	%μm
AIDNESVT01	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.1V	6.34	%μm
AIDNESVT02	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.2V	4.42	%μm
AIDNESVT04	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.4V	2.57	%μm
AIDNESVT06	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.6V	1.79	%μm
AIDNESVT08	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.8V	1.39	%μm
AIDNESVT10	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1V	1.17	%μm
AIDNESVT14	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1.4V	0.88	%μm
AVTNEVT	pelgrom coefficient threshold voltage mismatch	5.66	mVμm
DLTNEVT	transistor delta length	0.01	μm
DWTNEVT	transistor delta width	0.04	μm

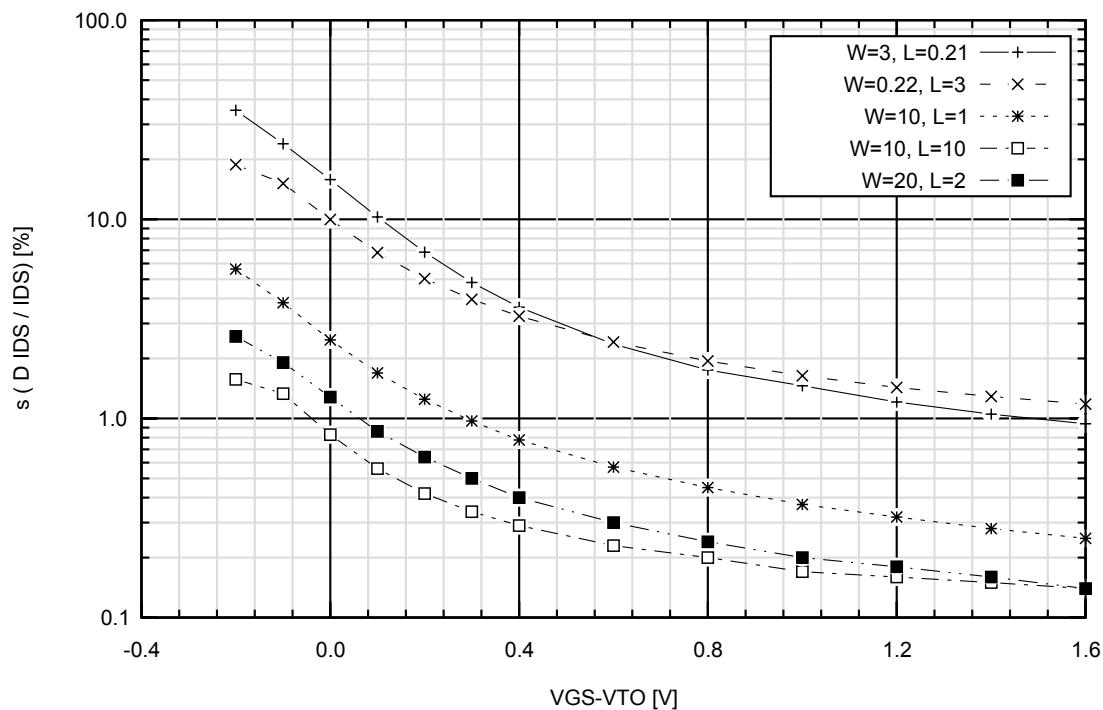


Figure 3.32 Device nesvt: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pesvt, pesvt_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VBptub	-40°C to 175°C	-0.5	0	1.98	2.3	V

⇒

3. Parameters → 3.14 SVT module→ 3.14.1 Device parameters→ pesvt, pesvt_5→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VPT-HW	-40°C to 175°C	-440	-400	400	440	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPEVTS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.21µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPESVT	mobility exponent	-	-	-1.02	-	-	-
FC_PESVT	corner frequency @ VD=-1.8V, Id=-1µA	-	-	0.76	-	-	kHz
GA_PESVT	body factor long channel @ L=10µm, W=10µm	-	-	0.65	-	-	√V
IDSPEVTS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.21µm, W=10µm	145	190	235	280	325	µA/µm
IOFPESVTS	off-state leakage @ VD=-1.8V, L=0.21µm, W=10µm	-	-	-	40	-	pA/µm
KP_PESVT	gain factor long channel @ L=10µm, W=10µm	-	-	61	-	-	µA/V²
LEFPESVT	effective channel length @ L=0.21µm	-	-	0.16	-	-	µm
NOIPESVT	input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	12.3	-	-	µVµm/√(Hz)
STSPESVT	subthreshold slope @ VD=-1.8V	-	-	11.7	-	-	decade/V
TC_VTXPESVT	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.79	-	-	mV/K
U0_PESVT	effective mobility	-	-	69.5	-	-	cm²/(Vs)
VTIPESVTL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.57	-0.54	-0.51	-0.48	-0.45	V
VTIPESVTS	threshold voltage short channel @ VD=-0.1V, L=0.21µm, W=10µm	-0.58	-0.52	-0.46	-0.4	-0.34	V
VTIPESVTSS	threshold voltage small channel @ VD=-0.1V, L=0.21µm, W=0.22µm	-	-	-0.47	-	-	V
VTXPESVTS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.21µm, W=10µm	-	-	-0.46	-	-	V
WEFPESVT	effective channel width @ W=0.22µm	-	-	0.23	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPESVT	pelgrom coefficient gain factor mismatch	0.76	%µm
AIDPESVT00	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0V	7.08	%µm
AIDPESVT01	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.1V	4.6	%µm
AIDPESVT02	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.2V	3.11	%µm
AIDPESVT04	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.4V	1.8	%µm
AIDPESVT06	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.6V	1.28	%µm
AIDPESVT08	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.8V	1	%µm
AIDPESVT10	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1V	0.84	%µm
AIDPESVT14	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1.4V	0.66	%µm
AVTPESVT	pelgrom coefficient threshold voltage mismatch	4.24	mVµm

3. Parameters → 3.14 SVT module→ 3.14.1 Device parameters→ pesvt, pesvt_5→ Matching parameters

Name	Description	Typ	Unit
DLTPESVT	transistor delta length	0.05	μm
DWTPESVT	transistor delta width	-0.01	μm

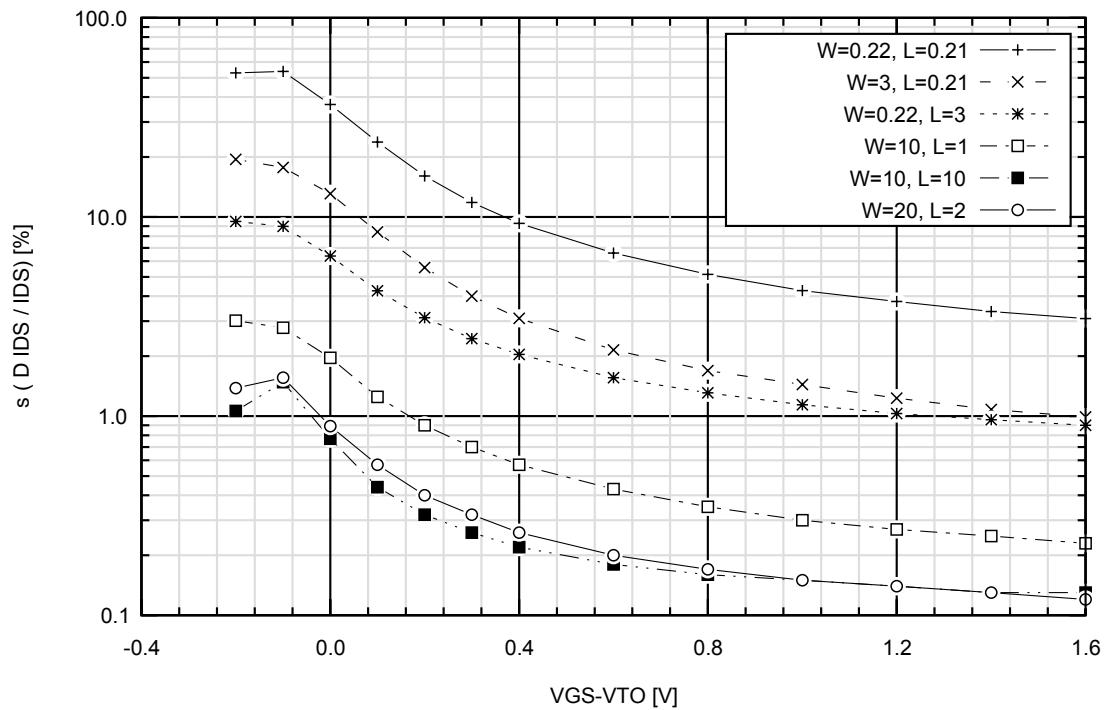


Figure 3.33 Device pesvt: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.15 BJTA module

3.15 BJTA module

3.15.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_NB	NBASE junction depth	2.4	μm

3.15.2 Device parameters

qpv5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	5.5	7	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	5.5	7	V
VC-HW ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BCEOPV5	collector to emitter breakdown voltage (base open) @ Ic=1μA	8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEBOPV5	emitter to base breakdown voltage (collector open) @ Ie=-1μA	-	8	-	-	-	V
BECOPV5	emitter to collector breakdown voltage (base open) @ Ie=-1μA	-	8	-	-	-	V
EVFPV5	early voltage forward @ Ib=-100nA	-	-	50	-	-	V
FT_PV5	transit frequency @ VCE=6V, LE=3μm	-	-	220	-	-	MHz
HFHPV5	forward current gain @ Ie=100μA, LE=10μm	-	-	25	-	-	-
HFLPV5	forward current gain @ Ie=100pA, LE=10μm	-	-	70	-	-	-
HF_PV5	forward current gain @ Ie=1μA, LE=10μm	51	63	75	87	99	-
TC_VBEPV5	base- emitter voltage temperature coefficient	-	-	-2.3	-	-	mV/K
VBEPV5	base-emitter voltage @ Ie=1μA, LE=10μm	584	589	594	599	604	mV

Matching parameters

Name	Description	Typ	Unit
SIBPV5101	standard deviation base current mismatch @ Ic=100nA, LE=10μm	0.85	%
SIBPV5102	standard deviation base current mismatch @ Ic=100μA, LE=10μm	0.68	%
SIBPV5201	standard deviation base current mismatch @ Ic=100nA, LE=20μm	0.75	%
SIBPV5202	standard deviation base current mismatch @ Ic=100μA, LE=20μm	0.58	%
SIBPV5501	standard deviation base current mismatch @ Ic=100nA, LE=50μm	0.64	%

3. Parameters → 3.15 BJTA module→ 3.15.2 Device parameters→ qpv5→ Matching parameters

Name	Description	Typ	Unit
SIBPV5502	standard deviation base current mismatch @ $I_c=100\mu A$, $LE=50\mu m$	0.5	%
SICPV5101	standard deviation collector current mismatch @ $I_c=100nA$, $LE=10\mu m$	0.68	%
SICPV5102	standard deviation collector current mismatch @ $I_c=100\mu A$, $LE=10\mu m$	0.25	%
SICPV5201	standard deviation collector current mismatch @ $I_c=100nA$, $LE=20\mu m$	0.65	%
SICPV5202	standard deviation collector current mismatch @ $I_c=100\mu A$, $LE=20\mu m$	0.29	%
SICPV5501	standard deviation collector current mismatch @ $I_c=100nA$, $LE=50\mu m$	0.52	%
SICPV5502	standard deviation collector current mismatch @ $I_c=100\mu A$, $LE=50\mu m$	0.31	%
SVBPV5101	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=10\mu m$	0.1	mV
SVBPV5102	standard deviation base emitter voltage mismatch @ $I_c=100\mu A$, $LE=10\mu m$	0.23	mV
SVBPV5201	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=20\mu m$	0.07	mV
SVBPV5202	standard deviation base emitter voltage mismatch @ $I_c=100\mu A$, $LE=20\mu m$	0.22	mV
SVBPV5501	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=50\mu m$	0.06	mV
SVBPV5502	standard deviation base emitter voltage mismatch @ $I_c=100\mu A$, $LE=50\mu m$	0.2	mV

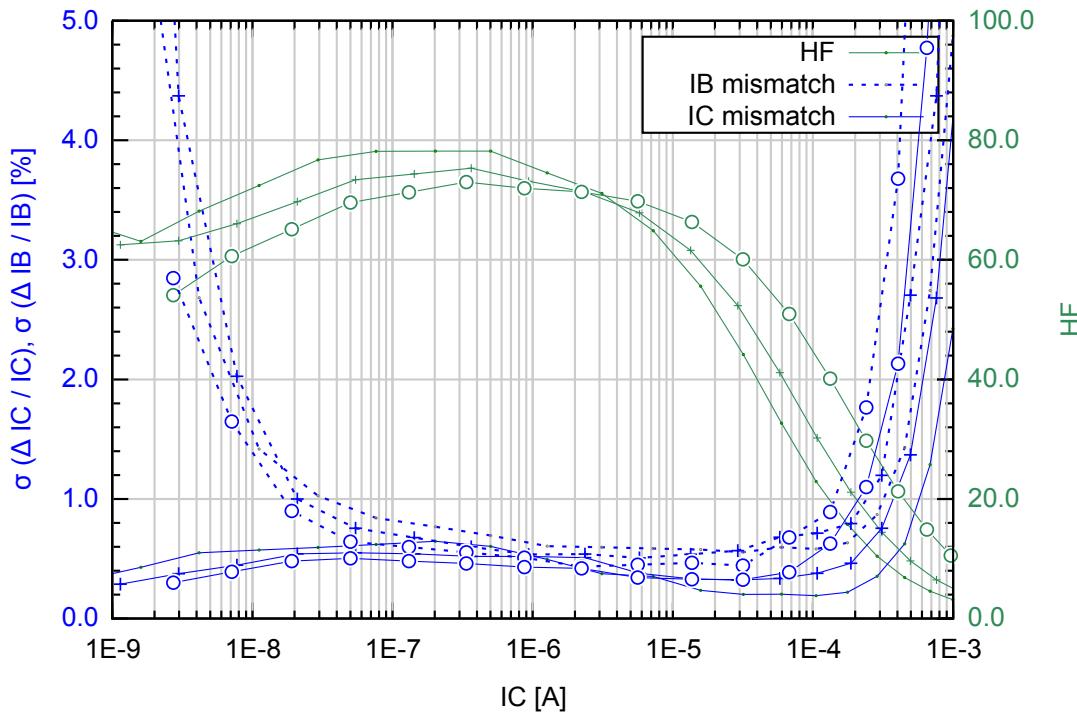


Figure 3.34 Device qpv5: IC matching and IB matching vs. IC
(typical values) ----- $LE=10\mu m$, ---+--- $LE=20\mu m$, --o-- $LE=50\mu m$

qpvha**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-28	-25	5.5	7	V
VEB	-40°C to 175°C	-7	-5.5	1.5	-	V
VBC	-40°C to 175°C	-0.5	0	25	28	V
VC-HW ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V

Note 1 This operating condition will not be checked by automatic check tools.

3. Parameters → 3.15 BJTA module→ 3.15.2 Device parameters→ qpvha→ Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BCEOPVHA	collector to emitter breakdown voltage (base open) @ $I_c=1\mu A$	35	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEBOPVHA	emitter to base breakdown voltage (collector open) @ $I_e=-1\mu A$	-	8	-	-	-	V
BECOPVHA	emitter to collector breakdown voltage (base open) @ $I_e=-1\mu A$	-	8	-	-	-	V
EVFPVHA	early voltage forward @ $I_b=-100nA$	-	-	163	-	-	V
FT_PVHA	transit frequency @ $V_{CE}=6V$, $LE=3\mu m$	-	-	100	-	-	MHz
HFHPVHA	forward current gain @ $I_e=100\mu A$, $LE=10\mu m$	-	-	19	-	-	-
HFLPVHA	forward current gain @ $I_e=100pA$, $LE=10\mu m$	-	-	69	-	-	-
HF_PVHA	forward current gain @ $I_e=1\mu A$, $LE=10\mu m$	51	63	75	87	99	-
TC_VBEPVHA	base- emitter voltage temperature coefficient	-	-	-2.3	-	-	mV/K
VBEPVHA	base-emitter voltage @ $I_e=1\mu A$, $LE=10\mu m$	584	589	594	599	604	mV

Matching parameters

Name	Description	Typ	Unit
SIBPVHA101	standard deviation base current mismatch @ $I_c=100nA$, $LE=10\mu m$	0.66	%
SIBPVHA102	standard deviation base current mismatch @ $I_c=10\mu A$, $LE=10\mu m$	0.37	%
SIBPVHA201	standard deviation base current mismatch @ $I_c=100nA$, $LE=20\mu m$	0.42	%
SIBPVHA202	standard deviation base current mismatch @ $I_c=10\mu A$, $LE=20\mu m$	0.3	%
SIBPVHA501	standard deviation base current mismatch @ $I_c=100nA$, $LE=50\mu m$	0.37	%
SIBPVHA502	standard deviation base current mismatch @ $I_c=10\mu A$, $LE=50\mu m$	0.19	%
SICPVHA101	standard deviation collector current mismatch @ $I_c=100nA$, $LE=10\mu m$	0.28	%
SICPVHA102	standard deviation collector current mismatch @ $I_c=10\mu A$, $LE=10\mu m$	0.25	%
SICPVHA201	standard deviation collector current mismatch @ $I_c=100nA$, $LE=20\mu m$	0.17	%
SICPVHA202	standard deviation collector current mismatch @ $I_c=10\mu A$, $LE=20\mu m$	0.12	%
SICPVHA501	standard deviation collector current mismatch @ $I_c=100nA$, $LE=50\mu m$	0.13	%
SICPVHA502	standard deviation collector current mismatch @ $I_c=10\mu A$, $LE=50\mu m$	0.16	%
SVBPVHA101	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=10\mu m$	0.17	mV
SVBPVHA102	standard deviation base emitter voltage mismatch @ $I_c=10\mu A$, $LE=10\mu m$	0.11	mV
SVBPVHA201	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=20\mu m$	0.18	mV
SVBPVHA202	standard deviation base emitter voltage mismatch @ $I_c=10\mu A$, $LE=20\mu m$	0.09	mV
SVBPVHA501	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=50\mu m$	0.22	mV
SVBPVHA502	standard deviation base emitter voltage mismatch @ $I_c=10\mu A$, $LE=50\mu m$	0.09	mV

3. Parameters → 3.15 BJTA module→ 3.15.2 Device parameters→ qpvha→ Matching parameters

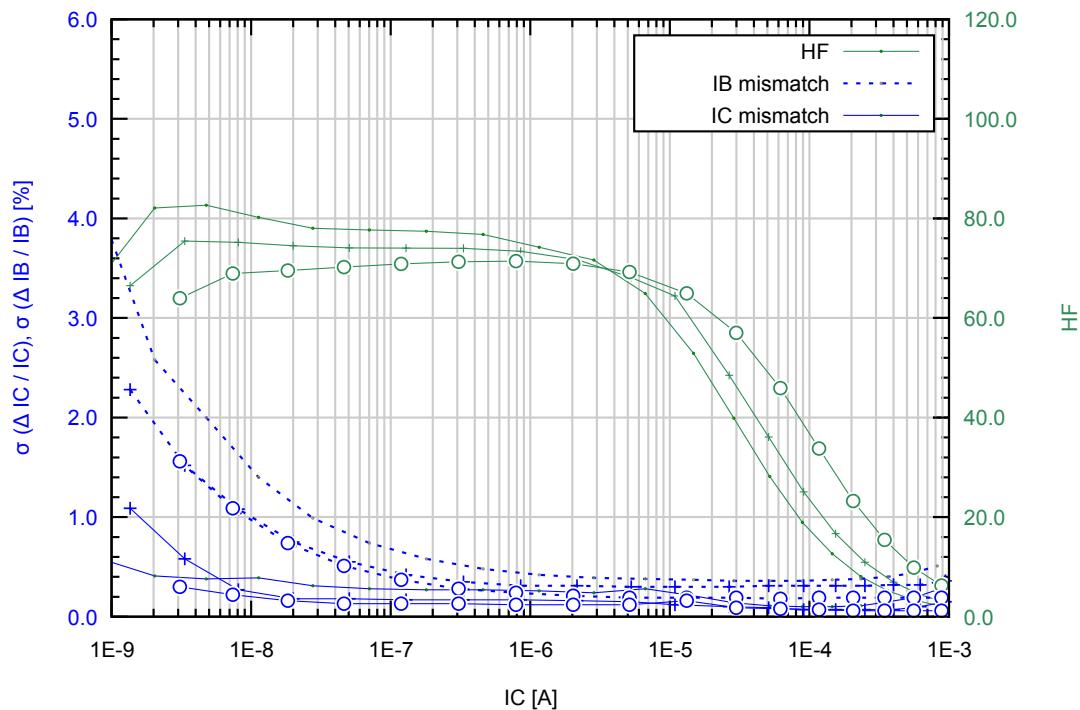


Figure 3.35 Device qpvha: IC matching and IB matching vs. IC
(typical values) ----- LE=10μm, -+-- LE=20μm, --o-- LE=50μm

3. Parameters → 3.16 BJTC module

3.16 BJTC module

3.16.1 Device parameters

qnv5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	5.5	7	V
VEB	-40°C to 175°C	-	-1.5	5.5	7	V
VBC	-40°C to 175°C	-7	-5.5	0	0.5	V
VC-HW ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BCEONV5	collector to emitter breakdown voltage (base open) @ Ic=1µA	8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEBONV5	emitter to base breakdown voltage (collector open) @ Ie=1µA	-	8	-	-	-	V
BECONV5	emitter to collector breakdown voltage (base open) @ Ie=1µA	-	8	-	-	-	V
EVFNV5	early voltage forward @ Ib=100nA	-	-	35	-	-	V
FT_NV5	transit frequency @ VCE=6V, LE=3µm	-	-	950	-	-	MHz
HFHNV5	forward current gain @ Ie=100µA, LE=10µm	-	-	84	-	-	-
HFLNV5	forward current gain @ Ie=1nA, LE=10µm	-	-	45	-	-	-
HF_NV5	forward current gain @ Ie=1µA, LE=10µm	50	70	90	110	130	-
TC_VBENV5	base-emitter voltage temperature coefficient	-	-	-2.3	-	-	mV/K
VBENV5	base-emitter voltage @ Ie=-1µA, LE=10µm	591	596	601	606	611	mV

Matching parameters

Name	Description	Typ	Unit
SIBNV5201	standard deviation base current mismatch @ Ic=100nA, LE=20µm	0.95	%
SIBNV5202	standard deviation base current mismatch @ Ic=100µA, LE=20µm	0.61	%
SIBNV531	standard deviation base current mismatch @ Ic=100nA, LE=3µm	1.7	%
SIBNV532	standard deviation base current mismatch @ Ic=100µA, LE=3µm	0.78	%
SIBNV5501	standard deviation base current mismatch @ Ic=100nA, LE=50µm	0.88	%
SIBNV5502	standard deviation base current mismatch @ Ic=100µA, LE=50µm	0.58	%
SICNV5201	standard deviation collector current mismatch @ Ic=100nA, LE=20µm	0.63	%
SICNV5202	standard deviation collector current mismatch @ Ic=100µA, LE=20µm	0.49	%
SICNV531	standard deviation collector current mismatch @ Ic=100nA, LE=3µm	0.63	%
SICNV532	standard deviation collector current mismatch @ Ic=100µA, LE=3µm	0.57	%
SICNV5501	standard deviation collector current mismatch @ Ic=100nA, LE=50µm	0.53	%

⇒

3. Parameters → 3.16 BJTC module→ 3.16.1 Device parameters→ qnv5→ Matching parameters

Name	Description	Typ	Unit
SICNV5502	standard deviation collector current mismatch @ $I_c=100\mu A$, $LE=50\mu m$	0.34	%
SVBNV5201	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=20\mu m$	0.08	mV
SVBNV5202	standard deviation base emitter voltage mismatch @ $I_c=100\mu A$, $LE=20\mu m$	0.32	mV
SVBNV531	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=3\mu m$	0.14	mV
SVBNV532	standard deviation base emitter voltage mismatch @ $I_c=100\mu A$, $LE=3\mu m$	0.34	mV
SVBNV5501	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=50\mu m$	0.07	mV
SVBNV5502	standard deviation base emitter voltage mismatch @ $I_c=100\mu A$, $LE=50\mu m$	0.3	mV

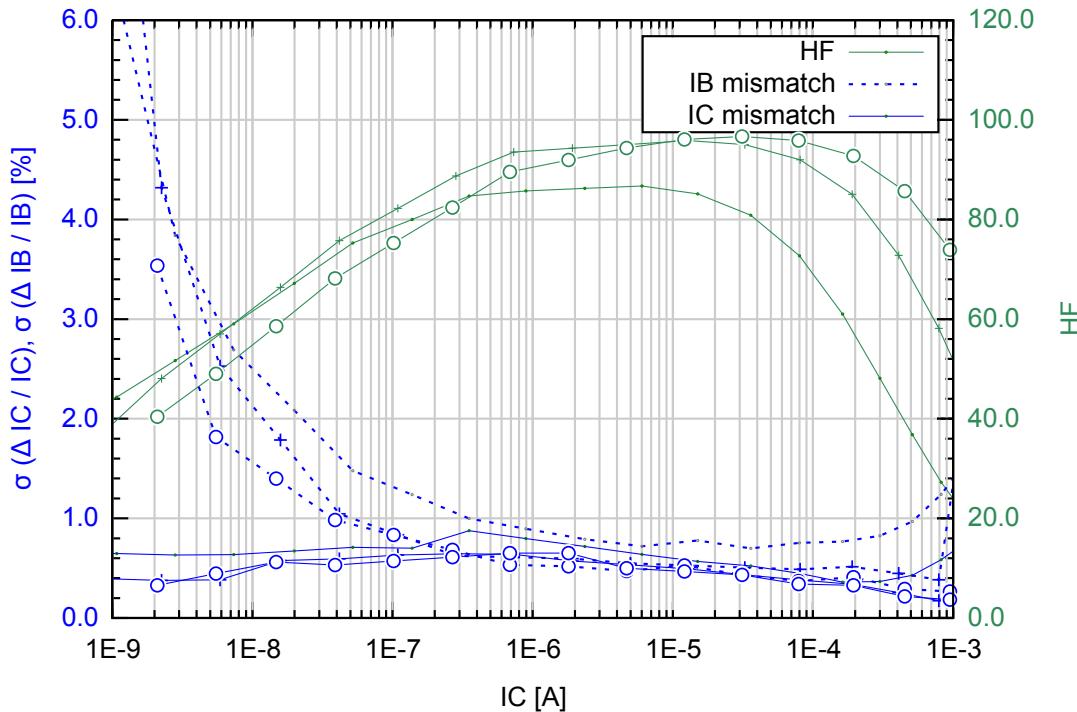


Figure 3.36 Device qnv5: IC matching and IB matching vs. IC
(typical values) ----- LE=3μm, ---+--- LE=20μm, --o-- LE=50μm

qnvha

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-7	-5.5	25	28	V
VEB	-40°C to 175°C	-	-1.5	5.5	7	V
VBC	-40°C to 175°C	-28	-25	0	0.5	V
VC-HW ⁽¹⁾	-40°C to 175°C	-110	-100	100	110	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BCEONVHA	collector to emitter breakdown voltage (base open) @ $I_c=1\mu A$	35	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

⇒

3. Parameters → 3.16 BJTC module→ 3.16.1 Device parameters→ qnvha→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BEBONVHA	emitter to base breakdown voltage (collector open) @ $I_e=1\mu A$	-	8	-	-	-	V
BECNVHA	emitter to collector breakdown voltage (base open) @ $I_e=1\mu A$	-	8	-	-	-	V
EVFNVHA	early voltage forward @ $I_b=100nA$	-	-	180	-	-	V
FT_NVHA	transit frequency @ $V_{CE}=6V$, $LE=3\mu m$	-	-	660	-	-	MHz
HFHNVHA	forward current gain @ $I_e=100\mu A$, $LE=10\mu m$	-	-	73	-	-	-
HFLNVHA	forward current gain @ $I_e=1nA$, $LE=10\mu m$	-	-	45	-	-	-
HF_NVHA	forward current gain @ $I_e=1\mu A$, $LE=10\mu m$	50	70	90	110	130	-
TC_VBENVHA	base- emitter voltage temperature coefficient	-	-	-2.2	-	-	mV/K
VBNVHA	base-emitter voltage @ $I_e=-1\mu A$, $LE=10\mu m$	591	596	601	606	611	mV

Matching parameters

Name	Description	Typ	Unit
SIBNVHA201	standard deviation base current mismatch @ $I_c=100nA$, $LE=20\mu m$	0.69	%
SIBNVHA202	standard deviation base current mismatch @ $I_c=10\mu A$, $LE=20\mu m$	0.28	%
SIBNVHA31	standard deviation base current mismatch @ $I_c=100nA$, $LE=3\mu m$	0.98	%
SIBNVHA32	standard deviation base current mismatch @ $I_c=10\mu A$, $LE=3\mu m$	0.63	%
SIBNVHA501	standard deviation base current mismatch @ $I_c=100nA$, $LE=50\mu m$	0.66	%
SIBNVHA502	standard deviation base current mismatch @ $I_c=10\mu A$, $LE=50\mu m$	0.23	%
SICNVHA201	standard deviation collector current mismatch @ $I_c=100nA$, $LE=20\mu m$	0.21	%
SICNVHA202	standard deviation collector current mismatch @ $I_c=10\mu A$, $LE=20\mu m$	0.19	%
SICNVHA31	standard deviation collector current mismatch @ $I_c=100nA$, $LE=3\mu m$	0.44	%
SICNVHA32	standard deviation collector current mismatch @ $I_c=10\mu A$, $LE=3\mu m$	0.39	%
SICNVHA501	standard deviation collector current mismatch @ $I_c=100nA$, $LE=50\mu m$	0.16	%
SICNVHA502	standard deviation collector current mismatch @ $I_c=10\mu A$, $LE=50\mu m$	0.16	%
SVBNVHA201	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=20\mu m$	0.06	mV
SVBNVHA202	standard deviation base emitter voltage mismatch @ $I_c=10\mu A$, $LE=20\mu m$	0.44	mV
SVBNVHA31	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=3\mu m$	0.12	mV
SVBNVHA32	standard deviation base emitter voltage mismatch @ $I_c=10\mu A$, $LE=3\mu m$	0.3	mV
SVBNVHA501	standard deviation base emitter voltage mismatch @ $I_c=100nA$, $LE=50\mu m$	0.05	mV
SVBNVHA502	standard deviation base emitter voltage mismatch @ $I_c=10\mu A$, $LE=50\mu m$	0.37	mV

3. Parameters → 3.16 BJTC module→ 3.16.1 Device parameters→ qnvha→ Matching parameters

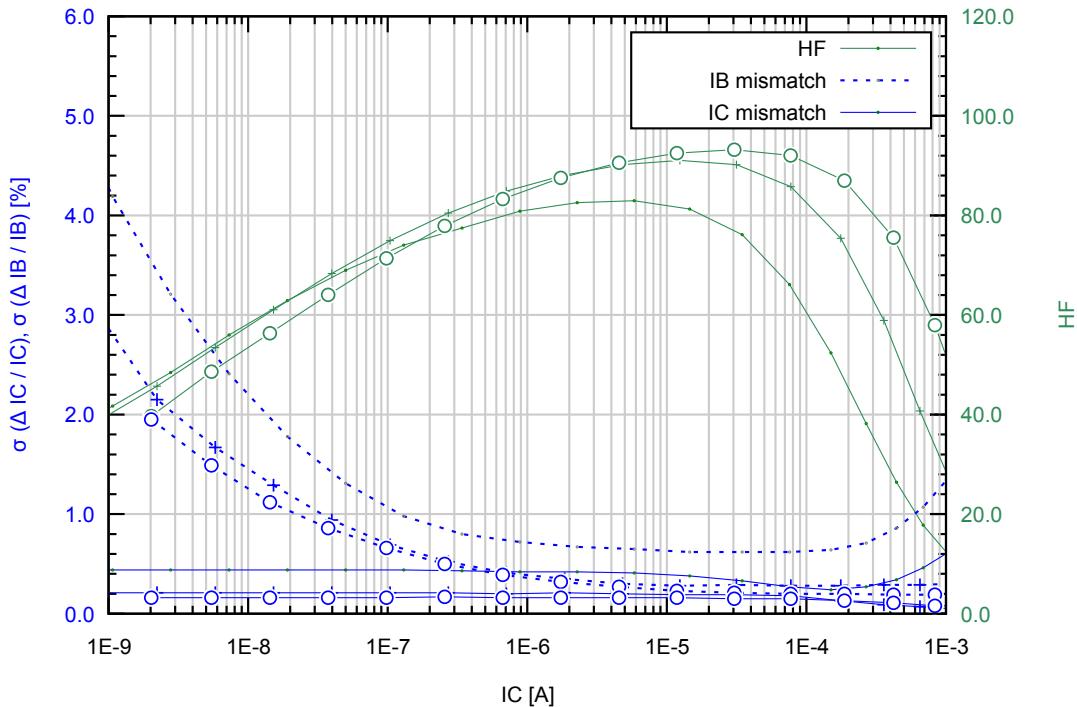


Figure 3.37 Device qnvha: IC matching and IB matching vs. IC (typical values)
--- LE=3µm, -+-- LE=20µm, --o-- LE=50µm

3. Parameters → 3.17 DEPL module

3.17 DEPL module

3.17.1 Device parameters

nd5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	5.5	7	V
VDS	-40°C to 175°C	-7	-5.5	5.5	7	V
VDB	-40°C to 175°C	-0.5	0	5.5	7	V
VSB	-40°C to 175°C	-0.5	0	5.5	7	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSND5S	drain-source breakdown @ VG=-4V, Id=1µA, L=0.7µm	8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BEXND5	mobility exponent	-	-	-1.58	-	-	-
FC_ND5	corner frequency @ VD=5V, Id=1µA	-	-	1.15	-	-	kHz
GAMND5	body factor long channel @ L=10µm, W=10µm	-	-	0.526	-	-	√V
ID0ND5S3	saturation current @ VG=0V, VD=3V, L=0.7µm, W=10µm	35	55	74	93	113	µA/µm
IDLND5L0	drain current in linear region @ VG=0V, VD=0.1V, L=10µm, W=10µm	-	-	0.75	-	-	µA/µm
IDLND5S0	drain current in linear region @ VG=0V, VD=0.1V, L=0.7µm, W=10µm	-	-	11.8	-	-	µA/µm
ISBND5S	bulk current @ VD=5V, L=0.7µm	-	-	2	-	-	µA/µm
LEFND5	effective length (transistor) @ L=0.7µm	-	-	0.81	-	-	µm
NOIND5	input referred noise @ VD=5V, Id=1µA, f=1Hz, L=10µm, W=10µm	-	-	18.3	-	-	µVµm/√(Hz)
TC_VTIND5	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	-2.3	-	-	mV/K
U0_ND5	effective mobility	-	-	378	-	-	cm²/(Vs)
VTIND5L	threshold voltage long channel @ VD=0.1V, L=10µm, W=10µm	-	-	-1.65	-	-	V
VTIND5S	threshold voltage short channel @ VD=0.1V, L=0.7µm, W=10µm	-2.14	-1.84	-1.54	-1.24	-0.94	V
WEFND5	transistor effective width @ W=0.44µm	-	-	0.375	-	-	µm

3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ nd5→ Matching parameters

Matching parameters

Name	Description	Typ	Unit
ABTND5	pelgrom coefficient gain factor mismatch	0.85	%μm
AIDND500	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	8.15	%μm
AIDND502	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	6.41	%μm
AIDND504	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	5.17	%μm
AIDND506	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.24	%μm
AIDND510	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.98	%μm
AIDND520	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.52	%μm
AIDND530	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.01	%μm
AIDND550	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.64	%μm
AVTND5	pelgrom coefficient threshold voltage mismatch	20.23	mVμm
DLTND5	transistor delta length	-0.11	μm
DWTND5	transistor delta width	0.065	μm

ndmvd

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-22	-20	5.5	7	V
VDS	-40°C to 175°C	-0.5	0	20	22	V
VDB	-40°C to 175°C	-0.5	0	20	22	V
VD-HW	-40°C to 175°C	-27	-25	400	440	V

Process parameters

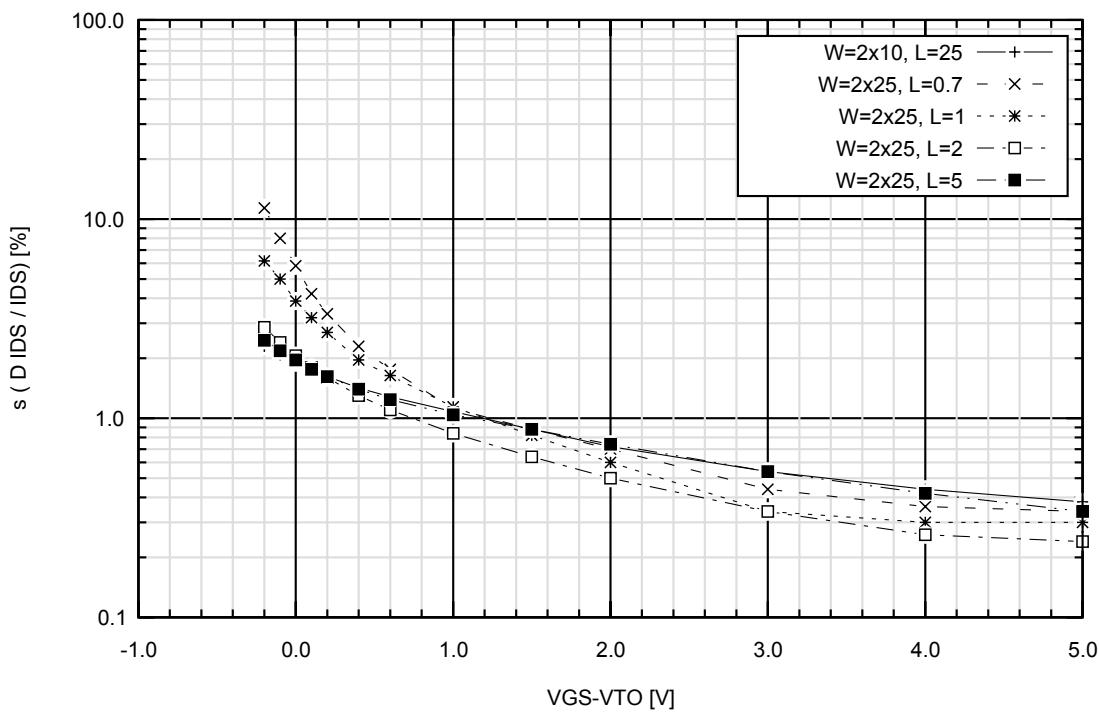
Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNDMVD	drain-source breakdown @ VG=-4V, Id=1μA, L=0.7μm	23	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID0NDMVDS	saturation current @ VG=0V, VD=5V, L=0.7μm, W=100μm, NF=4, WF=25μm	36	46.5	57	67.5	78	μA/μm
IDLNDMVDL0	drain current in linear region @ VG=0V, VD=0.1V, L=5μm, W=50μm, NF=2, WF=25μm	-	-	1.32	-	-	μA/μm
ROANDMVD0	area specific on resistance @ VG=0V, VD=0.1V, L=0.7μm, W=100μm, Pitch=2.24μm, NF=4, WF=25μm	-	-	34.6	-	-	mΩmm²
RONNDMVD0	on resistance @ VG=0V, VD=0.1V, L=0.7μm, W=100μm, NF=4, WF=25μm	12.3	13.9	15.5	17.1	18.7	kΩμm
TC_VTINDMVD	threshold voltage temperature coefficient @ L=5μm, W=50μm, NF=2, WF=25μm	-	-	-2.2	-	-	mV/K
VT1NDMVD	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=40μm	-	-	26	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							

3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndmvd→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VTINDMVDL	threshold voltage long channel @ VD=0.1V, L=5µm, W=50µm, NF=2, WF=25µm	-	-	-1.64	-	-	V
VTINDMVDS	threshold voltage short channel @ VD=0.1V, L=0.7µm, W=100µm, NF=4, WF=25µm	-1.88	-1.68	-1.48	-1.28	-1.08	V

Matching parameters

Name	Description	Typ	Unit
ABTNDMVD	pelgrom coefficient gain factor mismatch	2.14	%µm
AIDNDMVD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	22.52	%µm
AIDNDMVD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	15.66	%µm
AIDNDMVD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	12.16	%µm
AIDNDMVD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	9.7	%µm
AIDNDMVD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	7.46	%µm
AIDNDMVD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	5.06	%µm
AIDNDMVD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	3.62	%µm
AIDNDMVD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	2.68	%µm
AVTNDMVD	pelgrom coefficient threshold voltage mismatch	31.7	mVµm
DLTNDMVD	transistor delta length	0	µm
DWTNDMVD	transistor delta width	0	µm

**Figure 3.38** Device ndmvd: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndmvf→ Operating conditions

ndmvf

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-35	-32	5.5	7	V
VDS	-40°C to 175°C	-0.5	0	32	35	V
VDB	-40°C to 175°C	-0.5	0	32	35	V
VD-HW	-40°C to 175°C	-27	-25	400	440	V

Process parameters

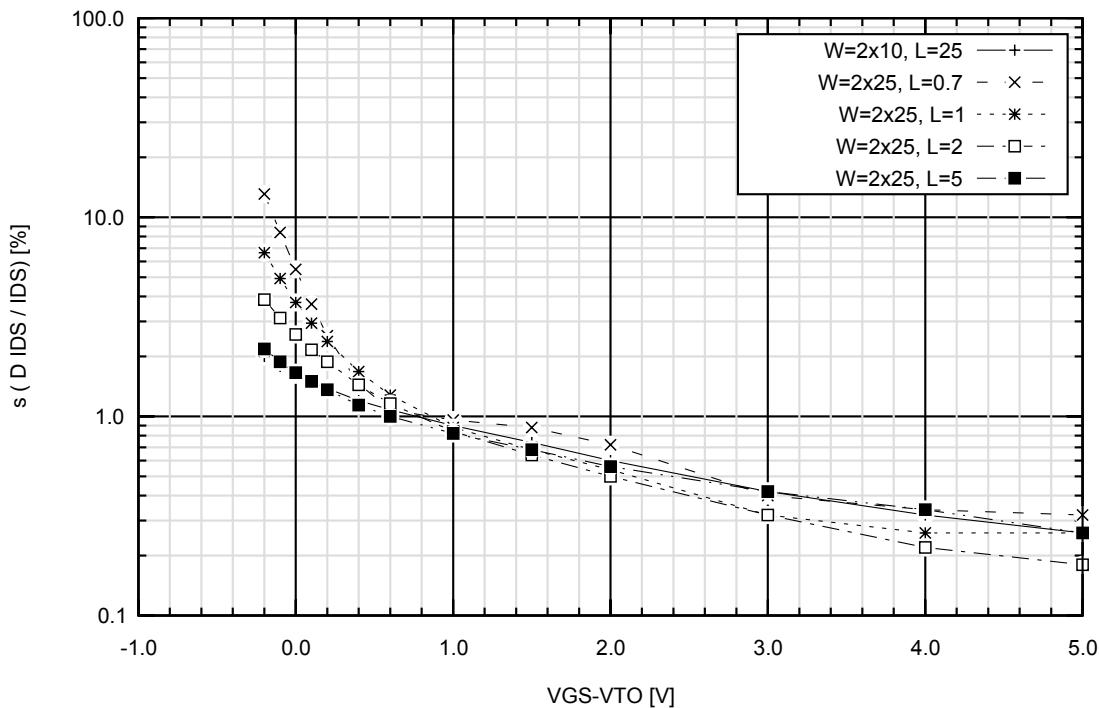
Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNDMVF	drain-source breakdown @ VG=-4V, Id=1µA, L=0.7µm	37	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID0NDMVFS	saturation current @ VG=0V, VD=5V, L=0.7µm, W=100µm, NF=4, WF=25µm	34	44.5	55	65.5	76	µA/µm
IDLNDMVFL0	drain current in linear region @ VG=0V, VD=0.1V, L=5µm, W=50µm, NF=2, WF=25µm	-	-	1.29	-	-	µA/µm
ROANDMVF0	area specific on resistance @ VG=0V, VD=0.1V, L=0.7µm, W=100µm, Pitch=3.06µm, NF=4, WF=25µm	-	-	53.5	-	-	mΩmm²
RONNDMVF0	on resistance @ VG=0V, VD=0.1V, L=0.7µm, W=100µm, NF=4, WF=25µm	13.9	15.7	17.5	19.3	21.1	kΩµm
TC_VTINDMVF	threshold voltage temperature coefficient @ L=5µm, W=50µm, NF=2, WF=25µm	-	-	-2.2	-	-	mV/K
VT1NDMVF	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=40µm	-	-	38	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"						
VTINDMVF	threshold voltage long channel @ VD=0.1V, L=5µm, W=50µm, NF=2, WF=25µm	-	-	-1.63	-	-	V
VTINDMVFS	threshold voltage short channel @ VD=0.1V, L=0.7µm, W=100µm, NF=4, WF=25µm	-1.86	-1.66	-1.46	-1.26	-1.06	V

Matching parameters

Name	Description	Typ	Unit
ABTNDMVF	pelgrom coefficient gain factor mismatch	2.17	%µm
AIDNDMVF00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	23.86	%µm
AIDNDMVF02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	16.64	%µm
AIDNDMVF04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	12.7	%µm
AIDNDMVF06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	10.36	%µm
AIDNDMVF10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	7.94	%µm
AIDNDMVF20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	5.32	%µm
AIDNDMVF30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	3.54	%µm

3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndmvf→ Matching parameters

Name	Description	Typ	Unit
AIDNDMVF50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	2.22	%μm
AVTNDMVF	pelgrom coefficient threshold voltage mismatch	36.16	mVμm
DLTNDMVF	transistor delta length	0	μm
DWTNDMVF	transistor delta width	0	μm

**Figure 3.39** Device ndmvf: drain current matching vs. VGS-VTO (typical values, drawn W and L)**ndhvt****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-42	-40	5.5	7	V
VDS	-40°C to 175°C	-0.5	0	40	42	V
VDB	-40°C to 175°C	-0.5	0	40	42	V
VD-HW	-40°C to 175°C	-110	-100	200	220	V

Note: The node B (BULK) is: PWELL4**Process parameters**

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNDHVT	drain-source breakdown @ VG=-4V, Id=1μA, L=0.5μm	50	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID0NDHVT	saturation current @ VG=0V, VD=10V, L=0.5μm, W=100μm, NF=4, WF=25μm	8	18.5	29	39.5	50	μA/μm



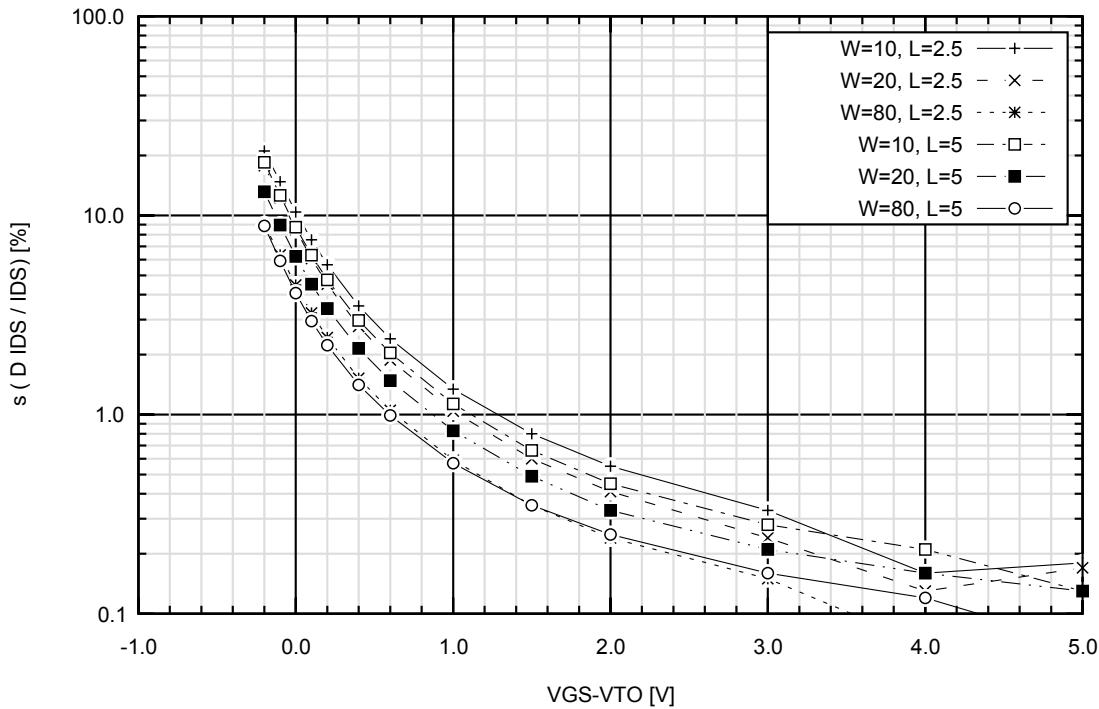
3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndhvt→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDLNNDHVTL0	drain current in linear region @ VG=0V, VD=0.1V, L=5µm, W=100µm, NF=4, WF=25µm	-	-	1.2	-	-	µA/µm
ROANDHVT0	area specific on resistance @ VG=0V, VD=0.1V, L=0.5µm, W=100µm, Pitch=4.29µm, NF=4, WF=25µm	-	-	116	128	-	mΩmm ²
RONNDHVT0	on resistance @ VG=0V, VD=0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	19.2	23.1	27	30.9	34.8	kΩµm
TC_VTINDHVT	threshold voltage temperature coefficient @ L=5µm, W=100µm, NF=4, WF=25µm	-	-	-2.5	-	-	mV/K
VT1NDHVT	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80µm	-	-	55	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTINDHVT	threshold voltage short channel @ VD=0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-1.35	-1.14	-0.93	-0.72	-0.51	V
VTINDHVTL	threshold voltage long channel @ VD=0.1V, L=5µm, W=100µm, NF=4, WF=25µm	-	-	-1.26	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTNDHVT	pelgrom coefficient gain factor mismatch	2.33	%µm
AIDNDHVT00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	58	%µm
AIDNDHVT02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	31.5	%µm
AIDNDHVT04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	19.6	%µm
AIDNDHVT06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	13.4	%µm
AIDNDHVT10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	7.5	%µm
AIDNDHVT20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	3	%µm
AIDNDHVT30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.9	%µm
AIDNDHVT50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1	%µm
AVTNDHVT	pelgrom coefficient threshold voltage mismatch	38.86	mVµm
DLTNDHVT	transistor delta length	0	µm
DWTNDHVT	transistor delta width	0	µm

3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndhvvt→ Matching parameters

**Figure 3.40** Device ndhvvt: drain current matching vs. VGS-VTO (typical values, drawn W and L)**ndhvta****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-42	-40	5.5	7	V
VDS	-40°C to 175°C	-0.5	0	40	42	V
VDB	-40°C to 175°C	-0.5	0	40	42	V
VD-HW	-40°C to 175°C	-110	-100	200	220	V

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNDHVTA	drain-source breakdown @ VG=-4V, Id=1µA, L=0.4µm	42	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID0NDHVTA	saturation current @ VG=0V, VD=10V, L=0.4µm, W=100µm, NF=4, WF=25µm	6	18	30	42	54	µA/µm
IDLNDHVTAL0	drain current in linear region @ VG=0V, VD=0.1V, L=1.5µm, W=100µm, NF=4, WF=25µm	-	-	2.6	-	-	µA/µm
ROANDHVTA0	area specific on resistance @ VG=0V, VD=0.1V, L=0.4µm, W=100µm, Pitch=2.89µm, NF=4, WF=25µm	-	-	65	73.7	-	mΩmm²



3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndhvta→ Process parameters

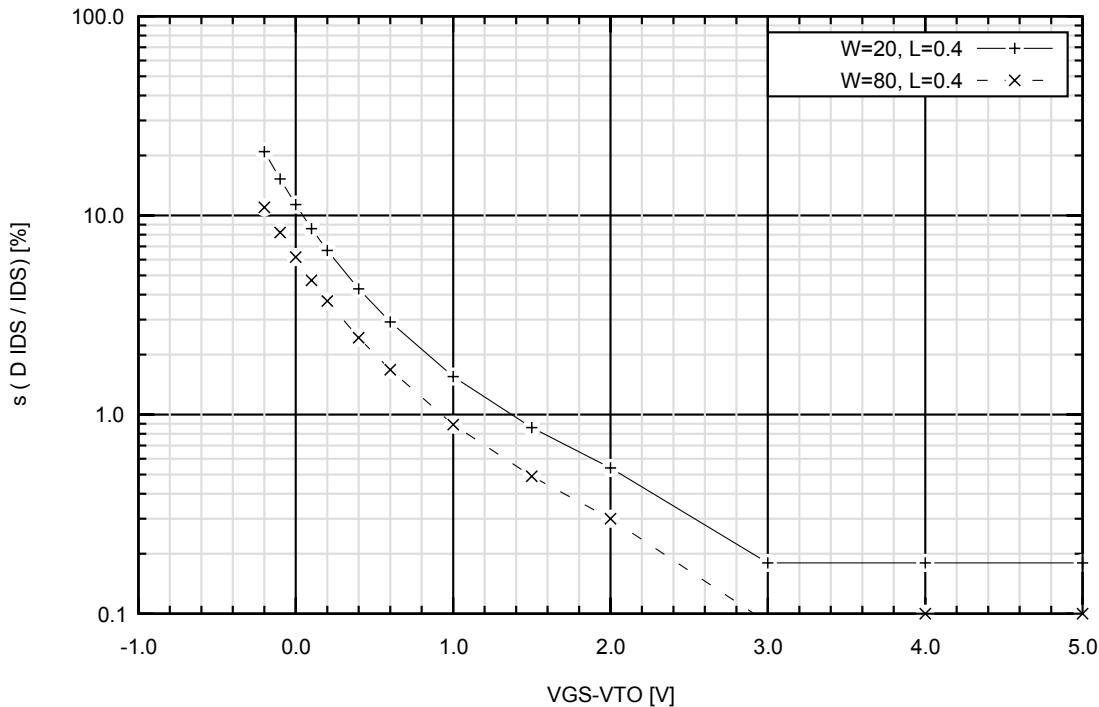
Name	Description	LSL	Low	Typ	High	USL	Unit
RONNDHVTA0	on resistance @ VG=0V, VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	13.5	18	22.5	27	31.5	kΩμm
TC_VTINDHVT	threshold voltage temperature coefficient @ L=1.5μm, W=100μm, NF=4, WF=25μm	-	-	-2.3	-	-	mV/K
VT1NDHVTA	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	45	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"						
VTINDHVT	threshold voltage short channel @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	-1.29	-1.08	-0.87	-0.66	-0.45	V
VTINDHVTAL	threshold voltage long channel @ VD=0.1V, L=1.5μm, W=100μm, NF=4, WF=25μm	-	-	-1.1	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTNDHVTA	pelgrom coefficient gain factor mismatch	2.37	%μm
AIDNDHVTA00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	33.01	%μm
AIDNDHVTA02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	19.43	%μm
AIDNDHVTA04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	12.61	%μm
AIDNDHVTA06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.78	%μm
AIDNDHVTA10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.89	%μm
AIDNDHVTA20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.88	%μm
AIDNDHVTA30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.87	%μm
AIDNDHVTA50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.66	%μm
AVTNDHVTA	pelgrom coefficient threshold voltage mismatch	32.7	mVμm
DLTNDHVTA	transistor delta length	0	μm
DWTNDHVTA	transistor delta width	0	μm

Note: Transistors with channel lengths > 0.5μm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndhvta→ Matching parameters

**Figure 3.41** Device ndhvta: drain current matching vs. VGS-VTO (typical values, drawn W and L)**ndhvtaa****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-42	-40	5.5	7	V
VDS	-40°C to 175°C	-0.5	0	40	42	V
VDB	-40°C to 175°C	-0.5	0	40	42	V
VD-HW	-40°C to 175°C	-110	-100	200	220	V

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNDHVTAA	drain-source breakdown @ VG=-4V, Id=1µA, L=0.4µm	45	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID0NDHVTAA	saturation current @ VG=0V, VD=10V, L=0.4µm, W=100µm, NF=4, WF=25µm	6	18	30	42	54	µA/µm
IDLNDHVTAA0	drain current in linear region @ VG=0V, VD=0.1V, L=1.5µm, W=100µm, NF=4, WF=25µm	-	-	2.6	-	-	µA/µm
ROANDHVTAA0	area specific on resistance @ VG=0V, VD=0.1V, L=0.4µm, W=100µm, Pitch=2.89µm, NF=4, WF=25µm	-	-	65	73.7	-	mΩmm ²



3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndhvtaa→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RONNDHVTAA0	on resistance @ VG=0V, VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	13.5	18	22.5	27	31.5	kΩμm
TC_VTINDHVTAA	threshold voltage temperature coefficient @ L=1.5μm, W=100μm, NF=4, WF=25μm	-	-	-2.3	-	-	mV/K
VT1NDHVTAA	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	45	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTINDHVTAA	threshold voltage short channel @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	-1.29	-1.08	-0.87	-0.66	-0.45	V
VTINDHVTAA	threshold voltage long channel @ VD=0.1V, L=1.5μm, W=100μm, NF=4, WF=25μm	-	-	-1.1	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTNDHVTAA	pelgrom coefficient gain factor mismatch	2.37	%μm
AIDNDHVTAA00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	33.01	%μm
AIDNDHVTAA02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	19.43	%μm
AIDNDHVTAA04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	12.61	%μm
AIDNDHVTAA06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.78	%μm
AIDNDHVTAA10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.89	%μm
AIDNDHVTAA20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.88	%μm
AIDNDHVTAA30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.87	%μm
AIDNDHVTAA50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.66	%μm
AVTNDHVTAA	pelgrom coefficient threshold voltage mismatch	32.7	mVμm
DLTNDHVTAA	transistor delta length	0	μm
DWTNDHVTAA	transistor delta width	0	μm

Note: Transistors with channel lengths > 0.5μm will exhibit greater mismatch of parameters. More information available on request.

Note: Matching parameters are copied over from ndhvta.

3. Parameters → 3.17 DEPL module→ 3.17.1 Device parameters→ ndhvtaa→ Matching parameters

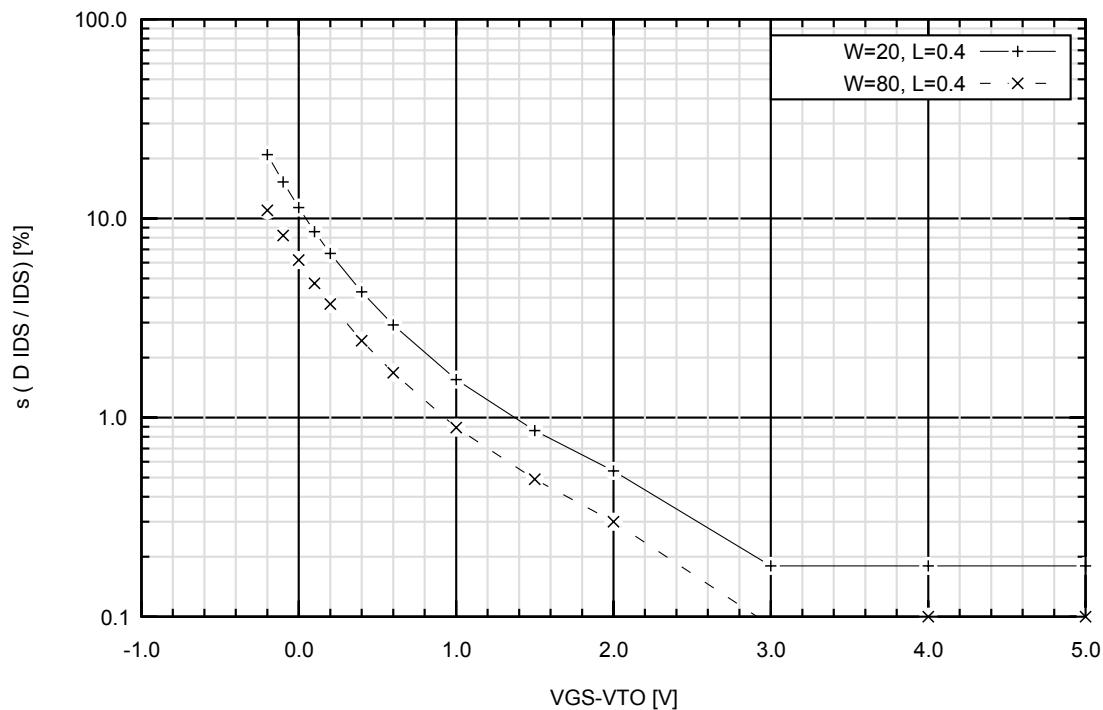


Figure 3.42 Device ndhvta: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.18 HVDEPL module

3.18 HVDEPL module

3.18.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_HVDEPL	HV Depletion junction depth	0.1	μm

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSHVDEPL	HVDEPL sheet resistance (STI terminated) @ W=5μm	9.6	kΩ/□

3.18.2 Device parameters

ndhvrd

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-93	-85	5.5	7	V
VDS	-40°C to 175°C	-0.5	0	85	93	V
VDB	-40°C to 175°C	-0.5	0	85	93	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNDHVRD	drain-source breakdown @ VG=-4V, Id=1μA, L=0.5μm	98	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID0NDHVRDS	saturation current @ VG=0V, VD=10V, L=0.5μm, W=100μm, NF=4, WF=25μm	11	19	27	35	43	μA/μm
IDLNDHVRDL0	drain current in linear region @ VG=0V, VD=0.1V, L=5μm, W=100μm, NF=4, WF=25μm	-	-	1.27	-	-	μA/μm
ROANDHVRD0	area specific on resistance @ VG=0V, VD=0.1V, L=0.5μm, W=100μm, Pitch=6.3μm, NF=4, WF=25μm	-	-	232	255	-	mΩmm ²
RONNDHVRD0	on resistance @ VG=0V, VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	29.7	33.3	36.9	40.5	44.1	kΩμm
TC_VTINDHVRD	threshold voltage temperature coefficient @ L=0.5μm, W=100μm, NF=4, WF=25μm	-	-	-2.3	-	-	mV/K

3. Parameters → 3.18 HVDEPL module→ 3.18.2 Device parameters→ ndhvrд→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VT1NDHVRD	snap-back trigger voltage @ VGS=5V, Ngates=8, WF=40μm	-	-	105	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"						
VTINDHVRDL	threshold voltage long channel @ VD=0.1V, L=5μm, W=100μm, NF=4, WF=25μm	-	-	-1.34	-	-	V
VTINDHVRDS	threshold voltage short channel @ VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	-1.55	-1.34	-1.14	-0.94	-0.73	V

Matching parameters

Name	Description	Typ	Unit
ABTNDHVRD	pelgrom coefficient gain factor mismatch	2.7	%μm
AIDNDHVRD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	46.42	%μm
AIDNDHVRD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	13.68	%μm
AIDNDHVRD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	8.52	%μm
AIDNDHVRD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	7.48	%μm
AIDNDHVRD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	6.82	%μm
AIDNDHVRD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	3.94	%μm
AIDNDHVRD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.44	%μm
AIDNDHVRD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1.52	%μm
AVTNDHVRD	pelgrom coefficient threshold voltage mismatch	36.2	mVμm
DLTNDHVRD	transistor delta length	0	μm
DWTNDHVRD	transistor delta width	0	μm

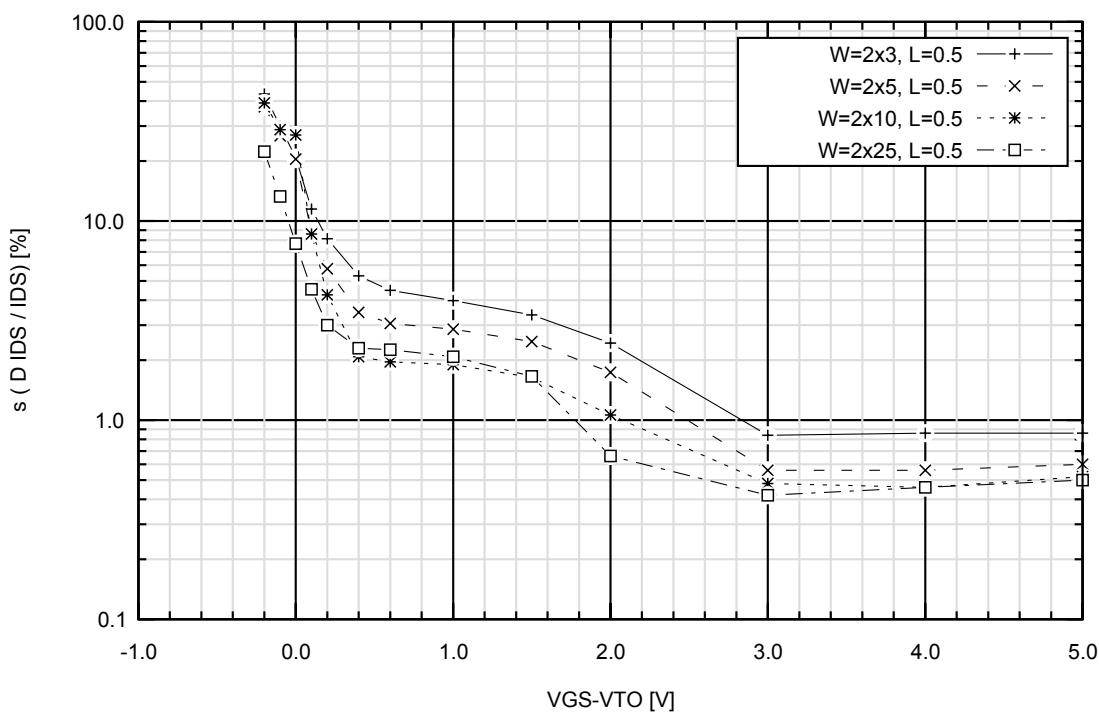


Figure 3.43 Device ndhvrд: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.18 HVDEPL module→ 3.18.2 Device parameters→ ndhvrf→ Operating conditions

ndhvrf

This device is intended to enhance the ESD design window for 100V applications. The ESD design window may not be suitable for applications up to 125V.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-127	-125	5.5	7	V
VDS	-40°C to 175°C	-0.5	0	125	127	V
VDB	-40°C to 175°C	-0.5	0	125	127	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNDHVRF	drain-source breakdown @ VG=-4V, Id=1µA, L=0.5µm	133	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID0NDHVRFS	saturation current @ VG=0V, VD=10V, L=0.5µm, W=100µm, NF=4, WF=25µm	1	9	17	25	33	µA/µm
IDLNDHVRFL0	drain current in linear region @ VG=0V, VD=0.1V, L=5µm, W=100µm, NF=4, WF=25µm	-	-	1.06	-	-	µA/µm
ROANDHVRF0	area specific on resistance @ VG=0V, VD=0.1V, L=0.5µm, W=100µm, Pitch=9.2µm, NF=4, WF=25µm	-	-	474	529	-	mΩmm ²
RONNDHVRF0	on resistance @ VG=0V, VD=0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	40	45.7	51.5	57.3	63	kΩµm
TC_VTINDHVRF	threshold voltage temperature coefficient @ L=0.5µm, W=100µm, NF=4, WF=25µm	-	-	-2.3	-	-	mV/K
VT1NDHVRF	snap-back trigger voltage @ VGS=5V, Ngates=8, WF=40µm	-	-	150	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTINDHVRFL	threshold voltage long channel @ VD=0.1V, L=5µm, W=100µm, NF=4, WF=25µm	-	-	-1.05	-	-	V
VTINDHVRFS	threshold voltage short channel @ VD=0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-1.44	-1.16	-0.88	-0.6	-0.32	V

3. Parameters → 3.19 1XN module

3.19 1XN module

3.19.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_SJNP	SJNP junction depth	1.75	μm

Sheet and contact resistance parameters

Name	Description	Low	Typ	High	Unit
RSRNSJNP	SJNP n-type sheet resistance	4	4.4	4.8	kΩ/□
RSRPSJNP	SJNP p-type sheet resistance	11.5	13	14.5	kΩ/□

3.19.2 Device parameters

nhsj1_7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-110	-100	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	100	110	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	100	110	V
VSB	-40°C to 175°C	-0.5	0	5.5	7	V
VD-HW	-40°C to 175°C	-	-1.5	200	220	V
VD-NB ⁽²⁾	-40°C to 175°C	-110	-100	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS7S	drain-source breakdown @ VG=0V, Id=1μA, L=0.5μm	110	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5NHS7S	saturation current @ VG=5V, VD=30V, L=0.5μm, W=50μm, NF=2, WF=25μm	97	106	115	124	133	μA/μm
IDPNHS7S	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	169	-	-	μA/μm

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3. Parameters → 3.19 1XN module→ 3.19.2 Device parameters→ nhsj1_7→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA_NHS7	area specific on resistance @ VG=5V, VD=0.1V, L=1µm, W=50µm, Pitch=9.5µm, NF=2, WF=25µm	-	-	309	340	-	mΩmm ²
ROA_NHS7S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=50µm, Pitch=9µm, NF=2, WF=25µm	-	-	277	306	-	mΩmm ²
RO_NHS7S	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=50µm, NF=2, WF=25µm	24.2	27.5	30.8	34.1	37.4	kΩµm
TC_VTNHS7S	Threshold voltage temperature coefficient @ L=0.5µm, W=50µm	-	-	-2	-	-	mV/K
VT1_NHSJ1_7	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=100µm	-	-	131	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTX_NHS7	extrapolated threshold voltage @ VD=0.1V, L=1µm, W=50µm, NF=2, WF=25µm	-	-	1.05	-	-	V
VTX_NHS7S	extrapolated threshold voltage @ VD=0.1V, L=0.5µm, W=50µm, NF=2, WF=25µm	1.01	1.08	1.16	1.24	1.31	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHS7	pelgrom coefficient gain factor mismatch	3	%µm
AID_NHS700	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	28	%µm
AID_NHS702	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.3	%µm
AID_NHS704	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	8.19	%µm
AID_NHS706	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	5.52	%µm
AID_NHS710	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	3.35	%µm
AID_NHS720	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.81	%µm
AID_NHS730	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID_NHS750	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.68	%µm
AVT_NHS7	pelgrom coefficient threshold voltage mismatch	17.2	mVµm
DLT_NHS7	transistor delta length	0	µm
DWT_NHS7	transistor delta width	0	µm

Note: Matching data are valid for up to L=1µm. Transistors with channel lengths > 1.0µm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.19 1XN module → 3.19.2 Device parameters → nhsj1_7 → Matching parameters

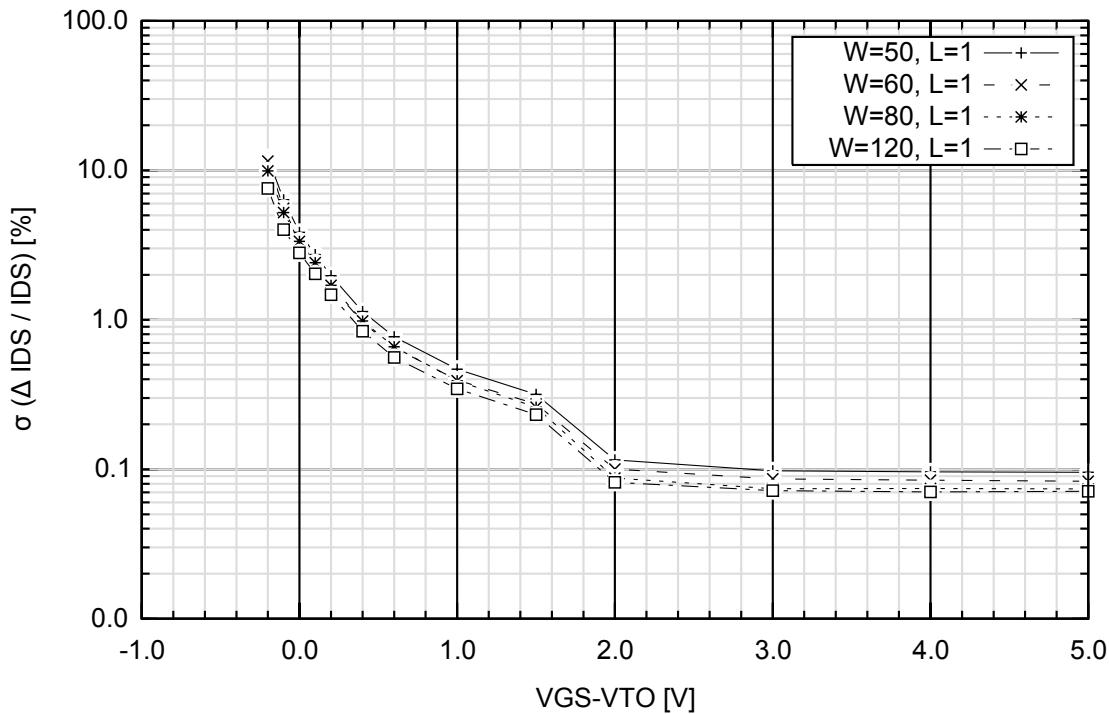


Figure 3.44 Device nhsj1_7: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-155	-140	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	140	155	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	140	155	V
VSB	-40°C to 175°C	-0.5	0	5.5	7	V
VD-HW	-40°C to 175°C	-	-1.5	200	220	V
VD-NB ⁽²⁾	-40°C to 175°C	-155	-140	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS10S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	155	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

3. Parameters → 3.19 1XN module→ 3.19.2 Device parameters→ nhsj1_10→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS10S	saturation current @ VG=5V, VD=30V, L=0.5μm, W=50μm, NF=2, WF=25μm	80	89	98	107	116	μA/μm
IDP NHS10S	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	134	-	-	μA/μm
ROA NHS10	area specific on resistance @ VG=5V, VD=0.1V, L=1μm, W=50μm, Pitch=12.5μm, NF=2, WF=25μm	-	-	570	625	-	mΩmm ²
ROA NHS10S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, Pitch=12μm, NF=2, WF=25μm	-	-	528	582	-	mΩmm ²
RO_NHS10S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	35	39.5	44	48.5	53	kΩμm
TC_VTNHS10S	threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	-2.1	-	-	mV/K
VT1NHSJ1_10	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=100μm	-	-	175	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 Technical Report UHV Characteristics" at "my X-FAB"						
VTXNHS10	extrapolated threshold voltage @ VD=0.1V, L=1μm, W=50μm, NF=2, WF=25μm	-	-	1.05	-	-	V
VTXNHS10S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	1.01	1.08	1.16	1.24	1.31	V

Matching parameters

Name	Description	Typ	Unit
ABT NHS10	pelgrom coefficient gain factor mismatch	3.2	%μm
AID NHS1000	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	31.6	%μm
AID NHS1002	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	15.8	%μm
AID NHS1004	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	8.9	%μm
AID NHS1006	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	5.93	%μm
AID NHS1010	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	3.55	%μm
AID NHS1020	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.64	%μm
AID NHS1030	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.59	%μm
AID NHS1050	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.58	%μm
AVT NHS10	pelgrom coefficient threshold voltage mismatch	18.1	mVμm
DLT NHS10	transistor delta length	0	μm
DWT NHS10	transistor delta width	0	μm

Note: Matching data are valid for up to L=1μm. Transistors with channel lengths > 1.0μm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.19 1XN module → 3.19.2 Device parameters → nhsj1_10 → Matching parameters

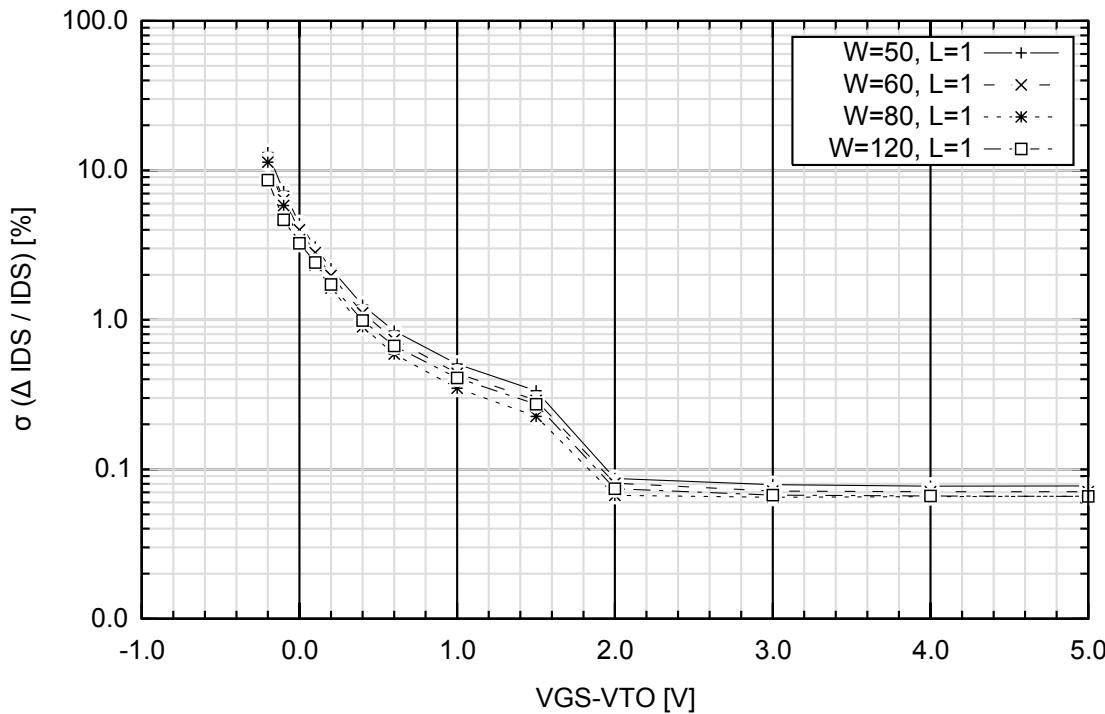


Figure 3.45 Device nhsj1_10: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1_16c

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-220	-200	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	200	220	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	200	220	V
VSB	-40°C to 175°C	-0.5	0	5.5	7	V
VD-HW	-40°C to 175°C	-	-1.5	200	220	V
VD-NB ⁽²⁾	-40°C to 175°C	-220	-200	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS16CS	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	220	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							



3. Parameters → 3.19 1XN module→ 3.19.2 Device parameters→ nhsj1_16c→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS16CS	saturation current @ VG=5V, VD=30V, L=0.5μm, W=50μm, NF=2, WF=25μm	71	80	89	98	107	μA/μm
IDP NHS16CS	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	117	-	-	μA/μm
ROA NHS16C	area specific on resistance @ VG=5V, VD=0.1V, L=1μm, W=50μm, Pitch=18.5μm, NF=2, WF=25μm	-	-	1270	1406	-	mΩmm ²
ROA NHS16CS	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, Pitch=18μm, NF=2, WF=25μm	-	-	1233	1359	-	mΩmm ²
RO_NHS16CHS	absolute high side on-resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	69.5	-	-	kΩμm
RO_NHS16CS	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	54.5	61.5	68.5	75.5	82.5	kΩμm
TC_VTNHS16CS	threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	-2.1	-	-	mV/K
VT1NHSJ1_16C	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=100μm	-	-	216	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS16C	extrapolated threshold voltage @ VD=0.1V, L=1μm, W=50μm, NF=2, WF=25μm	-	-	1.03	-	-	V
VTXNHS16CS	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	0.98	1.05	1.13	1.21	1.28	V

Matching parameters

Name	Description	Typ	Unit
ABTNHS16C	pelgrom coefficient gain factor mismatch	3.8	%μm
AIDNHS16C00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	33	%μm
AIDNHS16C02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	15.9	%μm
AIDNHS16C04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	8.68	%μm
AIDNHS16C06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	5.69	%μm
AIDNHS16C10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	3.39	%μm
AIDNHS16C20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.55	%μm
AIDNHS16C30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.52	%μm
AIDNHS16C50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVTNHS16C	pelgrom coefficient threshold voltage mismatch	17.2	mVμm
DLTNHS16C	transistor delta length	0	μm
DWTNHS16C	transistor delta width	0	μm

Note: Matching data are valid for up to L=1μm. Transistors with channel lengths > 1.0μm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.19 1XN module → 3.19.2 Device parameters → nhsj1_16c → Matching parameters

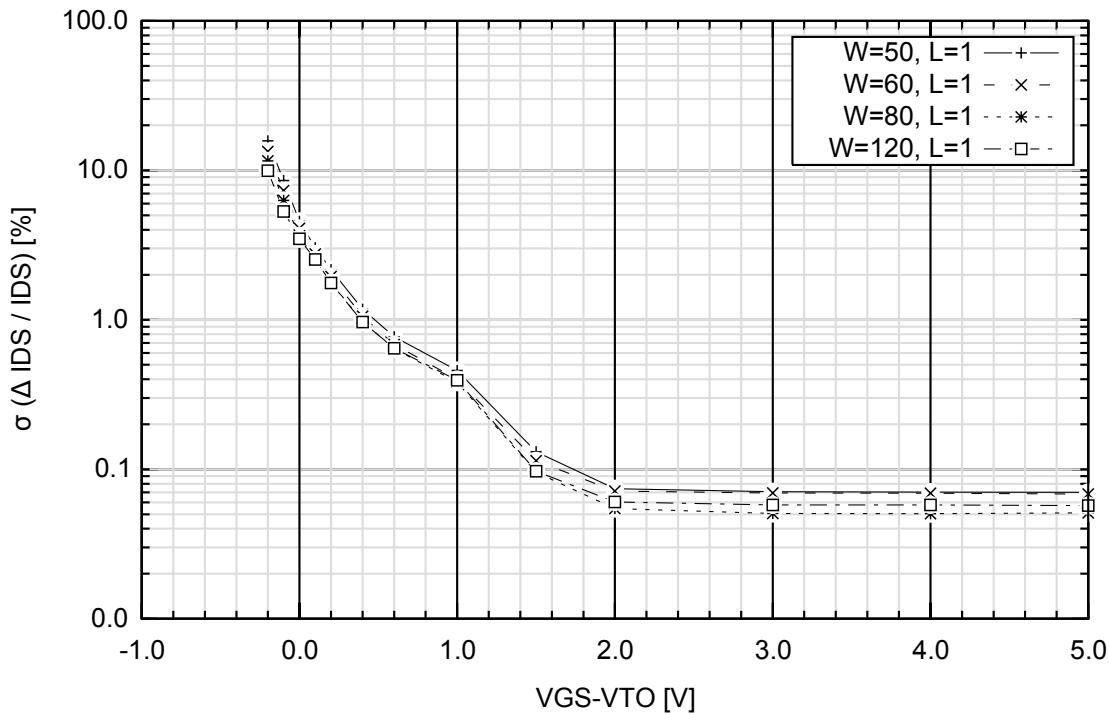


Figure 3.46 Device nhsj1_16c: drain current matching vs. VGS-VTO (typical values, drawn W and L)

dfwnsj1_7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-110	-100	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	200	220	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-110	-100	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ7	reverse breakdown voltage @ L=7μm, W=50μm, NF=2, WF=25μm	110	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DNSJ7	leakage current @ VL=100V, T=27°C, W=50μm, NF=2, WF=25μm	-	-	0.4	-	-	pA
IL_DNSJ7HT	leakage current @ VL=100V, T=175°C, W=50μm, NF=2, WF=25μm	-	-	1.4	-	-	nA

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3. Parameters → 3.19 1XN module → 3.19.2 Device parameters → dfwnsj1_7 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ7	forward voltage temperature coefficient	-	-	-1.9	-	-	mV/K
TM_RRDNSJ7	reverse recovery time @ Vrev=5V, Jfwd=0.5mA/μm, W=50μm, NF=2, WF=25μm	-	-	20	-	-	ns
VDFDNSJ7	diode forward voltage @ Idio=50μA, L=7μm, W=50μm, NF=2, WF=25μm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-155	-140	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	200	220	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-155	-140	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ10	reverse breakdown voltage @ L=10μm, W=50μm, NF=2, WF=25μm	155	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ10	leakage current @ VL=140V, T=27°C, W=50μm, NF=2, WF=25μm	-	-	1	-	-	pA
IL_DNSJ10HT	leakage current @ VL=140V, T=175°C, W=50μm, NF=2, WF=25μm	-	-	2.2	-	-	nA
TC_VDFDNSJ10	forward voltage temperature coefficient	-	-	-2	-	-	mV/K
TM_RRDNSJ10	reverse recovery time @ Vrev=5V, Jfwd=0.5mA/μm, W=50μm, NF=2, WF=25μm	-	-	20	-	-	ns
VDFDNSJ10	diode forward voltage @ Idio=50μA, L=10μm, W=50μm, NF=2, WF=25μm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1_16c

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-220	-200	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	200	220	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-220	-200	1	1.5	V

3. Parameters → 3.19 1XN module→ 3.19.2 Device parameters→ dfwnsj1_16c→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ16C	reverse breakdown voltage @ L=16µm, W=50µm, NF=2, WF=25µm	220	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ16C	leakage current @ VL=200V, T=27°C, W=50µm, NF=2, WF=25µm	-	-	1.4	-	-	pA
IL_DNSJ16CHT	leakage current @ VL=200V, T=175°C, W=50µm, NF=2, WF=25µm	-	-	2.9	-	-	nA
TC_VDFDNSJ16C	forward voltage temperature coefficient	-	-	-2	-	-	mV/K
TM_RRDNSJ16C	reverse recovery time @ Vrev=5V, Jfwd=0.5mA/µm, W=50µm, NF=2, WF=25µm	-	-	20	-	-	ns
VDFDNSJ16C	diode forward voltage @ Idio=50µA, L=16µm, W=50µm, NF=2, WF=25µm	0.74	0.76	0.78	0.8	0.82	V

3. Parameters → 3.20 1XP module

3.20 1XP module

3.20.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_SJPN	SJPN junction depth	1.75	μm

Sheet and contact resistance parameters

Name	Description	Low	Typ	High	Unit
RSRNSJPN	SJPN n-type sheet resistance	4.6	5	5.4	kΩ/□
RSRPSJPN	SJPN p-type sheet resistance	11.5	13	14.5	kΩ/□

3.20.2 Device parameters

phsj1_7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	100	110	V
VDS	-40°C to 175°C	-110	-100	1.5	-	V
VDB	-40°C to 175°C	-110	-100	1.5	-	V
VSB	-40°C to 175°C	-7	-5.5	0	0.5	V
VB-HW	-40°C to 175°C	-0.5	0	200	220	V
VB-NB ⁽¹⁾	-40°C to 175°C	-110	-100	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS7S	drain-source breakdown @ VG=0V, Id=1μA, L=0.5μm	110	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS7S	saturation current @ VG=-5V, VD=-50V, L=0.5μm, W=50μm, NF=2, WF=25μm	67	72	76	81	85	μA/μm
IDPPHS7S	pulsed drain current @ VG=-5V, VD=-50V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	111	-	-	μA/μm
ROAPHS7	area specific on resistance @ VG=-5V, VD=-0.1V, L=1μm, W=50μm, Pitch=9.5μm, NF=2, WF=25μm	-	-	1007	1112	-	mΩmm ²
ROAPHS7S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, Pitch=9μm, NF=2, WF=25μm	-	-	900	999	-	mΩmm ²

3. Parameters → 3.20 1XP module→ 3.20.2 Device parameters→ phsj1_7→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RO_PHS7LS	absolute low side on-resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	100	-	-	kΩμm
RO_PHS7S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	78	89	100	111	122	kΩμm
TC_VTPHS7S	threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	2	-	-	mV/K
VTXPHS7	extrapolated threshold voltage @ VD=-0.1V, L=1μm, W=50μm, NF=2, WF=25μm	-	-	-1.18	-	-	V
VTXPHS7S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	-1.35	-1.28	-1.2	-1.13	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABTPHS7	pelgrom coefficient gain factor mismatch	2.9	%μm
AIDPHS700	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	29.9	%μm
AIDPHS702	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	13.4	%μm
AIDPHS704	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.22	%μm
AIDPHS706	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.78	%μm
AIDPHS710	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.98	%μm
AIDPHS720	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.26	%μm
AIDPHS730	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.07	%μm
AIDPHS750	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1.04	%μm
AVTPHS7	pelgrom coefficient threshold voltage mismatch	15.7	mVμm
DLTPHS7	transistor delta length	0	μm
DWTPHS7	transistor delta width	0	μm

Note: Matching data are valid for up to L=1μm. Transistors with channel lengths > 1.0μm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.20 1XP module → 3.20.2 Device parameters → phsj1_7 → Matching parameters

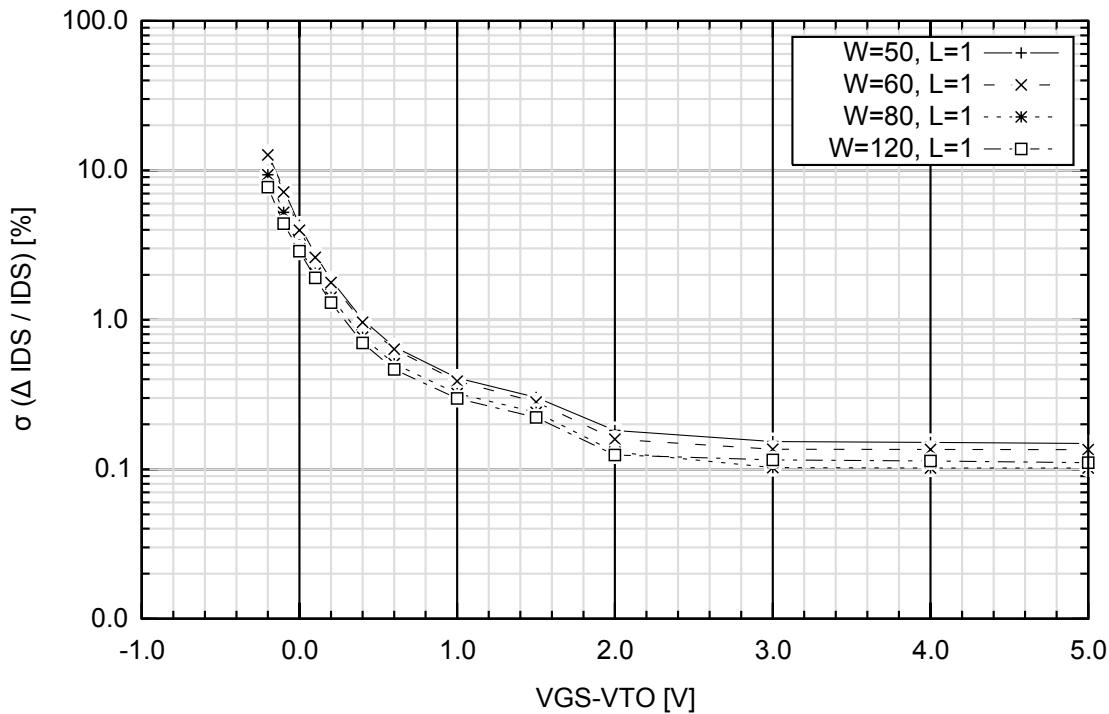


Figure 3.47 Device phsj1_7: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	140	155	V
VDS	-40°C to 175°C	-155	-140	1.5	-	V
VDB	-40°C to 175°C	-155	-140	1.5	-	V
VSB	-40°C to 175°C	-7	-5.5	0	0.5	V
VB-HW	-40°C to 175°C	-0.5	0	200	220	V
VB-NB ⁽¹⁾	-40°C to 175°C	-155	-140	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS10S	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	155	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS10S	saturation current @ VG=-5V, VD=-50V, L=0.5µm, W=50µm, NF=2, WF=25µm	54	59	63	68	72	µA/µm
IDPPHS10S	pulsed drain current @ VG=-5V, VD=-50V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=50µm, NF=2, WF=25µm	-	-	87	-	-	µA/µm

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3. Parameters → 3.20 1XP module→ 3.20.2 Device parameters→ phsj1_10→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA _{PHS10}	area specific on resistance @ VG=-5V, VD=-0.1V, L=1μm, W=50μm, Pitch=12.5μm, NF=2, WF=25μm	-	-	1815	2002	-	mΩmm ²
ROA _{PHS10S}	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, Pitch=12μm, NF=2, WF=25μm	-	-	1670	1814	-	mΩmm ²
RO _{_PHS10S}	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	115	127	139	151	163	kΩμm
TC _{_VTPHS10S}	threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	2	-	-	mV/K
VTX _{PHS10}	extrapolated threshold voltage @ VD=-0.1V, L=1μm, W=50μm, NF=2, WF=25μm	-	-	-1.18	-	-	V
VTX _{PHS10S}	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	-1.35	-1.28	-1.2	-1.13	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABT _{PHS10}	pelgrom coefficient gain factor mismatch	2.9	%μm
AID _{PHS1000}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	32.2	%μm
AID _{PHS1002}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.4	%μm
AID _{PHS1004}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.77	%μm
AID _{PHS1006}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	5.16	%μm
AID _{PHS1010}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	3.21	%μm
AID _{PHS1020}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1	%μm
AID _{PHS1030}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.94	%μm
AID _{PHS1050}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.92	%μm
AVT _{PHS10}	pelgrom coefficient threshold voltage mismatch	16.1	mVμm
DLT _{PHS10}	transistor delta length	0	μm
DWT _{PHS10}	transistor delta width	0	μm

Note: Matching data are valid for up to L=1μm. Transistors with channel lengths > 1.0μm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.20 1XP module → 3.20.2 Device parameters → phsj1_10 → Matching parameters

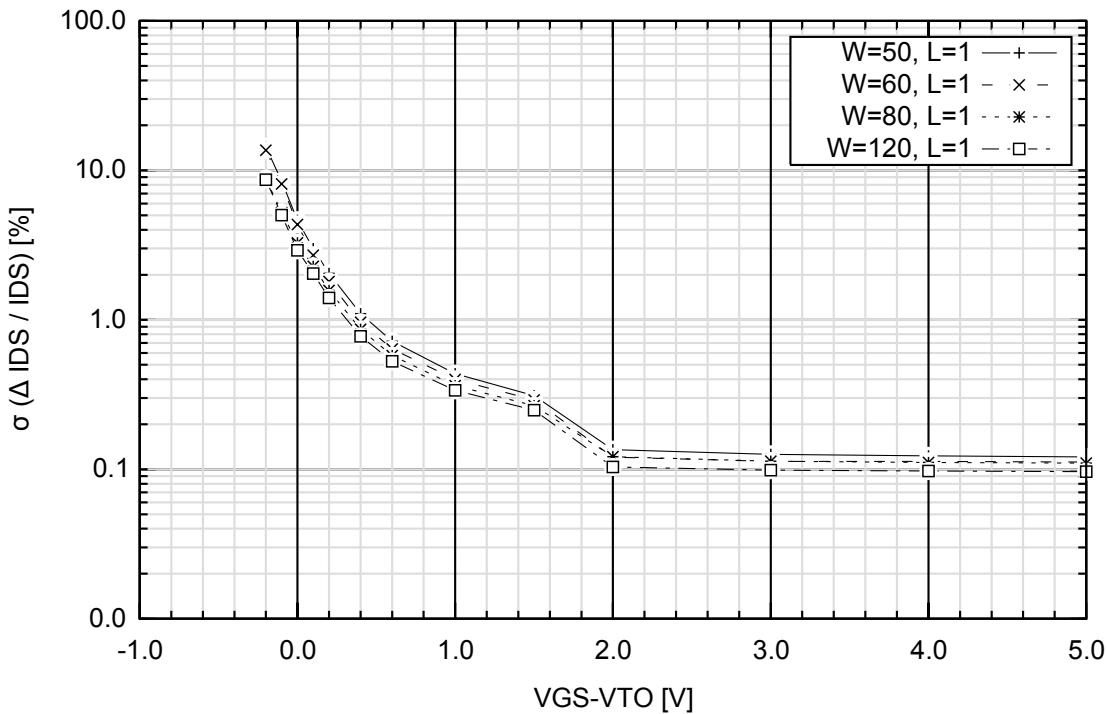


Figure 3.48 Device phsj1_10: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1_16c

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	200	220	V
VDS	-40°C to 175°C	-220	-200	1.5	-	V
VDB	-40°C to 175°C	-220	-200	1.5	-	V
VSB	-40°C to 175°C	-7	-5.5	0	0.5	V
VB-HW	-40°C to 175°C	-0.5	0	200	200	V
VB-NB ⁽¹⁾	-40°C to 175°C	-220	-200	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS16CS	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	220	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS16CS	saturation current @ VG=-5V, VD=-50V, L=0.5µm, W=50µm, NF=2, WF=25µm	40	44	49	54	58	µA/µm
IDPPHS16CS	pulsed drain current @ VG=-5V, VD=-50V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=50µm, NF=2, WF=25µm	-	-	62	-	-	µA/µm

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3. Parameters → 3.20 1XP module→ 3.20.2 Device parameters→ phsj1_16c→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA_PHS16C	area specific on resistance @ VG=-5V, VD=-0.1V, L=1μm, W=50μm, Pitch=18.5μm, NF=2, WF=25μm	-	-	4145	4626	-	mΩmm ²
ROA_PHS16CS	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, Pitch=18μm, NF=2, WF=25μm	-	-	3925	4141	-	mΩmm ²
RO_PHS16CLS	absolute low side on-resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	220	-	-	kΩμm
RO_PHS16CS	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	194	206	218	230	242	kΩμm
TC_VTPHS16CS	threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	2	-	-	mV/K
VTX_PHS16C	extrapolated threshold voltage @ VD=-0.1V, L=1μm, W=50μm, NF=2, WF=25μm	-	-	-1.18	-	-	V
VTX_PHS16CS	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	-1.35	-1.28	-1.2	-1.13	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABT_PHS16C	pelgrom coefficient gain factor mismatch	3.4	%μm
AID_PHS16C00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	34.2	%μm
AID_PHS16C02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	15.5	%μm
AID_PHS16C04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	8.15	%μm
AID_PHS16C06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	5.32	%μm
AID_PHS16C10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	3.27	%μm
AID_PHS16C20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.83	%μm
AID_PHS16C30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.78	%μm
AID_PHS16C50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.75	%μm
AVT_PHS16C	pelgrom coefficient threshold voltage mismatch	16.4	mVμm
DLT_PHS16C	transistor delta length	0	μm
DWT_PHS16C	transistor delta width	0	μm

Note: Matching data are valid for up to L=1μm. Transistors with channel lengths > 1.0μm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.20 1XP module → 3.20.2 Device parameters → phsj1_16c → Matching parameters

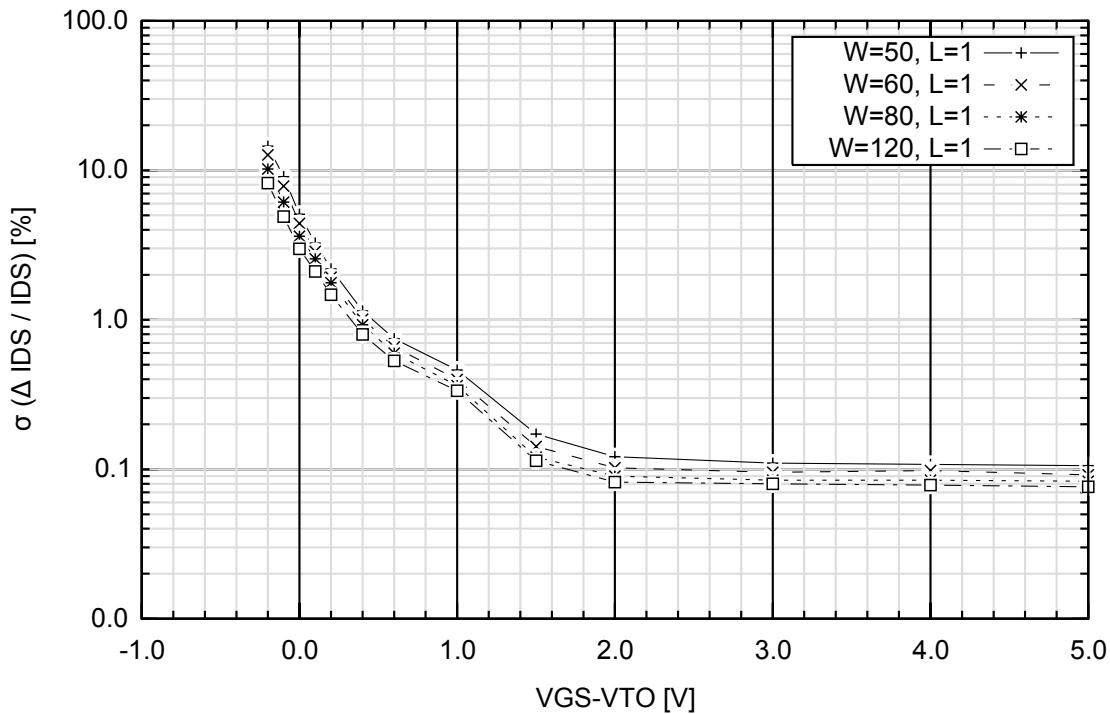


Figure 3.49 Device phsj1_16c: drain current matching vs. $VGS-VTO$ (typical values, drawn W and L)

3. Parameters → 3.21 2XP module

3.21 2XP module

3.21.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_SJ2XP	SJ2XP junction depth	2	µm
XJ_SJNTOP	SJNTOP junction depth	0.3	µm

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSNSJ2XP	SJ2XP n-type sheet resistance	6.1	kΩ/□
RSSNSJNTOP	SJNTOP n-type sheet resistance	3.3	kΩ/□
RSSPSJ2XP	SJ2XP p-type sheet resistance	7.8	kΩ/□
RSSPSJNTOP	SJNTOP p-type sheet resistance	15.2	kΩ/□

3.21.2 Device parameters

phsj2b_7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	115	125	V
VDS	-40°C to 175°C	-125	-115	1.5	-	V
VDB	-40°C to 175°C	-125	-115	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-125	-115	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS2B7S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	132	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS2B7S	saturation current @ VG=-5V, VD=-40V, L=0.5µm, W=20µm, NF=2, WF=10µm	78	88	97	106	116	µA/µm
IDPPHS2B7S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=20µm, NF=2, WF=10µm	-	-	130	-	-	µA/µm
ROAPHS2B7S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=9µm, NF=2, WF=10µm	-	-	568	625	-	mΩmm ²

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3. Parameters → 3.21 2XP module → 3.21.2 Device parameters → phsj2b_7 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RO_PHS2B7S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	51	57	63	69	75	kΩμm
TC_BDSPHS2B7S	breakdown temperature coefficient	-	-	0.12	-	-	V/K
TC_VTPHS2B7S	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	1.96	-	-	mV/K
VTXPHS2B7S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%μm
AIDPHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%μm
AIDPHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%μm
AIDPHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%μm
AIDPHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%μm
AIDPHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%μm
AIDPHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%μm
AIDPHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%μm
AIDPHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVTPHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVμm
DLTPHSJ2B	transistor delta length	0	μm
DWTPHSJ2B	transistor delta width	0	μm

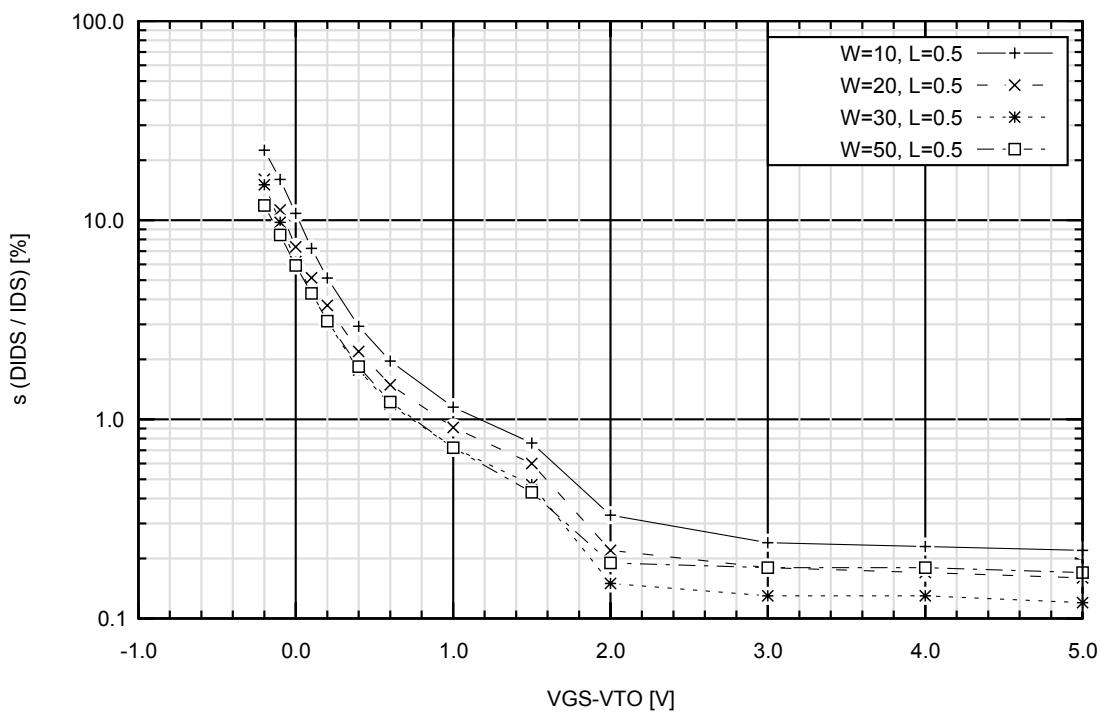


Figure 3.50 Device phsj2b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.21 2XP module → 3.21.2 Device parameters → phsj2b_8 → Operating conditions

phsj2b_8

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	140	155	V
VDS	-40°C to 175°C	-155	-140	1.5	-	V
VDB	-40°C to 175°C	-155	-140	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-155	-140	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS2B8S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	161	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS2B8S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	73	82	91	100	109	μA/μm
IDPPHS2B8S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	122	-	-	μA/μm
ROAPHS2B8S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, Pitch=10.5μm, NF=2, WF=10μm	-	-	750	825	-	mΩmm ²
RO_PHS2B8S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	57	64	71	78	85	kΩμm
TC_BDSPHS2B8S	breakdown temperature coefficient	-	-	0.14	-	-	V/K
TC_VTPHS2B8S	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	1.95	-	-	mV/K
VTXPHS2B8S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%μm
AIDPHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%μm
AIDPHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%μm
AIDPHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%μm
AIDPHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%μm
AIDPHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%μm
AIDPHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%μm
AIDPHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%μm

3. Parameters → 3.21 2XP module→ 3.21.2 Device parameters→ phsj2b_8→ Matching parameters

Name	Description	Typ	Unit
AIDPHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVTPHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVμm
DLTPHSJ2B	transistor delta length	0	μm
DWTPHSJ2B	transistor delta width	0	μm

phsj2b_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	155	170	V
VDS	-40°C to 175°C	-170	-155	1.5	-	V
VDB	-40°C to 175°C	-170	-155	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-170	-155	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS2B10S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	178	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5PHS2B10S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	68	77	85	93	102	μA/μm
IDPPHS2B10S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	115	-	-	μA/μm
ROAPHS2B10S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, Pitch=12μm, NF=2, WF=10μm	-	-	951	1046	-	mΩmm ²
RO_PHS2B10S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	64	71.5	79	86.5	94	kΩμm
TC_BDSPHS2B10S	breakdown temperature coefficient	-	-	0.16	-	-	V/K
TC_VTPHS2B10S	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	1.97	-	-	mV/K
VTXPHS2B10S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%μm
AIDPHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%μm

3. Parameters → 3.21 2XP module → 3.21.2 Device parameters → phsj2b_10 → Matching parameters

Name	Description	Typ	Unit
AIDPHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%μm
AIDPHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%μm
AIDPHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%μm
AIDPHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%μm
AIDPHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%μm
AIDPHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%μm
AIDPHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVTPHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVμm
DLTPHSJ2B	transistor delta length	0	μm
DWTPHSJ2B	transistor delta width	0	μm

phsj2b_13

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	195	215	V
VDS	-40°C to 175°C	-215	-195	1.5	-	V
VDB	-40°C to 175°C	-215	-195	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-215	-195	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS2B13S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	224	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS2B13S	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=50μm, NF=2, WF=25μm	60	68	75	82	90	μA/μm
IDPPHS2B13S	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	109	-	-	μA/μm
ROAPHS2B13S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, Pitch=15μm, NF=2, WF=25μm	-	-	1589	1748	-	mΩmm ²
RO_PHS2B13S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	85	95.5	106	116.5	127	kΩμm
TC_BDSPHS2B13S	breakdown temperature coefficient	-	-	0.18	-	-	V/K
TC_VTPHS2B13S	threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	2.03	-	-	mV/K

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3. Parameters → 3.21 2XP module → 3.21.2 Device parameters → phsj2b_13 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VTXPHS2B13S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=50µm, NF=2, WF=25µm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%µm
AIDPHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%µm
AIDPHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%µm
AIDPHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%µm
AIDPHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%µm
AIDPHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%µm
AIDPHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%µm
AIDPHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%µm
AIDPHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%µm
AVTPHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVµm
DLTPHSJ2B	transistor delta length	0	µm
DWTPHSJ2B	transistor delta width	0	µm

phsj2b_16

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	235	255	V
VDS	-40°C to 175°C	-255	-235	1.5	-	V
VDB	-40°C to 175°C	-255	-235	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-255	-235	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS2B16S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	270	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS2B16S	saturation current @ VG=-5V, VD=-60V, L=0.5µm, W=60µm, NF=2, WF=30µm	56.5	64	71.5	79	86.5	µA/µm
IDPPHS2B16S	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=60µm, NF=2, WF=30µm	-	-	101	-	-	µA/µm



3. Parameters → 3.21 2XP module→ 3.21.2 Device parameters→ phsj2b_16→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS2B16S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=60µm, Pitch=18µm, NF=2, WF=30µm	-	-	2286	2394	-	mΩmm ²
RO _PHS2B16S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=60µm, NF=2, WF=30µm	115	121	127	133	139	kΩµm
TC _BDSPHS2B16S	breakdown temperature coefficient	-	-	0.19	-	-	V/K
TC _VTPHS2B16S	threshold voltage temperature coefficient @ L=0.5µm, W=60µm	-	-	2.01	-	-	mV/K
VTX PHS2B16S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=60µm, NF=2, WF=30µm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%µm
AID PHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%µm
AID PHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%µm
AID PHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%µm
AID PHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%µm
AID PHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%µm
AID PHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%µm
AID PHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%µm
AID PHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%µm
AVT PHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVµm
DLT PHSJ2B	transistor delta length	0	µm
DWT PHSJ2B	transistor delta width	0	µm

3. Parameters → 3.22 DNC module

3.22 DNC module

The DNC module introduce additional NWELL1 for combination with HV module. Parameters are not defined for the DNC module

3. Parameters → 3.23 DPC module

3.23 DPC module

3.23.1 Device parameters

dnp7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-9.6	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	5	-	µA/µm

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DNP7	breakdown voltage @ Irev=1µA, L=1µm, W=10µm	7.61	7.73	7.85	7.97	8.09	V
IL_DNP7	leakage current @ VL=5.5V, T=27°C, L=1µm, W=10µm	-	-	4.3	-	-	pA
IL_DNP7HT	leakage current @ VL=5.5V, T=175°C, L=1µm, W=10µm	-	-	0.25	-	-	nA
TC_BVDNP7	breakdown temperature coefficient	-	-	3.6	-	-	mV/K

3. Parameters → 3.24 HVN module

3.24 HVN module

3.24.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSRHVNW	HVNWELL sheet resistance (DTI terminated)	200	Ω/□

3.24.2 Device parameters

peti

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VGD	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDS	-40°C to 175°C	-2.3	-1.98	1.98	2.3	V
VDB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VSB	-40°C to 175°C	-2.3	-1.98	0	0.5	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPETIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.18µm	3.6	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPETI	mobility exponent	-	-	-1	-	-	-
FC_PETI	corner frequency @ VD=-1.8V, Id=-1µA	-	-	0.43	-	-	kHz
GA_PETI	body factor long channel @ L=10µm, W=10µm	-	-	0.9	-	-	√V
IDS_PETIS	saturation current @ VG=-1.8V, VD=-1.8V, L=0.18µm, W=10µm	135	165	195	225	255	µA/µm
IOF_PETIS	off-state leakage @ VD=-1.8V, L=0.18µm, W=10µm	-	-	-	1.5	-	pA/µm
ISBPETIS	bulk current @ VD=-1.8V, L=0.18µm	-	-	0.2	-	-	nA/µm
KP_PETI	gain factor @ L=10µm, W=10µm	-	-	53.5	-	-	µA/V ²
LEFPETI	effective channel length @ L=0.18µm	-	-	0.12	-	-	µm
NOIPETI	input referred noise @ VD=-1.8V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	13.3	-	-	µVµm/√(Hz)
STS_PETI	subthreshold slope @ VD=-1.8V	-	-	11	-	-	decade/V
TC_VTXPETI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	0.91	-	-	mV/K
U0_PETI	effective mobility	-	-	65	-	-	cm ² /(Vs)
VTIPETIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.73	-0.698	-0.665	-0.632	-0.6	V
VTIPETIS	threshold voltage short channel @ VD=-0.1V, L=0.18µm, W=10µm	-0.7	-0.658	-0.615	-0.572	-0.53	V

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3. Parameters → 3.24 HVN module→ 3.24.2 Device parameters→ peti→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VTIPETISS	threshold voltage small channel @ VD=-0.1V, L=0.18μm, W=0.22μm	-	-	-0.55	-	-	V
VTXPETIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.18μm, W=10μm	-	-	-0.62	-	-	V
WEFPETI	effective channel width @ W=0.22μm	-	-	0.25	-	-	μm

Matching parameters

Name	Description	Typ	Unit
ABTPETI	pelgrom coefficient gain factor mismatch	0.94	%μm
AIDPETI00	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0V	7.7	%μm
AIDPETI01	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.1V	5.23	%μm
AIDPETI02	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.2V	3.66	%μm
AIDPETI04	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.4V	2.19	%μm
AIDPETI06	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.6V	1.55	%μm
AIDPETI08	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=0.8V	1.24	%μm
AIDPETI10	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1V	1.05	%μm
AIDPETI14	pelgrom coefficient drain current mismatch @ VDS=1.8V, VG-VT=1.4V	0.84	%μm
AVTPETI	pelgrom coefficient threshold voltage mismatch	5.41	mVμm
DLPETI	transistor delta length	0.06	μm
DWTPETI	transistor delta width	-0.03	μm

Note: It is strongly recommended to avoid the use of minimum length and/ or width for improved matching. Small sized devices show larger mismatch than predicted by the matching coefficients.

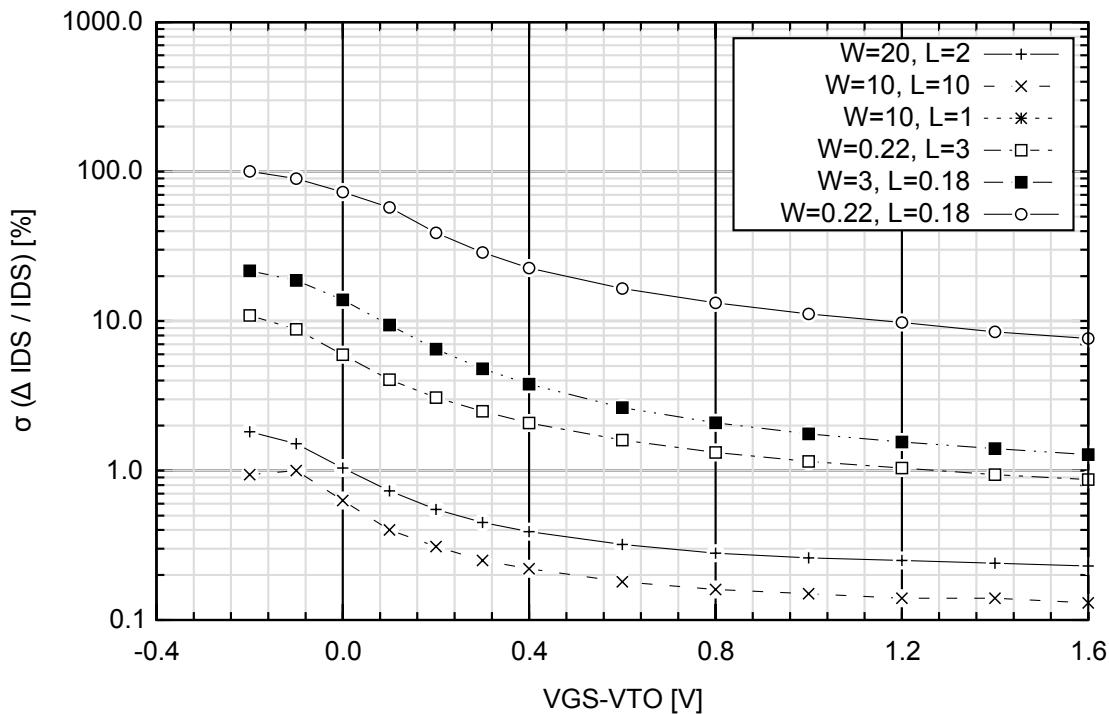


Figure 3.51 Device peti: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.24 HVN module→ 3.24.2 Device parameters→ pe5ti→ Operating conditions

pe5ti

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	5.5	7	V
VDS	-40°C to 175°C	-7	-5.5	5.5	7	V
VDB	-40°C to 175°C	-7	-5.5	0	0.5	V
VSB	-40°C to 175°C	-7	-5.5	0	0.5	V
VB-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPE5TIS	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	7.5	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
BEXPE5TI	mobility exponent	-	-	-1.2	-	-	-
FC_PE5TI	corner frequency @ VD=-5V, Id=-1µA	-	-	0.43	-	-	kHz
GA_PE5TI	body factor long channel @ L=10µm, W=10µm	-	-	1.1	-	-	√V
IDSPE5TIS	saturation current @ VG=-5V, VD=-5V, L=0.5µm, W=10µm	230	250	270	290	310	µA/µm
IOFPE5TIS	off-state leakage @ VD=-5V, L=0.5µm, W=10µm	-	-	-	1	-	pA/µm
KP_PE5TI	gain factor @ L=10µm, W=10µm	-	-	28	-	-	µA/V ²
LEFPE5TI	effective channel length @ L=0.5µm	-	-	0.36	-	-	µm
NOIPE5TI	input referred noise @ VD=-5V, Id=-1µA, f=1Hz, L=10µm, W=10µm	-	-	20.2	-	-	µVµm/√(Hz)
STSPE5TI	subthreshold slope @ VD=-5V	-	-	10	-	-	decade/V
TC_VTXPE5TI	threshold voltage temperature coefficient @ L=10µm, W=10µm	-	-	1.1	-	-	mV/K
U0_PE5TI	effective mobility	-	-	102	-	-	cm ² /(Vs)
VTIPE5TIL	threshold voltage long channel @ VD=-0.1V, L=10µm, W=10µm	-0.91	-0.865	-0.82	-0.775	-0.73	V
VTIPE5TIS	threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-0.94	-0.87	-0.8	-0.73	-0.66	V
VTXPE5TIS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=10µm	-	-	-0.76	-	-	V
WEFPE5TI	effective channel width @ W=0.22µm	-	-	0.21	-	-	µm

Matching parameters

Name	Description	Typ	Unit
ABTPE5TI	pelgrom coefficient gain factor mismatch	0.76	%µm
AIDPE5TI00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	10.9	%µm
AIDPE5TI02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	5.04	%µm
AIDPE5TI04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	2.99	%µm

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3. Parameters → 3.24 HVN module→ 3.24.2 Device parameters→ pe5ti→ Matching parameters

Name	Description	Typ	Unit
AIDPE5TI06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	2.11	%μm
AIDPE5TI10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	1.35	%μm
AIDPE5TI20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.78	%μm
AIDPE5TI30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.59	%μm
AIDPE5TI50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.44	%μm
AVTPE5TI	pelgrom coefficient threshold voltage mismatch	7.18	mVμm
DLTPE5TI	transistor delta length	0.14	μm
DWTPE5TI	transistor delta width	0.01	μm

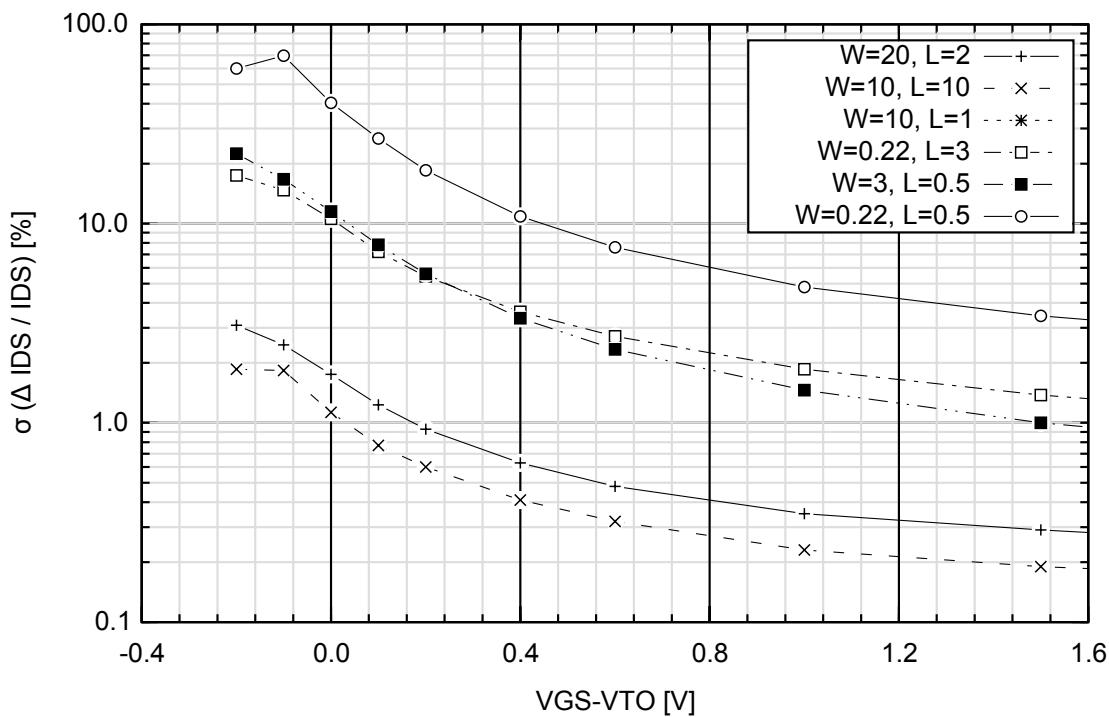


Figure 3.52 Device pe5ti: drain current matching vs. VGS-VTO (typical values, drawn W and L)

dfwdpa**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-7	-5.5	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-440	-400	400	440	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

3. Parameters → 3.24 HVN module→ 3.24.2 Device parameters→ dfwdpa→ Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DPA	breakdown voltage @ Irev=100µA, L=1µm, W=10µm, NF=4	7.1	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DFDPA	leakage current @ VL=5.5V, T=27°C	-	-	0.52	-	-	pA/µm ²
IL_DFDPAHT	leakage current @ VL=5.5V, T=175°C	-	-	25.8	-	-	pA/µm ²
TC_VDFDPA	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDPA	diode forward voltage @ Idio=1µA/µm, L=1µm, W=40µm, NF=4, WF=10µm	0.75	0.76	0.77	0.78	0.79	V

ds5a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-5.5	1.5	-	V
Vcathode-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DS5AL	breakdown voltage @ Irev=1mA, L=0.94µm, W=50µm	7.3	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
BV_DS5AS	breakdown voltage @ Irev=50µA, L=0.94µm, W=2.4µm	7.3	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDFDS5AL	diode forward current @ Vbias=0.6V, L=0.94µm, W=50µm	-	-	7000	-	-	µA
IDFDS5AS	diode forward current @ Vbias=0.6V, L=0.94µm, W=2.4µm	-	-	410	-	-	µA
IL_DS5AL2	leakage current @ VL=2V, L=0.94µm, W=50µm	-	-	100	-	-	nA
IL_DS5AL5	leakage current @ VL=5.5V, L=0.94µm, W=50µm	-	-	1150	-	300000	nA
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DS5AS2	leakage current @ VL=2V, L=0.94µm, W=2.4µm	-	-	4.8	-	-	nA
IL_DS5AS5	leakage current @ VL=5.5V, L=0.94µm, W=2.4µm	-	-	55	-	-	nA
TC_VDFDS5A	forward voltage temperature coefficient	-	-	-1.1	-	-	mV/K
VDFDS5AL	diode forward voltage @ Idio=200µA, L=0.94µm, W=50µm	-	-	0.37	-	-	V
VDFDS5AS	diode forward voltage @ Idio=10µA, L=0.94µm, W=2.4µm	0.31	0.345	0.38	0.415	0.45	V

3. Parameters → 3.24 HVN module→ 3.24.2 Device parameters→ dpp6→ Operating conditions

dpp6

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-7	0	0.5	V
Vcathode-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	5	-	µA/µm

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DPP6	breakdown voltage @ Irev=100µA, L=0.82µm, W=10µm	5.75	5.9	6.05	6.2	6.35	V
IL_DPP6	leakage current @ VL=4.5V, T=27°C, L=1µm, W=10µm	-	-	11	-	-	nA
IL_DPP6HT	leakage current @ VL=4.5V, T=175°C, L=1µm, W=10µm	-	-	17	-	-	nA
TC_BVDPP6	breakdown temperature coefficient	-	-	1.2	-	-	mV/K

dpp7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-9.4	0	0.5	V
Vcathode-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	5	-	µA/µm

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DPP7	breakdown voltage @ Irev=1µA, L=1µm, W=10µm	7.1	7.35	7.6	7.85	8.1	V
IL_DPP7	leakage current @ VL=5.5V, T=27°C, L=1µm, W=10µm	-	-	12	-	-	pA
IL_DPP7HT	leakage current @ VL=5.5V, T=175°C, L=1µm, W=10µm	-	-	0.36	-	-	nA
TC_BVDPP7	breakdown temperature coefficient	-	-	2.9	-	-	mV/K

3. Parameters → 3.25 HVP module

3.25 HVP module

3.25.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSRHVPW	HVPWELL sheet resistance (DTI terminated)	360	Ω/□

3. Parameters → 3.26 HWC module

3.26 HWC module

3.26.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RHWPNCNT	p-type handle wafer contact resistance @ Vbias=1V, L=25µm, W=1.5µm	-	-	220	-	5000	kΩ

Dielectric isolation electrical parameters

Name	Description	Low	Typ	High	Unit
VTA_NWPSUB	side-gate threshold voltage	17.5	20	22.5	V
VTG_NWPSUB	Back gate threshold voltage	34.5	39	43.5	V

3. Parameters → 3.27 NBUF module

3.27 NBUF module

3.27.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSNBUF	NBUF sheet resistance	140	Ω/□

3.27.2 Device parameters

nisj1_16

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VCE	-40°C to 175°C	-	-2	200	220	V
VGE	-40°C to 175°C	-7	-5.5	5.5	7	V
VGC	-40°C to 175°C	-220	-200	5.5	7	V
VC-HW	-40°C to 175°C	-0.5	0	200	220	V
VC-NB ⁽¹⁾	-40°C to 175°C	-220	-200	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: PWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BECNISJ16	emitter to collector breakdown voltage @ Ie=-1µA	-	-4	-	-	-	V
BVI _N ISJ16	collector to emitter breakdown voltage @ VG=0V, Ic=1µA, L=1µm	220	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
EOFNISJ16	turn-off energy @ T=27°C	-	-	1.68	-	-	mJ/cm ²
EOFNISJ16HT	turn-off energy @ T=175°C	-	-	2.28	-	-	mJ/cm ²
ICE2NISJ16	collector current @ VG=2V, VC=10V, L=1µm, W=48µm	-	-	24	-	-	µA/µm
ICE5NISJ16	collector current @ VG=5V, VC=10V, L=1µm, W=48µm	193	218	243	268	293	µA/µm
ICP1NISJ16	pulsed collector current @ VG=5V, VC=100V, Dcyc=1%, Pwid=200ns, L=1µm, W=48µm	-	-	280	-	-	µA/µm
ICP2NISJ16	pulsed collector current @ VG=5V, VC=10V, Dcyc=1%, Pwid=200ns, L=1µm, W=48µm	-	-	265	-	-	µA/µm
IOINISJ16	off state leakage current @ VG=0V, L=1µm, W=48µm	-	-	-	100	-	pA/µm
OSV150NISJ16	collector to emitter saturation voltage @ VG=5V, Ic=150A/cm ²	1	1.5	2	2.5	3	V
OSV300NISJ16	collector to emitter saturation voltage @ VG=5V, Ic=300A/cm ²	-	-	2.5	-	-	V
ROA5NISJ16	area specific on resistance @ VG=5V, VC=5V, L=1µm, W=48µm, Pitch=22.5µm	-	-	525	645	-	mΩmm ²

3. Parameters → 3.27 NBUF module→ 3.27.2 Device parameters→ nisj1_16→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RO_5NISJ16	on resistance @ VG=5V, VC=5V, L=1µm, W=48µm	12.7	18	23.3	28.7	34	kΩµm
TC_VTSNISJ16	threshold voltage temperature coefficient	-	-	-2	-	-	mV/K
TOF_NISJ16	turn-off time @ T=27°C	-	-	190	-	-	ns
TOF_NISJ16HT	turn-off time @ T=175°C	-	-	218	-	-	ns
VT1NISJ16	snap-back trigger voltage @ VGS=5V, Ngates=2, WF=200µm	-	-	270	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"							
VTINISJ16	threshold voltage @ VC=10V, L=1µm, W=48µm	0.98	1.04	1.1	1.16	1.22	V

Note: Short-circuit test result is summarized in "[Fast 200V Superjunction Lateral IGBT Characteristics](#)" on "my X-FAB"

3. Parameters → 3.28 NBUR module

3.28 NBUR module

3.28.1 Device independent parameters

Sheet and contact resistance parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RHWNCNT	n-type handle wafer contact resistance @ Vbias=1V, L=25μm, W=1.5μm	-	-	6.5	-	50	kΩ

Parasitic capacitance parameters

Name	Description	Typ	Unit
CPATUBDHW2	tub-handle wafer area capacitance	0.00256	fF/μm ²
CPATUBDHW2A	tub-handle wafer area capacitance	0.00298	fF/μm ²
CPATUBDHW2B	tub-handle wafer area capacitance	0.0028	fF/μm ²
CPATUBDHW2C	tub-handle wafer area capacitance	0.00244	fF/μm ²
CPATUBDHW3	tub-handle wafer area capacitance	0.00216	fF/μm ²
CPATUBDHW3C	tub-handle wafer area capacitance	0.00201	fF/μm ²
CPATUBDHW4C	tub-handle wafer area capacitance	0.00182	fF/μm ²
CPATUBDHW4D	tub-handle wafer area capacitance	0.00161	fF/μm ²
CPATUBDHW5D	tub-handle wafer area capacitance	0.00156	fF/μm ²

3.28.2 Device parameters

dhw2a

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-110	-100	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW2A	handle wafer diode breakdown voltage @ Irev=1μA, L=9.5μm, W=39μm	110	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CPATUBDHW2A	tub-handle wafer area capacitance	-	-	0.00298	-	-	fF/μm ²
IL_DHW2A	handle wafer diode leakage @ VL=100V, T=27°C, L=9.5μm, W=39μm	-	-	0.9	-	-	fA/μm ²
IL_DHW2AHT	leakage current @ VL=100V, T=175°C, L=9.5μm, W=39μm	-	-	300	-	-	pA/μm ²

dhw2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-155	-140	0	0.5	V

3. Parameters → 3.28 NBUR module→ 3.28.2 Device parameters→ dhw2→ Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW2	handle wafer diode breakdown voltage @ Irev=1µA, L=13.5µm, W=44µm	155	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CPATUBDHW2	tub-handle wafer area capacitance	-	-	0.00256	-	-	fF/µm²
IL_DHW2	handle wafer diode leakage @ VL=140V, T=27°C, L=13.5µm, W=44µm	-	-	2	-	-	fA/µm²
IL_DHW2HT	leakage current @ VL=140V, T=175°C, L=13.5µm, W=44µm	-	-	380	-	-	pA/µm²

dhw3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-220	-200	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW3	handle wafer diode breakdown voltage @ Irev=1µA, L=31.5µm, W=44µm	220	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CPATUBDHW3	tub-handle wafer area capacitance	-	-	0.00216	-	-	fF/µm²
IL_DHW3	handle wafer diode leakage @ VL=200V, T=27°C, L=31.5µm, W=44µm	-	-	3.1	-	-	fA/µm²
IL_DHW3HT	leakage current @ VL=200V, T=175°C, L=31.5µm, W=44µm	-	-	705	-	-	pA/µm²

dhw2b

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-125	-115	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW2B	handle wafer diode breakdown voltage @ Irev=1µA, L=20µm, W=40µm	132	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CPATUBDHW2B	tub-handle wafer area capacitance	-	-	0.0028	-	-	fF/µm²
IL_DHW2B	handle wafer diode leakage @ VL=115V, T=27°C, L=20µm, W=40µm	-	-	0.31	-	-	fA/µm²
IL_DHW2BHT	leakage current @ VL=115V, T=175°C, L=20µm, W=40µm	-	-	101	-	-	pA/µm²

3. Parameters → 3.28 NBUR module → 3.28.2 Device parameters → dhw2c → Operating conditions

dhw2c

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-175	-160	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW2C	handle wafer diode breakdown voltage @ Irev=1µA, L=20µm, W=40µm	184	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CPA_TUBDHW2C	tub-handle wafer area capacitance	-	-	0.00244	-	-	fF/µm²
IL_DHW2C	handle wafer diode leakage @ VL=160V, T=27°C, L=20µm, W=40µm	-	-	0.38	-	-	fA/µm²
IL_DHW2CHT	leakage current @ VL=160V, T=175°C, L=20µm, W=40µm	-	-	107	-	-	pA/µm²

dhw3c

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-255	-235	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW3C	handle wafer diode breakdown voltage @ Irev=1µA, L=20µm, W=40µm	270	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CPA_TUBDHW3C	tub-handle wafer area capacitance	-	-	0.00201	-	-	fF/µm²
IL_DHW3C	handle wafer diode leakage @ VL=235V, T=27°C, L=20µm, W=40µm	-	-	0.34	-	-	fA/µm²
IL_DHW3CHT	leakage current @ VL=235V, T=175°C, L=20µm, W=40µm	-	-	108	-	-	pA/µm²

dhw4c

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-310	-280	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW4C	handle wafer diode breakdown voltage @ Irev=1µA, L=35µm, W=40µm	322	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						

3. Parameters → 3.28 NBUR module→ 3.28.2 Device parameters→ dhw4c→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
CPA_TUBDHW4C	tub-handle wafer area capacitance	-	-	0.00182	-	-	fF/ μm^2
IL_DHW4C	handle wafer diode leakage @ VL=280V, T=27°C, L=35μm, W=40μm	-	-	0.35	-	-	fA/ μm^2
IL_DHW4CHT	leakage current @ VL=280V, T=175°C, L=35μm, W=40μm	-	-	132	-	-	pA/ μm^2

dhw4d**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-395	-360	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW4D	handle wafer diode breakdown voltage @ Irev=1μA, L=80μm, W=80μm	414	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CPA_TUBDHW4D	tub-handle wafer area capacitance	-	-	0.00161	-	-	fF/ μm^2
IL_DHW4D	handle wafer diode leakage @ VL=360V, T=27°C, L=80μm, W=80μm	-	-	0.41	-	-	fA/ μm^2
IL_DHW4DHT	leakage current @ VL=360V, T=175°C, L=80μm, W=80μm	-	-	163	-	-	pA/ μm^2

dhw5d**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-460	-420	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW5D	handle wafer diode breakdown voltage @ Irev=1μA, L=80μm, W=80μm	483	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CPA_TUBDHW5D	tub-handle wafer area capacitance	-	-	0.00156	-	-	fF/ μm^2
IL_DHW5D	handle wafer diode leakage @ VL=420V, T=27°C, L=80μm, W=80μm	-	-	0.53	-	-	fA/ μm^2
IL_DHW5DHT	leakage current @ VL=420V, T=175°C, L=80μm, W=80μm	-	-	222	-	-	pA/ μm^2

3. Parameters → 3.29 NHVA module

3.29 NHVA module

3.29.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_NDF	NDF junction depth	1.4	µm

3.29.2 Device parameters

nhvta

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-42	-40	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	40	42	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	40	42	V
VD-HW	-40°C to 175°C	-110	-100	200	220	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVTA	drain-source breakdown @ VG=0V, Id=1µA, L=0.4µm	45	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNHVTA	pulsed saturation current @ VG=5V, VD=10V, Dcyc=1%, Pwid=100ns, L=0.4µm, W=100µm, NF=4, WF=25µm	-	-	302	-	-	µA/µm
IDSNHVTA	saturation current @ VG=5V, VD=10V, L=0.4µm, W=100µm, NF=4, WF=25µm	150	175	200	225	250	µA/µm
KP_NHVTAL	gain factor long channel @ L=1.5µm, W=100µm, NF=4, WF=25µm	-	-	5310	-	-	µA/V ²
ROANHVTA	area specific on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, Pitch=2.89µm, NF=4, WF=25µm	-	-	26	29.8	-	mΩmm ²
RO_NHVTA	on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	6.4	7.7	9	10.3	11.6	kΩµm
TC_VTXNHVTA	threshold voltage temperature coefficient	-	-	-1.6	-	-	mV/K

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3. Parameters → 3.29 NHVA module→ 3.29.2 Device parameters→ nhvta→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VT1NHVTA	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	53	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"						
VTINHVTA	threshold voltage @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	-	1.03	1.1	1.17	-	V
VTXNHVTA	extrapolated threshold voltage @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	0.91	0.99	1.07	1.15	1.23	V
VTXNHVTAL	extrapolated threshold voltage long channel @ VD=0.1V, L=1.5μm, W=100μm, NF=4, WF=25μm	-	-	0.93	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTNHVTA	pelgrom coefficient gain factor mismatch	5.53	%μm
AIDNHVTA00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.79	%μm
AIDNHVTA02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.66	%μm
AIDNHVTA04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	10.16	%μm
AIDNHVTA06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	7.86	%μm
AIDNHVTA10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	5.2	%μm
AIDNHVTA20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	2.59	%μm
AIDNHVTA30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.36	%μm
AIDNHVTA50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.63	%μm
AVTNHVTA	pelgrom coefficient threshold voltage mismatch	19.8	mVμm
DLTNHVTA	transistor delta length	0	μm
DWTNHVTA	transistor delta width	0	μm

3. Parameters → 3.29 NHVA module → 3.29.2 Device parameters → nhvta → Matching parameters

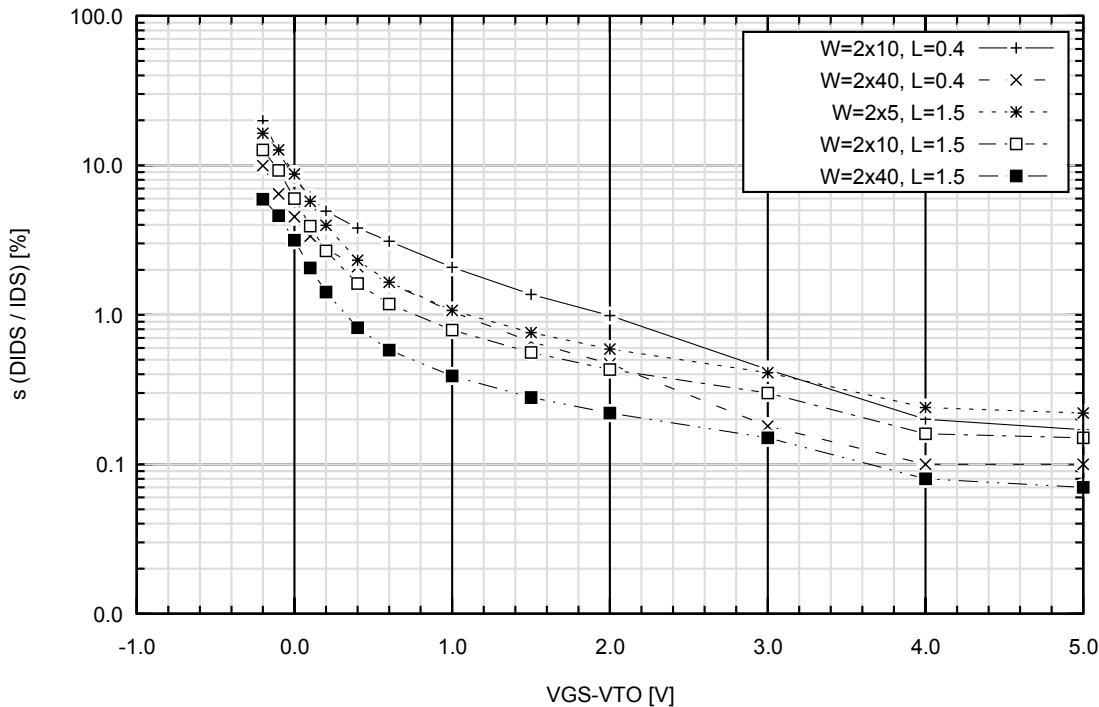


Figure 3.53 Device nhvta: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhvtaa

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-42	-40	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	40	42	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	40	42	V
VD-HW	-40°C to 175°C	-110	-100	200	220	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVTAA	drain-source breakdown @ VG=0V, Id=1µA, L=0.4µm	45	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNHVTAA	pulsed saturation current @ VG=5V, VD=10V, Dcyc=1%, Pwid=100ns, L=0.4µm, W=100µm, NF=4, WF=25µm	-	-	302	-	-	µA/µm

3. Parameters → 3.29 NHVA module→ 3.29.2 Device parameters→ nhvtaa→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDS_NHVTAA	saturation current @ VG=5V, VD=10V, L=0.4μm, W=100μm, NF=4, WF=25μm	150	175	200	225	250	μA/μm
KP_NHVTAA	gain factor long channel @ L=1.5μm, W=100μm, NF=4, WF=25μm	-	-	5310	-	-	μA/V ²
ROA_NHVTAA	area specific on resistance @ VG=5V, VD=0.1V, L=0.4μm, W=100μm, Pitch=2.89μm, NF=4, WF=25μm	-	-	26	29.8	-	mΩmm ²
RO_NHVTAA	on resistance @ VG=5V, VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	6.4	7.7	9	10.3	11.6	kΩμm
TC_VTXNHVTAA	threshold voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VT1_NHVTAA	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	53	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTI_NHVTAA	threshold voltage @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	-	1.03	1.1	1.17	-	V
VTX_NHVTAA	extrapolated threshold voltage @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	0.91	0.99	1.07	1.15	1.23	V
VTX_NHVTAA	extrapolated threshold voltage long channel @ VD=0.1V, L=1.5μm, W=100μm, NF=4, WF=25μm	-	-	0.93	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHVTAA	pelgrom coefficient gain factor mismatch	5.53	%μm
AID_NHVTAA00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.79	%μm
AID_NHVTAA02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.66	%μm
AID_NHVTAA04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	10.16	%μm
AID_NHVTAA06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	7.86	%μm
AID_NHVTAA10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	5.2	%μm
AID_NHVTAA20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	2.59	%μm
AID_NHVTAA30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.36	%μm
AID_NHVTAA50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.63	%μm
AVT_NHVTAA	pelgrom coefficient threshold voltage mismatch	19.8	mVμm
DLT_NHVTAA	transistor delta length	0	μm
DWT_NHVTAA	transistor delta width	0	μm

Note: <p>

Matching parameters are copied over from nhvta.

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3. Parameters → 3.29 NHVA module → 3.29.2 Device parameters → nhvtaa → Matching parameters

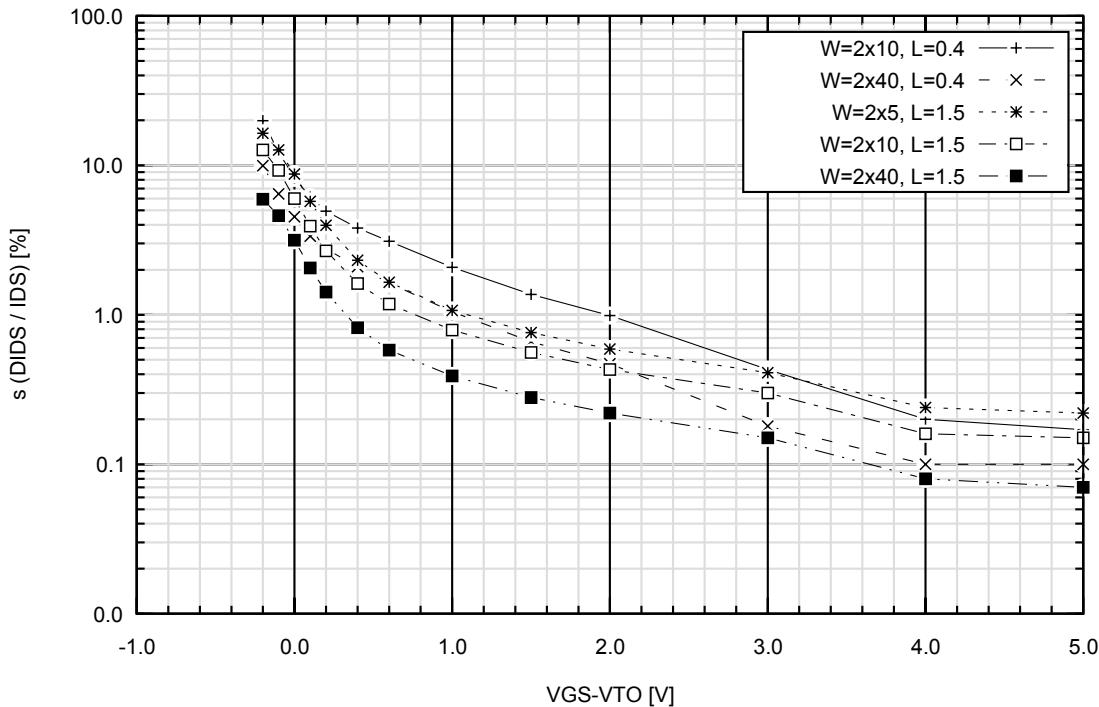


Figure 3.54 Device nhvta: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhvtb

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-42	-40	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	40	42	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	40	42	V
VD-HW	-40°C to 175°C	-110	-100	200	220	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVTB	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	50	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNHVTB	pulsed saturation current @ VG=5V, VD=10V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=100µm, NF=4, WF=25µm	-	-	272	-	-	µA/µm

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3. Parameters → 3.29 NHVA module→ 3.29.2 Device parameters→ nhvtb→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDS_NHVTB	saturation current @ VG=5V, VD=10V, L=0.5μm, W=100μm, NF=4, WF=25μm	150	170	190	210	230	μA/μm
KP_NHVTBL	gain factor long channel @ L=10μm, W=100μm, NF=4, WF=25μm	-	-	1295	-	-	μA/V ²
ROA_NHVTB	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=100μm, Pitch=4.29μm, NF=4, WF=25μm	-	-	52.3	58.8	-	mΩmm ²
RO_NHVTB	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	9.2	10.7	12.2	13.7	15.2	kΩμm
TC_VTXNHVTB	threshold voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VT1_NHVTB	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	77	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTI_NHVTB	threshold voltage @ VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	-	0.98	1.05	1.12	-	V
VTX_NHVTB	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	0.87	0.95	1.03	1.11	1.19	V
VTX_NHVTBL	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=100μm, NF=4, WF=25μm	-	-	0.82	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHVTB	pelgrom coefficient gain factor mismatch @ L=0.5μm	3.92	%μm
AID_NHVTB00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V, L=0.5μm	40.35	%μm
AID_NHVTB02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V, L=0.5μm	18.79	%μm
AID_NHVTB04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V, L=0.5μm	10.09	%μm
AID_NHVTB06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V, L=0.5μm	6.63	%μm
AID_NHVTB10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V, L=0.5μm	4.24	%μm
AID_NHVTB20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V, L=0.5μm	2.32	%μm
AID_NHVTB30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V, L=0.5μm	1	%μm
AID_NHVTB50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V, L=0.5μm	0.54	%μm
AVT_NHVTB	pelgrom coefficient threshold voltage mismatch @ L=0.5μm	23.52	mVμm
DLT_NHVTB	transistor delta length	0	μm
DWT_NHVTB	transistor delta width	0	μm

3. Parameters → 3.29 NHVA module→ 3.29.2 Device parameters→ nhvtb→ Matching parameters

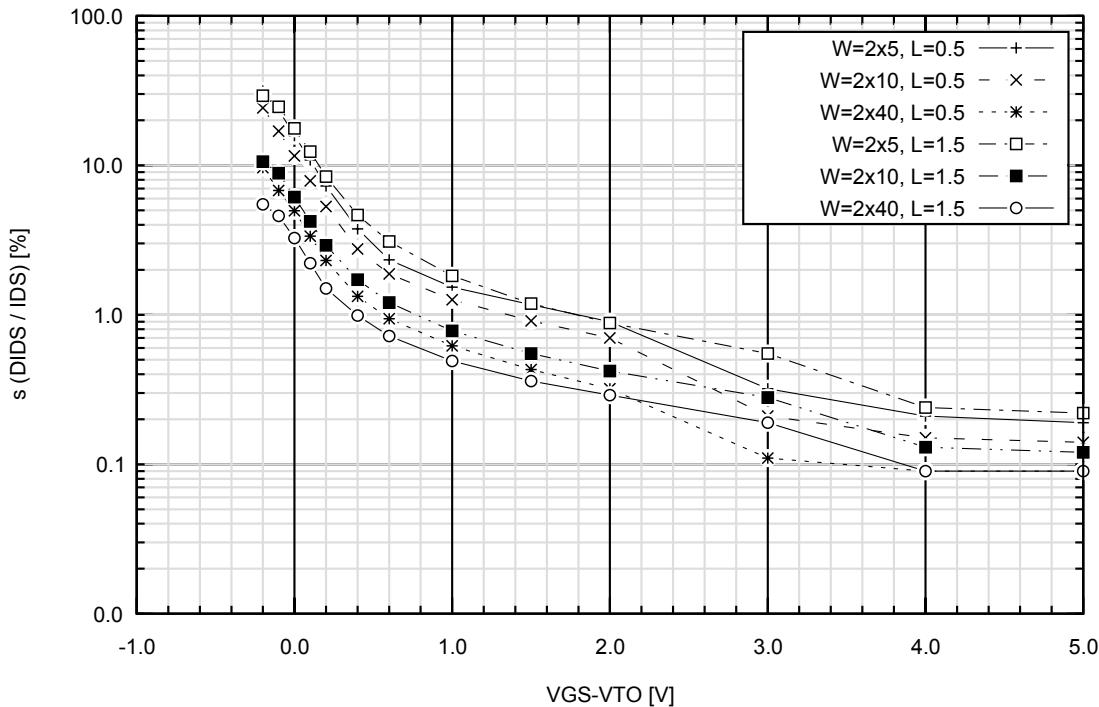


Figure 3.55 Device nhvtb: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhvu

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-62	-60	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	60	62	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	60	62	V
VD-HW	-40°C to 175°C	-110	-100	60	62	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVU	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	65	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDPNHVU	pulsed saturation current @ VG=5V, VD=10V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=100µm, NF=4, WF=25µm	-	-	235	-	-	µA/µm

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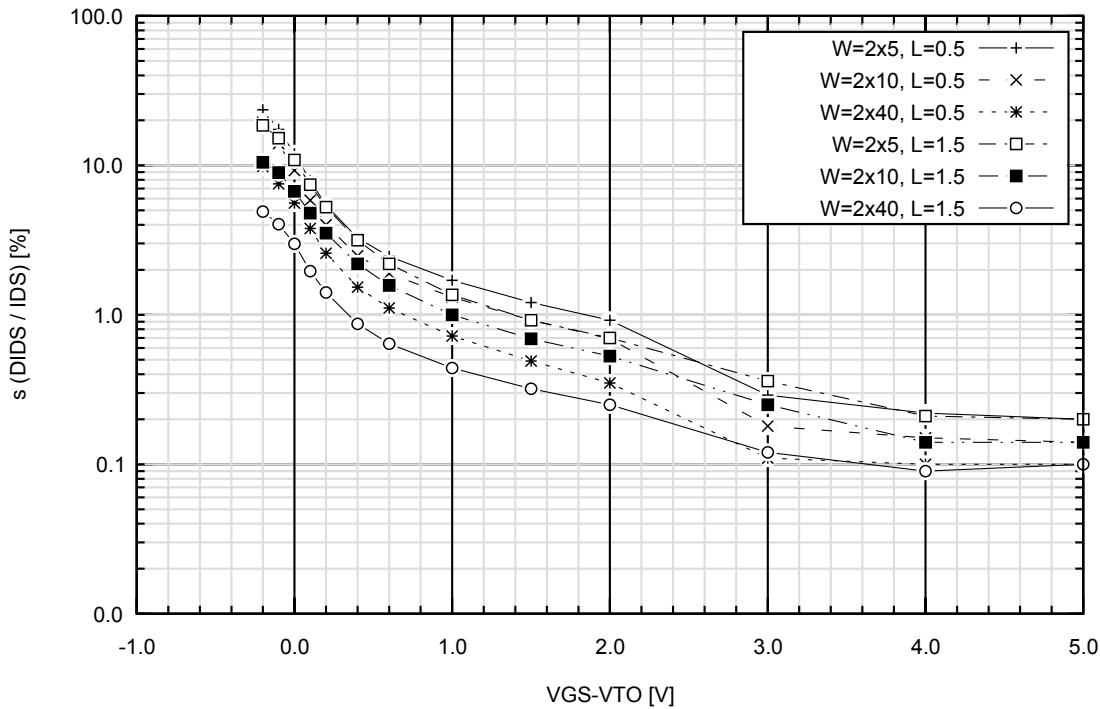
3. Parameters → 3.29 NHVA module→ 3.29.2 Device parameters→ nhvu→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDS _{NHVU}	saturation current @ VG=5V, VD=10V, L=0.5μm, W=100μm, NF=4, WF=25μm	128	148	168	188	208	μA/μm
KP _{NHVUL}	gain factor long channel @ L=10μm, W=100μm, NF=4, WF=25μm	-	-	1245	-	-	μA/V ²
ROA _{NHVU}	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=100μm, Pitch=6.34μm, NF=4, WF=25μm	-	-	114	130	-	mΩmm ²
RO _{NHVU}	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	13	15.5	18	20.5	23	kΩμm
TC _{VTXNHVU}	threshold voltage temperature coefficient	-	-	-1.7	-	-	mV/K
VT1 _{NHVU}	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	114	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTI _{NHVU}	threshold voltage @ VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	-	0.97	1.05	1.13	-	V
VTX _{NHVU}	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	0.84	0.92	1	1.08	1.16	V
VTX _{NHVUL}	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=100μm, NF=4, WF=25μm	-	-	0.83	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABT _{NHVU}	pelgrom coefficient gain factor mismatch	3.77	%μm
AID _{NHVU00}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	31.03	%μm
AID _{NHVU02}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.36	%μm
AID _{NHVU04}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	8.72	%μm
AID _{NHVU06}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	6.43	%μm
AID _{NHVU10}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.3	%μm
AID _{NHVU20}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	2.28	%μm
AID _{NHVU30}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.82	%μm
AID _{NHVU50}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.54	%μm
AVT _{NHVU}	pelgrom coefficient threshold voltage mismatch	18.43	mVμm
DLT _{NHVU}	transistor delta length	0	μm
DWT _{NHVU}	transistor delta width	0	μm

3. Parameters → 3.29 NHVA module→ 3.29.2 Device parameters→ nhvu→ Matching parameters

**Figure 3.56** Device nhvu: drain current matching vs. VGS-VTO (typical values, drawn W and L)**dfwdnt****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-42	-40	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-110	-100	200	220	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDNT	breakdown voltage @ Irev=1μA, L=3.36μm, W=25μm, NF=4	50	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
TC_VDFDFWDNT	forward voltage temperature coefficient	-	-	-1.9	-	-	mV/K
VDFDFWDNT	diode forward voltage @ Idio=1μA, L=3.36μm, W=100μm, NF=4, WF=25μm	0.662	0.667	0.672	0.677	0.682	V

3. Parameters → 3.29 NHVA module → 3.29.2 Device parameters → dfwdnu → Operating conditions

dfwdnu

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-62	-60	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-110	-100	60	62	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDNU	breakdown voltage @ Irev=1μA, L=5.41μm, W=25μm, NF=4	65	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
TC_VDFDFWDNU	forward voltage temperature coefficient	-	-	-1.9	-	-	mV/K
VDFDFWDNU	diode forward voltage @ Idio=1μA, L=5.41μm, W=100μm, NF=4, WF=25μm	0.662	0.667	0.672	0.677	0.682	V

dnpa

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-9	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	μA/μm
Ibr1000	-40°C to 175°C	-	-	5	-	μA/μm

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DNPA	breakdown voltage @ Irev=10μA, L=1μm, W=10μm	7.5	7.713	7.925	8.088	8.25	V
IL_DNPA	leakage current @ VL=4.5V, T=27°C, L=1μm, W=10μm	-	-	0.09	-	-	pA
IL_DNPAHT	leakage current @ VL=4.5V, T=175°C, L=1μm, W=10μm	-	-	200	-	-	pA
TC_BVDNPA	breakdown temperature coefficient	-	-	4.2	-	-	mV/K

dnpati

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-9	0	0.5	V

3. Parameters → 3.29 NHVA module→ 3.29.2 Device parameters→ dnpati→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	5	-	µA/µm

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DNPATI	breakdown voltage @ Irev=10µA, L=1µm, W=10µm	7.5	7.713	7.925	8.088	8.25	V
IL_DNPATI	leakage current @ VL=4.5V, T=27°C, L=1µm, W=10µm	-	-	0.09	-	-	pA/µm ²
IL_DNPATIHT	leakage current @ VL=4.5V, T=175°C, L=1µm, W=10µm	-	-	200	-	-	pA
TC_BVDNPATI	breakdown temperature coefficient	-	-	4.2	-	-	mV/K

3. Parameters → 3.30 NHVR module

3.30 NHVR module

3.30.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_DFN	HVMOS N-drift junction depth	3.5	μm
Note: DFN layers reaches BOX when drawn in ACTIVE			

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSDFN	DFN sheet resistance in PDD (DTI terminated) @ W=5μm	3.9	kΩ/□
RSSPDD	PDD sheet resistance in DFN (DTI terminated) @ W=5μm	23.8	kΩ/□

3.30.2 Device parameters

nhvra

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-44	-40	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	40	44	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	40	44	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVRA	drain-source breakdown @ VG=0V, Id=1μA, L=0.4μm	46	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNHVRA	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, NF=2, WF=25μm	-	-	300	-	-	μA/μm
IDSNHVRA	saturation current @ VG=5V, VD=20V, L=0.4μm, W=100μm, NF=4, WF=25μm	134	154	174	194	214	μA/μm
KP_NHVRAL	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	713	-	-	μA/V ²

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3. Parameters → 3.30 NHVR module→ 3.30.2 Device parameters→ nhvra→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROANHVRA	area specific on resistance @ VG=5V, VD=0.1V, L=0.4μm, W=100μm, Pitch=3.5μm, NF=4, WF=25μm	-	-	45	49	-	mΩmm ²
RONNHVRA	on resistance @ VG=5V, VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	10.1	11.4	12.7	14	15.3	kΩμm
TC_VTXNHVRA	threshold voltage temperature coefficient	-	-	-1.7	-	-	mV/K
VT1NHVRA	snap-back trigger voltage @ VGS=5V, Ngates=8, WF=40μm	-	-	60	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTXNHVRAL	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=50μm, NF=2, WF=25μm	-	-	0.88	-	-	V
VTXNHVRAS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	0.86	0.96	1.06	1.16	1.26	V

nhvrb

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-66	-60	5.5	7	V
VDS⁽¹⁾	-40°C to 175°C	-	-1.5	60	66	V
VDB⁽¹⁾	-40°C to 175°C	-	-1.5	60	66	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V
If⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVRB	drain-source breakdown @ VG=0V, Id=1μA, L=0.4μm	69	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNHVRB	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, NF=2, WF=25μm	-	-	230	-	-	μA/μm
IDSNHVRB	saturation current @ VG=5V, VD=20V, L=0.4μm, W=100μm, NF=4, WF=25μm	117	134	151	168	185	μA/μm

3. Parameters → 3.30 NHVR module→ 3.30.2 Device parameters→ nhvrb→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
KP_NHVRBL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	735	-	-	µA/V ²
ROANHVRB	area specific on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, Pitch=4.6µm, NF=4, WF=25µm	-	-	75	82.3	-	mΩmm ²
RONNHVRB	on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	13.1	14.7	16.3	17.9	19.5	kΩµm
TC_VTXNHVRB	threshold voltage temperature coefficient	-	-	-1.7	-	-	mV/K
VT1NHVRB	snap-back trigger voltage @ VGS=5V, Ngates=8, WF=40µm	-	-	85	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTXNHVRBL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	0.93	-	-	V
VTXNHVRBS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	0.88	0.98	1.08	1.18	1.28	V

nhvrc

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-77	-70	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	70	77	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	70	77	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVRC	drain-source breakdown @ VG=0V, Id=1µA, L=0.4µm	81	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNHVRC	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, NF=2, WF=25µm	-	-	210	-	-	µA/µm



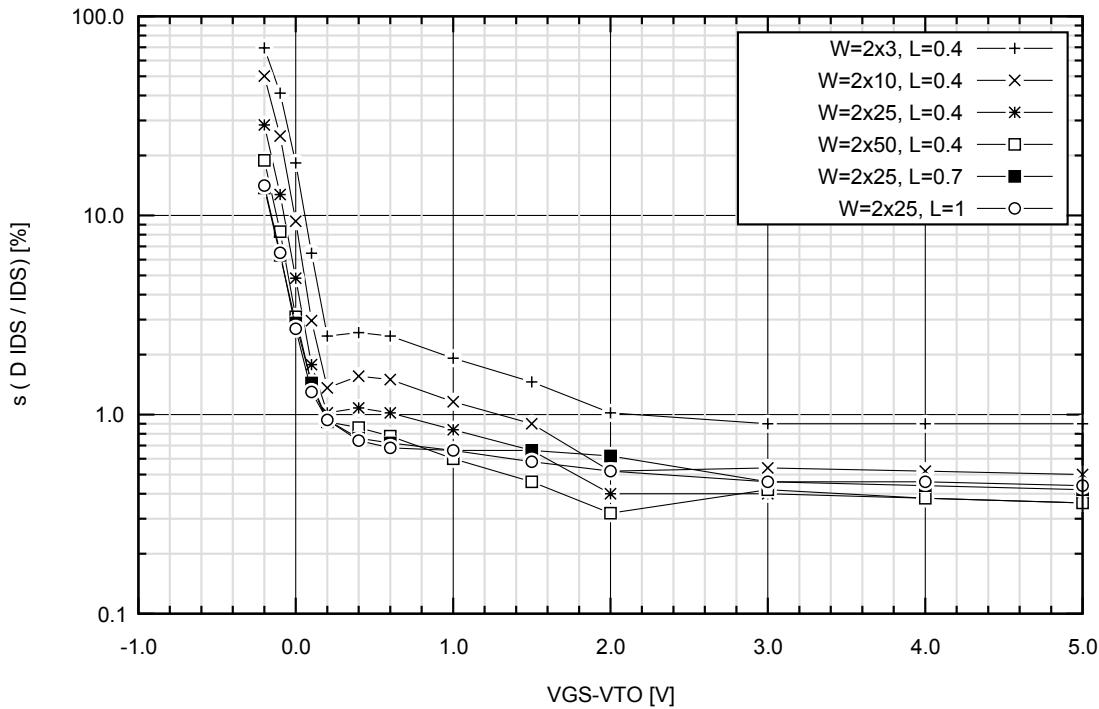
3. Parameters → 3.30 NHVR module→ 3.30.2 Device parameters→ nhvrc→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDS _{NHVRC}	saturation current @ VG=5V, VD=20V, L=0.4μm, W=100μm, NF=4, WF=25μm	111	127	143	159	175	μA/μm
KP _{NHVRCL}	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	763	-	-	μA/V ²
ROA _{NHVRC}	area specific on resistance @ VG=5V, VD=0.1V, L=0.4μm, W=100μm, Pitch=5.1μm, NF=4, WF=25μm	-	-	93	103	-	mΩmm ²
RON _{NHVRC}	on resistance @ VG=5V, VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	14.6	16.4	18.3	20.1	22	kΩμm
TC _{VTXNHVRC}	threshold voltage temperature coefficient	-	-	-1.7	-	-	mV/K
VT1 _{NHVRC}	snap-back trigger voltage @ VGS=5V, Ngates=8, WF=40μm	-	-	96	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTX _{NHVRCL}	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=50μm, NF=2, WF=25μm	-	-	0.97	-	-	V
VTX _{NHVRCS}	extrapolated threshold voltage short channel @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	0.89	0.99	1.09	1.19	1.29	V

Matching parameters

Name	Description	Typ	Unit
ABT _{NHVRC}	pelgrom coefficient gain factor mismatch	2.11	%μm
AID _{NHVRCC00}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	29.52	%μm
AID _{NHVRCC02}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	4.58	%μm
AID _{NHVRCC04}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	4.64	%μm
AID _{NHVRCC06}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.5	%μm
AID _{NHVRCC10}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	3.74	%μm
AID _{NHVRCC20}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	2.06	%μm
AID _{NHVRCC30}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.88	%μm
AID _{NHVRCC50}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1.82	%μm
AVT _{NHVRC}	pelgrom coefficient threshold voltage mismatch	13.68	mVμm
DLT _{NHVRC}	transistor delta length	0	μm
DWT _{NHVRC}	transistor delta width	0	μm

3. Parameters → 3.30 NHVR module → 3.30.2 Device parameters → nhvrc → Matching parameters

**Figure 3.57** Device nhvrc: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nhvrd**

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-93	-85	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	85	93	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	85	93	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVRD	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	97	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

3. Parameters → 3.30 NHVR module→ 3.30.2 Device parameters→ nhvrd→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDPNHVRD	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, NF=2, WF=25µm	-	-	190	-	-	µA/µm
IDSNHVRD	saturation current @ VG=5V, VD=20V, L=0.5µm, W=100µm, NF=4, WF=25µm	105	120	135	150	165	µA/µm
KP_NHVRDL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	787	-	-	µA/V ²
ROANHVRD	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=100µm, Pitch=6µm, NF=4, WF=25µm	-	-	124	137	-	mΩmm ²
RONHVRD	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	16.6	18.6	20.7	22.8	24.8	kΩµm
TC_VTXNHVRD	threshold voltage temperature coefficient	-	-	-1.8	-	-	mV/K
VT1NHVRD	snap-back trigger voltage @ VGS=5V, Ngates=8, WF=40µm	-	-	110	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"						
VTXNHVRDL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	1.01	-	-	V
VTXNHVRDS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	0.87	0.97	1.07	1.17	1.27	V

Matching parameters

Name	Description	Typ	Unit
ABTNHVRD	pelgrom coefficient gain factor mismatch	1.89	%µm
AIDNHVRD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	25.46	%µm
AIDNHVRD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	4.78	%µm
AIDNHVRD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	3.7	%µm
AIDNHVRD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	3.46	%µm
AIDNHVRD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.9	%µm
AIDNHVRD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.84	%µm
AIDNHVRD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.94	%µm
AIDNHVRD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1.9	%µm
AVTNHVRD	pelgrom coefficient threshold voltage mismatch	13.03	mVµm
DLTNHVRD	transistor delta length	0	µm
DWTNHVRD	transistor delta width	0	µm

3. Parameters → 3.30 NHVR module → 3.30.2 Device parameters → nhvrd → Matching parameters

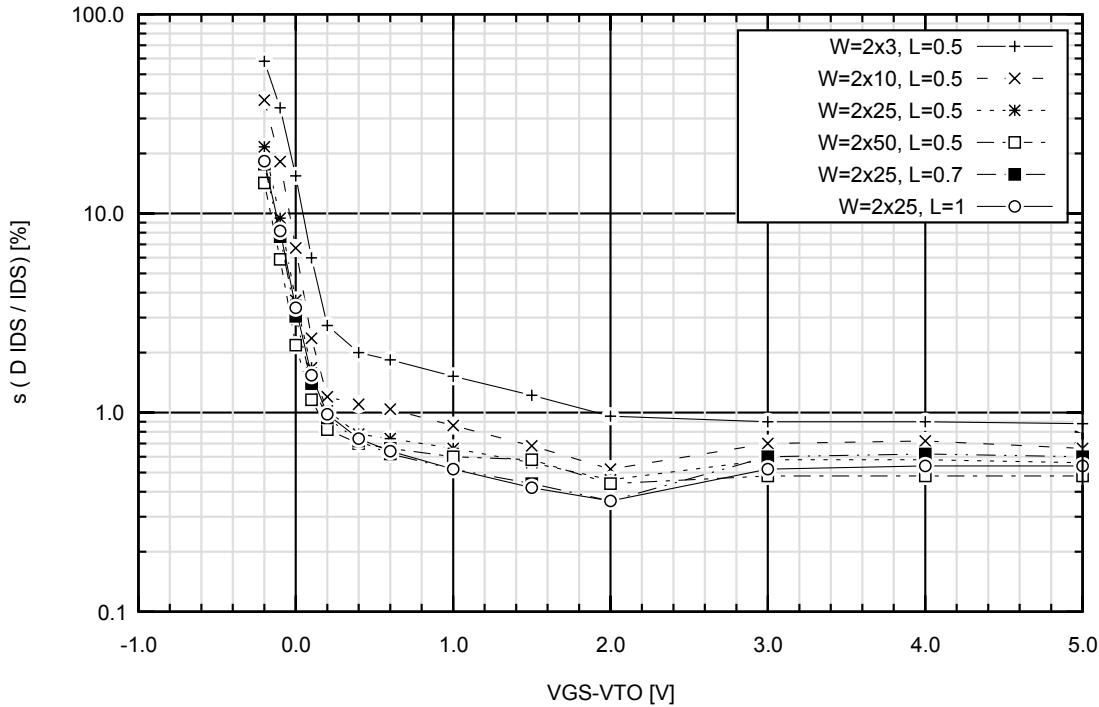


Figure 3.58 Device nhvrd: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhvre

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-110	-100	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	100	110	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	100	110	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVRE	drain-source breakdown @ VG=0V, Id=1µA, L=0.5µm	115	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

3. Parameters → 3.30 NHVR module→ 3.30.2 Device parameters→ nhvre→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDPNHVR	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, NF=2, WF=25µm	-	-	170	-	-	µA/µm
IDSNHVR	saturation current @ VG=5V, VD=20V, L=0.5µm, W=100µm, NF=4, WF=25µm	96	110	124	138	152	µA/µm
KP_NHVREL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	802	-	-	µA/V ²
ROANHVR	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=100µm, Pitch=7.2µm, NF=4, WF=25µm	-	-	188	207	-	mΩmm ²
RONHVR	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	20.8	23.4	26	28.6	31.2	kΩµm
TC_VTXNHVR	threshold voltage temperature coefficient	-	-	-1.8	-	-	mV/K
VT1NHVR	snap-back trigger voltage @ VGS=5V, Ngates=8, WF=40µm	-	-	130	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTXNHVREL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	1.05	-	-	V
VTXNHVRES	extrapolated threshold voltage short channel @ VD=0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	0.9	1	1.1	1.2	1.3	V

Matching parameters

Name	Description	Typ	Unit
ABTNHVR	pelgrom coefficient gain factor mismatch	2.28	%µm
AIDNHVRE00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	26.3	%µm
AIDNHVRE02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	4.94	%µm
AIDNHVRE04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	4.26	%µm
AIDNHVRE06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	3.96	%µm
AIDNHVRE10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	3.18	%µm
AIDNHVRE20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.96	%µm
AIDNHVRE30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	2.44	%µm
AIDNHVRE50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	2.42	%µm
AVTNHVR	pelgrom coefficient threshold voltage mismatch	14.68	mVµm
DLTNHVR	transistor delta length	0	µm
DWTNHVR	transistor delta width	0	µm

3. Parameters → 3.30 NHVR module → 3.30.2 Device parameters → nhvre → Matching parameters

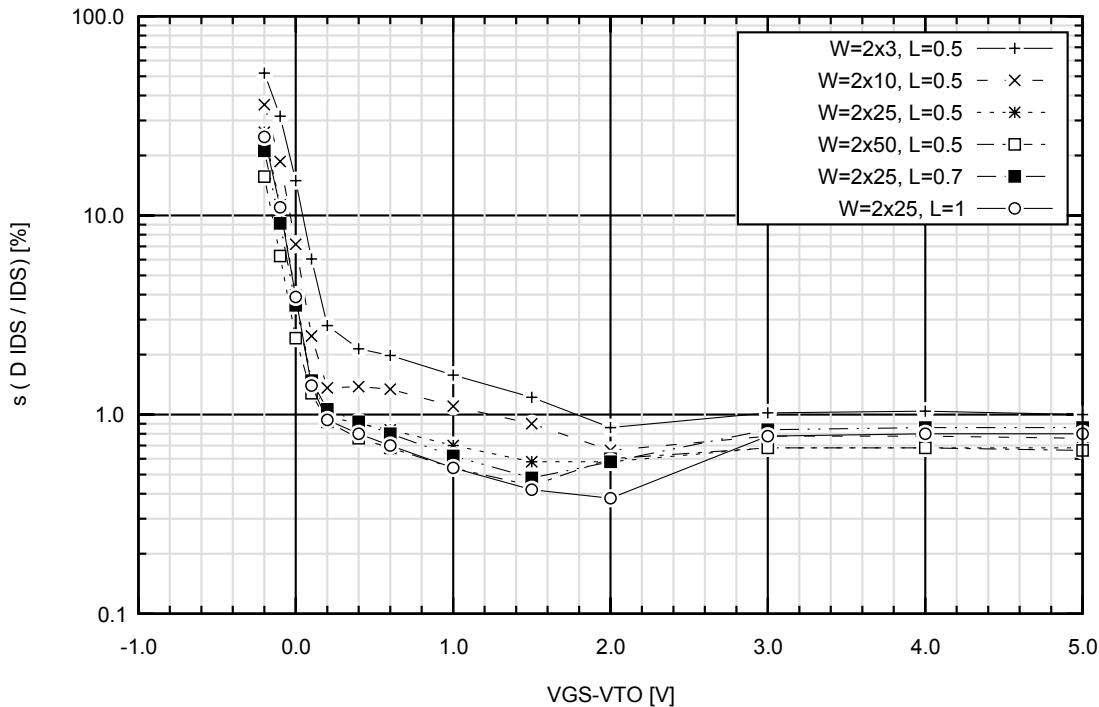


Figure 3.59 Device nhvre: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhvrf

This device is intended to enhance the ESD design window for 100V applications. The ESD design window may not be suitable for applications up to 125V.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-127	-125	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	125	127	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	125	127	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This forward current is allowed only for transistor's drain bulk junction

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL4

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHVRF	drain-source breakdown @ VG=0V, Id=1μA, L=0.5μm	133	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							⇒

3. Parameters → 3.30 NHVR module→ 3.30.2 Device parameters→ nhvrf→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDPNHVRF	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, NF=4, WF=25μm	-	-	140	-	-	μA/μm
IDS_NHVRF	saturation current @ VG=5V, VD=20V, L=0.5μm, W=100μm, NF=4, WF=25μm	86	99	112	125	138	μA/μm
KP_NHVRFL	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	822	-	-	μA/V ²
ROANHVRF	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=100μm, Pitch=9.2μm, NF=4, WF=25μm	-	-	303	334	-	mΩmm ²
RON_NHVRF	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	26.3	29.6	32.9	36.2	39.5	kΩμm
TC_VTXNHVRF	threshold voltage temperature coefficient	-	-	-1.8	-	-	mV/K
VT1_NHVRF	snap-back trigger voltage @ VGS=5V, Ngates=8, WF=40μm	-	-	156	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTX_NHVRFL	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=50μm, NF=2, WF=25μm	-	-	1.14	-	-	V
VTX_NHVRFS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	0.95	1.05	1.15	1.25	1.35	V

dfwdnhc**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-77	-70	1.5	-	V
Vcathode-HW	-40°C to 175°C	-27	-25	125	127	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽¹⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDNHC	breakdown voltage @ Irev=1μA, L=4μm, W=25μm	81	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DFWDNHC	leakage current @ VL=70V, T=27°C, W=200μm, NF=2, WF=100μm	-	-	5.4	-	-	pA
IL_DFWDNHCHT	leakage current @ VL=70V, T=175°C, W=200μm, NF=2, WF=100μm	-	-	4.9	-	-	nA
TC_VDFDFWDNHC	forward voltage temperature coefficient	-	-	-1.4	-	-	mV/K



3. Parameters → 3.30 NHVR module → 3.30.2 Device parameters → dfwdnhd → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VDFDFWDNHC	diode forward voltage @ Idio=100µA, L=4.16µm, W=100µm, NF=4, WF=25µm	0.76	0.78	0.8	0.82	0.84	V

dfwdnhd

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-97	-85	1.5	-	V
Vcathode-HW	-40°C to 175°C	-27	-25	125	127	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽¹⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDNHD	breakdown voltage @ Irev=1µA, L=4µm, W=25µm	97	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DFWDNHD	leakage current @ VL=85V, T=27°C, W=200µm, NF=2, WF=100µm	-	-	5.9	-	-	pA
IL_DFWDNHDHT	leakage current @ VL=85V, T=175°C, W=200µm, NF=2, WF=100µm	-	-	5.7	-	-	nA
TC_VDFDFWDNHD	forward voltage temperature coefficient	-	-	-1.4	-	-	mV/K
VDFDFWDNHD	diode forward voltage @ Idio=100µA, L=4.96µm, W=100µm, NF=4, WF=25µm	0.76	0.78	0.8	0.82	0.84	V

dfwdnhe

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-110	-100	1.5	-	V
Vcathode-HW	-40°C to 175°C	-27	-25	125	127	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽¹⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDNHE	breakdown voltage @ Irev=1µA, L=4µm, W=25µm	115	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DFWDNHE	leakage current @ VL=100V, T=27°C, W=200µm, NF=2, WF=100µm	-	-	5.3	-	-	pA

3. Parameters → 3.30 NHVR module→ 3.30.2 Device parameters→ dfwdnhe→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IL_DFWDNHEHT	leakage current @ VL=100V, T=175°C, W=200µm, NF=2, WF=100µm	-	-	6.7	-	-	nA
TC_VDFDFWDNHE	forward voltage temperature coefficient	-	-	-1.4	-	-	mV/K
VDFDFWDNHE	diode forward voltage @ Idio=100µA, L=6.16µm, W=100µm, NF=4, WF=25µm	0.76	0.78	0.8	0.82	0.84	V

dfwdnhf

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-127	-125	1.5	-	V
Vcathode-HW	-40°C to 175°C	-27	-25	125	127	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽¹⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDNHF	breakdown voltage @ Irev=1µA, L=4µm, W=25µm	133	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DFWDNHF	leakage current @ VL=125V, T=27°C, W=200µm, NF=2, WF=100µm	-	-	2.6	-	-	pA
IL_DFWDNFHT	leakage current @ VL=125V, T=175°C, W=200µm, NF=2, WF=100µm	-	-	6.6	-	-	nA
TC_VDFDFWDNHF	forward voltage temperature coefficient	-	-	-1.4	-	-	mV/K
VDFDFWDNHF	diode forward voltage @ Idio=100µA, L=8.16µm, W=100µm, NF=4, WF=25µm	0.76	0.78	0.8	0.82	0.84	V

dnpa

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-9	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	5	-	µA/µm

Note 1 This operating condition will not be checked by automatic check tools.

3. Parameters → 3.30 NHVR module → 3.30.2 Device parameters → dnpa → Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DNPA	breakdown voltage @ Irev=10µA, L=1µm, W=10µm	7.5	7.713	7.925	8.088	8.25	V
IL_DNPA	leakage current @ VL=4.5V, T=27°C, L=1µm, W=10µm	-	-	0.09	-	-	pA
IL_DNPAHT	leakage current @ VL=4.5V, T=175°C, L=1µm, W=10µm	-	-	200	-	-	pA
TC_BVDNPA	breakdown temperature coefficient	-	-	4.2	-	-	mV/K

dnpati

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-9	0	0.5	V
VA-HW⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	5	-	µA/µm

Note 1 This operating condition will not be checked by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DNPATI	breakdown voltage @ Irev=10µA, L=1µm, W=10µm	7.5	7.713	7.925	8.088	8.25	V
IL_DNPATI	leakage current @ VL=4.5V, T=27°C, L=1µm, W=10µm	-	-	0.09	-	-	pA/µm ²
IL_DNPATIHT	leakage current @ VL=4.5V, T=175°C, L=1µm, W=10µm	-	-	200	-	-	pA
TC_BVDNPATI	breakdown temperature coefficient	-	-	4.2	-	-	mV/K

3. Parameters → 3.31 NMV module

3.31 NMV module

3.31.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_NDFMV	NDFMV junction depth	1	μm

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSEMV	ESDMV sheet resistance (DTI terminated) @ W=5μm	0.63	kΩ/□
RSSNMVN	NDFMV(n) sheet resistance (DTI terminated) @ W=2μm	2.5	kΩ/□
RSSNMVP	NDFMV(p) sheet resistance (DTI terminated) @ W=2μm	25	kΩ/□

3.31.2 Device parameters

nmvb

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-13	-12	5.5	7	V
VDS	-40°C to 175°C	-	-1.5	12	13	V
VDB	-40°C to 175°C	-	-1.5	12	13	V
VD-HW	-40°C to 175°C	-27	-25	400	440	V
If ⁽¹⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽²⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 This forward current is allowed only for transistor's drain bulk junction

Note 2 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMVB	drain-source breakdown @ VG=0V, Id=1μA, L=0.4μm	13.8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNMVB	pulsed drain current @ VG=5V, VD=5V, Dcyc=1%, Pwid=100ns, NF=4, WF=25μm	-	-	457	-	-	μA/μm
IDSNMVB	saturation current @ VG=5V, VD=5V, L=0.4μm, W=100μm, NF=4, WF=25μm	228	266	304	342	380	μA/μm
KP_NMVBL	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	550	-	-	μA/V ²
ROANMVB	area specific on resistance @ VG=5V, VD=0.1V, L=0.4μm, W=100μm, Pitch=1.86μm, NF=4, WF=25μm	-	-	7.4	8.7	-	mΩmm ²
RONNMVB	on resistance @ VG=5V, VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	2.6	3.3	4	4.7	5.4	kΩμm

3. Parameters → 3.31 NMV module → 3.31.2 Device parameters → nmvb → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VTXNMVB	threshold voltage temperature coefficient	-	-	-1.3	-	-	mV/K
VT1NMVB	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=40μm	-	-	30	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 TLP Characteristics" at "my X-FAB"						
VTXNMVBL	extrapolated threshold voltage long channel @ VD=0.1V, L=10μm, W=50μm, NF=2, WF=25μm	-	-	0.72	-	-	V
VTXNMVBS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	0.67	0.75	0.82	0.89	0.97	V

Matching parameters

Name	Description	Typ	Unit
ABTNMVD	pelgrom coefficient gain factor mismatch	3.44	%μm
AIDNMVD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	40.6	%μm
AIDNMVD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.6	%μm
AIDNMVD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	9.8	%μm
AIDNMVD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8	%μm
AIDNMVD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	6	%μm
AIDNMVD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	3.6	%μm
AIDNMVD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	2.5	%μm
AIDNMVD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1	%μm
AVTNMVD	pelgrom coefficient threshold voltage mismatch	20.78	mVμm
DLTNMVD	transistor delta length	0	μm
DWTNMVD	transistor delta width	0	μm

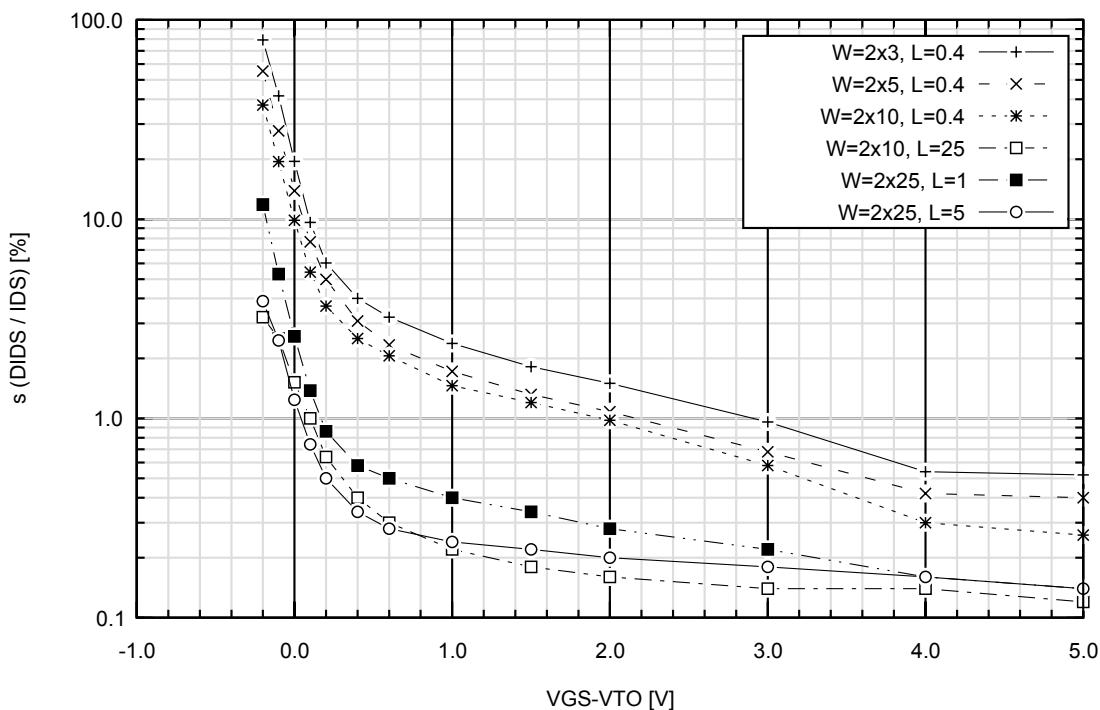


Figure 3.60 Device nmvd: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.31 NMV module→ 3.31.2 Device parameters→ nmvc→ Operating conditions

nmvc**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-16.5	-15	5.5	7	V
VDS	-40°C to 175°C	-	-1.5	15	16.5	V
VDB	-40°C to 175°C	-	-1.5	15	16.5	V
VD-HW	-40°C to 175°C	-27	-25	400	440	V
If ⁽¹⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽²⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 This forward current is allowed only for transistor's drain bulk junction**Note 2** Pulsed operation with negligible self-heating (<=100ns)**Process parameters**

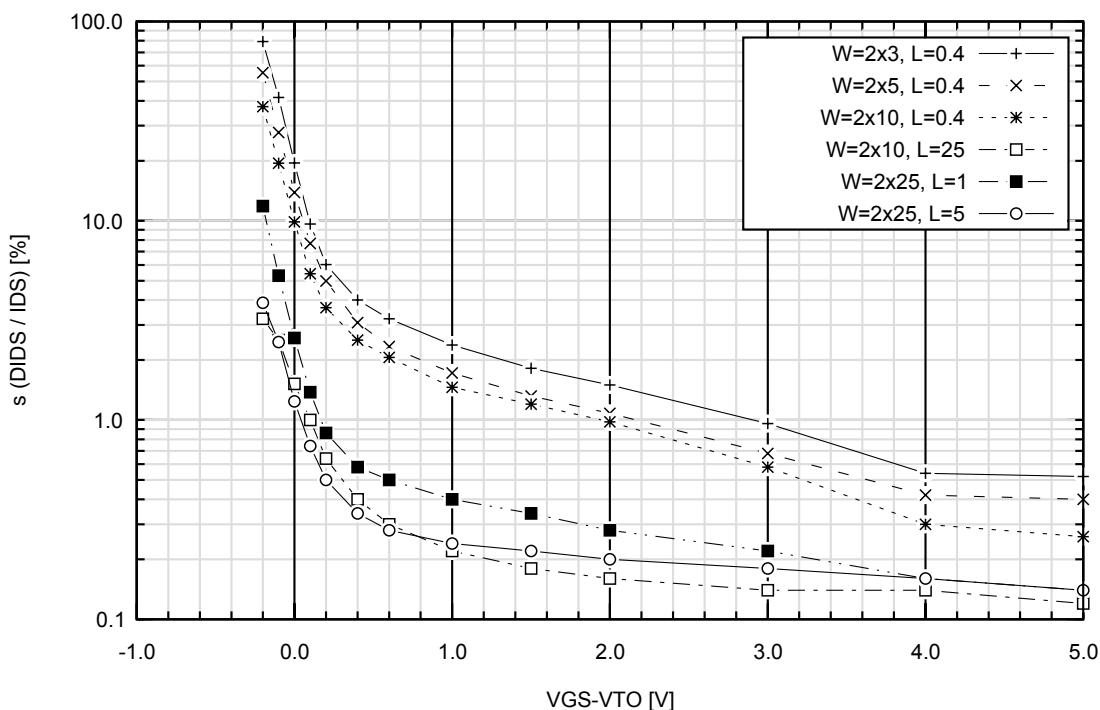
Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMVC	drain-source breakdown @ VG=0V, Id=1µA, L=0.4µm	17.3	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNMVC	pulsed drain current @ VG=5V, VD=6V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	420	-	-	µA/µm
IDSNMVC	saturation current @ VG=5V, VD=6V, L=0.4µm, W=100µm, NF=4, WF=25µm	212	247	282	317	352	µA/µm
KP_NMVCL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	550	-	-	µA/V ²
ROANMVC	area specific on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, Pitch=1.96µm, NF=4, WF=25µm	-	-	8.8	10.2	-	mΩmm ²
RONNMVC	on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	3.1	3.8	4.5	5.2	5.9	kΩµm
TC_VTXNMVC	threshold voltage temperature coefficient	-	-	-1.3	-	-	mV/K
VT1NMVC	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=40µm	-	-	32	-	-	V
Note: For detailed TLP I-V characteristics, refer to "XT018 TLP Characteristics" at "my X-FAB"							
VTXNMVCL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	0.72	-	-	V
VTXNMVCS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	0.67	0.75	0.82	0.89	0.97	V

Matching parameters

Name	Description	Typ	Unit
ABTNMVD	pelgrom coefficient gain factor mismatch	3.44	%µm
AIDNMVD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	40.6	%µm
AIDNMVD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.6	%µm

3. Parameters → 3.31 NMV module→ 3.31.2 Device parameters→ nmvc→ Matching parameters

Name	Description	Typ	Unit
AIDNMVD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	9.8	%μm
AIDNMVD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8	%μm
AIDNMVD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	6	%μm
AIDNMVD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	3.6	%μm
AIDNMVD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	2.5	%μm
AIDNMVD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1	%μm
AVTNMVD	pelgrom coefficient threshold voltage mismatch	20.78	mVμm
DLTNMVD	transistor delta length	0	μm
DWTNMVD	transistor delta width	0	μm

**Figure 3.61** Device nmvd: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nmvd****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-22	-20	5.5	7	V
VDS	-40°C to 175°C	-	-1.5	20	22	V
VDB	-40°C to 175°C	-	-1.5	20	22	V
VD-HW	-40°C to 175°C	-27	-25	400	440	V
If ⁽¹⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽²⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 This forward current is allowed only for transistor's drain bulk junction**Note 2** Pulsed operation with negligible self-heating (<=100ns)

3. Parameters → 3.31 NMV module→ 3.31.2 Device parameters→ nmvd→ Process parameters

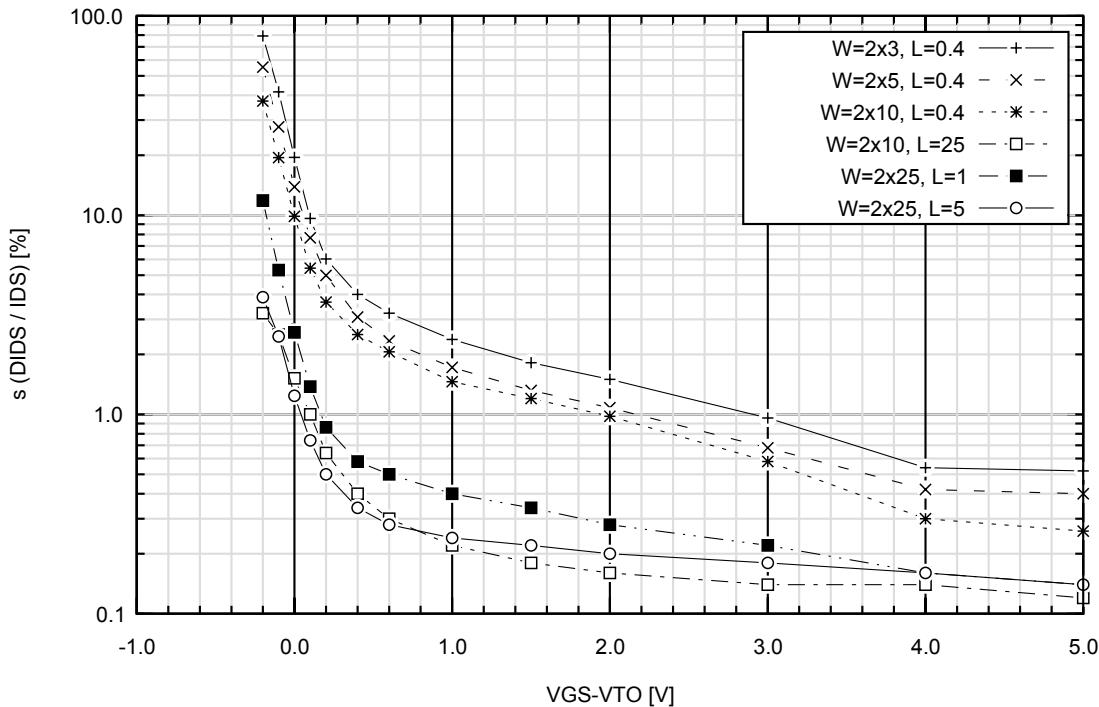
Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMVD	drain-source breakdown @ VG=0V, Id=1µA, L=0.4µm	23	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDPNMVD	pulsed drain current @ VG=5V, VD=8V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	362	-	-	µA/µm
IDSNMVD	saturation current @ VG=5V, VD=8V, L=0.4µm, W=100µm, NF=4, WF=25µm	178	208	238	268	298	µA/µm
KP_NMVDL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	545	-	-	µA/V ²
ROANMVD	area specific on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, Pitch=1.99µm, NF=4, WF=25µm	-	-	11.3	13.1	-	mΩmm ²
RONNMVD	on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	3.8	4.8	5.7	6.6	7.6	kΩµm
TC_VTXNMVD	threshold voltage temperature coefficient	-	-	-1.3	-	-	mV/K
VT1NMVD	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=40µm	-	-	37	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"						
VTXNMVDL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	0.72	-	-	V
VTXNMVDS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	0.67	0.75	0.82	0.89	0.97	V

Matching parameters

Name	Description	Typ	Unit
ABTNMVD	pelgrom coefficient gain factor mismatch	3.44	%µm
AIDNMVD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	40.6	%µm
AIDNMVD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.6	%µm
AIDNMVD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	9.8	%µm
AIDNMVD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8	%µm
AIDNMVD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	6	%µm
AIDNMVD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	3.6	%µm
AIDNMVD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	2.5	%µm
AIDNMVD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1	%µm
AVTNMVD	pelgrom coefficient threshold voltage mismatch	20.78	mVµm
DLTNMVD	transistor delta length	0	µm
DWTNMVD	transistor delta width	0	µm

3. Parameters → 3.31 NMV module → 3.31.2 Device parameters → nmvd → Matching parameters

**Figure 3.62** Device nmvd: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nmve****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-28	-25	5.5	7	V
VDS	-40°C to 175°C	-	-1.5	25	28	V
VDB	-40°C to 175°C	-	-1.5	25	28	V
VD-HW	-40°C to 175°C	-27	-25	400	440	V
If ⁽¹⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽²⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 This forward current is allowed only for transistor's drain bulk junction**Note 2** Pulsed operation with negligible self-heating (<=100ns)**Process parameters**

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMVE	drain-source breakdown @ VG=0V, Id=1µA, L=0.4µm	29	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNMVE	pulsed drain current @ VG=5V, VD=10V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	397	-	-	µA/µm
IDSNMVE	saturation current @ VG=5V, VD=10V, L=0.4µm, W=100µm, NF=4, WF=25µm	180	211	240	269	300	µA/µm

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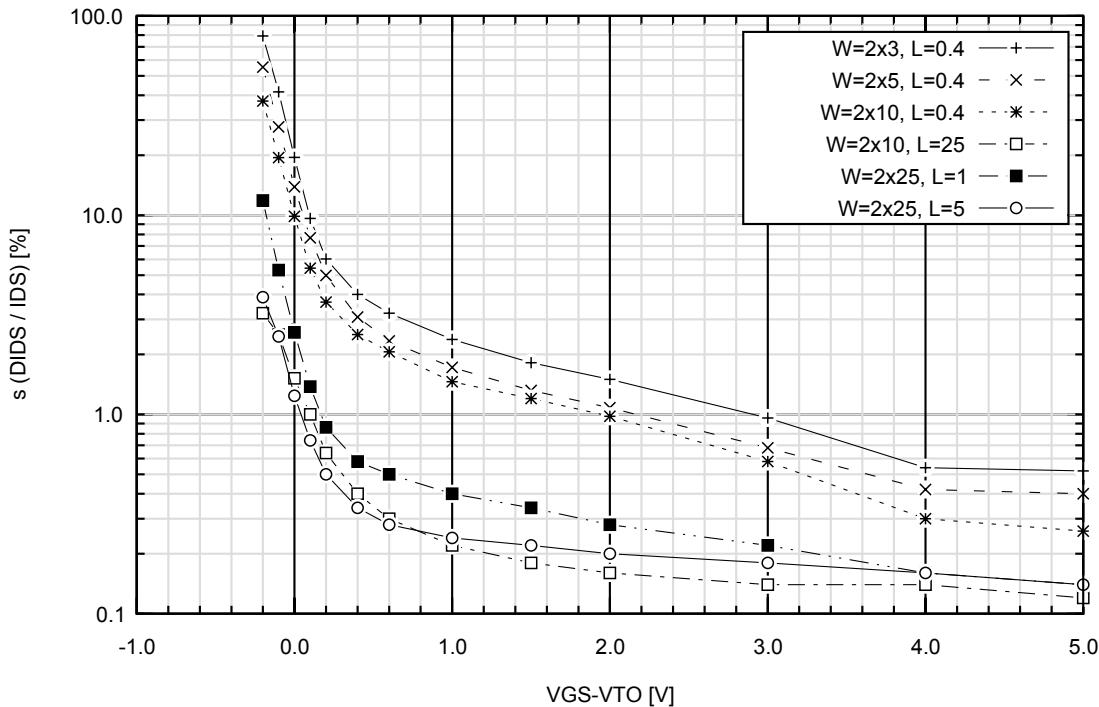
3. Parameters → 3.31 NMV module→ 3.31.2 Device parameters→ nmve→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
KP_NMVEL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	547	-	-	µA/V ²
ROANMVE	area specific on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, Pitch=2.24µm, NF=4, WF=25µm	-	-	13.3	15.5	-	mΩmm ²
RONNMVE	on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	3.9	4.9	5.9	6.9	7.9	kΩµm
TC_VTXNMVE	threshold voltage temperature coefficient	-	-	-1.3	-	-	mV/K
VT1NMVE	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=40µm	-	-	43	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTXNMVEL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	0.72	-	-	V
VTXNMVES	extrapolated threshold voltage short channel @ VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	0.67	0.75	0.82	0.89	0.97	V

Matching parameters

Name	Description	Typ	Unit
ABTNMVD	pelgrom coefficient gain factor mismatch	3.44	%µm
AIDNMVD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	40.6	%µm
AIDNMVD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.6	%µm
AIDNMVD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	9.8	%µm
AIDNMVD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8	%µm
AIDNMVD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	6	%µm
AIDNMVD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	3.6	%µm
AIDNMVD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	2.5	%µm
AIDNMVD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1	%µm
AVTNMVD	pelgrom coefficient threshold voltage mismatch	20.78	mVµm
DLTNMVD	transistor delta length	0	µm
DWTNMVD	transistor delta width	0	µm

3. Parameters → 3.31 NMV module → 3.31.2 Device parameters → nmve → Matching parameters

**Figure 3.63** Device nmvd: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nmvf****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-35	-32	5.5	7	V
VDS	-40°C to 175°C	-	-1.5	32	35	V
VDB	-40°C to 175°C	-	-1.5	32	35	V
VD-HW	-40°C to 175°C	-27	-25	400	440	V
If ⁽¹⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽²⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 This forward current is allowed only for transistor's drain bulk junction**Note 2** Pulsed operation with negligible self-heating (<=100ns)**Process parameters**

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNMVF	drain-source breakdown @ VG=0V, Id=1µA, L=0.4µm	37	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPNMVF	pulsed drain current @ VG=5V, VD=13V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	390	-	-	µA/µm
IDSNMVF	saturation current @ VG=5V, VD=13V, L=0.4µm, W=100µm, NF=4, WF=25µm	164	192	218	244	273	µA/µm

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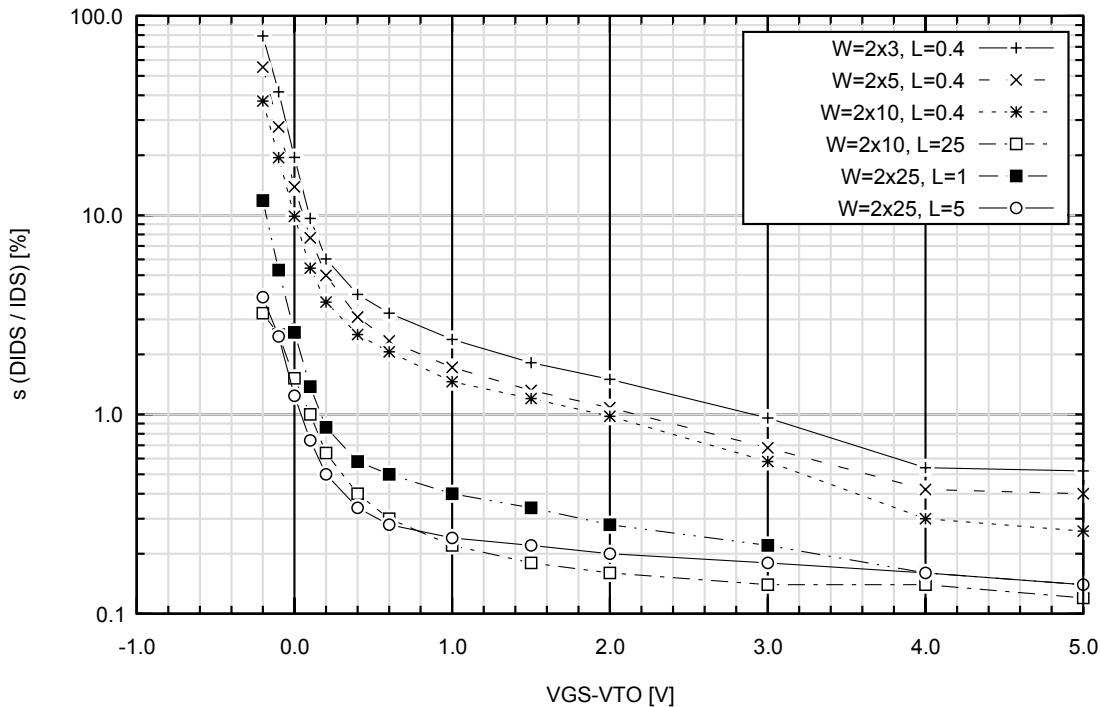
3. Parameters → 3.31 NMV module→ 3.31.2 Device parameters→ nmvf→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
KP_NMVFL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	540	-	-	µA/V ²
ROANMVF	area specific on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, Pitch=2.81µm, NF=4, WF=25µm	-	-	19.9	23	-	mΩmm ²
RONMVF	on resistance @ VG=5V, VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	4.8	6	7.1	8.2	9.4	kΩµm
TC_VTXNMVF	threshold voltage temperature coefficient	-	-	-1.3	-	-	mV/K
VT1NMVF	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=40µm	-	-	52	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 TLP Characteristics " at "my X-FAB"							
VTXNMVFL	extrapolated threshold voltage long channel @ VD=0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	0.72	-	-	V
VTXNMVFS	extrapolated threshold voltage short channel @ VD=0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	0.67	0.75	0.82	0.89	0.97	V

Matching parameters

Name	Description	Typ	Unit
ABTNMVD	pelgrom coefficient gain factor mismatch	3.44	%µm
AIDNMVD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	40.6	%µm
AIDNMVD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	14.6	%µm
AIDNMVD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	9.8	%µm
AIDNMVD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8	%µm
AIDNMVD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	6	%µm
AIDNMVD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	3.6	%µm
AIDNMVD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	2.5	%µm
AIDNMVD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1	%µm
AVTNMVD	pelgrom coefficient threshold voltage mismatch	20.78	mVµm
DLTNMVD	transistor delta length	0	µm
DWTNMVD	transistor delta width	0	µm

3. Parameters → 3.31 NMV module→ 3.31.2 Device parameters→ nmvf→ Matching parameters

**Figure 3.64** Device nmvd: drain current matching vs. VGS-VTO (typical values, drawn W and L)**dfwdnb****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-13	-12	1.5	-	V
Vcathode-HW	-40°C to 175°C	-27	-25	400	440	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽¹⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDNB	breakdown voltage @ Irev=1μA, L=4μm, W=25μm	13.8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DFWDNB	leakage current @ VL=12V, T=27°C, W=200μm, NF=2, WF=100μm	-	-	200	-	-	pA
IL_DFWDNBHT	leakage current @ VL=12V, T=175°C, W=200μm, NF=2, WF=100μm	-	-	13	-	-	nA
TC_VDFDFWDNB	forward voltage temperature coefficient	-	-	-1.4	-	-	mV/K ²
VDFDFWDNB	diode forward voltage @ Idio=100μA, L=1μm, W=100μm, NF=4, WF=25μm	0.76	0.78	0.8	0.82	0.84	V

3. Parameters → 3.31 NMV module→ 3.31.2 Device parameters→ dfwdnc→ Operating conditions

dfwdnc

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-16.5	-15	1.5	-	V
Vcathode-HW	-40°C to 175°C	-27	-25	400	440	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽¹⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDNC	breakdown voltage @ Irev=1μA, L=4μm, W=25μm	17.3	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DFWDNC	leakage current @ VL=15V, T=27°C, W=200μm, NF=2, WF=100μm	-	-	40	-	-	pA
IL_DFWDNCHT	leakage current @ VL=15V, T=175°C, W=200μm, NF=2, WF=100μm	-	-	7.6	-	-	nA
TC_VDFDFWDNC	forward voltage temperature coefficient	-	-	-1.4	-	-	mV/K ²
VDFDFWDNC	diode forward voltage @ Idio=100μA, L=1μm, W=100μm, NF=4, WF=25μm	0.76	0.78	0.8	0.82	0.84	V

dfwdnd

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-22	-20	1.5	-	V
Vcathode-HW	-40°C to 175°C	-27	-25	400	440	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽¹⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DFWDND	breakdown voltage @ Irev=1μA, L=4μm, W=25μm	23	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DFWDND	leakage current @ VL=20V, T=27°C, W=200μm, NF=2, WF=100μm	-	-	26	-	-	pA
IL_DFWDNHT	leakage current @ VL=20V, T=175°C, W=200μm, NF=2, WF=100μm	-	-	7.5	-	-	nA
TC_VDFDFWDND	forward voltage temperature coefficient	-	-	-1.4	-	-	mV/K ²
VDFDFWDND	diode forward voltage @ Idio=100μA, L=1μm, W=100μm, NF=4, WF=25μm	0.76	0.78	0.8	0.82	0.84	V

3. Parameters → 3.32 PHVA module

3.32 PHVA module

3.32.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_PDF	PDF junction depth	1.3	µm

3.32.2 Device parameters

phvta

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	40	42	V
VDS	-40°C to 175°C	-42	-40	1.5	-	V
VDB	-40°C to 175°C	-42	-40	1.5	-	V
VB-HW	-40°C to 175°C	-17	-15	200	220	V

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHVTA	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	45	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPHVTA	pulsed saturation current @ VG=-5V, VD=-10V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=100µm, NF=4, WF=25µm	-	-	178	-	-	µA/µm
IDSAPHVTA	saturation current @ VG=-5V, VD=-10V, Vhw=-10V, VPTUB=-10V, L=0.5µm, W=100µm, NF=4, WF=25µm	116	124	131	139	146	µA/µm
KP_PHVTAL	gain factor long channel @ L=1.5µm, W=100µm, NF=4, WF=25µm	-	-	1580	-	-	µA/V ²
ROAPHVTA	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, Pitch=3.59µm, NF=4, WF=25µm	-	-	100.5	107	-	mΩmm ²
RO_PHVTA	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	24.4	26.2	28	29.8	31.6	kΩµm
TC_VTXPHVTA	threshold voltage temperature coefficient	-	-	1.6	-	-	mV/K
VTIPHVTA	threshold voltage @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-	-1.09	-1.03	-0.97	-	V
VTXPHVTA	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-1.05	-0.99	-0.93	-0.87	-0.81	V

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3. Parameters → 3.32 PHVA module→ 3.32.2 Device parameters→ phvta→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VTXPHVTAL	extrapolated threshold voltage long channel @ VD=-0.1V, L=1.5μm, W=100μm, NF=4, WF=25μm	-	-	-0.92	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTPHVTA	pelgrom coefficient gain factor mismatch	1.48	%μm
AIDPHVTA00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	20.23	%μm
AIDPHVTA02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	9.51	%μm
AIDPHVTA04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	5.41	%μm
AIDPHVTA06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	3.65	%μm
AIDPHVTA10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.19	%μm
AIDPHVTA20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.12	%μm
AIDPHVTA30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.56	%μm
AIDPHVTA50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.44	%μm
AVTPHVTA	pelgrom coefficient threshold voltage mismatch	11.29	mVμm
DLTPHVTA	transistor delta length	0	μm
DWTPHVTA	transistor delta width	0	μm

Note: Transistors with channel lengths > 0.5μm will exhibit greater mismatch of parameters. More information available on request.

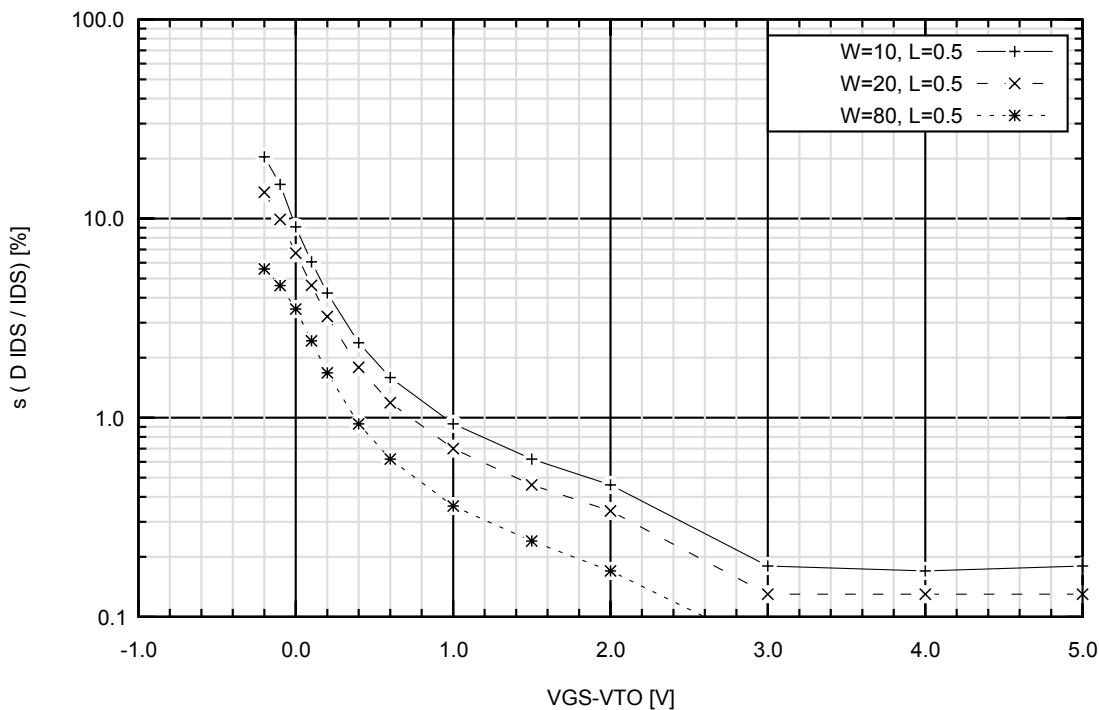


Figure 3.65 Device phvta: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phvtb

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V

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3. Parameters → 3.32 PHVA module→ 3.32.2 Device parameters→ phvtb→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGD	-40°C to 175°C	-7	-5.5	40	42	V
VDS	-40°C to 175°C	-42	-40	1.5	-	V
VDB	-40°C to 175°C	-42	-40	1.5	-	V
VB-HW	-40°C to 175°C	-22	-20	200	220	V

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHVTB	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	55	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPHVTB	pulsed saturation current @ VG=-5V, VD=-10V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=100µm, NF=4, WF=25µm	-	-	160	-	-	µA/µm
IDS _{PHVTB}	saturation current @ VG=-5V, VD=-10V, Vhw=-10V, VPTUB=-10V, L=0.5µm, W=100µm, NF=4, WF=25µm	108	114	120	126	132	µA/µm
KP _{PHVTBL}	gain factor long channel @ L=10µm, W=100µm, NF=4, WF=25µm	-	-	275	-	-	µA/V ²
ROA _{PHVTB}	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, Pitch=4.49µm, NF=4, WF=25µm	-	-	155	165	-	mΩmm ²
RO _{PHVTB}	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	30.3	32.4	34.5	36.6	38.7	kΩµm
TC _{VTXPHVTB}	threshold voltage temperature coefficient	-	-	1.5	-	-	mV/K
VTI _{PHVTB}	threshold voltage @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-	-1.1	-1.04	-0.98	-	V
VTX _{PHVTB}	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-1.05	-0.99	-0.93	-0.87	-0.81	V
VTX _{PHVTBL}	extrapolated threshold voltage long channel @ VD=-0.1V, L=10µm, W=100µm, NF=4, WF=25µm	-	-	-0.87	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTPHVTB	pelgrom coefficient gain factor mismatch @ L=0.5µm	2.04	%µm
AIDPHVTB00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V, L=0.5µm	23.4	%µm
AIDPHVTB02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V, L=0.5µm	11.2	%µm
AIDPHVTB04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V, L=0.5µm	6.2	%µm
AIDPHVTB06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V, L=0.5µm	4.2	%µm

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3. Parameters → 3.32 PHVA module→ 3.32.2 Device parameters→ phvtb→ Matching parameters

Name	Description	Typ	Unit
AIDPHVTB10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V, L=0.5μm	2.5	%μm
AIDPHVTB20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V, L=0.5μm	1.2	%μm
AIDPHVTB30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V, L=0.5μm	0.5	%μm
AIDPHVTB50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V, L=0.5μm	0.5	%μm
AVTPHVTB	pelgrom coefficient threshold voltage mismatch @ L=0.5μm	12.3	mVμm
DLTPHVTB	transistor delta length	0	μm
DWTPHVTB	transistor delta width	0	μm

Note: Transistors with channel lengths > 0.5μm will exhibit greater mismatch of parameters. More information available on request.

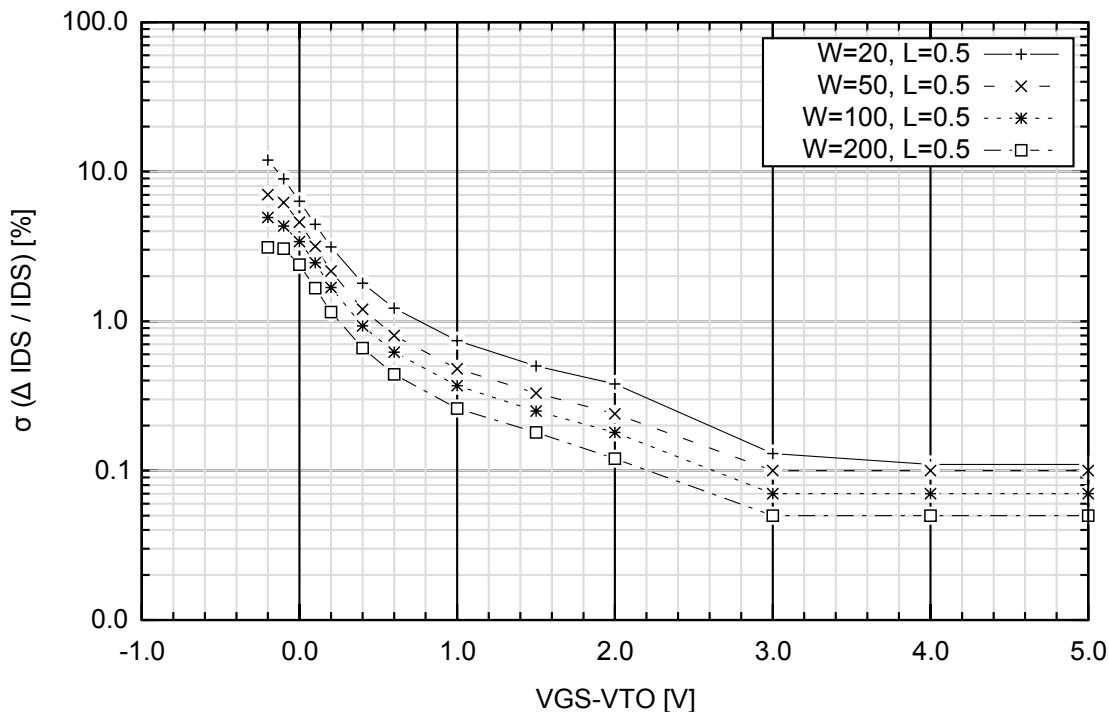


Figure 3.66 Device phvtb: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phvu**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	60	62	V
VDS	-40°C to 175°C	-62	-60	1.5	-	V
VDB	-40°C to 175°C	-62	-60	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	200	220	V

Note: The node B (BULK) is: NWELL2

3. Parameters → 3.32 PHVA module→ 3.32.2 Device parameters→ phvu→ Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHVU	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	65	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDPPHVU	pulsed saturation current @ VG=-5V, VD=-10V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=100µm, NF=4, WF=25µm	-	-	137	-	-	µA/µm
IDS PHVU	saturation current @ VG=-5V, VD=-10V, Vhw=-10V, VPTUB=-10V, L=0.5µm, W=100µm, NF=4, WF=25µm	97	102	107	112	117	µA/µm
KP_PHVUL	gain factor long channel @ L=10µm, W=100µm, NF=4, WF=25µm	-	-	272	-	-	µA/V ²
ROAPHVU	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, Pitch=5.84µm, NF=4, WF=25µm	-	-	257	269	-	mΩmm ²
RO_PHVU	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	40	42	44	46	48	kΩµm
TC_VTXPHVU	threshold voltage temperature coefficient	-	-	1.5	-	-	mV/K
VTIPHVU	threshold voltage @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-	-1.11	-1.05	-0.99	-	V
VTXPHVU	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-1.05	-0.99	-0.93	-0.87	-0.81	V
VTXPHVUL	extrapolated threshold voltage @ VD=-0.1V, L=10µm, W=100µm, NF=4, WF=25µm	-	-	-0.87	-	-	V

Matching parameters

Name	Description	Typ	Unit
ABTPHVU	pelgrom coefficient gain factor mismatch	1.62	%µm
AIDPHVU00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	21.08	%µm
AIDPHVU02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	9.53	%µm
AIDPHVU04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	5.3	%µm
AIDPHVU06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	3.55	%µm
AIDPHVU10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.12	%µm
AIDPHVU20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.98	%µm
AIDPHVU30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.5	%µm
AIDPHVU50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.39	%µm
AVTPHVU	pelgrom coefficient threshold voltage mismatch	10.7	mVµm
DLTPHVU	transistor delta length	0	µm
DWTPHVU	transistor delta width	0	µm

Note: Transistors with channel lengths > 0.5µm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.32 PHVA module→ 3.32.2 Device parameters→ phvu→ Matching parameters

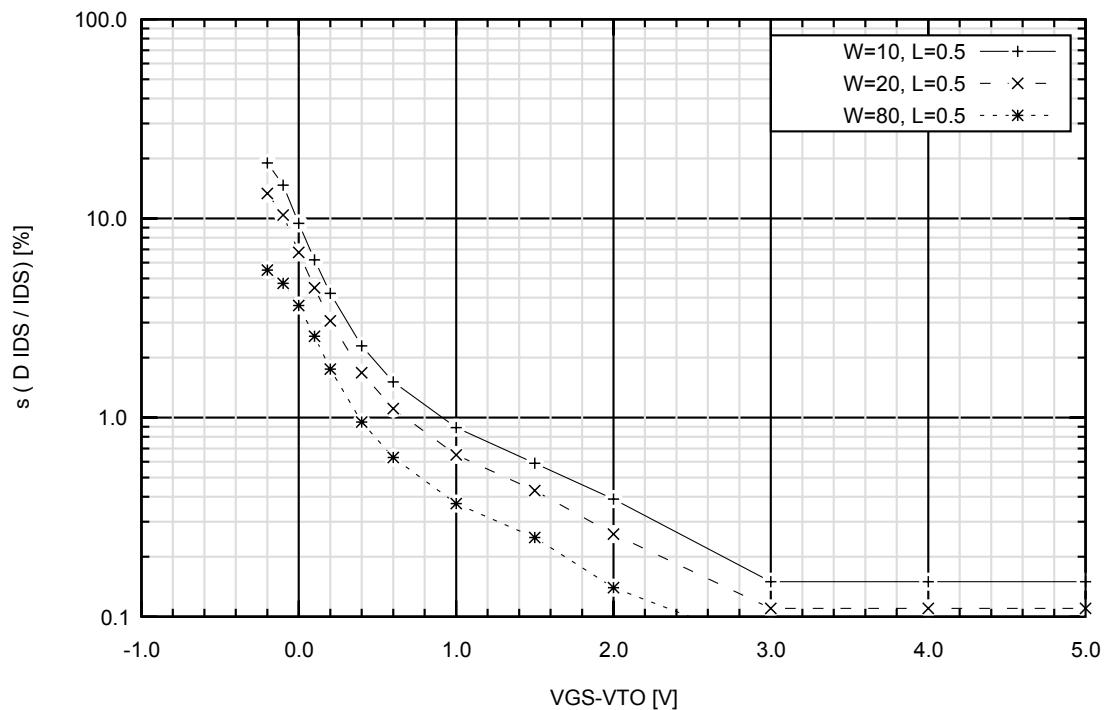


Figure 3.67 Device phvu: drain current matching vs. VGS-VTO (typical values, drawn W and L)

3. Parameters → 3.33 PHVR module

3.33 PHVR module

3.33.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_DFN	HVMOS N-drift junction depth	3.5	µm
	Note: DFN layers reaches BOX when drawn in ACTIVE		
XJ_DFP	HVMOS P-drift junction depth	1.8	µm

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSDFN	DFN sheet resistance in PDD (DTI terminated) @ W=5µm	3.9	kΩ/□
RSSDFPN	DFP(n) sheet resistance (DTI terminated) @ W=5µm	3.3	kΩ/□
RSSDFPP	DFP(p) sheet resistance (DTI terminated) @ W=5µm	6.9	kΩ/□

3.33.2 Device parameters

phvra

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	40	44	V
VDS ⁽¹⁾	-40°C to 175°C	-44	-40	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-44	-40	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	125	127	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHVRA	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	46	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IDPPHVRA	pulsed drain current @ VG=-5V, VD=-20V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	155	-	-	µA/µm
IDS_PHVRA	saturation current @ VG=-5V, VD=-20V, L=0.5µm, W=100µm, NF=4, WF=25µm	98	108	118	128	138	µA/µm
KP_PHVRAL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	145	-	-	µA/V ²

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3. Parameters → 3.33 PHVR module → 3.33.2 Device parameters → phvra → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHVRA	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=100μm, Pitch=3.3μm, NF=4, WF=25μm	-	-	90	102	-	mΩmm ²
RON PHVRA	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	20.3	23.8	27.3	30.8	34.3	kΩμm
TC _VTXPHVRA	threshold voltage temperature coefficient	-	-	1.6	-	-	mV/K
VTX PHVRAL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10μm, W=50μm, NF=2, WF=25μm	-	-	-0.95	-	-	V
VTX PHVRAS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	-1.19	-1.11	-1.03	-0.95	-0.87	V

phvrb

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	60	66	V
VDS ⁽¹⁾	-40°C to 175°C	-66	-60	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-66	-60	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	125	127	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS PHVRB	drain-source breakdown @ VG=0V, Id=-1μA, L=0.5μm	69	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDP PHVRB	pulsed drain current @ VG=-5V, VD=-20V, Dcyc=1%, Pwid=100ns, NF=4, WF=25μm	-	-	160	-	-	μA/μm
IDS PHVRB	saturation current @ VG=-5V, VD=-20V, L=0.5μm, W=100μm, NF=4, WF=25μm	94	104	114	124	134	μA/μm
KP _PHVRBL	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	145	-	-	μA/V ²
ROA PHVRB	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=100μm, Pitch=4.7μm, NF=4, WF=25μm	-	-	170	191	-	mΩmm ²

3. Parameters → 3.33 PHVR module→ 3.33.2 Device parameters→ phvrb→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RONPHVRB	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	27.2	31.7	36.2	40.7	45.2	kΩμm
TC_VTXPHVRB	threshold voltage temperature coefficient	-	-	1.7	-	-	mV/K
VTXPHVRBL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10μm, W=50μm, NF=2, WF=25μm	-	-	-0.96	-	-	V
VTXPHVRBS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	-1.2	-1.12	-1.04	-0.96	-0.88	V

phvrc

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	70	77	V
VDS ⁽¹⁾	-40°C to 175°C	-77	-70	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-77	-70	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	125	127	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHVRC	drain-source breakdown @ VG=0V, Id=-1μA, L=0.5μm	81	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPHVRC	pulsed drain current @ VG=-5V, VD=-20V, Dcyc=1%, Pwid=100ns, NF=4, WF=25μm	-	-	150	-	-	μA/μm
IDS_PHVRC	saturation current @ VG=-5V, VD=-20V, L=0.5μm, W=100μm, NF=4, WF=25μm	96	105	114	123	132	μA/μm
KP_PHVRCL	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	145	-	-	μA/V ²
ROAPHVRC	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=100μm, Pitch=5.3μm, NF=4, WF=25μm	-	-	210	236	-	mΩmm ²
RONPHVRC	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=100μm, NF=4, WF=25μm	29.8	34.7	39.6	44.5	49.4	kΩμm
TC_VTXPHVRC	threshold voltage temperature coefficient	-	-	1.7	-	-	mV/K

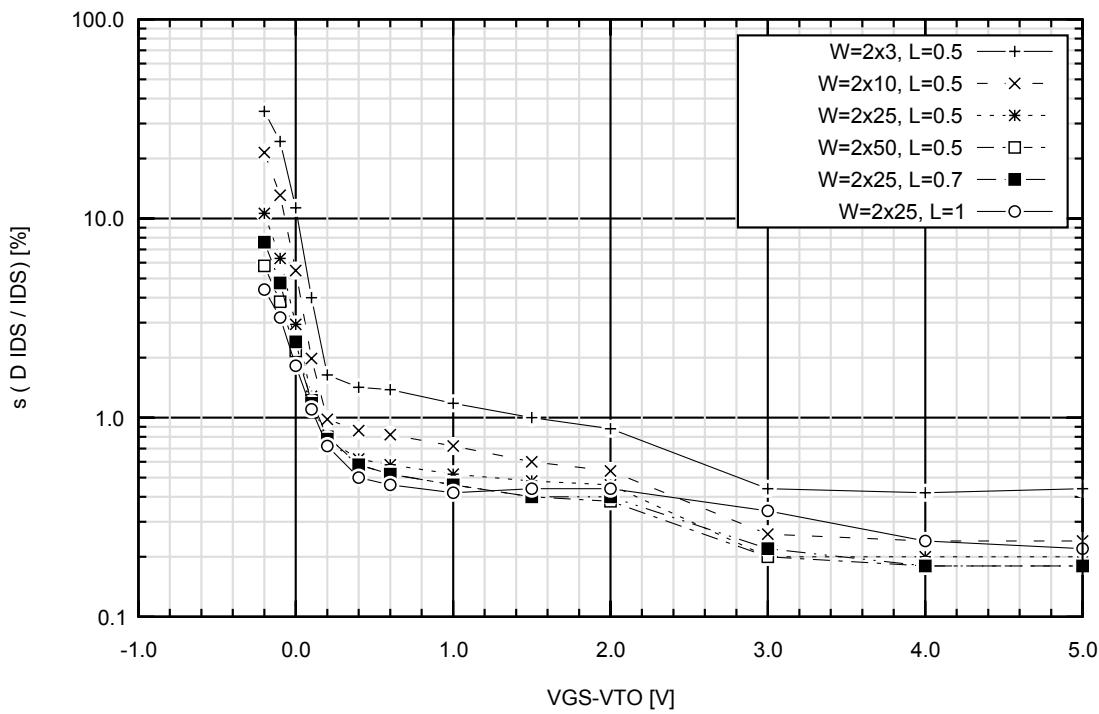
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3. Parameters → 3.33 PHVR module→ 3.33.2 Device parameters→ phvrc→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VTXPHVRCL	extrapolated threshold voltage long channel @ $V_D=-0.1V$, $L=10\mu m$, $W=50\mu m$, $NF=2$, $WF=25\mu m$	-	-	-0.96	-	-	V
VTXPHVRCS	extrapolated threshold voltage short channel @ $V_D=-0.1V$, $L=0.5\mu m$, $W=100\mu m$, $NF=4$, $WF=25\mu m$	-1.21	-1.13	-1.05	-0.97	-0.89	V

Matching parameters

Name	Description	Typ	Unit
ABTPHVRC	pelgrom coefficient gain factor mismatch	1.48	% μm
AIDPHVRC00	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=0V$	17.52	% μm
AIDPHVRC02	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=0.2V$	3.28	% μm
AIDPHVRC04	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=0.4V$	2.84	% μm
AIDPHVRC06	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=0.6V$	2.68	% μm
AIDPHVRC10	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=1V$	2.3	% μm
AIDPHVRC20	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=2V$	1.76	% μm
AIDPHVRC30	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=3V$	0.9	% μm
AIDPHVRC50	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=5V$	0.84	% μm
AVTPHVRC	pelgrom coefficient threshold voltage mismatch	10.89	mV μm
DLTPHVRC	transistor delta length	0	μm
DWTPHVRC	transistor delta width	0	μm

**Figure 3.68** Device phvrc: drain current matching vs. VGS-VTO (typical values, drawn W and L)**phvrd**

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

3. Parameters → 3.33 PHVR module → 3.33.2 Device parameters → phvrd → Operating conditions

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	85	87	V
VDS ⁽¹⁾	-40°C to 175°C	-87	-85	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-87	-85	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	125	127	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

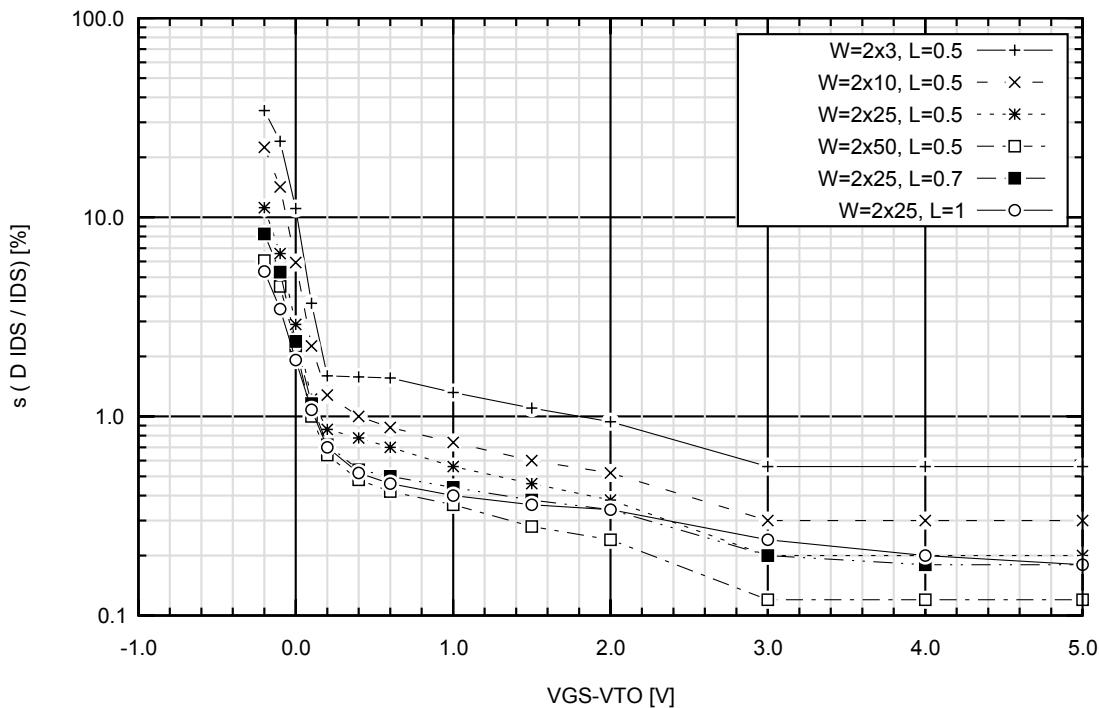
Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHVRD	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	92	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPHVRD	pulsed drain current @ VG=-5V, VD=-20V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	155	-	-	µA/µm
IDSPhVRD	saturation current @ VG=-5V, VD=-20V, L=0.5µm, W=100µm, NF=4, WF=25µm	93	102	111	120	129	µA/µm
KP_PHVRDL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	145	-	-	µA/V ²
ROAPHVRD	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, Pitch=6.1µm, NF=4, WF=25µm	-	-	270	304	-	mΩmm ²
RONPHVRD	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	33.1	38.7	44.3	49.9	55.5	kΩµm
TC_VTXPHVRD	threshold voltage temperature coefficient	-	-	1.7	-	-	mV/K
VTXPHVRDL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	-0.97	-	-	V
VTXPHVRDS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-1.21	-1.13	-1.05	-0.97	-0.89	V

Matching parameters

Name	Description	Typ	Unit
ABTPHVRD	pelgrom coefficient gain factor mismatch	1.66	%µm
AIDPHVRD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	18.62	%µm
AIDPHVRD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	3.48	%µm
AIDPHVRD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	3.06	%µm
AIDPHVRD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	2.86	%µm
AIDPHVRD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.4	%µm
AIDPHVRD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.72	%µm
AIDPHVRD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.04	%µm

3. Parameters → 3.33 PHVR module → 3.33.2 Device parameters → phvrd → Matching parameters

Name	Description	Typ	Unit
AIDPHVRD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1.02	% μ m
AVTPHVRD	pelgrom coefficient threshold voltage mismatch	11.04	mV μ m
DLTPHVRD	transistor delta length	0	μ m
DWTPHVRD	transistor delta width	0	μ m

**Figure 3.69** Device phvrd: drain current matching vs. VGS-VTO (typical values, drawn W and L)**phvre**

The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	100	102	V
VDS ⁽¹⁾	-40°C to 175°C	-102	-100	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-102	-100	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	125	127	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

3. Parameters → 3.33 PHVR module→ 3.33.2 Device parameters→ phvre→ Process parameters

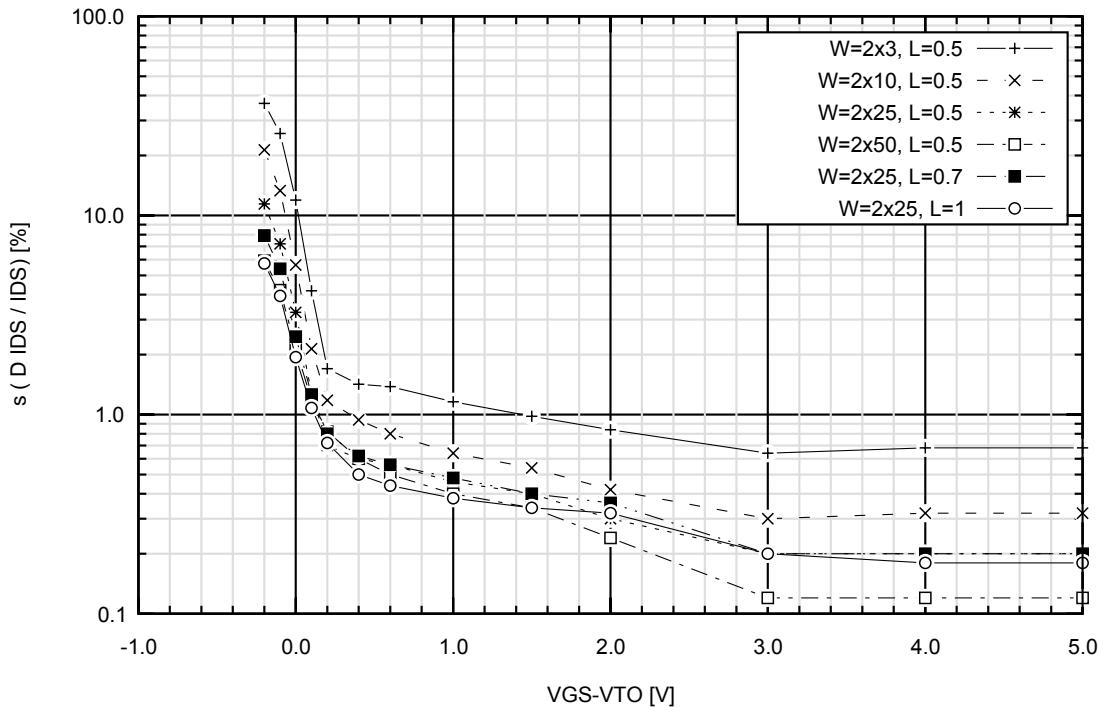
Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHVRE	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	110	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPHVRE	pulsed drain current @ VG=-5V, VD=-20V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	135	-	-	µA/µm
IDS PHVRE	saturation current @ VG=-5V, VD=-20V, L=0.5µm, W=100µm, NF=4, WF=25µm	88	96	104	112	120	µA/µm
KP_PHVREL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	143	-	-	µA/V ²
ROAPHVRE	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, Pitch=7.2µm, NF=4, WF=25µm	-	-	380	428	-	mΩmm ²
RONPHVRE	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	39.6	46.2	52.8	59.4	66	kΩµm
TC_VTXPHVRE	threshold voltage temperature coefficient	-	-	1.7	-	-	mV/K
VTXPHVREL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	-0.96	-	-	V
VTXPHVRES	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-1.2	-1.12	-1.04	-0.96	-0.88	V

Matching parameters

Name	Description	Typ	Unit
ABTPHVRE	pelgrom coefficient gain factor mismatch	1.54	%µm
AIDPHVRE00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	19.38	%µm
AIDPHVRE02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	3.52	%µm
AIDPHVRE04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	2.94	%µm
AIDPHVRE06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	2.74	%µm
AIDPHVRE10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.28	%µm
AIDPHVRE20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.58	%µm
AIDPHVRE30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.12	%µm
AIDPHVRE50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1.14	%µm
AVTPHVRE	pelgrom coefficient threshold voltage mismatch	11.1	mVµm
DLTPHVRE	transistor delta length	0	µm
DWTPHVRE	transistor delta width	0	µm

3. Parameters → 3.33 PHVR module → 3.33.2 Device parameters → phvre → Matching parameters

**Figure 3.70** Device phvre: drain current matching vs. VGS-VTO (typical values, drawn W and L)**phvrf**

This device is intended to enhance the ESD design window for 100V applications. The ESD design window may not be suitable for applications up to 125V.

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	125	127	V
VDS ⁽¹⁾	-40°C to 175°C	-127	-125	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-127	-125	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	125	127	V
VD-HW	-40°C to 175°C	-27	-25	125	127	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHVRF	drain-source breakdown @ VG=0V, Id=-1µA, L=0.5µm	132	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPHVRF	pulsed drain current @ VG=-5V, VD=-20V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	105	-	-	µA/µm
IDS PHVRF	saturation current @ VG=-5V, VD=-20V, L=0.5µm, W=100µm, NF=4, WF=25µm	76	83	90	97	104	µA/µm

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3. Parameters → 3.33 PHVR module→ 3.33.2 Device parameters→ phvrf→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
KP_PHVRF	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	139	-	-	µA/V ²
ROA _{PHVRF}	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, Pitch=10.2µm, NF=4, WF=25µm	-	-	725	816	-	mΩmm ²
RON _{PHVRF}	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	53.3	62.2	71.1	80	88.9	kΩµm
TC_VTXPHVRF	threshold voltage temperature coefficient	-	-	1.7	-	-	mV/K
VTX _{PHVRF}	extrapolated threshold voltage long channel @ VD=-0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	-0.95	-	-	V
VTX _{PHVRFS}	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.5µm, W=100µm, NF=4, WF=25µm	-1.19	-1.11	-1.03	-0.95	-0.87	V

3. Parameters → 3.34 PMV module

3.34 PMV module

3.34.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_PDFMV	Medium voltage P-drift junction depth	1.2	μm

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSPMVN	PDFMV(n) sheet resistance (DTI terminated) @ W=5μm	6.7	kΩ/□
RSSPMVP	PDFMV(p) sheet resistance (DTI terminated) @ W=5μm	8.2	kΩ/□

3.34.2 Device parameters

pmvb

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	12	13	V
VDS ⁽¹⁾	-40°C to 175°C	-13	-12	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-13	-12	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	400	440	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMVB	drain-source breakdown @ VG=0V, Id=-1μA, L=0.4μm	13.8	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPMVB	pulsed drain current @ VG=-5V, VD=-6V, Dcyc=1%, Pwid=100ns, NF=4, WF=25μm	-	-	260	-	-	μA/μm
IDSpmVB	saturation current @ VG=-5V, VD=-6V, L=0.4μm, W=100μm, NF=4, WF=25μm	149	167	185	203	221	μA/μm
KP_PMVBL	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	143	-	-	μA/V ²
ROAPMVB	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.4μm, W=100μm, Pitch=1.87μm, NF=4, WF=25μm	-	-	21.9	24.9	-	mΩmm ²
RONPMVB	on resistance @ VG=-5V, VD=-0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	8.5	10.1	11.7	13.3	14.9	kΩμm
TC_VTXPMVB	threshold voltage temperature coefficient	-	-	1.4	-	-	mV/K

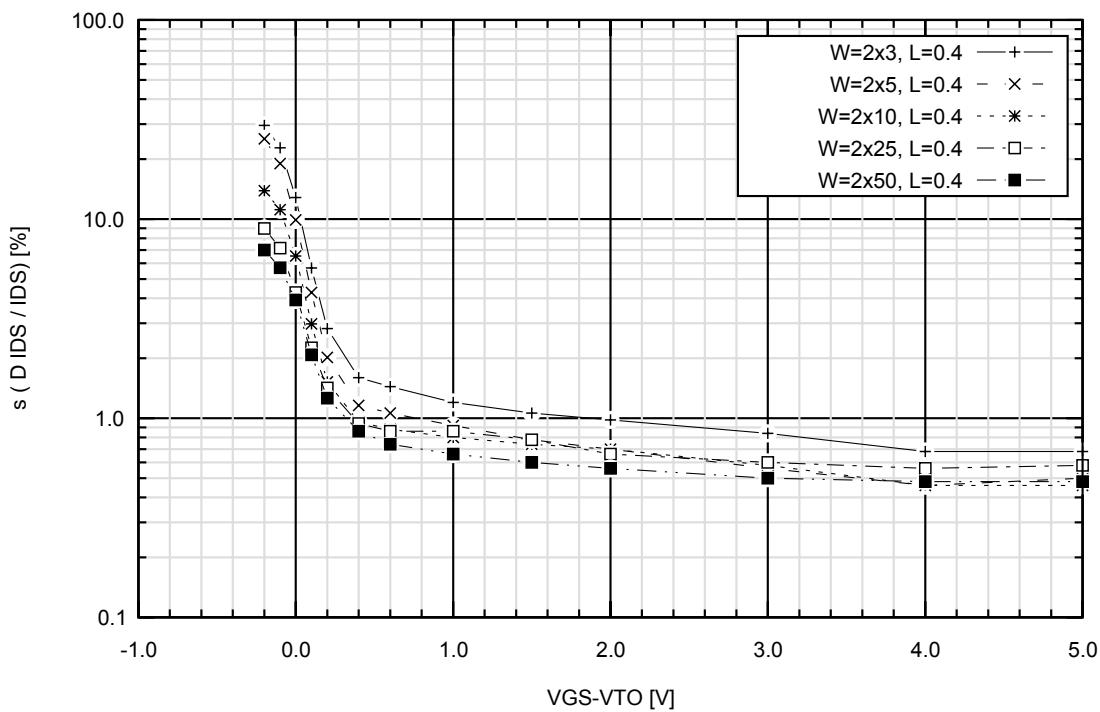
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3. Parameters → 3.34 PMV module→ 3.34.2 Device parameters→ pmvb→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VTXPMVBL	extrapolated threshold voltage long channel @ $V_D=-0.1V$, $L=10\mu m$, $W=50\mu m$, $NF=2$, $WF=25\mu m$	-	-	-0.83	-	-	V
VTXPMVBS	extrapolated threshold voltage short channel @ $V_D=-0.1V$, $L=0.4\mu m$, $W=100\mu m$, $NF=4$, $WF=25\mu m$	-1.02	-0.92	-0.82	-0.72	-0.62	V

Matching parameters

Name	Description	Typ	Unit
ABTPMV	pelgrom coefficient gain factor mismatch	1.41	% μm
AIDPMVB00	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=0V$	19.96	% μm
AIDPMVB02	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=0.2V$	4.62	% μm
AIDPMVB04	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=0.4V$	2.76	% μm
AIDPMVB06	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=0.6V$	2.5	% μm
AIDPMVB10	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=1V$	2.18	% μm
AIDPMVB20	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=2V$	1.78	% μm
AIDPMVB30	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=3V$	1.52	% μm
AIDPMVB50	pelgrom coefficient drain current mismatch @ $V_{DS}=5V$, $VG-VT=5V$	1.32	% μm
AVTPMVB	pelgrom coefficient threshold voltage mismatch	11.62	mV μm
DLTPMVB	transistor delta length	0	μm
DWTPMVB	transistor delta width	0	μm

**Figure 3.71** Device pmvb drain current matching vs. V_{GS-VTO} (typical values, drawn W and L)

3. Parameters → 3.34 PMV module→ 3.34.2 Device parameters→ pmvd→ Operating conditions

pmvd

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	18	20	V
VDS ⁽¹⁾	-40°C to 175°C	-20	-18	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-20	-18	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	400	440	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMVD	drain-source breakdown @ VG=0V, Id=-1µA, L=0.4µm	21	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPMVD	pulsed drain current @ VG=-5V, VD=-8V, Dcyc=1%, Pwid=100ns, NF=4, WF=25µm	-	-	240	-	-	µA/µm
IDSpmvd	saturation current @ VG=-5V, VD=-8V, L=0.4µm, W=100µm, NF=4, WF=25µm	136	153	170	187	204	µA/µm
KP_PMVDL	gain factor long channel @ L=10µm, W=50µm, NF=2, WF=25µm	-	-	142	-	-	µA/V ²
ROAPMVD	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.4µm, W=100µm, Pitch=1.94µm, NF=4, WF=25µm	-	-	27.9	31.8	-	mΩmm ²
RONPMVD	on resistance @ VG=-5V, VD=-0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	10.5	12.5	14.4	16.4	18.3	kΩµm
TC_VTXPMVD	threshold voltage temperature coefficient	-	-	1.4	-	-	mV/K
VTXPMVDL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10µm, W=50µm, NF=2, WF=25µm	-	-	-0.83	-	-	V
VTXPMVDS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.4µm, W=100µm, NF=4, WF=25µm	-1.02	-0.92	-0.82	-0.72	-0.62	V

Matching parameters

Name	Description	Typ	Unit
ABTPMVD	pelgrom coefficient gain factor mismatch	1.54	%µm
AIDPMVD00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	20.72	%µm
AIDPMVD02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	4.74	%µm
AIDPMVD04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	2.8	%µm
AIDPMVD06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	2.48	%µm
AIDPMVD10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.04	%µm
AIDPMVD20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.46	%µm
AIDPMVD30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	1.06	%µm

3. Parameters → 3.34 PMV module → 3.34.2 Device parameters → pmvd → Matching parameters

Name	Description	Typ	Unit
AIDPMVD50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	1.32	% μ m
AVTPMVD	pelgrom coefficient threshold voltage mismatch	12.87	mV μ m
DLTPMVD	transistor delta length	0	μ m
DWTPMVD	transistor delta width	0	μ m

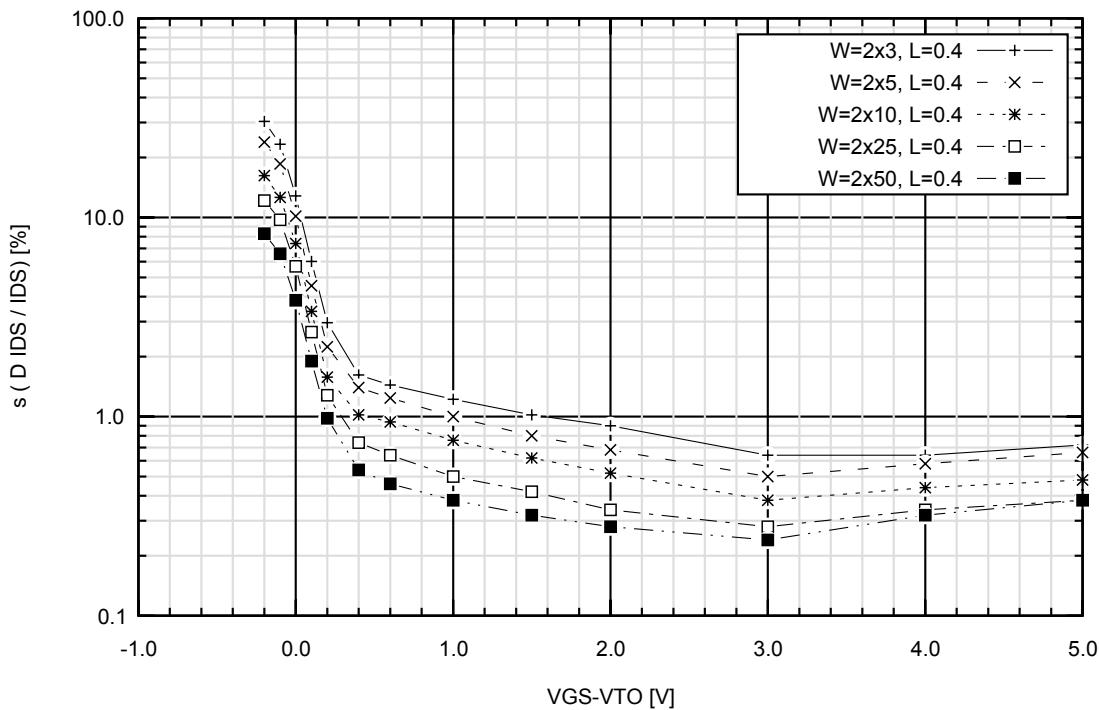


Figure 3.72 Device pmvd: drain current matching vs. VGS-VTO (typical values, drawn W and L)

pmve

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	25	28	V
VDS ⁽¹⁾	-40°C to 175°C	-28	-25	1.5	-	V
VDB ⁽¹⁾	-40°C to 175°C	-28	-25	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	400	440	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPMVE	drain-source breakdown @ VG=0V, Id=-1 μ A, L=0.4 μ m	29	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPMVE	pulsed drain current @ VG=-5V, VD=-10V, Dcyc=1%, Pwid=100ns, NF=4, WF=25 μ m	-	-	220	-	-	μ A/ μ m

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3. Parameters → 3.34 PMV module→ 3.34.2 Device parameters→ pmve→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IDS_{PMVE}	saturation current @ VG=-5V, VD=-10V, L=0.4μm, W=100μm, NF=4, WF=25μm	128	144	160	176	192	μA/μm
KP_{PMVEL}	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	141	-	-	μA/V ²
ROA_{PMVE}	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.4μm, W=100μm, Pitch=2.24μm, NF=4, WF=25μm	-	-	36.7	41.9	-	mΩmm ²
RON_{PMVE}	on resistance @ VG=-5V, VD=-0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	11.8	14.1	16.4	18.7	21	kΩμm
TC_{VTXPMVE}	threshold voltage temperature coefficient	-	-	1.4	-	-	mV/K
VTX_{PMVEL}	extrapolated threshold voltage long channel @ VD=-0.1V, L=10μm, W=50μm, NF=2, WF=25μm	-	-	-0.83	-	-	V
VTX_{PMVES}	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	-1.03	-0.93	-0.83	-0.73	-0.63	V

pmvf**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	32	35	V
VDS⁽¹⁾	-40°C to 175°C	-35	-32	1.5	-	V
VDB⁽¹⁾	-40°C to 175°C	-35	-32	1.5	-	V
VB-HW	-40°C to 175°C	-27	-25	400	440	V

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note: The node B (BULK) is: NWELL2

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS_{PMVF}	drain-source breakdown @ VG=0V, Id=-1μA, L=0.4μm	37	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IDPPMVF	pulsed drain current @ VG=-5V, VD=-15V, Dcyc=1%, Pwid=100ns, NF=4, WF=25μm	-	-	220	-	-	μA/μm
IDS_{PMVF}	saturation current @ VG=-5V, VD=-15V, L=0.4μm, W=100μm, NF=4, WF=25μm	118	132	146	160	174	μA/μm
KP_{PMVFL}	gain factor long channel @ L=10μm, W=50μm, NF=2, WF=25μm	-	-	141	-	-	μA/V ²
ROA_{PMVF}	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.4μm, W=100μm, Pitch=2.94μm, NF=4, WF=25μm	-	-	64.7	74.1	-	mΩmm ²

3. Parameters → 3.34 PMV module→ 3.34.2 Device parameters→ pmvf→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
RONPMVF	on resistance @ VG=-5V, VD=-0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	15.7	18.9	22	25.2	28.3	kΩμm
TC_VTXPMVF	threshold voltage temperature coefficient	-	-	1.4	-	-	mV/K
VTXPMVFL	extrapolated threshold voltage long channel @ VD=-0.1V, L=10μm, W=50μm, NF=2, WF=25μm	-	-	-0.83	-	-	V
VTXPMVFS	extrapolated threshold voltage short channel @ VD=-0.1V, L=0.4μm, W=100μm, NF=4, WF=25μm	-1.05	-0.95	-0.85	-0.75	-0.65	V

3. Parameters → 3.35 SJHVL module

3.35 SJHVL module

3.35.1 Device parameters

nhsj1b_2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-50	-45	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	45	50	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	45	50	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-50	-45	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B2S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	52	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5NHS1B2S	saturation current @ VG=5V, VD=15V, L=0.5µm, W=20µm, NF=2, WF=10µm	164	185	205	225	246	µA/µm
IDPNHS1B2S	pulsed drain current @ VG=5V, VD=15V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=20µm, NF=2, WF=10µm	-	-	248	-	-	µA/µm
ROANHS1B2S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=20µm, Pitch=4.25µm, NF=2, WF=10µm	-	-	45	49.5	-	mΩmm ²
RO_NHS1B2S	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	8.5	9.5	10.6	11.7	12.7	kΩµm
TC_BDSNHS1B2S	breakdown temperature coefficient	-	-	0.04	-	-	V/K
TC_VTNHS1B2S	Threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	-1.7	-	-	mV/K
VT1NHS1B2	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80µm	-	-	63	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 Technical Report UHV Characteristics" at "my X-FAB"						
VTXNHS1B2S	extrapolated threshold voltage @ VD=0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	0.78	0.88	0.98	1.08	1.18	V

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → nhsj1b_2 → Matching parameters

Matching parameters

Name	Description	Typ	Unit
ABTNHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AIDNHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AIDNHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AIDNHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AIDNHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AIDNHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AIDNHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AIDNHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AIDNHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVTNHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLTNHSJ1B	transistor delta length	0	μm
DWTNHSJ1B	transistor delta width	0	μm

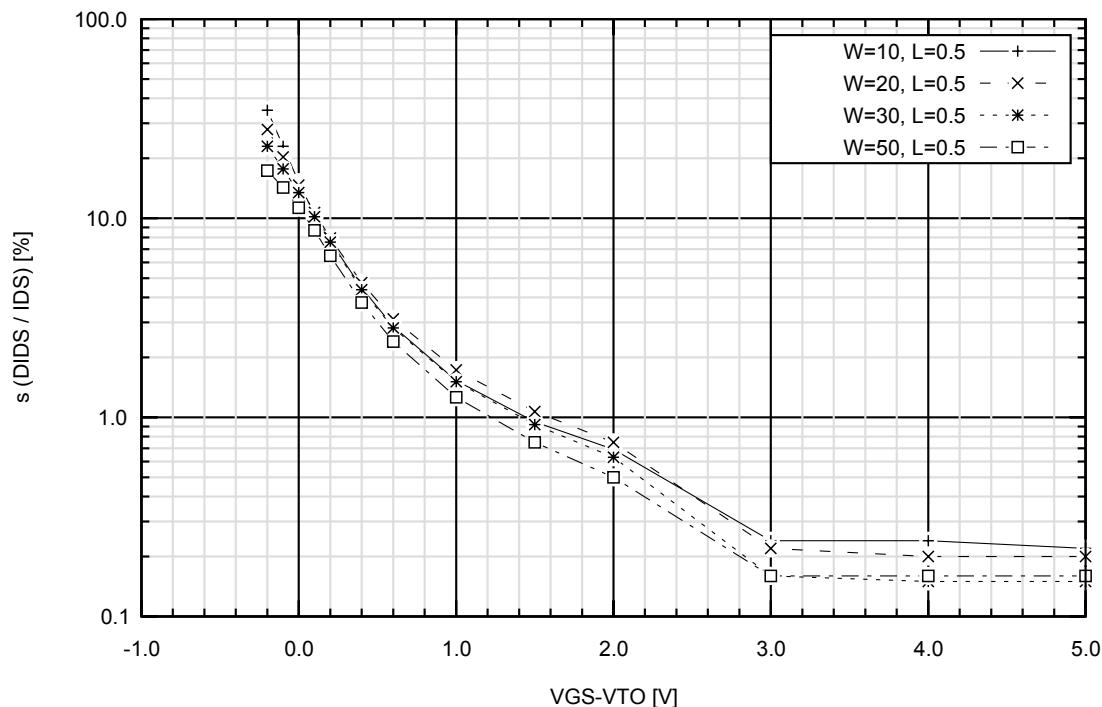


Figure 3.73 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1b_4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-80	-72	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	72	80	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	72	80	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-80	-72	1	1.5	V

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3. Parameters → 3.35 SJHVL module→ 3.35.1 Device parameters→ nhsj1b_4→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B4S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	83	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5NHS1B4S	saturation current @ VG=5V, VD=15V, L=0.5µm, W=20µm, NF=2, WF=10µm	136	153	170	187	204	µA/µm
IDPNHS1B4S	pulsed drain current @ VG=5V, VD=15V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=20µm, NF=2, WF=10µm	-	-	205	-	-	µA/µm
ROANHS1B4S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=20µm, Pitch=5.75µm, NF=2, WF=10µm	-	-	95	104.5	-	mΩmm ²
RO_NHS1B4S	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	13.2	14.9	16.5	18.1	19.8	kΩµm
TC_BDSNHS1B4S	breakdown temperature coefficient	-	-	0.08	-	-	V/K
TC_VTNHS1B4S	Threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	-1.8	-	-	mV/K
VT1NHS1B4	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80µm	-	-	94	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 Technical Report UHV Characteristics" at "my X-FAB"						
VTXNHS1B4S	extrapolated threshold voltage @ VD=0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	0.79	0.89	0.99	1.09	1.19	V

Matching parameters

Name	Description	Typ	Unit
ABTNHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%µm
AIDNHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%µm
AIDNHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%µm
AIDNHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%µm
AIDNHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%µm
AIDNHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%µm
AIDNHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%µm
AIDNHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%µm

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → nhsj1b_4 → Matching parameters

Name	Description	Typ	Unit
AIDNHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVTNHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLTNHSJ1B	transistor delta length	0	μm
DWTNHSJ1B	transistor delta width	0	μm

Note: Matching data are valid for L=0.5 μm. Transistors with channel lengths > 0.5 μm will exhibit greater mismatch of parameters. More information available on request.

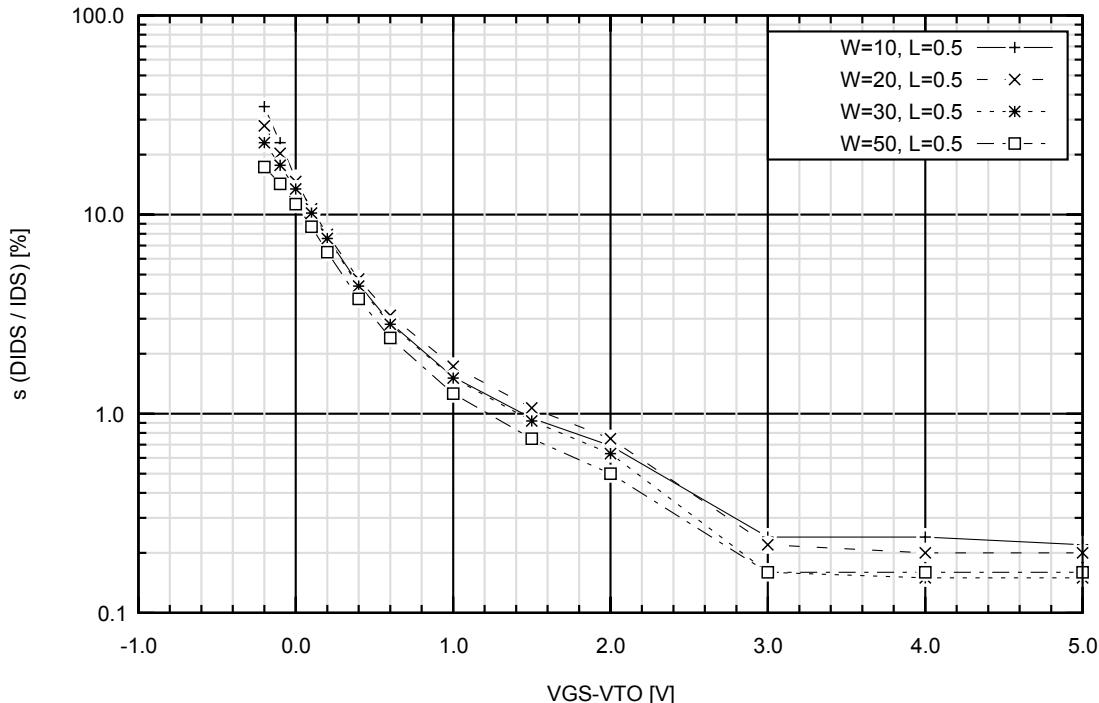


Figure 3.74 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1b_5**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-105	-95	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	95	105	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	95	105	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-105	-95	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → nhsj1b_5 → Operating conditions

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

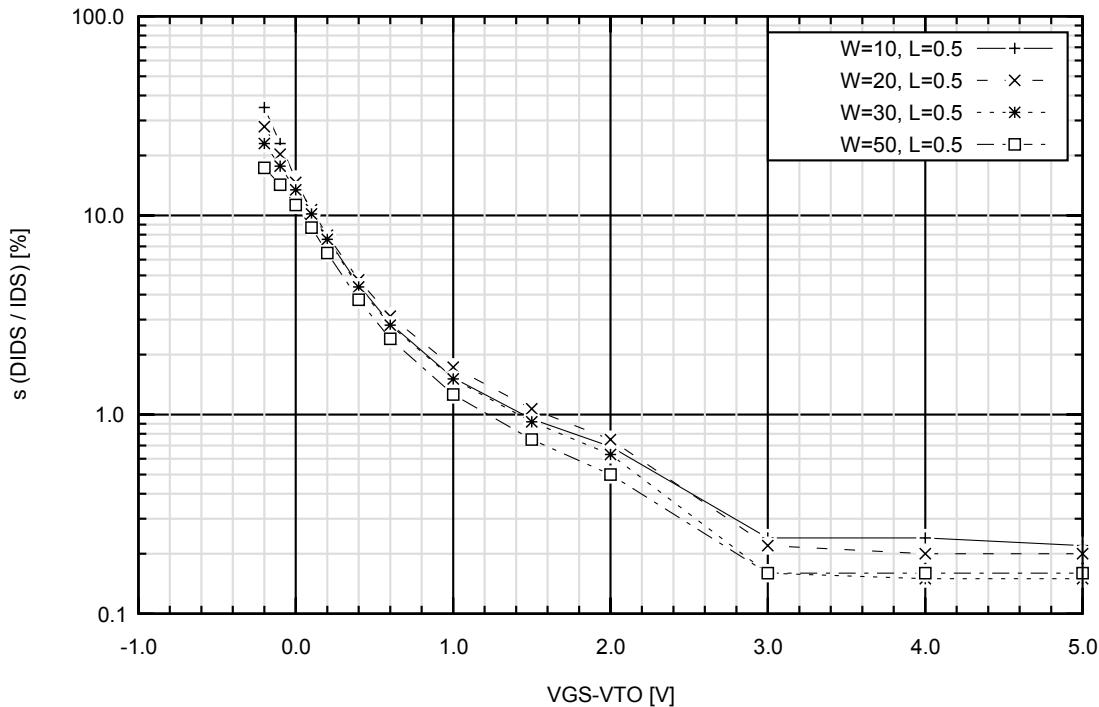
Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B5S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	109	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5NHS1B5S	saturation current @ VG=5V, VD=20V, L=0.5μm, W=20μm, NF=2, WF=10μm	128	144	160	176	192	μA/μm
IDPNHS1B5S	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	216	-	-	μA/μm
ROANHS1B5S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, Pitch=7.25μm, NF=2, WF=10μm	-	-	160	176	-	mΩmm ²
RO_NHS1B5S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	18	20	22	24	26	kΩμm
TC_BDSNHS1B5S	breakdown temperature coefficient	-	-	0.1	-	-	V/K
TC_VTNHS1B5S	Threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	-1.8	-	-	mV/K
VT1NHS1B5	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	122	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1B5S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	0.8	0.9	1	1.1	1.2	V

Matching parameters

Name	Description	Typ	Unit
ABTNHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AIDNHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AIDNHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AIDNHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AIDNHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AIDNHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AIDNHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AIDNHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AIDNHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVTNHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLTNHSJ1B	transistor delta length	0	μm
DWTNHSJ1B	transistor delta width	0	μm

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → nhsj1b_5 → Matching parameters

**Figure 3.75** Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nhsj1b_7****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-125	-115	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	115	125	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	115	125	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-125	-115	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B7S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	132	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.35 SJHVL module→ 3.35.1 Device parameters→ nhsj1b_7→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1B7S	saturation current @ VG=5V, VD=20V, L=0.5μm, W=30μm, NF=2, WF=15μm	112	126	140	154	168	μA/μm
IDP_NHS1B7S	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=30μm, NF=2, WF=15μm	-	-	200	-	-	μA/μm
ROA_NHS1B7S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=30μm, Pitch=8.75μm, NF=2, WF=15μm	-	-	250	275	-	mΩmm ²
RO_NHS1B7S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=30μm, NF=2, WF=15μm	22.9	25.7	28.6	31.5	34.3	kΩμm
TC_BDSNHS1B7S	breakdown temperature coefficient	-	-	0.12	-	-	V/K
TC_VTNHS1B7S	Threshold voltage temperature coefficient @ L=0.5μm, W=30μm	-	-	-1.9	-	-	mV/K
VT1NHS1B7	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	148	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1B7S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=30μm, NF=2, WF=15μm	0.81	0.91	1.01	1.11	1.21	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → nhsj1b_7 → Matching parameters

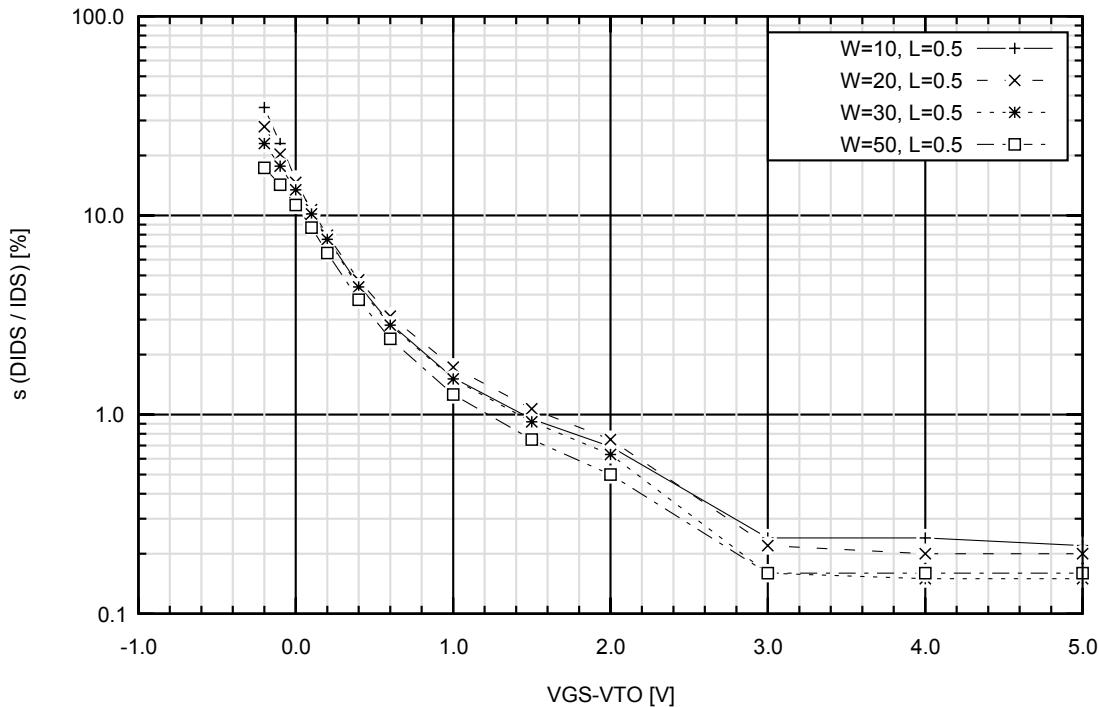


Figure 3.76 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj2b_7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	115	125	V
VDS	-40°C to 175°C	-125	-115	1.5	-	V
VDB	-40°C to 175°C	-125	-115	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-125	-115	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS2B7S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	132	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5PHS2B7S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	78	88	97	106	116	μA/μm
IDPPHS2B7S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	130	-	-	μA/μm

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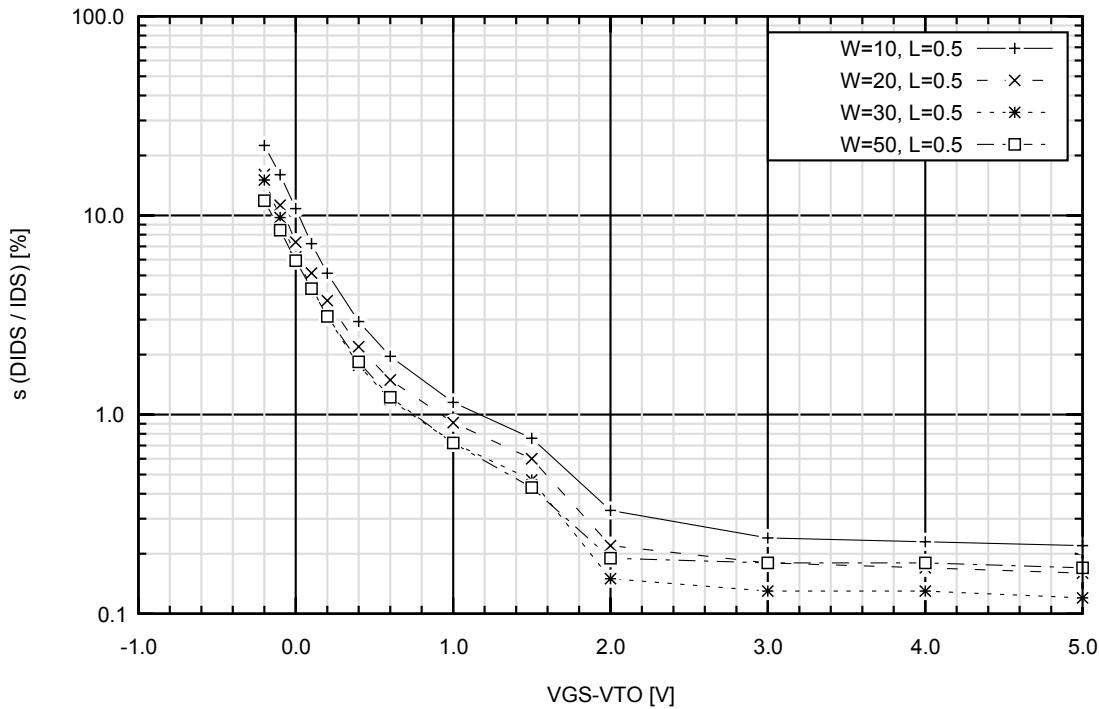
3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → phsj2b_7 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS2B7S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=9µm, NF=2, WF=10µm	-	-	568	625	-	mΩmm ²
RO _PHS2B7S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	51	57	63	69	75	kΩµm
TC _BDSPHS2B7S	breakdown temperature coefficient	-	-	0.12	-	-	V/K
TC _VTPHS2B7S	threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	1.96	-	-	mV/K
VTX PHS2B7S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%µm
AID PHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%µm
AID PHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%µm
AID PHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%µm
AID PHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%µm
AID PHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%µm
AID PHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%µm
AID PHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%µm
AID PHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%µm
AVT PHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVµm
DLT PHSJ2B	transistor delta length	0	µm
DWT PHSJ2B	transistor delta width	0	µm

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → phsj2b_7 → Matching parameters

**Figure 3.77** Device phsj2b: drain current matching vs. VGS-VTO (typical values, drawn W and L)**phsj1a_4****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	72	80	V
VDS	-40°C to 175°C	-80	-72	1.5	-	V
VDB	-40°C to 175°C	-80	-72	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-80	-72	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS _{1A4S}	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	83	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5 _{1A4S}	saturation current @ VG=-5V, VD=-30V, L=0.5μm, W=20μm, NF=2, WF=10μm	84	94.5	105	115.5	126	μA/μm
IDP _{1A4S}	pulsed drain current @ VG=-5V, VD=-30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	150	-	-	μA/μm

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3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → phsj1a_4 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA _{PHS1A4S}	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=6µm, NF=2, WF=10µm	-	-	395	435	-	mΩmm ²
RO _{PHS1A4S}	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	53	59	66	73	79	kΩµm
TC _{BDS_{PHS1A4S}}	breakdown temperature coefficient	-	-	0.1	-	-	V/K
TC _{VTP_{PHS1A4S}}	threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	1.9	-	-	mV/K
VTX _{PHS1A4S}	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT _{PHSJ1A}	pelgrom coefficient gain factor mismatch	3.04	%µm
AID _{PHSJ1A00}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID _{PHSJ1A02}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID _{PHSJ1A04}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID _{PHSJ1A06}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID _{PHSJ1A10}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID _{PHSJ1A20}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID _{PHSJ1A30}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID _{PHSJ1A50}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT _{PHSJ1A}	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT _{PHSJ1A}	transistor delta length	0	µm
DWT _{PHSJ1A}	transistor delta width	0	µm

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → phsj1a_4 → Matching parameters

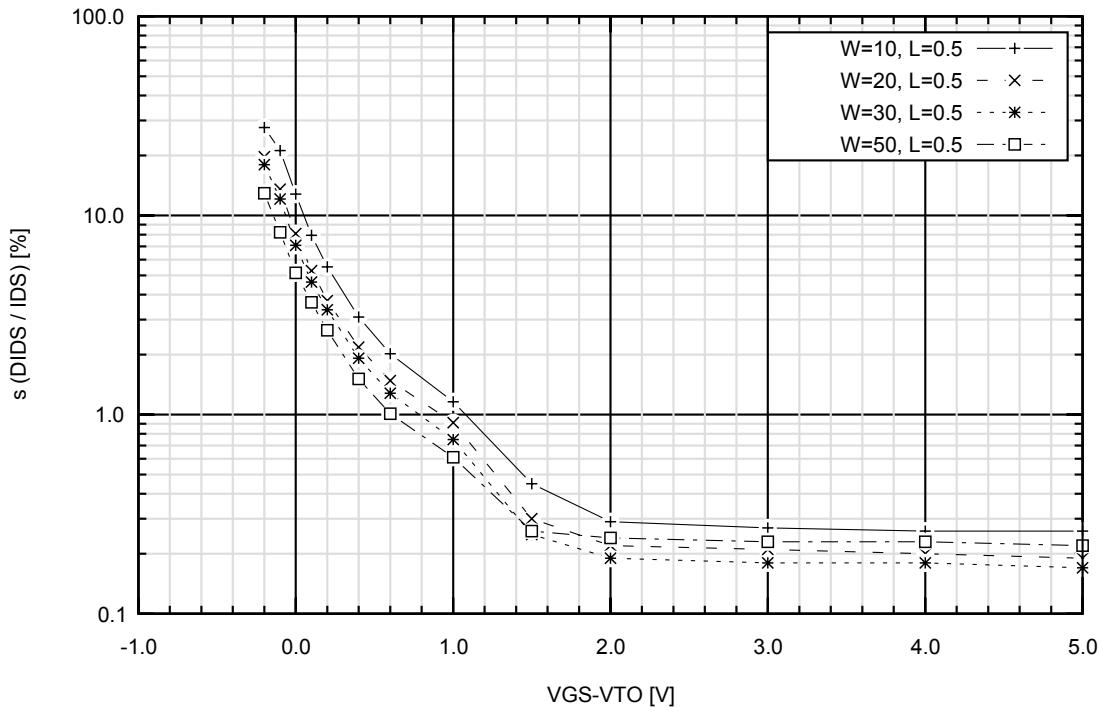


Figure 3.78 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	95	105	V
VDS	-40°C to 175°C	-105	-95	1.5	-	V
VDB	-40°C to 175°C	-105	-95	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-105	-95	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A5S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	109	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS1A5S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	76	85.5	95	104.5	114	μA/μm
IDPPHS1A5S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	126	-	-	μA/μm

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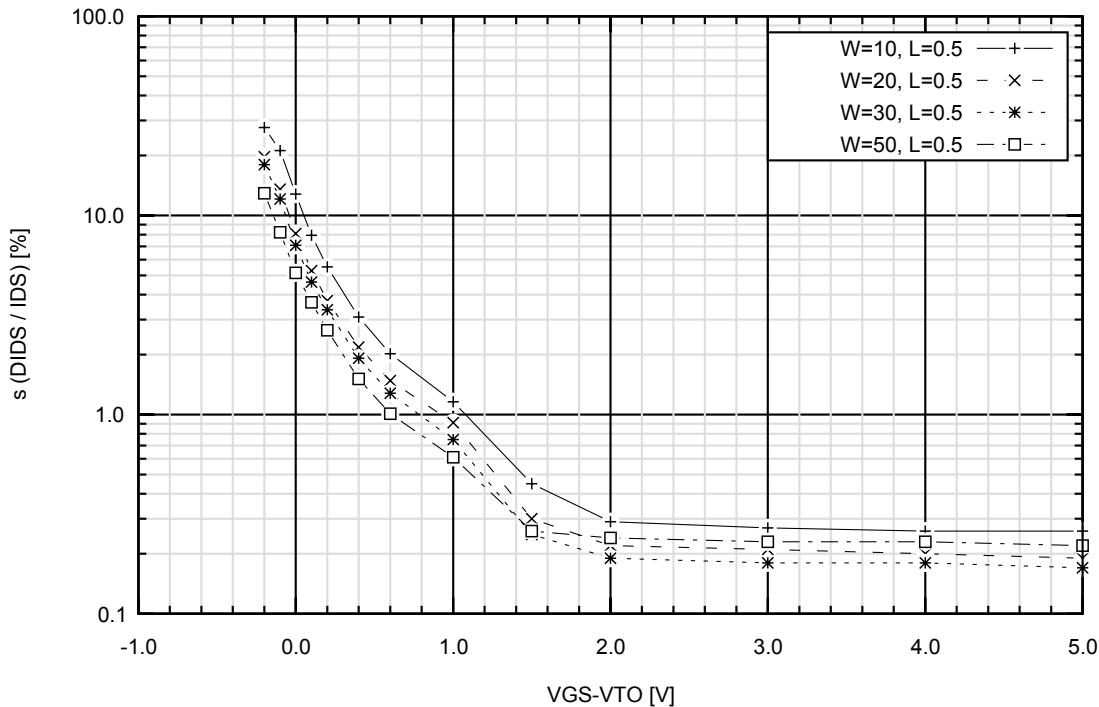
3. Parameters → 3.35 SJHVL module→ 3.35.1 Device parameters→ phsj1a_5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A5S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=7.5µm, NF=2, WF=10µm	-	-	630	693	-	mΩmm ²
RO _PHS1A5S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	67	76	84	92	101	kΩµm
TC _BDSPHS1A5S	breakdown temperature coefficient	-	-	0.11	-	-	V/K
TC _VTPHS1A5S	threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	1.9	-	-	mV/K
VTX PHS1A5S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → phsj1a_5 → Matching parameters

**Figure 3.79** Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)**phsj1a_7****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	115	125	V
VDS	-40°C to 175°C	-125	-115	1.5	-	V
VDB	-40°C to 175°C	-125	-115	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-125	-115	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS _{1A7S}	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	132	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5 _{1A7S}	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	67	75.5	84	92.5	101	μA/μm
IDP _{1A7S}	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	110	-	-	μA/μm

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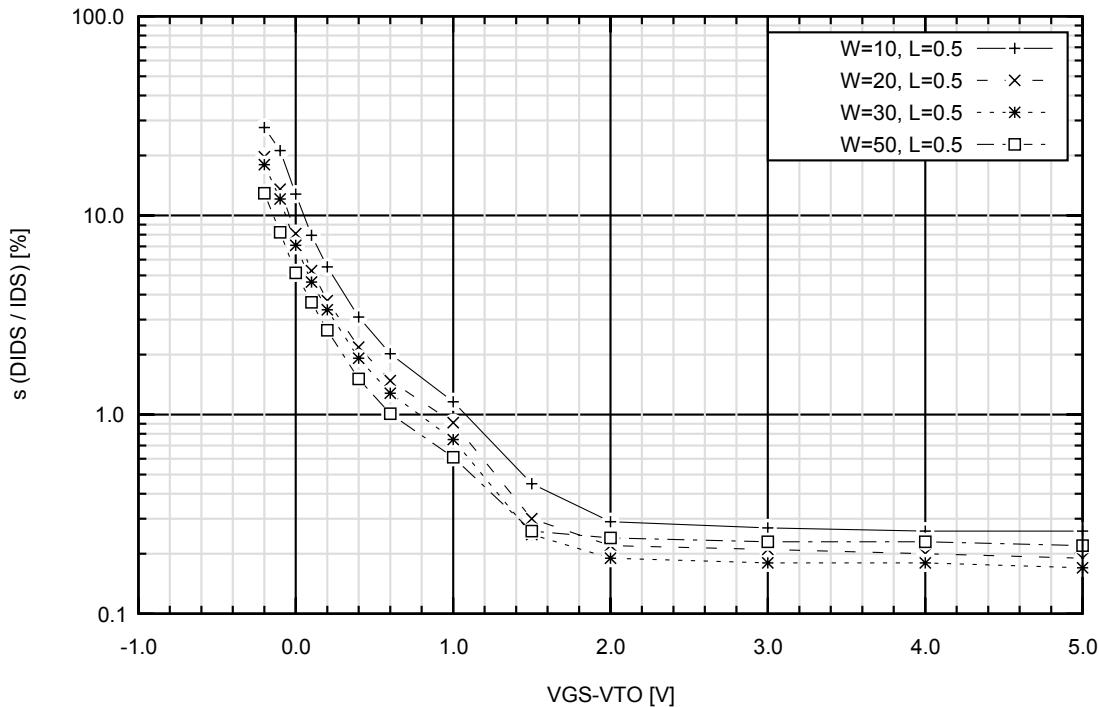
3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → phsj1a_7 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A7S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=9µm, NF=2, WF=10µm	-	-	920	1012	-	mΩmm ²
RO _PHS1A7S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	82	92	102	112	122	kΩµm
TC _BDSPHS1A7S	breakdown temperature coefficient	-	-	0.12	-	-	V/K
TC _VTPHS1A7S	threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	2	-	-	mV/K
VTX PHS1A7S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → phsj1a_7 → Matching parameters

**Figure 3.80** Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)**dfwnsj1b_2****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-50	-45	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-50	-45	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B2	reverse breakdown voltage @ L=2.5μm, W=22μm, NF=2, WF=11μm	52	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1B2	leakage current @ VL=45V, T=27°C, W=22μm, NF=2, WF=11μm	-	-	0.09	-	-	pA
IL_DNSJ1B2HT	leakage current @ VL=45V, T=175°C, W=22μm, NF=2, WF=11μm	-	-	0.33	-	-	nA

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3. Parameters → 3.35 SJHVL module → 3.35.1 Device parameters → dfwnsj1b_2 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ1B2	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B2	forward voltage @ Idio=22µA, L=2.5µm, W=22µm, NF=2, WF=11µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-80	-72	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-80	-72	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B4	reverse breakdown voltage @ L=4µm, W=22µm, NF=2, WF=11µm	83	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1B4	leakage current @ VL=72V, T=27°C, W=22µm, NF=2, WF=11µm	-	-	0.17	-	-	pA
IL_DNSJ1B4HT	leakage current @ VL=72V, T=175°C, W=22µm, NF=2, WF=11µm	-	-	0.47	-	-	nA
TC_VDFDNSJ1B4	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B4	forward voltage @ Idio=22µA, L=4µm, W=22µm, NF=2, WF=11µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-105	-95	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-105	-95	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm



3. Parameters → 3.35 SJHVL module→ 3.35.1 Device parameters→ dfwnsj1b_5→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B5	reverse breakdown voltage @ L=5.5µm, W=22µm, NF=2, WF=11µm	109	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DNSJ1B5	leakage current @ VL=95V, T=27°C, W=22µm, NF=2, WF=11µm	-	-	0.33	-	-	pA
IL_DNSJ1B5HT	leakage current @ VL=95V, T=175°C, W=22µm, NF=2, WF=11µm	-	-	0.78	-	-	nA
TC_VDFDNSJ1B5	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B5	forward voltage @ Idio=22µA, L=5.5µm, W=22µm, NF=2, WF=11µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_7**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-125	-115	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-125	-115	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B7	reverse breakdown voltage @ L=7µm, W=32µm, NF=2, WF=16µm	132	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DNSJ1B7	leakage current @ VL=115V, T=27°C, W=32µm, NF=2, WF=16µm	-	-	0.4	-	-	pA
IL_DNSJ1B7HT	leakage current @ VL=115V, T=175°C, W=32µm, NF=2, WF=16µm	-	-	0.97	-	-	nA

3. Parameters → 3.35 SJHVL module→ 3.35.1 Device parameters→ dfwnsj1b_7→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ1B7	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B7	forward voltage @ Idio=32µA, L=7µm, W=32µm, NF=2, WF=16µm	0.74	0.76	0.78	0.8	0.82	V

3. Parameters → 3.36 SJHVM module

3.36 SJHVM module

3.36.1 Device parameters

nhsj1b_8

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-155	-140	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	140	155	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	140	155	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-155	-140	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B8S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	161	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5NHS1B8S	saturation current @ VG=5V, VD=20V, L=0.5µm, W=36µm, NF=2, WF=18µm	104	117	130	143	156	µA/µm
IDPNHS1B8S	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=36µm, NF=2, WF=18µm	-	-	184	-	-	µA/µm
ROANHS1B8S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=36µm, Pitch=10.25µm, NF=2, WF=18µm	-	-	360	396	-	mΩmm ²
RO_NHS1B8S	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=36µm, NF=2, WF=18µm	28	32	35	38	42	kΩµm
TC_BDSNHS1B8S	breakdown temperature coefficient	-	-	0.14	-	-	V/K
TC_VTNHS1B8S	Threshold voltage temperature coefficient @ L=0.5µm, W=36µm	-	-	-1.9	-	-	mV/K
VT1NHS1B8	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80µm	-	-	172	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 Technical Report UHV Characteristics" at "my X-FAB"						
VTXNHS1B8S	extrapolated threshold voltage @ VD=0.1V, L=0.5µm, W=36µm, NF=2, WF=18µm	0.82	0.92	1.02	1.12	1.22	V

3. Parameters → 3.36 SJHVM module → 3.36.1 Device parameters → nhsj1b_8 → Matching parameters

Matching parameters

Name	Description	Typ	Unit
ABTNHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AIDNHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AIDNHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AIDNHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AIDNHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AIDNHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AIDNHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AIDNHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AIDNHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVTNHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLTNHSJ1B	transistor delta length	0	μm
DWTNHSJ1B	transistor delta width	0	μm

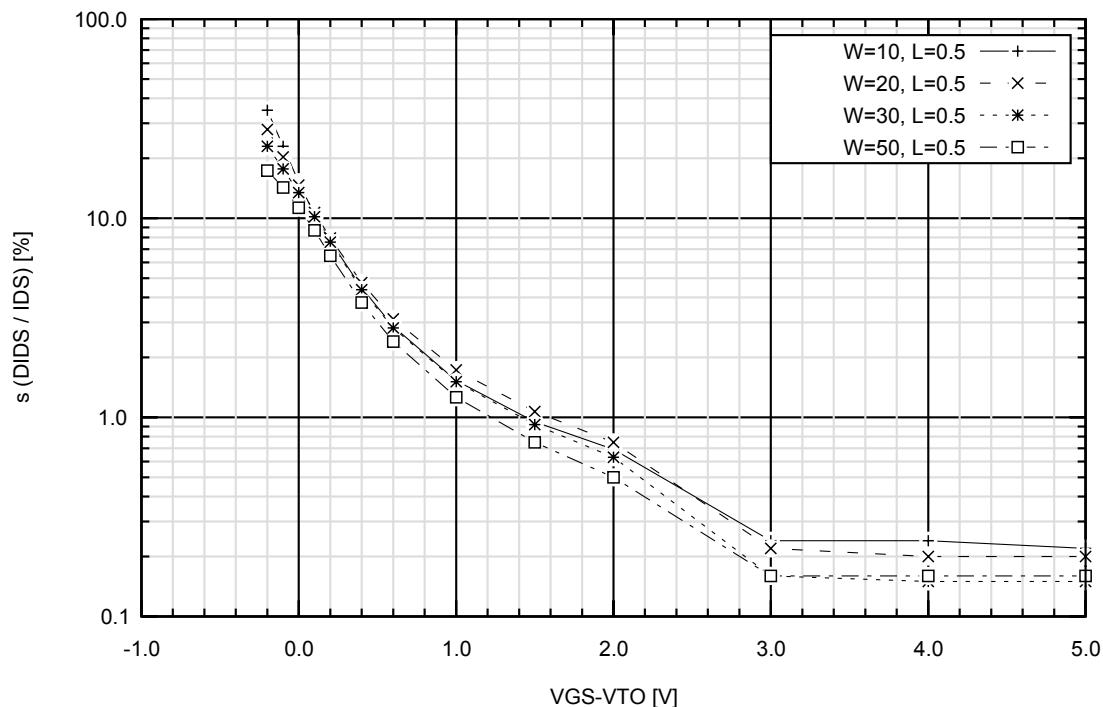


Figure 3.81 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1b_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-170	-155	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	155	170	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	155	170	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-170	-155	1	1.5	V

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3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ nhsj1b_10→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

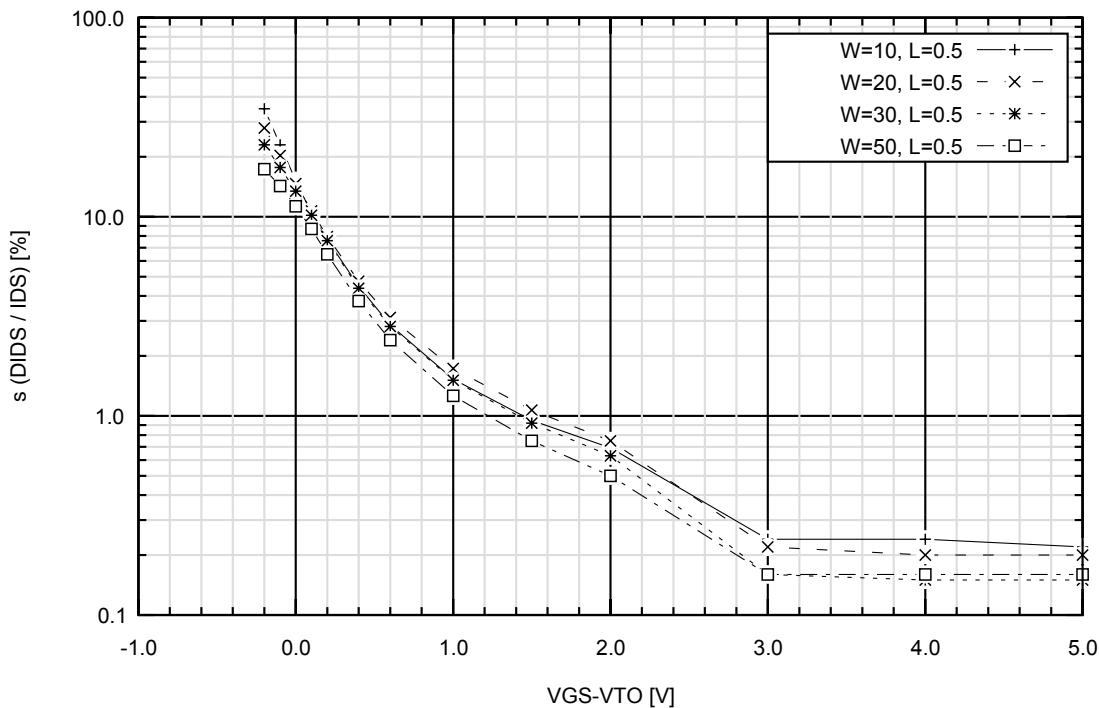
Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B10S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	178	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5NHS1B10S	saturation current @ VG=5V, VD=20V, L=0.5µm, W=40µm, NF=2, WF=20µm	100	113	125	137	150	µA/µm
IDPNHS1B10S	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=40µm, NF=2, WF=20µm	-	-	173	-	-	µA/µm
ROANHS1B10S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=40µm, Pitch=11.75µm, NF=2, WF=20µm	-	-	480	528	-	mΩmm²
RO_NHS1B10S	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=40µm, NF=2, WF=20µm	32.8	36.9	40.9	44.9	49	kΩµm
TC_BDSNHS1B10S	breakdown temperature coefficient	-	-	0.16	-	-	V/K
TC_VTNHS1B10S	Threshold voltage temperature coefficient @ L=0.5µm, W=40µm	-	-	-1.9	-	-	mV/K
VT1NHS1B10	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80µm	-	-	192	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 Technical Report UHV Characteristics" at "my X-FAB"						
VTXNHS1B10S	extrapolated threshold voltage @ VD=0.1V, L=0.5µm, W=40µm, NF=2, WF=20µm	0.83	0.93	1.03	1.13	1.23	V

Matching parameters

Name	Description	Typ	Unit
ABTNHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%µm
AIDNHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%µm
AIDNHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%µm
AIDNHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%µm
AIDNHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%µm
AIDNHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%µm
AIDNHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%µm
AIDNHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%µm

3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ nhsj1b_10→ Matching parameters

Name	Description	Typ	Unit
AIDNHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	% μ m
AVTNHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mV μ m
DLTNHSJ1B	transistor delta length	0	μ m
DWTNHSJ1B	transistor delta width	0	μ m

**Figure 3.82** Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nhsj1a_13****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-215	-195	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	195	215	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	195	215	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-215	-195	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/ μ m
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/ μ m

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.**Note 2** This operating condition will not be checked by automatic check tools.**Note 3** This forward current is allowed only for transistor's drain bulk junction**Note 4** Pulsed operation with negligible self-heating (<=100ns)**Note:** The node B (BULK) is: PWELL2**Note:** The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ nhsj1a_13→ Process parameters

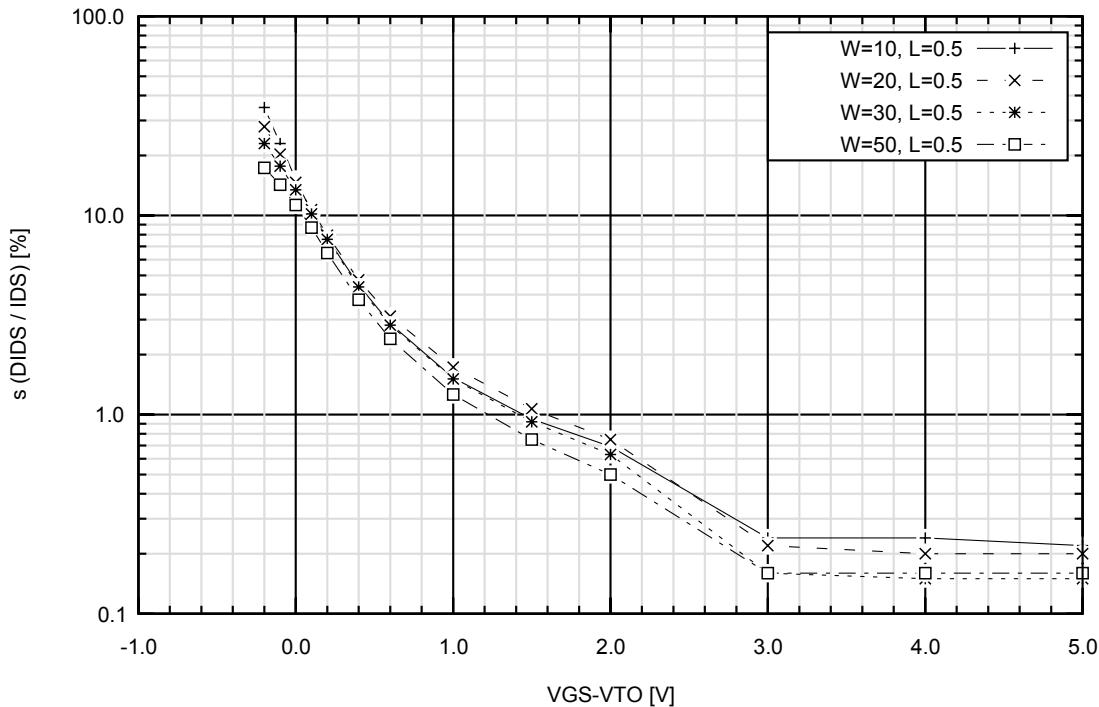
Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1A13S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	224	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5NHS1A13S	saturation current @ VG=5V, VD=30V, L=0.5μm, W=50μm, NF=2, WF=25μm	92	104	115	126	138	μA/μm
IDPNHS1A13S	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	163	-	-	μA/μm
ROANHS1A13S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, Pitch=15μm, NF=2, WF=25μm	-	-	770	847	-	mΩmm ²
RO_NHS1A13S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	41	46	51	56	61	kΩμm
TC_BDSNHS1A13S	breakdown temperature coefficient	-	-	0.2	-	-	V/K
TC_VTNHS1A13S	Threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	-1.9	-	-	mV/K
VT1NHS1A13	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	214	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1A13S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	0.87	0.97	1.07	1.17	1.27	V

Matching parameters

Name	Description	Typ	Unit
ABTNHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AIDNHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AIDNHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AIDNHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AIDNHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AIDNHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AIDNHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AIDNHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AIDNHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVTNHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLTNHSJ1B	transistor delta length	0	μm
DWTNHSJ1B	transistor delta width	0	μm

3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ nhsj1a_13→ Matching parameters

**Figure 3.83** Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nhsj1a_16****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-255	-235	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	235	255	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	235	255	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-255	-235	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1A16S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	270	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ nhsj1a_16→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1A16S	saturation current @ VG=5V, VD=30V, L=0.5μm, W=60μm, NF=2, WF=30μm	88	99	110	121	132	μA/μm
IDP_NHS1A16S	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=60μm, NF=2, WF=30μm	-	-	157	-	-	μA/μm
ROA_NHS1A16S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=60μm, Pitch=18μm, NF=2, WF=30μm	-	-	1150	1265	-	mΩmm ²
RO_NHS1A16S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=60μm, NF=2, WF=30μm	51	58	64	70	77	kΩμm
TC_BDSNHS1A16S	breakdown temperature coefficient	-	-	0.24	-	-	V/K
TC_VTNHS1A16S	Threshold voltage temperature coefficient @ L=0.5μm, W=60μm	-	-	-2	-	-	mV/K
VT1NHS1A16	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	236	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1A16S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=60μm, NF=2, WF=30μm	0.87	0.97	1.07	1.17	1.27	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ nhsj1a_16→ Matching parameters

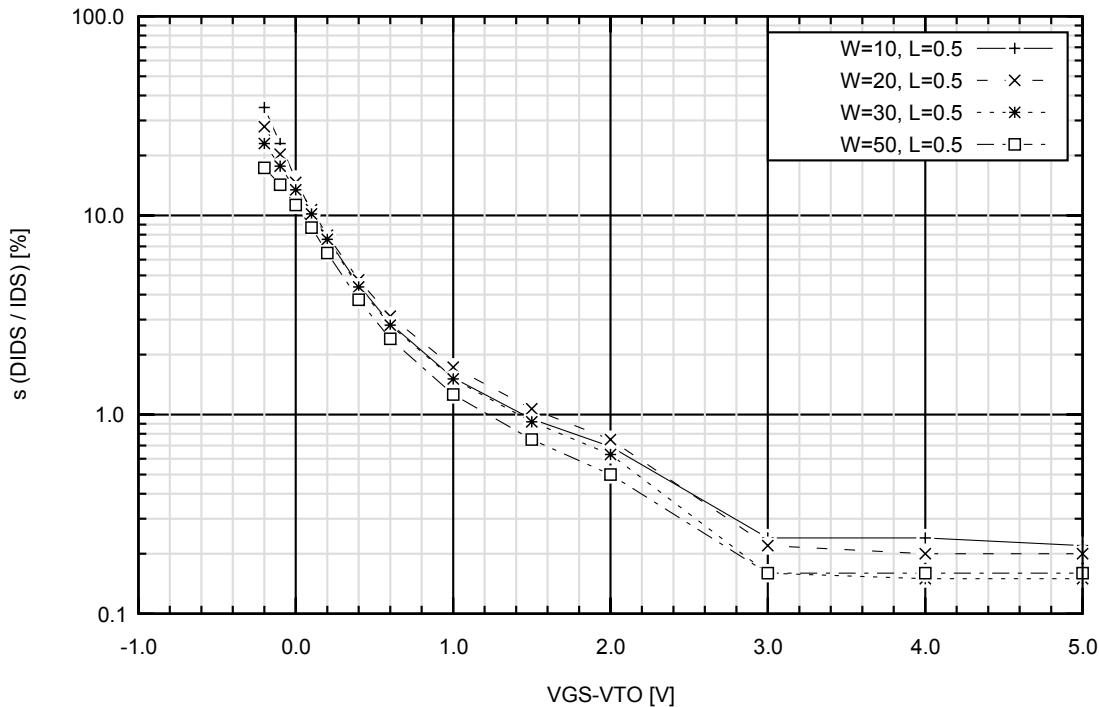


Figure 3.84 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj2b_8

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	140	155	V
VDS	-40°C to 175°C	-155	-140	1.5	-	V
VDB	-40°C to 175°C	-155	-140	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-155	-140	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS ₁ PHS2B8S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	161	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5 ₁ PHS2B8S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	73	82	91	100	109	μA/μm
IDP ₁ PHS2B8S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	122	-	-	μA/μm

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3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj2b_8→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA _{PHS2B8S}	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, Pitch=10.5μm, NF=2, WF=10μm	-	-	750	825	-	mΩmm ²
RO _{PHS2B8S}	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	57	64	71	78	85	kΩμm
TC _{BDS_{PHS2B8S}}	breakdown temperature coefficient	-	-	0.14	-	-	V/K
TC _{VTP_{PHS2B8S}}	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	1.95	-	-	mV/K
VTX _{PHS2B8S}	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABT _{PHSJ2B}	pelgrom coefficient gain factor mismatch	2.26	%μm
AID _{PHSJ2B00}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%μm
AID _{PHSJ2B02}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%μm
AID _{PHSJ2B04}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%μm
AID _{PHSJ2B06}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%μm
AID _{PHSJ2B10}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%μm
AID _{PHSJ2B20}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%μm
AID _{PHSJ2B30}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%μm
AID _{PHSJ2B50}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVT _{PHSJ2B}	pelgrom coefficient threshold voltage mismatch	13.83	mVμm
DLT _{PHSJ2B}	transistor delta length	0	μm
DWT _{PHSJ2B}	transistor delta width	0	μm

phsj2b_10**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	155	170	V
VDS	-40°C to 175°C	-170	-155	1.5	-	V
VDB	-40°C to 175°C	-170	-155	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-170	-155	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS _{PHS2B10S}	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	178	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj2b_10→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5PHS2B10S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	68	77	85	93	102	μA/μm
IDP_PHS2B10S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	115	-	-	μA/μm
ROA_PHS2B10S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, Pitch=12μm, NF=2, WF=10μm	-	-	951	1046	-	mΩmm ²
RO_PHS2B10S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	64	71.5	79	86.5	94	kΩμm
TC_BDSPHS2B10S	breakdown temperature coefficient	-	-	0.16	-	-	V/K
TC_VTPHS2B10S	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	1.97	-	-	mV/K
VTX_PHS2B10S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%μm
AIDPHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%μm
AIDPHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%μm
AIDPHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%μm
AIDPHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%μm
AIDPHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%μm
AIDPHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%μm
AIDPHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%μm
AIDPHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVTPHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVμm
DLTPHSJ2B	transistor delta length	0	μm
DWT_PHSJ2B	transistor delta width	0	μm

phsj2b_13

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	195	215	V
VDS	-40°C to 175°C	-215	-195	1.5	-	V
VDB	-40°C to 175°C	-215	-195	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-215	-195	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

3. Parameters → 3.36 SJHVM module → 3.36.1 Device parameters → phsj2b_13 → Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS2B13S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	224	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5PHS2B13S	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=50μm, NF=2, WF=25μm	60	68	75	82	90	μA/μm
IDPPHS2B13S	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	109	-	-	μA/μm
ROAPHS2B13S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, Pitch=15μm, NF=2, WF=25μm	-	-	1589	1748	-	mΩmm²
RO_PHS2B13S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	85	95.5	106	116.5	127	kΩμm
TC_BDSPHS2B13S	breakdown temperature coefficient	-	-	0.18	-	-	V/K
TC_VTPHS2B13S	threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	2.03	-	-	mV/K
VTXPHS2B13S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%μm
AIDPHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%μm
AIDPHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%μm
AIDPHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%μm
AIDPHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%μm
AIDPHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%μm
AIDPHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%μm
AIDPHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%μm
AIDPHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVTPHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVμm
DLTPHSJ2B	transistor delta length	0	μm
DWTPHSJ2B	transistor delta width	0	μm

phsj2b_16

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	235	255	V
VDS	-40°C to 175°C	-255	-235	1.5	-	V
VDB	-40°C to 175°C	-255	-235	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V

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3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj2b_16→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VB-NB ⁽¹⁾	-40°C to 175°C	-255	-235	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS2B16S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	270	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5PHS2B16S	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=60μm, NF=2, WF=30μm	56.5	64	71.5	79	86.5	μA/μm
IDPPHS2B16S	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=60μm, NF=2, WF=30μm	-	-	101	-	-	μA/μm
ROAPHS2B16S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=60μm, Pitch=18μm, NF=2, WF=30μm	-	-	2286	2394	-	mΩmm ²
RO_PHS2B16S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=60μm, NF=2, WF=30μm	115	121	127	133	139	kΩμm
TC_BDSPHS2B16S	breakdown temperature coefficient	-	-	0.19	-	-	V/K
TC_VTPHS2B16S	threshold voltage temperature coefficient @ L=0.5μm, W=60μm	-	-	2.01	-	-	mV/K
VTXPHS2B16S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=60μm, NF=2, WF=30μm	-1.35	-1.28	-1.2	-1.12	-1.05	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ2B	pelgrom coefficient gain factor mismatch	2.26	%μm
AIDPHSJ2B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	24.47	%μm
AIDPHSJ2B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.04	%μm
AIDPHSJ2B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	6.96	%μm
AIDPHSJ2B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.67	%μm
AIDPHSJ2B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.78	%μm
AIDPHSJ2B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.72	%μm
AIDPHSJ2B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.57	%μm
AIDPHSJ2B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.52	%μm
AVTPHSJ2B	pelgrom coefficient threshold voltage mismatch	13.83	mVμm
DLTPHSJ2B	transistor delta length	0	μm
DWTPHSJ2B	transistor delta width	0	μm

3. Parameters → 3.36 SJHVM module → 3.36.1 Device parameters → phsj1a_8 → Operating conditions

phsj1a_8

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	140	155	V
VDS	-40°C to 175°C	-155	-140	1.5	-	V
VDB	-40°C to 175°C	-155	-140	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-155	-140	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A8S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	161	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS1A8S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	62	69.5	77	84.5	92	μA/μm
IDPPHS1A8S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	105	-	-	μA/μm
ROAPHS1A8S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, Pitch=10.5μm, NF=2, WF=10μm	-	-	1250	1375	-	mΩmm ²
RO_PHS1A8S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	95	107	119	131	143	kΩμm
TC_BDSPHS1A8S	breakdown temperature coefficient	-	-	0.13	-	-	V/K
TC_VTPHS1A8S	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	2	-	-	mV/K
VTXPHS1A8S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%μm
AIDPHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%μm
AIDPHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%μm
AIDPHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%μm
AIDPHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%μm
AIDPHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%μm
AIDPHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%μm
AIDPHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%μm

3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj1a_8→ Matching parameters

Name	Description	Typ	Unit
AIDPHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	% μ m
AVTPHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mV μ m
DLTPHSJ1A	transistor delta length	0	μ m
DWTPHSJ1A	transistor delta width	0	μ m

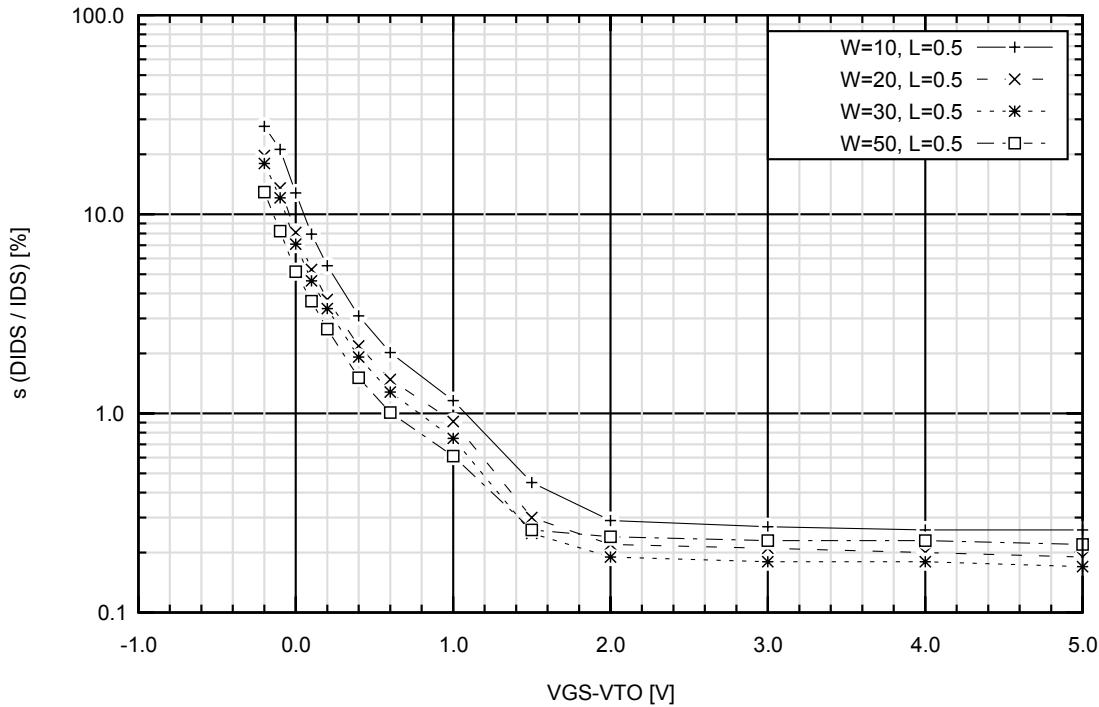


Figure 3.85 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_10**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	155	170	V
VDS	-40°C to 175°C	-170	-155	1.5	-	V
VDB	-40°C to 175°C	-170	-155	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-170	-155	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A10S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5 μ m	178	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							



3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj1a_10→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5PHS1A10S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	58	65	72	79	86	μA/μm
IDP ₁ PHS1A10S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	106	-	-	μA/μm
ROA ₁ PHS1A10S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, Pitch=12μm, NF=2, WF=10μm	-	-	1630	1793	-	mΩmm ²
RO ₁ PHS1A10S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	109	122	136	150	163	kΩμm
TC ₁ BDS ₁ PHS1A10S	breakdown temperature coefficient	-	-	0.14	-	-	V/K
TC ₁ VTPHS1A10S	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	2.1	-	-	mV/K
VTX ₁ PHS1A10S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%μm
AIDPHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%μm
AIDPHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%μm
AIDPHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%μm
AIDPHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%μm
AIDPHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%μm
AIDPHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%μm
AIDPHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%μm
AIDPHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%μm
AVTPHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVμm
DLTPHSJ1A	transistor delta length	0	μm
DWT ₁ PHSJ1A	transistor delta width	0	μm

3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj1a_10→ Matching parameters

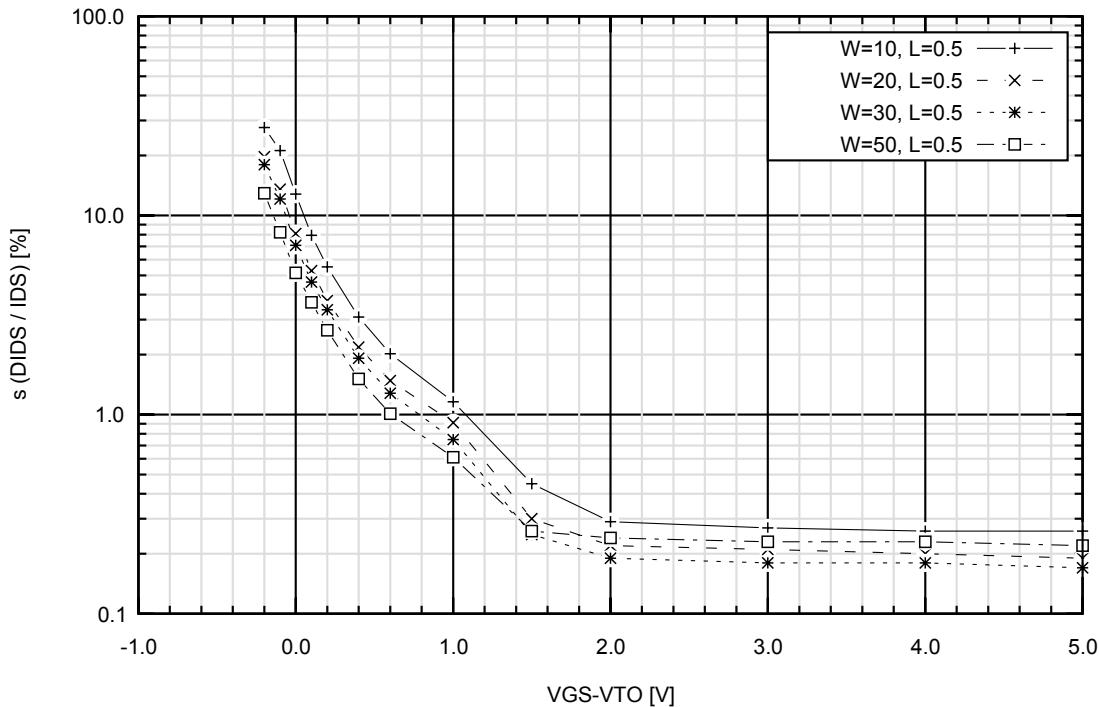


Figure 3.86 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_13

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	195	215	V
VDS	-40°C to 175°C	-215	-195	1.5	-	V
VDB	-40°C to 175°C	-215	-195	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-215	-195	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS _{1A13S}	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	224	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5 _{1A13S}	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=50μm, NF=2, WF=25μm	53	59.5	66	72.5	79	μA/μm
IDP _{1A13S}	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	92	-	-	μA/μm

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3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj1a_13→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A13S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=50µm, Pitch=15µm, NF=2, WF=25µm	-	-	2600	2860	-	mΩmm ²
RO _PHS1A13S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=50µm, NF=2, WF=25µm	138	156	173	190	208	kΩµm
TC _BDSPHS1A13S	breakdown temperature coefficient	-	-	0.15	-	-	V/K
TC _VTPHS1A13S	threshold voltage temperature coefficient @ L=0.5µm, W=50µm	-	-	2.1	-	-	mV/K
VTX PHS1A13S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=50µm, NF=2, WF=25µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj1a_13→ Matching parameters

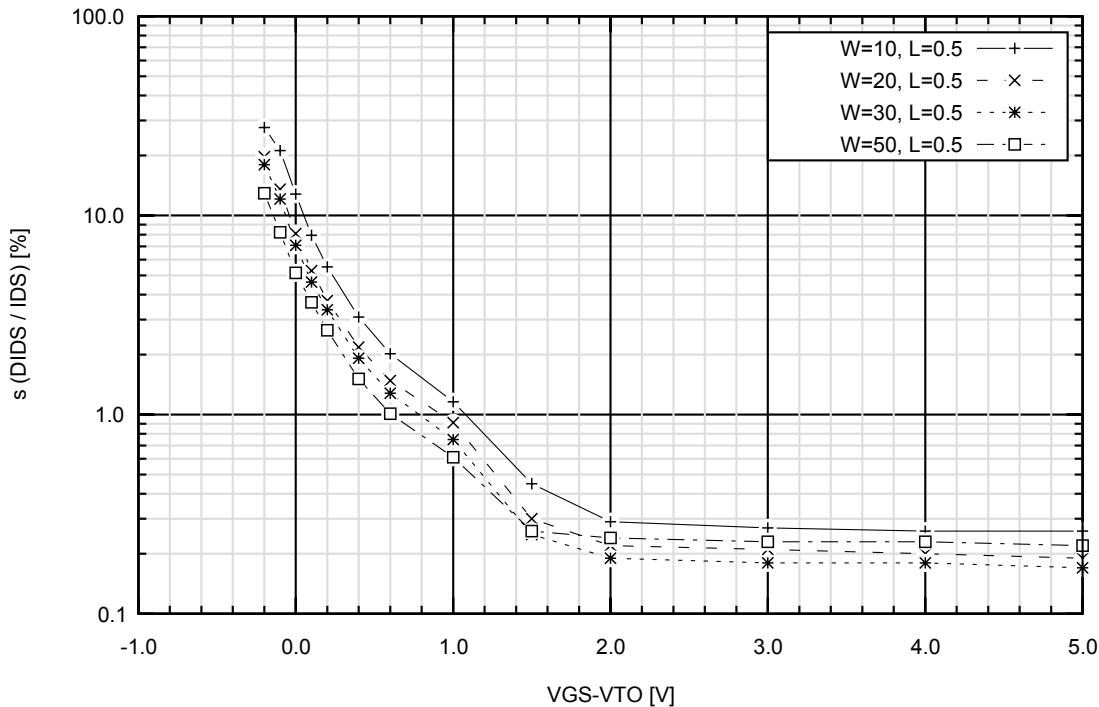


Figure 3.87 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_16

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	235	255	V
VDS	-40°C to 175°C	-255	-235	1.5	-	V
VDB	-40°C to 175°C	-255	-235	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-255	-235	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS _{PHS1A16S}	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	270	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5 _{PHS1A16S}	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=60μm, NF=2, WF=30μm	52	58.5	65	71.5	78	μA/μm
IDP _{PHS1A16S}	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=60μm, NF=2, WF=30μm	-	-	86	-	-	μA/μm

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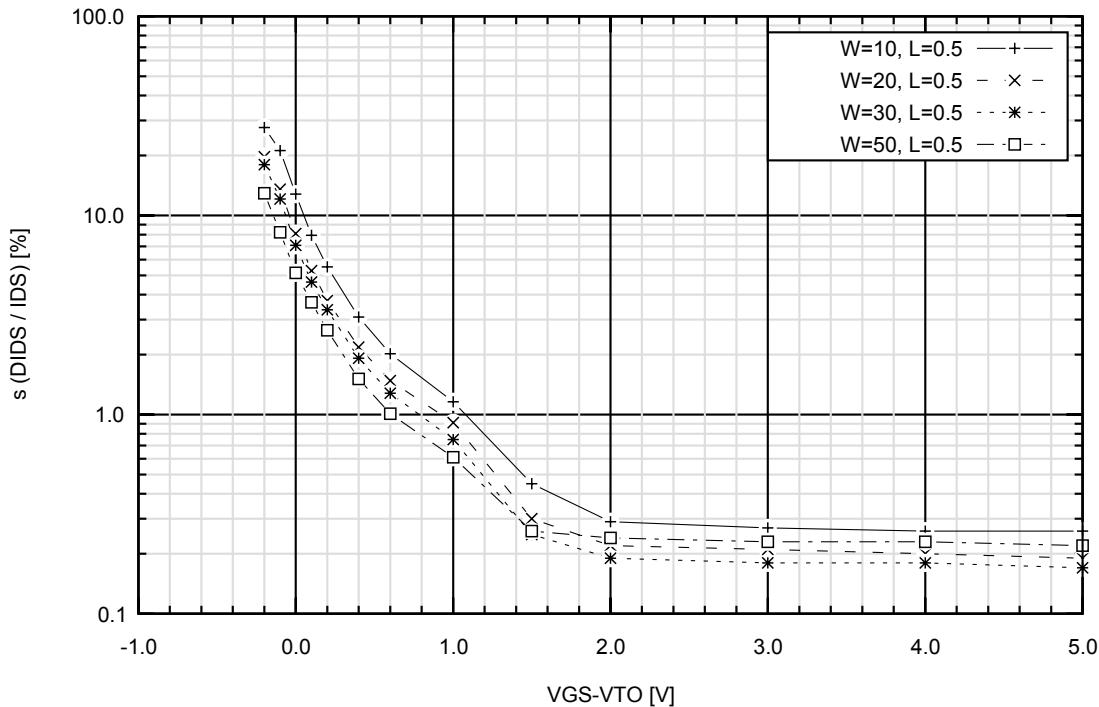
3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ phsj1a_16→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A16S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=60µm, Pitch=18µm, NF=2, WF=30µm	-	-	3720	4092	-	mΩmm ²
RO _PHS1A16S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=60µm, NF=2, WF=30µm	165	186	207	228	249	kΩµm
TC _BDSPHS1A16S	breakdown temperature coefficient	-	-	0.16	-	-	V/K
TC _VTPHS1A16S	threshold voltage temperature coefficient @ L=0.5µm, W=60µm	-	-	2.1	-	-	mV/K
VTX PHS1A16S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=60µm, NF=2, WF=30µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.36 SJHVM module → 3.36.1 Device parameters → phsj1a_16 → Matching parameters

**Figure 3.88** Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)**dfwnsj1b_8****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-155	-140	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-155	-140	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B8	reverse breakdown voltage @ L=8.5μm, W=38μm, NF=2, WF=19μm	161	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DNSJ1B8	leakage current @ VL=140V, T=27°C, W=38μm, NF=2, WF=19μm	-	-	1.7	-	-	pA
IL_DNSJ1B8HT	leakage current @ VL=140V, T=175°C, W=38μm, NF=2, WF=19μm	-	-	1.2	-	-	nA

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3. Parameters → 3.36 SJHVM module → 3.36.1 Device parameters → dfwnsj1b_8 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ1B8	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B8	forward voltage @ Idio=38µA, L=8.5µm, W=38µm, NF=2, WF=19µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-170	-155	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-170	-155	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B10	reverse breakdown voltage @ L=10µm, W=42µm, NF=2, WF=21µm	178	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1B10	leakage current @ VL=155V, T=27°C, W=42µm, NF=2, WF=21µm	-	-	0.6	-	-	pA
IL_DNSJ1B10HT	leakage current @ VL=155V, T=175°C, W=42µm, NF=2, WF=21µm	-	-	1.5	-	-	nA
TC_VDFDNSJ1B10	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B10	forward voltage @ Idio=42µA, L=10µm, W=42µm, NF=2, WF=21µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1a_13

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-215	-195	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-215	-195	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm



3. Parameters → 3.36 SJHVM module → 3.36.1 Device parameters → dfwnsj1a_13 → Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1A13	reverse breakdown voltage @ L=13µm, W=52µm, NF=2, WF=26µm	224	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DNSJ1A13	leakage current @ VL=195V, T=27°C, W=52µm, NF=2, WF=26µm	-	-	0.6	-	-	pA
IL_DNSJ1A13HT	leakage current @ VL=195V, T=175°C, W=52µm, NF=2, WF=26µm	-	-	1.9	-	-	nA
TC_VDFDNSJ1A13	forward voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VDFDNSJ1A13	forward voltage @ Idio=52µA, L=13µm, W=52µm, NF=2, WF=26µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1a_16

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-255	-235	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-255	-235	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1A16	reverse breakdown voltage @ L=16µm, W=62µm, NF=2, WF=31µm	270	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DNSJ1A16	leakage current @ VL=235V, T=27°C, W=62µm, NF=2, WF=31µm	-	-	0.8	-	-	pA
IL_DNSJ1A16HT	leakage current @ VL=235V, T=175°C, W=62µm, NF=2, WF=31µm	-	-	2.3	-	-	nA



3. Parameters → 3.36 SJHVM module→ 3.36.1 Device parameters→ dfwnsj1a_16→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ1A16	forward voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VDFDNSJ1A16	forward voltage @ Idio=62µA, L=16µm, W=62µm, NF=2, WF=31µm	0.74	0.76	0.78	0.8	0.82	V

3. Parameters → 3.37 SJHVU module

3.37 SJHVU module

3.37.1 Device parameters

nhsj1a_20

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-310	-290	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	290	310	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	290	310	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-310	-290	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1A20S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	320	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5NHS1A20S	saturation current @ VG=5V, VD=30V, L=0.5µm, W=80µm, NF=2, WF=40µm	80	90	100	110	120	µA/µm
IDPNHS1A20S	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=80µm, NF=2, WF=40µm	-	-	138	-	-	µA/µm
ROANHS1A20S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=80µm, Pitch=22.5µm, NF=2, WF=40µm	-	-	1800	1980	-	mΩmm ²
RO_NHS1A20S	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=80µm, NF=2, WF=40µm	64	72	80	88	96	kΩµm
TC_BDSNHS1A20S	breakdown temperature coefficient	-	-	0.3	-	-	V/K
TC_VTNHS1A20S	Threshold voltage temperature coefficient @ L=0.5µm, W=80µm	-	-	-2	-	-	mV/K
VT1NHS1A20	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80µm	-	-	262	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 Technical Report UHV Characteristics" at "my X-FAB"						
VTXNHS1A20S	extrapolated threshold voltage @ VD=0.1V, L=0.5µm, W=80µm, NF=2, WF=40µm	0.87	0.97	1.07	1.17	1.27	V

3. Parameters → 3.37 SJHVU module→ 3.37.1 Device parameters→ nhsj1a_20→ Matching parameters

Matching parameters

Name	Description	Typ	Unit
ABTNHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AIDNHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AIDNHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AIDNHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AIDNHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AIDNHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AIDNHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AIDNHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AIDNHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVTNHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLTNHSJ1B	transistor delta length	0	μm
DWTNHSJ1B	transistor delta width	0	μm

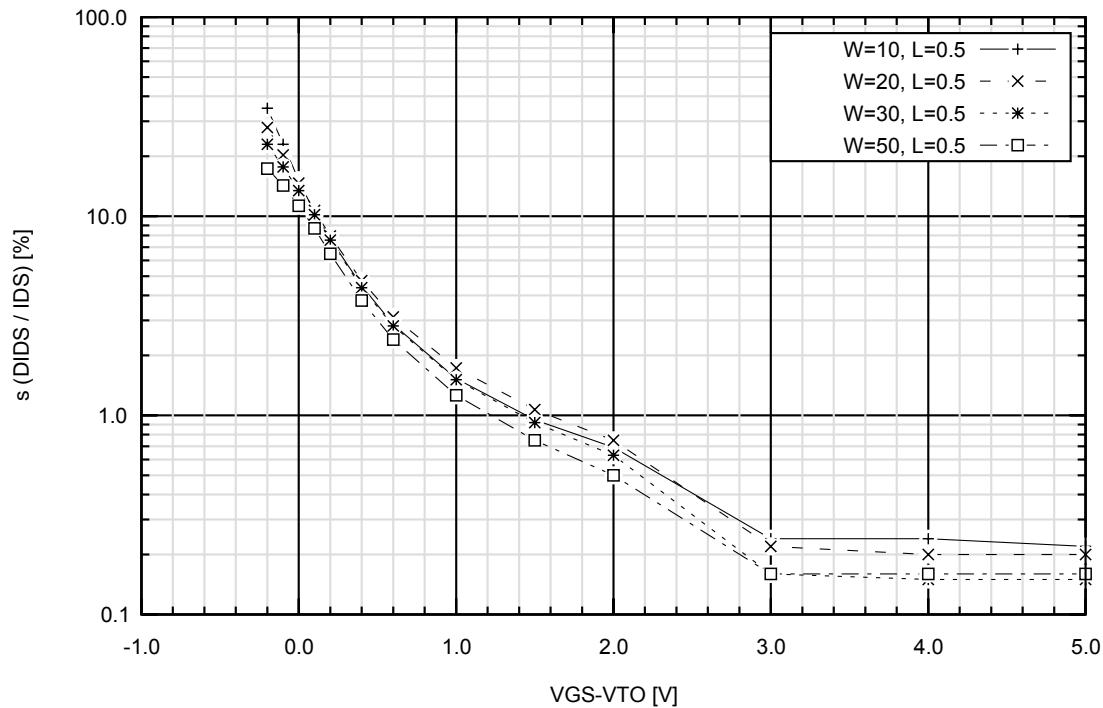


Figure 3.89 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1a_28

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-400	-375	5.5	7	V
VDS⁽¹⁾	-40°C to 175°C	-	-1.5	375	400	V
VDB⁽¹⁾	-40°C to 175°C	-	-1.5	375	400	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB⁽²⁾	-40°C to 175°C	-400	-375	1	1.5	V

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3. Parameters → 3.37 SJHVU module→ 3.37.1 Device parameters→ nhsj1a_28→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1A28S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	415	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5NHS1A28S	saturation current @ VG=5V, VD=50V, L=0.5µm, W=120µm, NF=2, WF=60µm	73	82	90	99	107	µA/µm
IDPNHS1A28S	pulsed drain current @ VG=5V, VD=50V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=120µm, NF=2, WF=60µm	-	-	131	-	-	µA/µm
ROANHS1A28S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=120µm, Pitch=30µm, NF=2, WF=60µm	-	-	3360	3690	-	mΩmm ²
RO_NHS1A28S	on resistance @ VG=5V, VD=0.1V, L=0.5µm, W=120µm, NF=2, WF=60µm	90	101	112	123	134	kΩµm
TC_BDSNHS1A28S	breakdown temperature coefficient	-	-	0.36	-	-	V/K
TC_VTNHS1A28S	Threshold voltage temperature coefficient @ L=0.5µm, W=120µm	-	-	-1.9	-	-	mV/K
VT1NHS1A28	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80µm	-	-	291	-	-	V
	Note: For detailed TLP I-V characteristics, refer to "XT018 Technical Report UHV Characteristics" at "my X-FAB"						
VTXNHS1A28S	extrapolated threshold voltage @ VD=0.1V, L=0.5µm, W=120µm, NF=2, WF=60µm	0.87	0.97	1.07	1.17	1.27	V

Matching parameters

Name	Description	Typ	Unit
ABTNHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%µm
AIDNHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%µm
AIDNHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%µm
AIDNHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%µm
AIDNHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%µm
AIDNHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%µm
AIDNHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%µm
AIDNHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%µm

3. Parameters → 3.37 SJHVU module→ 3.37.1 Device parameters→ nhsj1a_28→ Matching parameters

Name	Description	Typ	Unit
AIDNHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	% μ m
AVTNHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mV μ m
DLTNHSJ1B	transistor delta length	0	μ m
DWTNHSJ1B	transistor delta width	0	μ m

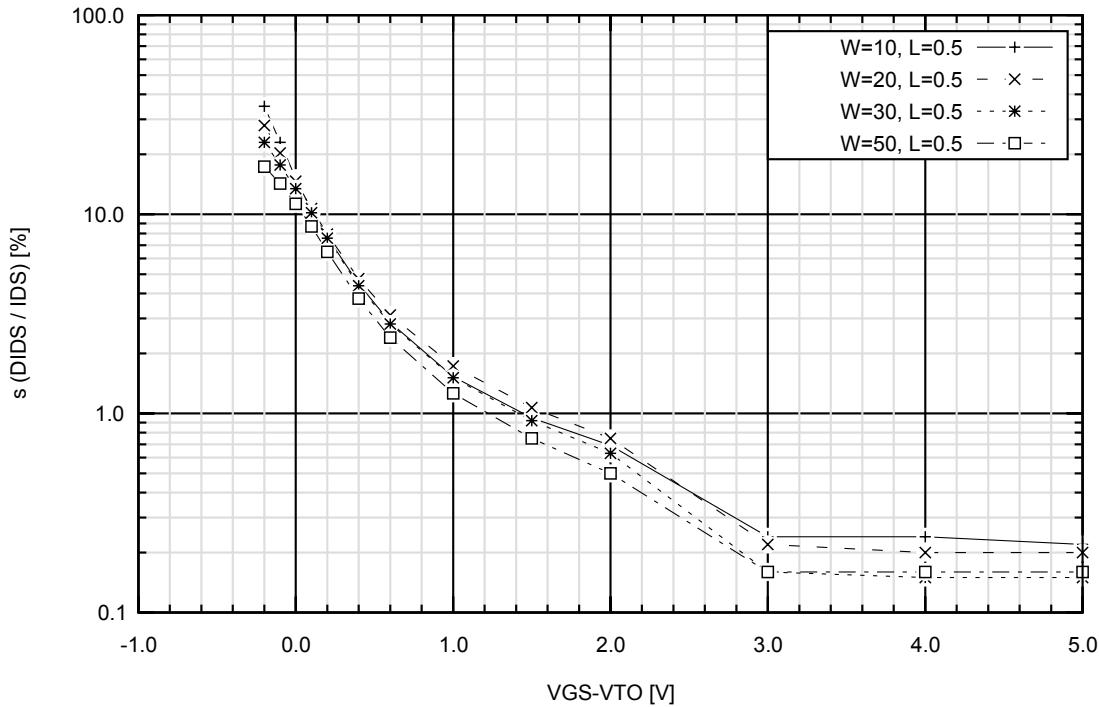


Figure 3.90 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_20

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	290	310	V
VDS	-40°C to 175°C	-310	-290	1.5	-	V
VDB	-40°C to 175°C	-310	-290	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-310	-290	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A20S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5 μ m	320	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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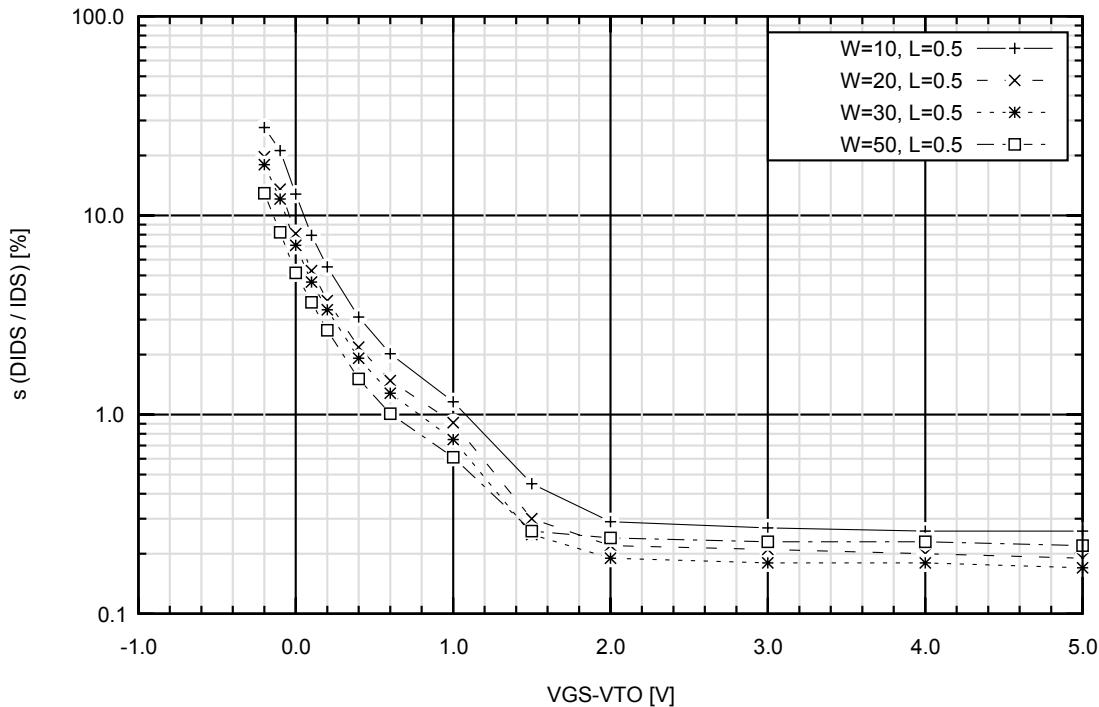
3. Parameters → 3.37 SJHVU module→ 3.37.1 Device parameters→ phsj1a_20→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5PHS1A20S	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=120μm, NF=2, WF=60μm	47	53	59	65	71	μA/μm
IDP PHS1A20S	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=120μm, NF=2, WF=60μm	-	-	74	-	-	μA/μm
ROA PHS1A20S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=120μm, Pitch=22.5μm, NF=2, WF=60μm	-	-	5890	6483	-	mΩmm ²
RO_PHS1A20S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=120μm, NF=2, WF=60μm	209	236	262	288	315	kΩμm
TC_BDSPHS1A20S	breakdown temperature coefficient	-	-	0.17	-	-	V/K
TC_VTPHS1A20S	threshold voltage temperature coefficient @ L=0.5μm, W=120μm	-	-	2.1	-	-	mV/K
VTXPHS1A20S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=120μm, NF=2, WF=60μm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%μm
AIDPHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%μm
AIDPHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%μm
AIDPHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%μm
AIDPHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%μm
AIDPHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%μm
AIDPHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%μm
AIDPHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%μm
AIDPHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%μm
AVTPHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVμm
DLTPHSJ1A	transistor delta length	0	μm
DWT PHSJ1A	transistor delta width	0	μm

3. Parameters → 3.37 SJHVU module→ 3.37.1 Device parameters→ phsj1a_20→ Matching parameters

**Figure 3.91** Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)**phsj1a_31****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	375	400	V
VDS	-40°C to 175°C	-400	-375	1.5	-	V
VDB	-40°C to 175°C	-400	-375	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-400	-375	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS _{1A31S}	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	415	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5 _{1A31S}	saturation current @ VG=-5V, VD=-100V, L=0.5μm, W=160μm, NF=2, WF=80μm	50	55.5	61	66.5	72	μA/μm
IDP _{1A31S}	pulsed drain current @ VG=-5V, VD=-100V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=160μm, NF=2, WF=80μm	-	-	94	-	-	μA/μm

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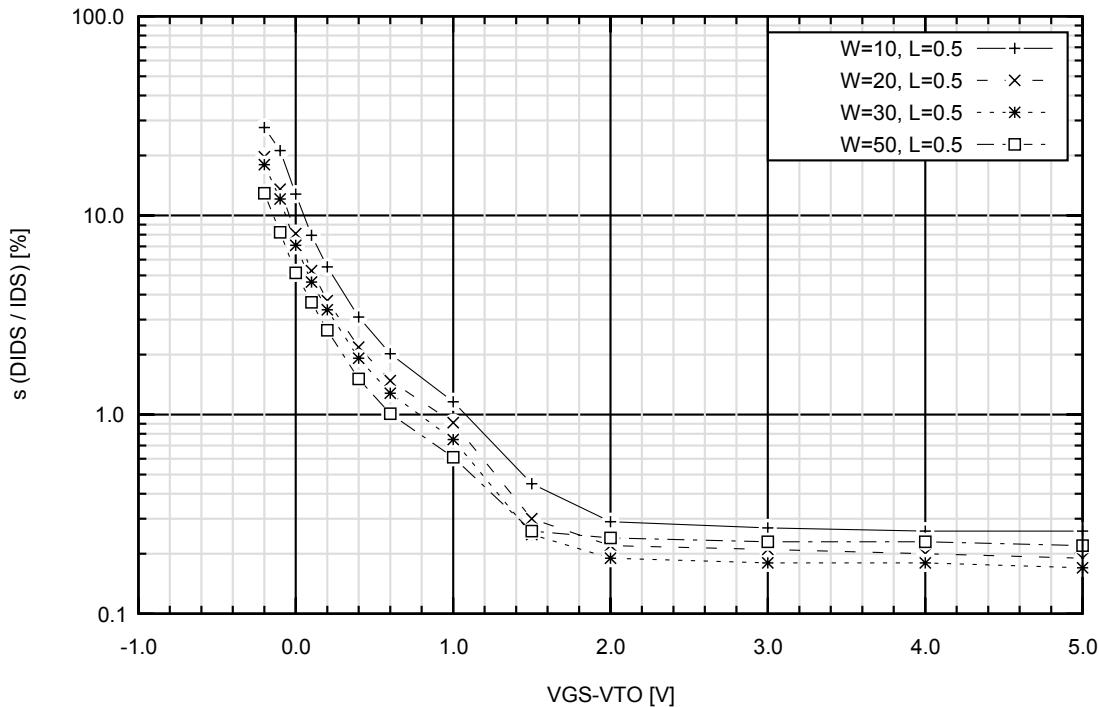
3. Parameters → 3.37 SJHVU module→ 3.37.1 Device parameters→ phsj1a_31→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA_PHS1A31S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=160µm, Pitch=33µm, NF=2, WF=80µm	-	-	11682	12903	-	mΩmm ²
RO_PHS1A31S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=160µm, NF=2, WF=80µm	280	317	354	391	428	kΩµm
TC_BDSPHS1A31S	breakdown temperature coefficient	-	-	0.19	-	-	V/K
TC_VTPHS1A31S	threshold voltage temperature coefficient @ L=0.5µm, W=160µm	-	-	2.2	-	-	mV/K
VTX_PHS1A31S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=160µm, NF=2, WF=80µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT_PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID_PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID_PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID_PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID_PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID_PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID_PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID_PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID_PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT_PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT_PHSJ1A	transistor delta length	0	µm
DWT_PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.37 SJHVU module → 3.37.1 Device parameters → phsj1a_31 → Matching parameters

**Figure 3.92** Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)**dfwnsj1a_20****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-310	-290	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-310	-290	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1A20	reverse breakdown voltage @ L=20.5μm, W=82μm, NF=2, WF=41μm	320	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1A20	leakage current @ VL=290V, T=27°C, W=82μm, NF=2, WF=41μm	-	-	0.9	-	-	pA
IL_DNSJ1A20HT	leakage current @ VL=290V, T=175°C, W=82μm, NF=2, WF=41μm	-	-	3	-	-	nA

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3. Parameters → 3.37 SJHVU module→ 3.37.1 Device parameters→ dfwnsj1a_20→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ1A20	forward voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VDFDNSJ1A20	forward voltage @ Idio=82µA, L=20.5µm, W=82µm, NF=2, WF=41µm	0.75	0.77	0.79	0.81	0.83	V

dfwnsj1a_28

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-400	-375	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-400	-375	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1A28	reverse breakdown voltage @ L=28µm, W=122µm, NF=2, WF=61µm	415	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1A28	leakage current @ VL=375V, T=27°C, W=122µm, NF=2, WF=61µm	-	-	1.1	-	-	pA
IL_DNSJ1A28HT	leakage current @ VL=375V, T=175°C, W=122µm, NF=2, WF=61µm	-	-	3.8	-	-	nA
TC_VDFDNSJ1A28	forward voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VDFDNSJ1A28	forward voltage @ Idio=122µA, L=28µm, W=122µm, NF=2, WF=61µm	0.75	0.77	0.79	0.81	0.83	V

dhw4d

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-395	-360	0	0.5	V

3. Parameters → 3.37 SJHVU module→ 3.37.1 Device parameters→ dhw4d→ Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW4D	handle wafer diode breakdown voltage @ Irev=1µA, L=80µm, W=80µm	414	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CPA_TUBDHW4D	tub-handle wafer area capacitance	-	-	0.00161	-	-	fF/µm ²
IL_DHW4D	handle wafer diode leakage @ VL=360V, T=27°C, L=80µm, W=80µm	-	-	0.41	-	-	fA/µm ²
IL_DHW4DHT	leakage current @ VL=360V, T=175°C, L=80µm, W=80µm	-	-	163	-	-	pA/µm ²

dhw5d

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-460	-420	0	0.5	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DHW5D	handle wafer diode breakdown voltage @ Irev=1µA, L=80µm, W=80µm	483	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CPA_TUBDHW5D	tub-handle wafer area capacitance	-	-	0.00156	-	-	fF/µm ²
IL_DHW5D	handle wafer diode leakage @ VL=420V, T=27°C, L=80µm, W=80µm	-	-	0.53	-	-	fA/µm ²
IL_DHW5DHT	leakage current @ VL=420V, T=175°C, L=80µm, W=80µm	-	-	222	-	-	pA/µm ²

3. Parameters → 3.38 SJ1XN module

3.38 SJ1XN module

3.38.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_SJ1XN	SJ1XN junction depth	1.8	µm

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSNSJ1XN	SJ1XN n-type sheet resistance	2.3	kΩ/□
RSSPSJ1XN	SJ1XN p-type sheet resistance	16.5	kΩ/□

3.38.2 Device parameters

nhsj1b_2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-50	-45	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	45	50	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	45	50	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-50	-45	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B2S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	52	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5NHS1B2S	saturation current @ VG=5V, VD=15V, L=0.5µm, W=20µm, NF=2, WF=10µm	164	185	205	225	246	µA/µm
IDPNHS1B2S	pulsed drain current @ VG=5V, VD=15V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=20µm, NF=2, WF=10µm	-	-	248	-	-	µA/µm

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3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1b_2→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA NHS1B2S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, Pitch=4.25μm, NF=2, WF=10μm	-	-	45	49.5	-	mΩmm ²
RO _NHS1B2S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	8.5	9.5	10.6	11.7	12.7	kΩμm
TC _BDSNHS1B2S	breakdown temperature coefficient	-	-	0.04	-	-	V/K
TC _VTNHS1B2S	Threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	-1.7	-	-	mV/K
VT1 NHS1B2	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	63	-	-	V
Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"							
VTX NHS1B2S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	0.78	0.88	0.98	1.08	1.18	V

Matching parameters

Name	Description	Typ	Unit
ABT NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT NHSJ1B	transistor delta length	0	μm
DWT NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1b_2 → Matching parameters

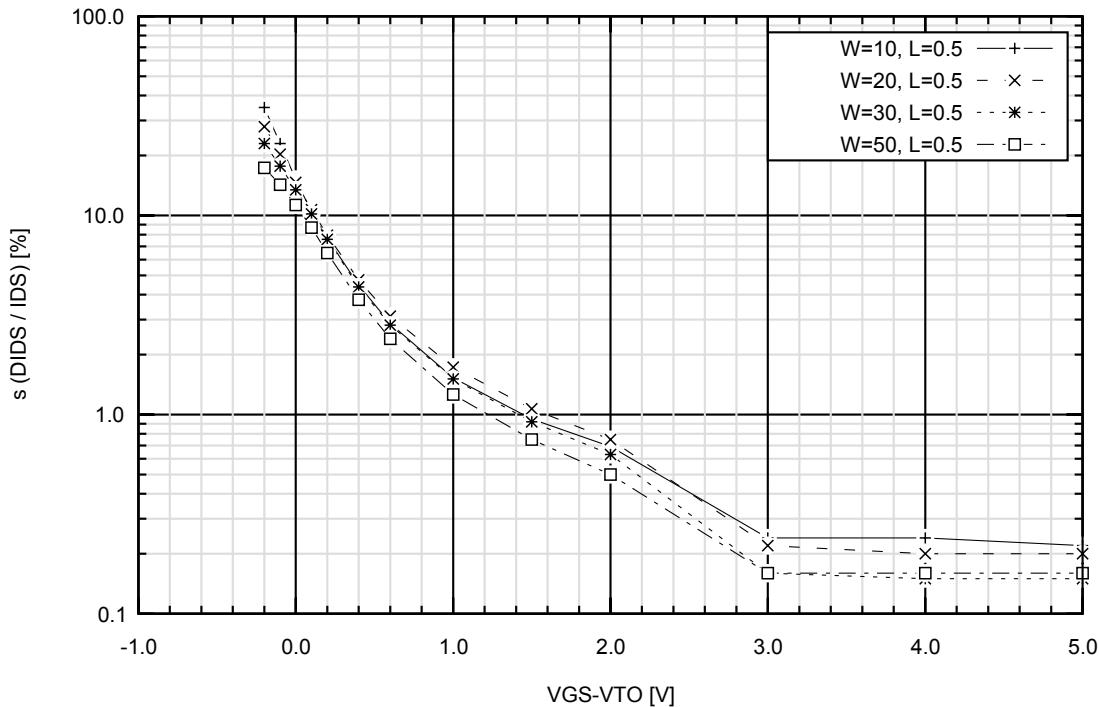


Figure 3.93 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1b_4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-80	-72	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	72	80	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	72	80	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-80	-72	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B4S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	83	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1b_4→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1B4S	saturation current @ VG=5V, VD=15V, L=0.5μm, W=20μm, NF=2, WF=10μm	136	153	170	187	204	μA/μm
IDP_NHS1B4S	pulsed drain current @ VG=5V, VD=15V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	205	-	-	μA/μm
ROA_NHS1B4S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, Pitch=5.75μm, NF=2, WF=10μm	-	-	95	104.5	-	mΩmm ²
RO_NHS1B4S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	13.2	14.9	16.5	18.1	19.8	kΩμm
TC_BDSNHS1B4S	breakdown temperature coefficient	-	-	0.08	-	-	V/K
TC_VTNHS1B4S	Threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	-1.8	-	-	mV/K
VT1NHS1B4	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	94	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1B4S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	0.79	0.89	0.99	1.09	1.19	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

Note: Matching data are valid for L=0.5 μm. Transistors with channel lengths > 0.5 μm will exhibit greater mismatch of parameters. More information available on request.

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1b_4 → Matching parameters

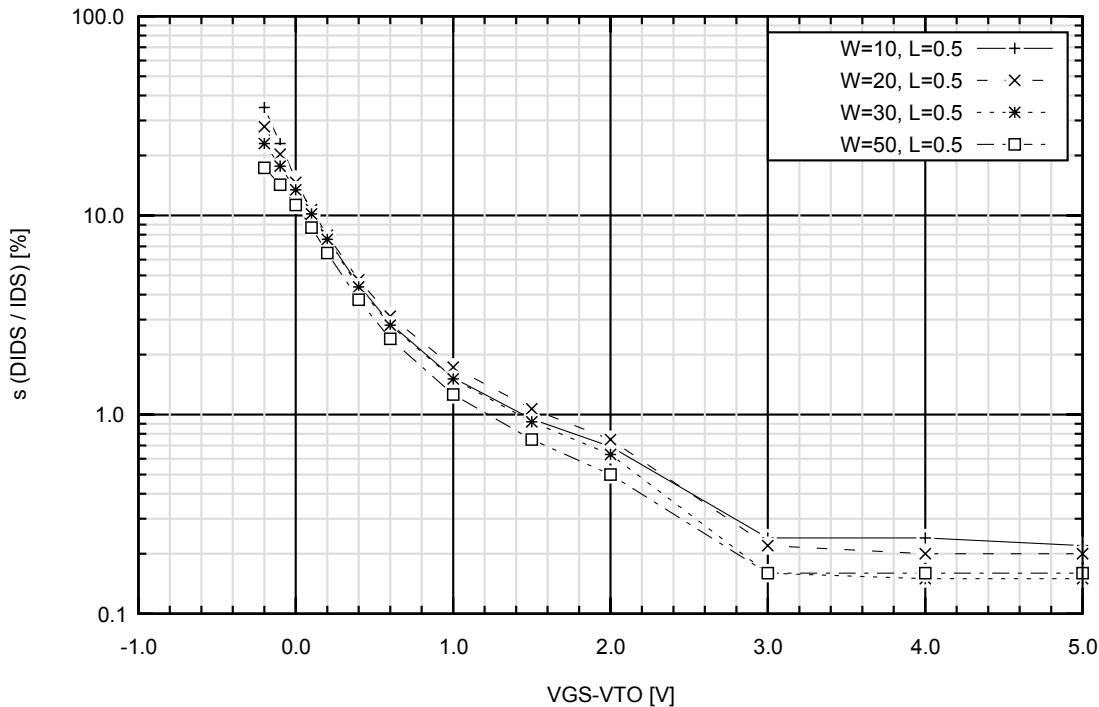


Figure 3.94 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1b_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-105	-95	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	95	105	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	95	105	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-105	-95	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B5S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	109	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							⇒

3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1b_5→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1B5S	saturation current @ VG=5V, VD=20V, L=0.5μm, W=20μm, NF=2, WF=10μm	128	144	160	176	192	μA/μm
IDP_NHS1B5S	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	216	-	-	μA/μm
ROA_NHS1B5S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, Pitch=7.25μm, NF=2, WF=10μm	-	-	160	176	-	mΩmm ²
RO_NHS1B5S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	18	20	22	24	26	kΩμm
TC_BDSNHS1B5S	breakdown temperature coefficient	-	-	0.1	-	-	V/K
TC_VTNHS1B5S	Threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	-1.8	-	-	mV/K
VT1NHS1B5	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	122	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1B5S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	0.8	0.9	1	1.1	1.2	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1b_5 → Matching parameters

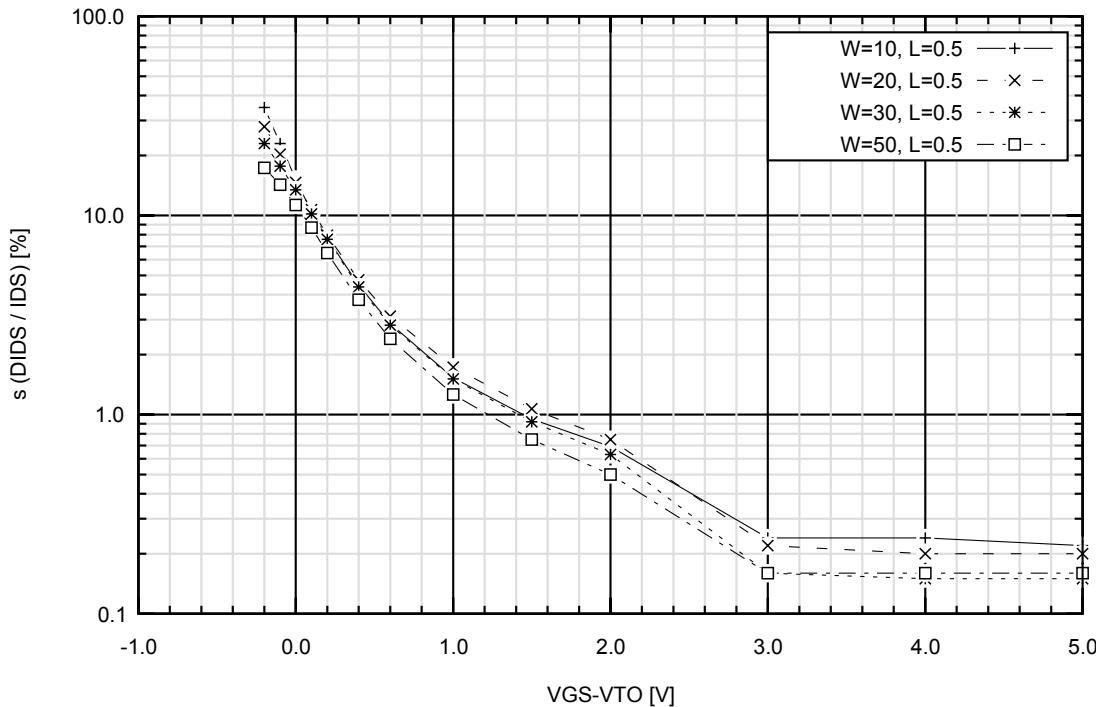


Figure 3.95 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1b_7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-125	-115	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	115	125	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	115	125	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-125	-115	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B7S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	132	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1b_7→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1B7S	saturation current @ VG=5V, VD=20V, L=0.5μm, W=30μm, NF=2, WF=15μm	112	126	140	154	168	μA/μm
IDP_NHS1B7S	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=30μm, NF=2, WF=15μm	-	-	200	-	-	μA/μm
ROA_NHS1B7S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=30μm, Pitch=8.75μm, NF=2, WF=15μm	-	-	250	275	-	mΩmm ²
RO_NHS1B7S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=30μm, NF=2, WF=15μm	22.9	25.7	28.6	31.5	34.3	kΩμm
TC_BDSNHS1B7S	breakdown temperature coefficient	-	-	0.12	-	-	V/K
TC_VTNHS1B7S	Threshold voltage temperature coefficient @ L=0.5μm, W=30μm	-	-	-1.9	-	-	mV/K
VT1NHS1B7	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	148	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1B7S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=30μm, NF=2, WF=15μm	0.81	0.91	1.01	1.11	1.21	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1b_7 → Matching parameters

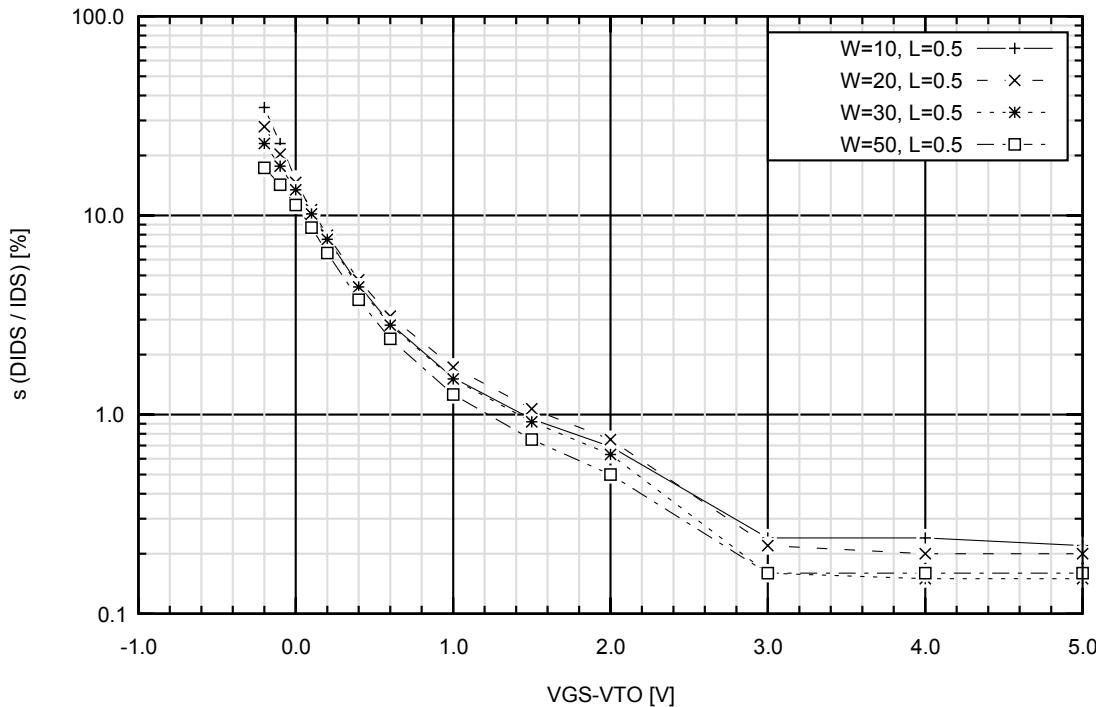


Figure 3.96 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1b_8

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-155	-140	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	140	155	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	140	155	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-155	-140	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B8S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	161	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1b_8→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1B8S	saturation current @ VG=5V, VD=20V, L=0.5μm, W=36μm, NF=2, WF=18μm	104	117	130	143	156	μA/μm
IDP_NHS1B8S	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=36μm, NF=2, WF=18μm	-	-	184	-	-	μA/μm
ROA_NHS1B8S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=36μm, Pitch=10.25μm, NF=2, WF=18μm	-	-	360	396	-	mΩmm ²
RO_NHS1B8S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=36μm, NF=2, WF=18μm	28	32	35	38	42	kΩμm
TC_BDSNHS1B8S	breakdown temperature coefficient	-	-	0.14	-	-	V/K
TC_VTNHS1B8S	Threshold voltage temperature coefficient @ L=0.5μm, W=36μm	-	-	-1.9	-	-	mV/K
VT1NHS1B8	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	172	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1B8S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=36μm, NF=2, WF=18μm	0.82	0.92	1.02	1.12	1.22	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1b_8 → Matching parameters

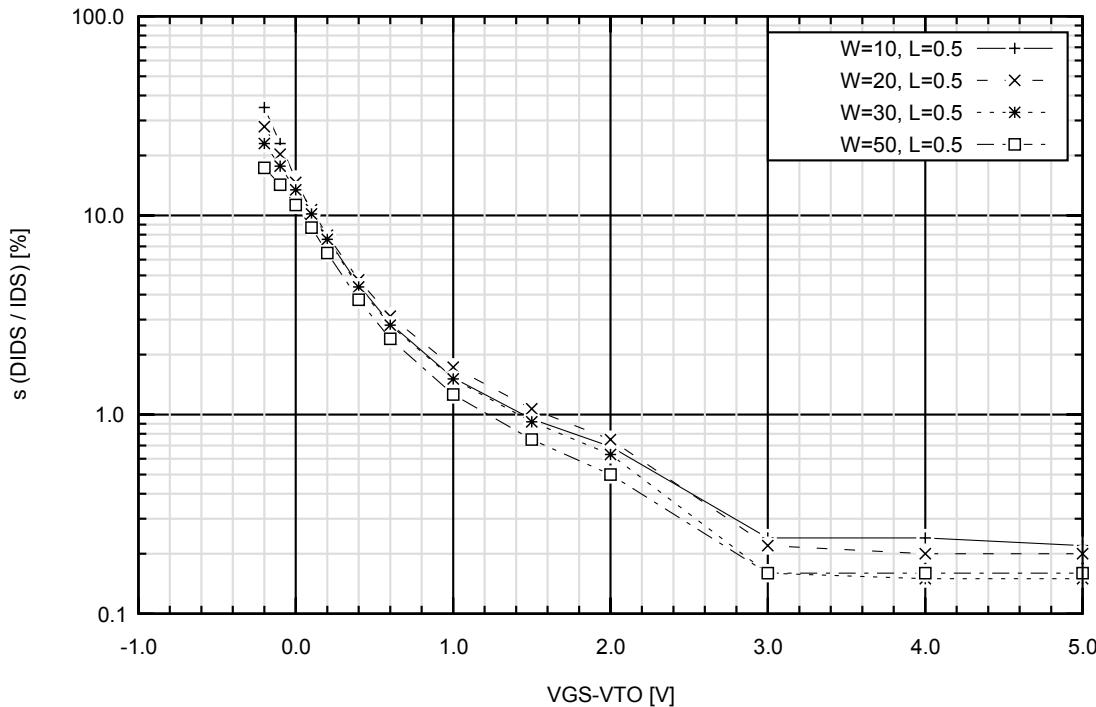


Figure 3.97 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1b_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-170	-155	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	155	170	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	155	170	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-170	-155	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1B10S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	178	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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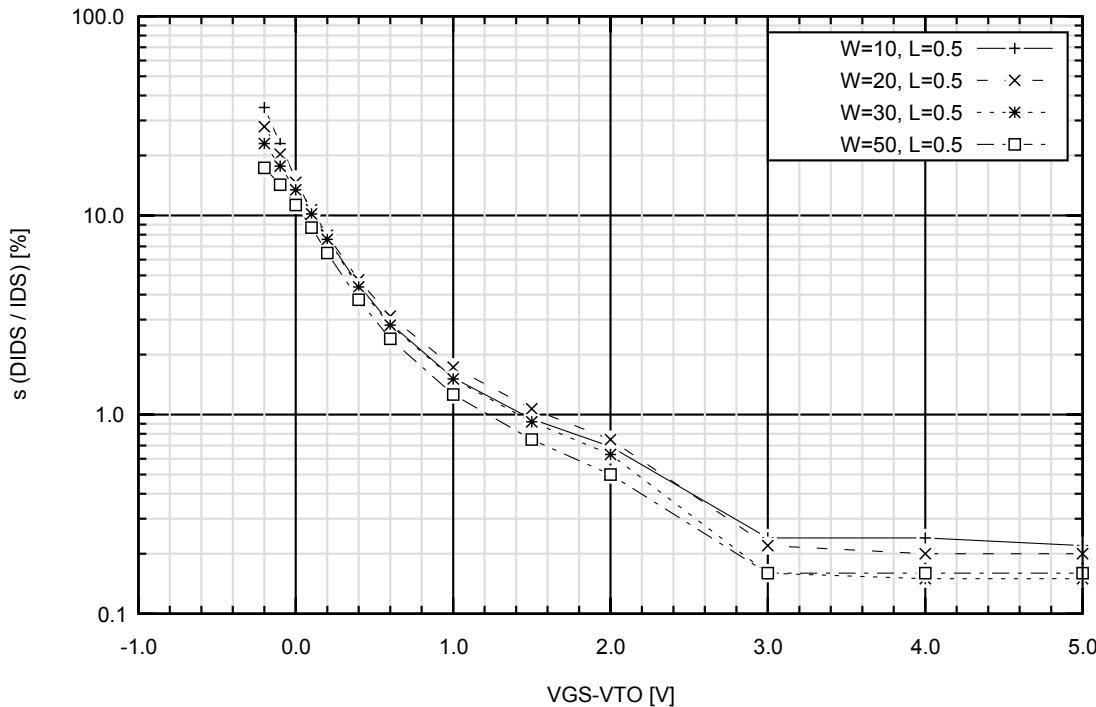
3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1b_10→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1B10S	saturation current @ VG=5V, VD=20V, L=0.5μm, W=40μm, NF=2, WF=20μm	100	113	125	137	150	μA/μm
IDP_NHS1B10S	pulsed drain current @ VG=5V, VD=20V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=40μm, NF=2, WF=20μm	-	-	173	-	-	μA/μm
ROA_NHS1B10S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=40μm, Pitch=11.75μm, NF=2, WF=20μm	-	-	480	528	-	mΩmm ²
RO_NHS1B10S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=40μm, NF=2, WF=20μm	32.8	36.9	40.9	44.9	49	kΩμm
TC_BDSNHS1B10S	breakdown temperature coefficient	-	-	0.16	-	-	V/K
TC_VTNHS1B10S	Threshold voltage temperature coefficient @ L=0.5μm, W=40μm	-	-	-1.9	-	-	mV/K
VT1NHS1B10	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	192	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1B10S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=40μm, NF=2, WF=20μm	0.83	0.93	1.03	1.13	1.23	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1b_10 → Matching parameters

**Figure 3.98** Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)**nhsj1a_13****Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-215	-195	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	195	215	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	195	215	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-215	-195	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1A13S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	224	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1a_13→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1A13S	saturation current @ VG=5V, VD=30V, L=0.5μm, W=50μm, NF=2, WF=25μm	92	104	115	126	138	μA/μm
IDP_NHS1A13S	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	163	-	-	μA/μm
ROA_NHS1A13S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, Pitch=15μm, NF=2, WF=25μm	-	-	770	847	-	mΩmm ²
RO_NHS1A13S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	41	46	51	56	61	kΩμm
TC_BDSNHS1A13S	breakdown temperature coefficient	-	-	0.2	-	-	V/K
TC_VTNHS1A13S	Threshold voltage temperature coefficient @ L=0.5μm, W=50μm	-	-	-1.9	-	-	mV/K
VT1NHS1A13	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	214	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1A13S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=50μm, NF=2, WF=25μm	0.87	0.97	1.07	1.17	1.27	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1a_13 → Matching parameters

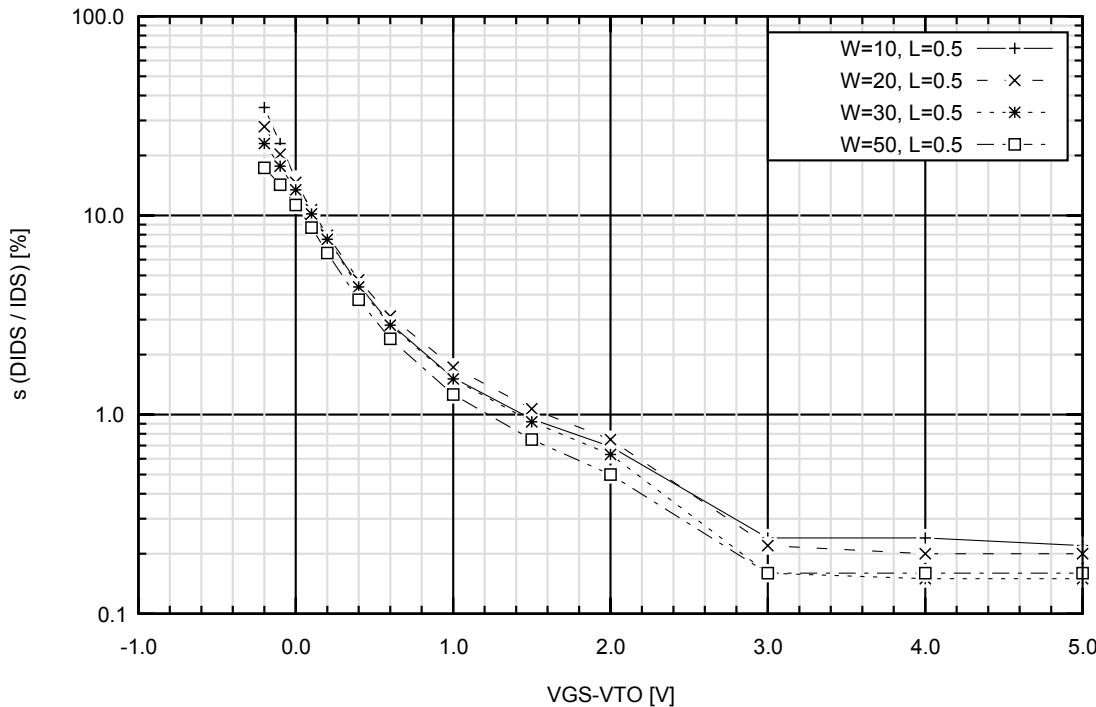


Figure 3.99 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1a_16

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-255	-235	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	235	255	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	235	255	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-255	-235	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1A16S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	270	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1a_16→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1A16S	saturation current @ VG=5V, VD=30V, L=0.5μm, W=60μm, NF=2, WF=30μm	88	99	110	121	132	μA/μm
IDP_NHS1A16S	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=60μm, NF=2, WF=30μm	-	-	157	-	-	μA/μm
ROA_NHS1A16S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=60μm, Pitch=18μm, NF=2, WF=30μm	-	-	1150	1265	-	mΩmm ²
RO_NHS1A16S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=60μm, NF=2, WF=30μm	51	58	64	70	77	kΩμm
TC_BDSNHS1A16S	breakdown temperature coefficient	-	-	0.24	-	-	V/K
TC_VTNHS1A16S	Threshold voltage temperature coefficient @ L=0.5μm, W=60μm	-	-	-2	-	-	mV/K
VT1NHS1A16	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	236	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1A16S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=60μm, NF=2, WF=30μm	0.87	0.97	1.07	1.17	1.27	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1a_16 → Matching parameters

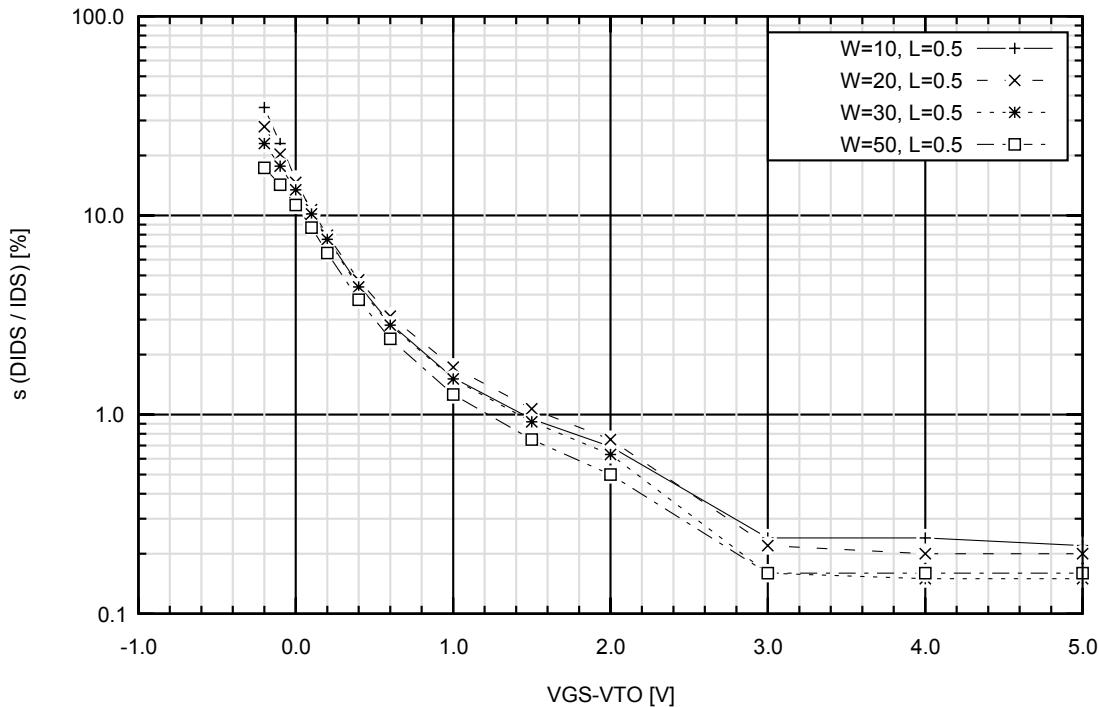


Figure 3.100 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1a_20

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-310	-290	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	290	310	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	290	310	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-310	-290	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1A20S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	320	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1a_20→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1A20S	saturation current @ VG=5V, VD=30V, L=0.5μm, W=80μm, NF=2, WF=40μm	80	90	100	110	120	μA/μm
IDP_NHS1A20S	pulsed drain current @ VG=5V, VD=30V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=80μm, NF=2, WF=40μm	-	-	138	-	-	μA/μm
ROA_NHS1A20S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=80μm, Pitch=22.5μm, NF=2, WF=40μm	-	-	1800	1980	-	mΩmm ²
RO_NHS1A20S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=80μm, NF=2, WF=40μm	64	72	80	88	96	kΩμm
TC_BDSNHS1A20S	breakdown temperature coefficient	-	-	0.3	-	-	V/K
TC_VTNHS1A20S	Threshold voltage temperature coefficient @ L=0.5μm, W=80μm	-	-	-2	-	-	mV/K
VT1NHS1A20	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	262	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1A20S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=80μm, NF=2, WF=40μm	0.87	0.97	1.07	1.17	1.27	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1a_20 → Matching parameters

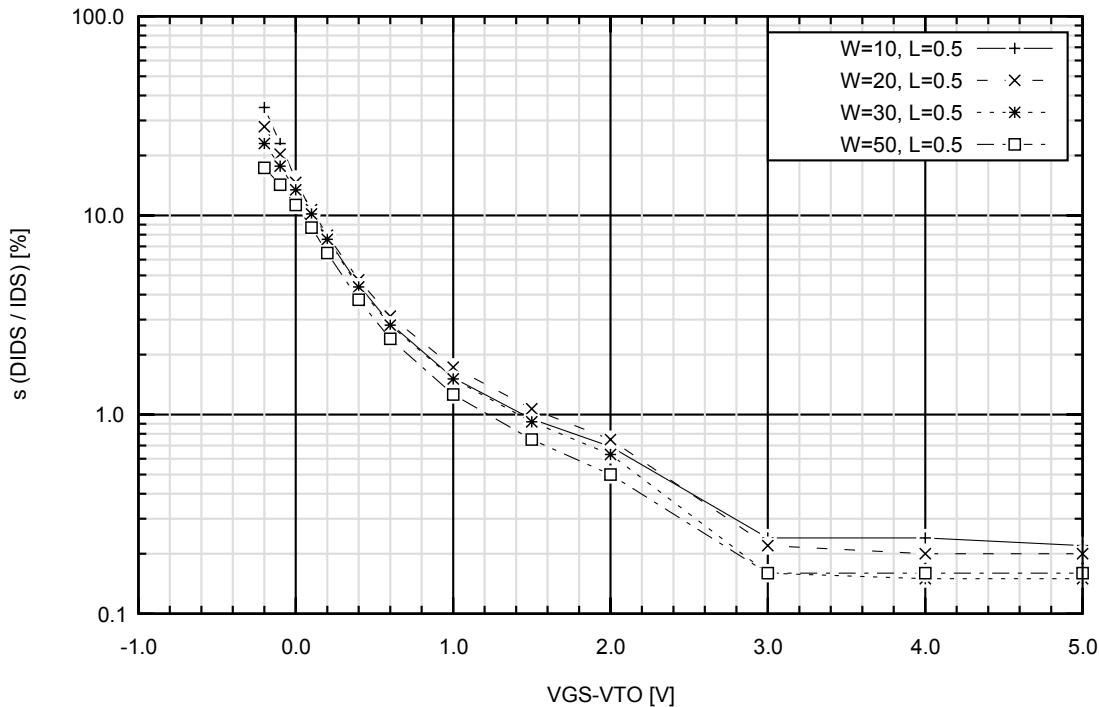


Figure 3.101 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

nhsj1a_28

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-400	-375	5.5	7	V
VDS ⁽¹⁾	-40°C to 175°C	-	-1.5	375	400	V
VDB ⁽¹⁾	-40°C to 175°C	-	-1.5	375	400	V
VD-HW	-40°C to 175°C	-	-1.5	400	440	V
VD-NB ⁽²⁾	-40°C to 175°C	-400	-375	1	1.5	V
If ⁽³⁾⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽⁴⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 This forward current is allowed only for transistor's drain bulk junction

Note 4 Pulsed operation with negligible self-heating (<=100ns)

Note: The node B (BULK) is: PWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSNHS1A28S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	415	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							

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3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ nhsj1a_28→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ID5NHS1A28S	saturation current @ VG=5V, VD=50V, L=0.5μm, W=120μm, NF=2, WF=60μm	73	82	90	99	107	μA/μm
IDP_NHS1A28S	pulsed drain current @ VG=5V, VD=50V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=120μm, NF=2, WF=60μm	-	-	131	-	-	μA/μm
ROA_NHS1A28S	area specific on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=120μm, Pitch=30μm, NF=2, WF=60μm	-	-	3360	3690	-	mΩmm ²
RO_NHS1A28S	on resistance @ VG=5V, VD=0.1V, L=0.5μm, W=120μm, NF=2, WF=60μm	90	101	112	123	134	kΩμm
TC_BDSNHS1A28S	breakdown temperature coefficient	-	-	0.36	-	-	V/K
TC_VTNHS1A28S	Threshold voltage temperature coefficient @ L=0.5μm, W=120μm	-	-	-1.9	-	-	mV/K
VT1NHS1A28	snap-back trigger voltage @ VGS=5V, Ngates=16, WF=80μm	-	-	291	-	-	V
	Note: For detailed TLP I-V characteristics, refer to " XT018 Technical Report UHV Characteristics " at "my X-FAB"						
VTXNHS1A28S	extrapolated threshold voltage @ VD=0.1V, L=0.5μm, W=120μm, NF=2, WF=60μm	0.87	0.97	1.07	1.17	1.27	V

Matching parameters

Name	Description	Typ	Unit
ABT_NHSJ1B	pelgrom coefficient gain factor mismatch	4.48	%μm
AID_NHSJ1B00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	42.18	%μm
AID_NHSJ1B02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	22.63	%μm
AID_NHSJ1B04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	13.24	%μm
AID_NHSJ1B06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	8.53	%μm
AID_NHSJ1B10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	4.61	%μm
AID_NHSJ1B20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	1.99	%μm
AID_NHSJ1B30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.61	%μm
AID_NHSJ1B50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.57	%μm
AVT_NHSJ1B	pelgrom coefficient threshold voltage mismatch	27.44	mVμm
DLT_NHSJ1B	transistor delta length	0	μm
DWT_NHSJ1B	transistor delta width	0	μm

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → nhsj1a_28 → Matching parameters

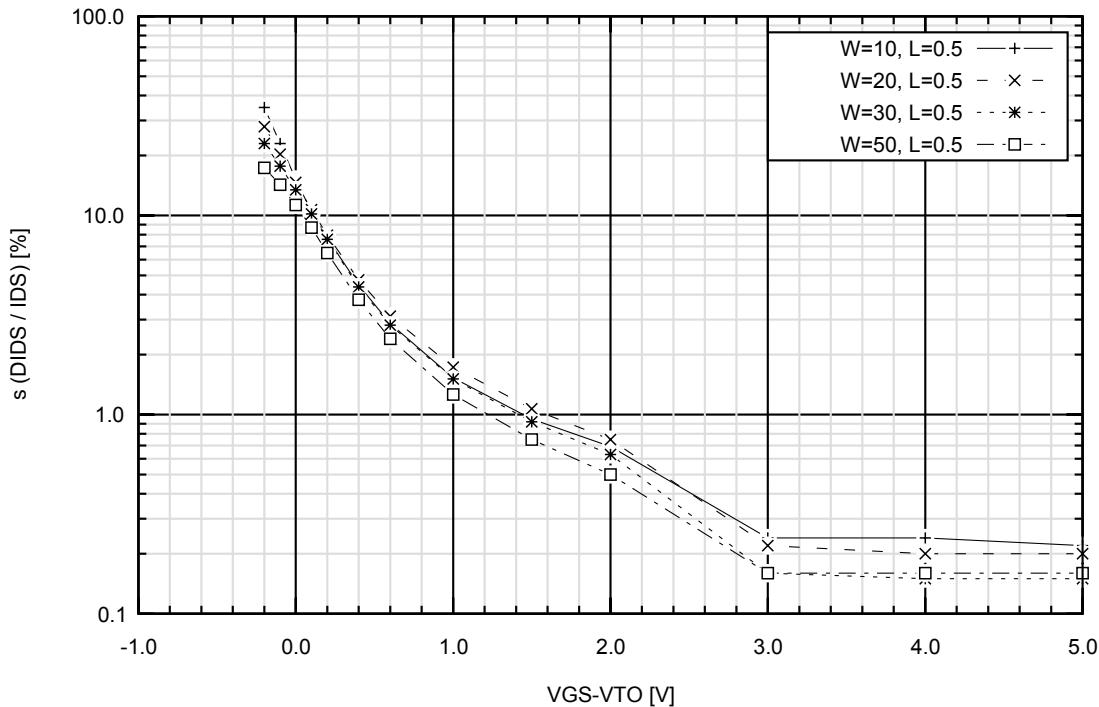


Figure 3.102 Device nhsj1a/b: drain current matching vs. VGS-VTO (typical values, drawn W and L)

dfwnsj1b_2

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-50	-45	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-50	-45	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/μm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B2	reverse breakdown voltage @ L=2.5μm, W=22μm, NF=2, WF=11μm	52	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1B2	leakage current @ VL=45V, T=27°C, W=22μm, NF=2, WF=11μm	-	-	0.09	-	-	pA
IL_DNSJ1B2HT	leakage current @ VL=45V, T=175°C, W=22μm, NF=2, WF=11μm	-	-	0.33	-	-	nA

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3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → dfwnsj1b_2 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ1B2	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B2	forward voltage @ Idio=22µA, L=2.5µm, W=22µm, NF=2, WF=11µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-80	-72	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-80	-72	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B4	reverse breakdown voltage @ L=4µm, W=22µm, NF=2, WF=11µm	83	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1B4	leakage current @ VL=72V, T=27°C, W=22µm, NF=2, WF=11µm	-	-	0.17	-	-	pA
IL_DNSJ1B4HT	leakage current @ VL=72V, T=175°C, W=22µm, NF=2, WF=11µm	-	-	0.47	-	-	nA
TC_VDFDNSJ1B4	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B4	forward voltage @ Idio=22µA, L=4µm, W=22µm, NF=2, WF=11µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-105	-95	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-105	-95	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm



3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ dfwnsj1b_5→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B5	reverse breakdown voltage @ L=5.5µm, W=22µm, NF=2, WF=11µm	109	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DNSJ1B5	leakage current @ VL=95V, T=27°C, W=22µm, NF=2, WF=11µm	-	-	0.33	-	-	pA
IL_DNSJ1B5HT	leakage current @ VL=95V, T=175°C, W=22µm, NF=2, WF=11µm	-	-	0.78	-	-	nA
TC_VDFDNSJ1B5	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B5	forward voltage @ Idio=22µA, L=5.5µm, W=22µm, NF=2, WF=11µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_7**Operating conditions**

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-125	-115	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-125	-115	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B7	reverse breakdown voltage @ L=7µm, W=32µm, NF=2, WF=16µm	132	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL_DNSJ1B7	leakage current @ VL=115V, T=27°C, W=32µm, NF=2, WF=16µm	-	-	0.4	-	-	pA
IL_DNSJ1B7HT	leakage current @ VL=115V, T=175°C, W=32µm, NF=2, WF=16µm	-	-	0.97	-	-	nA

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → dfwnsj1b_7 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ1B7	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B7	forward voltage @ Idio=32µA, L=7µm, W=32µm, NF=2, WF=16µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_8

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-155	-140	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-155	-140	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1B8	reverse breakdown voltage @ L=8.5µm, W=38µm, NF=2, WF=19µm	161	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1B8	leakage current @ VL=140V, T=27°C, W=38µm, NF=2, WF=19µm	-	-	1.7	-	-	pA
IL_DNSJ1B8HT	leakage current @ VL=140V, T=175°C, W=38µm, NF=2, WF=19µm	-	-	1.2	-	-	nA
TC_VDFDNSJ1B8	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDFDNSJ1B8	forward voltage @ Idio=38µA, L=8.5µm, W=38µm, NF=2, WF=19µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1b_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-170	-155	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-170	-155	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm



3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → dfwnsj1b_10 → Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
I _{fp} ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVR _{DNSJ1B10}	reverse breakdown voltage @ L=10µm, W=42µm, NF=2, WF=21µm	178	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL _{_DNSJ1B10}	leakage current @ VL=155V, T=27°C, W=42µm, NF=2, WF=21µm	-	-	0.6	-	-	pA
IL _{_DNSJ1B10HT}	leakage current @ VL=155V, T=175°C, W=42µm, NF=2, WF=21µm	-	-	1.5	-	-	nA
TC _{_VDFDNSJ1B10}	forward voltage temperature coefficient	-	-	-1.5	-	-	mV/K
VDF _{DNSJ1B10}	forward voltage @ Idio=42µA, L=10µm, W=42µm, NF=2, WF=21µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1a_13

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-215	-195	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-215	-195	1	1.5	V
I _f ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
I _{fp} ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be checked by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVR _{DNSJ1A13}	reverse breakdown voltage @ L=13µm, W=52µm, NF=2, WF=26µm	224	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
IL _{_DNSJ1A13}	leakage current @ VL=195V, T=27°C, W=52µm, NF=2, WF=26µm	-	-	0.6	-	-	pA
IL _{_DNSJ1A13HT}	leakage current @ VL=195V, T=175°C, W=52µm, NF=2, WF=26µm	-	-	1.9	-	-	nA

3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → dfwnsj1a_13 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VDFDNSJ1A13	forward voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VDFDNSJ1A13	forward voltage @ Idio=52µA, L=13µm, W=52µm, NF=2, WF=26µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1a_16

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-255	-235	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-255	-235	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1A16	reverse breakdown voltage @ L=16µm, W=62µm, NF=2, WF=31µm	270	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1A16	leakage current @ VL=235V, T=27°C, W=62µm, NF=2, WF=31µm	-	-	0.8	-	-	pA
IL_DNSJ1A16HT	leakage current @ VL=235V, T=175°C, W=62µm, NF=2, WF=31µm	-	-	2.3	-	-	nA
TC_VDFDNSJ1A16	forward voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VDFDNSJ1A16	forward voltage @ Idio=62µA, L=16µm, W=62µm, NF=2, WF=31µm	0.74	0.76	0.78	0.8	0.82	V

dfwnsj1a_20

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-310	-290	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-310	-290	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm



3. Parameters → 3.38 SJ1XN module → 3.38.2 Device parameters → dfwnsj1a_20 → Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1A20	reverse breakdown voltage @ L=20.5µm, W=82µm, NF=2, WF=41µm	320	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1A20	leakage current @ VL=290V, T=27°C, W=82µm, NF=2, WF=41µm	-	-	0.9	-	-	pA
IL_DNSJ1A20HT	leakage current @ VL=290V, T=175°C, W=82µm, NF=2, WF=41µm	-	-	3	-	-	nA
TC_VDFDNSJ1A20	forward voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VDFDNSJ1A20	forward voltage @ Idio=82µA, L=20.5µm, W=82µm, NF=2, WF=41µm	0.75	0.77	0.79	0.81	0.83	V

dfwnsj1a_28

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode ⁽¹⁾	-40°C to 175°C	-400	-375	1.5	-	V
Vcathode-HW ⁽²⁾	-40°C to 175°C	-	-1.5	400	440	V
Vcathode-NB ⁽²⁾	-40°C to 175°C	-400	-375	1	1.5	V
If ⁽²⁾	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽³⁾	-40°C to 175°C	-	-	1	1.5	mA/µm

Note 1 The max. forward current may restrict the forward voltage of this junction to below 1.5 V.

Note 2 This operating condition will not be check by automatic check tools.

Note 3 Pulsed operation with negligible self-heating (<=100ns)

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BVRDNSJ1A28	reverse breakdown voltage @ L=28µm, W=122µm, NF=2, WF=61µm	415	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
IL_DNSJ1A28	leakage current @ VL=375V, T=27°C, W=122µm, NF=2, WF=61µm	-	-	1.1	-	-	pA

3. Parameters → 3.38 SJ1XN module→ 3.38.2 Device parameters→ dfwnsj1a_28→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
IL_DNSJ1A28HT	leakage current @ VL=375V, T=175°C, W=122µm, NF=2, WF=61µm	-	-	3.8	-	-	nA
TC_VDFDNSJ1A28	forward voltage temperature coefficient	-	-	-1.6	-	-	mV/K
VDFDNSJ1A28	forward voltage @ Idio=122µA, L=28µm, W=122µm, NF=2, WF=61µm	0.75	0.77	0.79	0.81	0.83	V

3. Parameters → 3.39 SJ1XP module

3.39 SJ1XP module

3.39.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Typ	Unit
XJ_SJ1XP	SJ1XP junction depth	1.65	µm

Sheet and contact resistance parameters

Name	Description	Typ	Unit
RSSNSJ1XP	SJ1XP n-type sheet resistance	5.2	kΩ/□
RSSPSJ1XP	SJ1XP p-type sheet resistance	6.5	kΩ/□

3.39.2 Device parameters

phsj1a_4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	72	80	V
VDS	-40°C to 175°C	-80	-72	1.5	-	V
VDB	-40°C to 175°C	-80	-72	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-80	-72	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A4S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5µm	83	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS1A4S	saturation current @ VG=-5V, VD=-30V, L=0.5µm, W=20µm, NF=2, WF=10µm	84	94.5	105	115.5	126	µA/µm
IDPPHS1A4S	pulsed drain current @ VG=-5V, VD=-30V, Dcyc=1%, Pwid=100ns, L=0.5µm, W=20µm, NF=2, WF=10µm	-	-	150	-	-	µA/µm
ROAPHS1A4S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=6µm, NF=2, WF=10µm	-	-	395	435	-	mΩmm ²
RO_PHS1A4S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	53	59	66	73	79	kΩµm
TC_BDSPHS1A4S	breakdown temperature coefficient	-	-	0.1	-	-	V/K

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3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_4 → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
TC_VTPHS1A4S	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	1.9	-	-	mV/K
VTXPHS1A4S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%μm
AIDPHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%μm
AIDPHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%μm
AIDPHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%μm
AIDPHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%μm
AIDPHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%μm
AIDPHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%μm
AIDPHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%μm
AIDPHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%μm
AVTPHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVμm
DLTPHSJ1A	transistor delta length	0	μm
DWTPHSJ1A	transistor delta width	0	μm

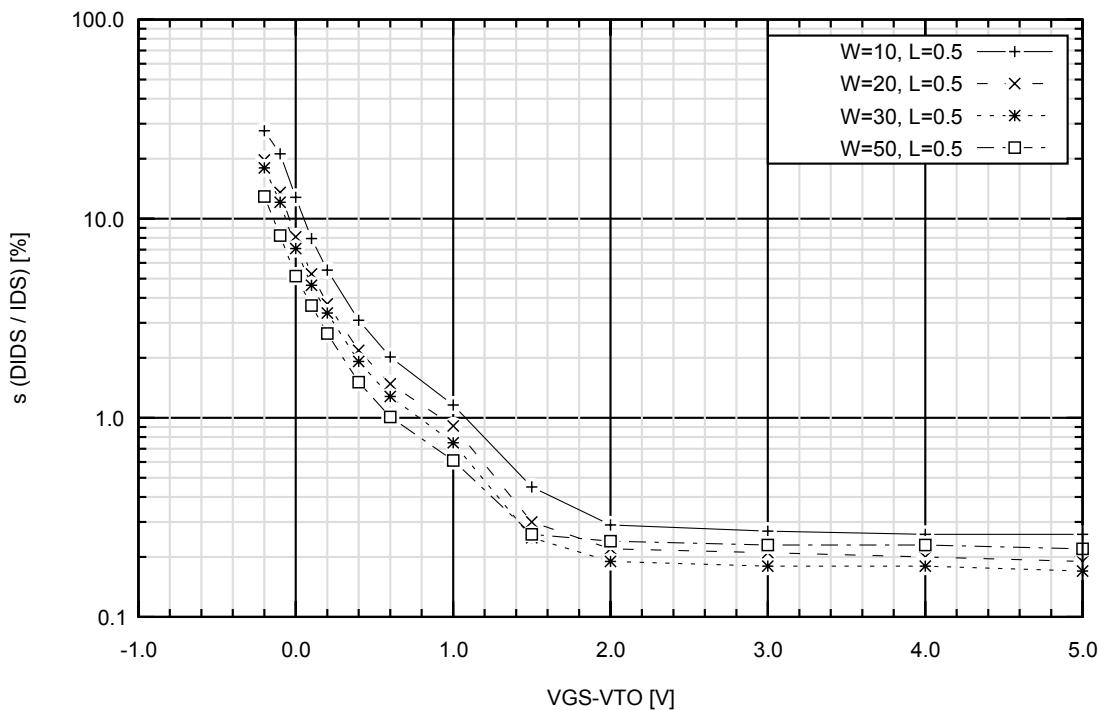


Figure 3.103 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V

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3. Parameters → 3.39 SJ1XP module→ 3.39.2 Device parameters→ phsj1a_5→ Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGD	-40°C to 175°C	-7	-5.5	95	105	V
VDS	-40°C to 175°C	-105	-95	1.5	-	V
VDB	-40°C to 175°C	-105	-95	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-105	-95	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A5S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	109	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5PHS1A5S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	76	85.5	95	104.5	114	μA/μm
IDPPHS1A5S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	126	-	-	μA/μm
ROAPHS1A5S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, Pitch=7.5μm, NF=2, WF=10μm	-	-	630	693	-	mΩmm ²
RO_PHS1A5S	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	67	76	84	92	101	kΩμm
TC_BDSPHS1A5S	breakdown temperature coefficient	-	-	0.11	-	-	V/K
TC_VTPHS1A5S	threshold voltage temperature coefficient @ L=0.5μm, W=20μm	-	-	1.9	-	-	mV/K
VTXPHS1A5S	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=20μm, NF=2, WF=10μm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABTPHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%μm
AIDPHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%μm
AIDPHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%μm
AIDPHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%μm
AIDPHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%μm
AIDPHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%μm
AIDPHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%μm
AIDPHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%μm
AIDPHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%μm
AVTPHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVμm
DLTPHSJ1A	transistor delta length	0	μm
DWTPHSJ1A	transistor delta width	0	μm

3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_5 → Matching parameters

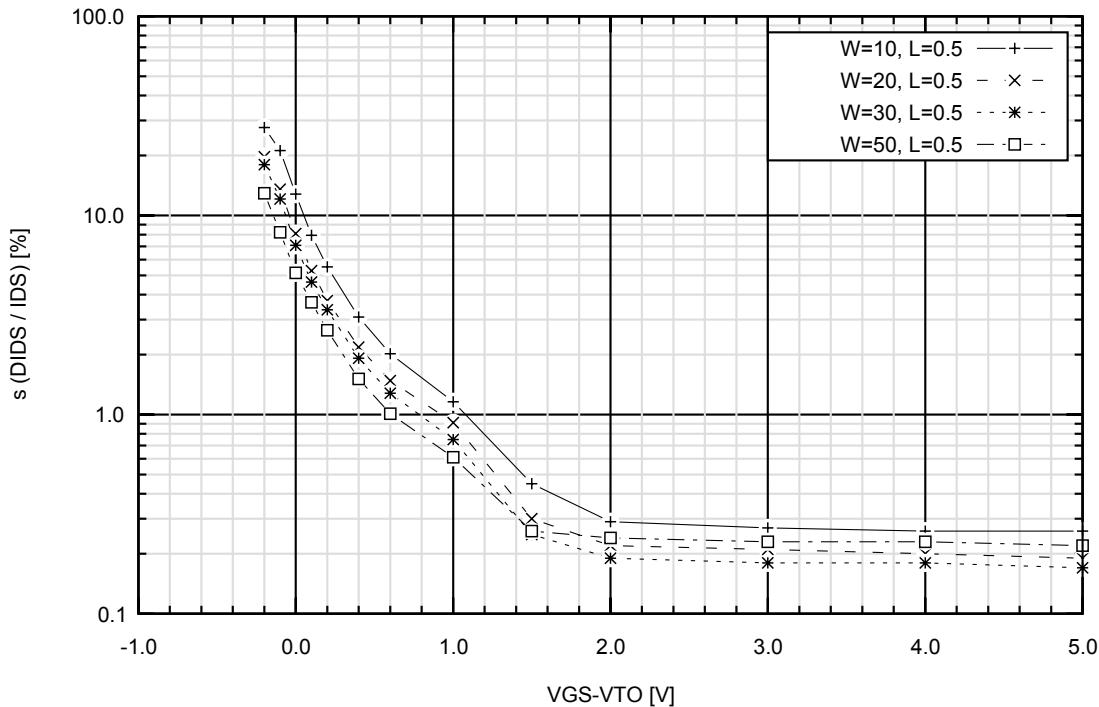


Figure 3.104 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_7

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	115	125	V
VDS	-40°C to 175°C	-125	-115	1.5	-	V
VDB	-40°C to 175°C	-125	-115	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-125	-115	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS _{1A7S}	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	132	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
ID5 _{1A7S}	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	67	75.5	84	92.5	101	μA/μm
IDP _{1A7S}	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	110	-	-	μA/μm

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3. Parameters → 3.39 SJ1XP module→ 3.39.2 Device parameters→ phsj1a_7→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A7S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=9µm, NF=2, WF=10µm	-	-	920	1012	-	mΩmm ²
RO _PHS1A7S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	82	92	102	112	122	kΩµm
TC _BDSPHS1A7S	breakdown temperature coefficient	-	-	0.12	-	-	V/K
TC _VTPHS1A7S	threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	2	-	-	mV/K
VTX PHS1A7S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_7 → Matching parameters

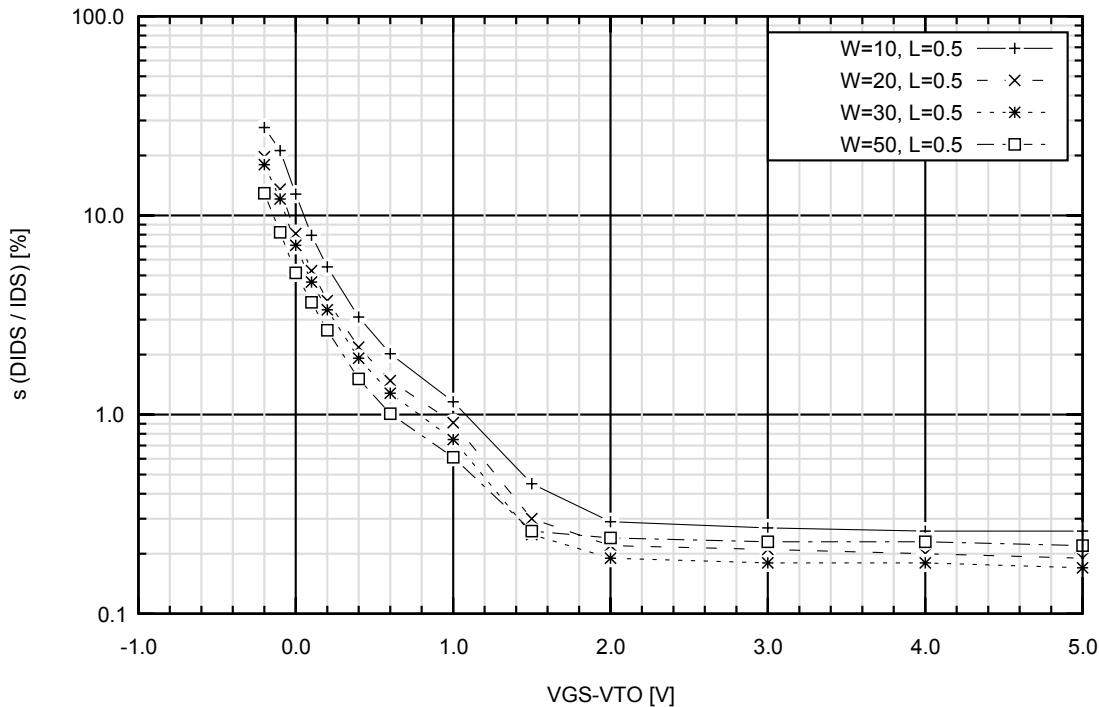


Figure 3.105 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_8

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	140	155	V
VDS	-40°C to 175°C	-155	-140	1.5	-	V
VDB	-40°C to 175°C	-155	-140	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-155	-140	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDS _{PHS1A8S}	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	161	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5 _{PHS1A8S}	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	62	69.5	77	84.5	92	μA/μm
IDP _{PHS1A8S}	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	105	-	-	μA/μm

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3. Parameters → 3.39 SJ1XP module→ 3.39.2 Device parameters→ phsj1a_8→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A8S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=10.5µm, NF=2, WF=10µm	-	-	1250	1375	-	mΩmm ²
RO _PHS1A8S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	95	107	119	131	143	kΩµm
TC _BDSPHS1A8S	breakdown temperature coefficient	-	-	0.13	-	-	V/K
TC _VTPHS1A8S	threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	2	-	-	mV/K
VTX PHS1A8S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_8 → Matching parameters

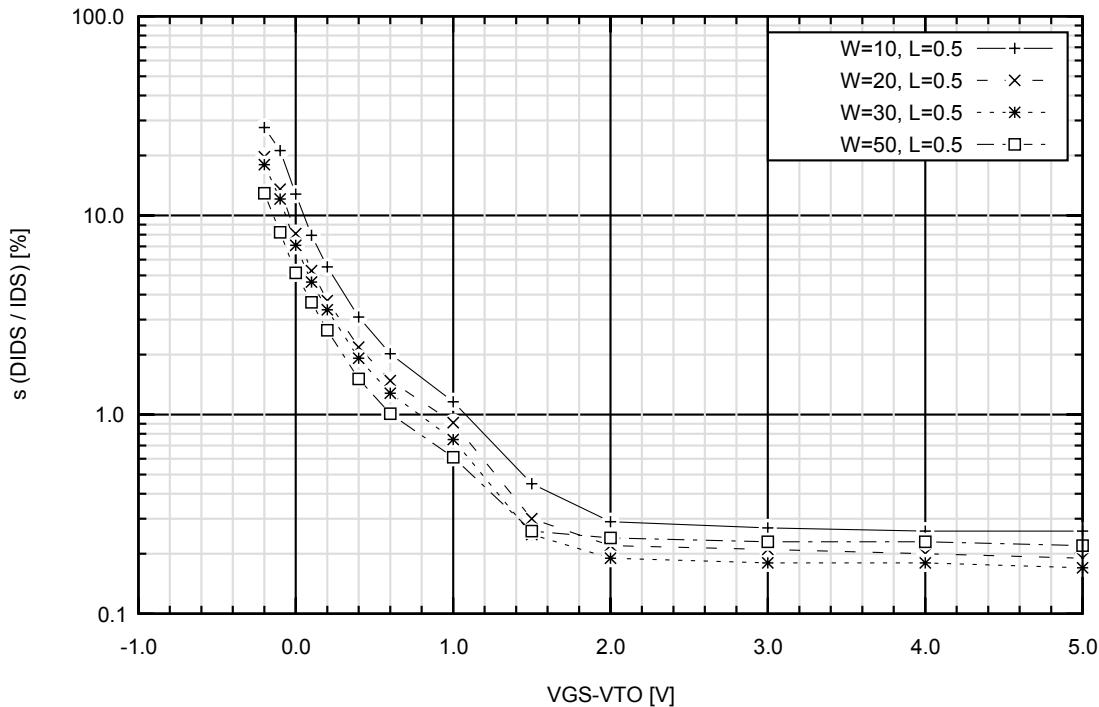


Figure 3.106 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_10

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	155	170	V
VDS	-40°C to 175°C	-170	-155	1.5	-	V
VDB	-40°C to 175°C	-170	-155	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-170	-155	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A10S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	178	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS1A10S	saturation current @ VG=-5V, VD=-40V, L=0.5μm, W=20μm, NF=2, WF=10μm	58	65	72	79	86	μA/μm
IDPPHS1A10S	pulsed drain current @ VG=-5V, VD=-40V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=20μm, NF=2, WF=10μm	-	-	106	-	-	μA/μm

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3. Parameters → 3.39 SJ1XP module→ 3.39.2 Device parameters→ phsj1a_10→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A10S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, Pitch=12µm, NF=2, WF=10µm	-	-	1630	1793	-	mΩmm ²
RO _PHS1A10S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	109	122	136	150	163	kΩµm
TC _BDSPHS1A10S	breakdown temperature coefficient	-	-	0.14	-	-	V/K
TC _VTPHS1A10S	threshold voltage temperature coefficient @ L=0.5µm, W=20µm	-	-	2.1	-	-	mV/K
VTX PHS1A10S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=20µm, NF=2, WF=10µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_10 → Matching parameters

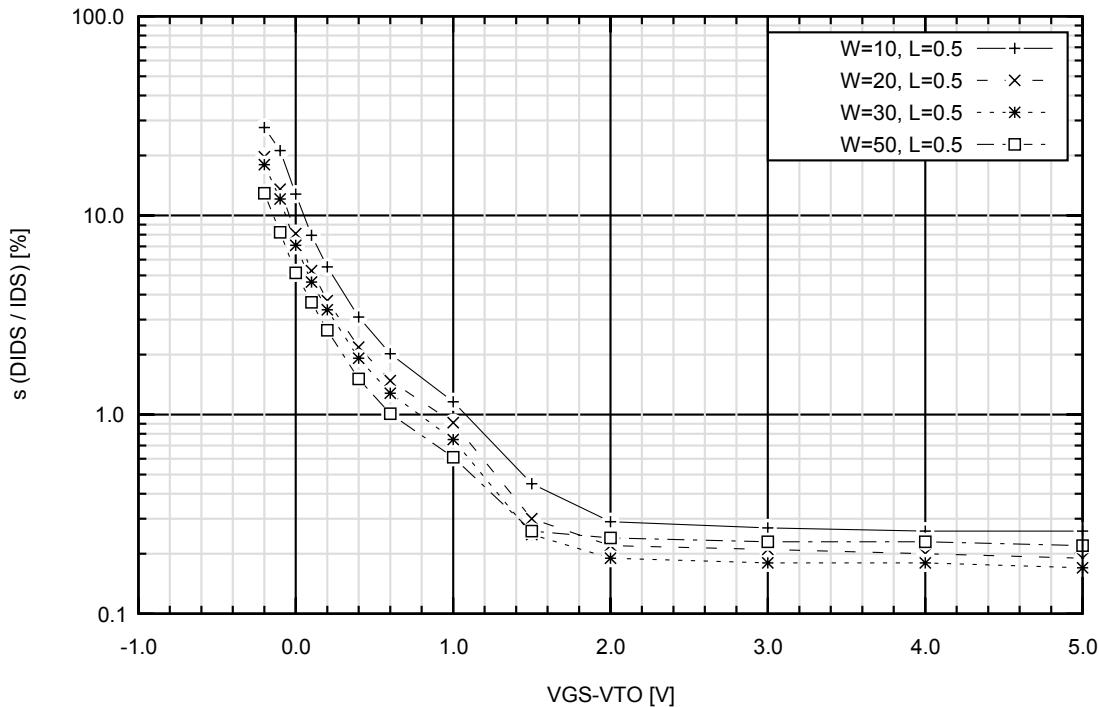


Figure 3.107 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_13

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	195	215	V
VDS	-40°C to 175°C	-215	-195	1.5	-	V
VDB	-40°C to 175°C	-215	-195	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-215	-195	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A13S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	224	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS1A13S	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=50μm, NF=2, WF=25μm	53	59.5	66	72.5	79	μA/μm
IDPPHS1A13S	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=50μm, NF=2, WF=25μm	-	-	92	-	-	μA/μm

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3. Parameters → 3.39 SJ1XP module→ 3.39.2 Device parameters→ phsj1a_13→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A13S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=50µm, Pitch=15µm, NF=2, WF=25µm	-	-	2600	2860	-	mΩmm ²
RO _PHS1A13S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=50µm, NF=2, WF=25µm	138	156	173	190	208	kΩµm
TC _BDSPHS1A13S	breakdown temperature coefficient	-	-	0.15	-	-	V/K
TC _TPHS1A13S	threshold voltage temperature coefficient @ L=0.5µm, W=50µm	-	-	2.1	-	-	mV/K
VTX PHS1A13S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=50µm, NF=2, WF=25µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_13 → Matching parameters

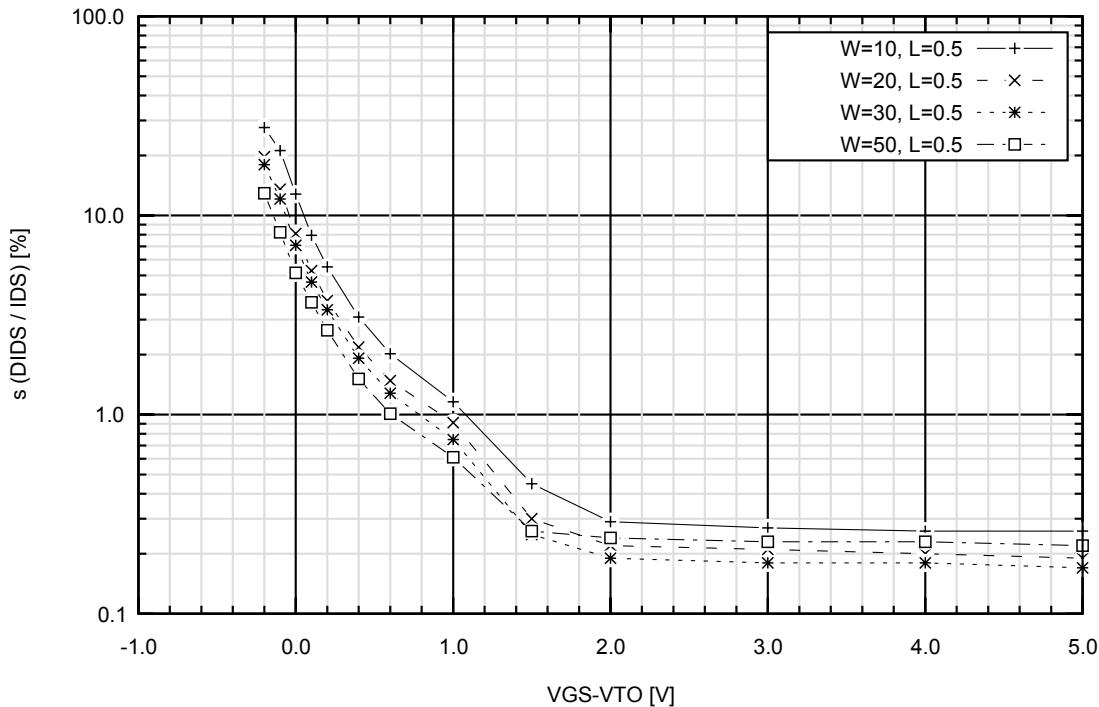


Figure 3.108 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_16

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	235	255	V
VDS	-40°C to 175°C	-255	-235	1.5	-	V
VDB	-40°C to 175°C	-255	-235	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-255	-235	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A16S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	270	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS1A16S	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=60μm, NF=2, WF=30μm	52	58.5	65	71.5	78	μA/μm
IDPPHS1A16S	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=60μm, NF=2, WF=30μm	-	-	86	-	-	μA/μm

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3. Parameters → 3.39 SJ1XP module→ 3.39.2 Device parameters→ phsj1a_16→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A16S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=60µm, Pitch=18µm, NF=2, WF=30µm	-	-	3720	4092	-	mΩmm ²
RO _PHS1A16S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=60µm, NF=2, WF=30µm	165	186	207	228	249	kΩµm
TC _BDSPHS1A16S	breakdown temperature coefficient	-	-	0.16	-	-	V/K
TC _VTPHS1A16S	threshold voltage temperature coefficient @ L=0.5µm, W=60µm	-	-	2.1	-	-	mV/K
VTX PHS1A16S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=60µm, NF=2, WF=30µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_16 → Matching parameters

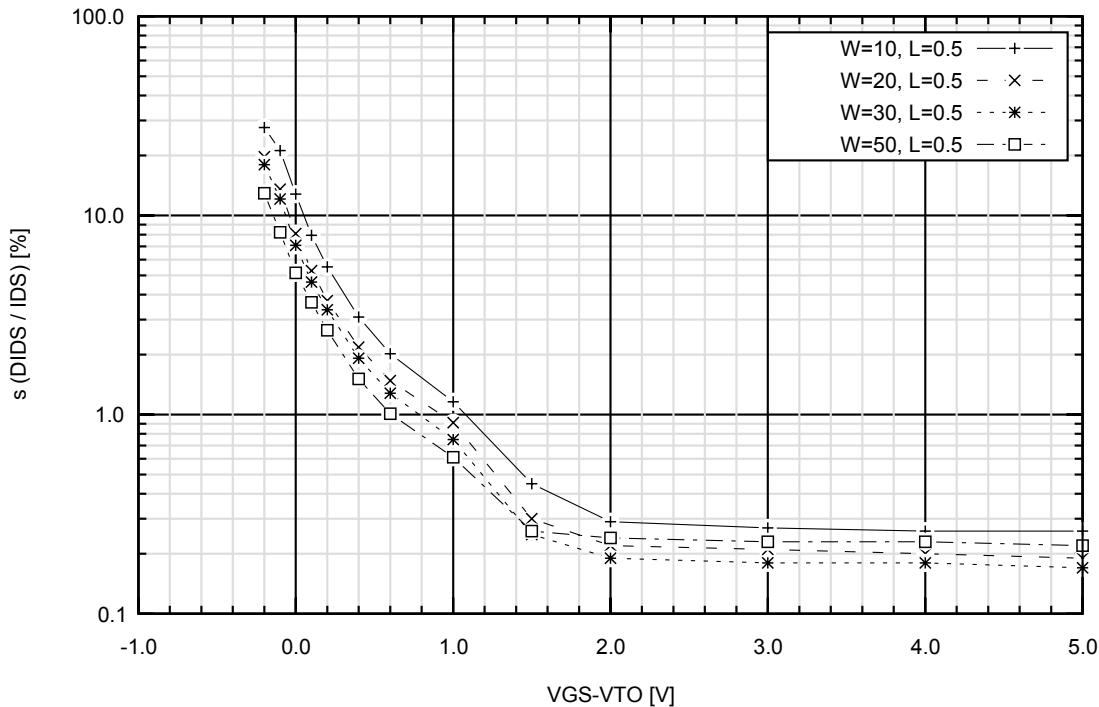


Figure 3.109 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_20

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	290	310	V
VDS	-40°C to 175°C	-310	-290	1.5	-	V
VDB	-40°C to 175°C	-310	-290	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-310	-290	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A20S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	320	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS1A20S	saturation current @ VG=-5V, VD=-60V, L=0.5μm, W=120μm, NF=2, WF=60μm	47	53	59	65	71	μA/μm
IDPPHS1A20S	pulsed drain current @ VG=-5V, VD=-60V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=120μm, NF=2, WF=60μm	-	-	74	-	-	μA/μm

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3. Parameters → 3.39 SJ1XP module→ 3.39.2 Device parameters→ phsj1a_20→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA PHS1A20S	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=120µm, Pitch=22.5µm, NF=2, WF=60µm	-	-	5890	6483	-	mΩmm ²
RO _PHS1A20S	on resistance @ VG=-5V, VD=-0.1V, L=0.5µm, W=120µm, NF=2, WF=60µm	209	236	262	288	315	kΩµm
TC _BDSPHS1A20S	breakdown temperature coefficient	-	-	0.17	-	-	V/K
TC _VTPHS1A20S	threshold voltage temperature coefficient @ L=0.5µm, W=120µm	-	-	2.1	-	-	mV/K
VTX PHS1A20S	extrapolated threshold voltage @ VD=-0.1V, L=0.5µm, W=120µm, NF=2, WF=60µm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT PHSJ1A	pelgrom coefficient gain factor mismatch	3.04	%µm
AID PHSJ1A00	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%µm
AID PHSJ1A02	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%µm
AID PHSJ1A04	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%µm
AID PHSJ1A06	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%µm
AID PHSJ1A10	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%µm
AID PHSJ1A20	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%µm
AID PHSJ1A30	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%µm
AID PHSJ1A50	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%µm
AVT PHSJ1A	pelgrom coefficient threshold voltage mismatch	13.22	mVµm
DLT PHSJ1A	transistor delta length	0	µm
DWT PHSJ1A	transistor delta width	0	µm

3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_20 → Matching parameters

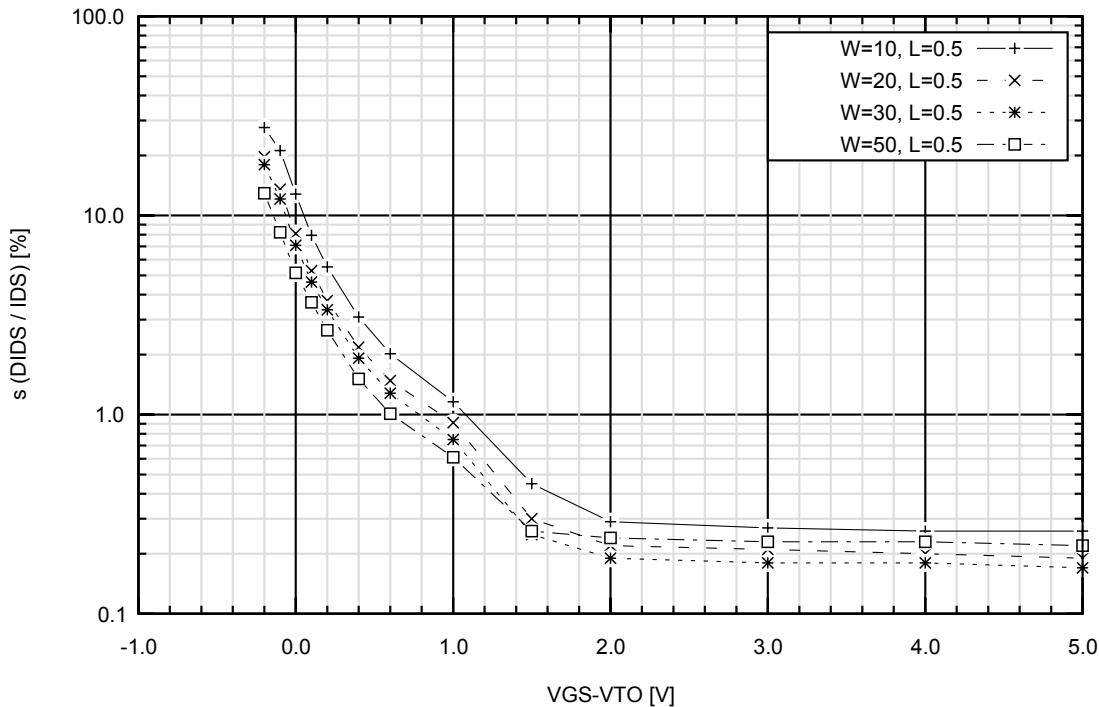


Figure 3.110 Device phsj1a: drain current matching vs. VGS-VTO (typical values, drawn W and L)

phsj1a_31

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
VGS	-40°C to 175°C	-7	-5.5	5.5	7	V
VGD	-40°C to 175°C	-7	-5.5	375	400	V
VDS	-40°C to 175°C	-400	-375	1.5	-	V
VDB	-40°C to 175°C	-400	-375	1.5	-	V
VB-HW	-40°C to 175°C	-0.5	0	400	440	V
VB-NB ⁽¹⁾	-40°C to 175°C	-400	-375	1	1.5	V

Note 1 This operating condition will not be checked by automatic check tools.

Note: The node B (BULK) is: NWELL2

Note: The dhw# junction diode must be reverse biased to Min VAC to achieve maximum operating condition stated.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDSPHS1A31S	drain-source breakdown @ VG=0V, Id=50nA, L=0.5μm	415	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
ID5PHS1A31S	saturation current @ VG=-5V, VD=-100V, L=0.5μm, W=160μm, NF=2, WF=80μm	50	55.5	61	66.5	72	μA/μm
IDPPHS1A31S	pulsed drain current @ VG=-5V, VD=-100V, Dcyc=1%, Pwid=100ns, L=0.5μm, W=160μm, NF=2, WF=80μm	-	-	94	-	-	μA/μm

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3. Parameters → 3.39 SJ1XP module→ 3.39.2 Device parameters→ phsj1a_31→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
ROA _{PHS1A31S}	area specific on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=160μm, Pitch=33μm, NF=2, WF=80μm	-	-	11682	12903	-	mΩmm ²
RO _{PHS1A31S}	on resistance @ VG=-5V, VD=-0.1V, L=0.5μm, W=160μm, NF=2, WF=80μm	280	317	354	391	428	kΩμm
TC _{BDS} _{PHS1A31S}	breakdown temperature coefficient	-	-	0.19	-	-	V/K
TC _{VTP} _{PHS1A31S}	threshold voltage temperature coefficient @ L=0.5μm, W=160μm	-	-	2.2	-	-	mV/K
VTX _{PHS1A31S}	extrapolated threshold voltage @ VD=-0.1V, L=0.5μm, W=160μm, NF=2, WF=80μm	-1.32	-1.24	-1.16	-1.08	-1	V

Matching parameters

Name	Description	Typ	Unit
ABT _{PHSJ1A}	pelgrom coefficient gain factor mismatch	3.04	%μm
AID _{PHSJ1A00}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0V	27.39	%μm
AID _{PHSJ1A02}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.2V	12.42	%μm
AID _{PHSJ1A04}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.4V	7.06	%μm
AID _{PHSJ1A06}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=0.6V	4.69	%μm
AID _{PHSJ1A10}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=1V	2.76	%μm
AID _{PHSJ1A20}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=2V	0.73	%μm
AID _{PHSJ1A30}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=3V	0.69	%μm
AID _{PHSJ1A50}	pelgrom coefficient drain current mismatch @ VDS=5V, VG-VT=5V	0.65	%μm
AVT _{PHSJ1A}	pelgrom coefficient threshold voltage mismatch	13.22	mVμm
DLT _{PHSJ1A}	transistor delta length	0	μm
DWT _{PHSJ1A}	transistor delta width	0	μm

3. Parameters → 3.39 SJ1XP module → 3.39.2 Device parameters → phsj1a_31 → Matching parameters

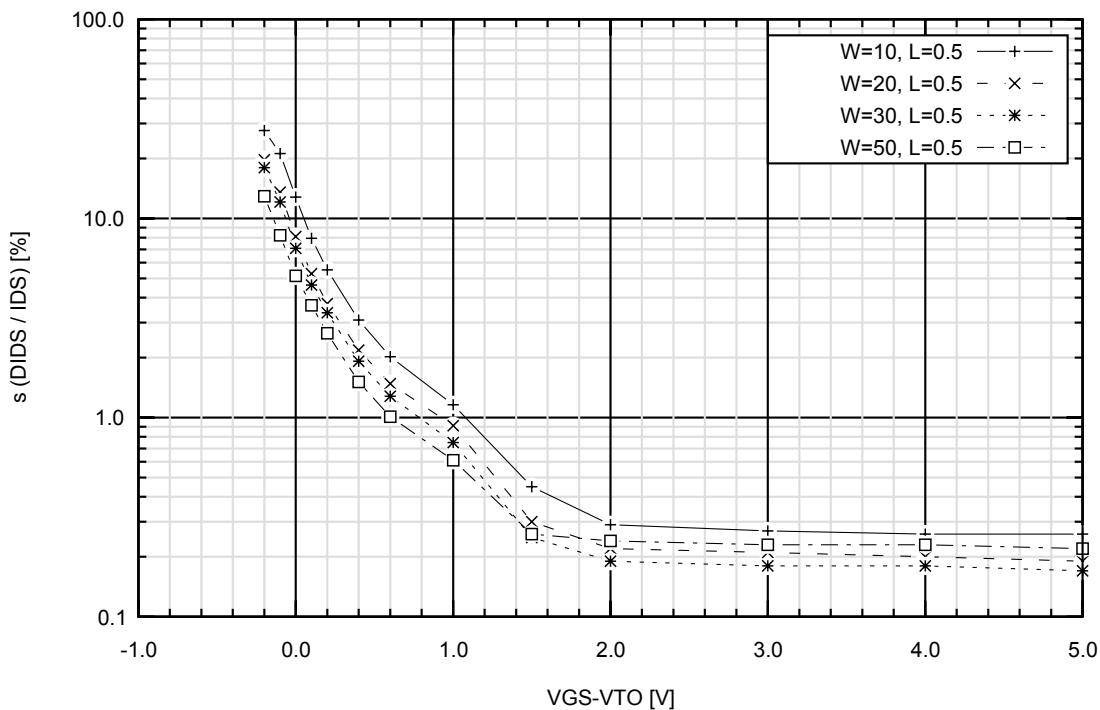


Figure 3.111 Device phsj1a: drain current matching vs. $V_{GS}-V_{TO}$ (typical values, drawn W and L)

3. Parameters → 3.40 DIODEA module

3.40 DIODEA module

3.40.1 Device parameters

dnpa

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-9	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	5	-	µA/µm

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DNPA	breakdown voltage @ Irev=10µA, L=1µm, W=10µm	7.5	7.713	7.925	8.088	8.25	V
IL_DNPA	leakage current @ VL=4.5V, T=27°C, L=1µm, W=10µm	-	-	0.09	-	-	pA
IL_DNPAAHT	leakage current @ VL=4.5V, T=175°C, L=1µm, W=10µm	-	-	200	-	-	pA
TC_BVDNPA	breakdown temperature coefficient	-	-	4.2	-	-	mV/K

dnpati

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-9	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	0.5	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	5	-	µA/µm

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DNPATI	breakdown voltage @ Irev=10µA, L=1µm, W=10µm	7.5	7.713	7.925	8.088	8.25	V
IL_DNPATI	leakage current @ VL=4.5V, T=27°C, L=1µm, W=10µm	-	-	0.09	-	-	µA/µm ²
IL_DNPATIHT	leakage current @ VL=4.5V, T=175°C, L=1µm, W=10µm	-	-	200	-	-	pA
TC_BVDNPATI	breakdown temperature coefficient	-	-	4.2	-	-	mV/K

3. Parameters → 3.41 DIODEB module

3.41 DIODEB module

3.41.1 Device parameters

dza

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-6.3	0	0.5	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	10	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	100	-	µA/µm

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DZA	breakdown voltage @ Irev=10µA, L=1µm, W=10µm	5.04	5.18	5.32	5.46	5.6	V
IL_DZA	leakage current @ VL=4.5V, T=27°C, L=1µm, W=10µm	-	-	10	-	-	nA/µm ²
IL_DZAHT	leakage current @ VL=4.5V, T=175°C, L=1µm, W=10µm	-	-	25	-	-	nA/µm ²
TC_BVDZA	breakdown temperature coefficient	-	-	0.8	-	-	mV/K

dzati

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-6	1.5	-	V
VA-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/µm
Ifp ⁽²⁾	-40°C to 175°C	-	-	1	1.5	mA/µm
Ibr	-40°C to 175°C	-	-	10	-	µA/µm
Ibr1000	-40°C to 175°C	-	-	100	-	µA/µm

Note 1 This operating condition will not be check by automatic check tools.

Note 2 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DZATI	breakdown voltage @ Irev=10µA, L=1µm, W=10µm	5.04	5.18	5.32	5.46	5.6	V
IL_DZATI	leakage current @ VL=4.5V, T=27°C, L=1µm, W=10µm	-	-	10	-	-	nA/µm ²
IL_DZATIHT	leakage current @ VL=4.5V, T=175°C, L=1µm, W=10µm	-	-	25	-	-	nA/µm ²
TC_BVDZATI	breakdown temperature coefficient	-	-	0.8	-	-	mV/K
TC_VDFDZATI	forward voltage temperature coefficient	-	-	-1.7	-	-	mV/K

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3. Parameters → 3.41 DIODEB module→ 3.41.1 Device parameters→ dzati→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VDFDZATI	diode forward voltage @ Idio=1µA, L=1µm, W=10µm	-	0.713	0.718	0.723	-	V

3. Parameters → 3.42 DIODEC module

3.42 DIODEC module

3.42.1 Device parameters

dzbt1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-	-6.3	0	0.5	V
Vcathode-Vpepi	-40°C to 175°C	-0.5	0	5.5	7	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-440	-400	400	440	V
Ibr	-40°C to 175°C	-	-	10	-	μA/μm
Ibr1000	-40°C to 175°C	-	-	100	-	μA/μm

Note 1 This operating condition will not be check by automatic check tools.

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DZBT1	breakdown voltage @ Irev=10μA, L=1.16μm, W=10μm	5.14	5.22	5.3	5.38	5.46	V
IL_DZBT1	leakage current @ VL=4.5V, T=27°C, L=1.16μm, W=10μm	-	-	0.7	-	-	nA/μm ²
IL_DZBT1HT	leakage current @ VL=4.5V, T=175°C, L=1.16μm, W=10μm	-	-	1.7	-	-	nA/μm ²
TC_BVDZBT1	breakdown temperature coefficient	-	-	1.3	-	-	mV/K

dzct1

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vanode-Vcathode	-40°C to 175°C	-7	-6	1.5	-	V
VPT-HW ⁽¹⁾	-40°C to 175°C	-	-6.3	200	220	V
If	-40°C to 175°C	-	-	0.1	0.15	mA/μm
Ifp ⁽²⁾	-40°C to 175°C	-	-	1	1.5	mA/μm
Ibr	-40°C to 175°C	-	-	10	-	μA/μm
Ibr1000	-40°C to 175°C	-	-	100	-	μA/μm

Note 1 This operating condition will not be check by automatic check tools.

Note 2 Pulsed operation with negligible self-heating (<=100ns)

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BV_DZCT1	breakdown voltage @ Irev=9μA, L=1.16μm, W=9μm	5.18	5.26	5.34	5.42	5.5	V
IL_DZCT1	leakage current @ VL=4.5V, T=27°C, L=1.16μm, W=9μm	-	-	0.6	-	-	nA/μm ²
IL_DZCT1HT	leakage current @ VL=4.5V, T=175°C, L=1.16μm, W=9μm	-	-	1.4	-	-	nA/μm ²
TC_BVDZCT1	breakdown temperature coefficient	-	-	1.25	-	-	mV/K
TC_VDFDZCT1	forward voltage temperature coefficient	-	-	-1.73	-	-	mV/K

⇒

3. Parameters → 3.42 DIODEC module→ 3.42.1 Device parameters→ dzcti→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VDFDZCTI	diode forward voltage @ Idio=1µA, L=1.16µm, W=9µm	-	0.696	0.701	0.706	-	V

3. Parameters → 3.43 MIM module

3.43 MIM module

3.43.1 Device parameters

cmm3t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM3T	cmm3t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIM3T	cmm3t area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/µm²
CAP_MIM3T	cmm3t perimeter capacitance	-	-	170	-	-	aF/µm
IL_MIM3T	cmm3t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCMIM3T	cmm3t temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM3T	cmm3t equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM3T	cmm3t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM3T	cmm3t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	pelgrom coefficient capacitor mismatch	0.28	%µm

cmm4t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM4T	cmm4t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIM4T	cmm4t area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/µm²
CAP_MIM4T	cmm4t perimeter capacitance	-	-	170	-	-	aF/µm
IL_MIM4T	cmm4t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCMIM4T	cmm4t temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM4T	cmm4t equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm

3. Parameters → 3.43 MIM module→ 3.43.1 Device parameters→ cmm4t→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VC1_MIM4T	cmm4t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM4T	cmm4t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	pelgrom coefficient capacitor mismatch	0.28	%μm

cmm5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM5T	cmm5t breakdown voltage @ Ibr=0.6μA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIM5T	cmm5t area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/μm ²
CAP_MIM5T	cmm5t perimeter capacitance	-	-	170	-	-	aF/μm
IL_MIM5T	cmm5t leakage current @ VL=7V	-	-	-	0.1	-	fA/μm ²
TCCMIM5T	cmm5t temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM5T	cmm5t equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM5T	cmm5t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM5T	cmm5t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	pelgrom coefficient capacitor mismatch	0.28	%μm

cmm6t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM6T	cmm6t breakdown voltage @ Ibr=0.6μA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIM6T	cmm6t area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/μm ²

⇒

3. Parameters → 3.43 MIM module→ 3.43.1 Device parameters→ cmm6t→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
CAP_MIM6T	cmm6t perimeter capacitance	-	-	170	-	-	aF/ μ m
IL_MIM6T	cmm6t leakage current @ VL=7V	-	-	-	0.1	-	fA/ μ m ²
TCCMIM6T	cmm6t temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM6T	cmm6t equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM6T	cmm6t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM6T	cmm6t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	pelgrom coefficient capacitor mismatch	0.28	% μ m

3. Parameters → 3.44 MIM23 module

3.44 MIM23 module

3.44.1 Device parameters

cmm3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM3	cmm3 breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIM3	cmm3 area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/µm²
CAP_MIM3	cmm3 perimeter capacitance	-	-	170	-	-	aF/µm
IL_MIM3	cmm3 leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCMIM3	cmm3 temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM3	cmm3 equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM3	cmm3 capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM3	cmm3 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	pelgrom coefficient capacitor mismatch	0.28	%µm

3. Parameters → 3.45 MIM34 module

3.45 MIM34 module

3.45.1 Device parameters

cmm4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM4	cmm4 breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIM4	cmm4 area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/µm²
CAP_MIM4	cmm4 perimeter capacitance	-	-	170	-	-	aF/µm
IL_MIM4	cmm4 leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCMIM4	cmm4 temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM4	cmm4 equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM4	cmm4 capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM4	cmm4 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	pelgrom coefficient capacitor mismatch	0.28	%µm

3. Parameters → 3.46 MIM45 module

3.46 MIM45 module

3.46.1 Device parameters

cmm5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIM5	cmm5 breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIM5	cmm5 area capacitance @ Vbias=0V	0.85	0.92	1	1.08	1.15	fF/µm²
CAP_MIM5	cmm5 perimeter capacitance	-	-	170	-	-	aF/µm
IL_MIM5	cmm5 leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCMIM5	cmm5 temperature coefficient	-	-	40	-	-	1e-06/K
THD_MIM5	cmm5 equivalent dielectric thickness @ Er=7.3	-	-	65	-	-	nm
VC1_MIM5	cmm5 capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_MIM5	cmm5 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIM	pelgrom coefficient capacitor mismatch	0.28	%µm

3. Parameters → 3.47 DMIM module

3.47 DMIM module

3.47.1 Device parameters

cdmm4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIM4	cdmm4 breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_DMIM4	cdmm4 area capacitance @ Vbias=0V	1.7	1.85	2	2.15	2.3	fF/µm²
CAP_DMIM4	cdmm4 perimeter capacitance	-	-	230	-	-	aF/µm
IL_DMIM4	cdmm4 leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCDMIM4	cdmm4 temperature coefficient	-	-	40	-	-	1e-06/K
THD_DMIM4	cdmm4 equivalent dielectric thickness @ Er=7.3	-	-	32.5	-	-	nm
VC1_DMIM4	cdmm4 capacitor voltage coefficient 1	-	-	3	-	-	ppm/V
Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.							
VC2_DMIM4	cdmm4 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_DMIM	pelgrom coefficient capacitor mismatch	0.2	%µm

cdmm4t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIM4T	cdmm4t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_DMIM4T	cdmm4t area capacitance @ Vbias=0V	1.7	1.85	2	2.15	2.3	fF/µm²
CAP_DMIM4T	cdmm4t perimeter capacitance	-	-	230	-	-	aF/µm
IL_DMIM4T	cdmm4t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCDMIM4T	cdmm4t temperature coefficient	-	-	40	-	-	1e-06/K

3. Parameters → 3.47 DMIM module→ 3.47.1 Device parameters→ cdmm4t→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
THD_DMIM4T	cdmm4t equivalent dielectric thickness @ Er=7.3	-	-	32.5	-	-	nm
VC1_DMIM4T	cdmm4t capacitor voltage coefficient 1	-	-	3	-	-	ppm/V
	Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.						
VC2_DMIM4T	cdmm4t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_DMIM	pelgrom coefficient capacitor mismatch	0.2	%μm

3. Parameters → 3.48 DMIM3 module

3.48 DMIM3 module

3.48.1 Device parameters

cdmm5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIM5	cdmm5 breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_DMIM5	cdmm5 area capacitance @ Vbias=0V	1.7	1.85	2	2.15	2.3	fF/µm²
CAP_DMIM5	cdmm5 perimeter capacitance	-	-	230	-	-	aF/µm
IL_DMIM5	cdmm5 leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCDMIM5	cdmm5 temperature coefficient	-	-	40	-	-	1e-06/K
THD_DMIM5	cdmm5 equivalent dielectric thickness @ Er=7.3	-	-	32.5	-	-	nm
VC1_DMIM5	cdmm5 capacitor voltage coefficient 1	-	-	3	-	-	ppm/V
Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.							
VC2_DMIM5	cdmm5 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_DMIM	pelgrom coefficient capacitor mismatch	0.2	%µm

cdmm5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIM5T	cdmm5t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_DMIM5T	cdmm5t area capacitance @ Vbias=0V	1.7	1.85	2	2.15	2.3	fF/µm²
CAP_DMIM5T	cdmm5t perimeter capacitance	-	-	230	-	-	aF/µm
IL_DMIM5T	cdmm5t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCCDMIM5T	cdmm5t temperature coefficient	-	-	40	-	-	1e-06/K

3. Parameters → 3.48 DMIM3 module→ 3.48.1 Device parameters→ cdmm5t→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
THD_DMIM5T	cdmm5t equivalent dielectric thickness @ Er=7.3	-	-	32.5	-	-	nm
VC1_DMIM5T	cdmm5t capacitor voltage coefficient 1	-	-	3	-	-	ppm/V
	Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.						
VC2_DMIM5T	cdmm5t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_DMIM	pelgrom coefficient capacitor mismatch	0.2	%μm

3. Parameters → 3.49 TMIM module

3.49 TMIM module

3.49.1 Device parameters

ctmm5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_TMIM5	ctmm5 breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_TMIM5	ctmm5 area capacitance @ Vbias=0V	2.55	2.77	3	3.23	3.45	fF/µm²
CAP_TMIM5	ctmm5 perimeter capacitance	-	-	365	-	-	aF/µm
IL_TMIM5	ctmm5 leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCC_TMIM5	ctmm5 temperature coefficient	-	-	40	-	-	1e-06/K
THD_TMIM5	ctmm5 equivalent dielectric thickness @ Er=7.3	-	-	22	-	-	nm
VC1_TMIM5	ctmm5 capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_TMIM5	ctmm5 capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_TMIM	pelgrom coefficient capacitor mismatch	0.16	%µm

ctmm5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-12	-10	10	12	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_TMIM5T	ctmm5t breakdown voltage @ Ibr=0.6µA	20	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_TMIM5T	ctmm5t area capacitance @ Vbias=0V	2.55	2.77	3	3.23	3.45	fF/µm²
CAP_TMIM5T	ctmm5t perimeter capacitance	-	-	365	-	-	aF/µm
IL_TMIM5T	ctmm5t leakage current @ VL=7V	-	-	-	0.1	-	fA/µm²
TCC_TMIM5T	ctmm5t temperature coefficient	-	-	40	-	-	1e-06/K
THD_TMIM5T	ctmm5t equivalent dielectric thickness @ Er=7.3	-	-	22	-	-	nm

3. Parameters → 3.49 TMIM module→ 3.49.1 Device parameters→ ctmm5t→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VC1_TMIM5T	ctmm5t capacitor voltage coefficient 1	-	-	-15	-	-	ppm/V
VC2_TMIM5T	ctmm5t capacitor voltage coefficient 2	-	-	3.5	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_TMIM	pelgrom coefficient capacitor mismatch	0.16	%μm

3. Parameters → 3.50 MIMH module

3.50 MIMH module

3.50.1 Device parameters

cmmh3t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH3T	cmmh3t breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIMH3TB	cmmh3t area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH3T	cmmh3t perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH3T	cmmh3t leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH3T	cmmh3t temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH3TB	cmmh3t equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH3T	cmmh3t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH3T	cmmh3t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	pelgrrom coefficient capacitor mismatch	0.3	%µm

cmmh4t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH4T	cmmh4t breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIMH4TB	cmmh4t area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH4T	cmmh4t perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH4T	cmmh4t leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH4T	cmmh4t temperature coefficient	-	-	47	-	-	1e-06/K

3. Parameters → 3.50 MIMH module → 3.50.1 Device parameters → cmmh4t → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
THD_MIMH4TB	cmmh4t equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH4T	cmmh4t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH4T	cmmh4t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	pelgrom coefficient capacitor mismatch	0.3	%μm

cmmh5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH5T	cmmh5t breakdown voltage @ Ibr=0.6μA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIMH5TB	cmmh5t area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/μm ²
CAP_MIMH5T	cmmh5t perimeter capacitance	-	-	67	-	-	aF/μm
IL_MIMH5T	cmmh5t leakage current @ VL=7V	-	-	-	10	-	fA/μm ²
TCCMIMH5T	cmmh5t temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH5TB	cmmh5t equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH5T	cmmh5t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH5T	cmmh5t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	pelgrom coefficient capacitor mismatch	0.3	%μm

cmmh6t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

3. Parameters → 3.50 MIMH module → 3.50.1 Device parameters → cmmh6t → Process parameters

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH6T	cmmh6t breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIMH6TB	cmmh6t area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH6T	cmmh6t perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH6T	cmmh6t leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH6T	cmmh6t temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH6TB	cmmh6t equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH6T	cmmh6t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH6T	cmmh6t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	pelgrom coefficient capacitor mismatch	0.3	%µm

cmmh4l

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH4L	cmmh4l breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIMH4LB	cmmh4l area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH4L	cmmh4l perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH4L	cmmh4l leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH4L	cmmh4l temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH4LB	cmmh4l equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH4L	cmmh4l capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH4L	cmmh4l capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMHL	pelgrom coefficient capacitor mismatch	0.3	%µm

3. Parameters → 3.50 MIMH module → 3.50.1 Device parameters → cmmh5l → Operating conditions

cmmh5l

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH5L	cmmh5l breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIMH5LB	cmmh5l area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH5L	cmmh5l perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH5L	cmmh5l leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH5L	cmmh5l temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH5LB	cmmh5l equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH5L	cmmh5l capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH5L	cmmh5l capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMHL	pelgrom coefficient capacitor mismatch	0.3	%µm

cmmh6l

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH6L	cmmh6l breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
	Note: The limits of this pass/fail parameter do not reflect the statistics of the process						
CAA_MIMH6LB	cmmh6l area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH6L	cmmh6l perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH6L	cmmh6l leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH6L	cmmh6l temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH6LB	cmmh6l equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH6L	cmmh6l capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V

3. Parameters → 3.50 MIMH module→ 3.50.1 Device parameters→ cmmh6l→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
VC2_MIMH6L	cmmh6l capacitor voltage coefficient 2	-	-	35	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_MIMHL	pelgrom coefficient capacitor mismatch	0.3	%μm

3. Parameters → 3.51 MIMH23 module

3.51 MIMH23 module

3.51.1 Device parameters

cmmh3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH3	cmmh3 breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIMH3B	cmmh3 area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH3	cmmh3 perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH3	cmmh3 leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH3	cmmh3 temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH3	cmmh3 equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH3	cmmh3 capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH3	cmmh3 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	pelgrom coefficient capacitor mismatch	0.3	%µm

3. Parameters → 3.52 MIMH34 module

3.52 MIMH34 module

3.52.1 Device parameters

cmmh4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH4	cmmh4 breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIMH4B	cmmh4 area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH4	cmmh4 perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH4	cmmh4 leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH4	cmmh4 temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH4	cmmh4 equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH4	cmmh4 capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH4	cmmh4 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	pelgrom coefficient capacitor mismatch	0.3	%µm

3. Parameters → 3.53 MIMH45 module

3.53 MIMH45 module

3.53.1 Device parameters

cmmh5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_MIMH5	cmmh5 breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_MIMH5B	cmmh5 area capacitance @ Vbias=0V	1.75	2.05	2.35	2.65	2.95	fF/µm²
CAP_MIMH5	cmmh5 perimeter capacitance	-	-	67	-	-	aF/µm
IL_MIMH5	cmmh5 leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCMIMH5	cmmh5 temperature coefficient	-	-	47	-	-	1e-06/K
THD_MIMH5	cmmh5 equivalent dielectric thickness @ Er=7.3	-	-	27.6	-	-	nm
VC1_MIMH5	cmmh5 capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_MIMH5	cmmh5 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_MIMH	pelgrom coefficient capacitor mismatch	0.3	%µm

3. Parameters → 3.54 DMIMH module

3.54 DMIMH module

3.54.1 Device parameters

cdmmh4

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIMH4	cdmmh4 breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_DMIMH4B	cdmmh4 area capacitance @ Vbias=0V	3.5	4.1	4.7	5.3	5.9	fF/µm²
CAP_DMIMH4	cdmmh4 perimeter capacitance	-	-	220	-	-	aF/µm
IL_DMIMH4	cdmmh4 leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCDMIMH4	cdmmh4 temperature coefficient	-	-	47	-	-	1e-06/K
THD_DMIMH4B	cdmmh4 equivalent dielectric thickness @ Er=7.3	-	-	13.8	-	-	nm
VC1_DMIMH4	cdmmh4 capacitor voltage coefficient 1	-	-	-20	-	-	ppm/V
Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.							
VC2_DMIMH4	cdmmh4 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_DMIMH	pelgrom coefficient capacitor mismatch	0.22	%µm

cdmmh4t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIMH4T	cdmmh4t breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_DMIMH4TB	cdmmh4t area capacitance @ Vbias=0V	3.5	4.1	4.7	5.3	5.9	fF/µm²
CAP_DMIMH4T	cdmmh4t perimeter capacitance	-	-	220	-	-	aF/µm
IL_DMIMH4T	cdmmh4t leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCDMIMH4T	cdmmh4t temperature coefficient	-	-	47	-	-	1e-06/K

3. Parameters → 3.54 DMIMH module→ 3.54.1 Device parameters→ cdmmh4t→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
THD_DMIMH4TB	cdmmh4t equivalent dielectric thickness @ Er=7.3	-	-	13.8	-	-	nm
VC1_DMIMH4T	cdmmh4t capacitor voltage coefficient 1	-	-	-20	-	-	ppm/V
	Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.						
VC2_DMIMH4T	cdmmh4t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_DMIMH	pelgrom coefficient capacitor mismatch	0.22	%µm

3. Parameters → 3.55 DMIMH3 module

3.55 DMIMH3 module

3.55.1 Device parameters

cdmmh5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIMH5	cdmmh5 breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_DMIMH5B	cdmmh5 area capacitance @ Vbias=0V	3.5	4.1	4.7	5.3	5.9	fF/µm²
CAP_DMIMH5	cdmmh5 perimeter capacitance	-	-	220	-	-	aF/µm
IL_DMIMH5	cdmmh5 leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCDMIMH5	cdmmh5 temperature coefficient	-	-	47	-	-	1e-06/K
THD_DMIMH5B	cdmmh5 equivalent dielectric thickness @ Er=7.3	-	-	13.8	-	-	nm
VC1_DMIMH5	cdmmh5 capacitor voltage coefficient 1	-	-	-20	-	-	ppm/V
Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.							
VC2_DMIMH5	cdmmh5 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_DMIMH	pelgrom coefficient capacitor mismatch	0.22	%µm

cdmmh5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_DMIMH5T	cdmmh5t breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_DMIMH5TB	cdmmh5t area capacitance @ Vbias=0V	3.5	4.1	4.7	5.3	5.9	fF/µm²
CAP_DMIMH5T	cdmmh5t perimeter capacitance	-	-	220	-	-	aF/µm
IL_DMIMH5T	cdmmh5t leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCCDMIMH5T	cdmmh5t temperature coefficient	-	-	47	-	-	1e-06/K

3. Parameters → 3.55 DMIMH3 module → 3.55.1 Device parameters → cdmmh5t → Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
THD_DMIMH5TB	cdmmh5t equivalent dielectric thickness @ Er=7.3	-	-	13.8	-	-	nm
VC1_DMIMH5T	cdmmh5t capacitor voltage coefficient 1	-	-	-20	-	-	ppm/V
	Note: As the capacitors' connections are cross-coupled, the linear voltage coefficient term is small.						
VC2_DMIMH5T	cdmmh5t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_DMIMH	pelgrom coefficient capacitor mismatch	0.22	%μm

3. Parameters → 3.56 TMIMH module

3.56 TMIMH module

3.56.1 Device parameters

ctmmh5

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_TMIMH5	ctmmh5 breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_TMIMH5B	ctmmh5 area capacitance @ Vbias=0V	5.25	6.15	7.05	7.95	8.85	fF/µm²
CAP_TMIMH5	ctmmh5 perimeter capacitance	-	-	300	-	-	aF/µm
IL_TMIMH5	ctmmh5 leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCC_TMIMH5	ctmmh5 temperature coefficient	-	-	47	-	-	1e-06/K
THD_TMIMH5B	ctmmh5 equivalent dielectric thickness @ Er=7.3	-	-	9.2	-	-	nm
VC1_TMIMH5	ctmmh5 capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_TMIMH5	ctmmh5 capacitor voltage coefficient 2	-	-	35	-	-	ppm/V²

Matching parameters

Name	Description	Typ	Unit
AC_TMIMH	pelgrrom coefficient capacitor mismatch	0.17	%µm

ctmmh5t

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-bulk	-40°C to 175°C	-460	-420	420	460	V
Vterm1-Vterm2	-40°C to 175°C	-7	-5.5	5.5	7	V

Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
BDO_TMIMH5T	ctmmh5t breakdown voltage @ Ibr=0.6µA	10	-	-	-	-	V
Note: The limits of this pass/fail parameter do not reflect the statistics of the process							
CAA_TMIMH5TB	ctmmh5t area capacitance @ Vbias=0V	5.25	6.15	7.05	7.95	8.85	fF/µm²
CAP_TMIMH5T	ctmmh5t perimeter capacitance	-	-	300	-	-	aF/µm
IL_TMIMH5T	ctmmh5t leakage current @ VL=7V	-	-	-	10	-	fA/µm²
TCC_TMIMH5T	ctmmh5t temperature coefficient	-	-	47	-	-	1e-06/K

3. Parameters → 3.56 TMIMH module→ 3.56.1 Device parameters→ ctmmh5t→ Process parameters

Name	Description	LSL	Low	Typ	High	USL	Unit
THD_TMIMH5TB	ctmmh5t equivalent dielectric thickness @ Er=7.3	-	-	9.2	-	-	nm
VC1_TMIMH5T	ctmmh5t capacitor voltage coefficient 1	-	-	-120	-	-	ppm/V
VC2_TMIMH5T	ctmmh5t capacitor voltage coefficient 2	-	-	35	-	-	ppm/V ²

Matching parameters

Name	Description	Typ	Unit
AC_TMIMH	pelgrom coefficient capacitor mismatch	0.17	%μm

3. Parameters → 3.57 CSP5L module

3.57 CSP5L module

3.57.1 Device parameters

csp5tl_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-HW ⁽¹⁾	-40°C to 175°C	-	-1.5	400	440	V
Vterm-NB ⁽²⁾⁽¹⁾	-40°C to 175°C	-410	-375	1	1.5	V
Vterm1-Vterm2	-40°C to 175°C	-330	-300	300	330	V

Note 1 In this instance, the node Vterm is the one which is connected to DIFF

Note 2 This voltage is achievable when used in conjunction with dhw5d diode. If other dhw* diodes are used, then Min (or Abs. min) Vterm-NB = Min (or Abs. min) Vanode-Vcathode of the selected diode.

Process parameters

Name	Description	Low	Typ	High	Unit
CAA_SP5TL	active/ metal1/ metal2/ metal3/ metal4/ top metal/ thick metal area capacitance	0.26	0.29	0.32	fF/μm ²
CAP_SP5TL	active/ metal1/ metal2/ metal3/ metal4/ top metal/ thick metal perimeter capacitance	-	0.118	-	fF/μm
IL_SP5TL	csp5tl leakage current @ VL=375V	-	-	20	pA/μm ²
TC1_SP5TL	csp5tl temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

csp5tla_3

Operating conditions

Name	Temp. range	Abs. min	Min	Max	Abs. max	Unit
Vterm-HW ⁽¹⁾	-40°C to 175°C	-	-1.5	400	440	V
Vterm-NB ⁽²⁾⁽¹⁾	-40°C to 175°C	-410	-375	1	1.5	V
Vterm1-Vterm2	-40°C to 175°C	-440	-400	400	440	V

Note 1 In this instance, the node Vterm is the one which is connected to DIFF

Note 2 This voltage is achievable when used in conjunction with dhw5d diode. If other dhw* diodes are used, then Min (or Abs. min) Vterm-NB = Min (or Abs. min) Vanode-Vcathode of the selected diode.

Process parameters

Name	Description	Low	Typ	High	Unit
CAA_SP5TLA	active/ metal2/ metal4/ thick metal area capacitance	0.06	0.07	0.08	fF/μm ²
CAP_SP5TLA	active/ metal2/ metal4/ thick metal perimeter capacitance	-	0.05	-	fF/μm
IL_SP5TLA	csp5tla leakage current @ VL=375V	-	-	10	pA/μm ²
TC1_SP5TLA	csp5tla temperature coefficient 1 @ Tnom=27°C	-	-70	-	1e-06/K

3. Parameters → 3.58 CEEPROM module

3.58 CEEPROM module

Ready-to-use CEEPROM or CEELATCH IP blocks are available for CEEPROM module. The parameters and characteristics of the CEEPROM/CEELATCH IP blocks are described in the corresponding block specification.

The parameters of special devices only used inside the non-volatile memory IP blocks are not described in this specification. Special additional tests are performed for the quality monitoring of the non-volatile memories.

3. Parameters → 3.59 NVM module

3.59 NVM module

Ready-to-use SONOS based non-volatile memory blocks are available for NVM module (FLASH and EEPROM).

The parameters of layers and devices only used for the non-volatile memories are not described in this specification. Special additional tests are performed for the quality monitoring of the non-volatile memories.

The parameters and characteristics of the different non-volatile IP blocks are described in the corresponding IP block specifications

3. Parameters → 3.60 OTP5 module

3.60 OTP5 module

Ready-to-use trim OTP blocks are available for OTP5 module (compiler). The parameters and characteristics of the OTP IP blocks are described in the corresponding block specification.

The parameters of special devices only used inside the non-volatile memory IP blocks are not described in this specification. Special additional tests are performed for the quality monitoring of the non-volatile memories.

3. Parameters → 3.61 BOTDIE module

3.61 BOTDIE module

3.61.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
DST_BD	BOTDIE polyimide dielectric strength	-	377	-	V/ μ m
EPS_BD	BOTDIE polyimide dielectric constant	-	3.3	-	-
TH_BD	BOTDIE polyimide thickness	3.5	5	6.5	μ m

3. Parameters → 3.62 FLATPV module

3.62 FLATPV module

For the FLATPV module, a planar passivation layer is offered as an alternative to the standard passivation, which is non-planar. The passivation thickness above the top metal layer is unchanged, refer to parameter THV. This alternative passivation scheme may be suitable for post-processing or packaging solutions requiring planar passivation. Primitive devices are not defined for the FLATPV module.

3.62.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
THV_FLAT	passivation thickness with FLATPV module	1470	1750	2030	nm
Note: Passivation is composed from the following stack (bottom to top): silicon oxide/silicon nitride					

3. Parameters → 3.63 SMALLPAD module

3.63 SMALLPAD module

There are no additional parameters for this module.

3. Parameters → 3.64 PIMIDE module

3.64 PIMIDE module

For the PIMIDE module, an additional resilient barrier layer on top of the passivation is applied. This overcoat of polyimide gives an improved passivation protection and stress relief of the chip.
Primitive devices are not defined for the PIMIDE module.

3.64.1 Device independent parameters

Structural and geometrical parameters

Name	Description	Low	Typ	High	Unit
THV_PMD	Polyimide thickness	3000	4000	5000	nm

3. Parameters → 3.65 Measurement principles

3.65 Measurement principles

ABT Pelgrom coefficient for MOSFET gain factor mismatch

The gain factor (BETA) of identically designed MOSFET transistor pairs is calculated from the maximum IDS slope (transconductance) divided by the applied drain voltage. The standard deviation of the relative gain factor mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

AC_ Pelgrom coefficient for capacitance mismatch

A floating gate measurement technique with a source follower at the (floating) middle node of a capacitive voltage divider is used for the determination of the relative capacitance mismatch of identically designed capacitor pairs. By applying two input voltages (typical values Vlow= 0.5V, Vhigh= 3.5V) and measuring the corresponding output voltages at the source of the p- channel transistor a slope S1 can be determined. After exchanging the nodes of the voltage divider a second slope S2 can be measured. The resulting capacitor mismatch is defined by:

$$\frac{\Delta C}{C} = 2 \cdot \frac{S1 - S2}{S1 + S2} = \frac{C1 - C2}{C1 + C2}$$

The standard deviation of the relative capacitance mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

AID Pelgrom coefficient for MOSFET drain current mismatch

The relative drain current mismatch of identically designed MOSFET transistor pairs is calculated from drain current measurements. The measurements IDS vs VGS-VTO (gate overdrive) are performed in the saturation region, with a VDS which matches the device voltage class but never exceeds 5V and at dedicated values for VGS-VTO. The standard deviation of the relative drain current mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient for selected gate overdrive voltages.

AR_ Pelgrom coefficient for resistance mismatch

The relative resistance mismatch of identically designed resistor pairs is calculated from resistance measurements with constant current density for all devices of one type with regard to the maximum allowed terminal voltage and current density. The standard deviation of the relative resistor mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

AVT Pelgrom coefficient for MOSFET threshold voltage mismatch

The linearly extrapolated threshold voltage of identically designed MOSFET transistor pairs is determined by linear regression around the IDS/VGS-point of maximum IDS slope. The intercept with the x- axis minus half the drain voltage is taken as VTO. The standard deviation of the absolute threshold voltage mismatch for selected device geometries is plotted versus the inverse square root of the device area. The slope of a linear regression through the origin of coordinates delivers the pelgrom coefficient.

BCE Collector-emitter breakdown voltage

The collector-emitter voltage is swept until the collector current reaches a defined value at the breakdown voltage BCE. The measurement is either performed with the base open (BCEO) or shorted (BCES) All other terminals are floating.

BDO Oxide breakdown

The voltage of the capacitor is swept until a defined current is reached at the breakdown voltage BV, or until the voltage limit is reached

3. Parameters → 3.65 Measurement principles

BDS Drain-source breakdown voltage

Source and substrate are connected to ground, specified gate voltage is applied, for VG=0V gate is also connected to ground. The drain voltage is swept until the current reaches the specified drain current at the breakdown voltage BDS or until the voltage limit is reached.

Note for BDSNHS10S, BDSNHS16CS, BDSNHS1A13S, BDSNHS1A16S, BDSNHS1A20S, BDSNHS1A28S, BDSNHS1B10S, BDSNHS1B2S, BDSNHS1B4S, BDSNHS1B5S, BDSNHS1B7S, BDSNHS1B8S, BDSNHS7S

Source and HWP are connected to ground, the specified gate voltage is applied, for VG=0V gate is also connected to ground. Drain and NBUR are tied and the voltage is swept until the current reaches the specified drain current at the breakdown voltage BDS or until the voltage limit is reached.

Note for BDSNHVRA, BDSNHVRB, BDSNHVRC, BDSNHVRD, BDSNHVRE, BDSNHVRF, BDSNHVTA, BDSNHVTAA, BDSNHVTB, BDSNHVU, BDSNMVA, BDSNMVAA, BDSNMVAB, BDSNMVB, BDSNMVC, BDSNMVD, BDSNMVE, BDSNMVF

Source and HWP are connected to ground, the specified gate voltage is applied, for VG=0V gate is also connected to ground. The drain voltage is swept until the current reaches the specified drain current at the breakdown voltage BDS or until the voltage limit is reached.

Note for BDSPHS10S, BDSPHS16CS, BDSPHS1A10S, BDSPHS1A13S, BDSPHS1A16S, BDSPHS1A20S, BDSPHS1A31S, BDSPHS1A4S, BDSPHS1A5S, BDSPHS1A7S, BDSPHS1A8S, BDSPHS2B10S, BDSPHS2B13S, BDSPHS2B16S, BDSPHS2B7S, BDSPHS2B8S, BDSPHS7S

Drain and HWP are connected to ground. Source, gate and NBUR are tied and the voltage is swept until the current reaches the specified drain current at the breakdown voltage BDS or until the voltage limit is reached.

Note for BDSPHVRA, BDSPHVRB, BDSPHVRC, BDSPHVRD, BDSPHVRE, BDSPHVRF, BDSPHVTAA, BDSPHVTB, BDSPHVU

Drain and HWP are connected to ground. Source and gate are tied and the voltage is swept until the current reaches the specified drain current at the breakdown voltage BDS or until the voltage limit is reached

BEB Emitter-base breakdown voltage

The emitter-base voltage is swept until the emitter current reaches the defined value at the breakdown voltage BEB. The measurement is either performed with the collector open (BEBO) or shorted (BEBS). All other terminals are floating.

BEC Emitter-collector breakdown voltage

Collector is connected to 0V and base is open. The specified current is forced into the emitter and the emitter voltage BEC is measured.

Note for BECNISJ16

Collector is connected to 0V. The specified current is forced into the emitter and the emitter voltage BEC is measured.

BEX Temperature exponent of mobility

The gain factor KP is measured as a function of the temperature T. The temperature exponent of mobility BEX is calculated from the slope of the linear regression:

$$VTO(T) = VTO(T_0) + TCV \cdot (T - T_0)$$

$$\ln [KP(T)] = \ln [KP(T_0)] + BEX \cdot [\ln(T) - \ln(T_0)]$$

BVI IGBT collector-emitter breakdown voltage

Emitter, Gate and HWP are connected to ground. Collector and NBUR are tied and the voltage is swept until the current reaches the specified collector current at the breakdown voltage BVI, or until the voltage limit is reached.

BVJ Diode junction breakdown voltage

The diode reverse voltage is swept until the diode reverse current reaches the specified current at the breakdown voltage BV, or until the voltage limit is reached. The BV values are valid for T0 = 27°C. The well to substrate breakdown is dominated by the diffusion to substrate breakdown if the well enclosure of the diffusion is not sufficient.

BVR Reverse breakdown voltage

Anode and HWP are connected to ground. Cathode and NBUR are tied together and the voltage is swept until the current reaches the specified drain current at the breakdown voltage BVR, or until the voltage limit is reached.

3. Parameters → 3.65 Measurement principles

BVT Trench breakdown voltage

One silicon tub is connected to ground. The voltage at the adjacent silicon tub (single DTI) or alternate silicon tub (double DTI) is swept until the tub current reaches the specified value at the breakdown voltage BV or until the voltage limit is reached.

BV_ Diode breakdown voltage

The diode reverse voltage is swept until the diode reverse current reaches the specified current at the breakdown voltage BV.

Note for BV_DFWDN5, BV_DFWDNB, BV_DFWDNC, BV_DFWDND, BV_DFWDNHC, BV_DFWDNHD, BV_DFWDNHE, BV_DFWDNHF, BV_DFWDNT, BV_DFWDNU

Anode and HWP are connected to ground. The Cathode voltage is swept until the current reaches the specified current at the breakdown voltage BV or until the voltage limit is reached.

CAA Area capacitance

The capacitance is measured at specified voltage and calculated per area.

CAP Perimeter capacitance

The fringing capacitance per length (one edge) of a single minimum width interconnect line is calculated using EDA field solver tools. Adjacent structures reduce this value.

CA_ Capacitance

The capacitance is measured at specified bias voltage.

Note for CA_CIF3, CA_CIF3A, CA_CIF4, CA_CIF4A, CA_CIF5, CA_CIF5A, CA_CIFT4, CA_CIFT4A, CA_CIFT5, CA_CIFT5A, CA_CIFT6, CA_CIFT6A, CA_SF3A_B, CA_SF3_B, CA_SF4A_B, CA_SF4_B, CA_SF5A_B, CA_SF5_B, CA_SFP2_B, CA_SFP3_B, CA_SFT4A_B, CA_SFT4_B, CA_SFT5A_B, CA_SFT5_B, CA_SFT6A_B, CA_SFT6_B

The capacitance for an array of capacitors is measured and the capacitance is quoted for a single cell.

CC_ Coupling Capacitance

The coupling capacitance per length of adjacent metal or poly lines with minimum separation is calculated using EDA field solver tools. Note, that in the case of adjacent lines the coupling capacitance dominates the fringing capacitance of the line.

CGA Oxide area capacitance

The capacitance per area of a large area capacitor is measured at specified bias voltage and calculated per area.

CGO Gate overlap capacitance

Gate to Source/Drain overlap capacitances are derived from C-V measurements of long perimeter structures ($W/L \gg 1$) and may differ from MOS model values. The model is adjusted to match measured switching performance.

CJA Area Junction capacitance

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

3. Parameters → 3.65 Measurement principles

CJP Perimeter junction capacitance

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

CNV Varactor capacitance at negative voltage

The specified terminal voltage is applied and the corresponding capacitance value C is measured at the specified frequency.

CPA Parasitic area capacitance

The dielectric, polysilicon and metal thicknesses are measured. The thickness values are then used by EDA field solver tools to calculate the capacitance of a large area capacitor.

CPP Parasitic perimeter capacitance

The fringing capacitance per length (one edge) of a single minimum width interconnect line is calculated using EDA field solver tools. Adjacent structures reduce this value.

CPV Varactor capacitance at positive voltage

The specified terminal voltage is applied and the corresponding capacitance value C is measured at the specified frequency.

DLT transistor delta length

The delta length is used for the calculation of effective length, according to the measurement principle for effective transistor channel length (refer to the note for LEF)

DST Dielectric strength

The dielectric strength is taken from the vendor specification.

DWR resistor delta width

The delta width is used in the calculation of the resistor mismatch pelgrom coefficient. It is determined according to the measurement principle for effective width (refer to the note for WER)

DWT transistor delta width

The delta width is used for the calculation of effective width, according to the measurement principle for effective transistor channel width (refer to the note for WEF)

3. Parameters → 3.65 Measurement principles

EOF Turn-off time and energy

The device under test is measured with an inductive clamping switching circuit. The on current before switch off is 150mA which is determined by V_{bus1} and pulse length. The turn-off energy EOF at time T_n is calculated from the following formula :

$$EOF_{T_n} = IC_{T_n}VC_{T_n}(T_n - T_{n-1})$$

The total switch-off energy is the integral of the energy over time TOF

$$EOF = \int_{t_{switchoff}}^{t_{off}} EOF_{tn} dt$$

Note for EOFNISJ16, EOFNISJ16HT

Inductive clamping switching circuit is used for turn-off energy loss and time measurement at wafer level

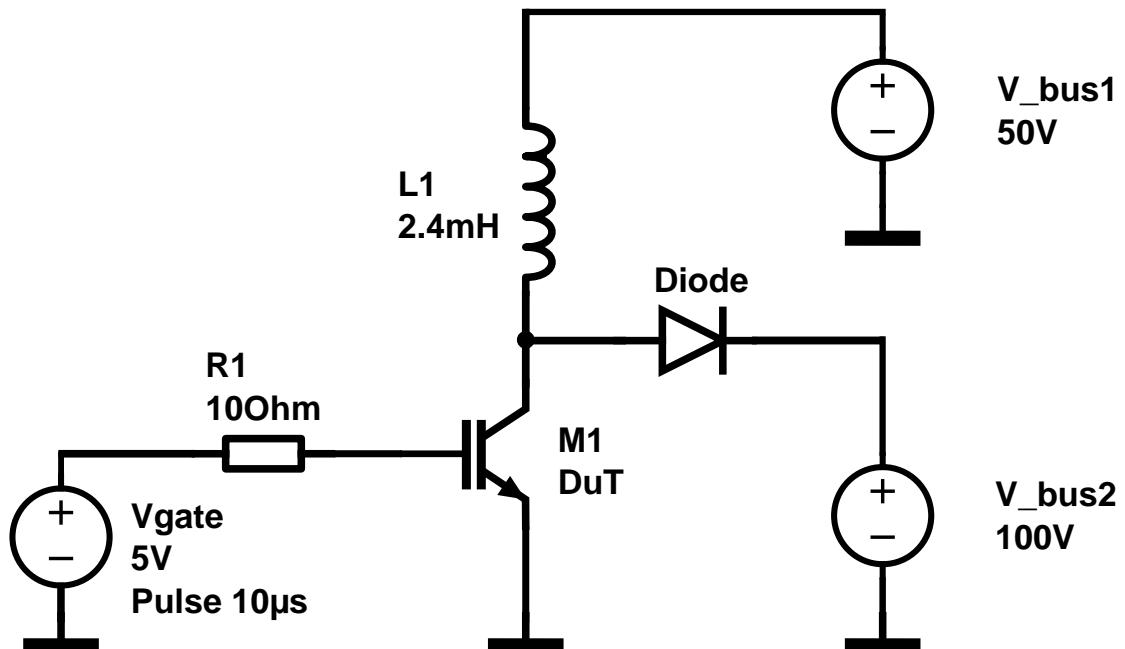


Figure 3.112 inductive clamping switching circuit

EPS Epsilon

The dielectric constant ϵ for a material is taken from published values. For dielectrics made from a stack of composite materials, the value is estimated based on the values of ϵ for the individual materials and their relative thickness in the stack.

EVF Early voltage forward

The emitter (and substrate, if applicable) are connected to 0V. The specified current I_B is forced in to the base. The collector voltage V_C is swept and the current I_C is measured, in order to find the minimum slope of the collector current as a function of the collector voltage. A tangent is taken from this slope. The early voltage is measured as the abscissa at the x-axis intercept of this tangent.

FC_ corner frequency

The corner frequency is the frequency at which the flicker noise density equals the thermal noise density. The operating point is taken at the specified drain voltage while the gate is forced to achieve the specified drain current. Source and body are connected to ground.

FT_ Transit frequency

The transit frequency is extracted from S-parameter measurements

3. Parameters → 3.65 Measurement principles

GAM **Gamma**

The threshold voltages VTX as a function of substrate bias voltage are extracted as described in the corresponding measurement note for VTX. The body factor GAMMA is then extracted from the slope of VT as a function of $\sqrt{2 \cdot PHI - VBS}$ by linear regression:

$$VTX = VT + GAMMA \cdot (\sqrt{2 \cdot PHI - VBS} - \sqrt{2 \cdot PHI})$$

The effective bulk doping concentration NSUB is calculated from GAMMA and COX (refer to measurement note regarding Oxide capacitance / Oxide thickness):

$$GAMMA = \frac{\sqrt{2 \cdot \epsilon_0 \cdot \epsilon_{Si} \cdot q \cdot NSUB}}{COX}$$

The Fermi potential PHI is a function of the doping concentration NSUB and the intrinsic carrier concentration NI

$$PHI = \frac{kT}{q} \cdot \ln \frac{NSUB}{NI}$$

PHI is recalculated using the extracted value of NSUB. This updated value of PHI is then used again in the extraction of GAMMA and NSUB in an iterative procedure.

GA_

Body factor

The threshold voltages VTX as a function of substrate bias voltage are extracted as described in the corresponding measurement note for VTX. The body factor GAMMA is then extracted from the slope of VT as a function of $\sqrt{2 \cdot PHI - VBS}$ by linear regression:

$$VTX = VT + GAMMA \cdot (\sqrt{2 \cdot PHI - VBS} - \sqrt{2 \cdot PHI})$$

The effective bulk doping concentration NSUB is calculated from GAMMA and COX (refer to measurement note regarding Oxide capacitance / Oxide thickness):

$$GAMMA = \frac{\sqrt{2 \cdot \epsilon_0 \cdot \epsilon_{Si} \cdot q \cdot NSUB}}{COX}$$

The Fermi potential PHI is a function of the doping concentration NSUB and the intrinsic carrier concentration NI

$$PHI = \frac{kT}{q} \cdot \ln \frac{NSUB}{NI}$$

PHI is recalculated using the extracted value of NSUB. This updated value of PHI is then used again in the extraction of GAMMA and NSUB in an iterative procedure.

HFH

Forward gain; high current

Base and collector are connected to 0V. The specified emitter current is forced. This is normally at a point above the current used to achieve the maximum gain. Base and collector current are measured. The gain HF is calculated as IC/IB.

HFL

Forward gain; low current

Base and collector are connected to 0V. The specified emitter current is forced. This is normally at a point below the current used to achieve the maximum gain. Base and collector current are measured. The gain HF is calculated as IC/IB.

HF_

Forward current gain

Base and collector are connected to 0V. The specific emitter current is forced. Base and collector current are measured. The gain HF is calculated as IC/IB.

Note for HF_PA, HF_PA5, HF_PB, HF_PB5, HF_PC, HF_PC5, HF_PE, HF_PE5, HF_PF, HF_PF5, HF_PG, HF_PG5

The gain HF is calculated as -IE/IB -1

ICE

collector current

The gate and collector are forced to specified voltages. Emitter and bulk are connected to ground. The transistor maximum collector current ICM is measured at collector. ICM is specified per drawn transistor width

3. Parameters → 3.65 Measurement principles

ICP Pulsed collector current

The pulsed collector current is measured with gate and collector at the specified voltages. Emitter and bulk are connected to ground. The gate is forced with the specified pulse width and duty cycle. The pulsed collector current ICP is measured at the collector and specified per drawn transistor width

ID0 Saturation current

The gate is set to 0V and drain are forced to the specified voltage. Source and bulk are connected to ground. The transistor saturation current IDS is measured at the drain. ID0 is specified per drawn transistor width.

ID5 Saturation current

The gate and drain are forced to the specified voltages. Source and bulk are connected to ground. The transistor saturation current IDS is measured at the drain. ID5 is specified per drawn transistor width.

Note for ID5NHS10S, ID5NHS16CS, ID5NHS1A13S, ID5NHS1A16S, ID5NHS1A20S, ID5NHS1A28S, ID5NHS1B10S, ID5NHS1B2S, ID5NHS1B4S, ID5NHS1B5S, ID5NHS1B7S, ID5NHS1B8S, ID5NHS7S

These parameters are measured in low side with measurement conditions NBUR[V] = Max VDS and HWP[V] = 0

Note for ID5PHS10S, ID5PHS16CS, ID5PHS1A10S, ID5PHS1A13S, ID5PHS1A16S, ID5PHS1A20S, ID5PHS1A31S, ID5PHS1A4S, ID5PHS1A5S, ID5PHS1A7S, ID5PHS1A8S, ID5PHS2B10S, ID5PHS2B13S, ID5PHS2B16S, ID5PHS2B7S, ID5PHS2B8S, ID5PHS7S

These parameters are measured in high side with measurement conditions NBUR[V] = 0 and HWP = - max VDS

IDF Forward current

The forward current is measured at the specified forward voltage

IDL Drain current

The gate and drain are forced to the specified voltages. Source and bulk are connected to ground. The transistor current IDL is measured at the drain. IDL is specified per drawn transistor width.

IDP Pulsed drain current

The pulsed drain current is measured with gate and drain at the specified voltages. Source and bulk are connected to ground. The gate is forced with the specified pulse width and duty cycle. The pulsed drain current IDP is measured at the drain and specified per drawn transistor width

Note for IDPNHS10S, IDPNHS16CS, IDPNHS1A13S, IDPNHS1A16S, IDPNHS1A20S, IDPNHS1A28S, IDPNHS1B10S, IDPNHS1B2S, IDPNHS1B4S, IDPNHS1B5S, IDPNHS1B7S, IDPNHS1B8S, IDPNHS7S

These parameters are measured in low side with measurement conditions NBUR[V] = Max VDS and HWP[V] = 0

Note for IDPPHS10S, IDPPHS16CS, IDPPHS1A10S, IDPPHS1A13S, IDPPHS1A16S, IDPPHS1A20S, IDPPHS1A31S, IDPPHS1A4S, IDPPHS1A5S, IDPPHS1A7S, IDPPHS1A8S, IDPPHS2B10S, IDPPHS2B13S, IDPPHS2B16S, IDPPHS2B7S, IDPPHS2B8S, IDPPHS7S

These parameters are measured in high side with measurement conditions NBUR[V] = 0 and HWP = - max VDS

IDS Saturation current

The gate and drain are forced to the specified voltages. Source and bulk are connected to ground. The transistor saturation current IDS is measured at the drain. IDS is specified per drawn transistor width.

ILA Diode Area Leakage Current

The specified reverse voltage is applied at the specified temperature. The diode leakage current IS is measured for diodes with different area to perimeter ratios. The leakage current per drawn area ILA and the leakage current per drawn perimeter ILP are then calculated from

$$IS = ILA \cdot W \cdot L + ILP(2 \cdot W + 2 \cdot L)$$

The values may not be applicable to junction diodes as part of other devices (e.g. MOS).

ILP Diode Perimeter Leakage Current

The specified reverse voltage is applied at the specified temperature. The diode leakage current IS is measured for diodes with different area to perimeter ratios. The leakage current per drawn area ILA and the leakage current per drawn perimeter ILP are then calculated from

$$IS = ILA \cdot W \cdot L + ILP(2 \cdot W + 2 \cdot L)$$

The values may not be applicable to junction diodes as part of other devices (e.g. MOS).

3. Parameters → 3.65 Measurement principles

IL_ Leakage current

The specified voltage VL is applied to high terminal(s), 0V is applied to low terminal(s). The leakage current between high and low terminal(s) is measured.

Note for IL_DNSJ10, IL_DNSJ10HT, IL_DNSJ16C, IL_DNSJ16CHT, IL_DNSJ1A13, IL_DNSJ1A13HT, IL_DNSJ1A16, IL_DNSJ1A16HT, IL_DNSJ1A20, IL_DNSJ1A20HT, IL_DNSJ1A28, IL_DNSJ1A28HT, IL_DNSJ1B10, IL_DNSJ1B10HT, IL_DNSJ1B2, IL_DNSJ1B2HT, IL_DNSJ1B4, IL_DNSJ1B4HT, IL_DNSJ1B5, IL_DNSJ1B5HT, IL_DNSJ1B7, IL_DNSJ1B7HT, IL_DNSJ1B8, IL_DNSJ1B8HT, IL_DNSJ7, IL_DNSJ7HT

These parameters are measured in low side operation with measurement conditions NBUR[V] = max VAC and HWP[V] = 0.

IOF Off current

A given voltage is applied to drain, all other transistor terminals are on ground. The drain leakage current is measured as IOF. IOF is normally specified per drawn transistor width

IOI off state leakage current for IGBT

A given voltage is applied to collector , all other transistor terminals are on ground. The collector leakage current is measured as IOI. IOI is normally specified per drawn transistor width

ISB Bulk current

A specified drain voltage is applied to the drain, the gate voltage is swept from Vlow to Vhigh within the allowed operating range in order to find the maximum bulk current ISB. ISB is specified per drawn transistor width.

KP_ Gain factor (beta)

The gain factor is measured along with the threshold voltage. The maximum slope referred in VTX measuring principle is the transconductance. This figure is divided by the applied drain voltage to calculate the gain factor.

LEF Effective transistor channel length

The effective gain factor KP' = KP · Weff / Leff is measured for a L - array of wide transistors according to threshold voltage measurement (refer to notes for VTX and KP_). The length reduction DL = L - Leff is calculated from the x-intercept of the linear regression:

$$\frac{1}{KP'} = \frac{1}{KP \cdot Weff} \cdot (L - DL)$$

MJA Area grading coefficient

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

3. Parameters → 3.65 Measurement principles

MJP Sidewall grading coefficient

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

NOI**input referred noise**

The input gate referred 1/f noise spectral density at the specified frequency is quoted, normalised to a specified active gate area. The operating point is taken at the specified drain voltage while the gate voltage is forced to achieve the specified drain current. Source and body are connected to ground.

OSV**On state voltage drop**

Gate voltage is forced as specified. The collector-emitter voltage at the specified collector current is measured.

PBA**Area junction potential**

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

3. Parameters → 3.65 Measurement principles

PBP Perimeter junction potential

The junction capacitances C of diodes with different area to perimeter ratios are measured as a function of the reverse bias voltage V. The junction capacitance parameters are then extracted from:

$$C = \frac{W \cdot L \cdot CJA}{(1 + \frac{V}{PBA})^{MJA}} + \frac{2 \cdot (W + L) \cdot CJP}{(1 + \frac{V}{PBP})^{MJP}}$$

Parameter	Description
W	diode width
L	diode length
V	diode reverse voltage
PBA	area junction potential
PBP	sidewall junction potential
CJA	area capacitance
CJP	sidewall capacitance
MJA	area grading coefficient
MJP	sidewall grading coefficient

RCT Contact resistance

The contact resistance is calculated from the resistance of a contact string divided by the number of contacts. For non-metal layers, except those which are silicided, the resistance between contacts is considered.

RHW Resistance of Handle Wafer contact

The handle wafer resistance is measured for two handle wafer contact resistors of specified width in series and spacing in-between where the current flows through the handle wafer

ROA On resistance

The area specific on resistance ROA is calculated as RO₀, RON or ROC multiplied by the minimum pitch for the device.

Note for ROANHS10, ROANHS10S, ROANHS16C, ROANHS16CS, ROANHS1A13S, ROANHS1A16S, ROANHS1A20S, ROANHS1A28S, ROANHS1B10S, ROANHS1B2S, ROANHS1B4S, ROANHS1B5S, ROANHS1B7S, ROANHS1B8S, ROANHS7, ROANHS7S

These parameters are measured in low side with measurement conditions NBUR[V] = Max VDS and HWP[V] = 0

Note for ROAPHS10, ROAPHS10S, ROAPHS16C, ROAPHS16CS, ROAPHS1A10S, ROAPHS1A13S, ROAPHS1A16S, ROAPHS1A20S, ROAPHS1A31S, ROAPHS1A4S, ROAPHS1A5S, ROAPHS1A7S, ROAPHS1A8S, ROAPHS2B10S, ROAPHS2B13S, ROAPHS2B16S, ROAPHS2B7S, ROAPHS2B8S, ROAPHS7, ROAPHS7S

These parameters are measured in high side with measurement conditions NBUR[V] = 0 and HWP = - max VDS

RON On resistance

A drain current is measured at the specified gate and drain voltages. The source and substrate are grounded. RON is calculated by the drain voltage divided by the drain current and multiplied by the transistor width.

3. Parameters → 3.65 Measurement principles

RO_ On resistance

A drain current is measured at the specified gate and drain voltages. The source and substrate are grounded. RO_ is calculated by the drain voltage divided by the drain current and multiplied by the transistor width.

Note for RO_5NISJ16

A collector current is measured at the specified gate and collector voltages. The emitter and substrate are grounded. RO_ is calculated by the collector voltage divided by the collector current and multiplied by the transistor width.

Note for RO_NHS10S, RO_NHS16CHS, RO_NHS16CS, RO_NHS1A13S, RO_NHS1A16S, RO_NHS1A20S, RO_NHS1A28S, RO_NHS1B10S, RO_NHS1B2S, RO_NHS1B4S, RO_NHS1B5S, RO_NHS1B7S, RO_NHS1B8S, RO_NHS7S

These parameters are measured in low side with measurement conditions NBUR[V] = Max VDS and HWP[V] = 0

Note for RO_NHS16CHS

These parameters are measured in high side operation with measurement conditions NBUR[V] = VD and HWP[V] = VD - maxVDS.

Note for RO_PHS10S, RO_PHS16CS, RO_PHS1A10S, RO_PHS1A13S, RO_PHS1A16S, RO_PHS1A20S, RO_PHS1A31S, RO_PHS1A4S, RO_PHS1A5S, RO_PHS1A7S, RO_PHS1A8S, RO_PHS2B10S, RO_PHS2B13S, RO_PHS2B16S, RO_PHS2B7S, RO_PHS2B8S, RO_PHS7S

These parameters are measured in high side with measurement conditions NBUR[V] = 0 and HWP = - max VDS

Note for RO_PHS16CLS, RO_PHS7LS

These parameters are measured in low side operation with measurement conditions NBUR[V] = VD + max VDS and HWP[V] = VD.

RP_ Programmed fuse resistance

A specified voltage is applied to the device. The fuse current is measured and the fuse resistance is calculated. The programming of poly fuse is performed according to the specified fusing conditions.

RSE Edge resistance

Connection from the silicided end region to the resistor body has a finite value. This is referred to as the SB edge resistance because it follows the line of the SB edge between the silicided and unsilicided resistor regions. The edge resistance varies inversely with resistor width. It arises from the contact resistance of the silicide to the doped silicon of the resistor body.

RSR Sheet resistance

A voltage VRES is applied to one terminal. The second terminal is connected to ground. In case of diffusion or well resistor measurements substrate or well is also connected to ground. The current IRES is measured at the first terminal. The measurements are performed for at least two widths W of long resistors (L_{eff} ~ L). The sheet resistance per square R is calculated from the slope and the width reduction DW = W - W_{eff} is calculated from the x-intercept of the linear regression:

$$\frac{IRES}{VRES} = \frac{1}{R \cdot L} \cdot (W - DW)$$

For metal sheet resistance, four terminal measurement structures are used.

RSS Sheet resistance

A voltage VRES is applied to one terminal. The second terminal is connected to ground. In case of diffusion or well resistor measurements substrate or well is also connected to ground. The current IRES is measured at the first terminal. RSS is calculated from number of drawn resistor squares.

RSW Start wafer resistivity

The resistivity of the start wafer material is taken from the wafer vendor specification

RU_ Unprogrammed fuse resistance

A specified current is forced into the device. The fuse voltage is measured and the fuse resistance is calculated.

RVI Via resistance

The via resistance is calculated from the resistance of a long via string divided by the number of vias.

3. Parameters → 3.65 Measurement principles

SIB Standard deviation for bipolar transistor base current mismatch

The standard deviation of the bipolar transistor base current mismatch is calculated using common statistical theory by assuming a normal distribution of the relative base current mismatch values of identically designed bipolar transistor pairs.

SIC Standard deviation for bipolar transistor collector current mismatch

The standard deviation of the bipolar transistor collector current mismatch is calculated using common statistical theory by assuming a normal distribution of the relative collector current mismatch values of identically designed bipolar transistor pairs.

STS Sub-threshold slope

The gate voltage is swept with the drain held at given drain voltage and the source and substrate grounded. STS is the maximum slope of the $\log_{10}(I_d/W)$ versus V_g plot.

SVB Standard deviation for bipolar transistor base emitter voltage mismatch

The standard deviation of the bipolar base emitter voltage mismatch is calculated using common statistical theory by assuming a normal distribution of the absolute base emitter voltage mismatch values of identically designed bipolar transistor pairs.

TC1 Linear temperature coefficient

Variable x is measured as a function of the temperature T. The temperature dependence is modelled using the following formula:

$$x = x_0(T_{nom}) [1 + TC1(T - T_{nom}) + TC2(T - T_{nom})^2]$$

$x_0(T_{nom})$ is the room temperature value for x

TC1 and TC2 are the polynomial temperature coefficients

TC2 Quadratic temperature coefficient

Variable x is measured as a function of the temperature T. The temperature dependence is modelled using the following formula:

$$x = x_0(T_{nom}) [1 + TC1(T - T_{nom}) + TC2(T - T_{nom})^2]$$

$x_0(T_{nom})$ is the room temperature value for x

TC1 and TC2 are the polynomial temperature coefficients

TCC Capacitor temperature coefficient

The capacitance is measured as a function of temperature T. The temperature coefficient of the capacitance TCC is calculated from the slope of the following linear regression:

$$\frac{C(T)}{C(T_0)} = 1 + TCC \cdot (T - T_0)$$

$C(T_0)$ is the room temperature capacitance value

3. Parameters → 3.65 Measurement principles

TC_ Temperature coefficient

Variable x is measured as a function of the temperature T. The temperature coefficient TC of the variable x is calculated from the slope of the linear regression:

$$x(T) = x_0(T_{nom}) + TC(T - T_{nom})$$

x₀(T_{nom}) is the room temperature value for x

TC is the linear temperature coefficient

Note for TC_VDFDNSJ10, TC_VDFDNSJ16C, TC_VDFDNSJ1A13, TC_VDFDNSJ1A16, TC_VDFDNSJ1A20, TC_VDFDNSJ1A28, TC_VDFDNSJ1B10, TC_VDFDNSJ1B2, TC_VDFDNSJ1B4, TC_VDFDNSJ1B5, TC_VDFDNSJ1B7, TC_VDFDNSJ1B8, TC_VDFDNSJ7

These parameters are measured in low side operation with measurement conditions NBUR[V] = max VAC and HWP[V] = 0.

Note for TC_VTNHS10S, TC_VTNHS16CS, TC_VTNHS1A13S, TC_VTNHS1A16S, TC_VTNHS1A20S, TC_VTNHS1A28S, TC_VTNHS1B10S, TC_VTNHS1B2S, TC_VTNHS1B4S, TC_VTNHS1B5S, TC_VTNHS1B7S, TC_VTNHS1B8S, TC_VTNHS7S

These parameters are measured in low side with measurement conditions NBUR[V] = Max VDS and HWP[V] = 0

Note for TC_VTPHS10S, TC_VTPHS16CS, TC_VTPHS1A10S, TC_VTPHS1A13S, TC_VTPHS1A16S, TC_VTPHS1A20S, TC_VTPHS1A31S, TC_VTPHS1A4S, TC_VTPHS1A5S, TC_VTPHS1A7S, TC_VTPHS1A8S, TC_VTPHS2B10S, TC_VTPHS2B13S, TC_VTPHS2B16S, TC_VTPHS2B7S, TC_VTPHS2B8S, TC_VTPHS7S

These parameters are measured in high side with measurement conditions NBUR[V] = 0 and HWP = - max VDS

THD Dielectric thickness

Thickness may be measured either on large area test structures within the wafer fabrication process, or may be determined electrically from capacitance measurements. The parameter values describe thicknesses of fully prepared wafers. For some parameters, the monitoring of these thicknesses is performed by separate monitoring of all separate layers which generate the final layer. For electrical measurements, the capacitance CAA of a large area capacitor is measured. The dielectric thickness THD is then calculated from:

$$THD = \frac{\epsilon_0 \cdot \epsilon_r}{CAA}$$

THG Gate oxide thickness

The capacitance per area COX of a large area capacitor is measured. The oxide thickness TOX is calculated from:

(with $\epsilon_{ox} = 3.9$)

$$TOX = \frac{\epsilon_0 \cdot \epsilon_{ox}}{COX}$$

THO Oxide thickness

Thickness is measured on large area test structures within the wafer fabrication process. The parameter values describe thicknesses of fully prepared wafers. For some parameters, the monitoring of these thicknesses is performed by separate monitoring of all separate layers which generate the final layer.

THV Passivation Thickness

Thickness is measured on large area test structures within the wafer fabrication process. The parameter values describe thicknesses of fully prepared wafers. For some parameters, the monitoring of these thicknesses is performed by separate monitoring of all separate layers which generate the final layer.

TH_ Thickness

Measurements may be performed either within the wafer fabrication process, or from cross-sections after fabrication. The parameter values describe the thickness of fully prepared wafers. For some parameters, the values come from the wafer supplier specification.

TLL Trench leakage current per length

One silicon tub is connected to ground. The voltage at the adjacent silicon tub (single DTI) or alternate silicon tub (double DTI) is set to the specified voltage. The leakage current is measured at this terminal. It is specified per drawn trench length.

3. Parameters → 3.65 Measurement principles

TM_ Diode reverse recovery time

The reverse recovery time is extracted from transient measurements. The forward voltage equivalent to the specified forward current density is forced. This forward voltage is then switched to the specified reverse voltage. The diode current is traced. The parameter extraction is performed according to standard MIL-STD-750E METHOD 4031.3 for soft recovery

Note for TM_RRDNSJ10, TM_RRDNSJ16C, TM_RRDNSJ7

These parameters are measured in low side operation with measurement conditions NBUR[V] = max VAC and HWP[V] = 0.

TOF**Turn-off time and energy**

The device under test is measured with an inductive clamping switching circuit. The on current before switch off is 150mA which is determined by V_bus1 and pulse length. Turn-off time, TOF is the time between 10% max IAS and 90% max IAS

Note for TOFNISJ16, TOFNISJ16HT

Inductive clamping switching circuit is used for turn-off energy loss and time measurement at wafer level

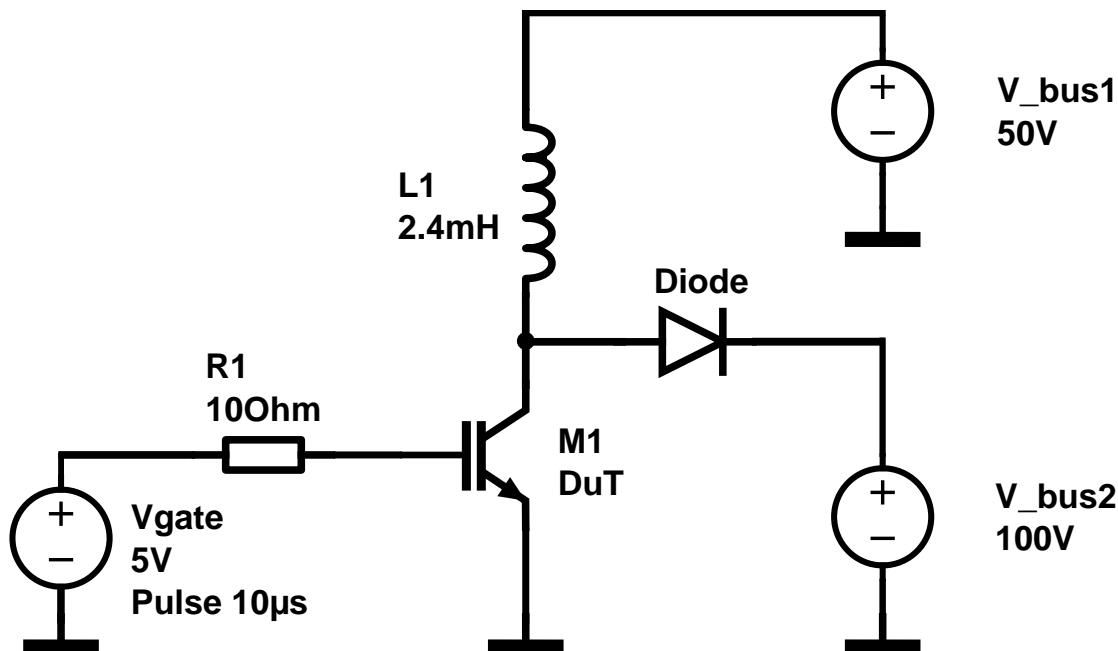


Figure 3.113 inductive clamping switching circuit

TUR**Tuning range**

The tuning range is the difference between the capacitance values at the specified voltages, expressed as a percentage.

U0_**Effective mobility**

The mobility U0_ is calculated from gain KP_ and gate oxide capacitance CGA:

$$U0 = \frac{KP}{CGA}$$

VBE**Base-emitter voltage**

The base, collector (and substrate, if applicable) are connected to 0V. The specified emitter current is forced into the emitter and the base-emitter voltage VBE is measured. For devices which have a gate connection, the specified voltage is applied to the gate. In some cases, an alternate method may be used; refer to device specific measurement notes.

3. Parameters → 3.65 Measurement principles

VC1 Linear voltage coefficient for capacitor

The capacitance C is measured as a function of the voltage V. The voltage dependence of a capacitor (V_{in} volts, $V_{nom} = 0V$) is modeled using the following formula:

$$C = C0(1 + VC1(V - V_{nom}) + VC2(V - V_{nom})^2)$$

$C0$ is the capacitance at $V = V_{nom}$ VC1 and VC2 are polynomial modeling coefficients.

VC2 Quadratic voltage coefficient for capacitor

The capacitance C is measured as a function of the voltage V. The voltage dependence of a capacitor (V_{in} volts, $V_{nom} = 0V$) is modeled using the following formula:

$$C = C0(1 + VC1(V - V_{nom}) + VC2(V - V_{nom})^2)$$

$C0$ is the capacitance at $V = V_{nom}$ VC1 and VC2 are polynomial modeling coefficients.

VCB Bulk voltage coefficient for resistor

The substrate or bulk voltage coefficient of a poly resistor is measured by applying bias voltage on to the bulk substrate, noted as node voltage v(3). The resistor terminal voltages are noted as v(1) and v(2) respectively. The slope for the voltage coefficient VCB of the sheet resistance is then calculated by linear regression method using a definition equation for the resistance:

$$R = R_0 \left[1 + VCB \frac{V_{(1,3)} + V_{(2,3)}}{2} \right]$$

VDF Forward voltage

A specified current is forced through the diode and the forward voltage is measured.

Note for VDFDNSJ10, VDFDNSJ16C, VDFDNSJ1A13, VDFDNSJ1A16, VDFDNSJ1A20, VDFDNSJ1A28, VDFDNSJ1B10, VDFDNSJ1B2, VDFDNSJ1B4, VDFDNSJ1B5, VDFDNSJ1B7, VDFDNSJ1B8, VDFDNSJ7

These parameters are measured in low side operation with measurement conditions NBUR[V] = max VAC and HWP[V] = 0.

VT1 Snap-back trigger voltage

Source and bulk are connected to ground. A static gate voltage VGS is applied at the gate. The output characteristic is measured by applying 100ns current pulses at the drain. At certain drain voltage the parasitic bipolar triggers, leading to device damage. This drain voltage defines the snap-back trigger voltage (or on-state breakdown voltage) VT1 at this particular gate bias.

Note for VT1NISJ16

Emitter and bulk are connected to ground. A static gate voltage VGS is applied at the gate. The output characteristic is measured by applying 100ns current pulses at the collector. At certain collector voltage the parasitic bipolar triggers, leading to device damage. This collector voltage defines the snap-back trigger voltage (or on-state breakdown voltage) VT1 at this particular gate bias.

VTA Side-gate threshold voltage

A rectangular PTUB is surrounded by PTUB's. Inside the main PTUB, two NWELL2's form the source and drain, the PWELL2 is the bulk. The adjacent PTUB's perpendicular to source and drain act as the (side) gate. The specified voltage is applied at the drain; source and bulk are connected to ground. The side-gate voltage is swept until the specified current flows from source to drain.

VTF Field threshold voltage

Drain is set to specified voltage. Source and bulk are connected to ground. The voltage at gate is swept until the current reaches a specified current density at the threshold voltage VTF.

VTG Back-gate threshold voltage

A rectangular PTUB is surrounded by PTUB's. Inside the main PTUB, two NWELL2's form the source and drain, the PTUB_SUB is the bulk. The adjacent PTUB's along the BULK, parallel to source and drain, together with the handle wafer, act as the (back) gate. The adjacent PTUB's perpendicular to source and drain act as the (side) gate. The specified voltage is applied at the drain; source, bulk and side-gate are connected to ground. The back-gate voltage is swept until the specified current flows from source to drain.

3. Parameters → 3.65 Measurement principles

VTI Constant current threshold voltage

The constant-current threshold voltage with zero substrate bias is measured as follows: The drain voltage is forced to VD, source and bulk are connected to ground. The gate voltage is swept until the drain current reaches Id at the threshold voltage VTI.

Note for VTINE5L, VTINE5S, VTINEL, VTINELL, VTINELSA, VTINELSSA, VTINES, VTINESS, VTINHVTA, VTINHVTAA, VTINHVTB, VTINHVU, VTIPE5L, VTIPE5S, VTIPE5TIL, VTIPE5TIS, VTIPEL, VTIPELL, VTIPELSA, VTIPELSSA, VTIPES, VTIPESS, VTIPETIL, VTIPETIS, VTIPETISS, VTIPHVTB, VTIPHVTB, VTIPHVU

The specific drain current Id is 0.1µA multiplied by (W/L).

Note for VTINISJ16

The constant-current turn on voltage of IGBT with zero substrate bias is measured as follows: The collector voltage is forced to VC, emitter and bulk are connected to ground. The gate voltage is swept until the collector current reaches Ic at the threshold voltage VTI.

The specific collector current Ic is 0.1µA multiplied by (W/L).

VTX**Extrapolated threshold voltage**

The linearly extrapolated threshold voltage with zero substrate bias is measured as follows: The drain voltage is forced to VD, all other terminals are connected to ground if not otherwise specified. The gate voltage is swept to find the maximum slope of the drain current as a function of the gate voltage. The voltage sweep is positive for n-channel devices and negative for p-channel devices. The intercept with the x-axis minus half the drain voltage VD/2 is taken as VT, the threshold voltage.

$$Id = \text{beta} \cdot Vd \cdot (Vg - Vt - \frac{Vd}{2})$$

Note for VTXNHS10, VTXNHS10S, VTXNHS16C, VTXNHS16CS, VTXNHS1A13S, VTXNHS1A16S, VTXNHS1A20S, VTXNHS1A28S, VTXNHS1B10S, VTXNHS1B2S, VTXNHS1B4S, VTXNHS1B5S, VTXNHS1B7S, VTXNHS1B8S, VTXNHS7, VTXNHS7S

These parameters are measured in low side with measurement conditions NBUR[V] = Max VDS and HWP[V] = 0

Note for VTXPHS10, VTXPHS10S, VTXPHS16C, VTXPHS16CS, VTXPHS1A10S, VTXPHS1A13S, VTXPHS1A16S, VTXPHS1A20S, VTXPHS1A31S, VTXPHS1A4S, VTXPHS1A5S, VTXPHS1A7S, VTXPHS1A8S, VTXPHS2B10S, VTXPHS2B13S, VTXPHS2B16S, VTXPHS2B7S, VTXPHS2B8S, VTXPHS7, VTXPHS7S

These parameters are measured in high side with measurement conditions NBUR[V] = 0 and HWP = - max VDS

WEF**Effective transistor channel width**

The effective gain factor KP' = KP · Weff/Leff is measured for a W – array of long transistors according to threshold voltage measurement (refer to notes for VTX and KP_). The width reduction DW = W – Weff is calculated from the x-intercept of the linear regression:

$$KP' = \frac{KP}{Leff} \cdot (W - DW)$$

WER**Effective width**

A voltage VRES is applied to one terminal. The second terminal is connected to ground. In case of diffusion or well resistor measurements substrate or well is also connected to ground. The current IRES is measured at first terminal. The measurements are performed for at least two widths W of long resistors (Leff ~ L). The width reduction DW = W - Weff is calculated from the x-intercept of the linear regression:

$$\frac{IRES}{VRES} = \frac{1}{R \cdot Leff} \cdot (W - DW)$$

For metal sheet resistance, four terminal Van Der Pauw measurement structures are used.

XJ_**Junction depth**

The junction depth is extracted from SIMS measurements. The measurements are performed on fully prepared wafers.

XT_**Trench depth**

The trench depth is measured by SEM cross-sections.

4. Process related guidelines

4.1 Matching Introduction

General matching information

This section presents fundamental parameters for description of matching behavior of MOS and bipolar transistors, resistors and capacitors. All matching parameters are information parameters and represent typical values only.

The matching parameters describe the short distance matching: the matching of two identically designed elements located close to each other (maximum distance about 120µm).

The stochastic matching between two parameters P1 and P2 measured at two identically designed elements is defined as the standard deviation of the normal distribution for:

- 1) absolute differences for threshold voltages, base-emitter voltage

$$\Delta P = (P_1 - P_2) \quad [mV]$$

- 2) relative differences for transistor currents, resistors, capacities

$$\frac{\Delta P}{P} = 200 \cdot \frac{P_1 - P_2}{P_1 + P_2} \quad [\%]$$

We assume that ΔP_i values are distributed normally with a variance σ^2 (squared standard deviation). The estimator μ of the distribution mean is close to zero except in the case of strong process parameter gradients or layout related asymmetries.

Matching measurements are performed for MOS transistors, bipolar transistors, resistors and capacitors at a temperature of 27°C. The following model describes the dependence of parameter matching on two identically designed devices with area ($W \cdot L$):

$$\sigma^2(P_1 - P_2) = \frac{A_p^2}{W \cdot L}$$

where A_p is the process-dependent matching parameter describing the area dependence.

Note: For the calculation of the transistor matching parameters A_p the effective channel lengths L_{eff} and the effective channel widths W_{eff} were used; for resistors the effective width W_{eff} and the drawn length L were used.

Note: The parameter differences are essential for matching characterization, not the absolute values of a parameter. Therefore sequential measurements with the same meters and multiple measurements (5 times for VTO and gain, 10 times for R and ΔC) of each parameter for both elements were performed to obtain maximum accuracy.

Note: For the simulation of device matching a special set of statistical models may be offered (search for the term "GSA Spice Model Checklist" at my.xfab.com). The model parameters used for these statistical models may differ from their corresponding matching parameters because of special simulator requirements.

Note: Two devices with higher distance to each other will exhibit greater mismatch of parameters (long distance mismatch). It is also advisable to avoid the use of minimum length or width for improved matching.

Note: Please also refer to the document [Design Guidelines for Improved Device Matching](#), available on "my X-FAB."

MOS Transistor Matching Parameters

MOS matching is characterized using Pelgrom coefficients (see M. J. Pelgrom et al, IEEE JSSC, vol SC-24 pp.1433-1439, October 1989) where the standard deviation of mismatch between adjacent MOSFETs is plotted versus the square root of the area ($W * L$). A line fit to the data passes through the origin with a slope which maybe characterized as the Pelgrom coefficient. For the calculation of the matching parameters the effective width (W_{eff}) and length (L_{eff}) of the transistors is used:



4. Process related guidelines → 4.1 Matching Introduction

$$\begin{aligned} W_{eff} &= W - \Delta W \\ L_{eff} &= L - \Delta L \end{aligned}$$

The threshold voltage matching and the linear region gain matching are described by:

$$\sigma(VTO) = \frac{AVTO}{\sqrt{W_{eff} \cdot L_{eff}}} \quad \sigma\left(\frac{\Delta BETA}{BETA}\right) = \frac{ABETA}{\sqrt{W_{eff} \cdot L_{eff}}}$$

The drain current matching is described by:

$$\sigma\left(\frac{\Delta ID}{ID}\right) = \frac{AIDx}{\sqrt{W_{eff} \cdot L_{eff}}} \quad \text{with } x \text{ for } (VG - VTO)$$

The drain current mismatch strongly depends on the effective gate voltage: $(VG - VTO)$.

Bipolar Transistor Matching Parameters

The matching of base-emitter voltage VBE, collector current IC and base current IB is described.

Resistor Matching Parameters

The resistor matching is calculated using the effective width (W_{eff}) of the resistors:

$$\sigma\left(\frac{\Delta R}{R}\right) = \frac{AR}{\sqrt{W_{eff} \cdot L}} \quad \text{with } W_{eff} = W - \Delta W$$

Note: Metal resistors are not recommended for matching applications.

Capacitor Matching Parameters

The capacitor matching is described by:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{AC}{\sqrt{W \cdot L}}$$

4. Process related guidelines → 4.2 Simulation Models

4.2 Simulation Models

This section presents a summary of circuit simulation models for the available devices (see "Primitive Devices" list). All model files, Application Notes, Checklists et cetera are available on <https://my.xfab.com> or within the actual model library.

For detailed information on supported circuit simulators, model classification, noise, matching, statistical variation and model-specific parameters such as junction temperature, please refer to the [GSA SPICE Model Checklist](#) and the related [Device Characteristics Documentation](#) (formerly known as Model Guides).

General guidelines how to setup the different simulation environments and on the simulation types itself can be found in [Application Note SPICE Models and Simulations](#).

X-FAB simulation models are intended to be used with the analog circuit simulators Spectre, HSPICE, T-Spice and ELD0. They can also be used in other spice compatible simulation programs if the required compact models are supported.

The simulation models are valid in the junction temperature range $-55^{\circ}\text{C} \leq T_j \leq +185^{\circ}\text{C}$.

Parameter Extraction

High precision mixed analog and digital circuit simulation requires good parameter extraction strategies and accurate models. In general, the quality of a parameter extraction procedure depends on the selection of measured data (1), on the parameter extraction program (2) and on the simulation model (3).

1. The Input Data

We use measured current-voltage and conductance-voltage characteristics of a matrix of element geometries under all operating conditions. The geometries and the operating points are carefully selected in order to fulfill the requirements of typical mixed analog-digital design applications.

2. The Parameter Extraction Program

This program contains tools for extracting and optimizing the SPICE model parameters. The non-linear least-square-fit routine can optimize multiple devices with respect to multiple bias conditions in order to reduce the error between the simulated data and the measured data.

3. The Simulation Model

MOS Transistor & IGBT Model

Four types of MOS & IGBT models are available for design:

1. NMOS & PMOS: 4-terminal subcircuits
2. LV PMOS variants: 5-terminal subcircuits | includes substrate diode
3. HV NMOS & PMOS: 5-terminal subcircuits | forward operation of D/B diode is modeled
4. NIGBT: 4-terminal subcircuits

We supply models which represent the following process corners:

- **tm** = typical mean = model parameters have been extracted from typical wafers
- **wp** = worst case power = fast NMOS & fast PMOS
- **ws** = worst case speed = slow NMOS & slow PMOS
- **wo** = worst case one = fast NMOS & slow PMOS
- **wz** = worst case zero = slow NMOS & fast PMOS
- **mc_g / mc_u** = statistical models

The circuit simulation parameters are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. The process control parameters are extracted from simplified model equations.

Hence, circuit simulation parameters may differ from their corresponding process control transistor parameters.



4. Process related guidelines → 4.2 Simulation Models

Bipolar Transistor Model

Two types of bipolar models are available for design:

1. vertical PNP: 3-terminal subcircuits
2. vertical NPN: 4-terminal subcircuits | includes parasitic PNP

We supply models which represent the following process corners:

- **tm** = typical mean = typical mean process condition
- **wp** = worst case power = high speed & high beta
- **ws** = worst case speed = low speed & low beta
- **mc_g / mc_u** = statistical models

The circuit simulation parameters are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. The process control parameters are extracted from simplified model equations.

Hence, the circuit simulation parameters BF and VAF may differ from their corresponding process control transistor parameters HF and EVF.

Resistor Model

Three types of resistor models are available for design:

1. polysilicon resistors: 3-terminal subcircuit with capacitors to the third node or 2-terminal subcircuit with capacitors to the global node 0
2. diffusion & well resistors: 3-terminal subcircuits with junction diodes to the 3rd node
3. metal resistors: 2-terminal subcircuits.

We supply models which represent the following process corners:

- **tm** = typical mean = typical mean process condition
- **wp** = worst case power = low resistance
- **ws** = worst case speed = high resistance
- **mc_g / mc_u** = statistical models

Capacitor Model

The sandwich, MIM & fringe capacitor are modeled as a 2-terminal subcircuit, parasitic metal capacitors are not part of the model. The ohmic resistances of the capacitor are not modelled.

We supply models which represent the following process corners:

- **tm** = typical mean = typical mean process condition
- **wp** = worst case power = low capacitance
- **ws** = worst case speed = high capacitance
- **mc_g / mc_u** = statistical models

If voltage coefficients VC1 and VC2 of capacitors were measured to be less than 10e-6/V and 10e-7/V² respectively, VC1 and VC2 are set to 0 in the device models.

Diode Model

Three types of diode models are available for design:

1. junction diodes: 2-terminal subcircuits | operation in reverse direction is modeled
2. protection & Zener diodes: 2-terminal subcircuits | breakdown region & operation in reverse direction is modeled
3. rectifier & Schottky diodes: 2-terminal subcircuits | operation in forward & reverse direction is modeled

We supply models which represent the following process corners:

- **tm** = typical mean = typical mean process condition
- **wp** = worst case power = low capacitance
- **ws** = worst case speed = high capacitance
- **mc_g / mc_u** = statistical models



4. Process related guidelines → 4.2 Simulation Models

Please note that parasitic diodes (indicated in the PDK by 'p_') and related diodes with the same name, but without the parasitic prefix ('p_'), are both using the same model name without the prefix ('p_').

Common Notes on Corner Models and Corner Simulation Parameters

The typical mean parameters have been extracted from typical wafers.

Additionally worst case tolerances of the main parameters are given.

The default spread from typical mean parameters is +/- 3sigma, additionally +/-4sigma, +/-5sigma or +/-6sigma variation can be chosen.

Common Notes on Statistical Models

Statistical models are provided to support Monte Carlo simulation of process variation and device mismatch. These models are available for a subset of primitive devices.

For statistical models two model cases are defined:

- **mc_g** = gaussian distribution of process parameters, gaussian distribution of matching parameters
- **mc_u** = uniform distribution of process parameters, gaussian distribution of matching parameters

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