



# Design Rule Specification

## XT018 - 0.18 µm HV SOI CMOS

Document DR\_018\_06  
Release 12.1.1

June 2023

**X-FAB Global  
Services GmbH**  
Haarbergstrasse 67  
D-99097 Erfurt  
Germany

**Company Confidential**

All rights reserved. No part of this document may be reproduced, distributed, or transmitted in any form or by any means, including photocopying, recording, or other electronic or mechanical methods, without the prior written permission of X-FAB.

p +49 361 427-6663  
f +49 361 427-6631  
e [hotline@xfab.com](mailto:hotline@xfab.com)  
w <http://www.xfab.com>

# Table of Contents

<b>1. Introduction.....</b>	<b>16</b>
1.1 Related documents.....	16
1.2 General notes.....	16
1.3 Support.....	16
1.4 SpecXplorer.....	16
<b>2. General.....</b>	<b>17</b>
2.1 Process modules.....	17
2.1.1 Main modules.....	17
Module restrictions for main modules.....	17
2.1.2 Additional modules for LP5MOS main module.....	17
Module restrictions for LP5MOS main module.....	20
2.1.3 Additional modules for MOS5 main module.....	22
Module restrictions for MOS5 main module.....	25
2.2 Design layers.....	27
2.2.1 LP5MOS main module.....	27
2.2.2 MOS5 main module.....	29
2.2.3 MET3 module.....	30
2.2.4 MET4 module.....	31
2.2.5 MET5 module.....	31
2.2.6 METMID module.....	32
2.2.7 METTHK module.....	32
2.2.8 THKCOP module.....	32
2.2.9 HRPOLY module.....	32
2.2.10 MRPOLY module.....	33
2.2.11 DTI module.....	33
2.2.12 PSUB module.....	33
2.2.13 LVT module.....	33
2.2.14 SVT module.....	33
2.2.15 BJTA module.....	33
2.2.16 BJTC module.....	33
2.2.17 DEPL module.....	33
2.2.18 HVDEPL module.....	33
2.2.19 1XN module.....	34
2.2.20 1XP module.....	34
2.2.21 2XP module.....	34
2.2.22 DNC module.....	34
2.2.23 DPC module.....	34
2.2.24 HVN module.....	34
2.2.25 HVP module.....	34
2.2.26 HWC module.....	34
2.2.27 NBUF module.....	35
2.2.28 NBUR module.....	35
2.2.29 NHVA module.....	35
2.2.30 NHVR module.....	35
2.2.31 NMV module.....	35
2.2.32 PHVA module.....	36
2.2.33 PHVR module.....	36
2.2.34 PMV module.....	36
2.2.35 SJ1XN module.....	36

2.2.36 SJ1XP module.....	36
2.2.37 DIODEA module.....	37
2.2.38 DIODEB module.....	37
2.2.39 DIODEC module.....	37
2.2.40 MIM module.....	37
2.2.41 MIM23 module.....	37
2.2.42 MIM34 module.....	37
2.2.43 MIM45 module.....	37
2.2.44 DMIM module.....	37
2.2.45 DMIM3 module.....	38
2.2.46 TMIM module.....	38
2.2.47 MIMH module.....	38
2.2.48 MIMH23 module.....	38
2.2.49 MIMH34 module.....	38
2.2.50 MIMH45 module.....	38
2.2.51 DMIMH module.....	38
2.2.52 DMIMH3 module.....	38
2.2.53 TMIMH module.....	39
2.2.54 NVM module.....	39
2.2.55 BOTDIE module.....	39
2.2.56 SMALLPAD module.....	39
2.2.57 PIMIDE module.....	39
2.3 Mask layers.....	40
2.3.1 LP5MOS main module.....	40
2.3.2 MOS5 main module.....	40
2.3.3 MET3 module.....	41
2.3.4 MET4 module.....	41
2.3.5 MET5 module.....	41
2.3.6 METMID module.....	41
2.3.7 METTHK module.....	41
2.3.8 THKCOP module.....	41
2.3.9 HRPOLY module.....	42
2.3.10 MRPOLY module.....	42
2.3.11 DTI module.....	42
2.3.12 PSUB module.....	42
2.3.13 LVT module.....	42
2.3.14 SVT module.....	42
2.3.15 BJTA module.....	42
2.3.16 BJTC module.....	42
2.3.17 DEPL module.....	42
2.3.18 HVDEPL module.....	43
2.3.19 1XN module.....	43
2.3.20 1XP module.....	43
2.3.21 2XP module.....	43
2.3.22 DNC module.....	43
2.3.23 DPC module.....	43
2.3.24 HVN module.....	43
2.3.25 HVP module.....	43
2.3.26 HWC module.....	43
2.3.27 NBUF module.....	44
2.3.28 NBUR module.....	44

2.3.29 NHVA module.....	44
2.3.30 NHVR module.....	44
2.3.31 NMV module.....	44
2.3.32 PHVA module.....	45
2.3.33 PHVR module.....	45
2.3.34 PMV module.....	45
2.3.35 SJ1XN module.....	46
2.3.36 SJ1XP module.....	46
2.3.37 DIODEA module.....	46
2.3.38 DIODEB module.....	46
2.3.39 DIODEC module.....	46
2.3.40 MIM module.....	46
2.3.41 MIM23 module.....	46
2.3.42 MIM34 module.....	46
2.3.43 MIM45 module.....	47
2.3.44 DMIM module.....	47
2.3.45 DMIM3 module.....	47
2.3.46 TMIM module.....	47
2.3.47 MIMH module.....	47
2.3.48 MIMH23 module.....	47
2.3.49 MIMH34 module.....	47
2.3.50 MIMH45 module.....	47
2.3.51 DMIMH module.....	47
2.3.52 DMIMH3 module.....	47
2.3.53 TMIMH module.....	48
2.3.54 NVM module.....	48
2.3.55 BOTDIE module.....	48
2.3.56 PIMIDE module.....	48
2.4 Definitions.....	49
2.5 Primitive devices.....	54
2.5.1 LP5MOS main module.....	54
MOS transistors.....	54
Bipolar transistors.....	57
Resistors.....	58
Capacitors.....	59
Diodes.....	61
Memories.....	65
IGBTs.....	65
Virtual devices.....	65
ESD devices.....	65
2.5.2 MOS5 main module.....	66
MOS transistors.....	66
Bipolar transistors.....	69
Resistors.....	69
Capacitors.....	70
Diodes.....	73
Memories.....	76
IGBTs.....	76
Virtual devices.....	76
ESD devices.....	77
2.6 Geometric relations and rule code.....	78
2.7 General requirements.....	80
<b>3. Layer and Device rules.....</b>	<b>81</b>

3.1 LP5MOS main module.....	81
3.1.1 Layer rules.....	81
NWELL.....	81
NWELL1, NWELL2, PWELL1, PWELL2, NWELL1_E, NWELL2_E, PWELL1_E, PWELL2_E.....	82
PWBLK.....	84
DIFF.....	85
DIFFDUMMY.....	87
MV.....	89
POLY1.....	90
P1DUMMY.....	93
SBLK.....	95
SALICIDE.....	96
NIMP.....	97
PIMP.....	99
CONT.....	101
MET1.....	103
M1SLOT.....	105
M1DUMMY.....	106
VIA1.....	107
MET2.....	108
M2SLOT.....	110
M2DUMMY.....	111
LOCKED, LOCKED1, LOCKED2.....	111
LOCKED3.....	112
LOCKED4.....	112
CAPDEF.....	112
DIODEF.....	112
XFLAY.....	112
3.1.2 Device rules.....	113
ne, pe.....	113
nn.....	114
pe_5.....	115
ne5, pe5.....	116
nn5.....	117
pe5_5.....	118
qpve, qpvf, qpvg.....	119
qpve5, qpvf5, qpvg5.....	120
rdn, rdp.....	121
rnw.....	122
rdn5, rdp5.....	123
rnw5.....	124
rnp1, rnp1_3, rnp1a_3, rpp1, rpp1_3, rpp1nw_3, rpp1s, rpp1s_3.....	125
rm1, rm2.....	128
mosvc.....	129
mosvc5.....	130
csf2p.....	130
dn, dp, dnw.....	131
dnn.....	132
dn5, dp5, dnw5.....	133
dnn5.....	134
pfuse.....	135
3.2 MOS5 main module.....	137
3.2.1 Layer rules.....	137
NWELL.....	137
NWELL2, PWELL2.....	138
NWELL2_E, PWELL2_E.....	139
PWBLK.....	140
DIFF.....	141

DIFFDUMMY.....	143
MV.....	145
POLY1.....	146
P1DUMMY.....	149
SBLK.....	151
SALICIDE.....	152
NIMP.....	153
PIMP.....	155
CONT.....	157
MET1.....	159
M1SLOT.....	161
M1DUMMY.....	162
VIA1.....	163
MET2.....	164
M2SLOT.....	166
M2DUMMY.....	167
LOCKED, LOCKED1, LOCKED2.....	167
LOCKED3.....	168
LOCKED4.....	168
CAPDEF.....	168
DIODEF.....	168
XFLAY.....	168
3.2.2 Device rules.....	169
ne5, pe5.....	169
nn5.....	170
pe5_5.....	171
qpve5, qpvf5, qpgv5.....	172
rdn5, rdp5.....	173
rnw5.....	174
rnp1, rnp1_3, rpp1, rpp1_3, rpp1nw_3, rpp1s, rpp1s_3.....	175
rm1, rm2.....	178
mosvc5.....	179
csf2p.....	179
dn5, dp5, dnw5.....	180
dnn5.....	181
pfuse.....	182
3.3 MET3 module.....	184
3.3.1 Layer rules.....	184
VIA2.....	184
MET3.....	185
M3SLOT.....	187
M3DUMMY.....	188
3.3.2 Device rules.....	189
rm3.....	189
csandwt3.....	190
cif3.....	190
csf3p, csf3, csf3a.....	190
cif3a.....	190
3.4 MET4 module.....	192
3.4.1 Layer rules.....	192
VIA3.....	192
MET4.....	193
M4SLOT.....	195
M4DUMMY.....	196
3.4.2 Device rules.....	197
rm4.....	197
csandwt4.....	198
cif4.....	198

cif4a.....	198
csf4, csf4a.....	198
3.5 MET5 module.....	199
3.5.1 Layer rules.....	199
VIA4.....	199
MET5.....	200
M5SLOT.....	202
M5DUMMY.....	203
3.5.2 Device rules.....	203
rm5.....	203
csandwt5.....	205
cif5.....	205
cif5a.....	205
csf5, csf5a.....	205
3.6 METMID module.....	207
3.6.1 Layer rules.....	207
VIATP.....	207
METTP.....	209
MTPSLOT.....	211
MTPDUMMY.....	212
3.6.2 Device rules.....	213
rmtpl.....	213
cift4, cift5, cift6.....	213
cift4a, cift5a, cift6a.....	214
csft4, csft4a, csft5, csft5a, csft6, csft6a.....	214
3.7 METTHK module.....	215
3.7.1 Layer rules.....	215
VIATPL.....	215
METTPL.....	216
MTPLDUMMY.....	218
3.7.2 Device rules.....	218
rmtpl.....	218
3.8 THKCOP module.....	220
3.8.1 Layer rules.....	220
VIACOP.....	220
METCOP.....	221
3.8.2 Device rules.....	223
rmdl.....	223
3.9 HRPOLY module.....	224
3.9.1 Layer rules.....	224
HRES.....	224
3.9.2 Device rules.....	224
rmp1h, rmp1h_3.....	224
3.10 MRPOLY module.....	226
3.10.1 Layer rules.....	226
MRES.....	226
3.10.2 Device rules.....	226
rpp1k1, rpp1k1_3.....	226
rpp1k1a, rpp1k1a_3.....	228
3.11 DTI module.....	229
3.11.1 Layer rules.....	229
DTI.....	229
3.11.2 Device rules.....	232
nmva.....	232
nmvaa.....	233
nmvab.....	235

pmva.....	237
pmvaa.....	238
pmvab.....	240
rxw2ti.....	242
mosvcti.....	243
mosvc5ti.....	244
3.12 PSUB module.....	245
3.12.1 Layer rules.....	245
SUBBLK.....	245
SUB, SUB_E.....	245
3.12.2 Device rules.....	246
qpva, qpvb, qpvc.....	246
qpva5, qpvb5, qpvc5.....	247
dfwdn5.....	248
ds5b.....	249
3.13 LVT module.....	250
3.13.1 Layer rules.....	250
LVT.....	250
NWELL3, PWELL3, NWELL3_E, PWELL3_E.....	251
3.13.2 Device rules.....	251
nel, pel.....	251
pel_5.....	253
3.14 SVT module.....	254
3.14.1 Layer rules.....	254
SVT.....	254
NWELL5, NWELL5_E, PWELL5, PWELL5_E.....	255
3.14.2 Device rules.....	256
nesvt, pesvt.....	256
pesvt_5.....	257
3.15 BJTA module.....	258
3.15.1 Layer rules.....	258
NBASE.....	258
NBASE_E.....	258
3.15.2 Device rules.....	258
qpv5.....	258
qpvha.....	260
3.16 BJTC module.....	261
3.16.1 Layer rules.....	261
PBASE.....	261
PBASE_E.....	261
3.16.2 Device rules.....	261
qnv5.....	261
qnvha.....	263
3.17 DEPL module.....	264
3.17.1 Layer rules.....	264
DEPL.....	264
3.17.2 Device rules.....	264
nd5.....	264
ndmvd.....	266
ndmvf.....	268
ndhvt.....	270
ndhvta.....	272
ndhvtaa.....	274
3.18 HVDEPL module.....	276
3.18.1 Layer rules.....	276
HVDEPL.....	276

3.18.2 Device rules.....	276
ndhvrdrd.....	276
ndhvrf.....	279
3.19 1XN module.....	281
3.19.1 Layer rules.....	281
SJNP.....	281
SJNP_E.....	282
3.19.2 Device rules.....	282
nhsj1_7.....	282
nhsj1_10.....	284
nhsj1_16c.....	286
dfwnsj1_7.....	288
dfwnsj1_10.....	290
dfwnsj1_16c.....	292
3.20 1XP module.....	294
3.20.1 Layer rules.....	294
SJPN.....	294
SJPN_E.....	294
3.20.2 Device rules.....	294
phsj1_7.....	294
phsj1_10.....	297
phsj1_16c.....	299
3.21 2XP module.....	301
3.21.1 Layer rules.....	301
SJ2XP.....	301
SJNTOP.....	302
SJ2XP_E.....	302
SJNTOP_E.....	302
3.21.2 Device rules.....	302
phsj2b_7.....	302
phsj2b_8.....	305
phsj2b_10.....	307
phsj2b_13.....	309
phsj2b_16.....	311
3.22 DNC module.....	313
3.22.1 Layer rules.....	313
DNC.....	313
3.23 DPC module.....	314
3.23.1 Layer rules.....	314
DPC.....	314
3.23.2 Device rules.....	314
dnp7.....	314
3.24 HVN module.....	316
3.24.1 Layer rules.....	316
HVNWELL.....	316
HVNWELL_E.....	316
3.24.2 Device rules.....	316
peti.....	316
pe5ti.....	318
dfwdpa.....	319
ds5a.....	320
dpp6.....	321
dpp7.....	322
3.25 HVP module.....	323
3.25.1 Layer rules.....	323
HVPWELL.....	323

HVPWELL_E.....	323
3.26 HWC module.....	324
3.26.1 Layer rules.....	324
HWC.....	324
3.27 NBUF module.....	325
3.27.1 Layer rules.....	325
NBUF.....	325
NBUF_E.....	325
3.27.2 Device rules.....	325
nisj1_16.....	325
3.28 NBUR module.....	328
3.28.1 Layer rules.....	328
NBUR.....	328
3.28.2 Device rules.....	328
dhw2a.....	328
dhw2.....	330
dhw3.....	331
dhw2b.....	333
dhw2c.....	335
dhw3c.....	337
dhw4c.....	339
dhw4d.....	341
dhw5d.....	343
3.29 NHVA module.....	345
3.29.1 Layer rules.....	345
NDF.....	345
NDF_E.....	345
PWELL4.....	346
PWELL4_E.....	346
3.29.2 Device rules.....	346
nhvta.....	346
nhvtaa.....	349
nhvtb.....	351
nhvu.....	353
dfwdnt.....	355
dfwdnu.....	357
dnpa.....	359
dnpati.....	360
3.30 NHVR module.....	361
3.30.1 Layer rules.....	361
DFN.....	361
DFN_E.....	361
PDD.....	362
PDD_E.....	362
PWELL4.....	363
3.30.2 Device rules.....	363
nhvra.....	363
nhvrb.....	366
nhvrc.....	368
nhvrd.....	370
nhvre.....	372
nhvrf.....	374
dfwdnhc.....	376
dfwdnhd.....	378
dfwdnhe.....	380
dfwdnhf.....	382
dnpa.....	384

dnpati.....	385
3.31 NMV module.....	386
3.31.1 Layer rules.....	386
ESDMV.....	386
ESDMV_E.....	386
NDFMV.....	387
NDFMV_E.....	387
3.31.2 Device rules.....	387
nmvb.....	387
nmvc.....	390
nmvd.....	392
nmve.....	394
nmvf.....	396
dfwdnb.....	398
dfwdnc.....	400
dfwdnd.....	402
3.32 PHVA module.....	404
3.32.1 Layer rules.....	404
PDF.....	404
PDF_E.....	404
3.32.2 Device rules.....	404
phvta.....	404
phvtb.....	407
phvu.....	409
3.33 PHVR module.....	411
3.33.1 Layer rules.....	411
DFN.....	411
DFP.....	412
DFP_E.....	412
3.33.2 Device rules.....	412
phvra.....	412
phvrb.....	415
phvrc.....	417
phvrd.....	419
phvre.....	421
phvrf.....	423
3.34 PMV module.....	425
3.34.1 Layer rules.....	425
PDFMV.....	425
PDFMV_E.....	425
3.34.2 Device rules.....	425
pmvb.....	425
pmvd.....	428
pmve.....	430
pmvf.....	432
3.35 SJHVL module.....	434
3.35.1 Device rules.....	434
nhsj1b_2.....	434
nhsj1b_4.....	436
nhsj1b_5.....	438
nhsj1b_7.....	440
phsj2b_7.....	442
phsj1a_4.....	444
phsj1a_5.....	446
phsj1a_7.....	448
dfwnsj1b_2.....	450
dfwnsj1b_4.....	452

dfwnsj1b_5.....	454
dfwnsj1b_7.....	456
3.36 SJHVM module.....	458
3.36.1 Device rules.....	458
nhsj1b_8.....	458
nhsj1b_10.....	460
nhsj1a_13.....	462
nhsj1a_16.....	464
phsj2b_8.....	466
phsj2b_10.....	468
phsj2b_13.....	470
phsj2b_16.....	472
phsj1a_8.....	474
phsj1a_10.....	476
phsj1a_13.....	478
phsj1a_16.....	480
dfwnsj1b_8.....	482
dfwnsj1b_10.....	484
dfwnsj1a_13.....	486
dfwnsj1a_16.....	488
3.37 SJHVU module.....	490
3.37.1 Device rules.....	490
nhsj1a_20.....	490
nhsj1a_28.....	492
phsj1a_20.....	494
phsj1a_31.....	496
dfwnsj1a_20.....	498
dfwnsj1a_28.....	500
dhw4d.....	502
dhw5d.....	504
3.38 SJ1XN module.....	506
3.38.1 Layer rules.....	506
SJ1XN.....	506
SJ1XN_E.....	506
3.38.2 Device rules.....	506
nhsj1b_2.....	506
nhsj1b_4.....	509
nhsj1b_5.....	511
nhsj1b_7.....	513
nhsj1b_8.....	515
nhsj1b_10.....	517
nhsj1a_13.....	519
nhsj1a_16.....	521
nhsj1a_20.....	523
nhsj1a_28.....	525
dfwnsj1b_2.....	527
dfwnsj1b_4.....	529
dfwnsj1b_5.....	531
dfwnsj1b_7.....	533
dfwnsj1b_8.....	535
dfwnsj1b_10.....	537
dfwnsj1a_13.....	539
dfwnsj1a_16.....	541
dfwnsj1a_20.....	543
dfwnsj1a_28.....	545
3.39 SJ1XP module.....	547
3.39.1 Layer rules.....	547
SJ1XP.....	547

SJ1XP_E.....	547
3.39.2 Device rules.....	547
phsj1a_4.....	547
phsj1a_5.....	550
phsj1a_7.....	552
phsj1a_8.....	554
phsj1a_10.....	556
phsj1a_13.....	558
phsj1a_16.....	560
phsj1a_20.....	562
phsj1a_31.....	564
3.40 DIODEA module.....	566
3.40.1 Layer rules.....	566
PWELL4.....	566
PWELL4_E.....	566
3.40.2 Device rules.....	567
dnpa.....	567
dnpati.....	568
3.41 DIODEB module.....	569
3.41.1 Layer rules.....	569
PZENER.....	569
PZENER_E.....	569
3.41.2 Device rules.....	569
dza.....	569
dzati.....	571
3.42 DIODEC module.....	572
3.42.1 Layer rules.....	572
NZENER.....	572
NZENER_E.....	572
3.42.2 Device rules.....	572
dzbt.....	572
dzcti.....	574
3.43 MIM module.....	575
3.43.1 Layer rules.....	575
CAPM.....	575
3.43.2 Device rules.....	577
cmm3t, cmm4t, cmm5t, cmm6t.....	577
3.44 MIM23 module.....	578
3.44.1 Layer rules.....	578
CAPM23F.....	578
3.44.2 Device rules.....	580
cmm3.....	580
3.45 MIM34 module.....	581
3.45.1 Layer rules.....	581
CAPM34F.....	581
3.45.2 Device rules.....	583
cmm4.....	583
3.46 MIM45 module.....	584
3.46.1 Layer rules.....	584
CAPM45F.....	584
3.46.2 Device rules.....	586
cmm5.....	586
3.47 DMIM module.....	587
3.47.1 Layer rules.....	587
CAPM2.....	587

3.47.2 Device rules.....	590
cdmm4, cdmm4t.....	590
3.48 DMIM3 module.....	591
3.48.1 Layer rules.....	591
CAPM2A.....	591
3.48.2 Device rules.....	594
cdmm5, cdmm5t.....	594
3.49 TMIM module.....	595
3.49.1 Layer rules.....	595
CAPM3.....	595
3.49.2 Device rules.....	598
ctmm5, ctmm5t.....	598
3.50 MIMH module.....	599
3.50.1 Layer rules.....	599
CAPMH.....	599
3.50.2 Device rules.....	601
cmmh3t, cmmh4t, cmmh5t, cmmh6t.....	601
cmmh4l, cmmh5l, cmmh6l.....	602
3.51 MIMH23 module.....	603
3.51.1 Layer rules.....	603
CAPMH23F.....	603
3.51.2 Device rules.....	605
cmmh3.....	605
3.52 MIMH34 module.....	606
3.52.1 Layer rules.....	606
CAPMH34F.....	606
3.52.2 Device rules.....	608
cmmh4.....	608
3.53 MIMH45 module.....	609
3.53.1 Layer rules.....	609
CAPMH45F.....	609
3.53.2 Device rules.....	611
cmmh5.....	611
3.54 DMIMH module.....	612
3.54.1 Layer rules.....	612
CAPMH2.....	612
3.54.2 Device rules.....	615
cdmmh4, cdmmh4t.....	615
3.55 DMIMH3 module.....	616
3.55.1 Layer rules.....	616
CAPMH2A.....	616
3.55.2 Device rules.....	619
cdmmh5, cdmmh5t.....	619
3.56 TMIMH module.....	620
3.56.1 Layer rules.....	620
CAPMH3.....	620
3.56.2 Device rules.....	623
ctmmh5, ctmmh5t.....	623
3.57 CSP5L module.....	624
3.57.1 Device rules.....	624
csp5tl_3.....	624
csp5tla_3.....	626
3.58 CEEPROM module.....	628
3.59 NVM module.....	629

3.59.1 Layer rules.....	629
PWS.....	629
SCI.....	629
3.60 OTP5 module.....	630
3.61 BOTDIE module.....	631
3.61.1 Layer rules.....	631
BDO.....	631
3.62 FLATPV module.....	633
3.63 SMALLPAD module.....	634
3.64 PIMIDE module.....	635
3.64.1 Layer rules.....	635
NOPIM.....	635
PIMIDE.....	636
<b>4. Periphery rules.....</b>	<b>637</b>
4.1 Layer rules.....	637
PAD.....	637
4.2 Pad-type rules.....	641
3 Metal METMID Bond Pad, 4 Metal METMID + METTHK Bond Pad, 4 Metal METMID Bond Pad, 5 Metal METMID + METTHK Bond Pad, 5 Metal METMID Bond Pad, 6 Metal METMID + METTHK Bond Pad, 6 Metal METMID Bond Pad, 4 Metal METTHK Bond Pad, 5 Metal METTHK Bond Pad, 6 Metal METTHK Bond Pad.....	641
4 Metal METMID + METTHK Circuit-Under-Pad Bond Pad, 4 Metal METMID Circuit-Under-Pad Bond Pad, 4 Metal METTHK Circuit-Under-Pad Bond Pad, 5 Metal METMID + METTHK Circuit-Under-Pad Bond Pad, 5 Metal METMID Circuit-Under-Pad Bond Pad, 5 Metal METTHK Circuit-Under-Pad Bond Pad, 6 Metal METMID + METTHK Circuit-Under-Pad Bond Pad, 6 Metal METMID Circuit-Under-Pad Bond Pad, 6 Metal METTHK Circuit-Under-Pad Bond Pad, 6 Metal METTHK Circuit-Under-Pad Bond Pad.....	645
Probe Pad.....	647
4.3 Scribe rules.....	648
4.4 Corner rules.....	649
<b>5. Design related guidelines.....</b>	<b>651</b>
5.1 Miscellaneous.....	651
5.2 Antenna Rule definitions.....	652
5.3 NLEAK.....	654
5.4 PLEAK.....	656
5.5 Dummy Pattern Generation.....	658
5.6 Voltage class definitions.....	660
5.7 Strategies for Avoiding Plasma Induced Damage (PID) Risks.....	661

## 1. Introduction

### 1.1 Related documents

**Note:** The specification documents listed in the table below do not contain information which is additional to that available in the SpecXplorer.

Description	Document number
Process and Device Specification XT018 - 0.18 µm HV SOI CMOS	PDS_018_06
PCM Acceptance Specification XT018 - 0.18 µm HV SOI CMOS	PAS_018_06
Process Reliability Specification XT018 - 0.18 µm HV SOI CMOS	PR_018_06

**Note:** Additional available specifications:

Design Rule Specification 0.18µm MIM Antenna Rules [DR\\_018\\_10](#)

**Note:** Note that additional documents and application notes related to this process family can be found in the relevant document container at "my X-FAB", under "[Process Selection Documents](#)" and "[Technical Documents](#)"

**Note:** Users may also wish to use the RelXplorer interactive application. This can provide information about device and layer reliability according to application specific mission profiles. For access to this see <https://relxplorer.xfab.com/>

### 1.2 General notes

It is strongly advised that all reported DRC errors are removed.

In addition to the rules for mask making, this document also contains the rules for design support layers which:

- aid chip construction
- aid scribe lane construction
- enable LVS extraction of components
- control automatic pattern fill

Scaling of these rules for application to or from the other processes is NOT guaranteed.

All data represent the drawn dimensions. Graphical illustrations are not to scale.

Predefined layout must not be changed.

Modified devices are not supported.

The specification values have been obtained during the pre-production phase of the processes.

This specification is valid excluding a process specific area around the wafer edge of 5mm width. In the affected area, the function, parameters and reliability of the structures are not guaranteed.

### 1.3 Support

Technical questions should be directed to:

X-FAB Global Services GmbH

web:	<a href="http://www.xfab.com">http://www.xfab.com</a>	phone:	+49 361 427-6663
email:	<a href="mailto:hotline@xfab.com">hotline@xfab.com</a>	fax:	+49 361 427-6631

### 1.4 SpecXplorer

All of the data in this specification document is also available online via the SpecXplorer website. For access to this, see <http://specxplorer.xfab.com>.

## 2. General

## 2. General

### 2.1 Process modules

For the process family, two main modules exist. One of the main modules must be chosen. This can then be combined with one or more additional modules. Please also refer to the tables showing the required and forbidden modules, because:

- some modules are only available in combination with other modules,
- some modules are not available in combination with other modules.

For a complete list of available metal layer combinations, refer to the table below:

#### Metal Options

number of metals	Available Metal Layer Combinations	Module name (main=LP5MOS or MOS5)
3	MET1-MET2-METTP	main+METMID
4	MET1-MET2-MET3-METTP	main+MET3+METMID
4	MET1-MET2-MET3-METTPL	main+MET3+METTHK
4	MET1-MET2-METTP-METTPL	main+METMID+METTHK
5	MET1-MET2-MET3-MET4-METTP	main+MET3+MET4+METMID
5	MET1-MET2-MET3-MET4-METTPL	main+MET3+MET4+METTHK
5	MET1-MET2-MET3-METTP-METTPL	main+MET3+METMID+METTHK
5	MET1-MET2-MET3-METTP-METCOP	main+MET3+METMID+THKCOP
5	MET1-MET2-MET3-METTPL-METCOP	main+MET3+METTHK+THKCOP
6	MET1-MET2-MET3-METTP-METTPL-METCOP	main+MET3+METMID+METTHK+THKCOP
6	MET1-MET2-MET3-MET4-MET5-METTP	main+MET3+MET4+MET5+METMID
6	MET1-MET2-MET3-MET4-MET5-METTPL	main+MET3+MET4+MET5+METTHK
6	MET1-MET2-MET3-MET4-METTP-METTPL	main+MET3+MET4+METMID+METTHK

#### 2.1.1 Main modules

Name	No. of masks	Description	Typical devices, applications
LP5MOS	19	1.8V / 5.0V low power CMOS module, single polysilicon, metal 1, metal 2	1.8V low power NMOS/ PMOS, 5.0V low power NMOS/ PMOS, well, polysilicon and metal resistors
MOS5	14	5.0V low power CMOS module, single polysilicon, metal 1, metal 2	5.0V low power NMOS/PMOS, well, polysilicon and metal resistors

#### Module restrictions for main modules

Name	Required modules	Forbidden modules
LP5MOS	METMID or (MET3 and METTHK)	MOS5
MOS5	METMID or (MET3 and METTHK)	LP5MOS

#### 2.1.2 Additional modules for LP5MOS main module

Name	No. of masks	Description	Typical devices, applications
MET3	2	3-metal module, additional via2/metal 3 layers	more complex wiring

## 2. General → 2.1 Process modules→ 2.1.2 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
MET4	2	4-metal module, additional via3/metal 4 layers	more complex wiring
MET5	2	5-metal module, additional via4/metal 5 layers	more complex wiring
METMID	2	top metal module, additional top metal & via layers	more complex wiring
METTHK	2	thick metal module, additional thick metal and thick via layers	power distribution
THKCOP	1	thick copper module	thick copper redistribution layer
	<p><b>Note:</b> Halogen free mold compound is strongly recommended to avoid the surface leakage. Only full wafer thickness is acceptable for THKCOP module (i.e. grinding has to be done afterwards). No ink dots is allowed, probe marks on chips are not recommended.</p>		
HRPOLY	1	high resistance polysilicon module	lightly N-doped Polysilicon resistor
	<p><b>Note:</b> When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.</p>		
MRPOLY	1	medium resistance polysilicon module	lightly P-doped Polysilicon resistor
DTI	1	deep trench isolation module	complete dielectric isolation for high and low side operation, 10V drain extension NMOS/ PMOS and well resistor
PSUB	1	sub block module	1.8V / 5.0V PNP bipolar transistors
LVT	2	1.8V low Vt module	1.8V low Vt NMOS and PMOS
SVT	2	1.8V medium Vt module	1.8V medium Vt NMOS and PMOS
BJTA	1	bipolar module	5V / 25V PNP bipolar transistor
BJTC	1	bipolar module	5V / 25V NPN bipolar transistor
DEPL	1	depletion module	5.0V / 20V / 32V / 40V depletion NMOS and Low Ron 40V depletion NMOS
HVDEPL	1	High voltage depletion module	85V / 125V depletion NMOS
1XN	1	Gen1 super-junction NDMOS module	100V / 140V / 200V SJNP HV NMOS and SJNP diode
1XP	1	Gen1 super-junction PDMOS module	100V / 140V / 200V SJPN HV PMOS
2XP	2	Gen2 Low Ron super-junction high voltage PMOS module	115V / 140V / 155V / 195V / 235V SJ2XP HV PMOS
DNC	1	DNC module	6.0V/7.0V P-Type protection diode, additional NWELL1 implant into NWELL2
	<p><b>Note:</b> When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.</p>		
DPC	1	DPC module	7.0V N-type protection diode, additional PWELL1 implant into PWELL2
	<p><b>Note:</b> When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.</p>		
HVN	1	Deep n-well module	1.8V/ 5.0V trench isolated PMOS, 5.0V schottky diode, 6.0V/7.0V P-type protection diode and 5.0V rectifier p+/n diode, additional HVNWELL implant for SJ MOS
HVP	1	Deep p-well module	additional HVPWELL implant for SJ MOS
HWC	1	handle wafer contact module	top side handle wafer contact
NBUF	1	n-buffer module	200V SJNP NIGBT
NBUR	1	n-buried handle wafer diode module	high voltage handle wafer diodes
NHVA	2	high voltage NMOS module	40V / 60V NMOS, Low Ron 40V NMOS and 40V / 60V rectifier diode
	<p><b>Note:</b> When this module is chosen in combination with DIODEA or NHVR module, the combined additional mask count is reduced by one.</p>		



## 2. General → 2.1 Process modules→ 2.1.2 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
NHVR	3	high voltage NMOS module	40V / 60V / 70V / 85V / 100V / 125V NMOS and 70V / 85V / 100V / 125V rectifier diode
	<b>Note:</b> When this module is chosen in combination with PHVR module, the combined additional mask count is reduced by one.		
	<b>Note:</b> When this module is chosen in combination with DIODEA or NHVA module, the combined additional mask count is reduced by one.		
NMV	2	mid voltage NMOS module	12V / 15V / 20V / 25V / 32V NMOS and 12V / 15V / 20V rectifier diode
PHVA	1	high voltage PMOS module	40V / 60V PMOS and Low Ron 40V PMOS
PHVR	2	high voltage PMOS module	40V / 60V / 70V / 85V / 100V / 125V PMOS
	<b>Note:</b> When this module is chosen in combination with NHVR module, the combined additional mask count is reduced by one.		
PMV	1	mid voltage PMOS module	12V / 18V / 25V / 32V PMOS
SJHVL	0	Gen2 super-junction modules <120V	45V / 72V / 95V / 115V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode, 2XP HV PMOS
SJHVM	0	Gen2 super-junction modules ≥120V and <250V	140V / 155V / 195V / 235V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode, 2XP HV PMOS
SJHVU	0	Gen2 super-junction modules >250V	290V / 375V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode
SJ1XN	1	Gen2 super-junction high voltage NMOS module	45V / 72V / 95V / 115V / 140V / 155V / 195V / 235V / 290V / 375V SJ1XN HV NMOS and diode
SJ1XP	1	Gen2 super-junction high voltage PMOS module	72V / 95V / 115V / 140V / 155V / 195V / 235V / 290V / 375V SJ1XP HV PMOS
DIODEA	1	diode a module	8V N-type protection diode
	<b>Note:</b> When this module is chosen in combination with NHVA or NHVR module, the combined additional mask count is reduced by one.		
DIODEB	1	diode b module	5.3V Zener diode
DIODEC	1	diode c module	5.3V Zener diode (DTI)
MIM	1	MIM capacitor module	MIM capacitor between metal top and metal layer underneath
MIM23	1	MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIM34	1	MIM capacitor module	MIM capacitor between metal 3 and metal 4
MIM45	1	MIM capacitor module	MIM capacitor between metal 4 and metal 5
DMIM	1	double MIM capacitor module	double MIM capacitor
DMIM3	1	double MIM capacitor module	double MIM capacitor between metal 3 and (metal 5 or metal top)
TMIM	1	triple MIM capacitor module	triple MIM capacitor
MIMH	1	single high capacitance MIM capacitor module	single high capacitance MIM capacitor
MIMH23	1	single high capacitance MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIMH34	1	high capacitance MIM capacitor module	MIM capacitor between metal 3 and metal 4
MIMH45	1	high capacitance MIM capacitor module	MIM capacitor between metal 4 and metal 5
DMIMH	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor
DMIMH3	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor between metal 3 and (metal 5 or metal top)

⇒

2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	No. of masks	Description	Typical devices, applications
TMIMH	1	triple high capacitance MIM capacitor module	triple high capacitance MIM capacitor
CSP5L	0	MOM capacitor module	MOM capacitor >250V
CEEPROM	0	EEPROM memory module	ready to use EEPROM memory blocks
<b>Note:</b> For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.			
NVM	4	non volatile memory module (SONOS based)	ready-to-use FLASH and EEPROM blocks
<b>Note:</b> For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.			
OTP5	0	One-Time Programmable memory module	ready to use OTP memory blocks
<b>Note:</b> For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.			
BOTDIE	1	bottom dielectric	stress relief between copper and X-Fab's passivation, required for chip size >2mm*2mm or passivation topography >0.5µm
FLATPV	0	Flat passivation	Flat passivation, post process
SMALLPAD	0	Smaller passivation opening	Smaller passivation opening for bumping process
PIMIDE	1	polyimide module, resilient barrier layer on top of passivation	wafer overcoat for stress relief and passivation protection

### Module restrictions for LP5MOS main module

Name	Required modules	Forbidden modules
MET3	-	-
MET4	MET3	THKCOP
MET5	MET4	(METMID and METTHK) or THKCOP
METMID	-	-
METTHK	MET3 or METMID	FLATPV
THKCOP	MET3 and BOTDIE	PIMIDE or MET4 or MET5 or SMALLPAD
HRPOLY	-	-
MRPOLY	-	-
DTI	-	-
PSUB	-	-
LVT	-	-
SVT	-	-
BJTA	DTI and PSUB	-
BJTC	DTI and PSUB	-
DEPL	-	-
HVDEPL	DTI and PSUB and NHVR	-
1XN	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR	-
1XP	DTI and PSUB and DNC and HVN and HVP and HWC and NBUR	-
2XP	DTI and PSUB and DNC and HVN and HWC and NBUR and (SJHVL or SJHVM)	-
DNC	-	-
DPC	-	-



2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	Required modules	Forbidden modules
HVN	DTI and PSUB	-
HVP	PSUB	-
HWC	DTI	-
NBUF	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR and 1XN	-
NBUR	HWC and DTI and HVN and PSUB	-
NHVA	DTI and PSUB	-
NHVR	DTI and PSUB	-
NMV	DTI	-
PHVA	DTI and PSUB	-
PHVR	DTI and PSUB	-
PMV	DTI and PSUB	-
SJHVL	SJ1XP or 2XP or SJ1XN or NBUR	-
SJHVM	SJ1XP or 2XP or SJ1XN or NBUR	-
SJHVU	SJ1XP or SJ1XN or NBUR	-
SJ1XN	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR and (SJHVL or SJHVM or SJHVU)	-
SJ1XP	DTI and PSUB and HVN and HWC and NBUR and DNC and (SJHVL or SJHVM or SJHVU)	-
DIODEA	PSUB	-
DIODEB	PSUB	-
DIODEC	DTI and PSUB	-
MIM	METMID	MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM23	MET3	MIM or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM34	MET4	MIM or MIM23 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM45	MET5	MIM or MIM23 or MIM34 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIM	MET4 or (MET3 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIM3	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
TMIM	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH	METMID or METTHK	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH23	MET3	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH

⇒

2. General → 2.1 Process modules → 2.1.2 Additional modules f... → Module restrictions ...

Name	Required modules	Forbidden modules
MIMH34	MET4	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH45	MET5	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or DMIMH or DMIMH3 or TMIMH
DMIMH	MET4 or (MET3 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or TMIMH
DMIMH3	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or TMIMH
TMIMH	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3
CSP5L	MET4 and METMID and METTHK and NBUR	MET5
EEPROM	-	-
NVM	-	-
OTP5	-	-
BOTDIE	THKCOP	-
FLATPV	METMID	METTHK
SMALLPAD	-	PIMIDE or THKCOP
PIMIDE	-	THKCOP or SMALLPAD

### 2.1.3 Additional modules for MOS5 main module

Name	No. of masks	Description	Typical devices, applications
MET3	2	3-metal module, additional via2/metal 3 layers	more complex wiring
MET4	2	4-metal module, additional via3/metal 4 layers	more complex wiring
MET5	2	5-metal module, additional via4/metal 5 layers	more complex wiring
METMID	2	top metal module, additional top metal & via layers	more complex wiring
METTHK	2	thick metal module, additional thick metal and thick via layers	power distribution
THKCOP	1	thick copper module	thick copper redistribution layer
	<b>Note:</b> Halogen free mold compound is strongly recommended to avoid the surface leakage. Only full wafer thickness is acceptable for THKCOP module (i.e. grinding has to be done afterwards). No ink dots is allowed, probe marks on chips are not recommended.		
HRPOLY	1	high resistance polysilicon module	lightly N-doped Polysilicon resistor
	<b>Note:</b> When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.		
MRPOLY	1	medium resistance polysilicon module	lightly P-doped Polysilicon resistor
DTI	1	deep trench isolation module	complete dielectric isolation for high and low side operation, 10V drain extension NMOS/PMOS and well resistor
PSUB	1	sub block module	1.8V / 5.0V PNP bipolar transistors
BJTA	1	bipolar module	5V / 25V PNP bipolar transistor
BJTC	1	bipolar module	5V / 25V NPN bipolar transistor



## 2. General → 2.1 Process modules→ 2.1.3 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
DEPL	1	depletion module	5.0V / 20V / 32V / 40V depletion NMOS and Low Ron 40V depletion NMOS
HVDEPL	1	High voltage depletion module	85V / 125V depletion NMOS
1XN	1	Gen1 super-junction NDMOS module	100V / 140V / 200V SJNP HV NMOS and SJNP diode
1XP	1	Gen1 super-junction PDMOS module	100V / 140V / 200V SJPN HV PMOS
2XP	2	Gen2 Low Ron super-junction high voltage PMOS module	115V / 140V / 155V / 195V / 235V SJ2XP HV PMOS
DNC	1	DNC module	6.0V/7.0V P-Type protection diode, additional NWELL1 implant into NWELL2
<b>Note:</b> When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.			
DPC	1	DPC module	7.0V N-type protection diode, additional PWELL1 implant into PWELL2
<b>Note:</b> When this module is chosen in combination with LP5MOS module, the combined additional mask count is reduced by one.			
HVN	1	Deep n-well module	1.8V/ 5.0V trench isolated PMOS, 5.0V schottky diode, 6.0V/7.0V P-type protection diode and 5.0V rectifier p+/n diode, additional HVNWELL implant for SJ MOS
HVP	1	Deep p-well module	additional HVPWELL implant for SJ MOS
HWC	1	handle wafer contact module	top side handle wafer contact
NBUF	1	n-buffer module	200V SJNP NIGBT
NBUR	1	n-buried handle wafer diode module	high voltage handle wafer diodes
NHVA	2	high voltage NMOS module	40V / 60V NMOS, Low Ron 40V NMOS and 40V / 60V rectifier diode
<b>Note:</b> When this module is chosen in combination with DIODEA or NHVR module, the combined additional mask count is reduced by one.			
NHVR	3	high voltage NMOS module	40V / 60V / 70V / 85V / 100V / 125V NMOS and 70V / 85V / 100V / 125V rectifier diode
<b>Note:</b> When this module is chosen in combination with PHVR module, the combined additional mask count is reduced by one.			
<b>Note:</b> When this module is chosen in combination with DIODEA or NHVA module, the combined additional mask count is reduced by one.			
NMV	2	mid voltage NMOS module	12V / 15V / 20V / 25V / 32V NMOS and 12V / 15V / 20V rectifier diode
PHVA	1	high voltage PMOS module	40V / 60V PMOS and Low Ron 40V PMOS
PHVR	2	high voltage PMOS module	40V / 60V / 70V / 85V / 100V / 125V PMOS
<b>Note:</b> When this module is chosen in combination with NHVR module, the combined additional mask count is reduced by one.			
PMV	1	mid voltage PMOS module	12V / 18V / 25V / 32V PMOS
SJHVL	0	Gen2 super-junction modules <120V	45V / 72V / 95V / 115V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode, 2XP HV PMOS
SJHVM	0	Gen2 super-junction modules ≥120V and <250V	140V / 155V / 195V / 235V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode, 2XP HV PMOS
SJHVU	0	Gen2 super-junction modules >250V	290V / 375V SJ1XN HV NMOS, SJ1XP HV PMOS, SJ1XN diode



## 2. General → 2.1 Process modules→ 2.1.3 Additional modules f...

Name	No. of masks	Description	Typical devices, applications
SJ1XN	1	Gen2 super-junction high voltage NMOS module	45V / 72V / 95V / 115V / 140V / 155V / 195V / 235V / 290V / 375V SJ1XN HV NMOS and diode
SJ1XP	1	Gen2 super-junction high voltage PMOS module	72V / 95V / 115V / 140V / 155V / 195V / 235V / 290V / 375V SJ1XP HV PMOS
DIODEA	1	diode a module	8V N-type protection diode
<b>Note:</b> When this module is chosen in combination with NHVA or NHVR module, the combined additional mask count is reduced by one.			
DIODEB	1	diode b module	5.3V Zener diode
DIODEC	1	diode c module	5.3V Zener diode (DTI)
MIM	1	MIM capacitor module	MIM capacitor between metal top and metal layer underneath
MIM23	1	MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIM34	1	MIM capacitor module	MIM capacitor between metal 3 and metal 4
MIM45	1	MIM capacitor module	MIM capacitor between metal 4 and metal 5
DMIM	1	double MIM capacitor module	double MIM capacitor
DMIM3	1	double MIM capacitor module	double MIM capacitor between metal 3 and (metal 5 or metal top)
TMIM	1	triple MIM capacitor module	triple MIM capacitor
MIMH	1	single high capacitance MIM capacitor module	single high capacitance MIM capacitor
MIMH23	1	single high capacitance MIM capacitor module	MIM capacitor between metal 2 and metal 3
MIMH34	1	high capacitance MIM capacitor module	MIM capacitor between metal 3 and metal 4
MIMH45	1	high capacitance MIM capacitor module	MIM capacitor between metal 4 and metal 5
DMIMH	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor
DMIMH3	1	double high capacitance MIM capacitor module	double high capacitance MIM capacitor between metal 3 and (metal 5 or metal top)
TMIMH	1	triple high capacitance MIM capacitor module	triple high capacitance MIM capacitor
CSP5L	0	MOM capacitor module	MOM capacitor >250V
EEPROM	0	EEPROM memory module	ready to use EEPROM memory blocks
	<b>Note:</b> For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.		
OTP5	0	One-Time Programmable memory module	ready to use OTP memory blocks
	<b>Note:</b> For ready-to-use memory blocks, refer to the memory block specification regarding the process module combination which is required for the specific block.		
BOTDIE	1	bottom dielectric	stress relief between copper and X-Fab's passivation, required for chip size >2mm*2mm or passivation topography >0.5µm
FLATPV	0	Flat passivation	Flat passivation, post process
SMALLPAD	0	Smaller passivation opening	Smaller passivation opening for bumping process
PIMIDE	1	polyimide module, resilient barrier layer on top of passivation	wafer overcoat for stress relief and passivation protection

2. General → 2.1 Process modules → 2.1.3 Additional modules f... → Module restrictions ...

### Module restrictions for MOS5 main module

Name	Required modules	Forbidden modules
MET3	-	-
MET4	MET3	THKCOP
MET5	MET4	(METMID and METTHK) or THKCOP
METMID	-	-
METTHK	MET3 or METMID	FLATPV
THKCOP	MET3 and BOTDIE	PIMIDE or MET4 or MET5 or SMALLPAD
HRPOLY	-	-
MRPOLY	-	-
DTI	-	-
PSUB	-	-
BJTA	DTI and PSUB	-
BJTC	DTI and PSUB	-
DEPL	-	-
HVDEPL	DTI and PSUB and NHVR	-
1XN	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR	-
1XP	DTI and PSUB and DNC and HVN and HVP and HWC and NBUR	-
2XP	DTI and PSUB and DNC and HVN and HWC and NBUR and (SJHVL or SJHVM)	-
DNC	-	-
DPC	-	-
HVN	DTI and PSUB	-
HVP	PSUB	-
HWC	DTI	-
NBUF	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR and 1XN	-
NBUR	HWC and DTI and HVN and PSUB	-
NHVA	DTI and PSUB	-
NHVR	DTI and PSUB	-
NMV	DTI	-
PHVA	DTI and PSUB	-
PHVR	DTI and PSUB	-
PMV	DTI and PSUB	-
SJHVL	SJ1XP or 2XP or SJ1XN or NBUR	-
SJHVM	SJ1XP or 2XP or SJ1XN or NBUR	-
SJHVU	SJ1XP or SJ1XN or NBUR	-
SJ1XN	DTI and PSUB and DPC and HVN and HVP and HWC and NBUR and (SJHVL or SJHVM or SJHVU)	-
SJ1XP	DTI and PSUB and HVN and HWC and NBUR and DNC and (SJHVL or SJHVM or SJHVU)	-
DIODEA	PSUB	-
DIODEB	PSUB	-



2. General → 2.1 Process modules → 2.1.3 Additional modules f... → Module restrictions ...

Name	Required modules	Forbidden modules
DIODEC	DTI and PSUB	-
MIM	METMID	MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM23	MET3	MIM or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM34	MET4	MIM or MIM23 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIM45	MET5	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIM	MET4 or (MET3 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIM3	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
TMIM	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH	METMID or METTHK	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH23	MET3	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH34	MET4	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
MIMH45	MET5	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or DMIMH or DMIMH3 or TMIMH
DMIMH	MET4 or (MET3 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3 or TMIMH
DMIMH3	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or TMIMH
TMIMH	MET5 or (MET4 and METMID)	MIM or MIM23 or MIM34 or MIM45 or DMIM or DMIM3 or TMIM or MIMH or MIMH23 or MIMH34 or MIMH45 or DMIMH or DMIMH3
CSP5L	MET4 and METMID and METTHK and NBUR	MET5
CEEPROM	-	-
OTP5	-	-
BOTDIE	THKCOP	-
FLATPV	METMID	METTHK
SMALLPAD	-	PIMIDE or THKCOP
PIMIDE	-	THKCOP or SMALLPAD

2. General → 2.2 Design layers

## 2.2 Design layers

The designer is responsible for the creation of all Design Layers needed by the targeted process module(s). They are necessary for mask layer generation and/or design tools, e.g. design rule check. Some of the layers defined may be optional dependent upon the design style being used: these are described in the text.

Design Layers may be used directly, or combined with other Design Layers, or sized to create the Mask Layers.

The order of the design layers in the table does not infer any process sequence.

Design layers with GDS numbers 480 to 499 are reserved for exclusive customer use. Any data for these layers will be ignored by X-FAB.

**Note:** If the module MOS5 is selected, the layer MV is first generated covering the complete chip area before further layer generation is performed.

### 2.2.1 LP5MOS main module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NWELL	N-well	NW	2	0	drawing	
				5	VERIFICATION	defined as NW_VERIFY
PWBLK	P-well Block	PB	10	0	drawing	
DIFF	Active Area	DF	3	0	drawing	
				1	DUMMY	
				14	NOBLK	not allowed for customer use
				15	VLABEL	
MV	5V Gate Oxide	MV	4	0	drawing	
POLY1	Poly 1	P1	13	0	drawing	
				1	DUMMY	
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.
				5	VERIFICATION	defined as POLY1_VERIFY
				14	NOBLK	not allowed for customer use
				15	VLABEL	defined voltage classes
SBLK	Silicide Block	SB	34	0	drawing	
SALICIDE	Salicidation	SA	155	0	drawing	
NIMP	N+ Implant	IN	8	0	drawing	
PIMP	P+ Implant	IP	7	0	drawing	
CONT	Contact	CT	15	0	drawing	
MET1	Metal 1	M1	16	0	drawing	
				1	DUMMY	
				2	SLOT	defined as M1SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.
				5	VERIFICATION	defined as M1VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defined voltage classes

## 2. General → 2.2 Design layers→ 2.2.1 LP5MOS main module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIA1	Via 1	V1	17	0	drawing	
MET2	Metal 2	M2	18	0	drawing	
				1	DUMMY	
				2	SLOT	defined as M2SLOT
				3	TEXT	defines top level nets
						blocks dummy generation.
				4	DMYBLK	Design related guidelines must be considered.
				5	VERIFICATION	defined as M2VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defined voltage classes
PAD	Passivation	PA	19	0	drawing	
				5	VERIFICATION	
				256	SMALLPAD	only to be used by SMALLPAD module
BLKALL	Dummy Block	BA	83	4	DMYBLK	blocks all dummy generation. Design related guidelines must be considered.
LOCKED	IP core definition	LOCK	20	10	boundary	
				19	ALL	
				20	LOCKED1	
				24	LOCKED2	
LOCKED1	IP core definition	LOCK	73	10	boundary	
LOCKED2	IP core definition	LOCK	74	10	boundary	
LOCKED3	IP core definition	LOCK	40	10	boundary	
LOCKED4	IP core definition	LOCK	41	10	boundary	
CAPDEF	Capacitor Definition	CDEF	78	5	VERIFICATION	
DIODEF	Diode Definition		56	5	VERIFICATION	
XFLAY	Reserved		1			
CORNER	Chip Corner box Definition	CB	330	5	VERIFICATION	
DEVLBL	Device label		100	5	VERIFICATION	
FAMARK	Failure Analysis Marker		64	0	drawing	
PRBNDRY	Place & Route Boundary		190	0	drawing	
				10	boundary	
DONOTUSE	Should not be used by customers		380	5	VERIFICATION	
DEVELOPMENT	Still under development should not be used by customers		379	5	VERIFICATION	
TEXT	Optional Information		230	0	drawing	

2. General → 2.2 Design layers→ 2.2.2 MOS5 main module

## 2.2.2 MOS5 main module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NWELL	N-well	NW	2	0	drawing	
				5	VERIFICATION	defined as NW_VERIFY
PWBLK	P-well Block	PB	10	0	drawing	
DIFF	Active Area	DF	3	0	drawing	
				1	DUMMY	
				14	NOBLK	not allowed for customer use
				15	VLABEL	
MV	5V Gate Oxide	MV	4	0	drawing	
POLY1	Poly 1	P1	13	0	drawing	
				1	DUMMY	
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.
				5	VERIFICATION	defined as POLY1_VERIFY
				14	NOBLK	not allowed for customer use
				15	VLABEL	defined voltage classes
SBLK	Silicide Block	SB	34	0	drawing	
SALICIDE	Salicidation	SA	155	0	drawing	
NIMP	N+ Implant	IN	8	0	drawing	
PIMP	P+ Implant	IP	7	0	drawing	
CONT	Contact	CT	15	0	drawing	
MET1	Metal 1	M1	16	0	drawing	
				1	DUMMY	
				2	SLOT	defined as M1SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.
				5	VERIFICATION	defined as M1VERIFY
				9	net	defines net shapes
				10	boundary	
VIA1	Via 1	V1	17	0	drawing	



## 2. General → 2.2 Design layers→ 2.2.2 MOS5 main module

Name	Description	Code	GDS#	Data type	Purpose	Comments
MET2	Metal 2	M2	18	0	drawing	
				1	DUMMY	
				2	SLOT	defined as M2SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.
				5	VERIFICATION	defined as M2VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defined voltage classes
				0	drawing	
PAD	Passivation	PA	19	5	VERIFICATION	
				256	SMALLPAD	only to be used by SMALLPAD module
BLKALL	Dummy Block	BA	83	4	DMYBLK	blocks all dummy generation. Design related guidelines must be considered.
LOCKED	IP core definition	LOCK	20	10	boundary	
				19	ALL	
				20	LOCKED1	
				24	LOCKED2	
LOCKED1	IP core definition	LOCK	73	10	boundary	
LOCKED2	IP core definition	LOCK	74	10	boundary	
LOCKED3	IP core definition	LOCK	40	10	boundary	
LOCKED4	IP core definition	LOCK	41	10	boundary	
CAPDEF	Capacitor Definition	CDEF	78	5	VERIFICATION	
DIODEF	Diode Definition		56	5	VERIFICATION	
XFLAY	Reserved		1			
CORNER	Chip Corner box Definition	CB	330	5	VERIFICATION	
DEVLBL	Device label		100	5	VERIFICATION	
FAMARK	Failure Analysis Marker		64	0	drawing	
PRBNDRY	Place & Route Boundary		190	0	drawing	
				10	boundary	
DONOTUSE	Should not be used by customers		380	5	VERIFICATION	
DEVELOPMENT	Still under development should not be used by customers		379	5	VERIFICATION	
TEXT	Optional Information		230	0	drawing	

## 2.2.3 MET3 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIA2	Via 2	V2	27	0	drawing	

⇒

2. General → 2.2 Design layers→ 2.2.3 MET3 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
MET3	Metal 3	M3	28	0	drawing	
				1	DUMMY	
				2	SLOT	defined as M3SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.
				5	VERIFICATION	defined as M3VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defined voltage classes

## 2.2.4 MET4 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIA3	Via 3	V3	29	0	drawing	
MET4	Metal 4	M4	31	0	drawing	
				1	DUMMY	
				2	SLOT	defined as M4SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.
				5	VERIFICATION	defined as M4VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defined voltage classes

## 2.2.5 MET5 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
VIA4	Via 4	V4	32	0	drawing	
MET5	Metal 5	M5	50	0	drawing	
				1	DUMMY	
				2	SLOT	defined as M5SLOT
				3	TEXT	defines top level nets
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.
				5	VERIFICATION	defined as M5VERIFY
				9	net	defines net shapes
				10	boundary	
				15	VLABEL	defined voltage classes

2. General → 2.2 Design layers→ 2.2.6 METMID module

## 2.2.6 METMID module

Name	Description	Code	GDS#	Data type	Purpose	Comments			
VIATP	Top Via	VT	51	0	drawing				
METTP				0	drawing				
				1	DUMMY				
				2	SLOT	defined as MTPSLOT			
				3	TEXT	defines top level nets			
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.			
				5	VERIFICATION	defined as MTPVERIFY			
				9	net	defines net shapes			
				10	boundary				
				15	VLABEL	defined voltage classes			

## 2.2.7 METTHK module

Name	Description	Code	GDS#	Data type	Purpose	Comments			
VIATPL	Thick Via	VL	36	0	drawing				
METTPL				0	drawing				
				1	DUMMY				
				3	TEXT	defines top level nets			
				4	DMYBLK	blocks dummy generation. Design related guidelines must be considered.			
				5	VERIFICATION	defined as MLVERIFY			
				9	net	defines net shapes			
				10	boundary				
				15	VLABEL	defined voltage classes			

## 2.2.8 THKCOP module

Name	Description	Code	GDS#	Data type	Purpose	Comments			
VIACOP	Via to copper	VC	59	0	drawing	modified PAD layer			
METCOP				0	drawing				
				3	TEXT	defines top level nets			
				5	VERIFICATION	defined as MTCVERIFY			
				9	net	defines net shapes			
				10	boundary				
				15	VLABEL	defined voltage classes			

## 2.2.9 HRPOLY module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HRES	Lightly N+ Poly implant	HR	65	0	drawing	

2. General → 2.2 Design layers→ 2.2.10 MRPOLY module

## 2.2.10 MRPOLY module

Name	Description	Code	GDS#	Data type	Purpose	Comments
MRES	Lightly P+ Poly Implant	MR	42	0	drawing	

## 2.2.11 DTI module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DTI	Deep trench isolation	DT	152	0	drawing	
DTICEXT	DTI Capacitance Extraction Definition		194	5	VERIFICATION	

## 2.2.12 PSUB module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SUBBLK	P-SUB block	HB	124	0	drawing	

## 2.2.13 LVT module

Name	Description	Code	GDS#	Data type	Purpose	Comments
LVT	LVT implant	LV	39	0	drawing	

## 2.2.14 SVT module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SVT	SVT implant	SV	309	0	drawing	

## 2.2.15 BJTA module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NBASE	PNP implant	QN	137	0	drawing	

## 2.2.16 BJTC module

Name	Description	Code	GDS#	Data type	Purpose	Comments
PBASE	NPN implant	QP	138	0	drawing	

## 2.2.17 DEPL module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DEPL	Depletion	DL	92	0	drawing	

## 2.2.18 HVDEPL module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HVDEPL	high voltage depletion	HL	114	0	drawing	

2. General → 2.2 Design layers → 2.2.19 1XN module

### 2.2.19 1XN module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SJNP	Super Junction N-P	NT	154	0	drawing	

### 2.2.20 1XP module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SJPN	Super Junction P-N	PT	156	0	drawing	

### 2.2.21 2XP module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SJ2XP	Super Junction P-N	X4	304	0	drawing	
SJNTOP	Super Junction NTOP	NS	306	0	drawing	

### 2.2.22 DNC module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DNC	Deep N-contact	NC	132	0	drawing	Not allowed for customer use. Layer for predefined devices only.

### 2.2.23 DPC module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DPC	Deep P-contact	PC	134	0	drawing	Not allowed for customer use. Layer for predefined devices only.

### 2.2.24 HVN module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HVNWELL	deep high voltage N-well	HN	87	0	drawing	

### 2.2.25 HVP module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HVPWELL	deep high voltage P-well	HP	86	0	drawing	
				1	DUMMY	Not allowed for customer use. Layer for predefined devices only

### 2.2.26 HWC module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HWC	Handle wafer contact	HW	150	0	drawing	
				3	TEXT	
				5	VERIFICATION	

2. General → 2.2 Design layers → 2.2.27 NBUF module

## 2.2.27 NBUF module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NBUF	N Buffer	NF	158	0	drawing	

## 2.2.28 NBUR module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NBUR	Buried N Region	NB	151	0	drawing	

## 2.2.29 NHVA module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HWC	Handle wafer contact	HW	150	3	TEXT	
				5	VERIFICATION	To use as an auxiliary handle wafer contact as it is necessary for NHVA, PHVA, PMV, NMV, NHVR or PHVR module.
NDF	N-drain extension implant	NX	146	0	drawing	Layer only allowed for predefined NHVA devices
PWELL4	High voltage P-well	P4	123	0	drawing	Layer only allowed for predefined NHVA, DIODEA or NHVR devices

## 2.2.30 NHVR module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DFN	HVMOS N-drift implant	FN	292	0	drawing	
HWC	Handle wafer contact	HW	150	3	TEXT	
				5	VERIFICATION	To use as an auxiliary handle wafer contact as it is necessary for NHVA, PHVA, PMV, NMV, NHVR or PHVR module.
PDD	HVMOS P-drift implant	PF	89	0	drawing	
PWELL4	High voltage P-well	P4	123	0	drawing	Layer only allowed for predefined NHVA, DIODEA or NHVR devices

## 2.2.31 NMV module

Name	Description	Code	GDS#	Data type	Purpose	Comments
ESDMV	ESD implant for medium voltage	ES	312	0	drawing	
HWC	Handle wafer contact	HW	150	3	TEXT	
				5	VERIFICATION	To use as an auxiliary handle wafer contact as it is necessary for NHVA, PHVA, PMV, NMV, NHVR or PHVR module.



2. General → 2.2 Design layers→ 2.2.31 NMV module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NDFMV	N-drift implant for medium voltage	ND	310	0	drawing	

### 2.2.32 PHVA module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HWC	Handle wafer contact	HW	150	3	TEXT	
				5	VERIFICATION	To use as an auxiliary handle wafer contact as it is necessary for NHVA, PHVA, PMV, NMV, NHVR or PHVR module.
PDF	P-drain extension implant	PX	147	0	drawing	Layer only allowed for predefined PHVA devices

### 2.2.33 PHVR module

Name	Description	Code	GDS#	Data type	Purpose	Comments
DFN	HVMOS N-drift implant	FN	292	0	drawing	
DFP	HVMOS P-drift implant	FP	293	0	drawing	
HWC	Handle wafer contact	HW	150	3	TEXT	
				5	VERIFICATION	To use as an auxiliary handle wafer contact as it is necessary for NHVA, PHVA, PMV, NMV, NHVR or PHVR module.

### 2.2.34 PMV module

Name	Description	Code	GDS#	Data type	Purpose	Comments
HWC	Handle wafer contact	HW	150	3	TEXT	
				5	VERIFICATION	To use as an auxiliary handle wafer contact as it is necessary for NHVA, PHVA, PMV, NMV, NHVR or PHVR module.
PDFMV	P-drift implant for medium voltage	PD	314	0	drawing	

### 2.2.35 SJ1XN module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SJ1XN	Super Junction N-P	X1	290	0	drawing	

### 2.2.36 SJ1XP module

Name	Description	Code	GDS#	Data type	Purpose	Comments
SJ1XP	Super Junction P-N	X2	291	0	drawing	

2. General → 2.2 Design layers → 2.2.37 DIODEA module

### 2.2.37 DIODEA module

Name	Description	Code	GDS#	Data type	Purpose	Comments
PWELL4	High voltage P-well	P4	123	0	drawing	Layer only allowed for predefined NHVA, DIODEA or NHVR devices

### 2.2.38 DIODEB module

Name	Description	Code	GDS#	Data type	Purpose	Comments
PZENER	PZENER implant	PZ	209	0	drawing	

### 2.2.39 DIODEC module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NZENER	NZENER implant	NZ	208	0	drawing	

### 2.2.40 MIM module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM	Single MIM Top Plate Metal	CM	47	0	drawing	

### 2.2.41 MIM23 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM23F	Single MIM Top Plate Metal	C3	115	0	drawing	

### 2.2.42 MIM34 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM34F	Single MIM Top Plate Metal	C4	117	0	drawing	

### 2.2.43 MIM45 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM45F	Single MIM Top Plate Metal	C5	119	0	drawing	

### 2.2.44 DMIM module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM2	Double MIM Capacitor Metal	DM	37	0	drawing	

2. General → 2.2 Design layers → 2.2.45 DMIM3 module

## 2.2.45 DMIM3 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM2A	Double MIM capacitor Metal	D3	176	0	drawing	

## 2.2.46 TMIM module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPM3	Triple MIM Capacitor Metal	TM	38	0	drawing	

## 2.2.47 MIMH module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH	Single High Capacitance MIM Top Plate Metal	CH	173	0	drawing	

## 2.2.48 MIMH23 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH23F	Single High Capacitance MIM Top Plate Metal	H3	116	0	drawing	

## 2.2.49 MIMH34 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH34F	Single high Capacitance MIM Top Plate Metal	H4	118	0	drawing	

## 2.2.50 MIMH45 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH45F	Single high Capacitance MIM Top Plate Metal	H5	120	0	drawing	

## 2.2.51 DMIMH module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH2	Double High Capacitance MIM Top Plate Metal	DH	174	0	drawing	

## 2.2.52 DMIMH3 module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH2A	Double High Capacitance MIM Top Plate Metal	K3	177	0	drawing	

2. General → 2.2 Design layers → 2.2.53 TMIMH module

### 2.2.53 TMIMH module

Name	Description	Code	GDS#	Data type	Purpose	Comments
CAPMH3	Triple High Capacitance MIM Top Plate Metal	TH	175	0	drawing	

### 2.2.54 NVM module

Name	Description	Code	GDS#	Data type	Purpose	Comments
PWS	SONOS P-well	PS	140	0	drawing	not allowed for customer use
SCI	SONOS channel implant	SC	90	0	drawing	not allowed for customer use

### 2.2.55 BOTDIE module

Name	Description	Code	GDS#	Data type	Purpose	Comments
BDO	Bottom dielectric opening	BD	112	0	drawing	Polyimide opening, polyimide window
				5	VERIFICATION	defined as BDO_VERIFY

### 2.2.56 SMALLPAD module

Name	Description	Code	GDS#	Data type	Purpose	Comments
PAD	Passivation	PA	19	0	drawing	
				5	VERIFICATION	
				256	SMALLPAD	only to be used by SMALLPAD module

### 2.2.57 PIMIDE module

Name	Description	Code	GDS#	Data type	Purpose	Comments
NOPIM	No Polyimide	IB	46	0	drawing	
PIMIDE	Marker layer cover PAD area for PIMIDE design	PM	221	5	VERIFICATION	marker layer for chip boundary, if PIMIDE module is used

2. General → 2.3 Mask layers

## 2.3 Mask layers

The layout rules are defined in microns and bear some physical relationship to the finished on-silicon dimensions. Changes and biases will be generated during the process of mask making / Pattern Generation (under control of the X-FAB) to produce the declared electrical feature sizes which are the only maintained parameters.

The Mask Layers are produced from the Design Layers by manipulation during the mask data preparation activity.

Sizing values used for process mask manufacturing have not been included here.

According to the mask generation and mask sizing procedure, change to data on a design layer could result in more than one mask layer being affected. Additionally, some details of the mask data preparation are factory specific.

The order of the process layers in the table does not infer any process sequence.

**Note:** If the module MOS5 is selected, the layer MV is first generated covering the complete chip area before further layer generation is performed.

### 2.3.1 LP5MOS main module

Name	Mask ID	GDS#	Generated from drawn design layers
CONT	CON	15	= CONT
DIFF	ACT	3	= DIFF (DRAWING OR DUMMY)
LDN	LDN	61	derived from NIMP, PWELL1, PWELL3, PWELL5, DPC and HRES
LDP	LDP	54	derived from PIMP, NWELL1, NWELL3, NWELL5 and DNC
LNH	LNH	14	derived from NIMP, PWELL2, PWELL4 and HRES
LPH	LPH	70	derived from PIMP and NWELL2
MET1	M1	16	= MET1 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
MET2	M2	18	= MET2 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
MV	MV	4	derived from MV and DTI
NIMP	NP	8	= NIMP
NWELL1	NW1	79	= (NWELL AND NOT (MV OR LVT OR SVT)) OR DNC
NWELL2	NW2	81	= (MV AND NWELL) OR DNC
PAD	PAD	19	= PAD OR VIACOP
PIMP	PP	7	= PIMP
POLY1	GP	13	= POLY1 (DRAWING OR DUMMY)
PWELL1	PW1	80	= NOT (MV OR NWELL OR PWBLK OR LVT OR SVT OR NBASE OR PBASE OR PWS) OR DPC
PWELL2	PW2	82	= (MV AND NOT (NWELL OR PWBLK OR NBASE OR PBASE OR PWS)) OR DPC
SBLK	SAB	34	derived from SBLK, SALICIDE, POLY1, SJNP, SJPN, NBUF, PIMP and DTI
VIA1	V1	17	= VIA1

### 2.3.2 MOS5 main module

Name	Mask ID	GDS#	Generated from drawn design layers
CONT	CON	15	= CONT
DIFF	ACT	3	= DIFF (DRAWING OR DUMMY)
LNH	LNH	14	derived from NIMP, PWELL2, PWELL4 and HRES
LPH	LPH	70	derived from PIMP and NWELL2
MET1	M1	16	= MET1 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
MET2	M2	18	= MET2 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)

## 2. General → 2.3 Mask layers→ 2.3.2 MOS5 main module

Name	Mask ID	GDS#	Generated from drawn design layers
NIMP	NP	8	= NIMP
NWELL2	NW2	81	= (MV AND NWELL) OR DNC
PAD	PAD	19	= PAD OR VIACOP
PIMP	PP	7	= PIMP
POLY1	GP	13	= POLY1 (DRAWING OR DUMMY)
PWELL2	PW2	82	= (MV AND NOT (NWELL OR PWBLK OR NBASE OR PBASE OR PWS)) OR DPC
SBLK	SAB	34	derived from SBLK, SALICIDE, POLY1, SJNP, SJPN, NBUF, PIMP and DTI
VIA1	V1	17	= VIA1

**2.3.3 MET3 module**

Name	Mask ID	GDS#	Generated from drawn design layers
MET3	M3	28	= MET3 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
VIA2	V2	27	= VIA2

**2.3.4 MET4 module**

Name	Mask ID	GDS#	Generated from drawn design layers
MET4	M4	31	= MET4 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
VIA3	V3	29	= VIA3

**2.3.5 MET5 module**

Name	Mask ID	GDS#	Generated from drawn design layers
MET5	M5	50	= MET5 (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
VIA4	V4	32	= VIA4

**2.3.6 METMID module**

Name	Mask ID	GDS#	Generated from drawn design layers
METTP	MTP	33	= METTP (((DRAWING OR net) AND NOT SLOT) OR DUMMY)
VIATP	VTP	51	= VIATP

**2.3.7 METTHK module**

Name	Mask ID	GDS#	Generated from drawn design layers
METTPL	MPL	35	= METTPL ((DRAWING OR net) OR DUMMY)
VIATPL	VPL	36	= VIATPL

**2.3.8 THKCOP module**

Name	Mask ID	GDS#	Generated from drawn design layers
METCOP	MC	60	= METCOP

2. General → 2.3 Mask layers→ 2.3.9 HRPOLY module

### 2.3.9 HRPOLY module

Name	Mask ID	GDS#	Generated from drawn design layers
LDN	LDN	61	derived from NIMP, PWELL1, PWELL3, PWELL5, DPC and HRES

### 2.3.10 MRPOLY module

Name	Mask ID	GDS#	Generated from drawn design layers
MRPOLY	LPP	42	= MRES

### 2.3.11 DTI module

Name	Mask ID	GDS#	Generated from drawn design layers
DTI	DTI	152	= DTI

### 2.3.12 PSUB module

Name	Mask ID	GDS#	Generated from drawn design layers
SUB	SUB	58	= NOT (SUBBLK OR HVPWELL OR HVNWELL)

### 2.3.13 LVT module

Name	Mask ID	GDS#	Generated from drawn design layers
NWELL3	NW3	30	= (NWELL AND NOT MV) AND LVT
PWELL3	PW3	49	= NOT (MV OR NWELL OR PWBLK OR NBASE OR PBASE OR PWS) AND LVT

### 2.3.14 SVT module

Name	Mask ID	GDS#	Generated from drawn design layers
NWELL5	NW5	307	= (NWELL AND NOT MV) AND SVT
PWELL5	PW5	308	= NOT (MV OR NWELL OR PWBLK OR NBASE OR PBASE OR PWS) AND SVT

### 2.3.15 BJTA module

Name	Mask ID	GDS#	Generated from drawn design layers
NBASE	NBS	137	= NBASE

### 2.3.16 BJTC module

Name	Mask ID	GDS#	Generated from drawn design layers
PBASE	PBS	138	= PBASE

### 2.3.17 DEPL module

Name	Mask ID	GDS#	Generated from drawn design layers
DEPL	DPL	92	= DEPL

2. General → 2.3 Mask layers→ 2.3.18 HVDEPL module

### 2.3.18 HVDEPL module

Name	Mask ID	GDS#	Generated from drawn design layers
HVDEPL	HPL	114	= HVDEPL

### 2.3.19 1XN module

Name	Mask ID	GDS#	Generated from drawn design layers
SJNP	DN1	154	= SJNP

### 2.3.20 1XP module

Name	Mask ID	GDS#	Generated from drawn design layers
SJPN	DP1	156	= SJPN

### 2.3.21 2XP module

Name	Mask ID	GDS#	Generated from drawn design layers
SJ2XP	XP2	304	= SJ2XP
SJNTOP	NTP	306	= SJNTOP

### 2.3.22 DNC module

Name	Mask ID	GDS#	Generated from drawn design layers
NWELL1	NW1	79	= (NWELL AND NOT (MV OR LVT OR SVT)) OR DNC

### 2.3.23 DPC module

Name	Mask ID	GDS#	Generated from drawn design layers
PWELL1	PW1	80	= NOT (MV OR NWELL OR PWBLK OR LVT OR SVT OR NBASE OR PBASE OR PWS) OR DPC

### 2.3.24 HVN module

Name	Mask ID	GDS#	Generated from drawn design layers
HVNWELL	NBD	87	= HVNWELL

### 2.3.25 HVP module

Name	Mask ID	GDS#	Generated from drawn design layers
HVPWELL	PBD	86	= HVPWELL (DRAWING OR DUMMY)

### 2.3.26 HWC module

Name	Mask ID	GDS#	Generated from drawn design layers
HWC	HWC	150	= HWC

2. General → 2.3 Mask layers→ 2.3.27 NBUF module

### 2.3.27 NBUF module

Name	Mask ID	GDS#	Generated from drawn design layers
NBUF	NBF	158	= NBUF

### 2.3.28 NBUR module

Name	Mask ID	GDS#	Generated from drawn design layers
NBUR	NBR	151	= NBUR

### 2.3.29 NHVA module

Name	Mask ID	GDS#	Generated from drawn design layers	Description
NDF	NDF	146	= NDF	
NIMP	NP	8	= NIMP	This mask is not used with this module
NIMPA	NPA	52	= NIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				
PIMP	PP	7	= PIMP	This mask is not used with this module
PIMPA	PPA	53	= PIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				
PWELL4	PW4	123	= PWELL4	

### 2.3.30 NHVR module

Name	Mask ID	GDS#	Generated from drawn design layers	Description
DFN	DFN	292	= DFN	
NIMP	NP	8	= NIMP	This mask is not used with this module
NIMPA	NPA	52	= NIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				
PDD	PDD	89	= PDD	
PIMP	PP	7	= PIMP	This mask is not used with this module
PIMPA	PPA	53	= PIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				
PWELL4	PW4	123	= PWELL4	

### 2.3.31 NMV module

Name	Mask ID	GDS#	Generated from drawn design layers	Description
ESDMV	EMV	312	= ESDMV	
NDFMV	NFM	310	= NDFMV	
NIMP	NP	8	= NIMP	This mask is not used with this module

⇒

## 2. General → 2.3 Mask layers→ 2.3.31 NMV module

Name	Mask ID	GDS#	Generated from drawn design layers	Description
NIMPA	NPA	52	= NIMP	
	<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.			
PIMP	PP	7	= PIMP	This mask is not used with this module
	PPA	53	= PIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				

## 2.3.32 PHVA module

Name	Mask ID	GDS#	Generated from drawn design layers	Description
NIMP	NP	8	= NIMP	This mask is not used with this module
	NPA	52	= NIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				
PDF	PDF	147	= PDF	
	PP	7	= PIMP	This mask is not used with this module
PIMP				
PPA	53	= PIMP		
				<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.

## 2.3.33 PHVR module

Name	Mask ID	GDS#	Generated from drawn design layers	Description
DFN	DFN	292	= DFN	
	DFP	293	= DFP	
NIMP	NP	8	= NIMP	This mask is not used with this module
	NPA	52	= NIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				
PIMP	PP	7	= PIMP	This mask is not used with this module
	PPA	53	= PIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				

## 2.3.34 PMV module

Name	Mask ID	GDS#	Generated from drawn design layers	Description
NIMP	NP	8	= NIMP	This mask is not used with this module
	NPA	52	= NIMP	
<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.				
PDFMV	PFM	314	= PDFMV	

2. General → 2.3 Mask layers→ 2.3.34 PMV module

Name	Mask ID	GDS#	Generated from drawn design layers	Description
PIMP	PP	7	= PIMP	This mask is not used with this module
PIMPA	PPA	53	= PIMP	<b>Note:</b> When NMV, PMV, NHVA, PHVA, NHVR or PHVR module is chosen, NIMPA and PIMPA will replace NIMP and PIMP respectively.

### 2.3.35 SJ1XN module

Name	Mask ID	GDS#	Generated from drawn design layers
SJ1XN	DNT	290	= SJ1XN

### 2.3.36 SJ1XP module

Name	Mask ID	GDS#	Generated from drawn design layers
SJ1XP	DPT	291	= SJ1XP

### 2.3.37 DIODEA module

Name	Mask ID	GDS#	Generated from drawn design layers
PWELL4	PW4	123	= PWELL4

### 2.3.38 DIODEB module

Name	Mask ID	GDS#	Generated from drawn design layers
PZENER	PZN	209	= PZENER

### 2.3.39 DIODEC module

Name	Mask ID	GDS#	Generated from drawn design layers
NZENER	NZN	208	= NZENER

### 2.3.40 MIM module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM

### 2.3.41 MIM23 module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM23F

### 2.3.42 MIM34 module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM34F

2. General → 2.3 Mask layers→ 2.3.43 MIM45 module

### **2.3.43 MIM45 module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM45F

### **2.3.44 DMIM module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM2

### **2.3.45 DMIM3 module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM2A

### **2.3.46 TMIM module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPM	CM	47	= CAPM3

### **2.3.47 MIMH module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH

### **2.3.48 MIMH23 module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH23F

### **2.3.49 MIMH34 module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH34F

### **2.3.50 MIMH45 module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH45F

### **2.3.51 DMIMH module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH2

### **2.3.52 DMIMH3 module**

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH2A

2. General → 2.3 Mask layers→ 2.3.53 TMIMH module

### 2.3.53 TMIMH module

Name	Mask ID	GDS#	Generated from drawn design layers
CAPMH	CMH	173	= CAPMH3

### 2.3.54 NVM module

Name	Mask ID	GDS#	Generated from drawn design layers
LLN	LLN	129	derived from NIMP, PWS, MV
PWS	PWS	140	= PWS
SCI	SCI	90	= SCI
SOC	SOC	97	derived from SCI and DIFF

### 2.3.55 BOTDIE module

Name	Mask ID	GDS#	Generated from drawn design layers
BDO	BD	112	= BDO

### 2.3.56 PIMIDE module

Name	Mask ID	GDS#	Generated from drawn design layers
PIMIDE	PIB	46	= NOPIM OR (PAD + sizing)

2. General → 2.4 Definitions

## 2.4 Definitions

The 2-character code is intended for rule codes. The rule codes are used for short design rule check error messages.

Name	Code	Logical	Electrical feature
2FOXTI		2 FOXDTIs in parallel with minimum spacing separated by ISOTUB	
3FOXTI		3 FOXDTIs in parallel with minimum spacing separated by ISOTUB	
ACTIVE		DIFF AND NOT DTI AND NOT ISOTUB	
BM	BM	single MIM bottom metal layer (differs with the selected metal option) see also "Table for BM and VIAn assignment"	
CHANNEL	GA	(GATE AND NIMP AND PWELL) OR (GATE AND PIMP AND NWELL)	
DFN_E		DFN AND NOT (DTI OR TIEDTUB OR ISOTUB)	
DFP_E		DFP AND NOT (DTI OR TIEDTUB OR ISOTUB)	
DIFFCON	CT	diffusion contact (DIFF AND CONT)	
DIFFDTI	DI	DTI AND DIFF	
DIFFDUMMY	YD	DIFF purpose DUMMY	
ESDMV_E		ESDMV AND NOT (DTI OR TIEDTUB OR ISOTUB)	
EXCLUSIVE_WELL	WX	PTUB XOR NWELL	
EXTENT		least enclosing rectangle of the database	
FOXDTI		DTI AND NOT DIFF	
GATE	GA	gate area (POLY1 AND ACTIVE)	
HVNWELL_E		HVNWELL AND NOT (DTI OR TIEDTUB OR ISOTUB)	
HVPWELL_E		HVPWELL AND NOT (DTI OR TIEDTUB OR ISOTUB)	
HWNTUB	TN	HWTUB containing NTUB	
HWPTUB	TP	HWTUB containing PTUB	
HWTUB	TB	DTI isolated silicon tub containing HWC AND ACTIVE	
ISOTUB		Floating TUB between multiple DTI rings of minimum spacing ((0.5 µm for DIFFDTI and (1 µm to 6 µm for FOXDTI)) AND NOT SALICIDE)	
M1DUMMY	Y1	MET1 purpose DUMMY	
M1SLOT		MET1 purpose SLOT	
M1VERIFY		MET1 purpose VERIFICATION	
M1_FP		predefined floating MET1 in SJ1XN, SJ1XP module	
M1_FPLATE	F1	MET1 OR POLY1	
M2DUMMY	Y2	MET2 purpose DUMMY	
M2SLOT		MET2 purpose SLOT	
M2VERIFY		MET2 purpose VERIFICATION	
M2_FPLATE	F2	MET2 OR POLY1	
M3DUMMY	Y3	MET3 purpose DUMMY	
M3SLOT		MET3 purpose SLOT	

## 2. General → 2.4 Definitions

Name	Code	Logical	Electrical feature
M3VERIFY		MET3 purpose VERIFICATION	
M3_FPLATE	F3	(MET3 if MET3 module is selected) OR (METTP if MET3 module is not selected)	
M4DUMMY	Y4	MET4 purpose DUMMY	
M4SLOT		MET4 purpose SLOT	
M4VERIFY		MET4 purpose VERIFICATION	
M5DUMMY	Y5	MET5 purpose DUMMY	
M5SLOT		MET5 purpose SLOT	
M5VERIFY		MET5 purpose VERIFICATION	
MET1BLK		MET1 purpose DMYBLK	
MET2BLK		MET2 purpose DMYBLK	
MLVERIFY		METTPL purpose VERIFICATION	
MTCVERIFY		METCOP purpose VERIFICATION	
MTPDUMMY	YT	METTP purpose DUMMY	
MTPLDUMMY	YL	METTPL purpose DUMMY	
MTPSLOT		METTP purpose SLOT	
MTPVERIFY		METTP purpose VERIFICATION	
NBASE_E		NBASE AND NOT (DTI OR TIEDTUB OR ISOTUB)	
NBUF_E		NBUF AND NOT (DTI OR TIEDTUB OR ISOTUB)	
NDFMV_E		NDFMV AND NOT (DTI OR TIEDTUB OR ISOTUB)	
NDF_E		NDF AND NOT (DTI OR TIEDTUB OR ISOTUB)	
NDIFF	DN	NIMP AND ACTIVE	
NIMP or PIMP	IR	NIMP or PIMP	N+ or P+ diffusion - (Implant region)
NTUB	BN	TUB covered by HVNWELL	
NTYPE_WELL		n-doped well ((NWELL OR SJNP OR NDF OR NBASE OR DNC OR NBUF OR DFN OR SJ1XN) AND NOT DTI)	
NTYPE_WELL1		n-doped well (NWELL OR NBASE)	
NW4DMY	NW	NWELL OR HVNWELL OR DNC OR NDF OR NBASE OR DFN OR NDFMV	
NWELL1	W1	1.8V N-well (((NWELL AND NOT MV) AND NOT LVT) AND NOT SVT) OR DNC	
NWELL1_E	W7	NWELL1 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
NWELL2	W3	5V N-well ((MV AND NWELL) OR DNC)	
NWELL2_E	W9	NWELL2 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
NWELL3	W5	1.8V N-well ((NWELL AND NOT MV) AND LVT)	
NWELL3_E	W11	NWELL3 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
NWELL5	W13	1.8V N-well ((NWELL AND NOT MV) AND SVT)	
NWELL5_E	W15	NWELL5 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
NW_VERIFY		NWELL purpose VERIFICATION	

⇒

## 2. General → 2.4 Definitions

Name	Code	Logical	Electrical feature
NZENER_E		NZENER AND NOT (DTI OR TIEDTUB OR ISOTUB)	
P1DUMMY	YP	POLY1 purpose DUMMY	
P1_FP		predefined floating POLY1 in SJ1XN module	
PBASE_E		PBASE AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PDD_E		PDD AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PDFMV_E		PDFMV AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PDF_E		PDF AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PDIFF	DP	PIMP AND ACTIVE	
PEPI		TUB AND SUBBLK AND NOT (HVNWELL OR HVPWELL)	
PIMIDE marker		mark PAD in case of PIMIDE module	
POLY1DTI		POLY1 AND DTI	
POLY1HV		high voltage POLY1: POLY1 over NTYPE_WELL OR PTYPE_WELL OR PWBLK, if $ V_{POLY1-WELL}  > 6\text{ V}$	
POLY1_VERIFY		POLY1 purpose VERIFICATION	
PTUB	BP	TUB AND NOT NTUB	
PTUB_SUB		TUB AND NOT (HVNWELL OR HVPWELL OR SUBBLK)	
PTYPE_WELL		p-doped well (PWELL OR SJPN OR PDF OR PWS OR PBASE OR DPC OR PWELL4 OR PDFMV OR PDD OR DFP OR SJ1XP OR SJ2XP) AND NOT DTI	
PW4DMY	PI	HVPWELL OR PWELL4 OR PWS OR PDF OR PBASE OR SUBBLK OR DPC OR PDFMV OR PDD OR DFP or ESDMV	
PWELL	PW	PWELL1 OR PWELL2 OR PWELL3 OR PWELL5	
PWELL1	W2	1.8V P-well (((((NOT NTYPE_WELL1 AND NOT MV) AND NOT LVT) AND NOT SVT) AND NOT PWBLK) AND NOT PWS) AND NOT PBASE) OR DPC)	
PWELL1_E	W8	PWELL1 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PWELL2	W4	5V P-well ((MV AND NOT (NTYPE_WELL1 OR PWBLK OR PWS OR PBASE)) OR DPC)	
PWELL2_E	W10	PWELL2 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PWELL3	W6	1.8V P-well (((((NOT NTYPE_WELL1 AND NOT MV) AND NOT PWBLK) AND NOT PWS) AND NOT PBASE) AND LVT)	
PWELL3_E	W12	PWELL3 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PWELL4_E		PWELL4 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PWELL5	W14	1.8V P-well (((((NOT NTYPE_WELL1 AND NOT MV) AND NOT PWBLK) AND NOT PWS) AND NOT PBASE) AND SVT)	

⇒

## 2. General → 2.4 Definitions

Name	Code	Logical	Electrical feature
PWELL5_E	W16	PWELL5 AND NOT (DTI OR TIEDTUB OR ISOTUB)	
PZENER_E		PZENER AND NOT (DTI OR TIEDTUB OR ISOTUB)	
SJ1XN_E		SJ1XN AND NOT (DTI OR TIEDTUB OR ISOTUB)	
SJ1XP_E		SJ1XP AND NOT (DTI OR TIEDTUB OR ISOTUB)	
SJ2XP_E		SJ2XP AND NOT (DTI OR TIEDTUB OR ISOTUB)	
SJNP_E		SJNP AND NOT (DTI OR TIEDTUB OR ISOTUB)	
SJNTOP_E		SJNTOP AND NOT (DTI OR TIEDTUB OR ISOTUB)	
SJPN_E		SJPN AND NOT (DTI OR TIEDTUB OR ISOTUB)	
SUB	BS	NOT (HVNWELL OR HVPWELL OR SUBBLK)	
SUB_E		SUB AND NOT (DTI OR TIEDTUB OR ISOTUB)	
TIEDTUB		TUB between multiple DIFFDTI rings of minimum spacing (0.50 µm) and SALICIDE	
TUB	BT	DTI isolated silicon tub (NOT DTI)	
VIA <sub>n</sub>	VN	VIA (except VIATP) to connect the single MIM bottom layer (differs with the selected metal option) see also "Table for BM and VIA <sub>n</sub> assignment"	
		MET1 width and length > 10 µm	
WIDE_MET1		<b>Note:</b> The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.	
		MET2 width and length > 10 µm	
WIDE_MET2		<b>Note:</b> The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.	
		MET3 width and length > 10 µm	
WIDE_MET3		<b>Note:</b> The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.	
		MET4 width and length > 10 µm	
WIDE_MET4		<b>Note:</b> The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.	
		MET5 width and length > 10 µm	
WIDE_MET5		<b>Note:</b> The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.	
		METTP width and length > 10 µm	
WIDE_METTP		<b>Note:</b> The wide metal definition includes all extensions from the wide metal which extend by 1.0µm or less from the wide piece.	
dfwd#		dfwdnb, dfwdnc, dfwdnd	
dfwdn#		dfwdnt, dfwdnu	
dfwdnh#		dfwdnhc, dfwdnhd, dfwdnhe, dfwdnhf	
dfwnsj1_#		dfwnsj1_7, dfwnsj1_10, dfwnsj1_16c	
dfwnsj1a_#		dfwnsj1a_13, dfwnsj1a_16, dfwnsj1a_20, dfwnsj1a_28	
dfwnsj1b_#		dfwnsj1b_2, dfwnsj1b_4, dfwnsj1b_5, dfwnsj1b_7, dfwnsj1b_8, dfwnsj1b_10	
dhw#		dhw2a, dhw2, dhw3	

⇒

## 2. General → 2.4 Definitions

Name	Code	Logical	Electrical feature
dhw#c		dhw2b, dhw2c, dhw3c, dhw4c	
dhw#d		dhw4d, dhw5d	
ndhv#		ndhvt, ndhvta, ndhvtaa	
ndhvr#		ndhvrdf, ndhvrff	
ndmv#		ndmvd, ndmvf	
nhsj1_#		nhsj1_7, nhsj1_10, nhsj1_16c	
nhsj1a_#		nhsj1a_13, nhsj1a_16, nhsj1a_20, nhsj1a_28	
nhsj1b_#		nhsj1b_2, nhsj1b_4, nhsj1b_5, nhsj1b_7, nhsj1b_8, nhsj1b_10	
nhv#		nhvta, nhvtaa, nhvtb, nhvu	
nhvr#		nhvra, nhvrb, nhvrc, nhvrd, nhvre, nhvrf	
nmv#		nmvb, nmvc, nmvd, nmve, nmvf	
nmva#		nmva, nmvaa, nmvab	
phsj1_#		phsj1_7, phsj1_10, phsj1_16c	
phsj1a_#		phsj1a_4, phsj1a_5, phsj1a_7, phsj1a_8, phsj1a_10, phsj1a_13, phsj1a_16, phsj1a_20, phsj1a_31	
phsj2b_#		phsj2b_7, phsj2b_8, phsj2b_10, phsj2b_13, phsj2b_16	
phv#		phvta, phvrb, phvu	
phvr#		phvra, phvrb, phvrc, phvrd, phvre, phvrf	
pmv#		pmvb, pmvd, pmve, pmvf	
pmva#		pmva, pmvaa, pmvab	
qpv#		qpva, qpvb, qpvc, qpva5, qpvb5, qpvc5	
rnp1#		rnp1, rnp1_3, rnp1a_3	
rnp1h#		rnp1h, rnp1h_3	
rpp1#		rpp1, rpp1_3, rpp1nw_3	
rpp1k1#		rpp1k1, rpp1k1_3, rpp1k1a, rpp1k1a_3	
rpp1s#		rpp1s, rpp1s_3	
tag_#		tag_25v, tag_60v, tag_100v, tag_200v, tag_300v, tag_400v, tag_m25v, tag_m60v, tag_m100v, tag_m200v, tag_m300v, tag_m400v	

2. General → 2.5 Primitive devices

## 2.5 Primitive devices

The primitive device list does not include all the required module combinations for the stated modules. Refer also to the Module restrictions tables.

In addition to the capacitors stated in the primitive device list, it is also possible to use the capacitors built by the different gate oxides. These capacitors can be simulated by using the model of a transistor which has the respective oxide: for instance the ne and pe models in case of the 1.8V gate oxide. The operating conditions of the relating transistors are valid as well for these capacitors.

Minor changes of the simulation models might be generated due to continuous improvement of device and circuit simulation. Minor changes of models are described within the actual model data files. Please refer to further information within the current model path.

The qualification status of single devices can be checked in the Application Note "Primitive device release status" at "my X-FAB"

In addition to the listed primitive devices, non-volatile memory blocks are also available; please refer to the applicable process module details.

The following devices are available for design:

### 2.5.1 LP5MOS main module

#### MOS transistors

Name	Description	Required modules	Model rev.
ne	1.8V low power NMOS	-	10.0
nn	1.8V native Vt NMOS	-	10.0
pe	1.8V low power PMOS	-	10.0
pe_5 <sup>(1)</sup>	1.8V low power PMOS, 5 terminals	-	10.0
nel	1.8V low VT NMOS	LVT	10.0
pel	1.8V low VT PMOS	LVT	10.0
pel_5 <sup>(1)</sup>	1.8V low VT PMOS, 5 terminals	LVT	10.0
nesvt	1.8V medium VT NMOS	SVT	10.0
pesvt	1.8V medium VT PMOS 4 terminals	SVT	12.0
pesvt_5 <sup>(1)</sup>	1.8V medium VT PMOS 5 terminals	SVT	12.0
ne5	5.0V NMOS	-	12.0
nn5	5.0V native Vt NMOS	-	10.0
pe5	5.0V PMOS	-	12.0
pe5_5 <sup>(1)</sup>	5.0V PMOS, 5 terminals	-	12.0
peti	1.8V PMOS (NTUB)	DTI and HVN	12.0
pe5ti	5.0V PMOS (NTUB)	DTI and HVN	12.0
nd5	5.0V depletion NMOS	DEPL	10.0
nmva <sup>(2)(3)</sup>	10V drain extension NMOS	DTI	
nmvaa <sup>(3)</sup>	10V drain extension NMOS	DTI	12.0
nmvab <sup>(3)</sup>	10V drain extension NMOS, with drain ballast resistor	DTI	12.0
nmvb	12V NMOS	DTI and NMV	11.0
nmvc	15V NMOS	DTI and NMV	11.0
nmvd	20V NMOS	DTI and NMV	11.0
nmve	25V NMOS	DTI and NMV	11.0
nmvf	32V NMOS	DTI and NMV	11.0
ndmvd	20V depletion NMOS	DTI and DEPL and NMV	11.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ MOS transistors

Name	Description	Required modules	Model rev.
ndmvf	32V depletion NMOS	DTI and DEPL and NMV	11.0
pmva <sup>(4)(3)</sup>	10V drain extension PMOS	DTI	
pmvaa <sup>(3)</sup>	10V drain extension PMOS	DTI	12.0
pmvab <sup>(3)</sup>	10V drain extension PMOS, with drain ballast resistor	DTI	12.0
pmvb	12V PMOS	DTI and PSUB and PMV	11.0
pmvd	18V PMOS	DTI and PSUB and PMV	11.0
pmve	25V PMOS	DTI and PSUB and PMV	11.0
pmvf	32V PMOS	DTI and PSUB and PMV	11.0
nhvta <sup>(5)</sup>	Low Ron 40V NMOS	DTI and PSUB and NHVA	11.0
nhvtaa <sup>(6)(5)</sup>	Low Ron 40V NMOS	DTI and PSUB and NHVA	11.0
nhvtb <sup>(5)</sup>	40V NMOS	DTI and PSUB and NHVA	11.0
nhvu <sup>(5)</sup>	60V NMOS	DTI and PSUB and NHVA	11.0
ndhvt <sup>(5)</sup>	40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
ndhvta <sup>(5)</sup>	Low Ron 40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
ndhvtaa <sup>(7)(5)</sup>	Low Ron 40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
phvta	Low Ron 40V PMOS	DTI and PSUB and PHVA	11.1
phvtb	40V PMOS	DTI and PSUB and PHVA	11.1
phvu	60V PMOS	DTI and PSUB and PHVA	11.1
nhvra <sup>(8)</sup>	40V NMOS	DTI and PSUB and NHVR	10.0
nhvrb <sup>(8)</sup>	60V NMOS	DTI and PSUB and NHVR	10.0
nhvrc <sup>(8)</sup>	70V NMOS	DTI and PSUB and NHVR	10.0
nhvrd <sup>(8)</sup>	85V NMOS	DTI and PSUB and NHVR	10.0
nhvre <sup>(8)</sup>	100V NMOS	DTI and PSUB and NHVR	10.0
nhvrf <sup>(9)</sup>	125V NMOS	DTI and PSUB and NHVR	10.0
ndhvrd <sup>(8)</sup>	85V depletion NMOS	DTI and PSUB and NHVR and HVDEPL	10.0
ndhvrf <sup>(9)</sup>	125V depletion NMOS	DTI and PSUB and NHVR and HVDEPL	10.0
phvra <sup>(8)</sup>	40V PMOS	DTI and PSUB and PHVR	10.0
phvrb <sup>(8)</sup>	60V PMOS	DTI and PSUB and PHVR	10.0
phvrc <sup>(8)</sup>	70V PMOS	DTI and PSUB and PHVR	10.0
phvrd <sup>(8)</sup>	85V PMOS	DTI and PSUB and PHVR	10.0
phvre <sup>(8)</sup>	100V PMOS	DTI and PSUB and PHVR	10.0
phvrf <sup>(9)</sup>	125V PMOS	DTI and PSUB and PHVR	10.0
nhsj1_7	100V Gen1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1_10	140V Gen 1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1_16c	200V Gen1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1b_2	45V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ MOS transistors

Name	Description	Required modules	Model rev.
nhsj1b_4	72V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_5	95V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_7	115V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_8	140V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1b_10	155V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_13	195V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_16	235V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_20	290V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVU	12.0
nhsj1a_28	375V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVU	12.0
phsj1_7	100V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj1_10	140V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj1_16c	200V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj2b_7	115V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
phsj2b_8	140V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_10	155V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_13	195V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_16	235V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_4	72V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_5	95V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_7	115V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_8	140V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_10	155V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ MOS transistors

Name	Description	Required modules	Model rev.
phsj1a_13	195V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_16	235V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_20	290V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	12.0
phsj1a_31	375V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	12.0

**Note 1** This device is a variant of the corresponding basic device with connections to the underlying wells. Parameters of this device are identical to the corresponding basic device.

**Note 2** The device nmva is superseded by nmvaa. nmvaa must not be used for any new designs.

**Note 3** Please also refer to the "[xt018-ApplicationNote-10V\\_MOSFET](#)" available on "my X-FAB".

**Note 4** The device pmva is superseded by pmvaa. pmvaa must not be used for any new designs.

**Note 5** Please also refer to the "[xt018-ApplicationNote-NHVA\\_Module\\_HV\\_Transistors](#)" available on "my X-FAB".

**Note 6** nhvtaa provides better avalanche robustness than nhvta

**Note 7** ndhvtaa provides better avalanche robustness than ndhvta

**Note 8** The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.

**Note 9** This device is intended to enhance the ESD design window for 100V applications. The ESD design window may not be suitable for applications up to 125V.

## Bipolar transistors

Name	Description	Required modules	Model rev.
qpva	1.8V vertical PNP bipolar transistor in PEPI; emitter area = 2µm x 2µm	PSUB	5.0
qpvb	1.8V vertical PNP bipolar transistor in PEPI; emitter area = 5µm x 5µm	PSUB	5.0
qpvc	1.8V vertical PNP bipolar transistor in PEPI; emitter area = 10µm x 10µm	PSUB	5.0
qpve	1.8V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 2µm x 2µm	-	5.0
qpvf	1.8V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 5µm x 5µm	-	5.0
qpvg	1.8V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 10µm x 10µm	-	5.0
qpva5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 2 µm x 2 µm	PSUB	5.0
qpvb5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 5 µm x 5 µm	PSUB	5.0
qpvc5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 10 µm x 10 µm	PSUB	5.0
qpve5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 2 µm x 2 µm	-	5.0
qpvf5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 5 µm x 5 µm	-	5.0
qpvg5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 10 µm x 10 µm	-	5.0
qnv5	5V high gain NPN bipolar transistor	DTI and PSUB and BJTC	5.0



## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ Bipolar transistors

Name	Description	Required modules	Model rev.
qpv5	5V high gain PNP bipolar transistor	DTI and PSUB and BJTA	5.0
qnvha	25V high gain NPN bipolar transistor	DTI and PSUB and BJTC	10.0
qpvha	25V high gain PNP bipolar transistor	DTI and PSUB and BJTA	10.0

**Resistors**

Name	Description	Required modules	Model rev.
rdn	1.8V NDIFF / PWELL1 resistor (non salicided)	-	6.0
rdp	1.8V PDIFF / NWELL1 resistor (non salicided)	-	6.0
rnw	1.8V NWELL1 / PSUB resistor (STI terminated)	-	10.0
rxw2ti	NWELL Resistor under active (DTI)	DTI and PSUB	10.0
rdn5	5.0V NDIFF / PWELL2 resistor (non salicided)	-	6.0
rdp5	5.0V PDIFF / NWELL2 resistor (non salicided)	-	10.0
rnw5	5.0V NWELL2 / PSUB resistor (STI terminated)	-	10.0
rnp1 <sup>(1)</sup>	N-doped POLY1 resistor (non salicided), 2 terminals	-	12.0
rnp1_3 <sup>(2)</sup>	N-doped POLY1 resistor (non-salicided, underlying NWELL/PWELL2), 3 terminals	-	12.0
rnp1a_3 <sup>(2)</sup>	N-doped POLY1 resistor (non-salicided, underlying PWELL1/PWELL3/PWELL5), 3 terminals	-	12.0
rpp1 <sup>(1)</sup>	P-doped POLY1 resistor (non-salicided), 2 terminals	-	12.0
rpp1_3 <sup>(2)</sup>	P-doped POLY1 resistor (non-salicided, underlying PWELL), 3 terminals	-	12.0
rpp1nw_3 <sup>(2)</sup>	P-doped POLY1 resistor (non-salicided, underlying NWELL), 3 terminals	-	12.0
rpp1s	salicided P-doped POLY1 resistor, 2 terminals	-	10.0
rpp1s_3 <sup>(3)</sup>	salicided P-doped POLY1 resistor, 3 terminals	-	10.0
rnp1h	high ohmic N-doped POLY1 resistor (non salicided), 2 terminals	HRPOLY	10.0
rnp1h_3 <sup>(3)</sup>	high ohmic N-doped POLY1 resistor (non salicided), 3 terminals	HRPOLY	10.0
rpp1k1	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.0
rpp1k1_3 <sup>(3)</sup>	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.0
rpp1k1a	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.0
rpp1k1a_3 <sup>(3)</sup>	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.0
rm1	metal 1 resistor	-	6.0
rm2	metal 2 resistor	-	6.0
rm3	metal 3 resistor	MET3	6.0
rm4	metal 4 resistor	MET4	6.0
rm5	metal 5 resistor	MET5	6.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ Resistors

Name	Description	Required modules	Model rev.
rmtpl	top metal resistor	METMID	6.0
rmtpl	thick metal resistor	METTHK	6.0
rmdl	thick copper redistribution resistor	THKCOP	4.1

**Note 1** The 2-terminal poly resistor devices do not consider the underlying wells. As a result of this simplification, the models are less accurate than their 3-terminal counterparts, which do account for the underlying well configuration.

**Note 2** These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency.

**Note 3** These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency. Parameters of these devices are identical to the corresponding basic device.

## Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
mosvc	1.8V N-type Varactor	-	-	5.0
mosvc5	5V N-type Varactor	-	-	5.0
mosvcti	1.8V P-type Varactor (DTI)	DTI	-	5.0
mosvcti5	5V P-type Varactor (DTI)	DTI	-	5.0
csandwt3	POLY1 / metal1/ metal2/ metal3 capacitor	MET3	-	6.0
csandwt4	POLY1 / metal1/ metal2/ metal3/ metal4 capacitor	MET4	-	6.0
csandwt5	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 capacitor	MET5	-	6.0
csp5tl_3	300V active/ metal 1/ metal 2/ metal 3/ metal 4/ top metal/ thick metal capacitor, 3 terminals	CSP5L	MET5	12.0
csp5tla_3	400V active/ metal 2/ metal 4/ thick metal capacitor, 3 terminals	CSP5L	MET5	12.0
cif3	100V metal1/metal2/metal3 fringe capacitor	MET3	-	8.0
cif4	100V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	8.0
cif5	100V metal1/metal2/metal3/metal4/ metal5 fringe capacitor	MET5	-	8.0
cift4	100V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	9.0
cift5	100V metal1/metal2/metal3/metal4/ metaltop fringe capacitor	MET4 and METMID	MET5	9.0
cift6	100V metal1/metal2/metal3/metal4/ metal5/metaltop fringe capacitor	MET5 and METMID	-	9.0
csf2p	POLY1/metal1/metal2 fringe capacitor	-	-	6.1
csf3p	POLY1/metal1/metal2/metal3 fringe capacitor	MET3	-	6.1
cif3a	30V metal1/metal2/metal3 fringe capacitor	MET3	-	12.0
csf3	10V metal1/metal2/metal3 fringe capacitor	MET3	-	6.0
csf3a	60V metal1/metal2/metal3 fringe capacitor	MET3	-	6.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cif4a	30V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	12.0
csf4	10V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	6.0
csf4a	60V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	6.0
cif5a	30V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	12.0
csf5	10V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	6.0
csf5a	60V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	6.0
cift4a <sup>(1)</sup>	30V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	12.0
csft4	10V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	6.0
csft4a	60V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	6.0
cift5a <sup>(1)</sup>	30V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	12.0
csft5	10V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	6.0
csft5a	60V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	6.0
cift6a <sup>(1)</sup>	30V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	12.0
csft6	10V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	6.0
csft6a	60V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	6.0
cmm3	single MIM capacitor between metal2 and metal3	MET3 and MIM23	-	7.0
cmm4	single MIM capacitor between metal3 and metal4	MET4 and MIM34	-	6.0
cmm5	single MIM capacitor between metal4 and metal5	MET5 and MIM45	-	7.0
cmm3t	single MIM capacitor between metal 2 and metaltop	METMID and MIM	MET3	6.0
cmm4t	single MIM capacitor between metal3 and metaltop	MET3 and METMID and MIM	MET4	6.0
cmm5t	single MIM capacitor between metal4 and metaltop	MET4 and METMID and MIM	MET5	6.0
cmm6t	single MIM capacitor between metal5 and metaltop	MET5 and METMID and MIM	-	6.0
cmmh3	single MIM capacitor (high capacitance) between metal2 and metal3	MET3 and MIMH23	-	7.0
cmmh4	single MIM capacitor (high capacitance) between metal3 and metal4	MET4 and MIMH34	-	7.0
cmmh5	single MIM capacitor (high capacitance) between metal4 and metal5	MET5 and MIMH45	-	7.0



## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cmmh3t	single MIM capacitor (high capacitance) between metal2 and metaltop	METMID and MIMH	MET3	6.0
cmmh4t	single MIM capacitor (high capacitance) between metal3 and metaltop	MET3 and METMID and MIMH	MET4	6.0
cmmh5t	single MIM capacitor (high capacitance) between metal4 and metaltop	MET4 and METMID and MIMH	MET5	6.0
cmmh6t	single MIM capacitor (high capacitance) between metal5 and metaltop	MET5 and METMID and MIMH	-	6.0
cdmm4	double MIM capacitor between metal2, metal3 and metal4	MET4 and DMIM	-	6.0
cdmm4t	double MIM capacitor between metal2, metal3 and metaltop	MET3 and METMID and DMIM	MET4	6.0
cdmmh4	double MIM capacitor (high capacitance) between metal2, metal3 and metal4	MET4 and DMIMH	-	6.0
cdmmh4t	double MIM capacitor (high capacitance) between metal2, metal3 and metaltop	MET3 and METMID and DMIMH	MET4	6.0
cdmm5	double MIM capacitor between metal3, metal4 and metal5	MET5 and DMIM3	-	7.0
cdmm5t	double MIM capacitor between metal3, metal4 and metaltop	MET4 and METMID and DMIM3	MET5	7.0
ctmm5	triple MIM capacitor between metal2, metal3, metal4 and metal5	MET5 and TMIM	-	6.0
cdmmh5	double MIM capacitor (high capacitance) between metal3, metal4 and metal5	MET5 and DMIMH3	-	7.0
ctmm5t	triple MIM capacitor between metal2, metal3, metal4 and metaltop	MET4 and METMID and TMIM	MET5	6.0
cdmmh5t	double MIM capacitor (high capacitance) between metal3, metal4 and metaltop	MET4 and METMID and DMIMH3	MET5	7.0
ctmmh5	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metal5	MET5 and TMIMH	-	6.0
ctmmh5t	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metaltop	MET4 and METMID and TMIMH	MET5	6.0
cmmh4l	single MIM capacitor (high capacitance) between metal3 and metal thick	MIMH and MET3 and METTHK	MET4 or METMID	6.0
cmmh5l	single MIM capacitor (high capacitance) between metal4 and metal thick	MIMH and MET4 and METTHK	MET5 or METMID	6.0
cmmh6l	single MIM capacitor (high capacitance) between metal5 and metal thick	MIMH and MET5 and METTHK	METMID	6.0

**Note 1** This device is under development. All values represent the status which have been obtained during the development phase and are subject to change.

**Diodes**

Name	Description	Required modules	Model rev.
dn	diode NDIFF / PWELL1,3,5 (1.8V)	-	7.0

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ Diodes

Name	Description	Required modules	Model rev.
dnn <sup>(1)</sup>	diode NDIFF / PTUB_SUB (1.8V)	-	7.0
dp	diode PDIFF / NWELL1,3,5 (1.8V)	-	7.0
dnw	diode NWELL1,3,5 / PWELL1 (1.8V)	-	7.0
dn5	diode NDIFF / PWELL2 (5.0V)	-	7.0
dnn5 <sup>(1)</sup>	diode NDIFF / PTUB_SUB (5.0V)	-	7.0
dp5	diode PDIFF / NWELL2 (5.0V)	-	7.0
dnw5	diode NWELL2 / PWELL2 (5.0V)	-	7.0
dfwdpa	5.0V rectifier p+/n diode	DTI and PSUB and HVN and DNC	7.0
dfwdn5	6.0V rectifier n+/p diode	DTI and PSUB	10.0
dfwdnb	12V rectifier diode	DTI and NMV	9.0
dfwdnc	15V rectifier diode	DTI and NMV	9.0
dfwdnd	20V rectifier diode	DTI and NMV	9.0
dfwdnt	40V rectifier diode	DTI and PSUB and NHVA	10.0
dfwdnu	60V rectifier diode	DTI and PSUB and NHVA	10.0
dfwdnhc	70V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhd	85V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhe	100V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhf	125V rectifier diode	DTI and PSUB and NHVR	9.0
dfwnsj1_7	100V Gen 1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1_10	140V Gen 1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1_16c	200V Gen1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1b_2	45V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_4	72V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_5	95V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_7	115V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_8	140V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1b_10	155V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_13	195V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_16	235V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_20	290V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	12.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ Diodes

Name	Description	Required modules	Model rev.
dfwnsj1a_28	375V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVU	12.0
dhw2a	100V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw2	140V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw3	200V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw2b	115V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw2c	160V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw3c	235V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw4c	280V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVM	11.0
dhw4d	360V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVU	11.0
dhw5d	420V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVU	11.0
ds5a	5V Schottky diode	HVN and DTI	12.0
ds5b <sup>(2)</sup>	5V Schottky diode	PSUB and DTI	12.0
dpp6	6V P-type protection diode (DTI)	HVN and DNC and DTI	10.0
dnp7	7V N-type protection diode (DTI)	DPC and DTI	12.0
dpp7	7V P-type protection diode (DTI)	HVN and DNC and DTI	10.0
dnpa	8V N-type protection diode	PSUB and (DIODEA or NHVA or NHVR)	11.0
dnpati	8V N-type protection diode (DTI)	DTI and PSUB and (DIODEA or NHVA or NHVR)	11.0
dza <sup>(3)</sup>	5.3V Zener diode, 2 terminals	PSUB and DIODEB	10.0
dzati <sup>(3)</sup>	5.3V Zener diode (DTI), 2 terminals	DTI and PSUB and DIODEB	11.1
dzbt <sup>(3)</sup>	5.3V Zener diode (DTI), 3 terminals	DTI and PSUB and DIODEC	7.0
dzcti <sup>(4)(3)</sup>	5.3V Zener diode (DTI), 2 terminals	DTI and PSUB and DIODEC	12.0
dfwdnha <sup>(5)</sup>	diode drain / bulk for nhvra	DTI and PSUB and NHVR	8.0
dfwdnhb <sup>(5)</sup>	diode drain / bulk for nhvrb	DTI and PSUB and NHVR	8.0
dfwdpta <sup>(5)</sup>	diode drain / bulk for phvta	DTI and PSUB and PHVA	10.0
dfwdptb <sup>(5)</sup>	diode drain / bulk for phvtb	DTI and PSUB and PHVA	10.0
dfwdpdu <sup>(5)</sup>	diode drain / bulk for phvu	DTI and PSUB and PHVA	10.0
dfwdgne <sup>(5)</sup>	diode drain / bulk for nmve	DTI and NMV	9.0
dfwddnf <sup>(5)</sup>	diode drain / bulk for nmvf	DTI and NMV	9.0
dfwdpaa <sup>(5)</sup>	diode drain / bulk for pmvaa	DTI	12.0
dfwdpab <sup>(5)</sup>	diode drain / bulk for pmvab	DTI	12.0
dfwdpbb <sup>(5)</sup>	diode drain / bulk for pmvb	DTI and PSUB and PMV	11.0
dfwdpd <sup>(5)</sup>	diode drain / bulk for pmvd	DTI and PSUB and PMV	10.0
dfwdpe <sup>(5)</sup>	diode drain / bulk for pmve	DTI and PSUB and PMV	8.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ Diodes

Name	Description	Required modules	Model rev.
dfwdpf <sup>(5)</sup>	diode drain / bulk for pmvf	DTI and PSUB and PMV	8.0
dfwdpha <sup>(5)</sup>	diode drain / bulk for phvra	DTI and PSUB and PHVR	8.0
dfwdphb <sup>(5)</sup>	diode drain / bulk for phvrb	DTI and PSUB and PHVR	8.0
dfwdphc <sup>(5)</sup>	diode drain / bulk for phvrc	DTI and PSUB and PHVR	8.0
dfwdphd <sup>(5)</sup>	diode drain / bulk for phvrd	DTI and PSUB and PHVR	9.0
dfwdphe <sup>(5)</sup>	diode drain / bulk for phvre	DTI and PSUB and PHVR	9.0
dfwdphf <sup>(5)</sup>	diode drain / bulk for phvrf	DTI and PSUB and PHVR	8.1
dfwpsj1_7 <sup>(5)</sup>	diode drain / bulk for phsj1_7	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj1_10 <sup>(5)</sup>	diode drain / bulk for phsj1_10	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj1_16c <sup>(5)</sup>	diode drain / bulk for phsj1_16c	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj2b_7 <sup>(5)</sup>	diode drain / bulk for phsj2b_7	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj2b_8 <sup>(5)</sup>	diode drain / bulk for phsj2b_8	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_10 <sup>(5)</sup>	diode drain / bulk for phsj2b_10	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_13 <sup>(5)</sup>	diode drain / bulk for phsj2b_13	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_16 <sup>(5)</sup>	diode drain / bulk for phsj2b_16	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_4 <sup>(5)</sup>	diode drain / bulk for phsj1a_4	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_5 <sup>(5)</sup>	diode drain / bulk for phsj1a_5	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_7 <sup>(5)</sup>	diode drain / bulk for phsj1a_7	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_8 <sup>(5)</sup>	diode drain / bulk for phsj1a_8	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_10 <sup>(5)</sup>	diode drain / bulk for phsj1a_10	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_13 <sup>(5)</sup>	diode drain / bulk for phsj1a_13	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_16 <sup>(5)</sup>	diode drain / bulk for phsj1a_16	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_20 <sup>(5)</sup>	diode drain / bulk for phsj1a_20	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	11.0
dfwpsj1a_31 <sup>(5)</sup>	diode drain / bulk for phsj1a_31	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	11.0
dfwdnaa <sup>(5)</sup>	diode drain / bulk for nmvaa	DTI	12.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ Diodes

Name	Description	Required modules	Model rev.
dfwdnab <sup>(5)</sup>	diode drain / bulk for nmvab	DTI	12.0

**Note 1** This diode is only available along with the corresponding transistor where it is used as source/drain**Note 2** ds5b provides a similar device to ds5a but with a lower mask count**Note 3** Please also refer to the "[xt018-ApplicationNote-Zener\\_Diodes](#)" available in "my X-FAB".**Note 4** dzcti provides a similar device to dzbt1 but with a smaller pitch**Note 5** This device can only be used as a parasitic diode of the transistor noted in the description**Memories**

Name	Description	Required modules	Model rev.
pfuse	polysilicon fuse	-	5.0

**IGBTs**

Name	Description	Required modules	Model rev.
nisj1_16	200V Gen1 SJ NIGBT	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and NBUF and DPC	12.0

**Virtual devices**

Name	Description	Required modules	Model rev.
tag_m400v <sup>(1)</sup>	defines voltage class for net < -300V	-	11.0
tag_m300v <sup>(1)</sup>	defines voltage class for net $\geq$ -300V < -200V	-	11.0
tag_m200v <sup>(1)</sup>	defines voltage class for net $\geq$ -200V < -100V	-	7.0
tag_m100v <sup>(1)</sup>	defines voltage class for net $\geq$ -100V < -60V	-	7.0
tag_m60v <sup>(1)</sup>	defines voltage class for net $\geq$ -60V < -25V	-	7.0
tag_m25v <sup>(1)</sup>	defines voltage class for net $\geq$ -25V < 0V	-	7.0
tag_25v <sup>(1)</sup>	defines voltage class for net $\geq$ 0V $\leq$ 25V	-	7.0
tag_60v <sup>(1)</sup>	defines voltage class for net >25V $\leq$ 60V	-	7.0
tag_100v <sup>(1)</sup>	defines voltage class for net >60V $\leq$ 100V	-	7.0
tag_200v <sup>(1)</sup>	defines voltage class for net >100V $\leq$ 200V	-	7.0
tag_300v <sup>(1)</sup>	defines voltage class for net > 200V $\leq$ 300V	-	11.0
tag_400v <sup>(1)</sup>	defines voltage class for net > 300V	-	11.0

**Note 1** These devices are not fabricated on silicon; they are available for DRC and LVS voltage class checks only. For further information, please refer to the design related guideline "Voltage class definitions".**ESD devices**

Name	Description	Required modules	Model rev.
rdn5_dpc <sup>(1)</sup>	NDIFF drain ballast resistor of ESD NMOS (DPC in PWELL2)	DPC	6.0
rdn5_pw4 <sup>(1)</sup>	NDIFF drain ballast resistor of ESD NMOS (PWELL4 in PWELL2)	NHVA or DIODEA or NHVR	6.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.1 LP5MOS main module→ ESD devices

Name	Description	Required modules	Model rev.
rnw_scr <sup>(1)</sup>	1.8V LV NMOS triggered SCR dio/res network resistor	-	10.0
rnw5_scr <sup>(1)</sup>	5V LV NMOS triggered SCR dio/res network resistor	-	10.0

**Note 1** These devices are only allowed to be used for ESD protection.  
 Please refer to ESD documentation on "my X-FAB":  
["XT018-DesignGuideline-ESD\\_and\\_LU"](#)  
["XT018 TLP Characteristics"](#)  
["XT018 Technical Report MOS TLP Characteristics"](#)  
["XT018 Technical Report UHV TLP Characteristics"](#)

**2.5.2 MOS5 main module****MOS transistors**

Name	Description	Required modules	Model rev.
ne5	5.0V NMOS	-	12.0
nn5	5.0V native Vt NMOS	-	10.0
pe5	5.0V PMOS	-	12.0
pe5_5 <sup>(1)</sup>	5.0V PMOS, 5 terminals	-	12.0
pe5ti	5.0V PMOS (NTUB)	DTI and HVN	12.0
nd5	5.0V depletion NMOS	DEPL	10.0
nmva <sup>(2)(3)</sup>	10V drain extension NMOS	DTI	
nmvaa <sup>(3)</sup>	10V drain extension NMOS	DTI	12.0
nmvab <sup>(3)</sup>	10V drain extension NMOS, with drain ballast resistor	DTI	12.0
nmvb	12V NMOS	DTI and NMV	11.0
nmvc	15V NMOS	DTI and NMV	11.0
nmvd	20V NMOS	DTI and NMV	11.0
nmve	25V NMOS	DTI and NMV	11.0
nmvf	32V NMOS	DTI and NMV	11.0
ndmvd	20V depletion NMOS	DTI and DEPL and NMV	11.0
ndmvf	32V depletion NMOS	DTI and DEPL and NMV	11.0
pmva <sup>(4)(3)</sup>	10V drain extension PMOS	DTI	
pmvaa <sup>(3)</sup>	10V drain extension PMOS	DTI	12.0
pmvab <sup>(3)</sup>	10V drain extension PMOS, with drain ballast resistor	DTI	12.0
pmvb	12V PMOS	DTI and PSUB and PMV	11.0
pmvd	18V PMOS	DTI and PSUB and PMV	11.0
pmve	25V PMOS	DTI and PSUB and PMV	11.0
pmvf	32V PMOS	DTI and PSUB and PMV	11.0
nhvta <sup>(5)</sup>	Low Ron 40V NMOS	DTI and PSUB and NHVA	11.0
nhvtaa <sup>(6)(5)</sup>	Low Ron 40V NMOS	DTI and PSUB and NHVA	11.0
nhvtb <sup>(5)</sup>	40V NMOS	DTI and PSUB and NHVA	11.0
nhvu <sup>(5)</sup>	60V NMOS	DTI and PSUB and NHVA	11.0
ndhvt <sup>(5)</sup>	40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ MOS transistors

Name	Description	Required modules	Model rev.
ndhvta <sup>(5)</sup>	Low Ron 40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
ndhvtaa <sup>(7)(5)</sup>	Low Ron 40V depletion NMOS	DTI and PSUB and NHVA and DEPL	11.1
phvta	Low Ron 40V PMOS	DTI and PSUB and PHVA	11.1
phvtb	40V PMOS	DTI and PSUB and PHVA	11.1
phvu	60V PMOS	DTI and PSUB and PHVA	11.1
nhvra <sup>(8)</sup>	40V NMOS	DTI and PSUB and NHVR	10.0
nhvrb <sup>(8)</sup>	60V NMOS	DTI and PSUB and NHVR	10.0
nhvrc <sup>(8)</sup>	70V NMOS	DTI and PSUB and NHVR	10.0
nhvrd <sup>(8)</sup>	85V NMOS	DTI and PSUB and NHVR	10.0
nhvre <sup>(8)</sup>	100V NMOS	DTI and PSUB and NHVR	10.0
nhvrf <sup>(9)</sup>	125V NMOS	DTI and PSUB and NHVR	10.0
ndhvrd <sup>(8)</sup>	85V depletion NMOS	DTI and PSUB and NHVR and HVDEPL	10.0
ndhvrf <sup>(9)</sup>	125V depletion NMOS	DTI and PSUB and NHVR and HVDEPL	10.0
phvra <sup>(8)</sup>	40V PMOS	DTI and PSUB and PHVR	10.0
phvrb <sup>(8)</sup>	60V PMOS	DTI and PSUB and PHVR	10.0
phvrc <sup>(8)</sup>	70V PMOS	DTI and PSUB and PHVR	10.0
phvrd <sup>(8)</sup>	85V PMOS	DTI and PSUB and PHVR	10.0
phvre <sup>(8)</sup>	100V PMOS	DTI and PSUB and PHVR	10.0
phvrf <sup>(9)</sup>	125V PMOS	DTI and PSUB and PHVR	10.0
nhsj1_7	100V Gen1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1_10	140V Gen 1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1_16c	200V Gen1 SJ NMOS	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and DPC	11.1
nhsj1b_2	45V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_4	72V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_5	95V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_7	115V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVL	12.0
nhsj1b_8	140V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1b_10	155V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_13	195V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ MOS transistors

Name	Description	Required modules	Model rev.
nhsj1a_16	235V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVM	12.0
nhsj1a_20	290V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVU	12.0
nhsj1a_28	375V Gen2 SJ NMOS	DTI and PSUB and SJ1XN and HVN and HVP and HWC and NBUR and DPC and SJHVU	12.0
phsj1_7	100V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj1_10	140V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj1_16c	200V Gen1 SJ PMOS	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	11.1
phsj2b_7	115V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
phsj2b_8	140V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_10	155V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_13	195V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
phsj2b_16	235V Gen2 Low Ron SJ PMOS	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_4	72V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_5	95V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_7	115V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	12.0
phsj1a_8	140V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_10	155V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_13	195V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_16	235V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	12.0
phsj1a_20	290V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	12.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ MOS transistors

Name	Description	Required modules	Model rev.
phsj1a_31	375V Gen2 SJ PMOS	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVU	12.0

- Note 1** This device is a variant of the corresponding basic device with connections to the underlying wells. Parameters of this device are identical to the corresponding basic device.
- Note 2** The device nmva is superseded by nmvaa. nmva must not be used for any new designs.
- Note 3** Please also refer to the "[xt018-ApplicationNote-10V\\_MOSFET](#)" available on "my X-FAB".
- Note 4** The device pmva is superseded by pmvaa. pmva must not be used for any new designs.
- Note 5** Please also refer to the "[xt018-ApplicationNote-NHVA\\_Module\\_HV\\_Transistors](#)" available on "my X-FAB".
- Note 6** nhvtaa provides better avalanche robustness than nhvta
- Note 7** ndhvtaa provides better avalanche robustness than ndhvta
- Note 8** The ESD design window may not be sufficient for applications using the maximum operating voltage of the device. To increase the ESD design window for a particular operating voltage, the primitive device of the next voltage class should be used as an alternative.
- Note 9** This device is intended to enhance the ESD design window for 100V applications. The ESD design window may not be suitable for applications up to 125V.

**Bipolar transistors**

Name	Description	Required modules	Model rev.
qpva5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 2 μm x 2 μm	PSUB	5.0
qpvb5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 5 μm x 5 μm	PSUB	5.0
qpvc5	5.0V vertical PNP bipolar transistor in PEPI; emitter area = 10 μm x 10 μm	PSUB	5.0
qpve5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 2 μm x 2 μm	-	5.0
qpvf5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 5 μm x 5 μm	-	5.0
qpgv5	5.0V vertical PNP bipolar transistor in PTUB_SUB; emitter area = 10 μm x 10 μm	-	5.0
qnv5	5V high gain NPN bipolar transistor	DTI and PSUB and BJTC	5.0
qpv5	5V high gain PNP bipolar transistor	DTI and PSUB and BJTA	5.0
qnvha	25V high gain NPN bipolar transistor	DTI and PSUB and BJTC	10.0
qpvha	25V high gain PNP bipolar transistor	DTI and PSUB and BJTA	10.0

**Resistors**

Name	Description	Required modules	Model rev.
rxw2ti	NWELL Resistor under active (DTI)	DTI and PSUB	10.0
rdn5	5.0V NDIFF / PWELL2 resistor (non salicided)	-	6.0
rdp5	5.0V PDIFF / NWELL2 resistor (non salicided)	-	10.0
rnw5	5.0V NWELL2 / PSUB resistor (STI terminated)	-	10.0
rnp1 <sup>(1)</sup>	N-doped POLY1 resistor (non salicided), 2 terminals	-	12.0
rnp1_3 <sup>(2)</sup>	N-doped POLY1 resistor (non-salicided, underlying NWELL/PWELL2), 3 terminals	-	12.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ Resistors

Name	Description	Required modules	Model rev.
rpp1 <sup>(1)</sup>	P-doped POLY1 resistor (non-salicided), 2 terminals	-	12.0
rpp1_3 <sup>(2)</sup>	P-doped POLY1 resistor (non-salicided, underlying PWELL), 3 terminals	-	12.0
rpp1nw_3 <sup>(2)</sup>	P-doped POLY1 resistor (non-salicided, underlying NWELL), 3 terminals	-	12.0
rpp1s	salicided P-doped POLY1 resistor, 2 terminals	-	10.0
rpp1s_3 <sup>(3)</sup>	salicided P-doped POLY1 resistor, 3 terminals	-	10.0
rnp1h	high ohmic N-doped POLY1 resistor (non salicided), 2 terminals	HRPOLY	10.0
rnp1h_3 <sup>(3)</sup>	high ohmic N-doped POLY1 resistor (non salicided), 3 terminals	HRPOLY	10.0
rpp1k1	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.0
rpp1k1_3 <sup>(3)</sup>	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.0
rpp1k1a	lightly P-doped POLY1 resistor (non salicided), 2 terminals	MRPOLY	6.0
rpp1k1a_3 <sup>(3)</sup>	lightly P-doped POLY1 resistor (non salicided), 3 terminals	MRPOLY	6.0
rm1	metal 1 resistor	-	6.0
rm2	metal 2 resistor	-	6.0
rm3	metal 3 resistor	MET3	6.0
rm4	metal 4 resistor	MET4	6.0
rm5	metal 5 resistor	MET5	6.0
rmtpl	top metal resistor	METMID	6.0
rmtpl	thick metal resistor	METTHK	6.0
rnrld	thick copper redistribution resistor	THKCOP	4.1

**Note 1** The 2-terminal poly resistor devices do not consider the underlying wells. As a result of this simplification, the models are less accurate than their 3-terminal counterparts, which do account for the underlying well configuration.

**Note 2** These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency.

**Note 3** These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency. Parameters of these devices are identical to the corresponding basic device.

## Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
mosvc5	5V N-type Varactor	-	-	5.0
mosvc5ti	5V P-type Varactor (DTI)	DTI	-	5.0
csandwt3	POLY1 / metal1/ metal2/ metal3 capacitor	MET3	-	6.0
csandwt4	POLY1 / metal1/ metal2/ metal3/ metal4 capacitor	MET4	-	6.0
csandwt5	POLY1 / metal1/ metal2/ metal3/ metal4/ metal5 capacitor	MET5	-	6.0



## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
csp5tl_3	300V active/ metal 1/ metal 2/ metal 3/ metal 4/ top metal/ thick metal capacitor, 3 terminals	CSP5L	MET5	12.0
csp5tla_3	400V active/ metal 2/ metal 4/ thick metal capacitor, 3 terminals	CSP5L	MET5	12.0
cif3	100V metal1/metal2/metal3 fringe capacitor	MET3	-	8.0
cif4	100V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	8.0
cif5	100V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	8.0
cift4	100V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	9.0
cift5	100V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	9.0
cift6	100V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	9.0
csf2p	POLY1/metal1/metal2 fringe capacitor	-	-	6.1
csf3p	POLY1/metal1/metal2/metal3 fringe capacitor	MET3	-	6.1
cif3a	30V metal1/metal2/metal3 fringe capacitor	MET3	-	12.0
csf3	10V metal1/metal2/metal3 fringe capacitor	MET3	-	6.0
csf3a	60V metal1/metal2/metal3 fringe capacitor	MET3	-	6.0
cif4a	30V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	12.0
csf4	10V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	6.0
csf4a	60V metal1/metal2/metal3/metal4 fringe capacitor	MET4	-	6.0
cif5a	30V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	12.0
csf5	10V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	6.0
csf5a	60V metal1/metal2/metal3/metal4/metal5 fringe capacitor	MET5	-	6.0
cift4a <sup>(1)</sup>	30V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	12.0
csft4	10V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	6.0
csft4a	60V metal1/metal2/metal3/metaltop fringe capacitor	MET3 and METMID	MET4	6.0
cift5a <sup>(1)</sup>	30V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	12.0
csft5	10V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	6.0
csft5a	60V metal1/metal2/metal3/metal4/metaltop fringe capacitor	MET4 and METMID	MET5	6.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cift6a <sup>(1)</sup>	30V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	12.0
csft6	10V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	6.0
csft6a	60V metal1/metal2/metal3/metal4/metal5/metaltop fringe capacitor	MET5 and METMID	-	6.0
cmm3	single MIM capacitor between metal2 and metal3	MET3 and MIM23	-	7.0
cmm4	single MIM capacitor between metal3 and metal4	MET4 and MIM34	-	6.0
cmm5	single MIM capacitor between metal4 and metal5	MET5 and MIM45	-	7.0
cmm3t	single MIM capacitor between metal 2 and metaltop	METMID and MIM	MET3	6.0
cmm4t	single MIM capacitor between metal3 and metaltop	MET3 and METMID and MIM	MET4	6.0
cmm5t	single MIM capacitor between metal4 and metaltop	MET4 and METMID and MIM	MET5	6.0
cmm6t	single MIM capacitor between metal5 and metaltop	MET5 and METMID and MIM	-	6.0
cmmh3	single MIM capacitor (high capacitance) between metal2 and metal3	MET3 and MIMH23	-	7.0
cmmh4	single MIM capacitor (high capacitance) between metal3 and metal4	MET4 and MIMH34	-	7.0
cmmh5	single MIM capacitor (high capacitance) between metal4 and metal5	MET5 and MIMH45	-	7.0
cmmh3t	single MIM capacitor (high capacitance) between metal2 and metaltop	METMID and MIMH	MET3	6.0
cmmh4t	single MIM capacitor (high capacitance) between metal3 and metaltop	MET3 and METMID and MIMH	MET4	6.0
cmmh5t	single MIM capacitor (high capacitance) between metal4 and metaltop	MET4 and METMID and MIMH	MET5	6.0
cmmh6t	single MIM capacitor (high capacitance) between metal5 and metaltop	MET5 and METMID and MIMH	-	6.0
cdmm4	double MIM capacitor between metal2, metal3 and metal4	MET4 and DMIM	-	6.0
cdmm4t	double MIM capacitor between metal2, metal3 and metaltop	MET3 and METMID and DMIM	MET4	6.0
cdmmh4	double MIM capacitor (high capacitance) between metal2, metal3 and metal4	MET4 and DMIMH	-	6.0
cdmmh4t	double MIM capacitor (high capacitance) between metal2, metal3 and metaltop	MET3 and METMID and DMIMH	MET4	6.0
cdmm5	double MIM capacitor between metal3, metal4 and metal5	MET5 and DMIM3	-	7.0
cdmm5t	double MIM capacitor between metal3, metal4 and metaltop	MET4 and METMID and DMIM3	MET5	7.0
ctmm5	triple MIM capacitor between metal2, metal3, metal4 and metal5	MET5 and TMIM	-	6.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ Capacitors

Name	Description	Required modules	Forbidden modules	Model rev.
cdmmh5	double MIM capacitor (high capacitance) between metal3, metal4 and metal5	MET5 and DMIMH3	-	7.0
ctmm5t	triple MIM capacitor between metal2, metal3, metal4 and metatop	MET4 and METMID and TMIM	MET5	6.0
cdmmh5t	double MIM capacitor (high capacitance) between metal3, metal4 and metatop	MET4 and METMID and DMIMH3	MET5	7.0
ctmmh5	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metal5	MET5 and TMIMH	-	6.0
ctmmh5t	triple MIM capacitor (high capacitance) between metal2, metal3, metal4 and metatop	MET4 and METMID and TMIMH	MET5	6.0
cmmh4l	single MIM capacitor (high capacitance) between metal3 and metal thick	MIMH and MET3 and METTHK	MET4 or METMID	6.0
cmmh5l	single MIM capacitor (high capacitance) between metal4 and metal thick	MIMH and MET4 and METTHK	MET5 or METMID	6.0
cmmh6l	single MIM capacitor (high capacitance) between metal5 and metal thick	MIMH and MET5 and METTHK	METMID	6.0

**Note 1** This device is under development. All values represent the status which have been obtained during the development phase and are subject to change.

**Diodes**

Name	Description	Required modules	Model rev.
dn5	diode NDIFF / PWELL2 (5.0V)	-	7.0
dnn5 <sup>(1)</sup>	diode NDIFF / PTUB_SUB (5.0V)	-	7.0
dp5	diode PDIFF / NWELL2 (5.0V)	-	7.0
dnw5	diode NWELL2 / PWELL2 (5.0V)	-	7.0
dfwdpa	5.0V rectifier p+/n diode	DTI and PSUB and HVN and DNC	7.0
dfwdn5	6.0V rectifier n+/p diode	DTI and PSUB	10.0
dfwdnb	12V rectifier diode	DTI and NMV	9.0
dfwdnc	15V rectifier diode	DTI and NMV	9.0
dfwdnd	20V rectifier diode	DTI and NMV	9.0
dfwdnt	40V rectifier diode	DTI and PSUB and NHVA	10.0
dfwdnu	60V rectifier diode	DTI and PSUB and NHVA	10.0
dfwdnhc	70V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhd	85V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhe	100V rectifier diode	DTI and PSUB and NHVR	8.0
dfwdnhf	125V rectifier diode	DTI and PSUB and NHVR	9.0
dfwnsj1_7	100V Gen 1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1_10	140V Gen 1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0
dfwnsj1_16c	200V Gen1 SJ diode	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR	10.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ Diodes

Name	Description	Required modules	Model rev.
dfwnsj1b_2	45V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_4	72V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_5	95V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_7	115V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVL	11.0
dfwnsj1b_8	140V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1b_10	155V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_13	195V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_16	235V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	11.0
dfwnsj1a_20	290V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	12.0
dfwnsj1a_28	375V Gen2 SJ diode	DTI and PSUB and HVN and HVP and HWC and NBUR and SJ1XN and SJHVM	12.0
dhw2a	100V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw2	140V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw3	200V Gen1 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR	5.0
dhw2b	115V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw2c	160V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw3c	235V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVL	11.0
dhw4c	280V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVM	11.0
dhw4d	360V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVM	11.0
dhw5d	420V Gen2 handle wafer diode	DTI and PSUB and HVN and HWC and NBUR and SJHVM	11.0
ds5a	5V Schottky diode	HVN and DTI	12.0
ds5b <sup>(2)</sup>	5V Schottky diode	PSUB and DTI	12.0
dpp6	6V P-type protection diode (DTI)	HVN and DNC and DTI	10.0
dnp7	7V N-type protection diode (DTI)	DPC and DTI	12.0
dpp7	7V P-type protection diode (DTI)	HVN and DNC and DTI	10.0
dnpa	8V N-type protection diode	PSUB and (DIODEA or NHVA or NHVR)	11.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ Diodes

Name	Description	Required modules	Model rev.
dnpati	8V N-type protection diode (DTI)	DTI and PSUB and (DIODEA or NHVA or NHVR)	11.0
dza <sup>(3)</sup>	5.3V Zener diode, 2 terminals	PSUB and DIODEB	10.0
dzati <sup>(3)</sup>	5.3V Zener diode (DTI), 2 terminals	DTI and PSUB and DIODEB	11.1
dzbt <sup>(3)</sup>	5.3V Zener diode (DTI), 3 terminals	DTI and PSUB and DIODEC	7.0
dzcti <sup>(4)(3)</sup>	5.3V Zener diode (DTI), 2 terminals	DTI and PSUB and DIODEC	12.0
dfwdnha <sup>(5)</sup>	diode drain / bulk for nhvra	DTI and PSUB and NHVR	8.0
dfwdnhb <sup>(5)</sup>	diode drain / bulk for nhvrb	DTI and PSUB and NHVR	8.0
dfwdpta <sup>(5)</sup>	diode drain / bulk for phvta	DTI and PSUB and PHVA	10.0
dfwdptb <sup>(5)</sup>	diode drain / bulk for phvtb	DTI and PSUB and PHVA	10.0
dfwdpdu <sup>(5)</sup>	diode drain / bulk for phvu	DTI and PSUB and PHVA	10.0
dfwdgne <sup>(5)</sup>	diode drain / bulk for nmve	DTI and NMV	9.0
dfwdnfv <sup>(5)</sup>	diode drain / bulk for nmvf	DTI and NMV	9.0
dfwdpaa <sup>(5)</sup>	diode drain / bulk for pmvaa	DTI	12.0
dfwdpab <sup>(5)</sup>	diode drain / bulk for pmvab	DTI	12.0
dfwdpb <sup>(5)</sup>	diode drain / bulk for pmvb	DTI and PSUB and PMV	11.0
dfwdpd <sup>(5)</sup>	diode drain / bulk for pmvd	DTI and PSUB and PMV	10.0
dfwdpe <sup>(5)</sup>	diode drain / bulk for pmve	DTI and PSUB and PMV	8.0
dfwdpf <sup>(5)</sup>	diode drain / bulk for pmvf	DTI and PSUB and PMV	8.0
dfwdpha <sup>(5)</sup>	diode drain / bulk for phvra	DTI and PSUB and PHVR	8.0
dfwdphb <sup>(5)</sup>	diode drain / bulk for phvrb	DTI and PSUB and PHVR	8.0
dfwdphc <sup>(5)</sup>	diode drain / bulk for phvrc	DTI and PSUB and PHVR	8.0
dfwdphd <sup>(5)</sup>	diode drain / bulk for phvrd	DTI and PSUB and PHVR	9.0
dfwdphe <sup>(5)</sup>	diode drain / bulk for phvre	DTI and PSUB and PHVR	9.0
dfwdphf <sup>(5)</sup>	diode drain / bulk for phvrf	DTI and PSUB and PHVR	8.1
dfwpsj1_7 <sup>(5)</sup>	diode drain / bulk for phsj1_7	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj1_10 <sup>(5)</sup>	diode drain / bulk for phsj1_10	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj1_16c <sup>(5)</sup>	diode drain / bulk for phsj1_16c	DTI and PSUB and 1XP and HVN and HVP and HWC and NBUR and DNC	10.0
dfwpsj2b_7 <sup>(5)</sup>	diode drain / bulk for phsj2b_7	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj2b_8 <sup>(5)</sup>	diode drain / bulk for phsj2b_8	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_10 <sup>(5)</sup>	diode drain / bulk for phsj2b_10	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_13 <sup>(5)</sup>	diode drain / bulk for phsj2b_13	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj2b_16 <sup>(5)</sup>	diode drain / bulk for phsj2b_16	DTI and PSUB and 2XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_4 <sup>(5)</sup>	diode drain / bulk for phsj1a_4	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0

⇒

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ Diodes

Name	Description	Required modules	Model rev.
dfwpsj1a_5 <sup>(5)</sup>	diode drain / bulk for phsj1a_5	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_7 <sup>(5)</sup>	diode drain / bulk for phsj1a_7	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_8 <sup>(5)</sup>	diode drain / bulk for phsj1a_8	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_10 <sup>(5)</sup>	diode drain / bulk for phsj1a_10	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_13 <sup>(5)</sup>	diode drain / bulk for phsj1a_13	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_16 <sup>(5)</sup>	diode drain / bulk for phsj1a_16	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVM	11.0
dfwpsj1a_20 <sup>(5)</sup>	diode drain / bulk for phsj1a_20	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwpsj1a_31 <sup>(5)</sup>	diode drain / bulk for phsj1a_31	DTI and PSUB and SJ1XP and HVN and HWC and NBUR and DNC and SJHVL	11.0
dfwdnaa <sup>(5)</sup>	diode drain / bulk for nmvaa	DTI	12.0
dfwdnab <sup>(5)</sup>	diode drain / bulk for nmvab	DTI	12.0

**Note 1** This diode is only available along with the corresponding transistor where it is used as source/drain

**Note 2** ds5b provides a similar device to ds5a but with a lower mask count

**Note 3** Please also refer to the "[xt018-ApplicationNote-Zener\\_Diodes](#)" available in "my X-FAB".

**Note 4** dzcti provides a similar device to dzbt1 but with a smaller pitch

**Note 5** This device can only be used as a parasitic diode of the transistor noted in the description

## Memories

Name	Description	Required modules	Model rev.
pfuse	polysilicon fuse	-	5.0

## IGBTs

Name	Description	Required modules	Model rev.
nisj1_16	200V Gen1 SJ NIGBT	DTI and PSUB and 1XN and HVN and HVP and HWC and NBUR and NBUF and DPC	12.0

## Virtual devices

Name	Description	Required modules	Model rev.
tag_m400v <sup>(1)</sup>	defines voltage class for net < -300V	-	11.0
tag_m300v <sup>(1)</sup>	defines voltage class for net $\geq$ -300V < -200V	-	11.0
tag_m200v <sup>(1)</sup>	defines voltage class for net $\geq$ -200V < -100V	-	7.0
tag_m100v <sup>(1)</sup>	defines voltage class for net $\geq$ -100V < -60V	-	7.0
tag_m60v <sup>(1)</sup>	defines voltage class for net $\geq$ -60V < -25V	-	7.0
tag_m25v <sup>(1)</sup>	defines voltage class for net $\geq$ -25V < 0V	-	7.0

## 2. General → 2.5 Primitive devices→ 2.5.2 MOS5 main module→ Virtual devices

Name	Description	Required modules	Model rev.
tag_25v <sup>(1)</sup>	defines voltage class for net $\geq 0V \leq 25V$	-	7.0
tag_60v <sup>(1)</sup>	defines voltage class for net $>25V \leq 60V$	-	7.0
tag_100v <sup>(1)</sup>	defines voltage class for net $>60V \leq 100V$	-	7.0
tag_200v <sup>(1)</sup>	defines voltage class for net $>100V \leq 200V$	-	7.0
tag_300v <sup>(1)</sup>	defines voltage class for net $> 200V \leq 300V$	-	11.0
tag_400v <sup>(1)</sup>	defines voltage class for net $> 300V$	-	11.0

**Note 1** These devices are not fabricated on silicon; they are available for DRC and LVS voltage class checks only. For further information, please refer to the design related guideline "Voltage class definitions".

**ESD devices**

Name	Description	Required modules	Model rev.
rdn5_dpc <sup>(1)</sup>	NDIFF drain ballast resistor of ESD NMOS (DPC in PWELL2)	DPC	6.0
rdn5_pw4 <sup>(1)</sup>	NDIFF drain ballast resistor of ESD NMOS (PWELL4 in PWELL2)	NHVA or DIODEA or NHVR	6.0
rnw5_scr <sup>(1)</sup>	5V LV NMOS triggered SCR dio/res network resistor	-	10.0

**Note 1** These devices are only allowed to be used for ESD protection.  
Please refer to ESD documentation on "my X-FAB":  
["XT018-DesignGuideline-ESD\\_and\\_LU"](#)  
["XT018 TLP Characteristics"](#)  
["XT018 Technical Report MOS TLP Characteristics"](#)  
["XT018 Technical Report UHV TLP Characteristics"](#)

2. General → 2.6 Geometric relations and rule code

## 2.6 Geometric relations and rule code

The rule codes, in general, use the description of the geometric relation (e.g. "S" for spacing) and also the design layer/definition code (e.g. "M1" for Metal 1). Rule codes are intended for short design rule check error messages.

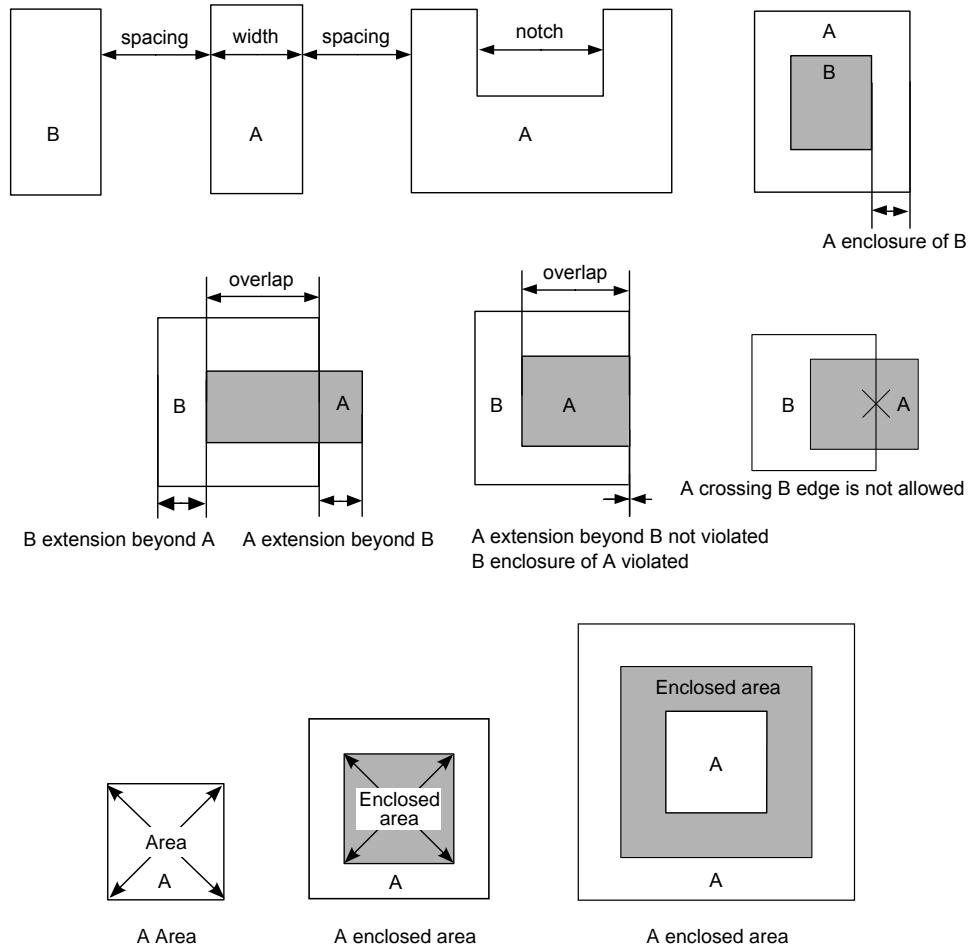
Design rules that are not checked by DRC are indicated by printing the rule code in red underlined italics. The designer must ensure manually that these rules are adhered to.

'QnA(B)' - Query/ warning based rules are not considered to be DRC failures.

The rule types M\_A, N\_A, G\_A are used to check that predefined devices adhere to the following statement: "The layout of the device is predefined and must not be changed". Please note, that for these devices, it is a requirement that the layout is not to be changed (except for the described conditions). The checks related to the rule codes M\_A, N\_A, G\_A are a supporting tool to achieve this requirement. These rules are available for viewing only via the SpecXplorer website.

Rule text	Description	Rule code
(arbitrary text)	Illegal construct	BnA(B)
A crossing B edge is not allowed	Not allowed for layer A polygon to have portions both inside and outside layer B	BnA
A width	Distance inside_A - inside_A	WnA
A size	(Distance inside_A - inside_A) x (Distance inside_A - inside_A)	WnA
A spacing / notch	Distance outside_A - outside_A	SnA
A spacing to B	Distance outside_A - outside_B	SnAB or SnBA
A enclosure of B	Distance inside_A - outside_B (A contains B)	EnAB or EnBA
A extension beyond B	Distance inside_A - outside_B (A must intersect B)	EnAB or EnBA
A overlap of B	Distance inside_A - inside_B	OnAB or OnBA
A area	Area	AnA
A enclosed area	Area enclosed by A	AnA
ratio of A to B	Ratio	RnAB
(arbitrary text)	Recommend investigation (query or warning)	QnA(B)
curvature	Curvature	CnA
Predefined area must have A	Area restriction	M_A
Predefined area must not have A	Area restriction	N_A
Predefined geometry of A violated	Area restriction	G_A

## 2. General → 2.6 Geometric relations and rule code

**Figure 2.1** Geometric relations

2. General → 2.7 General requirements

## 2.7 General requirements

Grid	0.005 µm
Recommended working grid	0.01 µm
Corners	90°, 135°
Data extrema including Peripheral Ring and Scribe Lane <b>Note:</b> Data extrema requirements cover demands of the mask generation procedure and the wafer manufacturing process only.	multiple of 1 µm

It is **MANDATORY** that all layout data, including path edges (centre line & width defined), lie on the minimum grid. Designers are recommended to work with a 0.01µm grid because the data edges can be 0.005µm when 0.01µm is used for the centre line of 'paths'.

45 degree data must not be used for:

- minimum width lines;
- minimum spaced lines;
- or for components with a critical tolerance;

since 'snapping to grid' can occur at mask generation.

Self intersecting polygons must be avoided.

Off-grid data points are checked by X-FAB at GDS tape-in. Off-grid elements will be snapped on-grid for mask generation.

## 3. Layer and Device rules

### 3. Layer and Device rules

#### 3.1 LP5MOS main module

##### 3.1.1 Layer rules

###### NWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1NW	NW_VERIFY overlap of DIFF is not allowed (except rxw2ti)	-	-
B8NW	NW_VERIFY overlap of DTI is not allowed	-	-
W1NW	Minimum NWELL width	0.86	μm
S1NW	Minimum NWELL spacing/notch	0.6	μm
S2NW	Minimum NWELL spacing (different net)	1.4	μm
<b>Note:</b> Valid inside the same TUB			
<b>S4NW</b>	Minimum NWELL spacing (different net)	2.0	μm
	<b>Note:</b> Valid inside the same TUB		
	<b>Note:</b> Valid if one NWELL to PTUB_SUB voltage is less than 1V		
S3NW	Minimum (N WELL AND MV) spacing to N WELL (different net)	2.0	μm
<b>Note:</b> Valid inside the same TUB			
A1NW	Minimum NWELL area	1.0	μm <sup>2</sup>
Q1NW	N WELL should be contacted by NDIFF	-	-

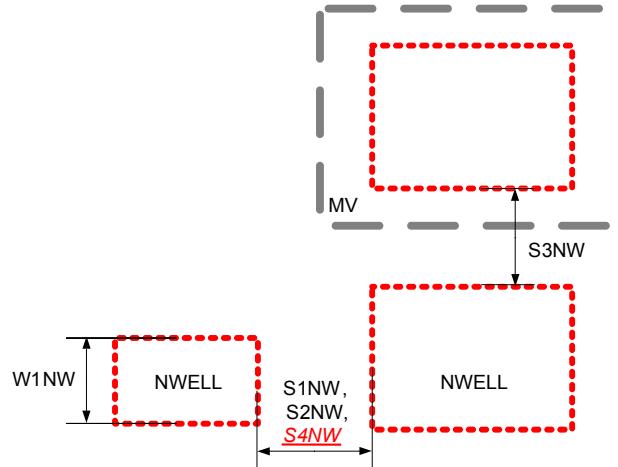


Figure 3.1 NWELL

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → NWELL1, NWELL2, PWELL...

### **NWELL1, NWELL2, PWELL1, PWELL2, NWELL1\_E, NWELL2\_E, PWELL1\_E, PWELL2\_E**

These rules are related to a combination of design layers (refer to section "2.4 Definitions").

Name	Description	Value	Unit
W1W1	Minimum NWELL1 width	0.86	μm
	<b>Note:</b> Not valid between adjacent corners if the virtual line which joins them is orthogonal with respect to the coordinate system axes. The minimum length of this line is 0.56μm.		
W1W7	Minimum NWELL1_E width	0.5	μm
W1W8	Minimum PWELL1_E width	0.5	μm
W1W9	Minimum NWELL2_E width	0.5	μm
W1W10	Minimum PWELL2_E width	0.5	μm
W1W2	Minimum PWELL1 width	0.6	μm
	<b>Note:</b> Not valid between adjacent corners if the virtual line which joins them is orthogonal with respect to the coordinate system axes. The minimum length of this line is 0.56μm.		
W1W3	Minimum NWELL2 width	0.86	μm
W1W4	Minimum PWELL2 width	0.6	μm
A1W1	Minimum NWELL1 area	2.25	μm <sup>2</sup>
A1W2	Minimum PWELL1 area	0.8	μm <sup>2</sup>
A1W3	Minimum NWELL2 area	2.25	μm <sup>2</sup>
A1W4	Minimum PWELL2 area	0.8	μm <sup>2</sup>

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → NWELL1, NWELL2, PWELL...

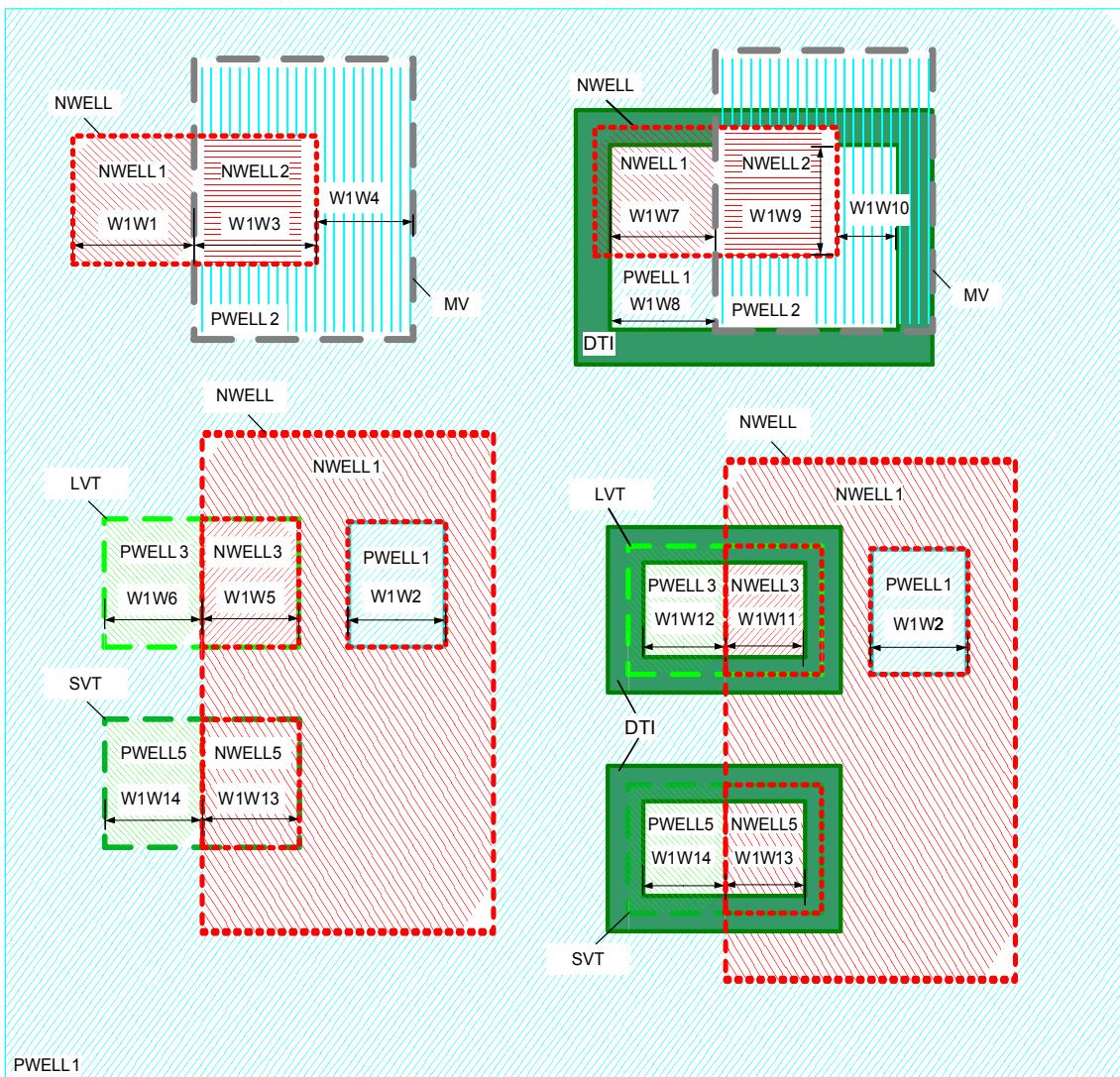


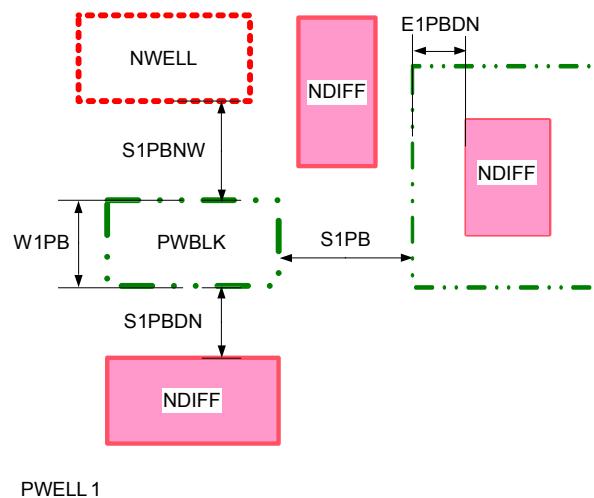
Figure 3.2 NWELL, PWELL

3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ PWBLK

## PWBLK

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B2PB	PWBLK overlap of NWELL is not allowed	-	-
B3PB	PWBLK overlap of PIMP is not allowed (except over SJPN, DTI, SJ1XN, SJ1XP, SJ2XP, nisj1_16, dfwdn#, phv#, pmv#, phvr#, dfwdnh#)	-	-
B6PB	Only a single rectangular NDIFF inside PWBLK is allowed (except nhsj1_#, nisj1_16, ndhv#, dfwdn#, nhv#, nhvr#, ndhvr#, dfwdnh#, nmv#, ndmv#, dfwd#, nhsj1a_#, nhsj1b_#, dfwnsj1a_#, dfwnsj1b_#)	-	-
B4PB	ACTIVE crossing PWBLK edge is not allowed (except over SJNP, SJPN, SJ1XN, SJ1XP or SJ2XP, nisj1_16, nhv#, phv#, ndhv#, dfwdn#, pmv#, nhvr#, phvr#, ndhvr#, dfwdnh#, nmv#, ndmv#, dfwd#)	-	-
W1PB	Minimum PWBLK width (except nmvb, pmvb, dfwdnb)	0.6	μm
S1PB	Minimum PWBLK spacing/notch (except nhv#, ndhv#, dfwdn#, pmvd, pmve, pmvf, nhvr#, ndhvr#, dfwdnh#)	0.86	μm
S1PBDN	Minimum PWBLK spacing to NDIFF (except over SJNP, SJ1XN or SJ2XP)	0.12	μm
S1PBNW	Minimum PWBLK spacing to NWELL (except over SJNP, SJPN, SJ1XN, SJ1XP or SJ2XP, phv#, pmv#, nhvr#, phvr#, ndhvr#, dfwdnh#, nmvb, nmvc, dfwdnb, dfwdnc, qnvha)	0.86	μm
E1PBDN	Fixed PWBLK enclosure of NDIFF (except over SJPN, SJ1XN, SJ1XP or SJ2XP, TIEDTUB, nhv#, phv#, ndhv#, dfwdn#, nhvr#, ndhvr#, dfwdnh#, nmv#, ndmv#, dfwd#)	0.12	μm



**Figure 3.3 PWBLK**

## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ DIFF

**DIFF**

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
	ACTIVE without NIMP or PIMP is not allowed	-	-
	<b>Note:</b> Not valid for DIFFDUMMY.		
B1DF	<b>Note:</b> except SJNP SJPN, SJ1XN, SJ1XP or SJ2XP region in nhsj1_#, phsj1_#, dfwnsj1_#, nhsj1a_#, nhsj1b_#, phsj1a_#, phsj2b_#, dfwnsj1a_#, dfwnsj1b_#, nisj1_16 NBUF region, dpp6, ds5a, ds5b, dzbt1, rxw2ti, qnv5, qnvha, qpv5, qpvha <b>Note:</b> except SJ2XP with oversizing of 0.29µm in DRAIN PWELL2 region		
BDDF	Not allowed to be used by customers <b>Note:</b> Only valid for DIFF purpose NOBLK. Reserved layer.	-	-
B3DF	ACTIVE crossing NWELL edge is not allowed (except nmva#, pmva#, phv#, nmv#, pmv#, ndmv#, phvr#, dfwd#, dpp6, ds5a, ds5b, rxw2ti, qnv5, qnvha, (SJNP, SJPN, SJ1XN, SJ1XP or SJ2XP region in nhsj1_#, phsj1_#, dfwnsj1_#, nhsj1a_#, phsj1a_#, phsj2b_#, dfwnsj1a_#))	-	-
W1DF	Minimum DIFF width	0.22	µm
W2DF	Minimum length of coincident NDIFF/PDIFF path edge	0.42	µm
S1DF	Minimum DIFF spacing/notch	0.28	µm
S1DFDT	Minimum DIFF spacing to DTI	0.5	µm
S1DNNW	Minimum NDIFF spacing to NWELL (except nmvb, nmvc, dfwdnb, dfwdnc)	0.43	µm
S1DPNW	Minimum PDIFF spacing to NWELL	0.12	µm
S2DF	Minimum NDIFF in NWELL spacing to PDIFF in PWELL	0.36	µm
E1DFHW	Minimum DIFF enclosure of HWC	3.0	µm
E1NWDN	Minimum NWELL enclosure of NDIFF (except DIFFDTI, (SJNP region of nhsj1_# and dfwnsj1_#, SJ1XN region of nhsj1a_# and dfwnsj1a_#, SJ1XN region of nhsj1b_# and dfwnsj1b_#, SJ1XP region of phsj1a_#, SJ2XP region of phsj2b_#))	0.12	µm
E1NWDP	Minimum NWELL enclosure of PDIFF (except TIEDTUB)	0.43	µm
E1DFDT	Minimum DIFF extension beyond DTI	0.5	µm
O1DFDT	Minimum DIFF overlap of DTI	0.5	µm
A1DF	Minimum ACTIVE area <b>Note:</b> DIFF dimension greater than 200 µm x 200 µm must not be used.	0.202	µm <sup>2</sup>
<i>R1DF</i>	Minimum local DIFF density (except SJ1XN, SJ1XP)	15.0	%
	<b>Note:</b> Valid in any 200µm x 200µm window, step size 100µm.		
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
<i>R2DF</i>	Minimum local DIFF density (for SJ1XN, SJ1XP)	5.0	%
	<b>Note:</b> Valid in any 200µm x 200µm window, step size 100µm.		
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
R3DF	Maximum ratio of DIFF (in PWELL1_E) to PWELL1_E area	50.0	%
	<b>Note:</b> Only valid for LP5MOS module.		
	<b>Note:</b> Only valid if PWELL1_E covering TUB completely with PWELL1_E area > 30000 µm <sup>2</sup> .		
	<b>Note:</b> The use of a single large size primitive device with PWELL1_E > 30000µm <sup>2</sup> is not permitted. <b>Note:</b> R3DF violation requires reduction of tub size rather than adding other well types.		

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → DIFF

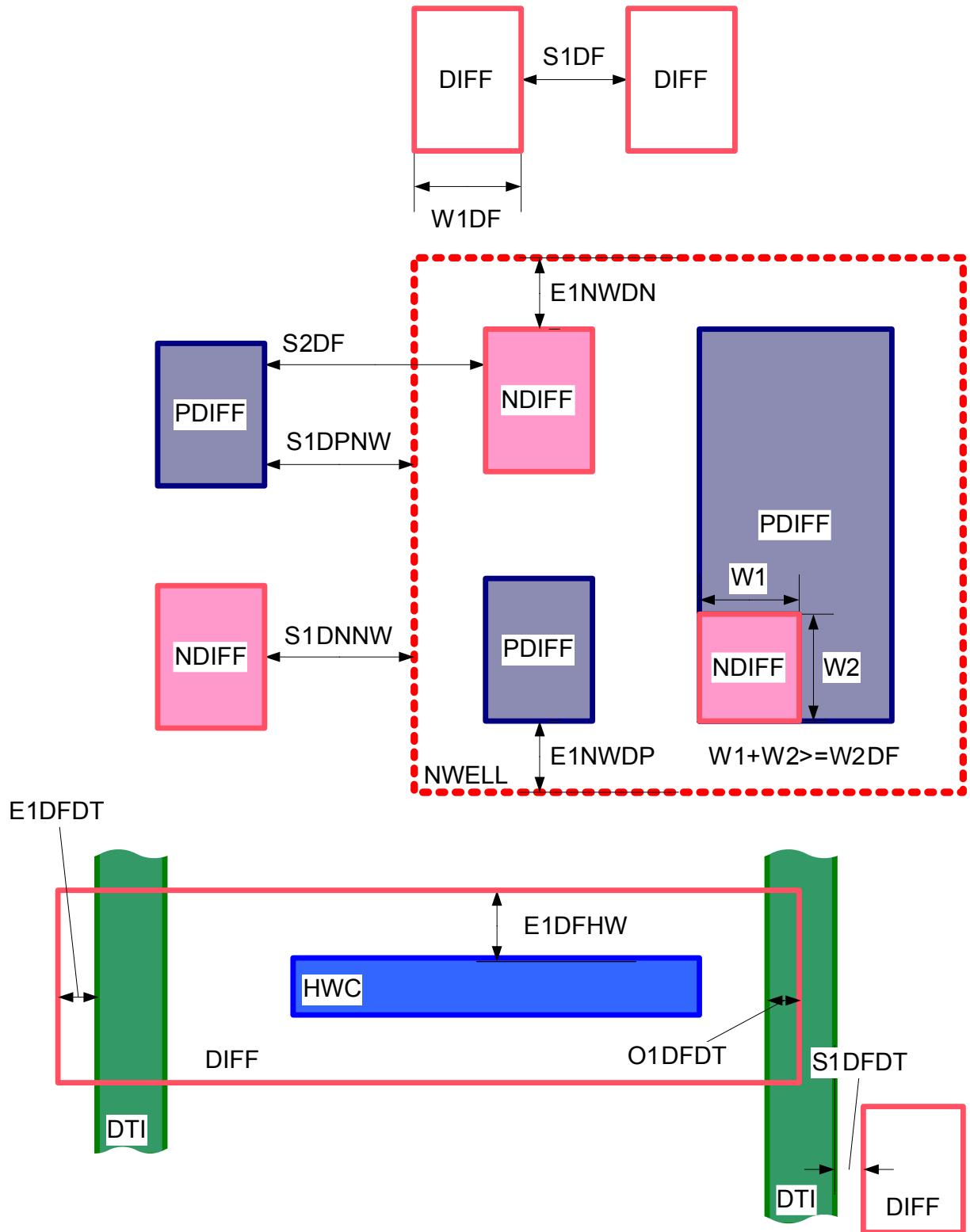


Figure 3.4 DIFF

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → DIFFDUMMY

**DIFFDUMMY**

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B10YD	DIFFDUMMY overlap of NBUF is not allowed	-	-
B11YD	DIFFDUMMY overlap of PZENER is not allowed	-	-
B12YD	DIFFDUMMY overlap of NZENER is not allowed	-	-
B13YD	DIFFDUMMY overlap of SJ1XN is not allowed	-	-
B14YD	DIFFDUMMY overlap of SJ2XP is not allowed	-	-
B15YD	DIFFDUMMY overlap of SJ1XP is not allowed	-	-
B16YD	DIFFDUMMY overlap of HVDEPL is not allowed	-	-
B1YD	DIFFDUMMY overlap of DIFF is not allowed	-	-
B2YD	DIFFDUMMY overlap of NIMP or PIMP is not allowed	-	-
B3YD	DIFFDUMMY overlap of CONT is not allowed	-	-
B5YD	DIFFDUMMY overlap of SBLK is not allowed	-	-
B7YD	DIFFDUMMY overlap of DTI is not allowed	-	-
B8YD	DIFFDUMMY overlap of SJPN is not allowed	-	-
B9YD	DIFFDUMMY overlap of SJNP is not allowed	-	-
W1YD	Minimum DIFFDUMMY width	0.4	μm
S1YD	Minimum DIFFDUMMY spacing/notch	0.5	μm
S10YD	Minimum DIFFDUMMY spacing to LOCKED	3.6	μm
S11YD	Minimum DIFFDUMMY spacing to LOCKED1	3.6	μm
S12YD	Minimum DIFFDUMMY spacing to LOCKED2	3.6	μm
S13YD	Minimum DIFFDUMMY spacing to LOCKED3	3.6	μm
S14YD	Minimum DIFFDUMMY spacing to LOCKED4	3.6	μm
S1YDDF	Minimum DIFFDUMMY spacing to DIFF	3.0	μm
S1YDDT	Minimum DIFFDUMMY spacing to DTI	1.0	μm
S1YDHL	Minimum DIFFDUMMY spacing to HVDEPL	5.0	μm
S1YDIN	Minimum DIFFDUMMY spacing to NIMP	0.3	μm
S1YDIP	Minimum DIFFDUMMY spacing to PIMP	0.3	μm
S1YDNF	Minimum DIFFDUMMY spacing to NBUF	5.0	μm
S1YDNT	Minimum DIFFDUMMY spacing to SJNP	5.0	μm
S1YDNW	Minimum DIFFDUMMY spacing to NW4DMY	5.0	μm
S1YDNZ	Minimum DIFFDUMMY spacing to NZENER	5.0	μm
S1YDP1	Minimum DIFFDUMMY spacing to POLY1	3.0	μm
S1YDPI	Minimum DIFFDUMMY spacing to PW4DMY	5.0	μm
S1YDPT	Minimum DIFFDUMMY spacing to SJPN	5.0	μm
S1YDPZ	Minimum DIFFDUMMY spacing to PZENER	5.0	μm
S1YDSB	Minimum DIFFDUMMY spacing to SBLK	3.0	μm
S1YDX1	Minimum DIFFDUMMY spacing to SJ1XN	5.0	μm
S1YDX2	Minimum DIFFDUMMY spacing to SJ1XP	5.0	μm
S1YDX4	Minimum DIFFDUMMY spacing to SJ2XP	5.0	μm

⇒

## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ DIFFDUMMY

Name	Description	Value	Unit
E1YDNW	Minimum NW4DMY enclosure of DIFFDUMMY	5.0	μm
E1YDPI	Minimum PW4DMY enclosure of DIFFDUMMY	5.0	μm
A1YD	Minimum DIFFDUMMY area	1.2	μm <sup>2</sup>

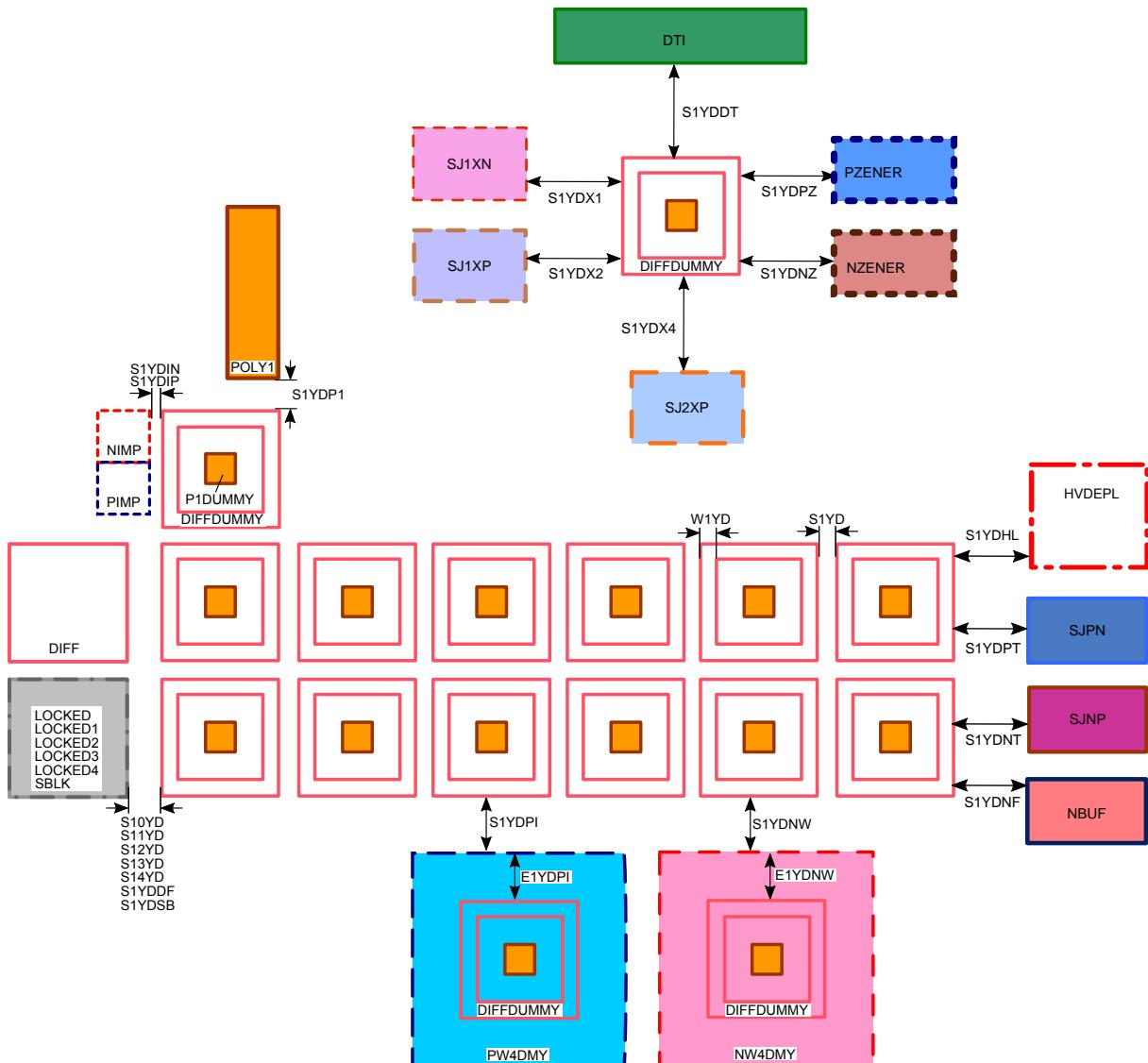


Figure 3.5 DIFFDUMMY

## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ MV

**MV**

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

If the module MOS5 is selected, the layer MV is first generated covering the complete chip area before further layer generation is performed, so the design rules for the MV layer are checked by DRC after MV generation.

Name	Description	Value	Unit
B1MV	ACTIVE crossing MV edge is not allowed <b>Note:</b> Not valid for DIFFDUMMY.	-	-
B2MV	NW_VERIFY crossing MV edge is not allowed	-	-
W1MV	Minimum MV width	0.6	μm
S1MV	Minimum MV spacing/notch	0.86	μm
S1MVDF	Minimum MV spacing to ACTIVE <b>Note:</b> Not valid for DIFFDUMMY.	0.32	μm
S1MVDT	Minimum MV spacing to DTI	0.7	μm
S1MVGA	Minimum MV spacing to GATE	0.4	μm
E1MVDF	Minimum MV enclosure of ACTIVE <b>Note:</b> Not valid for DIFFDUMMY.	0.32	μm
E1MVGA	Minimum MV enclosure of GATE	0.4	μm

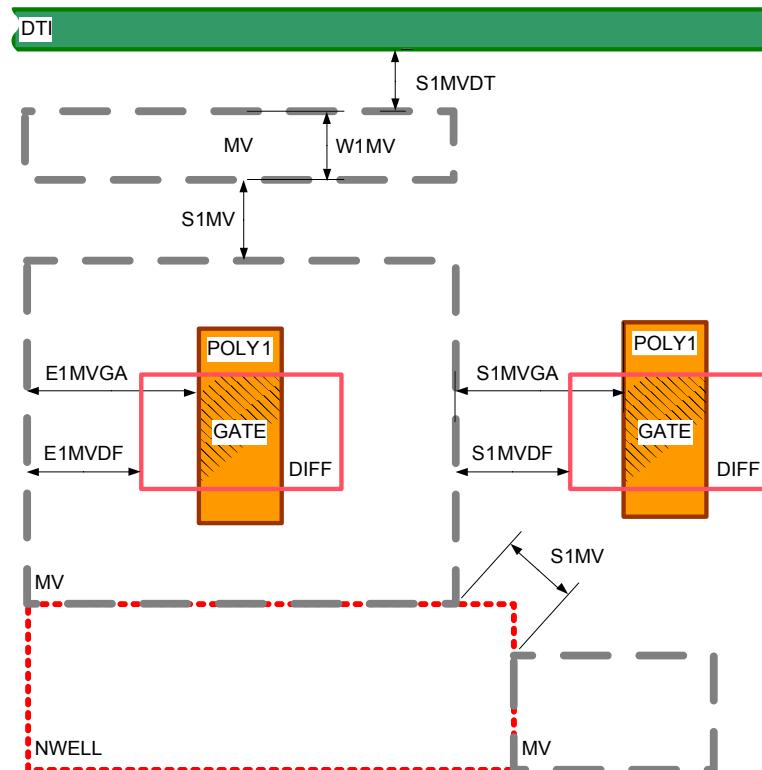


Figure 3.6 MV

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → POLY1

**POLY1**

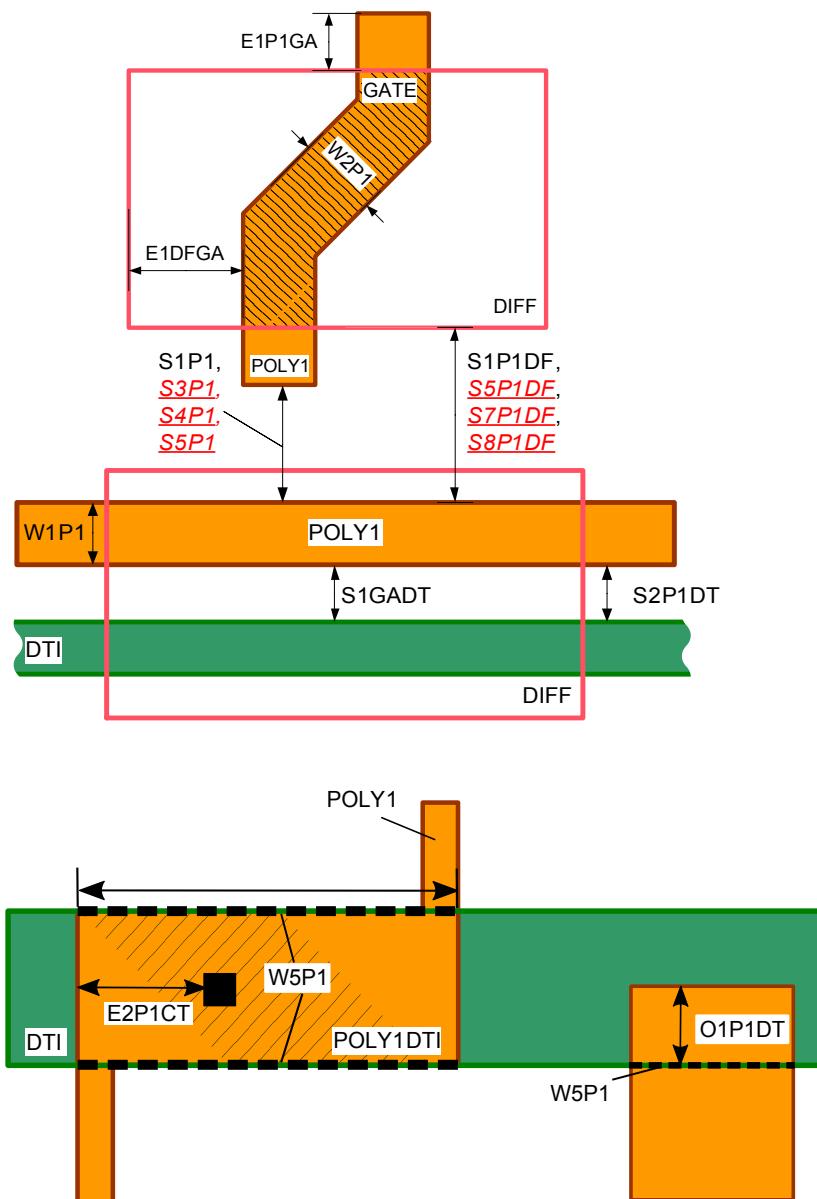
This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B10P1	POLY1 overlap of ISOTUB is not allowed  <b>Note:</b> Valid if the voltage difference of the affected elements (TUBs, POLY1) >100V, however the design rule check is performed without voltage rating considerations.	-	-
B11P1	POLY1DTI must be rectangular	-	-
B1GA	90 degree bent GATE is not allowed  <b>Note:</b> Only valid for POLY1 over DIFF or for DIFF over POLY1 structures with > 4 vertices.	-	-
B1P1	(POLY1 and SBLK and not (HRES or MRES)) without NIMP or PIMP is not allowed  <b>Note:</b> NIMP touching PIMP under (POLY1 and SBLK and not (HRES or MRES)) is not allowed.	-	-
B2GA	Illegal GATE construct  <b>Note:</b> GATE region has been identified as having no association with supported devices.	-	-
B3P1	POLY1 overlap of DIFFDTI is not allowed	-	-
BDP1	Not allowed to be used by customers  <b>Note:</b> Only valid for POLY1 purpose NOBLK. Reserved layer.	-	-
W1P1	Minimum POLY1 width	0.18	μm
W2P1	Minimum POLY1 width (for 45 degree bent GATE)	0.21	μm
W5P1	Minimum length of POLY1DTI edge coinciding with DTI edge (except pmv#, P1_FP)	1.0	μm
S1P1	Minimum POLY1 spacing/notch	0.25	μm
S3P1	Minimum POLY1 spacing (different net, tag_#, difference >25V ≤ 60V)  <b>Note:</b> Valid for spacing of all POLY1 shapes with label tag_## to all POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".	0.5	μm
S4P1	Minimum POLY1 spacing (different net, tag_#, difference >60V ≤100V)  <b>Note:</b> Valid for spacing of all POLY1 shapes with label tag_## to all POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".	0.8	μm
S5P1	Minimum POLY1 spacing (different net, tag_#, difference >100V)  <b>Note:</b> Valid for spacing of all POLY1 shapes with label tag_## to all POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of > 100V. Refer to the design related guideline "Voltage class definitions".	1.3	μm
S1GADT	Minimum GATE spacing to DTI	0.5	μm
S1P1DF	Minimum POLY1 spacing to ACTIVE	0.1	μm
S2P1DT	Minimum POLY1 spacing to DTI	0.08	μm
S5P1DF	Minimum POLY1 spacing to DIFF (different net, tag_#, difference >25V ≤ 60V)  <b>Note:</b> Valid for spacing of all POLY1/DIFF shapes with label tag_## to all DIFF/POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".	0.5	μm
S7P1DF	Minimum POLY1 spacing to DIFF (different net, tag_#, difference >60V ≤100V)  <b>Note:</b> Valid for spacing of all POLY1/DIFF shapes with label tag_## to all DIFF/POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".	0.8	μm
S8P1DF	Minimum POLY1 spacing to DIFF (different net, tag_#, difference >100V)  <b>Note:</b> Valid for spacing of all POLY1/DIFF shapes with label tag_## to all DIFF/POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of > 100V. Refer to the design related guideline "Voltage class definitions".	1.3	μm

## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ POLY1

Name	Description	Value	Unit
E2P1CT	Minimum POLY1DTI enclosure of CONT (in the direction of POLY1DTI edge inside DTI)	0.44	µm
E1DFGA	Minimum DIFF extension beyond GATE	0.32	µm
E1P1GA	Minimum POLY1 extension beyond GATE (except nmva#, pmva#)	0.22	µm
O1P1DT	Minimum POLY1 overlap of DTI (except ds5a, ds5b)	0.5	µm
A1P1	Minimum POLY1 area	0.118	µm <sup>2</sup>
A2P1	Maximum POLY1 area	10000.0	µm <sup>2</sup>
<i>R1P1</i>	Minimum ratio of POLY1 area to EXTENT area  <b>Note:</b> Not checked with standard DRC, option for check is available.	14.0	%
R2P1	Maximum ratio of POLY1 area to connected GATE area  <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	200.0	-
Q1P1	Resistor terminal net without VLABEL  <b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".	-	-

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → POLY1

**Figure 3.7 POLY1**

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → P1DUMMY

## P1DUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B10YP	P1DUMMY overlap of NBUF is not allowed	-	-
B11YP	P1DUMMY overlap of PZENER is not allowed	-	-
B12YP	P1DUMMY overlap of NZENER is not allowed	-	-
B13YP	P1DUMMY overlap of SJ1XN is not allowed	-	-
B14YP	P1DUMMY overlap of SJ2XP is not allowed	-	-
B15YP	P1DUMMY overlap of SJ1XP is not allowed	-	-
B16YP	P1DUMMY overlap of HVDEPL is not allowed	-	-
B1YP	Only rectangular P1DUMMY is allowed	-	-
B2YP	P1DUMMY overlap of POLY1 is not allowed	-	-
B3YP	P1DUMMY overlap of CONT is not allowed	-	-
B4YP	P1DUMMY overlap of DIFF is not allowed	-	-
B5YP	P1DUMMY overlap of SBLK is not allowed	-	-
B6YP	P1DUMMY overlap of MRES or HRES is not allowed	-	-
B7YP	P1DUMMY overlap of DTI is not allowed	-	-
B8YP	P1DUMMY overlap of SJPN is not allowed	-	-
B9YP	P1DUMMY overlap of SJNP is not allowed	-	-
W1YP	Minimum P1DUMMY width	1.0	µm
S1YP	Minimum P1DUMMY spacing	1.0	µm
S10YP	Minimum P1DUMMY spacing to LOCKED	3.6	µm
S11YP	Minimum P1DUMMY spacing to LOCKED1	3.6	µm
S12YP	Minimum P1DUMMY spacing to LOCKED2	3.6	µm
S13YP	Minimum P1DUMMY spacing to LOCKED3	3.6	µm
S14YP	Minimum P1DUMMY spacing to LOCKED4	3.6	µm
S1YPDF	Minimum P1DUMMY spacing to DIFF	3.0	µm
S1YPDT	Minimum P1DUMMY spacing to DTI	1.0	µm
S1YPHL	Minimum P1DUMMY spacing to HVDEPL	5.0	µm
S1YPNF	Minimum P1DUMMY spacing to NBUF	5.0	µm
S1YPNT	Minimum P1DUMMY spacing to SJNP	5.0	µm
S1YPNW	Minimum P1DUMMY spacing to NW4DMY	5.0	µm
S1YPNZ	Minimum P1DUMMY spacing to NZENER	5.0	µm
S1YPP1	Minimum P1DUMMY spacing to POLY1	3.0	µm
S1YPP1	Minimum P1DUMMY spacing to PW4DMY	5.0	µm
S1YPPT	Minimum P1DUMMY spacing to SJPN	5.0	µm
S1YPPZ	Minimum P1DUMMY spacing to PZENER	5.0	µm
S1YPSB	Minimum P1DUMMY spacing to SBLK	3.0	µm
S1YPX1	Minimum P1DUMMY spacing to SJ1XN	5.0	µm
S1YPX2	Minimum P1DUMMY spacing to SJ1XP	5.0	µm
S1YPX4	Minimum P1DUMMY spacing to SJ2XP	5.0	µm



## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ P1DUMMY

Name	Description	Value	Unit
S1YPYD	Minimum P1DUMMY spacing to DIFFDUMMY	0.4	μm
E1YPNW	Minimum NW4DMY enclosure of P1DUMMY	5.0	μm
E1YPP1	Minimum PW4DMY enclosure of P1DUMMY	5.0	μm

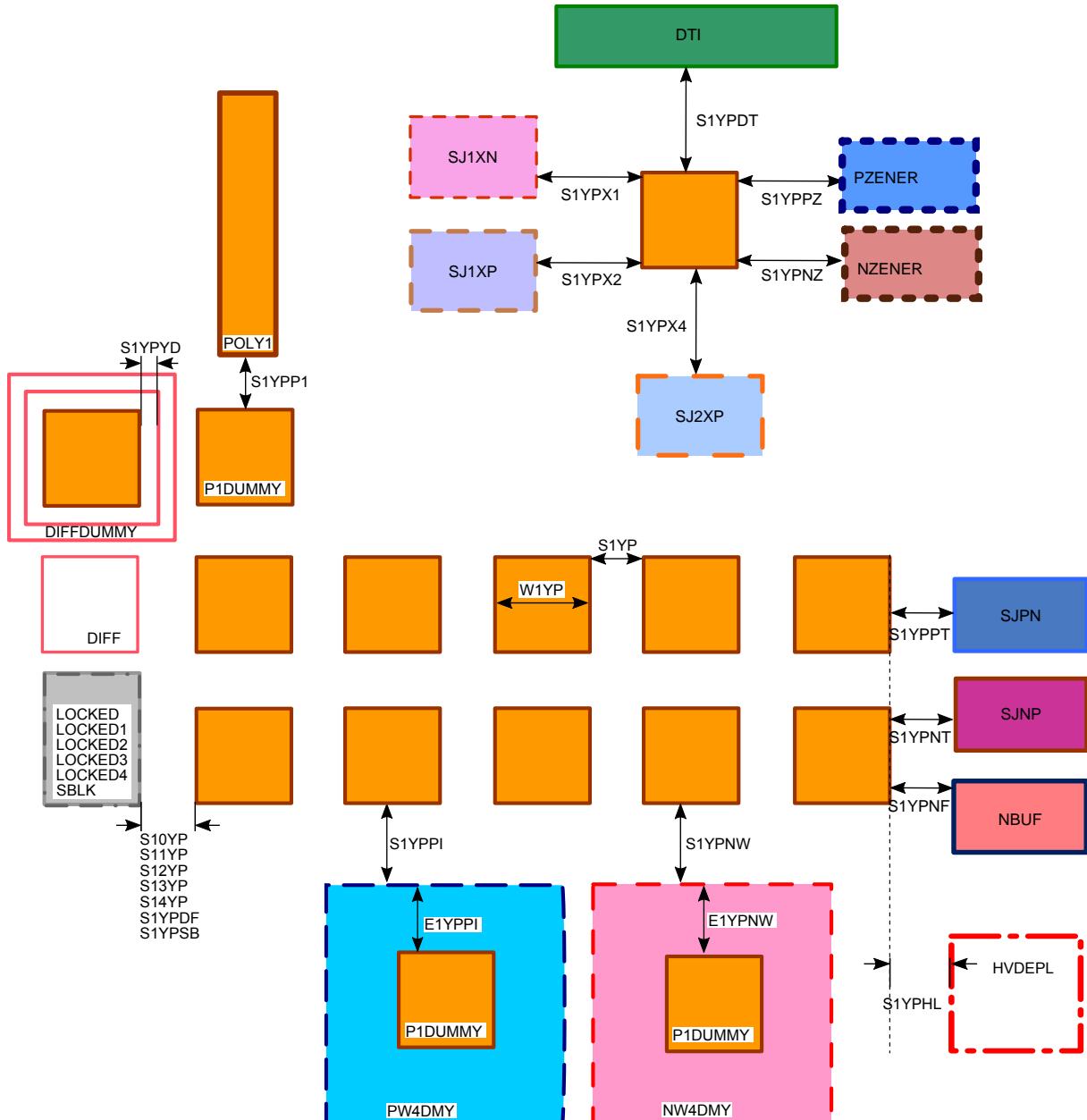


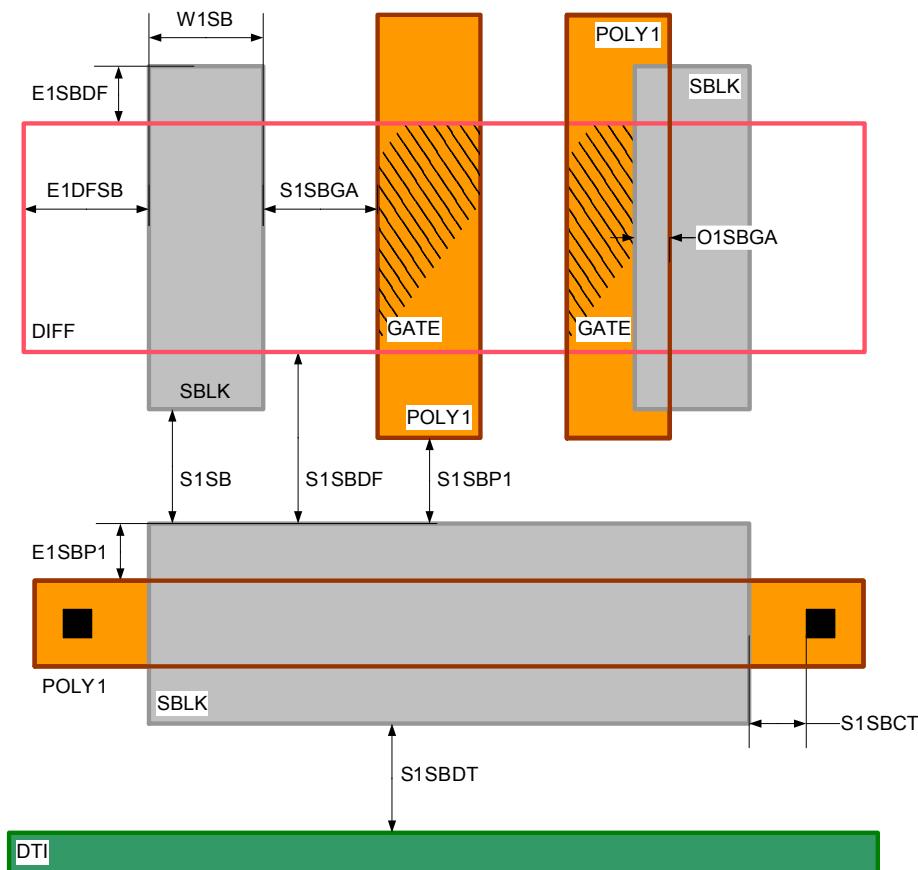
Figure 3.8 P1DUMMY

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → SBLK

## SBLK

SBLK is only allowed for primitive devices.

Name	Description	Value	Unit
W1SB	Minimum SBLK width	0.43	μm
S1SB	Minimum SBLK spacing/notch	0.43	μm
S1SBCT	Minimum SBLK spacing to CONT	0.22	μm
S1SBDF	Minimum SBLK spacing to DIFF (except nmvab, pmvab)	0.22	μm
S1SBDT	Minimum SBLK spacing to DTI	0.25	μm
S1SBGA	Minimum SBLK spacing to GATE (except nmvab, pmvab)	0.45	μm
S1SBP1	Minimum SBLK spacing to POLY1	0.3	μm
E1DFSB	Minimum ACTIVE extension beyond SBLK	0.22	μm
E1SBDF	Minimum SBLK extension beyond ACTIVE	0.22	μm
E1SBP1	Minimum SBLK extension beyond POLY1 (except nmvab, pmvab)	0.22	μm
O1SBGA	Minimum SBLK overlap of GATE	0.05	μm
<b>Note:</b> It is recommended to use SBLK over GATE only for IO blocks and ESD protection.			
A1SB	Minimum SBLK area	2.0	μm <sup>2</sup>

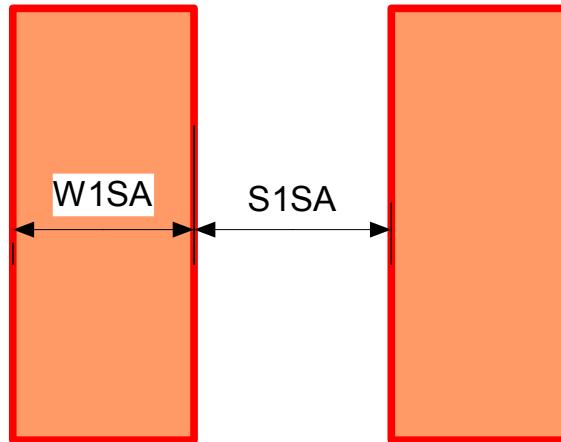


**Figure 3.9** SBLK

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → SALICIDE

## SALICIDE

Name	Description	Value	Unit
B1SA	SALICIDE is only allowed inside TUB between multiple DIFFDTI rings	-	-
B2SA	SALICIDE must connect to DIFFCON	-	-
B3SA	SALICIDE without DIFF is not allowed	-	-
W1SA	Minimum SALICIDE width	0.5	μm
S1SA	Minimum SALICIDE spacing/notch	0.43	μm



**Figure 3.10** SALICIDE

3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ NIMP

## NIMP

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
W1IN	Minimum NIMP width (except phv#)	0.44	μm
S1IN	Minimum NIMP spacing/notch (except nhv#, ndhv#, nmv#, ndmv#)	0.44	μm
S1INDP	Minimum NIMP spacing to PDIFF	0.1	μm
S2INDP	Minimum NIMP spacing to PDIFF (in NWELL) (except phsj1_#, dfwdpa, phsj1a_#)	0.26	μm
S3INDP	Minimum NIMP spacing to PDIFF (if PDIFF to NWELL spacing is <0.43μm)	0.18	μm
E1DNP1	Minimum NDIFF extension beyond POLY1 (except nhvta, nhvtaa, ndhvta, ndhvtaa, nmv#, ndmv# and nisj1_16)	0.32	μm
E1INDF	Minimum NIMP extension beyond ACTIVE (except TIEDTUB, nhsj1_# and dfwdpa)	0.18	μm
E1INDN	Minimum NIMP extension beyond POLY1/NDIFF in direction of POLY1 (except nisj1_16)	0.35	μm
E2INDF	Minimum NIMP extension beyond ACTIVE (in NWELL) (if NWELL enclosure of NDIFF is >=0.43μm )	0.02	μm
O1INDF	Minimum ACTIVE overlap of NIMP	0.23	μm
A1IN	Minimum NIMP area	0.3844	μm <sup>2</sup>

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → NIMP

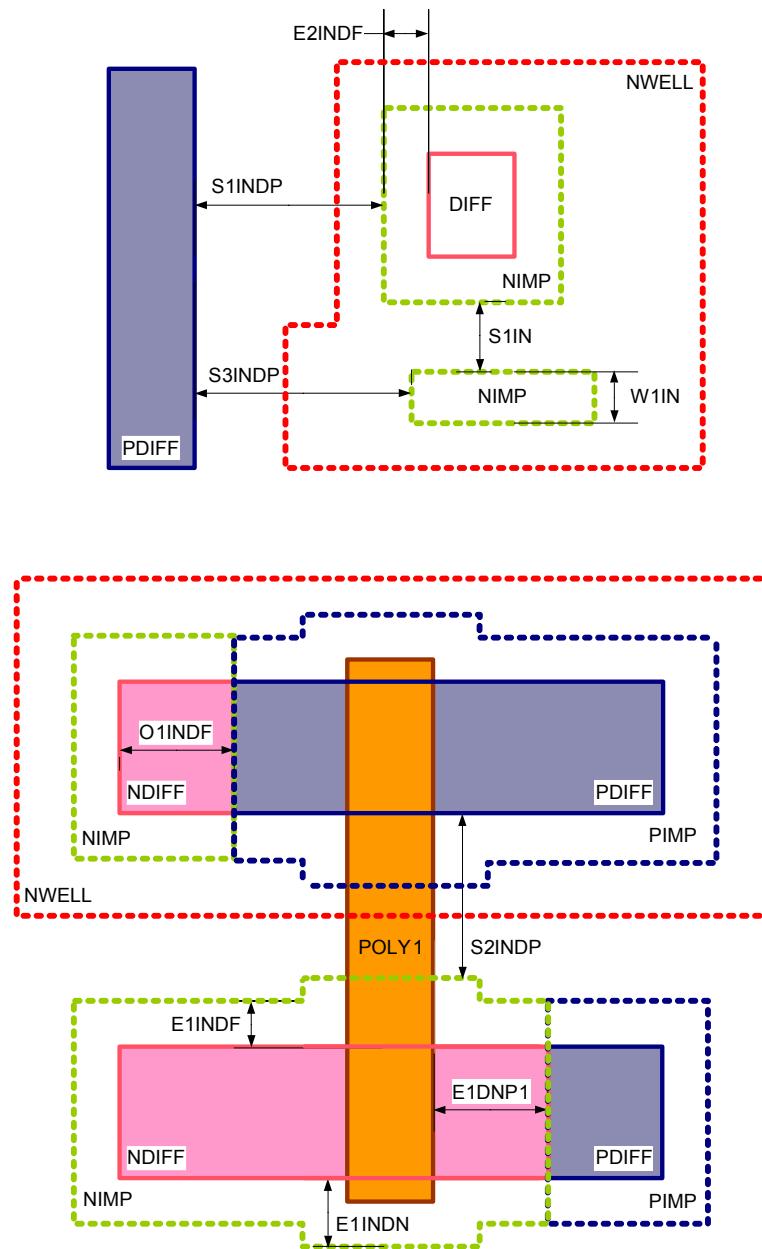


Figure 3.11 NIMP

3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ PIMP

## PIMP

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1IPIN	PIMP overlap of NIMP is not allowed	-	-
W1IP	Minimum PIMP width (except nhv#, ndhv#, nmv#, ndmv#)	0.44	μm
S1IP	Minimum PIMP spacing/notch (except phv#)	0.44	μm
S1IPDN	Minimum PIMP spacing to NDIFF (outside NWELL) (except nhsj1_#, nhsj1a_#, nhsj1b_#)	0.26	μm
S2IPDN	Minimum PIMP spacing to NDIFF (in NWELL) (if NWELL enclosure of NDIFF is >=0.43μm)	0.1	μm
S3IPDN	Minimum PIMP spacing to NDIFF (in NWELL) (if NWELL enclosure of NDIFF is <0.43μm)	0.18	μm
E1DPP1	Minimum PDIFF extension beyond POLY1 (except ds5a, ds5b)	0.32	μm
E1IPDF	Minimum PIMP extension beyond ACTIVE (except TIEDTUB, phsj1_#, dfwdpa, phsj1a_#, phsj2b_#)	0.18	μm
E1IPDP	Minimum PIMP extension beyond POLY1/PDIFF in direction of POLY1	0.35	μm
E2IPDF	Minimum PIMP extension beyond ACTIVE (outside NWELL) (if NWELL spacing to PDIFF is >=0.43μm)	0.02	μm
O1IPDF	Minimum ACTIVE overlap of PIMP	0.23	μm
A1IP	Minimum PIMP area	0.3844	μm <sup>2</sup>

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → PIMP

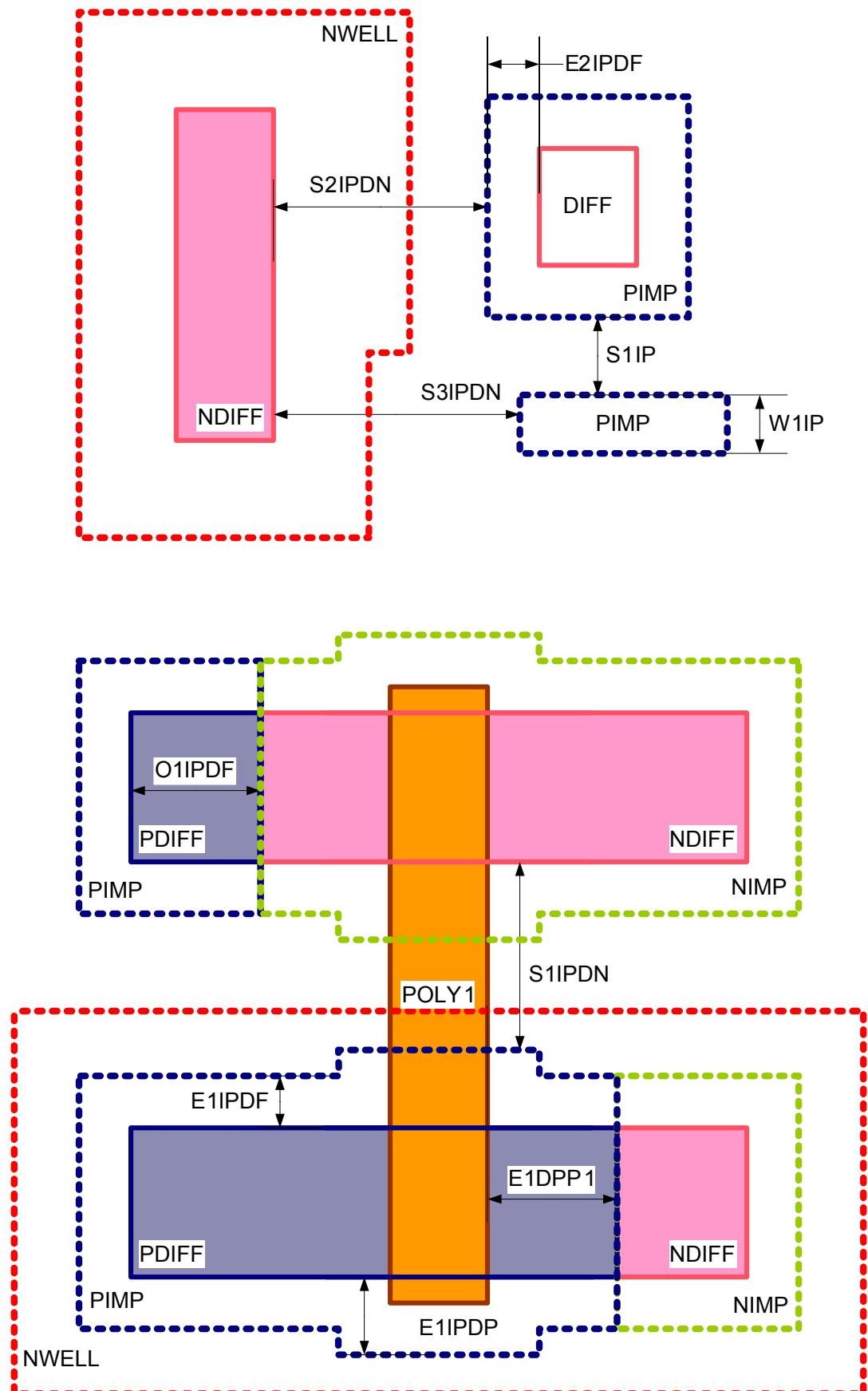


Figure 3.12 PIMP

3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ CONT

## CONT

Name	Description	Value	Unit
B1CT	CONT without NDIFF or PDIFF or POLY1 is not allowed (except ds5a, ds5b)	-	-
B1CTDT	DIFFCON overlap of DTI is not allowed	-	-
B1CTGA	CONT overlap of GATE is not allowed	-	-
B1CTSB	CONT overlap of SBLK is not allowed	-	-
W1CT	Fixed CONT size	0.22 x 0.22	µm x µm
S1CT	Minimum CONT spacing	0.25	µm
S2CT	Minimum CONT spacing (for contact arrays containing more than 4x4 elements)	0.28	µm
	<b>Note:</b> Two contact regions within 0.3 µm spacing are considered to be in the same array.		
S1CTDF	Minimum CONT spacing to DIFF	0.2	µm
S1CTDT	Minimum DIFFCON spacing to DTI	0.14	µm
S1CTHW	Minimum CONT spacing to HWC	3.5	µm
S1CTP1	Minimum CONT spacing to POLY1	0.16	µm
S2CTDT	Minimum DIFFCON spacing to DTI corner (except TIEDTUB)	0.5	µm
E1DFCT	Minimum DIFF enclosure of CONT	0.1	µm
E1IRCT	Minimum (NIMP or PIMP) enclosure of DIFFCON	0.12	µm
E1P1CT	Minimum POLY1 enclosure of CONT	0.1	µm
R1CT	Maximum ratio of CONT area to connected GATE area	10.0	-

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → CONT

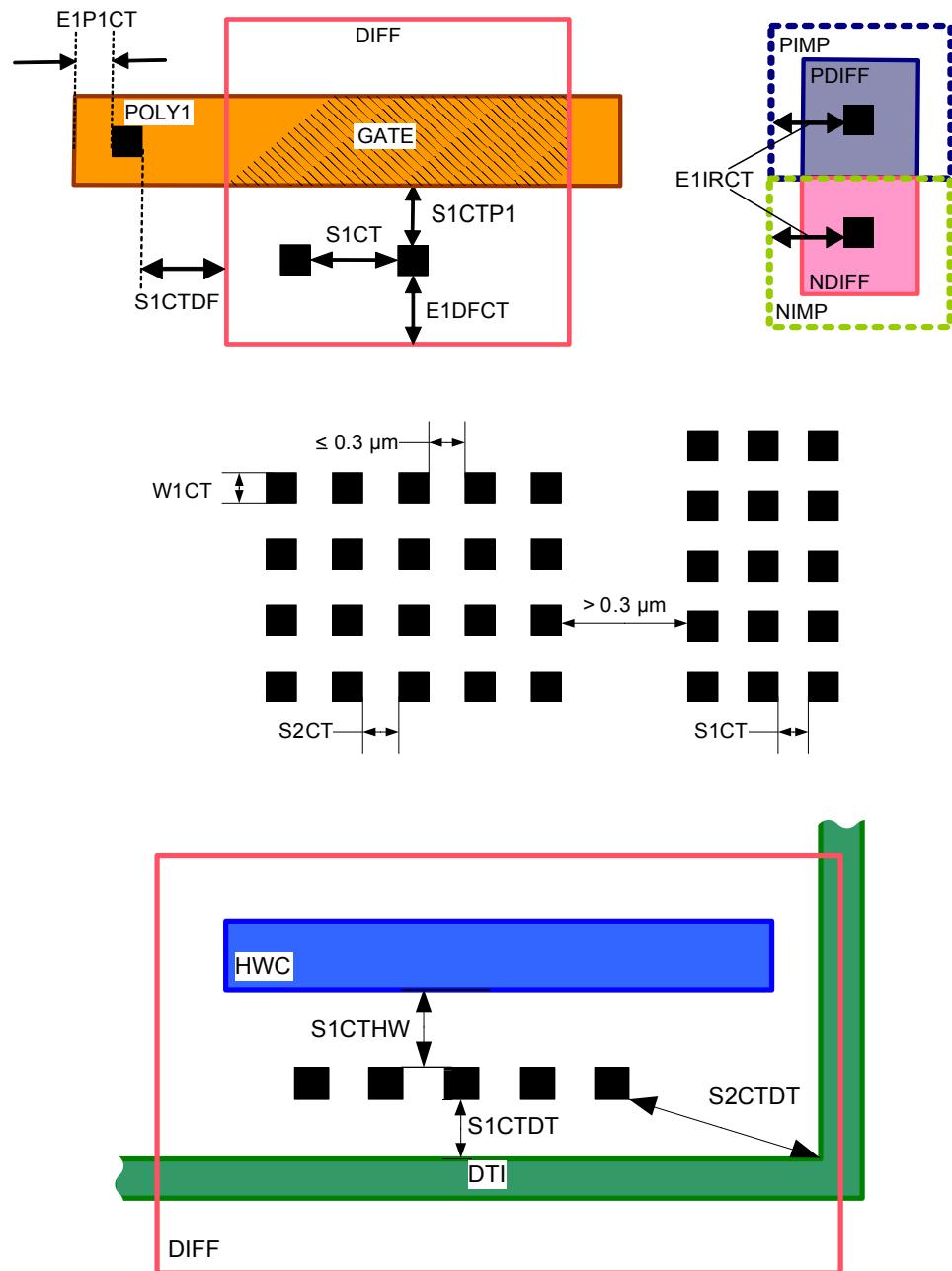


Figure 3.13 CONT

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → MET1

**MET1**

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1CTM1	CONT must be covered by MET1	-	-
B1M1DF	MET1 overlap of ACTIVE is not allowed (different net, tag_#, ACTIVE, MET1 difference >300V)	-	-
B1M1P1	MET1 overlap of POLY1 is not allowed (different net, tag_#, POLY1, MET1 difference >200V)	-	-
W1M1	Minimum MET1 width	0.23	μm
<u>W4M1</u>	Minimum MET1 width joining wide MET1 track (> 35 μm)	10.0	μm
	<b>Note:</b> No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 μm from the main track prior to narrowing.		
<u>W5M1</u>	Maximum MET1 region size	17.0 x 17.0	μm x μm
	<b>Note:</b> MET1 regions are defined as MET1 shapes (single MET1 shapes or a bundle of MET1 shapes, with width > 2.0 μm, inclusive of the spacing if the spacing is <= 1.0 μm) without any other metal layer above. For further information and design guidelines, please refer to the application note about <a href="#">IMD popping</a> on "my X-FAB".		
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
S1M1	Minimum MET1 spacing/notch	0.23	μm
S4M1	Minimum MET1 spacing (different net, tag_#, difference >25V ≤ 60V)	0.38	μm
	<b>Note:</b> Except nhvta/ndhvta DRAIN MET1 to GATE MET1		
	<b>Note:</b> Valid for spacing of all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".		
S5M1	Minimum MET1 spacing (different net, tag_#, difference >60V ≤100V)	0.6	μm
	<b>Note:</b> Valid for spacing of all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Minimum MET1 spacing (different net, tag_#, difference >100V ≤200V)	0.8	μm
S6M1	<b>Note:</b> Valid for spacing to all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >100V ≤ 200V. Refer to the design related guideline "Voltage class definitions".		
	Minimum MET1 spacing (different net, tag_#, difference >200V ≤300V)	1.2	μm
	<b>Note:</b> Valid for spacing to all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤ 300V. Refer to the design related guideline "Voltage class definitions".		
S9M1	Minimum MET1 spacing (different net, tag_#, difference >300V)	1.6	μm
	<b>Note:</b> Valid for spacing to all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Minimum MET1 spacing to ACTIVE (different net, tag_#, difference >300V)		
S1M1DF	<b>Note:</b> Valid for spacing of all MET1/ACTIVE shapes with label tag_# to all ACTIVE/MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Valid if the voltage difference between ACTIVE, MET1 is >300V.		
	Minimum MET1 spacing to WIDE_MET1	0.6	μm
S2M1P1	Minimum MET1 spacing to POLY1 (different net, tag_#, difference >200V ≤300V)	1.2	μm
	<b>Note:</b> Valid if MET1 to POLY1 voltage is >200V ≤300V.		
	<b>Note:</b> Valid for spacing of all MET1/POLY1 shapes with label tag_# to all POLY1/MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤300V. Refer to the design related guideline "Voltage class definitions".		

## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ MET1

Name	Description	Value	Unit
S3M1P1	Minimum MET1 spacing to POLY1 (different net, tag #, difference >300V)	1.6	μm
<b>Note:</b> Valid if MET1 to POLY1 voltage is >300V.			
<b>Note:</b> Valid for spacing of all MET1/POLY1 shapes with label tag # to all POLY1/MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".			
E1M1CT	Minimum MET1 enclosure of CONT	0.005	μm
E2M1CT	Minimum MET1 enclosure of CONT (in one direction of CONT corner)	0.06	μm
A1M1	Minimum MET1 area	0.202	μm <sup>2</sup>
<i>R1M1</i>	Minimum ratio of MET1 area to EXTENT area	30.0	%
<b>Note:</b> Not checked with standard DRC, option for check is available.			
<i>R2M1</i>	Maximum ratio of MET1 area to EXTENT area	65.0	%
<b>Note:</b> Not checked with standard DRC, option for check is available.			
R1M1P1	Maximum ratio of MET1 area to connected GATE area	400.0	-
<b>Note:</b> Refer to section "Antenna Rule definitions" as well.			
R2M1P1	Maximum ratio of MET1 area to connected GATE area	400.0	-
<b>Note:</b> Refer to section "Antenna Rule definitions" as well.			
Q1M1	Resistor terminal net without VLABEL	-	-
<b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".			

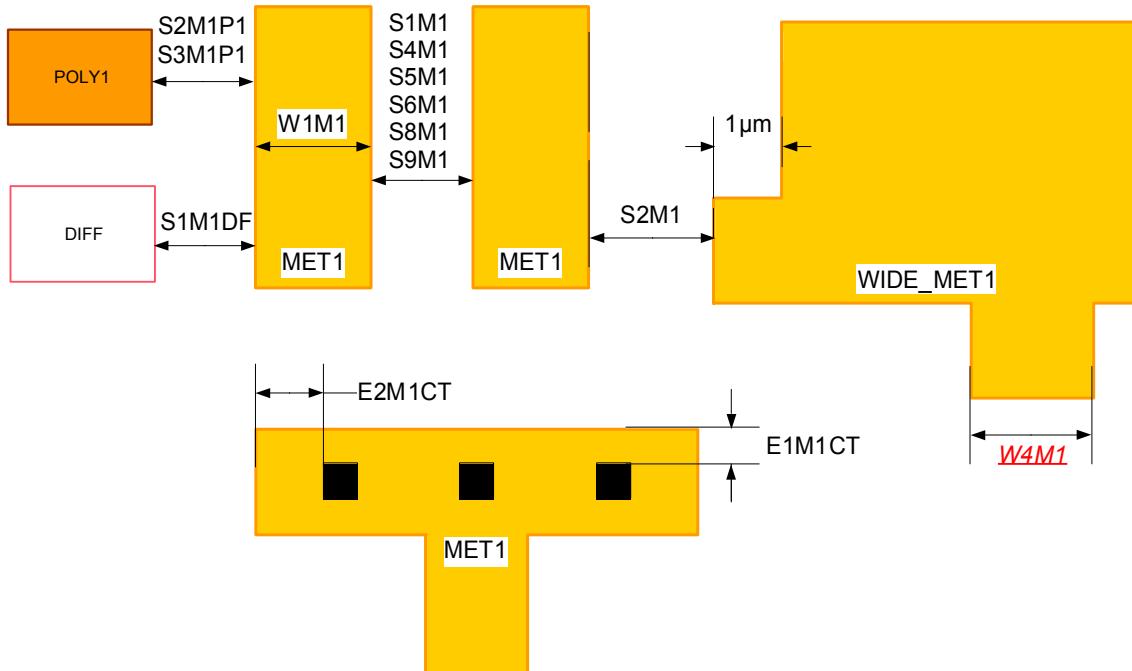


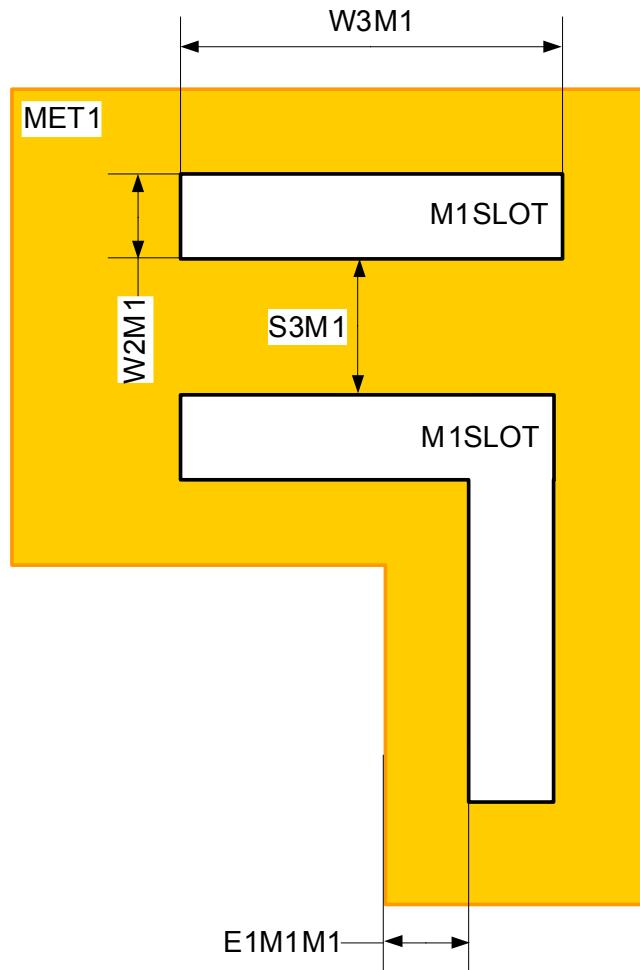
Figure 3.14 MET1

3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ M1SLOT

## M1SLOT

Name	Description	Value	Unit
B1M1	All MET1 tracks > 35µm wide to be slotted (except Pads)	-	-
W2M1	Minimum M1SLOT width	0.6	µm
W3M1	Minimum M1SLOT length	20.0	µm
S3M1	<b>Note:</b> If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
E1M1M1	Minimum MET1 enclosure of M1SLOT	10.0	µm
	<b>Note:</b> M1SLOT without MET1 is not allowed.		

**Note:** Insert M1SLOTS in direction of current flow.



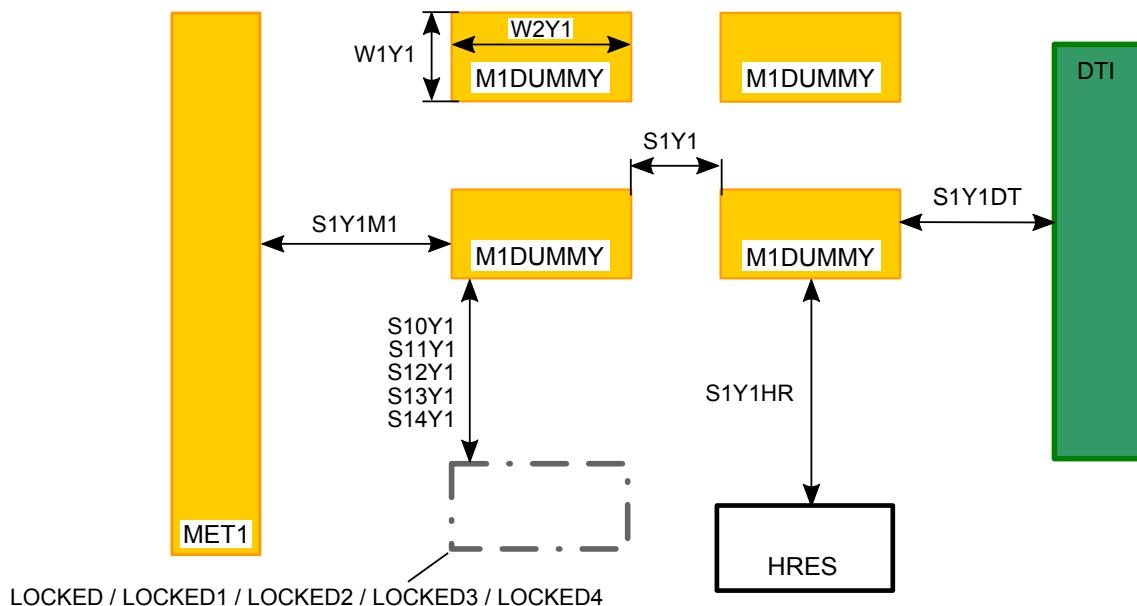
**Figure 3.15 M1SLOT**

## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ M1DUMMY

**M1DUMMY**

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y1	Only rectangular M1DUMMY is allowed	-	-
B2Y1	M1DUMMY overlap of MET1 is not allowed	-	-
B3Y1	M1DUMMY overlap of CONT or VIA1 is not allowed	-	-
B4Y1	M1DUMMY overlap of HRES is not allowed	-	-
B5Y1	M1DUMMY overlap of DTI is not allowed	-	-
W1Y1	Minimum M1DUMMY width	2.0	μm
W2Y1	Maximum M1DUMMY edge length	20.0	μm
S1Y1	Minimum M1DUMMY spacing	2.0	μm
S10Y1	Minimum M1DUMMY spacing to LOCKED	4.0	μm
S11Y1	Minimum M1DUMMY spacing to LOCKED1	4.0	μm
S12Y1	Minimum M1DUMMY spacing to LOCKED2	4.0	μm
S13Y1	Minimum M1DUMMY spacing to LOCKED3	4.0	μm
S14Y1	Minimum M1DUMMY spacing to LOCKED4	4.0	μm
S1Y1DT	Minimum M1DUMMY spacing to DTI	0.5	μm
S1Y1HR	Minimum M1DUMMY spacing to HRES	5.0	μm
S1Y1M1	Minimum M1DUMMY spacing to MET1	4.0	μm

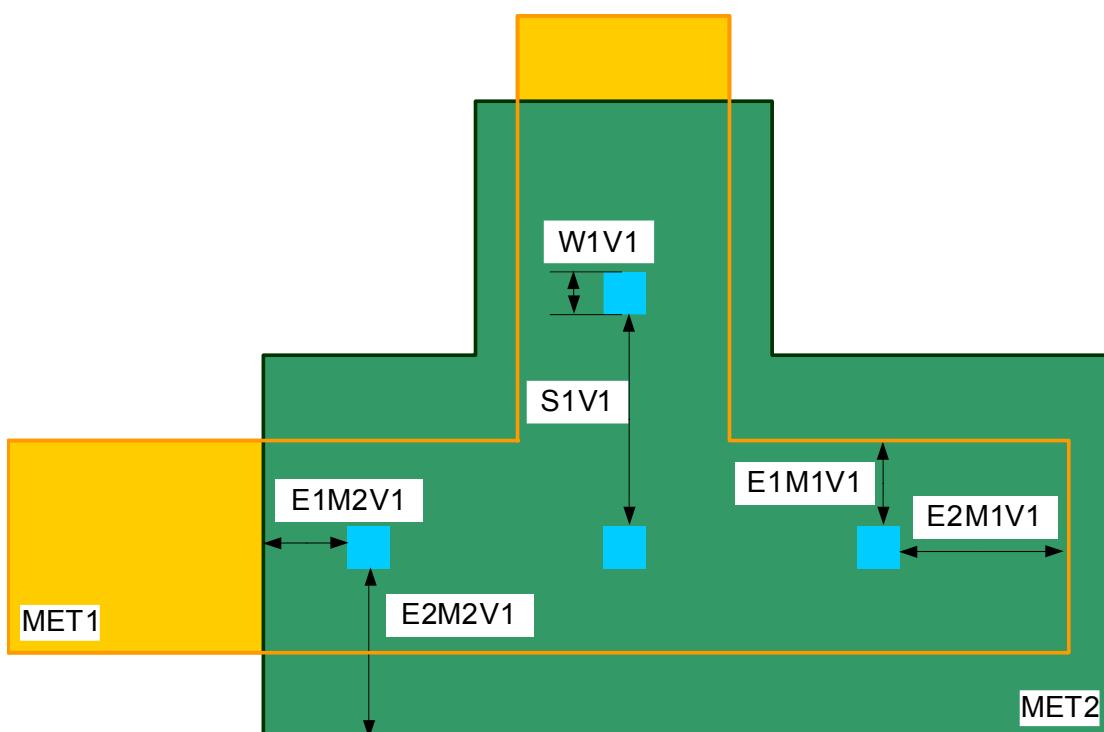
**Figure 3.16 M1DUMMY**

3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ VIA1

### VIA1

Name	Description	Value	Unit
B1V1	VIA1 must be covered by MET1 and MET2	-	-
W1V1	Fixed VIA1 size	0.26 x 0.26	μm x μm
S1V1	Minimum VIA1 spacing	0.26	μm
E1M1V1	Minimum MET1 enclosure of VIA1	0.01	μm
E1M2V1	Minimum MET2 enclosure of VIA1	0.01	μm
E2M1V1	Minimum MET1 enclosure of VIA1 (in one direction of VIA1 corner)	0.06	μm
E2M2V1	Minimum MET2 enclosure of VIA1 (in one direction of VIA1 corner)	0.06	μm
R1V1	Maximum ratio of VIA1 area to connected GATE area	20.0	-

**Note:** Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".



**Figure 3.17 VIA1**

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → MET2

## MET2

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1M2M1	MET2 overlap of MET1 is not allowed (different net, tag_#, MET1, MET2 difference >300V)	-	-
W1M2	Minimum MET2 width	0.28	μm
<i>W4M2</i>	Minimum MET2 width joining wide MET2 track (> 35 μm)	10.0	μm
<i>W4M2</i>	<b>Note:</b> No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 μm from the main track prior to narrowing.		
<i>W5M2</i>	Maximum MET2 region size	17.0 x 17.0	μm x μm
<i>W5M2</i>	<b>Note:</b> MET2 regions are defined as MET2 shapes (single MET2 shapes or a bundle of MET2 shapes, with width > 2.0μm, inclusive of the spacing if the spacing is <= 1.0μm) without any other metal layer above. For further information and design guidelines, please refer to the application note about <a href="#">IMD popping</a> on "my X-FAB".		
<i>W5M2</i>	<b>Note:</b> Not checked with standard DRC, option for check is available.		
S1M2	Minimum MET2 spacing/notch	0.28	μm
<i>S4M2</i>	Minimum MET2 spacing (different net, tag_#, difference >25V ≤ 60V)	0.4	μm
<i>S4M2</i>	<b>Note:</b> Valid for spacing of all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".		
<i>S5M2</i>	Minimum MET2 spacing (different net, tag_#, difference >60V ≤100V)	0.6	μm
<i>S5M2</i>	<b>Note:</b> Valid for spacing of all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".		
<i>S6M2</i>	Minimum MET2 spacing (different net, tag_#, difference >100V ≤200V)	0.8	μm
<i>S6M2</i>	<b>Note:</b> Valid for spacing to all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >100V ≤ 200V. Refer to the design related guideline "Voltage class definitions".		
<i>S7M2</i>	Minimum MET2 spacing (different net, tag_#, difference >200V ≤300V)	1.2	μm
<i>S7M2</i>	<b>Note:</b> Valid for spacing to all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤ 300V. Refer to the design related guideline "Voltage class definitions".		
<i>S8M2</i>	Minimum MET2 spacing (different net, tag_#, difference >300V)	1.6	μm
<i>S8M2</i>	<b>Note:</b> Valid for spacing to all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
S2M2	Minimum MET2 spacing to WIDE_MET2	0.6	μm
<i>S2M2M1</i>	Minimum MET2 spacing to MET1 (different net, tag_#, difference >300V)	1.6	μm
<i>S2M2M1</i>	<b>Note:</b> Valid if the voltage difference between MET1, MET2 voltage is >300V.		
<i>S2M2M1</i>	<b>Note:</b> Valid for spacing of all MET2/MET1 shapes with label tag_# to all MET1/MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
A1M2	Minimum MET2 area	0.202	μm <sup>2</sup>
<i>R1M2</i>	Minimum ratio of MET2 area to EXTENT area	30.0	%
<i>R1M2</i>	<b>Note:</b> Not checked with standard DRC, option for check is available.		
<i>R2M2</i>	Maximum ratio of MET2 area to EXTENT area	65.0	%
<i>R2M2</i>	<b>Note:</b> Not checked with standard DRC, option for check is available.		
<i>R1M2P1</i>	Maximum ratio of MET2 area to connected GATE area	400.0	-
<i>R1M2P1</i>	<b>Note:</b> Refer to section "Antenna Rule definitions" as well.		



## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ MET2

Name	Description	Value	Unit
R2M2P1	Maximum ratio of MET2 area to connected GATE area <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	400.0	-
Q1M2	Resistor terminal net without VLABEL <b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".	-	-

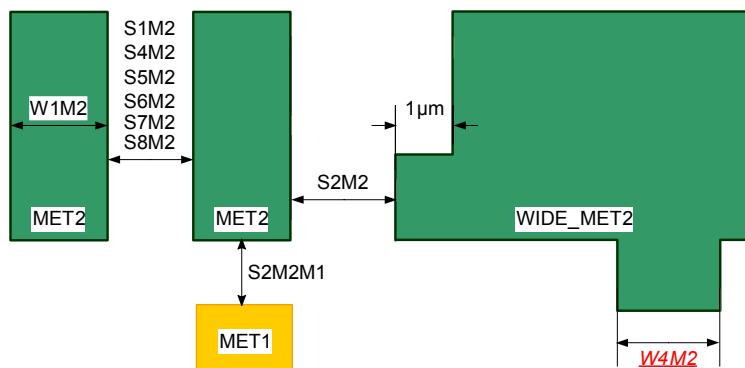


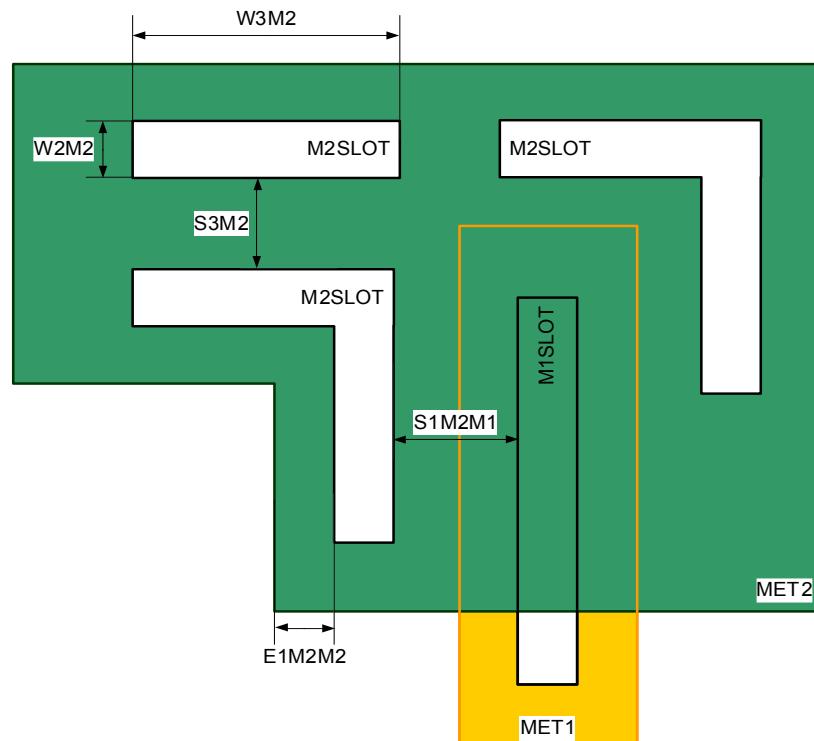
Figure 3.18 MET2

3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.1 Layer rules→ M2SLOT

## M2SLOT

Name	Description	Value	Unit
B1M2	All MET2 tracks > 35µm wide to be slotted (except Pads)	-	-
W2M2	Minimum M2SLOT width	0.6	µm
W3M2	Minimum M2SLOT length	20.0	µm
	<b>Note:</b> If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M2	Minimum M2SLOT spacing/notch	10.0	µm
S1M2M1	Minimum M2SLOT spacing to M1SLOT	2.0	µm
	<b>Note:</b> M2SLOT is not allowed over M1SLOT.		
E1M2M2	Minimum MET2 enclosure of M2SLOT	10.0	µm
	<b>Note:</b> M2SLOT without MET2 is not allowed		

**Note:** Insert M2SLOTS in direction of current flow.



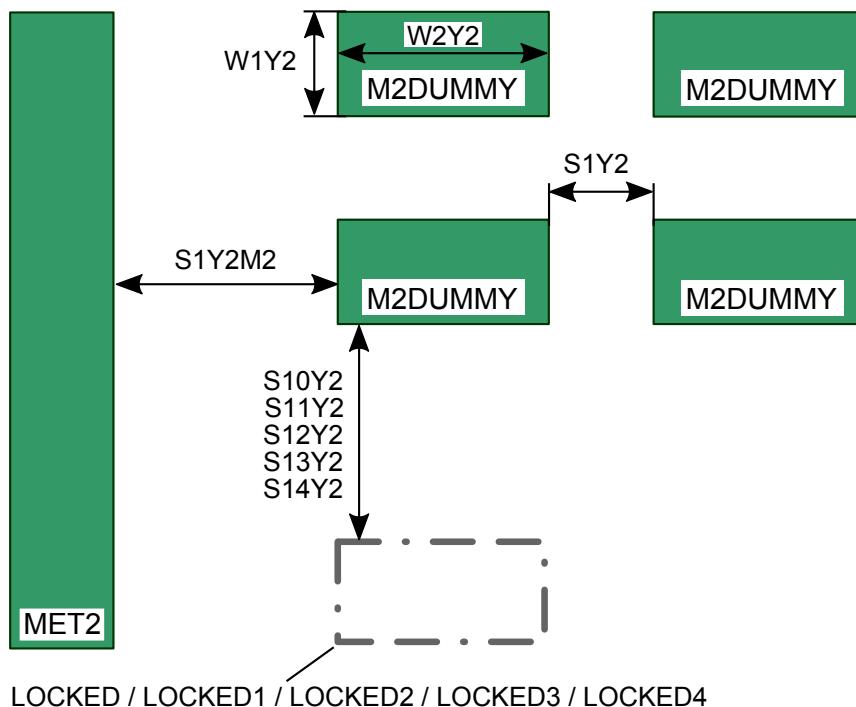
**Figure 3.19 M2SLOT**

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → M2DUMMY

**M2DUMMY**

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y2	Only rectangular M2DUMMY is allowed	-	-
B2Y2	M2DUMMY overlap of MET2 is not allowed	-	-
B3Y2V1	M2DUMMY overlap of VIA1 is not allowed	-	-
B3Y2V2	M2DUMMY overlap of VIA2 is not allowed	-	-
B3Y2VT	M2DUMMY overlap of VIATP is not allowed	-	-
<b>Note:</b> Only valid if module MET3 is not selected.			
W1Y2	Minimum M2DUMMY width	2.0	μm
W2Y2	Maximum M2DUMMY edge length	20.0	μm
S1Y2	Minimum M2DUMMY spacing	2.0	μm
S10Y2	Minimum M2DUMMY spacing to LOCKED	4.0	μm
S11Y2	Minimum M2DUMMY spacing to LOCKED1	4.0	μm
S12Y2	Minimum M2DUMMY spacing to LOCKED2	4.0	μm
S13Y2	Minimum M2DUMMY spacing to LOCKED3	4.0	μm
S14Y2	Minimum M2DUMMY spacing to LOCKED4	4.0	μm
S1Y2M2	Minimum M2DUMMY spacing to MET2	4.0	μm

**Figure 3.20 M2DUMMY****LOCKED, LOCKED1, LOCKED2**

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED\* layers are part of the X-FAB provided IP LEF file.

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.1 Layer rules → LOCKED, LOCKED1, LOC...

Name	Description	Value	Unit
BDLOCK	Any structure over LOCKED (ALL) or LOCKED (boundary) is not allowed	-	-
B1LOCK	Any structure over LOCKED (LOCKED1) or LOCKED1 (boundary) is not allowed  <b>Note:</b> Except: - METTPL if (MET4 and METMID) modules are selected or MET5 module is selected - METTP if MET5 module is selected - METCOP	-	-
B2LOCK	Any structure over LOCKED (LOCKED2) or LOCKED2 (boundary) is not allowed  <b>Note:</b> Except: - METTPL if (MET3 and METMID) modules are selected or MET4 module is selected - METTP if MET4 module is selected - MET5 - METCOP	-	-

## LOCKED3

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED\* layers are part of the X-FAB provided IP LEF file.

Name	Description	Value	Unit
B3LOCK	Any structure over LOCKED3 is not allowed  <b>Note:</b> Except: - METTPL if METMID module is selected or MET3 module is selected - METTP if MET3 module is selected - MET5 - MET4 - METCOP	-	-

## LOCKED4

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED\* layers are part of the X-FAB provided IP LEF file.

Name	Description	Value	Unit
B4LOCK	Any structure over LOCKED4 is not allowed  <b>Note:</b> Except: - METTPL, METTP, MET5, MET4, MET3, METCOP	-	-

## CAPDEF

This layer is only used to define certain capacitors.

## DIODEF

This layer is used to define diodes that are to be extracted into the netlist. All diodes without DIODEF are extracted as parasitic components. DIODEF must encompass the entire P/N junction forming the diode.

## XFLAY

This layer is a reserved layer.

Name	Description	Value	Unit
BDXF	Not allowed to be used by customers	-	-

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → ne, pe

### 3.1.2 Device rules

**ne, pe**

Name	Description	Value	Unit
W3DF	Minimum GATE width  <b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22µm.	0.22	µm
W4P1	Minimum GATE length  <b>Note:</b> The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18µm at any dimension.	0.18	µm

**Note:** If the module MOS5 is selected, ne, pe are not available

**Note:** For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

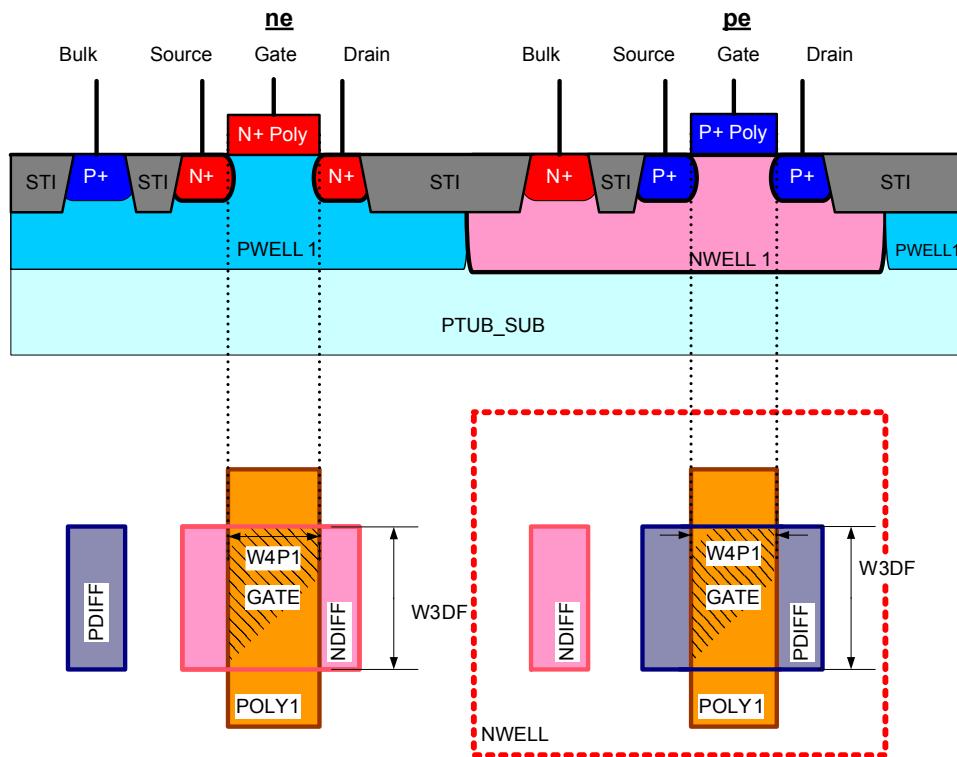


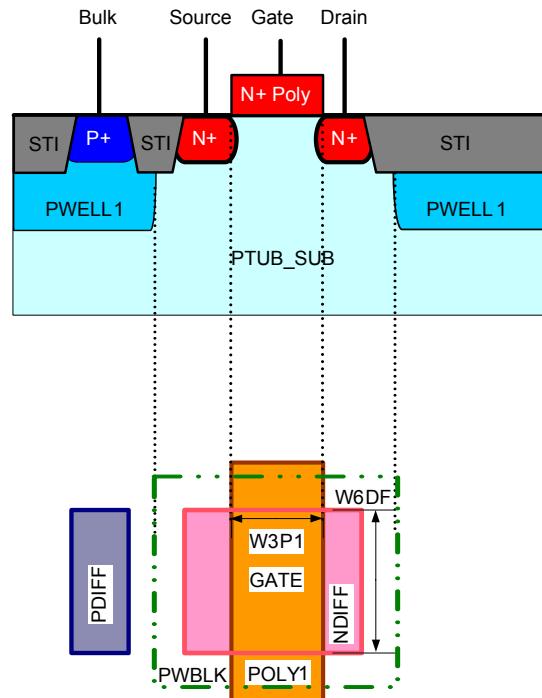
Figure 3.21 ne,pe

## 3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.2 Device rules→ nn

**nn**

Name	Description	Value	Unit
B3GA	Only rectangular GATE inside PWBLK is allowed	-	-
W3P1	Minimum GATE length	1.0	μm
W6DF	Minimum GATE width	1.0	μm

**Note:** If the module MOS5 is selected, nn is not available

**Figure 3.22 nn**

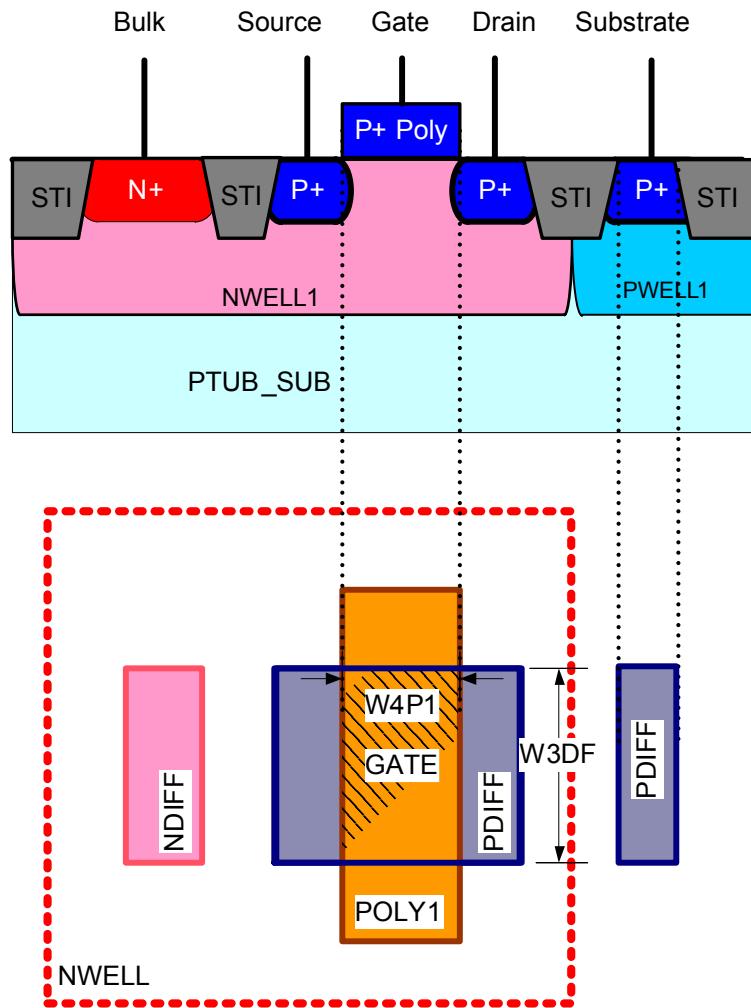
3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → pe\_5

### **pe\_5**

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.		
W4P1	Minimum GATE length	0.18	μm
	<b>Note:</b> The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18μm at any dimension.		

**Note:** If the module MOS5 is selected, pe\_5 is not available

### **pe\_5**



**Figure 3.23 pe\_5**

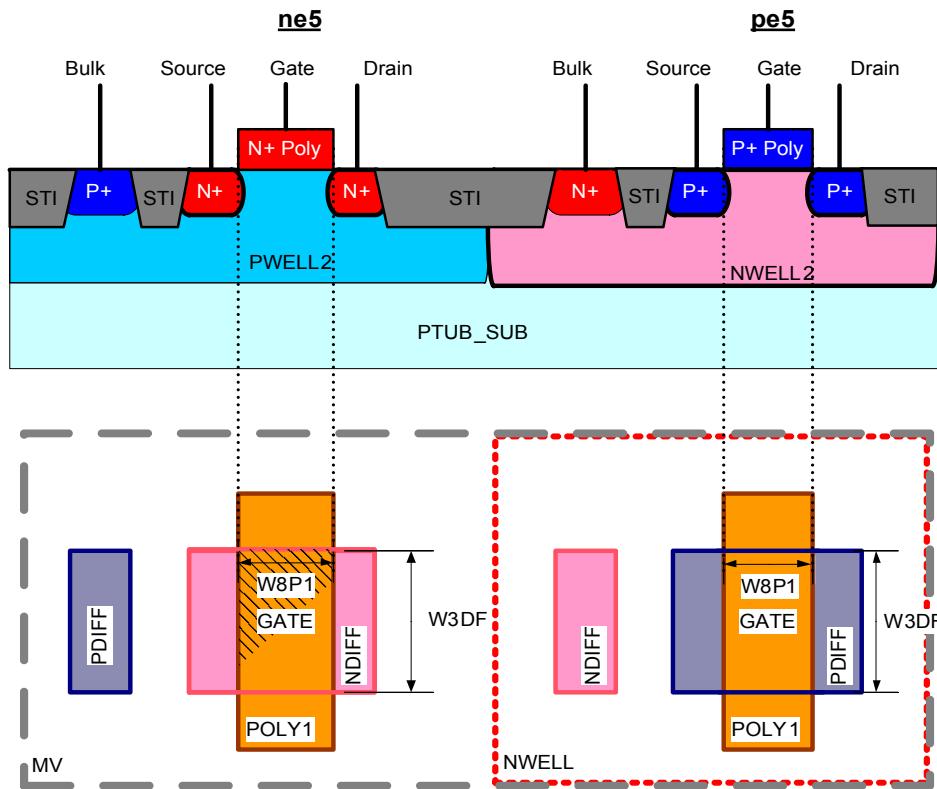
3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → ne5, pe5

### ne5, pe5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.		
W8P1	Minimum GATE length	0.5	μm

**Note:** MV is necessary for ne5 and pe5

**Note:** For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.



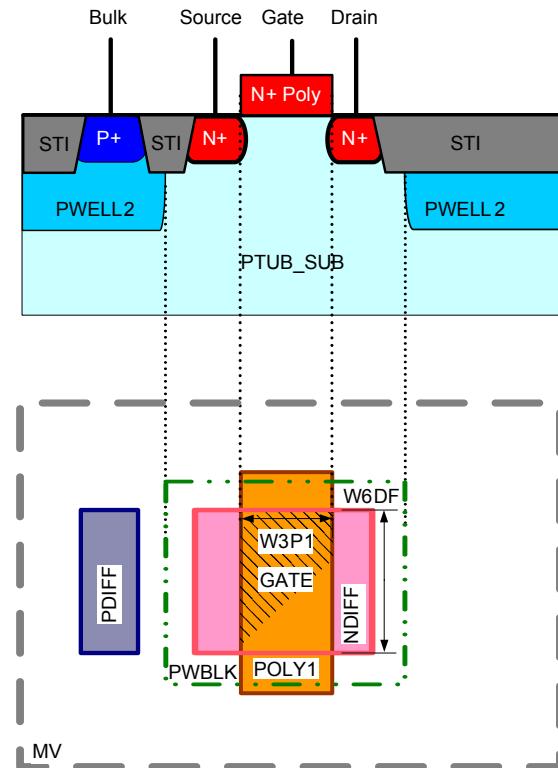
**Figure 3.24** ne5,pe5

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → nn5

### nn5

Name	Description	Value	Unit
B3GA	Only rectangular GATE inside PWBLK is allowed	-	-
W3P1	Minimum GATE length	1.0	μm
W6DF	Minimum GATE width	1.0	μm

**Note:** MV is necessary for nn5



**Figure 3.25 nn5**

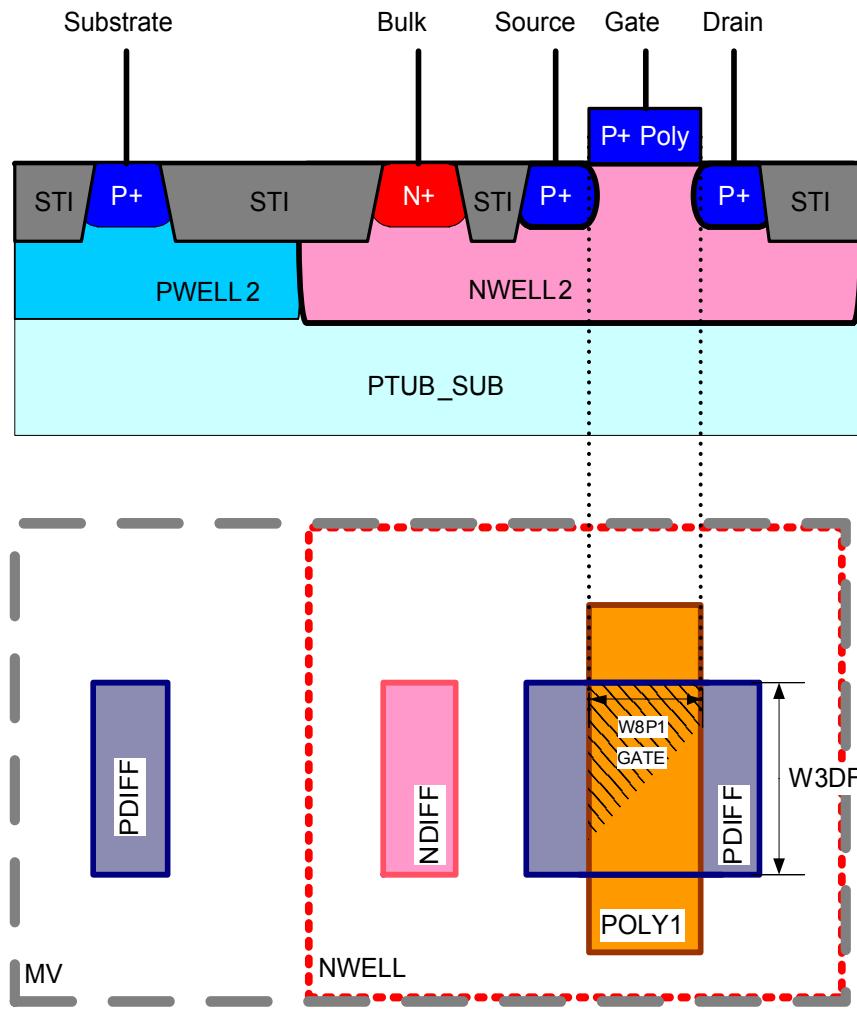
3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → pe5\_5

### **pe5\_5**

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.		
W8P1	Minimum GATE length	0.5	μm

**Note:** MV is necessary for pe5\_5

### **pe5\_5**



**Figure 3.26 pe5\_5**

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → qpve, qpvf, qpvg

### **qpve, qpvf, qpvg**

The devices qpve, qpvf and qpvg use PDIFF as emitter, NWELL1 as base and PWELL1 as collector. The layouts of qpve, qpvf and qpvg are predefined. They must not be changed.

#### **qpve**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $2 \times 2 \mu\text{m}^2$

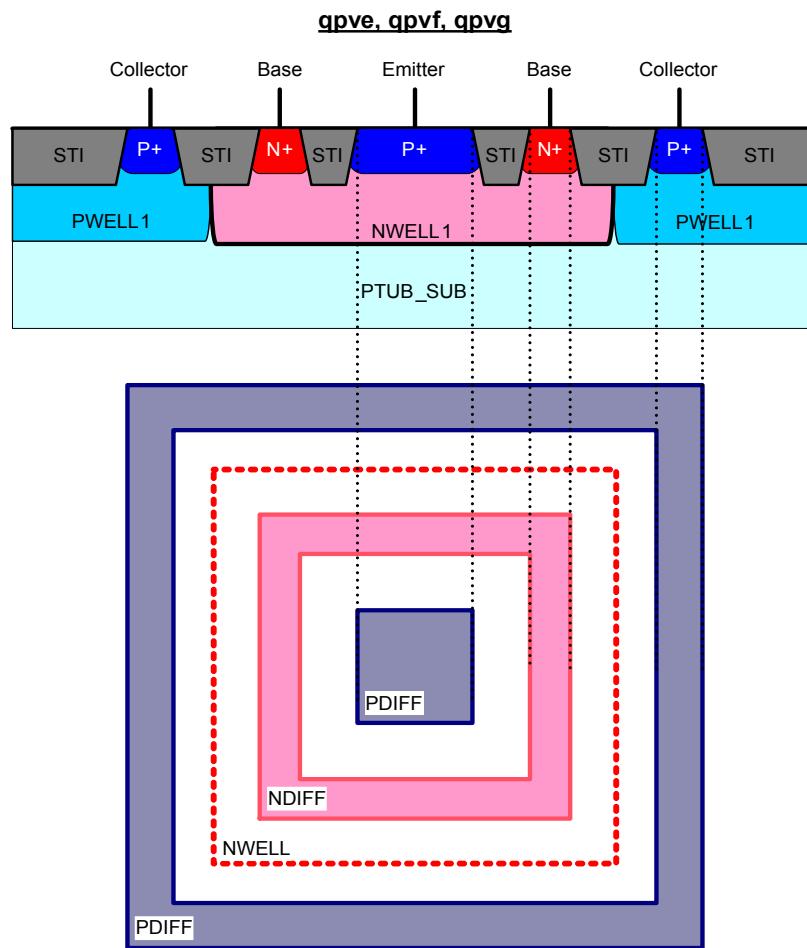
#### **qpvf**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $5 \times 5 \mu\text{m}^2$

#### **qpvg**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $10 \times 10 \mu\text{m}^2$

**Note:** If the module MOS5 is selected, qpve, qpvf, qpvg are not available



**Figure 3.27 qpve,qpvf,qpvg**

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → qpve5, qpvf5, qpvg5

### **qpve5, qpvf5, qpvg5**

This section describes the vertical PNP transistors qpve5, qpvf5, and qpvg5.

These transistors use PDIFF as emitter, NWELL2 as base and PWELL2 as collector. Their layouts are predefined. They must not be changed.

#### **qpve5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $2 \times 2 \mu\text{m}^2$

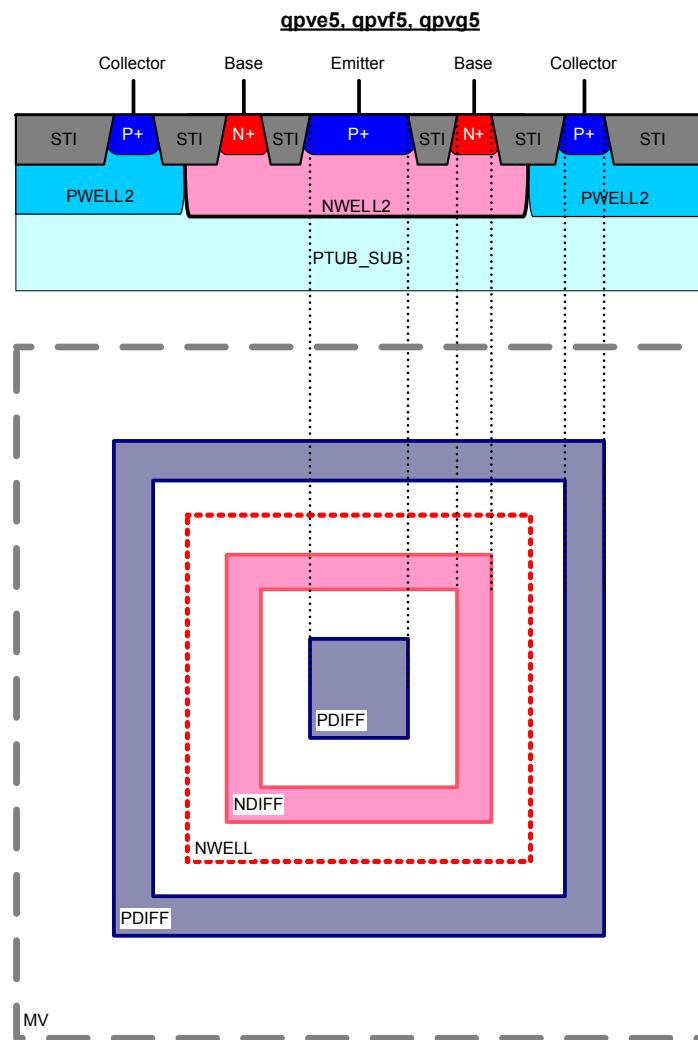
#### **qpvf5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $5 \times 5 \mu\text{m}^2$

#### **qpvg5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $10 \times 10 \mu\text{m}^2$

**Note:** MV is necessary for qpve5, qpvf5 and qpvg5.



**Figure 3.28 qpve5, qpvf5, qpvg5**

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → rdn, rdp

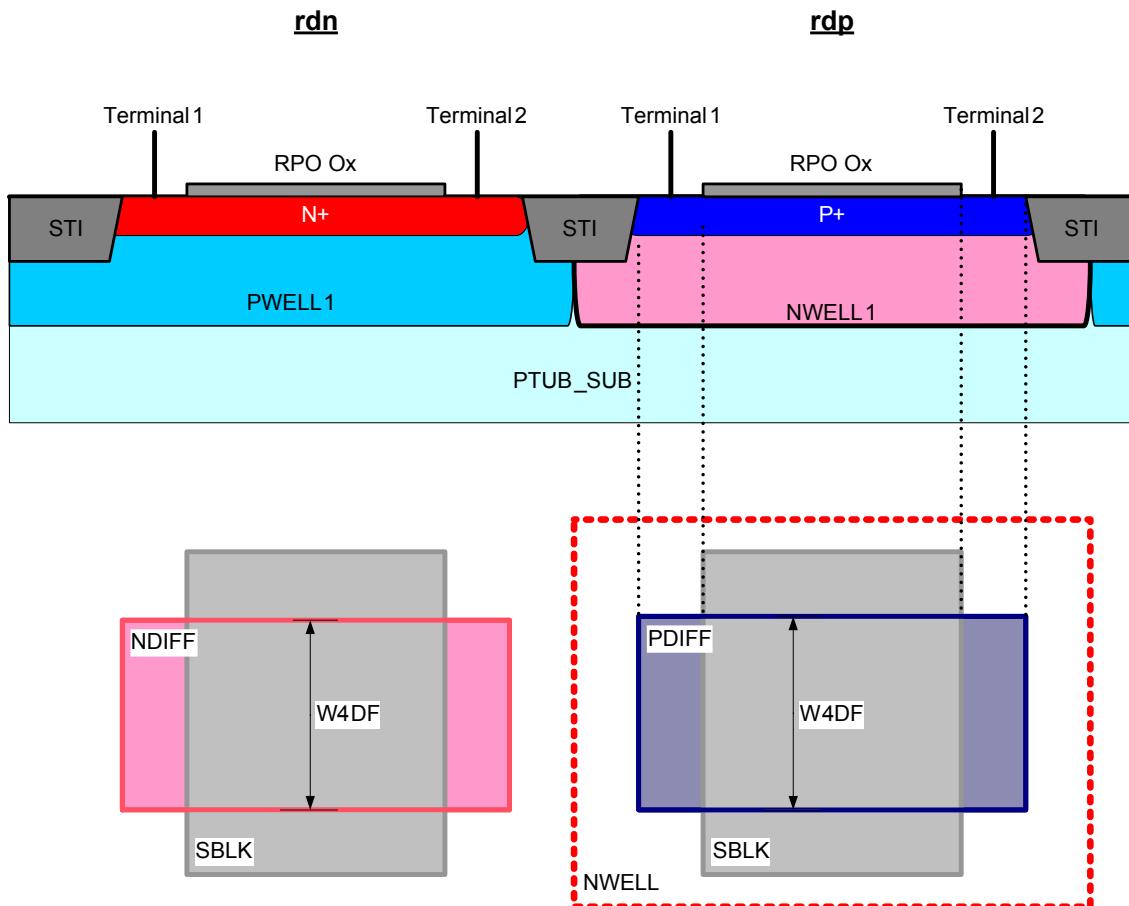
### rdn, rdp

Name	Description	Value	Unit
W4DF	Minimum width	0.42	μm

**Note:** rdn resistor definition: SBLK and not NWELL and NDIFF (except GATE)  
rdp resistor definition: SBLK and NWELL and PDIFF (except GATE)

**Note:** Recommended minimum number of squares is L/W ≥ 5.

**Note:** If the module MOS5 is selected, rdn, rdp, are not available



**Figure 3.29** rdn, rdp

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → rnw

**rnw**

Name	Description	Value	Unit
W2NW	Minimum width	2.0	μm

**Note:** Recommended minimum number of squares is L/W ≥ 5.

**Note:** rnw resistor definition: NWELL and NW\_VERIFY

**Note:** If the module MOS5 is selected, rnw is not available

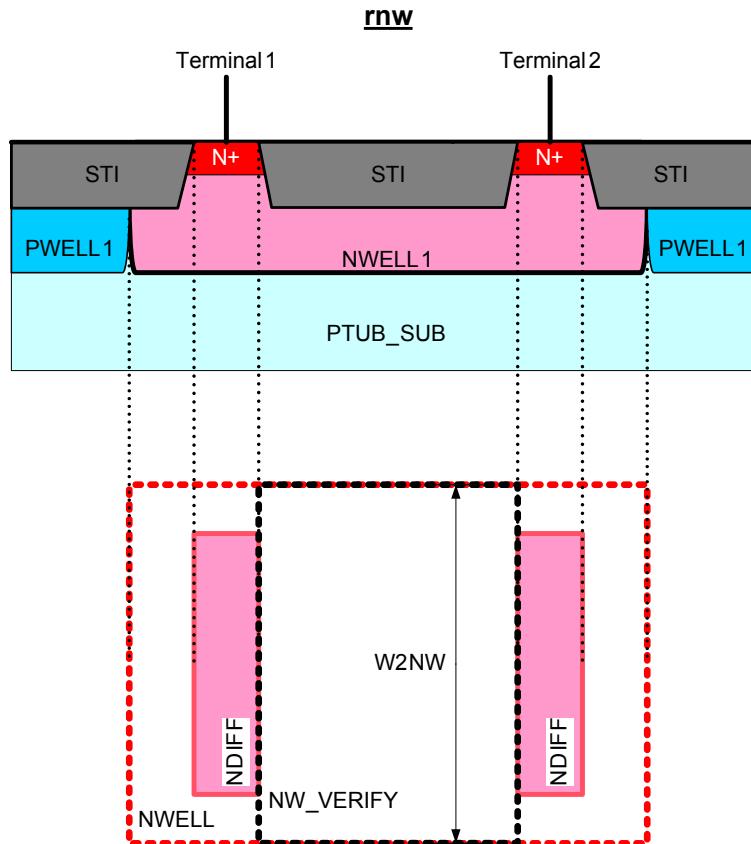


Figure 3.30 rnw

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → rdn5, rdp5

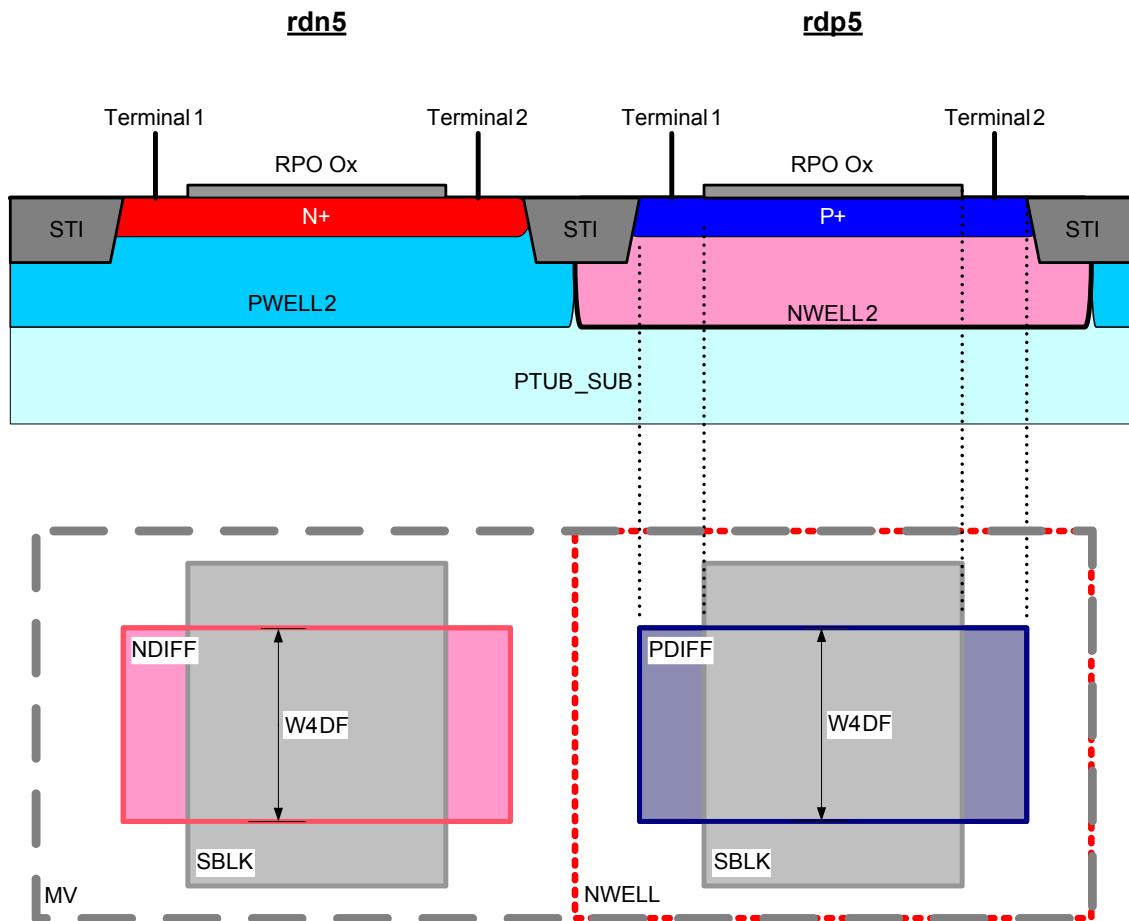
### **rdn5, rdp5**

Name	Description	Value	Unit
B1DN	rdn5 overlap of DEPL or HVDEPL is not allowed	-	-
W4DF	Minimum width	0.42	μm

**Note:** Recommended minimum number of squares is L/W ≥ 5.

**Note:** MV is necessary for rdn5, rdp5

**Note:** rdn5 resistor definition: SBLK and not NWELL and NDIFF (except GATE)  
rdp5 resistor definition: SBLK and NWELL and PDIFF (except GATE)



**Figure 3.31** rdn5, rdp5

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → rnw5

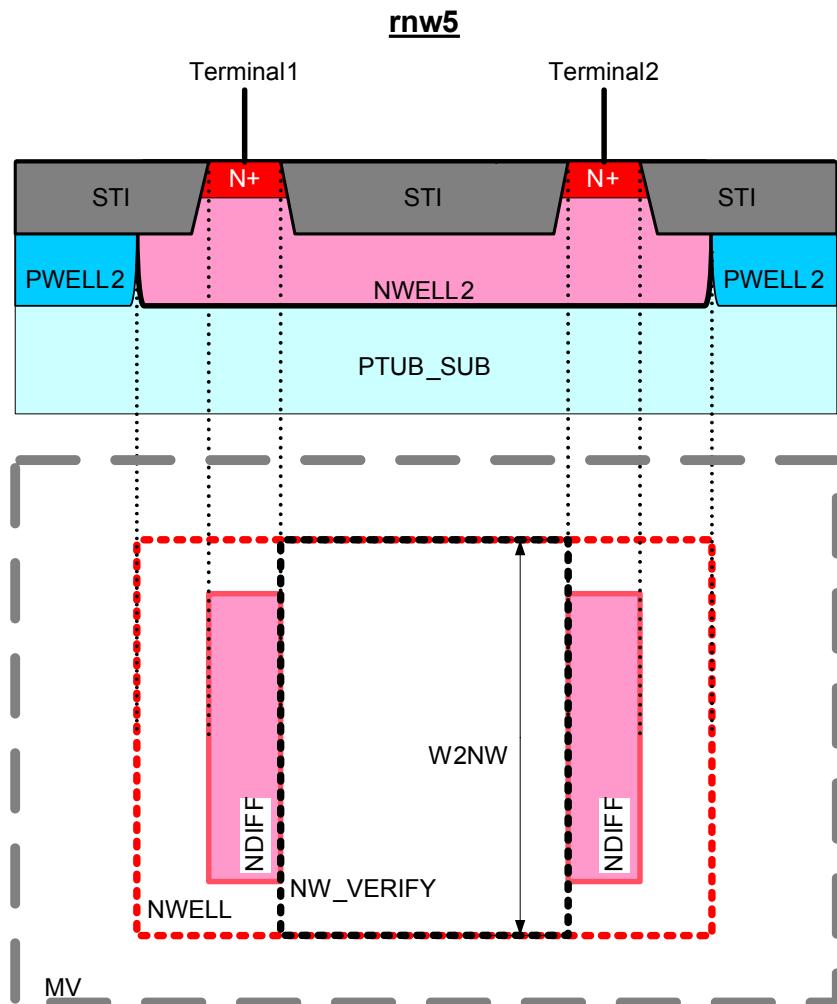
### **rnw5**

Name	Description	Value	Unit
W2NW	Minimum width	2.0	μm

**Note:** Recommended minimum number of squares is  $L/W \geq 5$ .

**Note:** rnw5 resistor definition: NWELL and NW\_VERIFY

**Note:** MV is necessary for rnw5



**Figure 3.32 rnw5**

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → rnp1, rnp1\_3, rnp1a\_...

### **rnp1, rnp1\_3, rnp1a\_3, rpp1, rpp1\_3, rpp1nw\_3, rpp1s, rpp1s\_3**

Name	Description	Value	Unit
B16P1	rpp1#, rnp1#, rpp1s# overlap of DTI is not allowed	-	-
B22P1	(rnp1_3 NOT NWELL) without MV is not allowed	-	-
B23P1	rnp1a_3 overlap of NWELL or MV is not allowed	-	-
B24P1	rpp1nw_3 without NWELL is not allowed	-	-
B25P1	rpp1nw_3 overlap of rnw/rnw5 is not allowed	-	-
B27P1	rnp1a_3 overlap of rnw/rnw5 is not allowed	-	-
B2CT	CONT is not allowed within rpp1s#	-	-
B6P1	rnp1_3 overlap of rnw/rnw5 is not allowed	-	-
B7P1	rpp1_3 overlap of NWELL is not allowed	-	-
B8P1	rpp1s_3 overlap of rnw/rnw5 is not allowed	-	-
B4P1	rnp1_3 crossing NWELL edge is not allowed	-	-
B5P1	rpp1s_3 crossing NWELL edge is not allowed	-	-
W15P1	Minimum rnp1#, rpp1# width	0.42	μm
S1INP1	Minimum NIMP spacing to rpp1# or rpp1s#	0.26	μm
S1IPP1	Minimum PIMP spacing to rnp1#	0.26	μm
E1INP1	Minimum NIMP extension beyond rnp1#	0.18	μm
E1IPP1	Minimum PIMP extension beyond rpp1# or rpp1s#	0.18	μm

**Note:** Recommended minimum number of squares is L/W ≥ 5.

**Note:** Do not use dog-bone at the end of POLY1 resistor for CONT pickup.

**Note:** CONT array for POLY1 resistor should be a single column.

**Note:** rnp1# resistor definition: POLY1 and SBLK and NIMP (except GATE oversized by 0.22μm and except POLY1 nmvab oversized by 0.05μm (in the direction of GATE length)).

**Note:** rnp1\_3 device must be labeled "rnp1\_3" using POLY1 (VERIFICATION) layer

**Note:** rnp1a\_3 device must be labeled "rnp1a\_3" using POLY1 (VERIFICATION) layer

**Note:** rpp1# resistor definition: POLY1 and SBLK and PIMP (except GATE oversized by 0.22μm and except POLY1 of pmvab oversized by 0.05μm (in the direction of GATE length)).

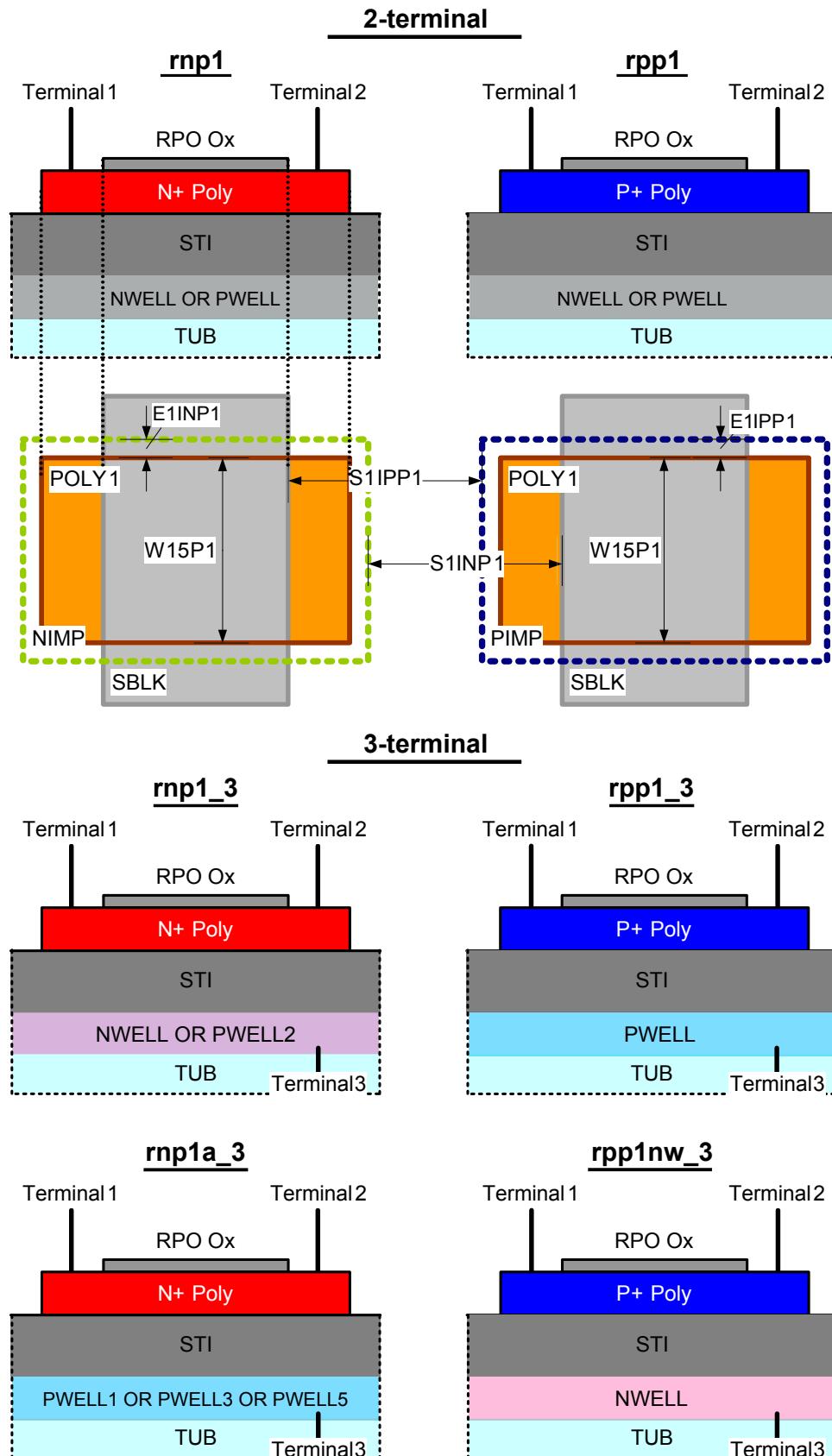
**Note:** rpp1\_3 device must be labeled "rpp1\_3" using POLY1 (VERIFICATION) layer.

**Note:** rpp1nw\_3 device must be labeled "rpp1nw\_3" using POLY1 (VERIFICATION) layer.

**Note:** rpp1s# resistor definition: POLY1 and POLY1\_VERIFY and PIMP. (except rpp1 oversized by 0.22 μm and not GATE)

**Note:** rpp1s\_3 device must be labeled "rpp1s\_3" using POLY1 (VERIFICATION) layer.

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → rnp1, rnp1\_3, rnp1a\_...



**Figure 3.33 rnp1# and rpp1#**

3. Layer and Device rules → 3.1 LP5MOS main module→ 3.1.2 Device rules→ rnp1, rnp1\_3, rnp1a\_...

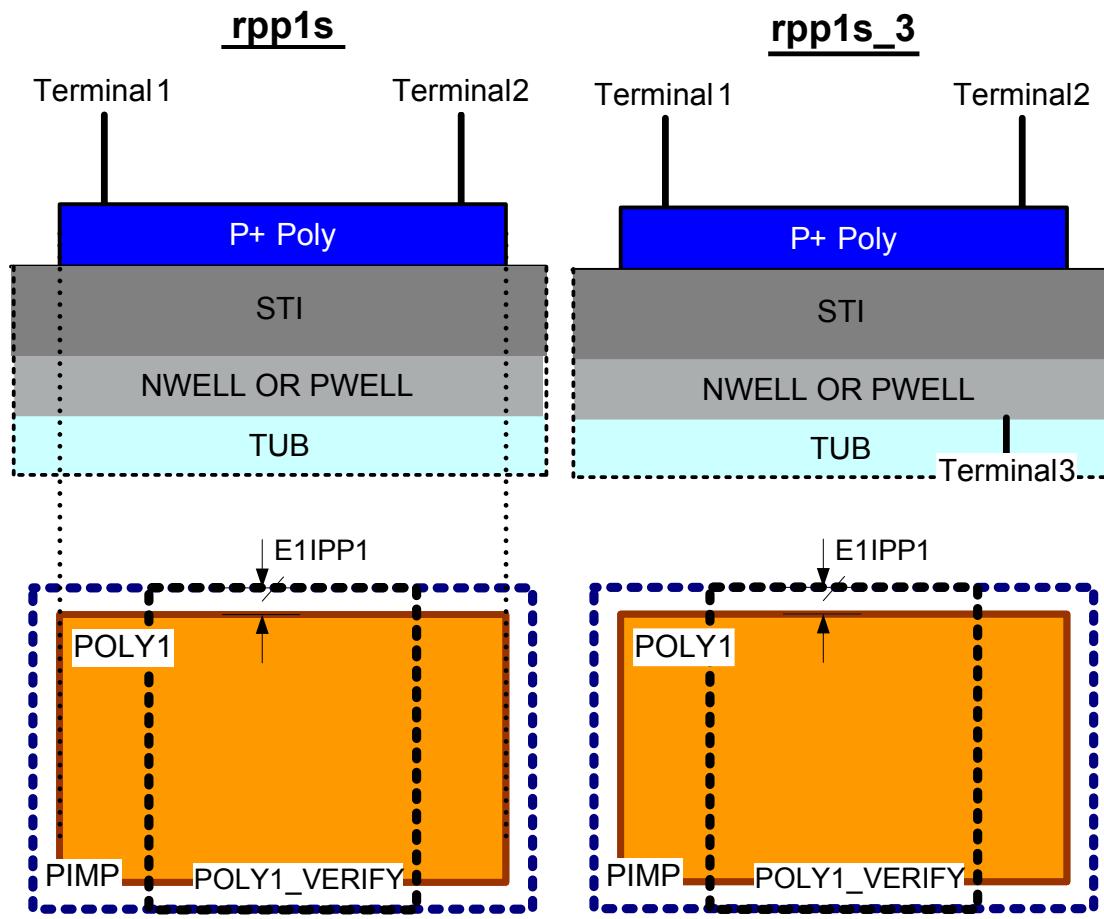


Figure 3.34 rpp1s#

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → rm1, rm2

### **rm1, rm2**

Name	Description	Value	Unit
B2M1	CONT or VIA1 is not allowed within rm1	-	-
B2M2	VIA1 is not allowed within rm2	-	-
B3M2	VIATP is not allowed within rm2	-	-
	<b>Note:</b> valid if MET3 module is not selected		
B4M2	VIA2 is not allowed within rm2	-	-
	<b>Note:</b> Valid if MET3 module is selected.		

**Note:** rm1 resistor definition: MET1 and M1VERIFY.

**Note:** rm2 resistor definition: MET2 and M2VERIFY.



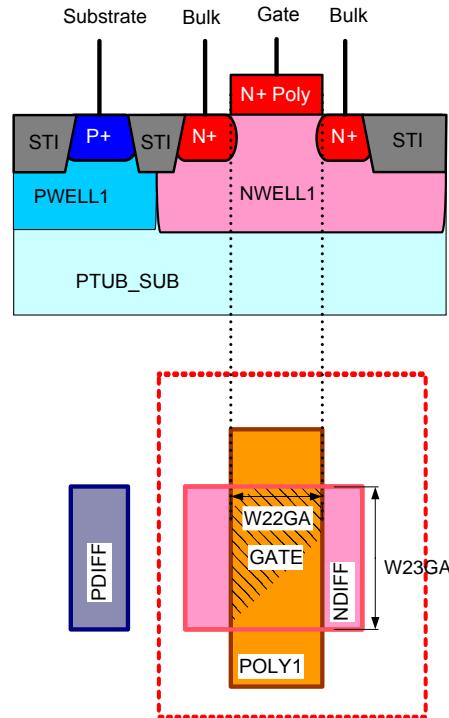
**Figure 3.35** rm1, rm2

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → mosvc

### mosvc

Name	Description	Value	Unit
B5GA	Only rectangular GATE is allowed	-	-
W22GA	Minimum GATE length	2.0	μm
W23GA	Minimum GATE width	2.0	μm

**Note:** If the module MOS5 is selected, mosvc is not available



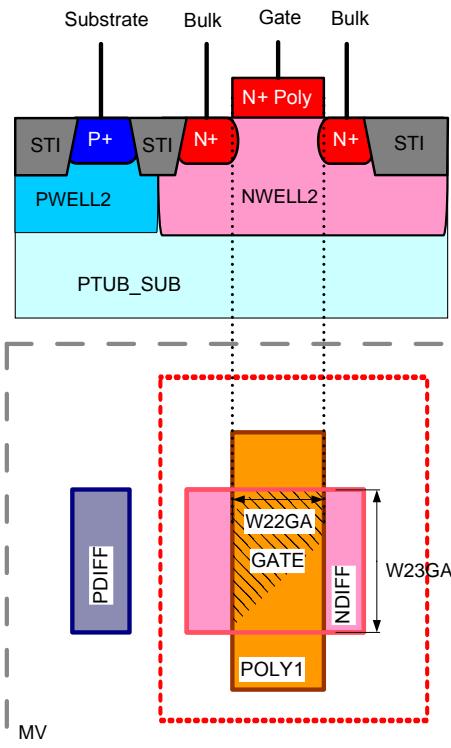
**Figure 3.36** mosvc

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → mosvc5

### mosvc5

Name	Description	Value	Unit
B5GA	Only rectangular GATE is allowed	-	-
W22GA	Minimum GATE length	2.0	μm
W23GA	Minimum GATE width	2.0	μm

**Note:** MV is necessary for mosvc5



**Figure 3.37** mosvc5

### csf2p

The layout of the device csf2p is fixed and must not be changed. A single cell instance has an area of 4.48 μm × 10.80 μm.

Name	Description	Value	Unit
B20P1	csf2p overlap of DTI is not allowed	-	-

**Note:** CAPDEF is necessary for csf2p.

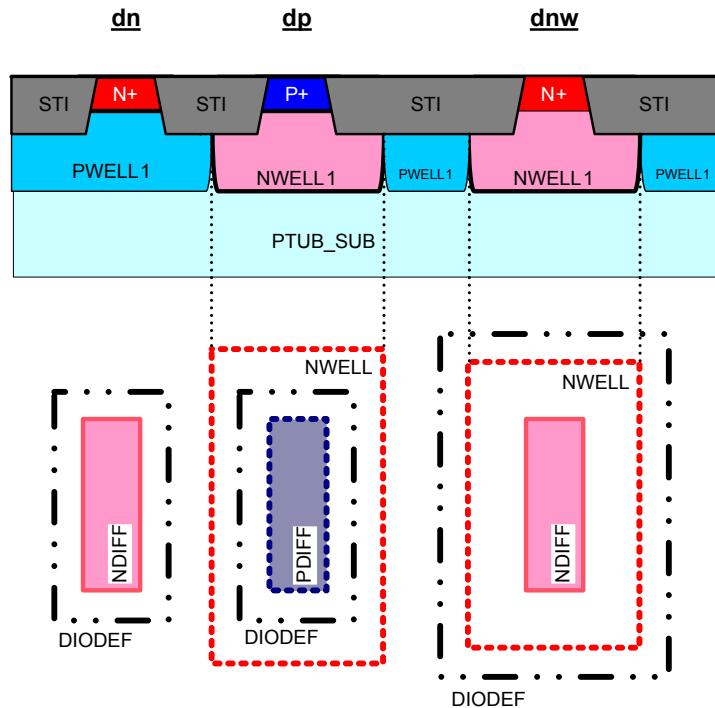
**Note:** Higher values may be achieved by the formation of arrays.

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → dn, dp, dnw

### **dn, dp, dnw**

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.

**Note:** If the module MOS5 is selected, dn, dp, dnw are not available



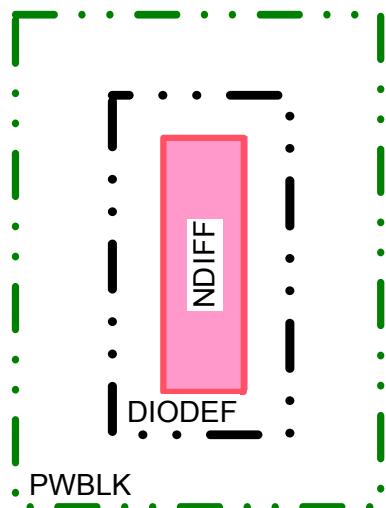
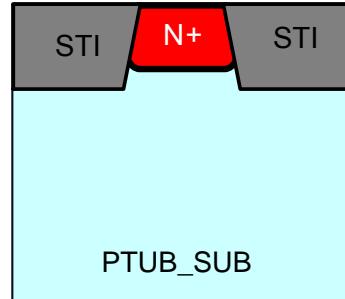
**Figure 3.38 dn,dp,dnw**

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → dnn

### dnn

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.  
**Note:** If the module MOS5 is selected, dnn is not available

dnn



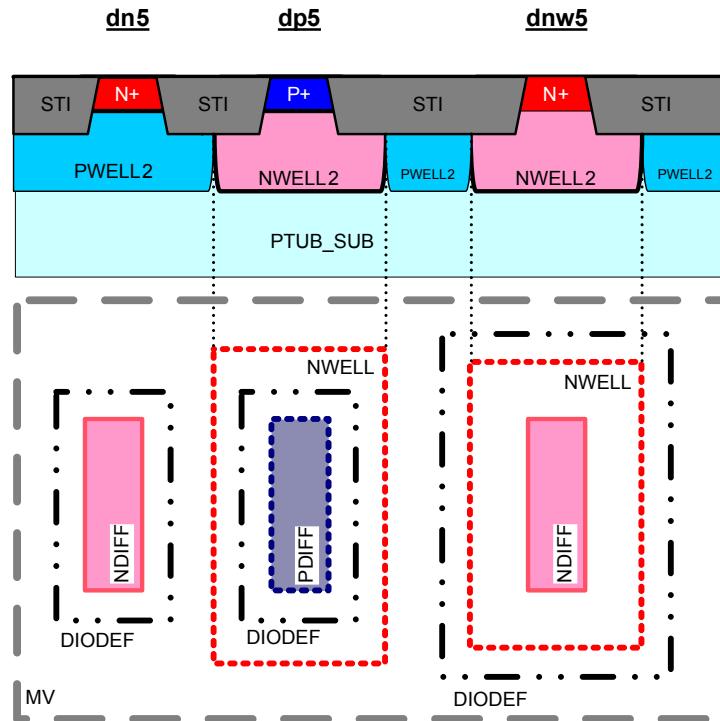
**Figure 3.39** dnn

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → dn5, dp5, dnw5

### **dn5, dp5, dnw5**

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.

**Note:** MV is necessary for dn5, dp5 and dnw5.

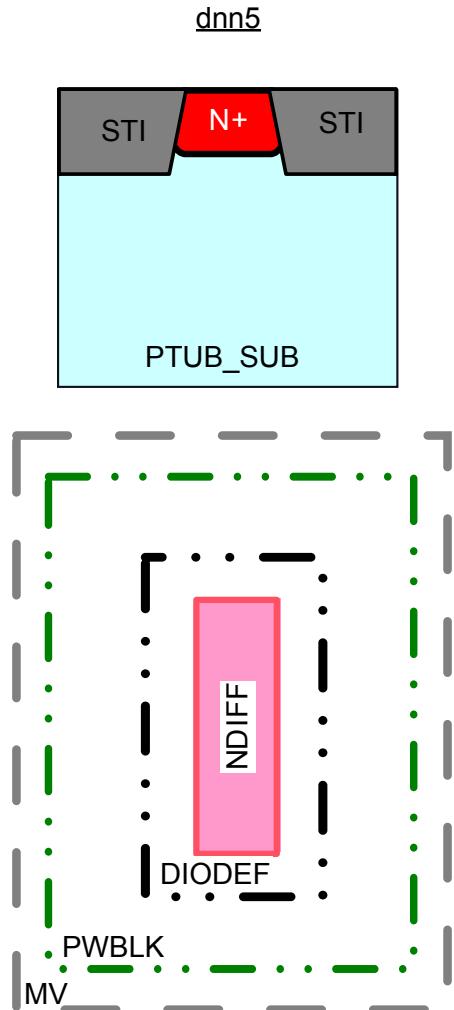


**Figure 3.40 dn5,dp5,dnw5**

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → dnn5

### dnn5

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.  
**Note:** MV is necessary for dnn5.



**Figure 3.41** dnn5

3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → pfuse

## pfuse

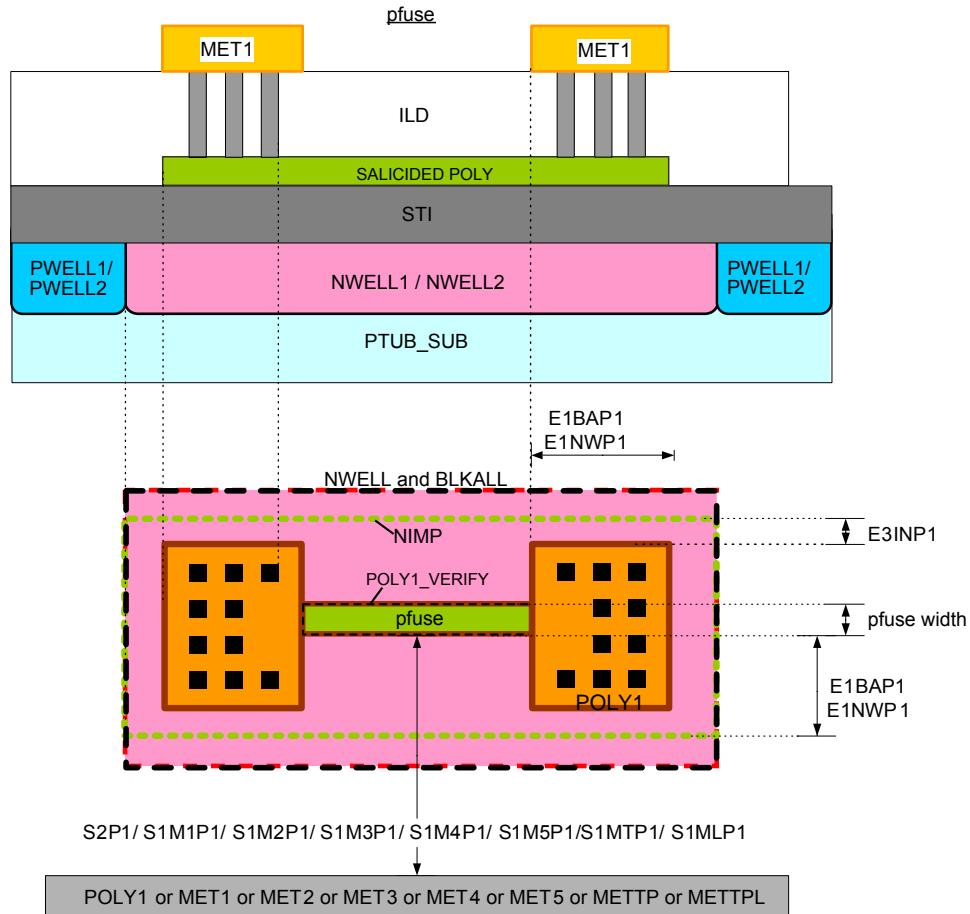
The layout of pfuse is predefined. It must not be changed. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B12P1	pfuse overlap of SBLK or DIFF is not allowed	-	-
B13P1	pfuse without NIMP and BLKALL is not allowed	-	-
B14P1	pfuse overlap of DTI is not allowed	-	-
B15P1	METCOP overlap of pfuse is not allowed	-	-
B2P1	pfuse overlap of MET1, MET2, MET3, MET4, MET5, METTP or METTPL is not allowed	-	-
S1DFP1	Minimum DIFF spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	2.0	μm
S1M1P1	Minimum MET1 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	0.8	μm
S1M2P1	Minimum MET2 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	0.8	μm
S1M3P1	Minimum MET3 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1M4P1	Minimum MET4 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1M5P1	Minimum MET5 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1MCP1	Minimum METCOP spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	10.0	μm
S1MLP1	Minimum METTPL spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1MTP1	Minimum METTP spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1P1DT	Minimum pfuse spacing to DTI	1.7	μm
S2P1	Minimum POLY1 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	2.0	μm
S2SBP1	Minimum SBLK spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	2.0	μm
E1BAP1	Minimum BLKALL enclosure of pfuse	1.7	μm
E1NWP1	Fixed NWELL enclosure of pfuse <b>Note:</b> NWELL is an electrically floating area without any connections.	1.7	μm
E3INP1	Minimum NIMP enclosure of POLY1	0.3	μm

**Note:** pfuse device must be marked with text "PFUSE" on layer POLY1\_VERIFY.

**Note:** pfuse device must have POLY1\_VERIFY layer.

## 3. Layer and Device rules → 3.1 LP5MOS main module → 3.1.2 Device rules → pfuse

**Figure 3.42** pfuse

3. Layer and Device rules → 3.2 MOS5 main module

## 3.2 MOS5 main module

### 3.2.1 Layer rules

#### NWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1NW	NW_VERIFY overlap of DIFF is not allowed (except rxw2ti)	-	-
B8NW	NW_VERIFY overlap of DTI is not allowed	-	-
W1NW	Minimum NWELL width	0.86	μm
S1NW	Minimum NWELL spacing/notch	0.6	μm
S2NW	Minimum NWELL spacing (different net)	1.4	μm
<b>Note:</b> Valid inside the same TUB			
<b>S4NW</b>	Minimum NWELL spacing (different net)	2.0	μm
	<b>Note:</b> Valid inside the same TUB		
	<b>Note:</b> Valid if one NWELL to PTUB_SUB voltage is less than 1V		
S3NW	Minimum (N WELL AND MV) spacing to N WELL (different net)	2.0	μm
<b>Note:</b> Valid inside the same TUB			
A1NW	Minimum NWELL area	1.0	μm <sup>2</sup>
Q1NW	N WELL should be contacted by NDIFF	-	-

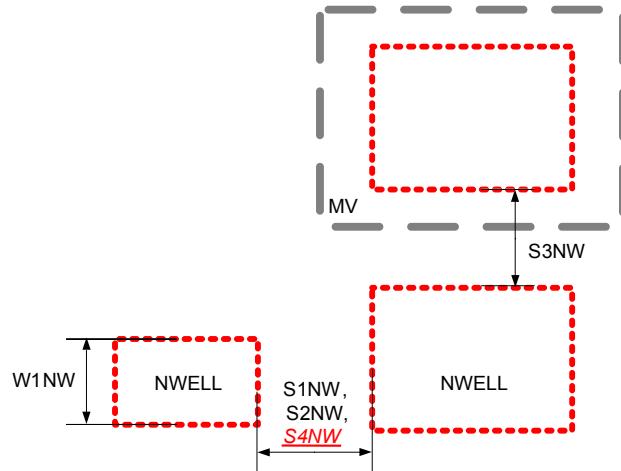


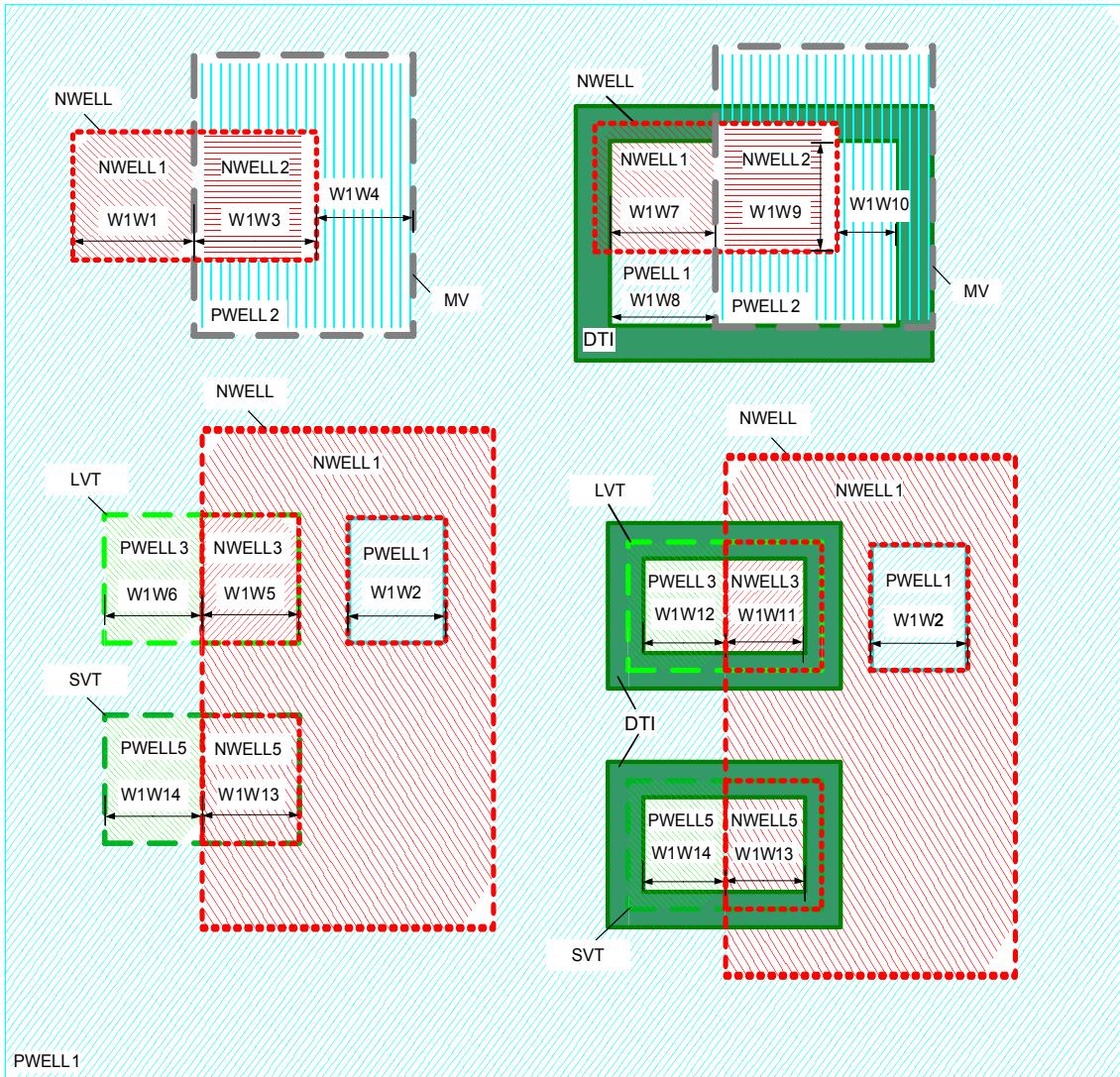
Figure 3.43 NWELL

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → NWELL2, PWELL2

### NWELL2, PWELL2

These rules are related to a combination of design layers (refer to section "2.4 Definitions").

Name	Description	Value	Unit
W1W3	Minimum NWELL2 width	0.86	μm
W1W4	Minimum PWELL2 width	0.6	μm
A1W3	Minimum NWELL2 area	2.25	μm <sup>2</sup>
A1W4	Minimum PWELL2 area	0.8	μm <sup>2</sup>



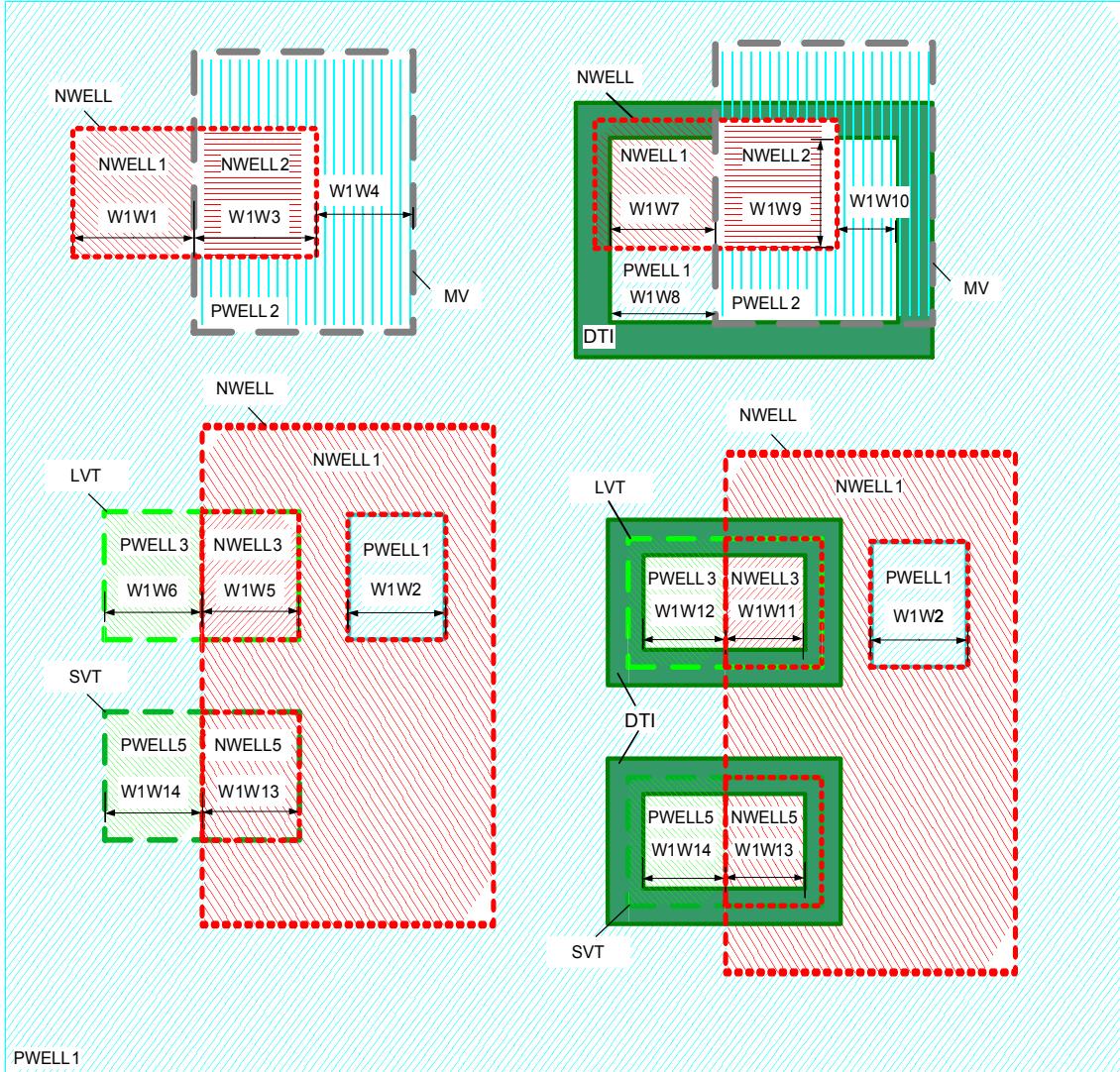
**Figure 3.44 NWELL, PWELL**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → NWELL2\_E, PWELL2\_E

### NWELL2\_E, PWELL2\_E

These rules are related to a combination of design layers (refer to section "2.4 Definitions").

Name	Description	Value	Unit
W1W9	Minimum NWELL2_E width	0.5	μm
W1W10	Minimum PWELL2_E width	0.5	μm



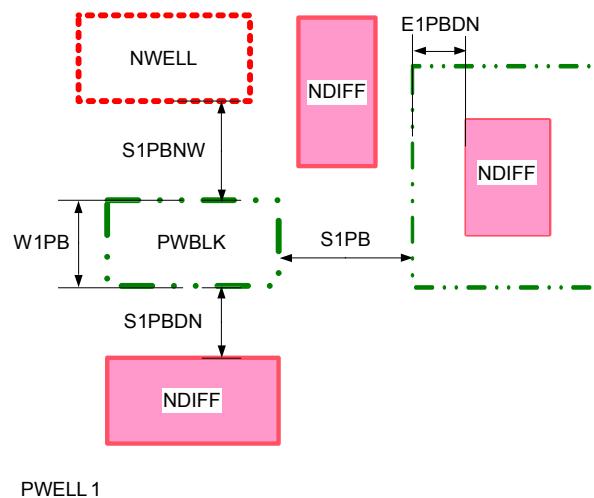
**Figure 3.45 NWELL, PWELL**

3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ PWBLK

## PWBLK

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B2PB	PWBLK overlap of NWELL is not allowed	-	-
B3PB	PWBLK overlap of PIMP is not allowed (except over SJPN, DTI, SJ1XN, SJ1XP, SJ2XP, nisj1_16, dfwdn#, phv#, pmv#, phvr#, dfwdnh#)	-	-
B6PB	Only a single rectangular NDIFF inside PWBLK is allowed (except nhsj1_#, nisj1_16, ndhv#, dfwdn#, nhv#, nhvr#, ndhvr#, dfwdnh#, nmv#, ndmv#, dfwd#, nhsj1a_#, nhsj1b_#, dfwnsj1a_#, dfwnsj1b_#)	-	-
B4PB	ACTIVE crossing PWBLK edge is not allowed (except over SJNP, SJPN, SJ1XN, SJ1XP or SJ2XP, nisj1_16, nhv#, phv#, ndhv#, dfwdn#, pmv#, nhvr#, phvr#, ndhvr#, dfwdnh#, nmv#, ndmv#, dfwd#)	-	-
W1PB	Minimum PWBLK width (except nmvb, pmvb, dfwdnb)	0.6	μm
S1PB	Minimum PWBLK spacing/notch (except nhv#, ndhv#, dfwdn#, pmvd, pmve, pmvf, nhvr#, ndhvr#, dfwdnh#)	0.86	μm
S1PBDN	Minimum PWBLK spacing to NDIFF (except over SJNP, SJ1XN or SJ2XP)	0.12	μm
S1PBNW	Minimum PWBLK spacing to NWELL (except over SJNP, SJPN, SJ1XN, SJ1XP or SJ2XP, phv#, pmv#, nhvr#, phvr#, ndhvr#, dfwdnh#, nmvb, nmvc, dfwdnb, dfwdnc, qnvha)	0.86	μm
E1PBDN	Fixed PWBLK enclosure of NDIFF (except over SJPN, SJ1XN, SJ1XP or SJ2XP, TIEDTUB, nhv#, phv#, ndhv#, dfwdn#, nhvr#, ndhvr#, dfwdnh#, nmv#, ndmv#, dfwd#)	0.12	μm



**Figure 3.46 PWBLK**

## 3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ DIFF

**DIFF**

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
	ACTIVE without NIMP or PIMP is not allowed	-	-
	<b>Note:</b> Not valid for DIFFDUMMY.		
B1DF	<b>Note:</b> except SJNP SJPN, SJ1XN, SJ1XP or SJ2XP region in nhsj1_#, phsj1_#, dfwnsj1_#, nhsj1a_#, nhsj1b_#, phsj1a_#, phsj2b_#, dfwnsj1a_#, dfwnsj1b_#, nisj1_16 NBUF region, dpp6, ds5a, ds5b, dzbt1, rxw2ti, qnv5, qnvha, qpv5, qpvh		
	<b>Note:</b> except SJ2XP with oversizing of 0.29µm in DRAIN PWELL2 region		
BDDF	Not allowed to be used by customers	-	-
	<b>Note:</b> Only valid for DIFF purpose NOBLK. Reserved layer.		
B3DF	ACTIVE crossing NWELL edge is not allowed (except nmva#, pmva#, phv#, nmv#, pmv#, ndmv#, phvr#, dfwd#, dpp6, ds5a, ds5b, rxw2ti, qnv5, qnvha, (SJNP, SJPN, SJ1XN, SJ1XP or SJ2XP region in nhsj1_#, phsj1_#, dfwnsj1_#, nhsj1a_#, phsj1a_#, phsj2b_#, dfwnsj1a_#))	-	-
W1DF	Minimum DIFF width	0.22	µm
W2DF	Minimum length of coincident NDIFF/PDIFF path edge	0.42	µm
S1DF	Minimum DIFF spacing/notch	0.28	µm
S1DFDT	Minimum DIFF spacing to DTI	0.5	µm
S1DNNW	Minimum NDIFF spacing to NWELL (except nmvb, nmvc, dfwdnb, dfwdnc)	0.43	µm
S1DPNW	Minimum PDIFF spacing to NWELL	0.12	µm
S2DF	Minimum NDIFF in NWELL spacing to PDIFF in PWELL	0.36	µm
E1DFHW	Minimum DIFF enclosure of HWC	3.0	µm
E1NWDN	Minimum NWELL enclosure of NDIFF (except DIFFDTI, (SJNP region of nhsj1_# and dfwnsj1_#, SJ1XN region of nhsj1a_# and dfwnsj1a_#, SJ1XN region of nhsj1b_# and dfwnsj1b_#, SJ1XP region of phsj1a_#, SJ2XP region of phsj2b_#))	0.12	µm
E1NWDP	Minimum NWELL enclosure of PDIFF (except TIEDTUB)	0.43	µm
E1DFDT	Minimum DIFF extension beyond DTI	0.5	µm
O1DFDT	Minimum DIFF overlap of DTI	0.5	µm
A1DF	Minimum ACTIVE area	0.202	µm <sup>2</sup>
	<b>Note:</b> DIFF dimension greater than 200 µm x 200 µm must not be used.		
<i>R1DF</i>	Minimum local DIFF density (except SJ1XN, SJ1XP)	15.0	%
	<b>Note:</b> Valid in any 200µm x 200µm window, step size 100µm.		
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
<i>R2DF</i>	Minimum local DIFF density (for SJ1XN, SJ1XP)	5.0	%
	<b>Note:</b> Valid in any 200µm x 200µm window, step size 100µm.		
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
R3DF	Maximum ratio of DIFF (in PWELL1_E) to PWELL1_E area	50.0	%
	<b>Note:</b> Only valid for LP5MOS module.		
	<b>Note:</b> Only valid if PWELL1_E covering TUB completely with PWELL1_E area > 30000 µm <sup>2</sup> .		
	<b>Note:</b> The use of a single large size primitive device with PWELL1_E > 30000µm <sup>2</sup> is not permitted.		
	<b>Note:</b> R3DF violation requires reduction of tub size rather than adding other well types.		

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → DIFF

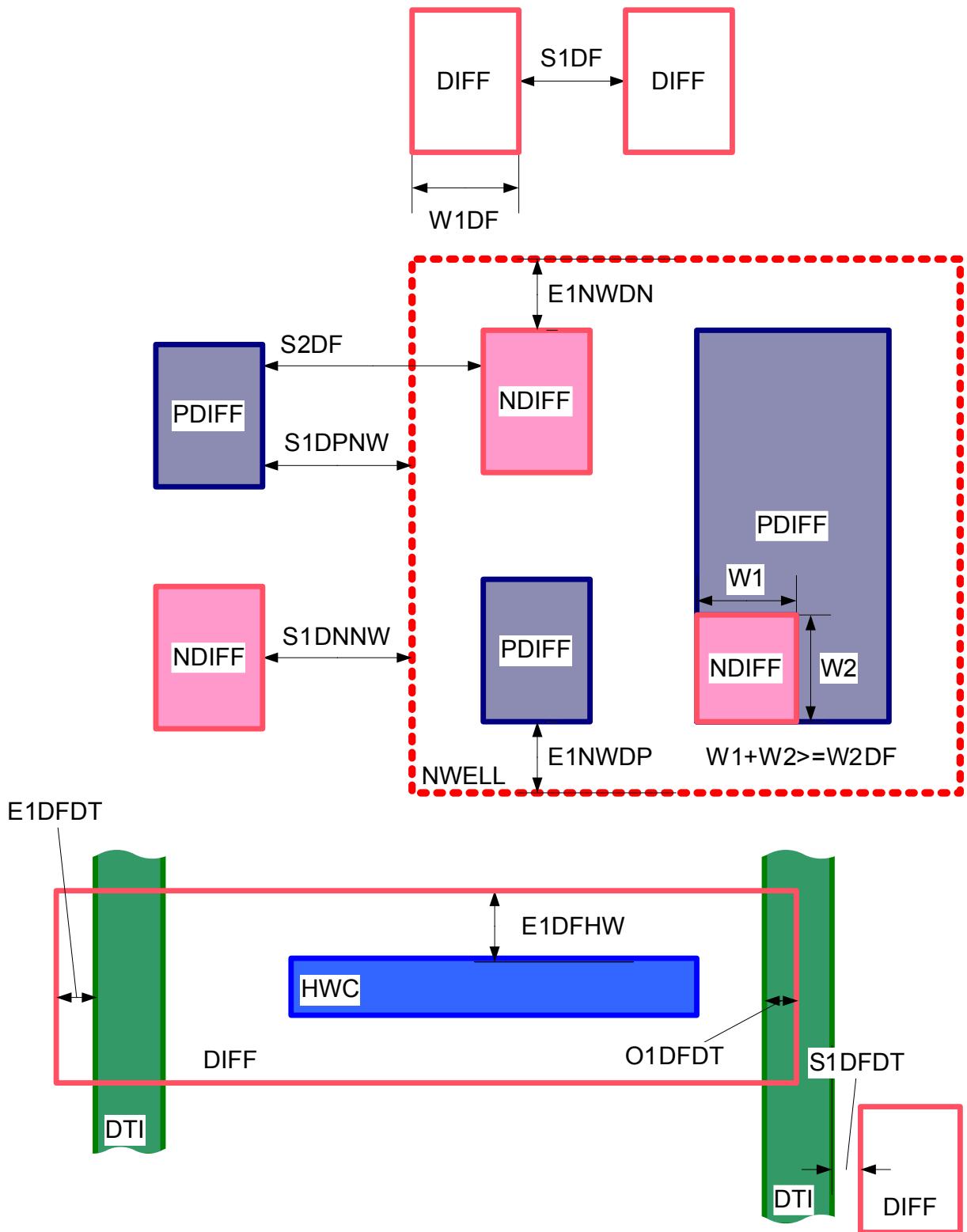


Figure 3.47 DIFF

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → DIFFDUMMY

## DIFFDUMMY

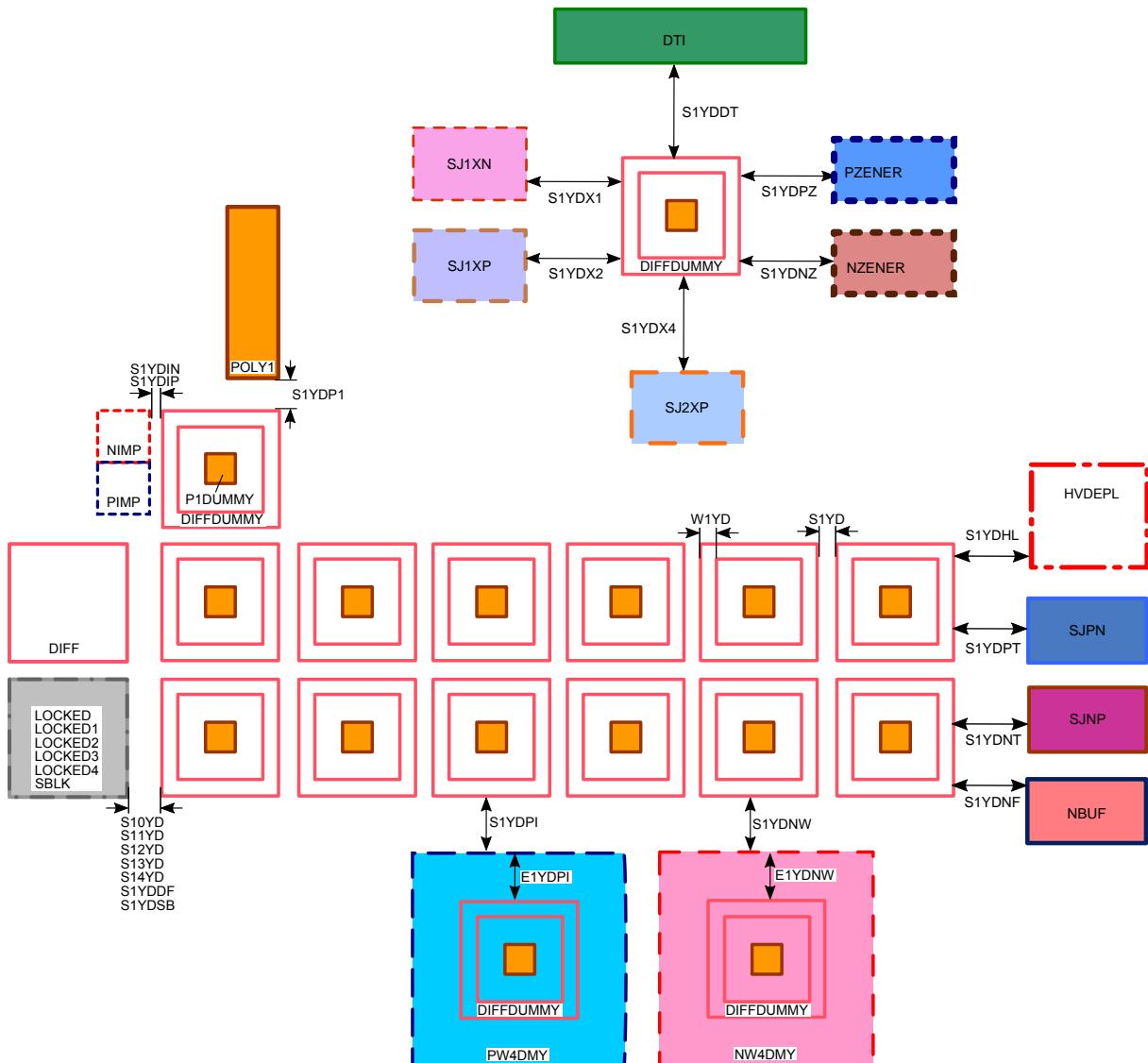
It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B10YD	DIFFDUMMY overlap of NBUF is not allowed	-	-
B11YD	DIFFDUMMY overlap of PZENER is not allowed	-	-
B12YD	DIFFDUMMY overlap of NZENER is not allowed	-	-
B13YD	DIFFDUMMY overlap of SJ1XN is not allowed	-	-
B14YD	DIFFDUMMY overlap of SJ2XP is not allowed	-	-
B15YD	DIFFDUMMY overlap of SJ1XP is not allowed	-	-
B16YD	DIFFDUMMY overlap of HVDEPL is not allowed	-	-
B1YD	DIFFDUMMY overlap of DIFF is not allowed	-	-
B2YD	DIFFDUMMY overlap of NIMP or PIMP is not allowed	-	-
B3YD	DIFFDUMMY overlap of CONT is not allowed	-	-
B5YD	DIFFDUMMY overlap of SBLK is not allowed	-	-
B7YD	DIFFDUMMY overlap of DTI is not allowed	-	-
B8YD	DIFFDUMMY overlap of SJPN is not allowed	-	-
B9YD	DIFFDUMMY overlap of SJNP is not allowed	-	-
W1YD	Minimum DIFFDUMMY width	0.4	μm
S1YD	Minimum DIFFDUMMY spacing/notch	0.5	μm
S10YD	Minimum DIFFDUMMY spacing to LOCKED	3.6	μm
S11YD	Minimum DIFFDUMMY spacing to LOCKED1	3.6	μm
S12YD	Minimum DIFFDUMMY spacing to LOCKED2	3.6	μm
S13YD	Minimum DIFFDUMMY spacing to LOCKED3	3.6	μm
S14YD	Minimum DIFFDUMMY spacing to LOCKED4	3.6	μm
S1YDDF	Minimum DIFFDUMMY spacing to DIFF	3.0	μm
S1YDDT	Minimum DIFFDUMMY spacing to DTI	1.0	μm
S1YDHL	Minimum DIFFDUMMY spacing to HVDEPL	5.0	μm
S1YDIN	Minimum DIFFDUMMY spacing to NIMP	0.3	μm
S1YDIP	Minimum DIFFDUMMY spacing to PIMP	0.3	μm
S1YDNF	Minimum DIFFDUMMY spacing to NBUF	5.0	μm
S1YDNT	Minimum DIFFDUMMY spacing to SJNP	5.0	μm
S1YDNW	Minimum DIFFDUMMY spacing to NW4DMY	5.0	μm
S1YDNZ	Minimum DIFFDUMMY spacing to NZENER	5.0	μm
S1YDP1	Minimum DIFFDUMMY spacing to POLY1	3.0	μm
S1YDPI	Minimum DIFFDUMMY spacing to PW4DMY	5.0	μm
S1YDPT	Minimum DIFFDUMMY spacing to SJPN	5.0	μm
S1YDPZ	Minimum DIFFDUMMY spacing to PZENER	5.0	μm
S1YDSB	Minimum DIFFDUMMY spacing to SBLK	3.0	μm
S1YDX1	Minimum DIFFDUMMY spacing to SJ1XN	5.0	μm
S1YDX2	Minimum DIFFDUMMY spacing to SJ1XP	5.0	μm
S1YDX4	Minimum DIFFDUMMY spacing to SJ2XP	5.0	μm

⇒

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → DIFFDUMMY

Name	Description	Value	Unit
E1YDNW	Minimum NW4DMY enclosure of DIFFDUMMY	5.0	µm
E1YDPI	Minimum PW4DMY enclosure of DIFFDUMMY	5.0	µm
A1YD	Minimum DIFFDUMMY area	1.2	µm <sup>2</sup>



**Figure 3.48** DIFFDUMMY

## 3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ MV

**MV**

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

If the module MOS5 is selected, the layer MV is first generated covering the complete chip area before further layer generation is performed, so the design rules for the MV layer are checked by DRC after MV generation.

Name	Description	Value	Unit
B1MV	ACTIVE crossing MV edge is not allowed <b>Note:</b> Not valid for DIFFDUMMY.	-	-
B2MV	NW_VERIFY crossing MV edge is not allowed	-	-
W1MV	Minimum MV width	0.6	μm
S1MV	Minimum MV spacing/notch	0.86	μm
S1MVDF	Minimum MV spacing to ACTIVE <b>Note:</b> Not valid for DIFFDUMMY.	0.32	μm
S1MVDT	Minimum MV spacing to DTI	0.7	μm
S1MVGA	Minimum MV spacing to GATE	0.4	μm
E1MVDF	Minimum MV enclosure of ACTIVE <b>Note:</b> Not valid for DIFFDUMMY.	0.32	μm
E1MVGA	Minimum MV enclosure of GATE	0.4	μm

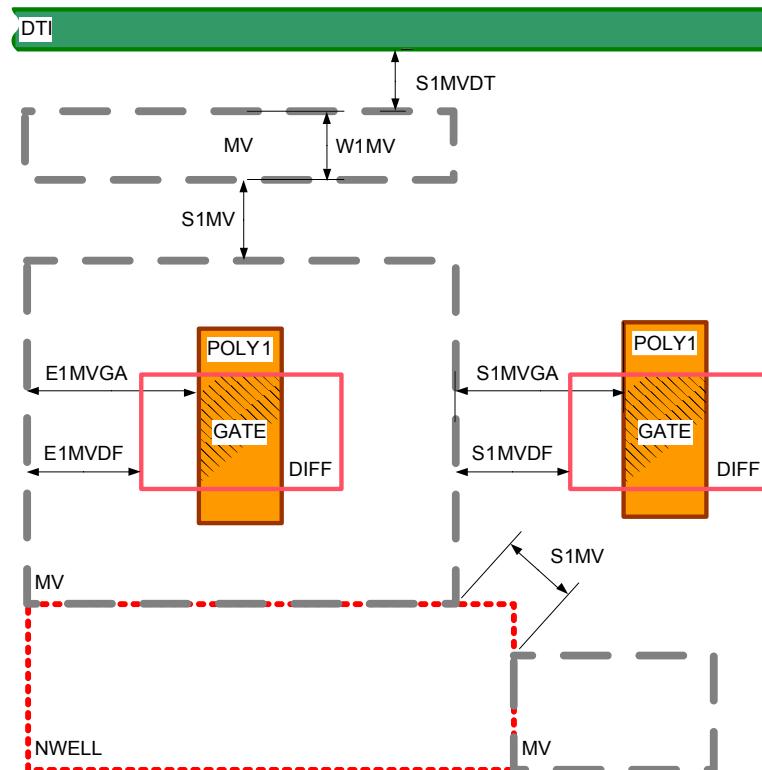


Figure 3.49 MV

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → POLY1

**POLY1**

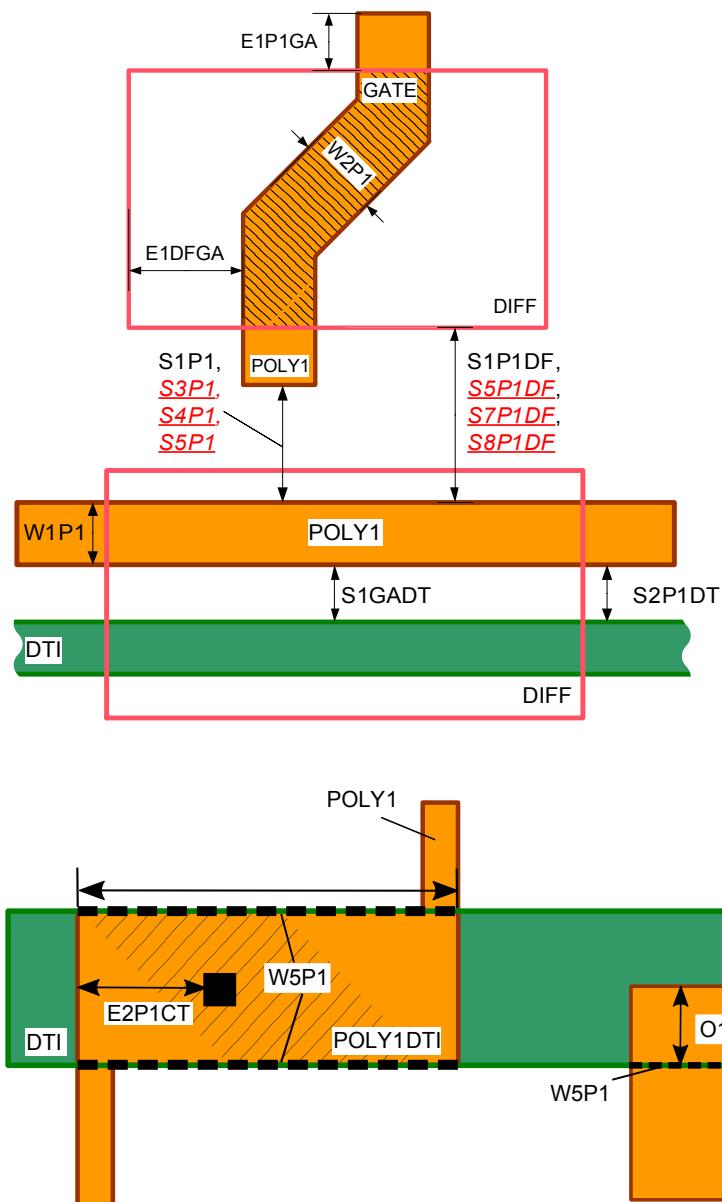
This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B10P1	POLY1 overlap of ISOTUB is not allowed  <b>Note:</b> Valid if the voltage difference of the affected elements (TUBs, POLY1) >100V, however the design rule check is performed without voltage rating considerations.	-	-
B11P1	POLY1DTI must be rectangular	-	-
B1GA	90 degree bent GATE is not allowed  <b>Note:</b> Only valid for POLY1 over DIFF or for DIFF over POLY1 structures with > 4 vertices.	-	-
B1P1	(POLY1 and SBLK and not (HRES or MRES)) without NIMP or PIMP is not allowed  <b>Note:</b> NIMP touching PIMP under (POLY1 and SBLK and not (HRES or MRES)) is not allowed.	-	-
B2GA	Illegal GATE construct  <b>Note:</b> GATE region has been identified as having no association with supported devices.	-	-
B3P1	POLY1 overlap of DIFFDTI is not allowed	-	-
BDP1	Not allowed to be used by customers  <b>Note:</b> Only valid for POLY1 purpose NOBLK. Reserved layer.	-	-
W1P1	Minimum POLY1 width	0.18	μm
W2P1	Minimum POLY1 width (for 45 degree bent GATE)	0.21	μm
W5P1	Minimum length of POLY1DTI edge coinciding with DTI edge (except pmv#, P1_FP)	1.0	μm
S1P1	Minimum POLY1 spacing/notch	0.25	μm
S3P1	Minimum POLY1 spacing (different net, tag_#, difference >25V ≤ 60V)  <b>Note:</b> Valid for spacing of all POLY1 shapes with label tag_## to all POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".	0.5	μm
S4P1	Minimum POLY1 spacing (different net, tag_#, difference >60V ≤100V)  <b>Note:</b> Valid for spacing of all POLY1 shapes with label tag_## to all POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".	0.8	μm
S5P1	Minimum POLY1 spacing (different net, tag_#, difference >100V)  <b>Note:</b> Valid for spacing of all POLY1 shapes with label tag_## to all POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of > 100V. Refer to the design related guideline "Voltage class definitions".	1.3	μm
S1GADT	Minimum GATE spacing to DTI	0.5	μm
S1P1DF	Minimum POLY1 spacing to ACTIVE	0.1	μm
S2P1DT	Minimum POLY1 spacing to DTI	0.08	μm
S5P1DF	Minimum POLY1 spacing to DIFF (different net, tag_#, difference >25V ≤ 60V)  <b>Note:</b> Valid for spacing of all POLY1/DIFF shapes with label tag_## to all DIFF/POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".	0.5	μm
S7P1DF	Minimum POLY1 spacing to DIFF (different net, tag_#, difference >60V ≤100V)  <b>Note:</b> Valid for spacing of all POLY1/DIFF shapes with label tag_## to all DIFF/POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".	0.8	μm
S8P1DF	Minimum POLY1 spacing to DIFF (different net, tag_#, difference >100V)  <b>Note:</b> Valid for spacing of all POLY1/DIFF shapes with label tag_## to all DIFF/POLY1 shapes having other voltage classes and a difference between the numbers of the voltage class names of > 100V. Refer to the design related guideline "Voltage class definitions".	1.3	μm

## 3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ POLY1

Name	Description	Value	Unit
E2P1CT	Minimum POLY1DTI enclosure of CONT (in the direction of POLY1DTI edge inside DTI)	0.44	µm
E1DFGA	Minimum DIFF extension beyond GATE	0.32	µm
E1P1GA	Minimum POLY1 extension beyond GATE (except nmva#, pmva#)	0.22	µm
O1P1DT	Minimum POLY1 overlap of DTI (except ds5a, ds5b)	0.5	µm
A1P1	Minimum POLY1 area	0.118	µm <sup>2</sup>
A2P1	Maximum POLY1 area	10000.0	µm <sup>2</sup>
<i>R1P1</i>	Minimum ratio of POLY1 area to EXTENT area  <b>Note:</b> Not checked with standard DRC, option for check is available.	14.0	%
R2P1	Maximum ratio of POLY1 area to connected GATE area  <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	200.0	-
Q1P1	Resistor terminal net without VLABEL  <b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".	-	-

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → POLY1

**Figure 3.50** POLY1

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → P1DUMMY

## P1DUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B10YP	P1DUMMY overlap of NBUF is not allowed	-	-
B11YP	P1DUMMY overlap of PZENER is not allowed	-	-
B12YP	P1DUMMY overlap of NZENER is not allowed	-	-
B13YP	P1DUMMY overlap of SJ1XN is not allowed	-	-
B14YP	P1DUMMY overlap of SJ2XP is not allowed	-	-
B15YP	P1DUMMY overlap of SJ1XP is not allowed	-	-
B16YP	P1DUMMY overlap of HVDEPL is not allowed	-	-
B1YP	Only rectangular P1DUMMY is allowed	-	-
B2YP	P1DUMMY overlap of POLY1 is not allowed	-	-
B3YP	P1DUMMY overlap of CONT is not allowed	-	-
B4YP	P1DUMMY overlap of DIFF is not allowed	-	-
B5YP	P1DUMMY overlap of SBLK is not allowed	-	-
B6YP	P1DUMMY overlap of MRES or HRES is not allowed	-	-
B7YP	P1DUMMY overlap of DTI is not allowed	-	-
B8YP	P1DUMMY overlap of SJPN is not allowed	-	-
B9YP	P1DUMMY overlap of SJNP is not allowed	-	-
W1YP	Minimum P1DUMMY width	1.0	µm
S1YP	Minimum P1DUMMY spacing	1.0	µm
S10YP	Minimum P1DUMMY spacing to LOCKED	3.6	µm
S11YP	Minimum P1DUMMY spacing to LOCKED1	3.6	µm
S12YP	Minimum P1DUMMY spacing to LOCKED2	3.6	µm
S13YP	Minimum P1DUMMY spacing to LOCKED3	3.6	µm
S14YP	Minimum P1DUMMY spacing to LOCKED4	3.6	µm
S1YPDF	Minimum P1DUMMY spacing to DIFF	3.0	µm
S1YPDT	Minimum P1DUMMY spacing to DTI	1.0	µm
S1YPHL	Minimum P1DUMMY spacing to HVDEPL	5.0	µm
S1YPNF	Minimum P1DUMMY spacing to NBUF	5.0	µm
S1YPNT	Minimum P1DUMMY spacing to SJNP	5.0	µm
S1YPNW	Minimum P1DUMMY spacing to NW4DMY	5.0	µm
S1YPNZ	Minimum P1DUMMY spacing to NZENER	5.0	µm
S1YPP1	Minimum P1DUMMY spacing to POLY1	3.0	µm
S1YPP1	Minimum P1DUMMY spacing to PW4DMY	5.0	µm
S1YPPT	Minimum P1DUMMY spacing to SJPN	5.0	µm
S1YPPZ	Minimum P1DUMMY spacing to PZENER	5.0	µm
S1YPSB	Minimum P1DUMMY spacing to SBLK	3.0	µm
S1YPX1	Minimum P1DUMMY spacing to SJ1XN	5.0	µm
S1YPX2	Minimum P1DUMMY spacing to SJ1XP	5.0	µm
S1YPX4	Minimum P1DUMMY spacing to SJ2XP	5.0	µm



## 3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ P1DUMMY

Name	Description	Value	Unit
S1YPYD	Minimum P1DUMMY spacing to DIFFDUMMY	0.4	μm
E1YPNW	Minimum NW4DMY enclosure of P1DUMMY	5.0	μm
E1YPP1	Minimum PW4DMY enclosure of P1DUMMY	5.0	μm

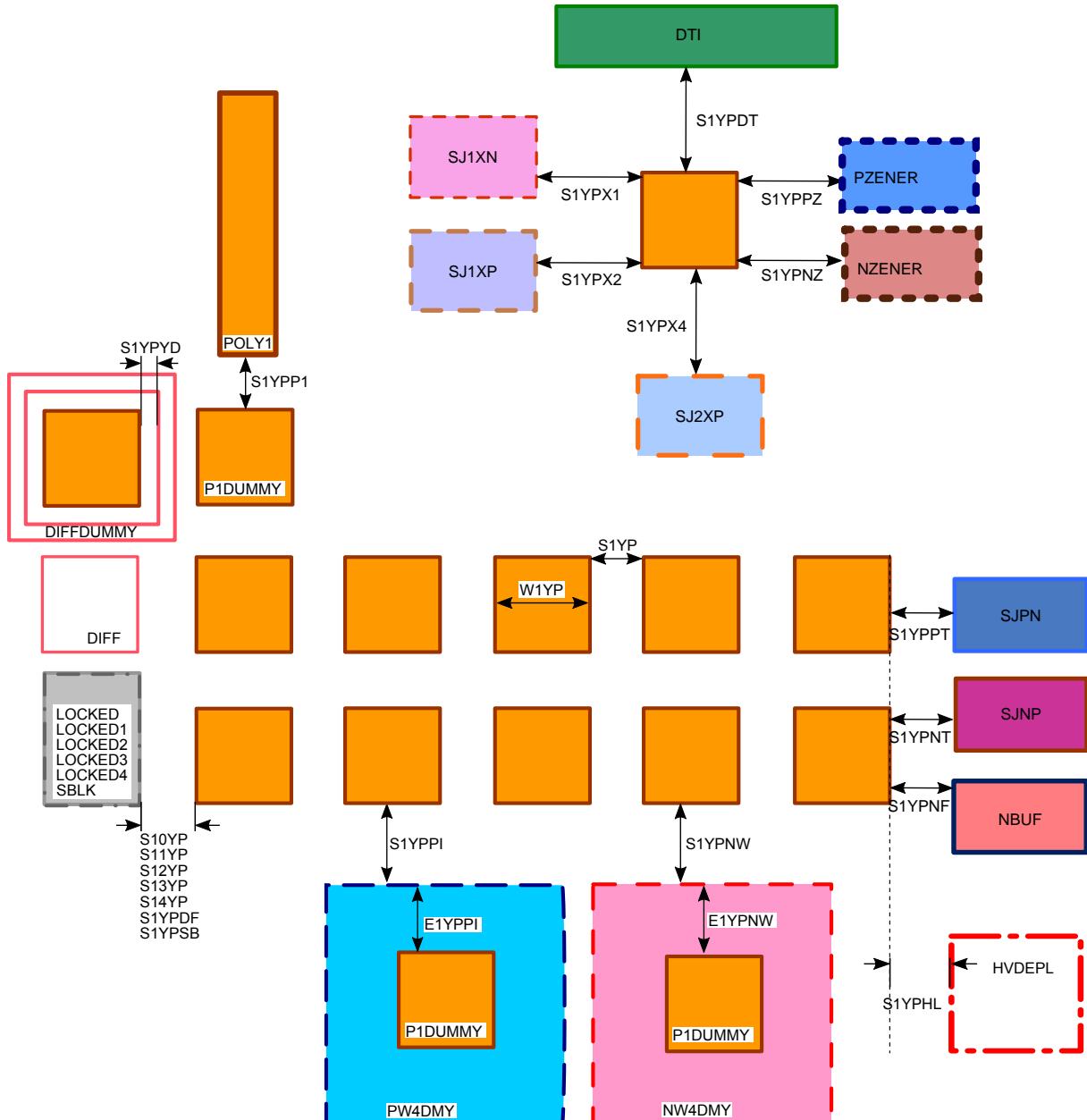


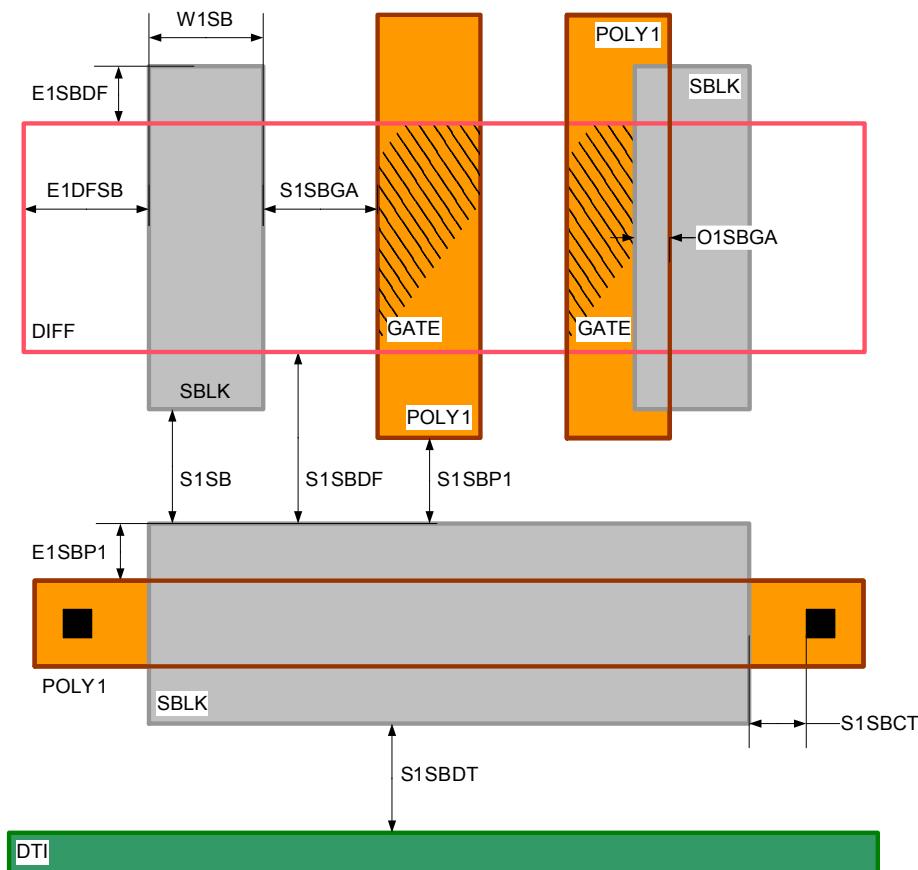
Figure 3.51 P1DUMMY

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → SBLK

## SBLK

SBLK is only allowed for primitive devices.

Name	Description	Value	Unit
W1SB	Minimum SBLK width	0.43	μm
S1SB	Minimum SBLK spacing/notch	0.43	μm
S1SBCT	Minimum SBLK spacing to CONT	0.22	μm
S1SBDF	Minimum SBLK spacing to DIFF (except nmvab, pmvab)	0.22	μm
S1SBDT	Minimum SBLK spacing to DTI	0.25	μm
S1SBGA	Minimum SBLK spacing to GATE (except nmvab, pmvab)	0.45	μm
S1SBP1	Minimum SBLK spacing to POLY1	0.3	μm
E1DFSB	Minimum ACTIVE extension beyond SBLK	0.22	μm
E1SBDF	Minimum SBLK extension beyond ACTIVE	0.22	μm
E1SBP1	Minimum SBLK extension beyond POLY1 (except nmvab, pmvab)	0.22	μm
O1SBGA	Minimum SBLK overlap of GATE	0.05	μm
<b>Note:</b> It is recommended to use SBLK over GATE only for IO blocks and ESD protection.			
A1SB	Minimum SBLK area	2.0	μm <sup>2</sup>



**Figure 3.52 SBLK**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → SALICIDE

## SALICIDE

Name	Description	Value	Unit
B1SA	SALICIDE is only allowed inside TUB between multiple DIFFDTI rings	-	-
B2SA	SALICIDE must connect to DIFFCON	-	-
B3SA	SALICIDE without DIFF is not allowed	-	-
W1SA	Minimum SALICIDE width	0.5	µm
S1SA	Minimum SALICIDE spacing/notch	0.43	µm

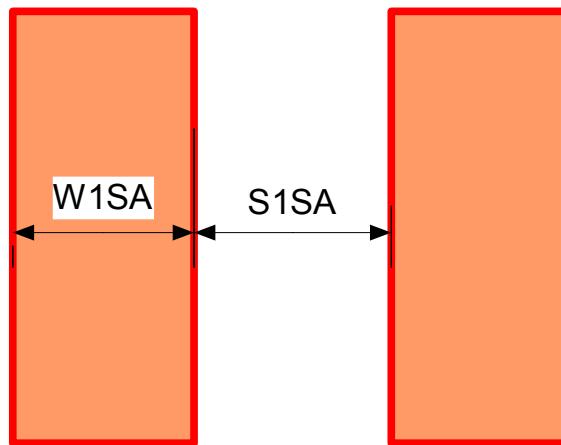


Figure 3.53 SALICIDE

3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ NIMP

## NIMP

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
W1IN	Minimum NIMP width (except phv#)	0.44	μm
S1IN	Minimum NIMP spacing/notch (except nhv#, ndhv#, nmv#, ndmv#)	0.44	μm
S1INDP	Minimum NIMP spacing to PDIFF	0.1	μm
S2INDP	Minimum NIMP spacing to PDIFF (in NWELL) (except phsj1_#, dfwdpa, phsj1a_#)	0.26	μm
S3INDP	Minimum NIMP spacing to PDIFF (if PDIFF to NWELL spacing is <0.43μm)	0.18	μm
E1DNP1	Minimum NDIFF extension beyond POLY1 (except nhvta, nhvtaa, ndhvta, ndhvtaa, nmv#, ndmv# and nisj1_16)	0.32	μm
E1INDF	Minimum NIMP extension beyond ACTIVE (except TIEDTUB, nhsj1_# and dfwdpa)	0.18	μm
E1INDN	Minimum NIMP extension beyond POLY1/NDIFF in direction of POLY1 (except nisj1_16)	0.35	μm
E2INDF	Minimum NIMP extension beyond ACTIVE (in NWELL) (if NWELL enclosure of NDIFF is >=0.43μm )	0.02	μm
O1INDF	Minimum ACTIVE overlap of NIMP	0.23	μm
A1IN	Minimum NIMP area	0.3844	μm <sup>2</sup>

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → NIMP

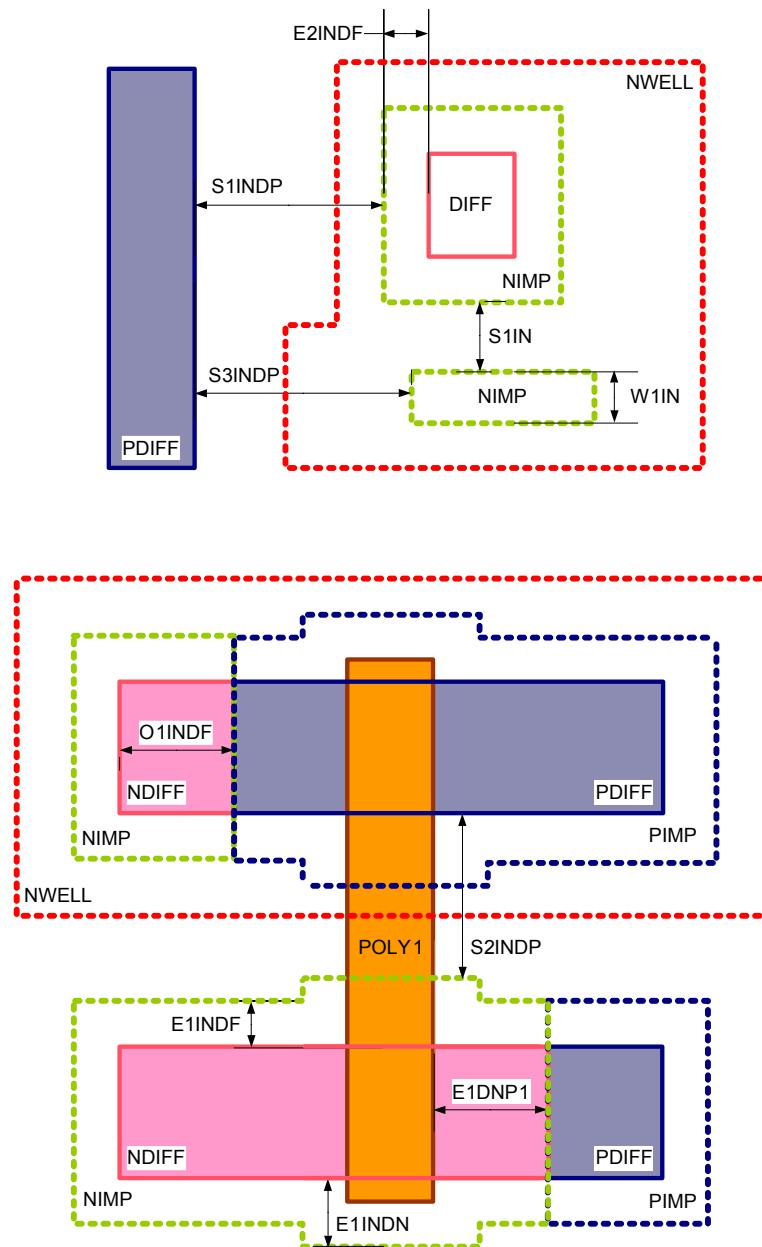


Figure 3.54 NIMP

3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ PIMP

## PIMP

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1IPIN	PIMP overlap of NIMP is not allowed	-	-
W1IP	Minimum PIMP width (except nhv#, ndhv#, nmv#, ndmv#)	0.44	μm
S1IP	Minimum PIMP spacing/notch (except phv#)	0.44	μm
S1IPDN	Minimum PIMP spacing to NDIFF (outside NWELL) (except nhsj1_#, nhsj1a_#, nhsj1b_#)	0.26	μm
S2IPDN	Minimum PIMP spacing to NDIFF (in NWELL) (if NWELL enclosure of NDIFF is >=0.43μm)	0.1	μm
S3IPDN	Minimum PIMP spacing to NDIFF (in NWELL) (if NWELL enclosure of NDIFF is <0.43μm)	0.18	μm
E1DPP1	Minimum PDIFF extension beyond POLY1 (except ds5a, ds5b)	0.32	μm
E1IPDF	Minimum PIMP extension beyond ACTIVE (except TIEDTUB, phsj1_#, dfwdpa, phsj1a_#, phsj2b_#)	0.18	μm
E1IPDP	Minimum PIMP extension beyond POLY1/PDIFF in direction of POLY1	0.35	μm
E2IPDF	Minimum PIMP extension beyond ACTIVE (outside NWELL) (if NWELL spacing to PDIFF is >=0.43μm)	0.02	μm
O1IPDF	Minimum ACTIVE overlap of PIMP	0.23	μm
A1IP	Minimum PIMP area	0.3844	μm <sup>2</sup>

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → PIMP

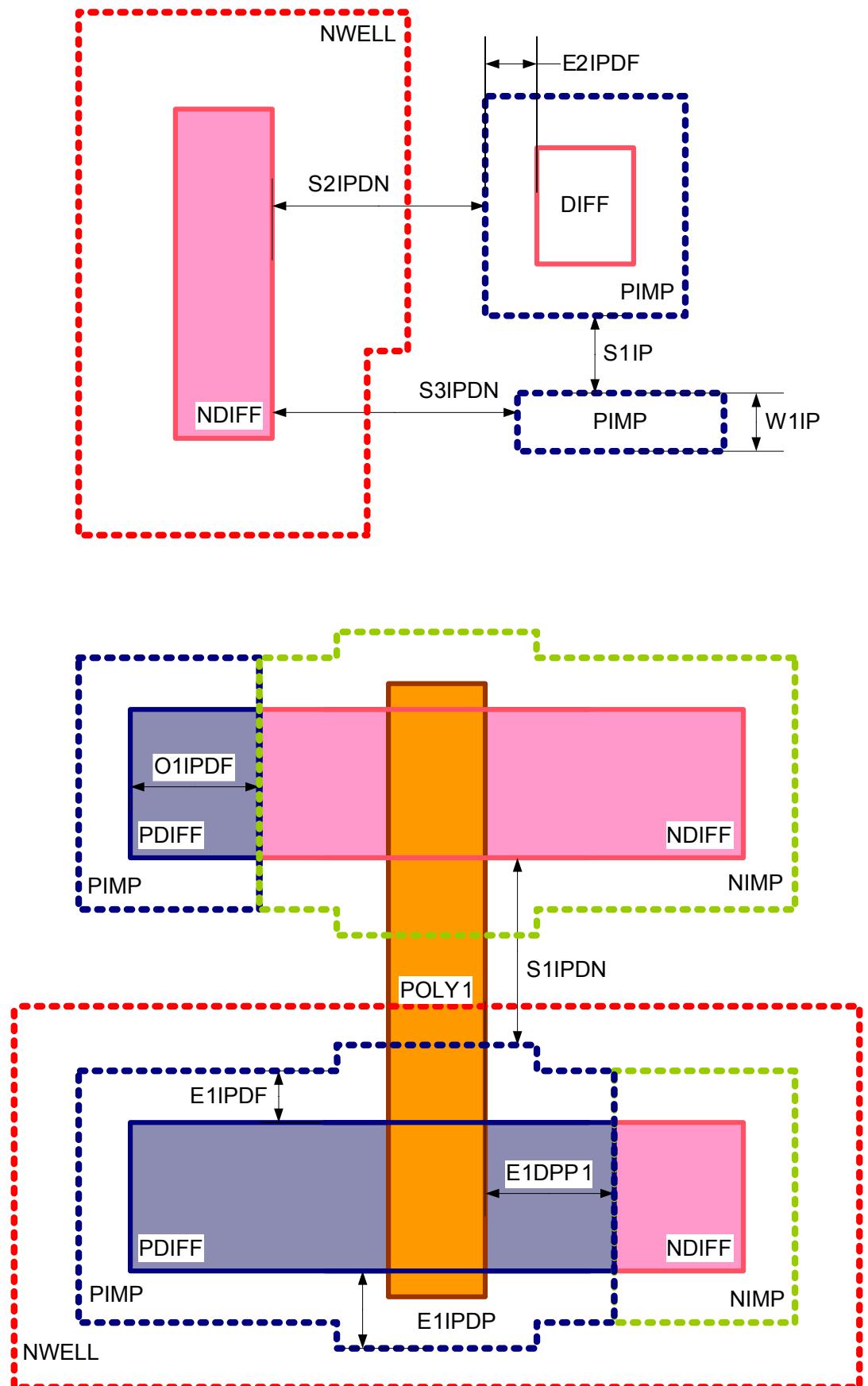


Figure 3.55 PIMP

3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ CONT

## CONT

Name	Description	Value	Unit
B1CT	CONT without NDIFF or PDIFF or POLY1 is not allowed (except ds5a, ds5b)	-	-
B1CTDT	DIFFCON overlap of DTI is not allowed	-	-
B1CTGA	CONT overlap of GATE is not allowed	-	-
B1CTSB	CONT overlap of SBLK is not allowed	-	-
W1CT	Fixed CONT size	0.22 x 0.22	µm x µm
S1CT	Minimum CONT spacing	0.25	µm
S2CT	Minimum CONT spacing (for contact arrays containing more than 4x4 elements)  <b>Note:</b> Two contact regions within 0.3 µm spacing are considered to be in the same array.	0.28	µm
S1CTDF	Minimum CONT spacing to DIFF	0.2	µm
S1CTDT	Minimum DIFFCON spacing to DTI	0.14	µm
S1CTHW	Minimum CONT spacing to HWC	3.5	µm
S1CTP1	Minimum CONT spacing to POLY1	0.16	µm
S2CTDT	Minimum DIFFCON spacing to DTI corner (except TIEDTUB)	0.5	µm
E1DFCT	Minimum DIFF enclosure of CONT	0.1	µm
E1IRCT	Minimum (NIMP or PIMP) enclosure of DIFFCON	0.12	µm
E1P1CT	Minimum POLY1 enclosure of CONT	0.1	µm
R1CT	Maximum ratio of CONT area to connected GATE area	10.0	-

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → CONT

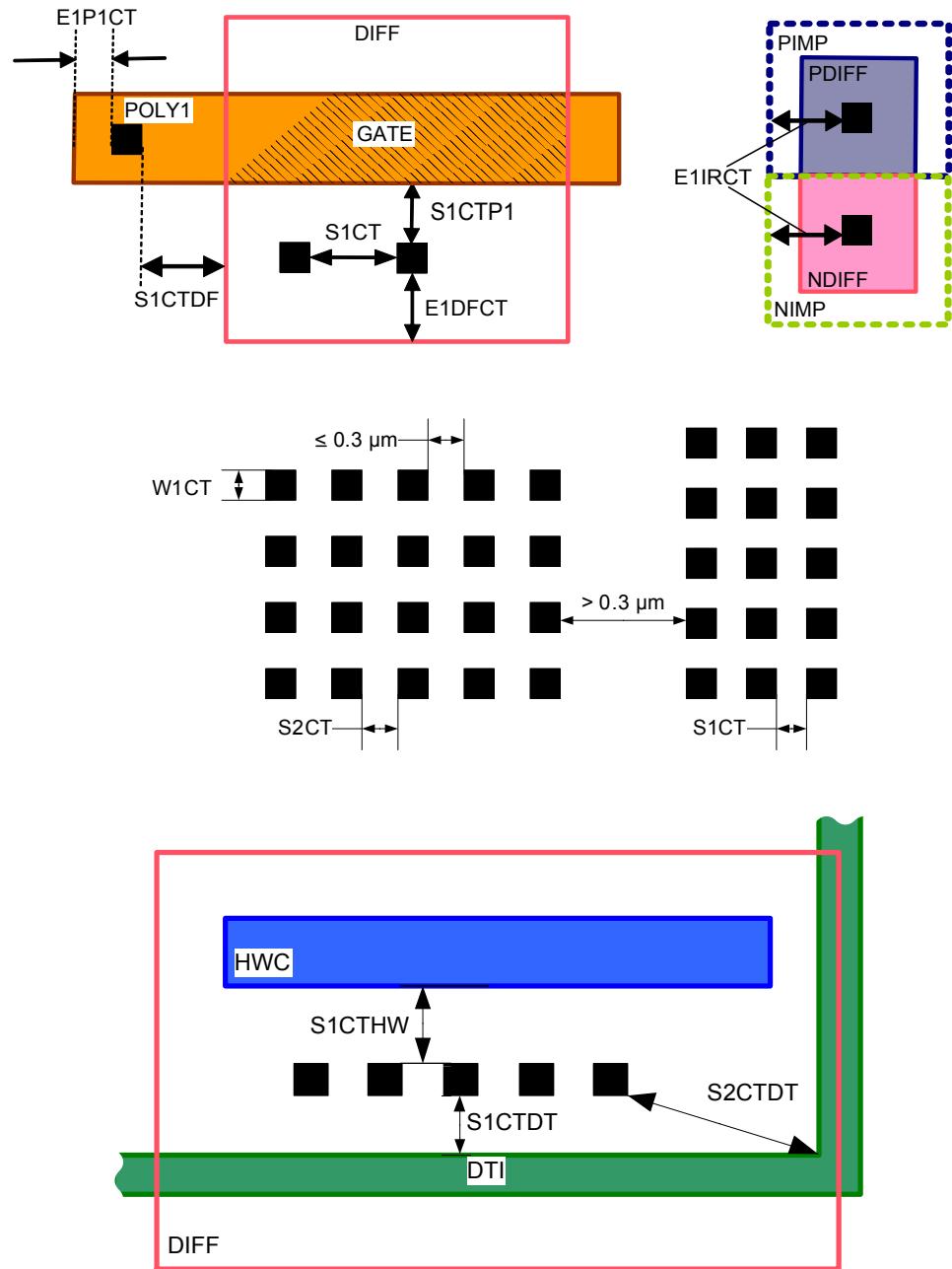


Figure 3.56 CONT

## 3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ MET1

**MET1**

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1CTM1	CONT must be covered by MET1	-	-
B1M1DF	MET1 overlap of ACTIVE is not allowed (different net, tag_#, ACTIVE, MET1 difference >300V)	-	-
B1M1P1	MET1 overlap of POLY1 is not allowed (different net, tag_#, POLY1, MET1 difference >200V)	-	-
W1M1	Minimum MET1 width	0.23	μm
<u>W4M1</u>	Minimum MET1 width joining wide MET1 track (> 35 μm)	10.0	μm
	<b>Note:</b> No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 μm from the main track prior to narrowing.		
<u>W5M1</u>	Maximum MET1 region size	17.0 x 17.0	μm x μm
	<b>Note:</b> MET1 regions are defined as MET1 shapes (single MET1 shapes or a bundle of MET1 shapes, with width > 2.0μm, inclusive of the spacing if the spacing is <= 1.0μm) without any other metal layer above. For further information and design guidelines, please refer to the application note about <a href="#">IMD popping</a> on "my X-FAB".		
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
S1M1	Minimum MET1 spacing/notch	0.23	μm
S4M1	Minimum MET1 spacing (different net, tag_#, difference >25V ≤ 60V)	0.38	μm
	<b>Note:</b> Except nhvta/ndhvta DRAIN MET1 to GATE MET1		
	<b>Note:</b> Valid for spacing of all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".		
S5M1	Minimum MET1 spacing (different net, tag_#, difference >60V ≤100V)	0.6	μm
	<b>Note:</b> Valid for spacing of all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Minimum MET1 spacing (different net, tag_#, difference >100V ≤200V)	0.8	μm
S6M1	<b>Note:</b> Valid for spacing to all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >100V ≤ 200V. Refer to the design related guideline "Voltage class definitions".		
	Minimum MET1 spacing (different net, tag_#, difference >200V ≤300V)	1.2	μm
	<b>Note:</b> Valid for spacing to all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤ 300V. Refer to the design related guideline "Voltage class definitions".		
S9M1	Minimum MET1 spacing (different net, tag_#, difference >300V)	1.6	μm
	<b>Note:</b> Valid for spacing to all MET1 shapes with label tag_# to all MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Minimum MET1 spacing to ACTIVE (different net, tag_#, difference >300V)		
S1M1DF	<b>Note:</b> Valid for spacing of all MET1/ACTIVE shapes with label tag_# to all ACTIVE/MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Valid if the voltage difference between ACTIVE, MET1 is >300V.		
	Minimum MET1 spacing to WIDE_MET1	0.6	μm
S2M1P1	Minimum MET1 spacing to POLY1 (different net, tag_#, difference >200V ≤300V)	1.2	μm
	<b>Note:</b> Valid if MET1 to POLY1 voltage is >200V ≤300V.		
	<b>Note:</b> Valid for spacing of all MET1/POLY1 shapes with label tag_# to all POLY1/MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤300V. Refer to the design related guideline "Voltage class definitions".		

## 3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ MET1

Name	Description	Value	Unit
S3M1P1	Minimum MET1 spacing to POLY1 (different net, tag #, difference >300V)	1.6	µm
<b>Note:</b> Valid if MET1 to POLY1 voltage is >300V.			
<b>Note:</b> Valid for spacing of all MET1/POLY1 shapes with label tag # to all POLY1/MET1 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".			
E1M1CT	Minimum MET1 enclosure of CONT	0.005	µm
E2M1CT	Minimum MET1 enclosure of CONT (in one direction of CONT corner)	0.06	µm
A1M1	Minimum MET1 area	0.202	µm <sup>2</sup>
<i>R1M1</i>	Minimum ratio of MET1 area to EXTENT area	30.0	%
<b>Note:</b> Not checked with standard DRC, option for check is available.			
<i>R2M1</i>	Maximum ratio of MET1 area to EXTENT area	65.0	%
<b>Note:</b> Not checked with standard DRC, option for check is available.			
R1M1P1	Maximum ratio of MET1 area to connected GATE area	400.0	-
<b>Note:</b> Refer to section "Antenna Rule definitions" as well.			
R2M1P1	Maximum ratio of MET1 area to connected GATE area	400.0	-
<b>Note:</b> Refer to section "Antenna Rule definitions" as well.			
Q1M1	Resistor terminal net without VLABEL	-	-
<b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".			

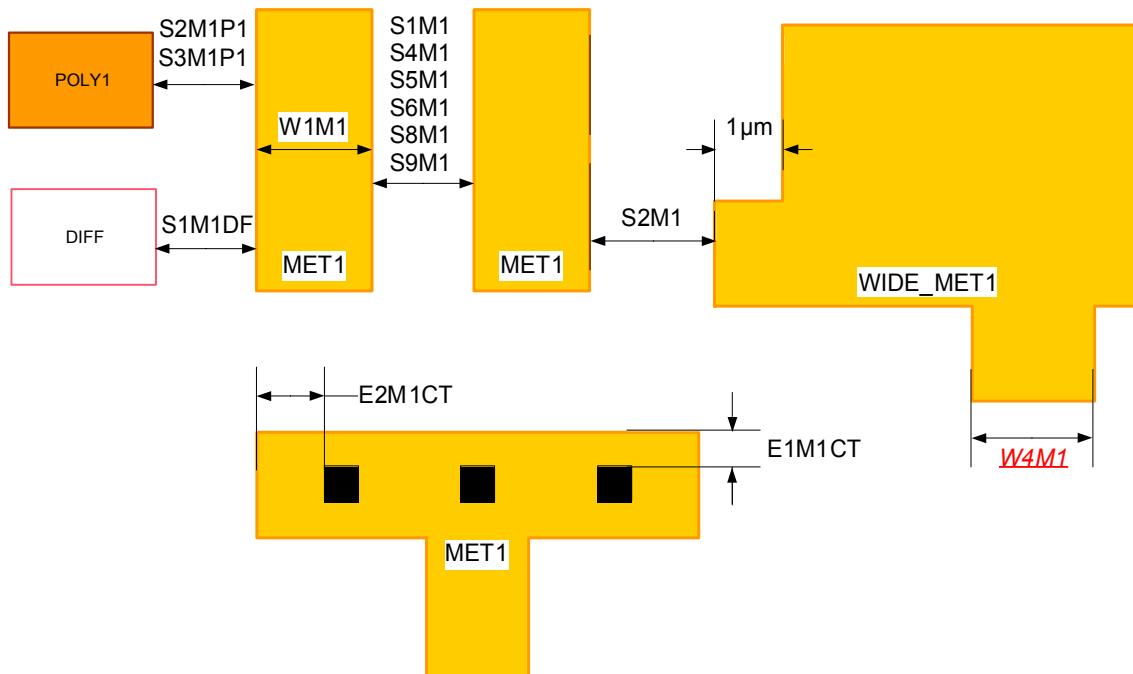


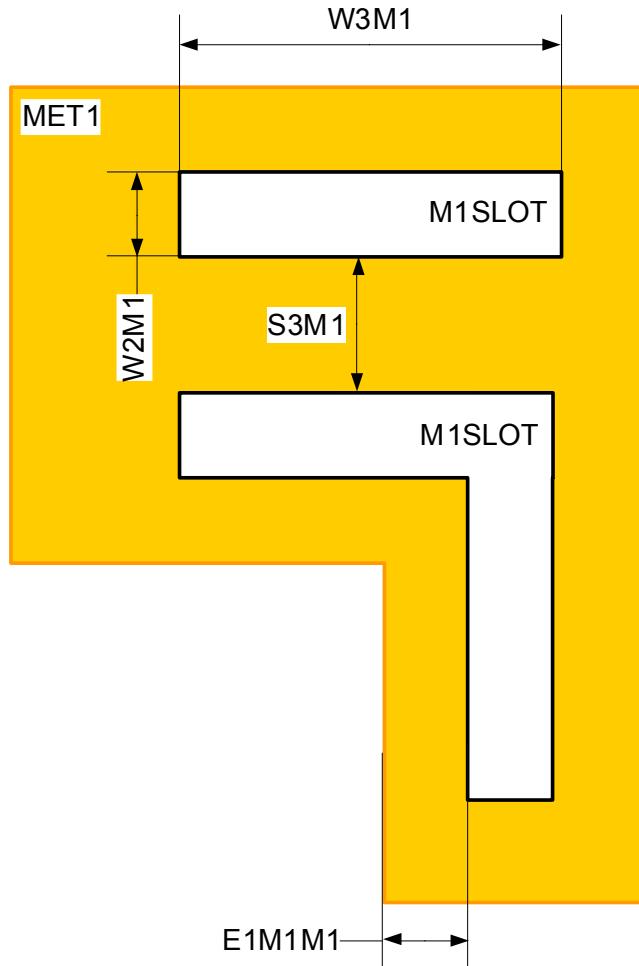
Figure 3.57 MET1

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → M1SLOT

## M1SLOT

Name	Description	Value	Unit
B1M1	All MET1 tracks > 35µm wide to be slotted (except Pads)	-	-
W2M1	Minimum M1SLOT width	0.6	µm
W3M1	Minimum M1SLOT length	20.0	µm
S3M1	Note: If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
E1M1M1	Minimum MET1 enclosure of M1SLOT Note: M1SLOT without MET1 is not allowed.	10.0	µm

**Note:** Insert M1SLOTS in direction of current flow.



**Figure 3.58 M1SLOT**

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → M1DUMMY

**M1DUMMY**

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y1	Only rectangular M1DUMMY is allowed	-	-
B2Y1	M1DUMMY overlap of MET1 is not allowed	-	-
B3Y1	M1DUMMY overlap of CONT or VIA1 is not allowed	-	-
B4Y1	M1DUMMY overlap of HRES is not allowed	-	-
B5Y1	M1DUMMY overlap of DTI is not allowed	-	-
W1Y1	Minimum M1DUMMY width	2.0	μm
W2Y1	Maximum M1DUMMY edge length	20.0	μm
S1Y1	Minimum M1DUMMY spacing	2.0	μm
S10Y1	Minimum M1DUMMY spacing to LOCKED	4.0	μm
S11Y1	Minimum M1DUMMY spacing to LOCKED1	4.0	μm
S12Y1	Minimum M1DUMMY spacing to LOCKED2	4.0	μm
S13Y1	Minimum M1DUMMY spacing to LOCKED3	4.0	μm
S14Y1	Minimum M1DUMMY spacing to LOCKED4	4.0	μm
S1Y1DT	Minimum M1DUMMY spacing to DTI	0.5	μm
S1Y1HR	Minimum M1DUMMY spacing to HRES	5.0	μm
S1Y1M1	Minimum M1DUMMY spacing to MET1	4.0	μm

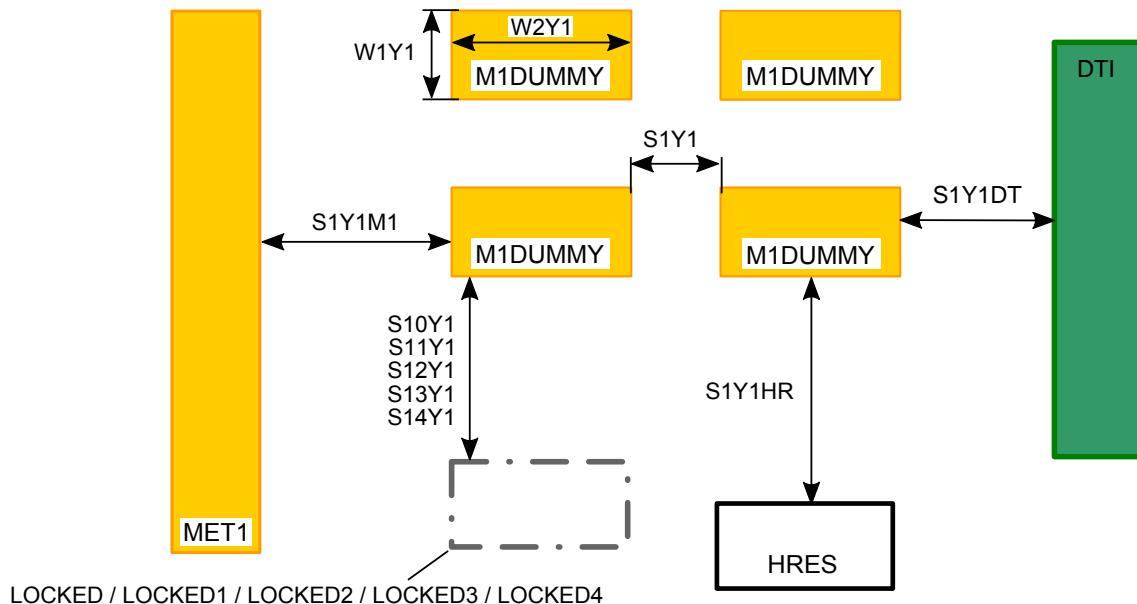


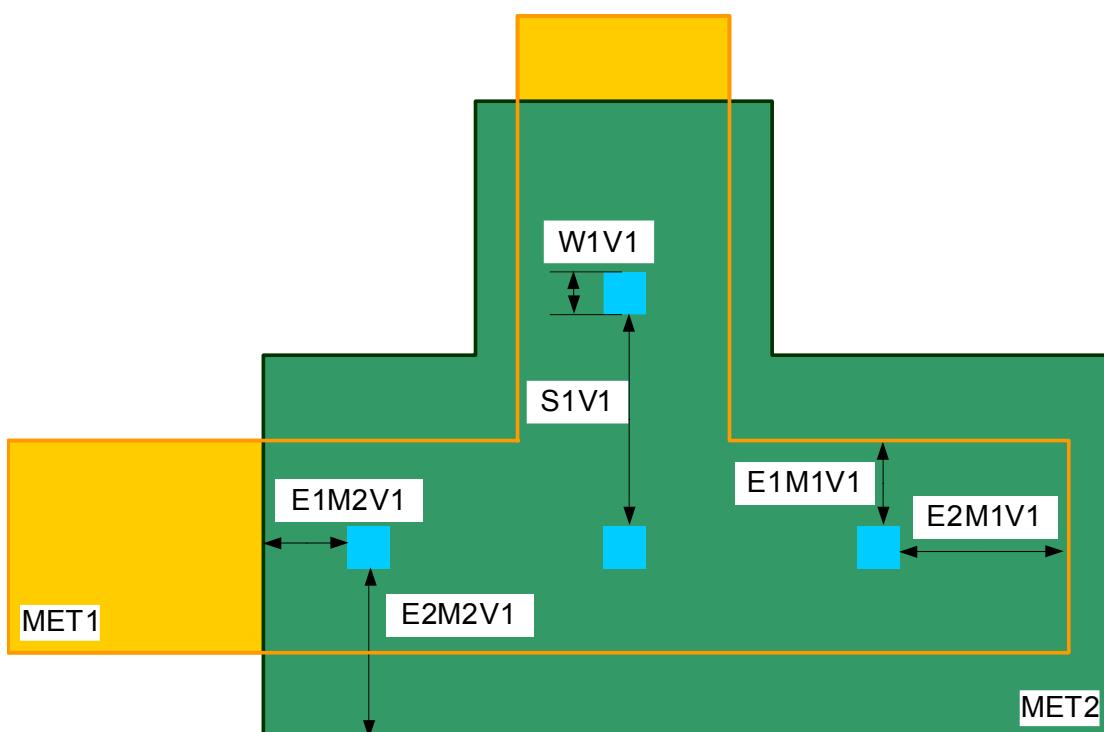
Figure 3.59 M1DUMMY

3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ VIA1

### VIA1

Name	Description	Value	Unit
B1V1	VIA1 must be covered by MET1 and MET2	-	-
W1V1	Fixed VIA1 size	0.26 x 0.26	μm x μm
S1V1	Minimum VIA1 spacing	0.26	μm
E1M1V1	Minimum MET1 enclosure of VIA1	0.01	μm
E1M2V1	Minimum MET2 enclosure of VIA1	0.01	μm
E2M1V1	Minimum MET1 enclosure of VIA1 (in one direction of VIA1 corner)	0.06	μm
E2M2V1	Minimum MET2 enclosure of VIA1 (in one direction of VIA1 corner)	0.06	μm
R1V1	Maximum ratio of VIA1 area to connected GATE area	20.0	-

**Note:** Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".



**Figure 3.60 VIA1**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → MET2

## MET2

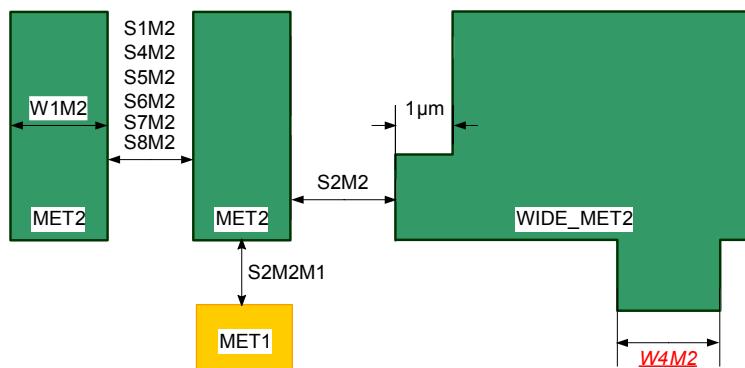
This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1M2M1	MET2 overlap of MET1 is not allowed (different net, tag_#, MET1, MET2 difference >300V)	-	-
W1M2	Minimum MET2 width	0.28	μm
<i>W4M2</i>	Minimum MET2 width joining wide MET2 track (> 35 μm)	10.0	μm
<i>W4M2</i>	<b>Note:</b> No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 μm from the main track prior to narrowing.		
<i>W5M2</i>	Maximum MET2 region size	17.0 x 17.0	μm x μm
<i>W5M2</i>	<b>Note:</b> MET2 regions are defined as MET2 shapes (single MET2 shapes or a bundle of MET2 shapes, with width > 2.0μm, inclusive of the spacing if the spacing is <= 1.0μm) without any other metal layer above. For further information and design guidelines, please refer to the application note about <a href="#">IMD popping</a> on "my X-FAB".		
<i>W5M2</i>	<b>Note:</b> Not checked with standard DRC, option for check is available.		
S1M2	Minimum MET2 spacing/notch	0.28	μm
<i>S4M2</i>	Minimum MET2 spacing (different net, tag_#, difference >25V ≤ 60V)	0.4	μm
<i>S4M2</i>	<b>Note:</b> Valid for spacing of all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".		
<i>S5M2</i>	Minimum MET2 spacing (different net, tag_#, difference >60V ≤100V)	0.6	μm
<i>S5M2</i>	<b>Note:</b> Valid for spacing of all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".		
<i>S6M2</i>	Minimum MET2 spacing (different net, tag_#, difference >100V ≤200V)	0.8	μm
<i>S6M2</i>	<b>Note:</b> Valid for spacing to all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >100V ≤ 200V. Refer to the design related guideline "Voltage class definitions".		
<i>S7M2</i>	Minimum MET2 spacing (different net, tag_#, difference >200V ≤300V)	1.2	μm
<i>S7M2</i>	<b>Note:</b> Valid for spacing to all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤ 300V. Refer to the design related guideline "Voltage class definitions".		
<i>S8M2</i>	Minimum MET2 spacing (different net, tag_#, difference >300V)	1.6	μm
<i>S8M2</i>	<b>Note:</b> Valid for spacing to all MET2 shapes with label tag_# to all MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
S2M2	Minimum MET2 spacing to WIDE_MET2	0.6	μm
<i>S2M2M1</i>	Minimum MET2 spacing to MET1 (different net, tag_#, difference >300V)	1.6	μm
<i>S2M2M1</i>	<b>Note:</b> Valid if the voltage difference between MET1, MET2 voltage is >300V.		
<i>S2M2M1</i>	<b>Note:</b> Valid for spacing of all MET2/MET1 shapes with label tag_# to all MET1/MET2 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
A1M2	Minimum MET2 area	0.202	μm <sup>2</sup>
<i>R1M2</i>	Minimum ratio of MET2 area to EXTENT area	30.0	%
<i>R1M2</i>	<b>Note:</b> Not checked with standard DRC, option for check is available.		
<i>R2M2</i>	Maximum ratio of MET2 area to EXTENT area	65.0	%
<i>R2M2</i>	<b>Note:</b> Not checked with standard DRC, option for check is available.		
<i>R1M2P1</i>	Maximum ratio of MET2 area to connected GATE area	400.0	-
<i>R1M2P1</i>	<b>Note:</b> Refer to section "Antenna Rule definitions" as well.		



## 3. Layer and Device rules → 3.2 MOS5 main module→ 3.2.1 Layer rules→ MET2

Name	Description	Value	Unit
R2M2P1	Maximum ratio of MET2 area to connected GATE area <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	400.0	-
Q1M2	Resistor terminal net without VLABEL <b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".	-	-

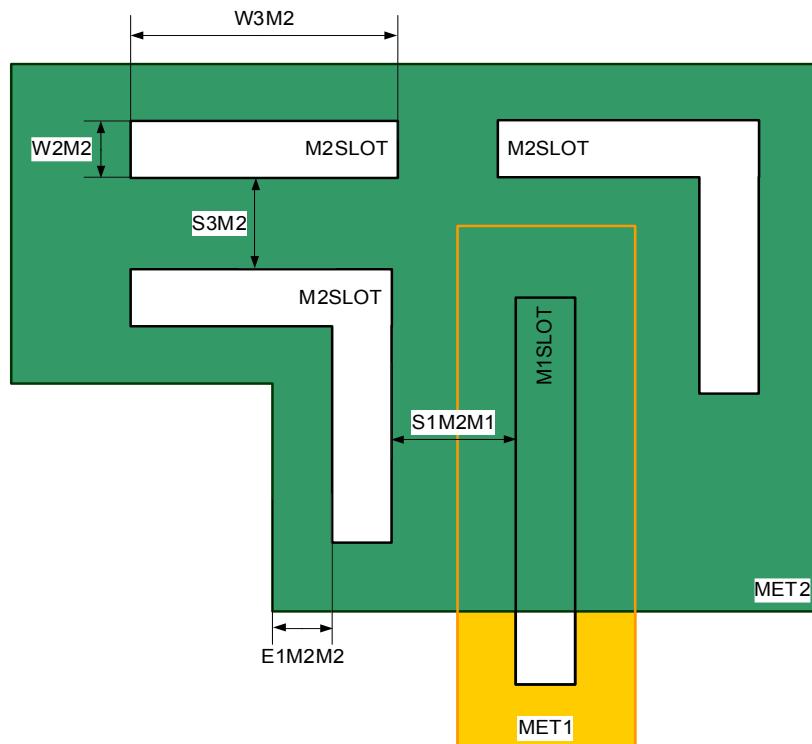
**Figure 3.61** MET2

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → M2SLOT

## M2SLOT

Name	Description	Value	Unit
B1M2	All MET2 tracks > 35µm wide to be slotted (except Pads)	-	-
W2M2	Minimum M2SLOT width	0.6	µm
W3M2	Minimum M2SLOT length	20.0	µm
	<b>Note:</b> If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M2	Minimum M2SLOT spacing/notch	10.0	µm
S1M2M1	Minimum M2SLOT spacing to M1SLOT	2.0	µm
	<b>Note:</b> M2SLOT is not allowed over M1SLOT.		
E1M2M2	Minimum MET2 enclosure of M2SLOT	10.0	µm
	<b>Note:</b> M2SLOT without MET2 is not allowed		

**Note:** Insert M2SLOTS in direction of current flow.



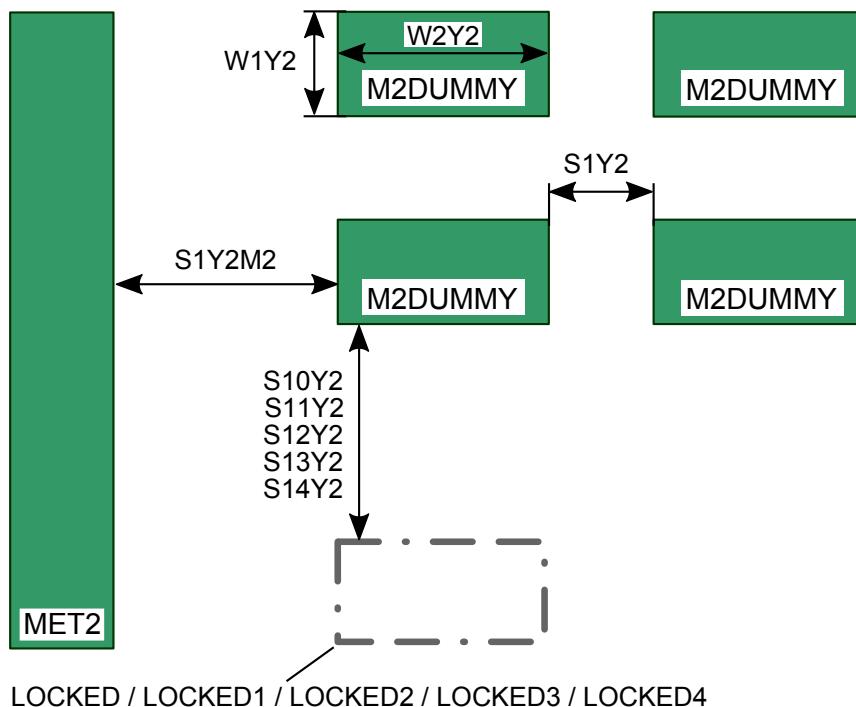
**Figure 3.62** M2SLOT

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → M2DUMMY

**M2DUMMY**

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y2	Only rectangular M2DUMMY is allowed	-	-
B2Y2	M2DUMMY overlap of MET2 is not allowed	-	-
B3Y2V1	M2DUMMY overlap of VIA1 is not allowed	-	-
B3Y2V2	M2DUMMY overlap of VIA2 is not allowed	-	-
B3Y2VT	M2DUMMY overlap of VIATP is not allowed	-	-
<b>Note:</b> Only valid if module MET3 is not selected.			
W1Y2	Minimum M2DUMMY width	2.0	μm
W2Y2	Maximum M2DUMMY edge length	20.0	μm
S1Y2	Minimum M2DUMMY spacing	2.0	μm
S10Y2	Minimum M2DUMMY spacing to LOCKED	4.0	μm
S11Y2	Minimum M2DUMMY spacing to LOCKED1	4.0	μm
S12Y2	Minimum M2DUMMY spacing to LOCKED2	4.0	μm
S13Y2	Minimum M2DUMMY spacing to LOCKED3	4.0	μm
S14Y2	Minimum M2DUMMY spacing to LOCKED4	4.0	μm
S1Y2M2	Minimum M2DUMMY spacing to MET2	4.0	μm

**Figure 3.63 M2DUMMY****LOCKED, LOCKED1, LOCKED2**

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED\* layers are part of the X-FAB provided IP LEF file.

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.1 Layer rules → LOCKED, LOCKED1, LOC...

Name	Description	Value	Unit
BDLOCK	Any structure over LOCKED (ALL) or LOCKED (boundary) is not allowed	-	-
B1LOCK	Any structure over LOCKED (LOCKED1) or LOCKED1 (boundary) is not allowed  <b>Note:</b> Except: - METTPL if (MET4 and METMID) modules are selected or MET5 module is selected - METTP if MET5 module is selected - METCOP	-	-
B2LOCK	Any structure over LOCKED (LOCKED2) or LOCKED2 (boundary) is not allowed  <b>Note:</b> Except: - METTPL if (MET3 and METMID) modules are selected or MET4 module is selected - METTP if MET4 module is selected - MET5 - METCOP	-	-

## LOCKED3

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED\* layers are part of the X-FAB provided IP LEF file.

Name	Description	Value	Unit
B3LOCK	Any structure over LOCKED3 is not allowed  <b>Note:</b> Except: - METTPL if METMID module is selected or MET3 module is selected - METTP if MET3 module is selected - MET5 - MET4 - METCOP	-	-

## LOCKED4

This layer protects the IP core against routing (of specific layers) and is used to increase the safety of designs during IP replacement. LOCKED\* layers are part of the X-FAB provided IP LEF file.

Name	Description	Value	Unit
B4LOCK	Any structure over LOCKED4 is not allowed  <b>Note:</b> Except: - METTPL, METTP, MET5, MET4, MET3, METCOP	-	-

## CAPDEF

This layer is only used to define certain capacitors.

## DIODEF

This layer is used to define diodes that are to be extracted into the netlist. All diodes without DIODEF are extracted as parasitic components. DIODEF must encompass the entire P/N junction forming the diode.

## XFLAY

This layer is a reserved layer.

Name	Description	Value	Unit
BDXF	Not allowed to be used by customers	-	-

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → ne5, pe5

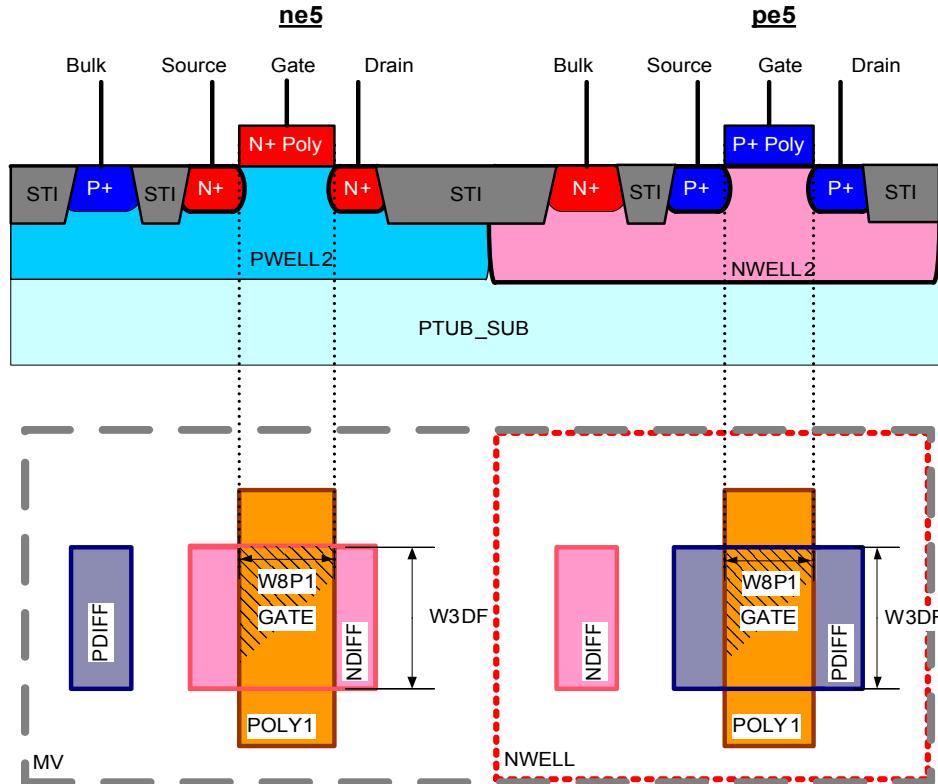
### 3.2.2 Device rules

#### ne5, pe5

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.		
W8P1	Minimum GATE length	0.5	μm

**Note:** MV is necessary for ne5 and pe5

**Note:** For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.



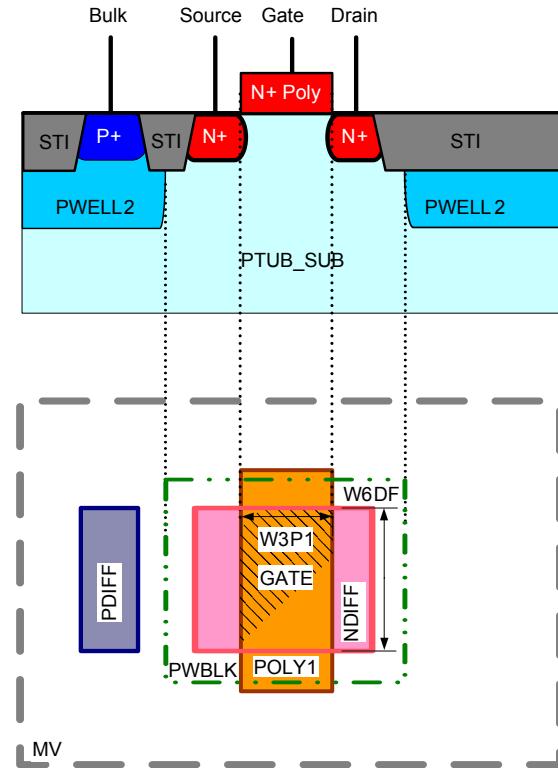
**Figure 3.64** ne5,pe5

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → nn5

### nn5

Name	Description	Value	Unit
B3GA	Only rectangular GATE inside PWBLK is allowed	-	-
W3P1	Minimum GATE length	1.0	μm
W6DF	Minimum GATE width	1.0	μm

**Note:** MV is necessary for nn5



**Figure 3.65 nn5**

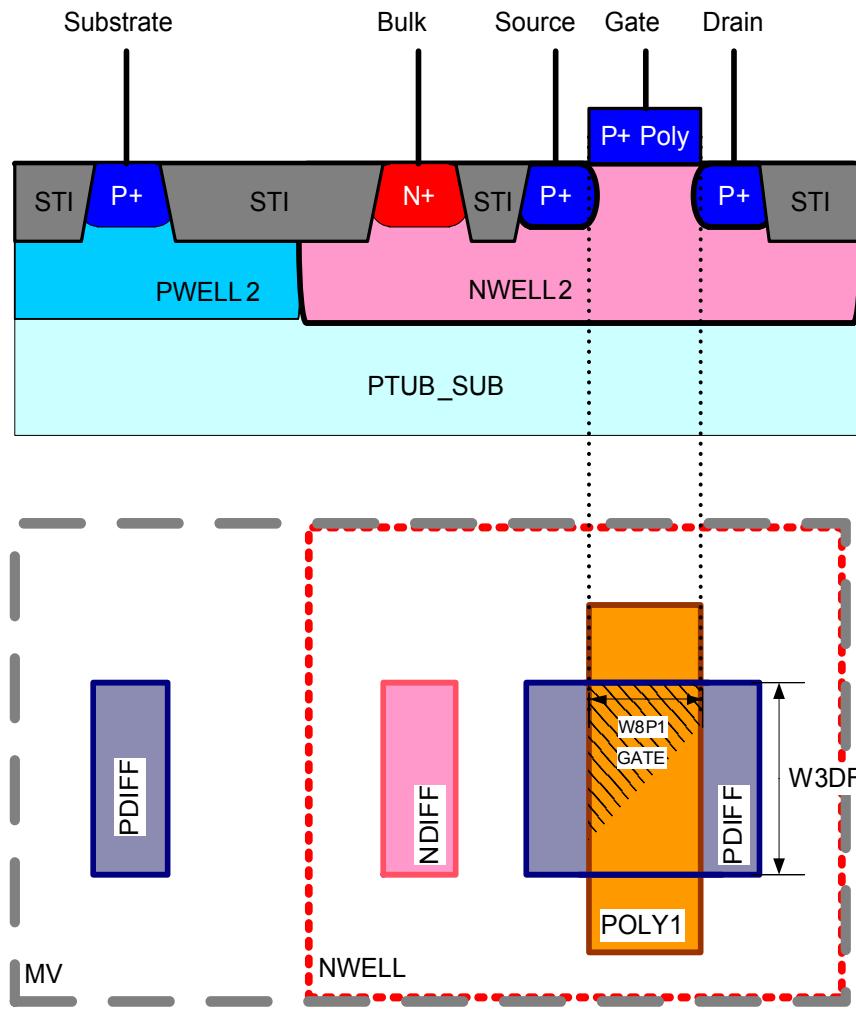
3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → pe5\_5

### **pe5\_5**

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.		
W8P1	Minimum GATE length	0.5	μm

**Note:** MV is necessary for pe5\_5

### **pe5\_5**



**Figure 3.66 pe5\_5**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → qpve5, qpvf5, qpvg5

### **qpve5, qpvf5, qpvg5**

This section describes the vertical PNP transistors qpve5, qpvf5, and qpvg5.

These transistors use PDIFF as emitter, NWELL2 as base and PWELL2 as collector. Their layouts are predefined. They must not be changed.

#### **qpve5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $2 \times 2 \mu\text{m}^2$

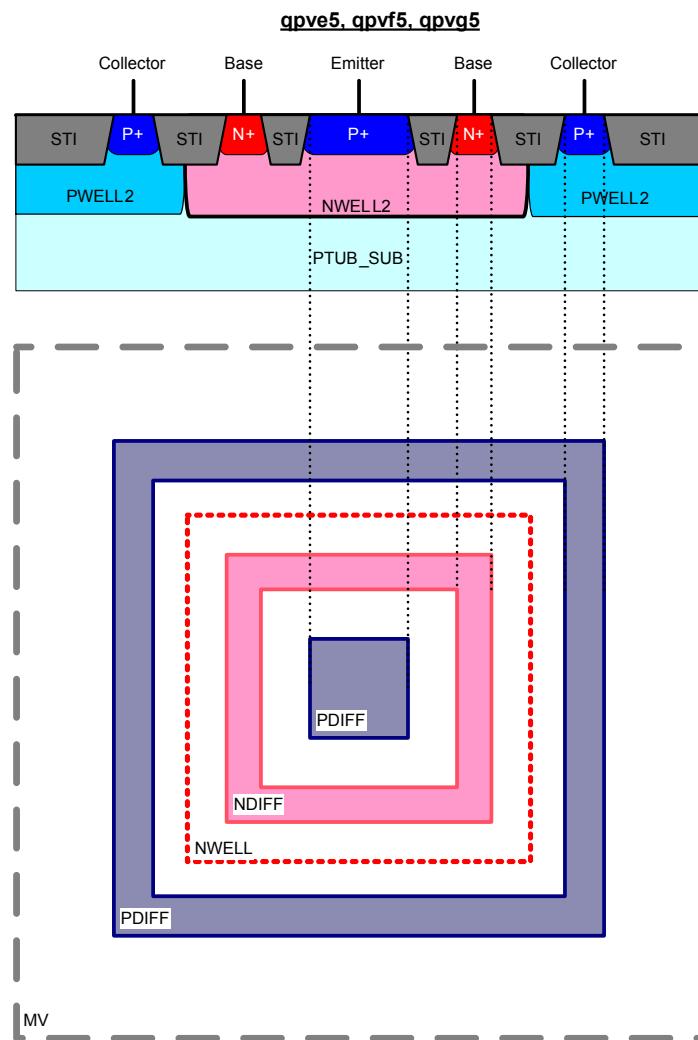
#### **qpvf5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $5 \times 5 \mu\text{m}^2$

#### **qpvg5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $10 \times 10 \mu\text{m}^2$

**Note:** MV is necessary for qpve5, qpvf5 and qpvg5.



**Figure 3.67 qpve5, qpvf5, qpvg5**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → rdn5, rdp5

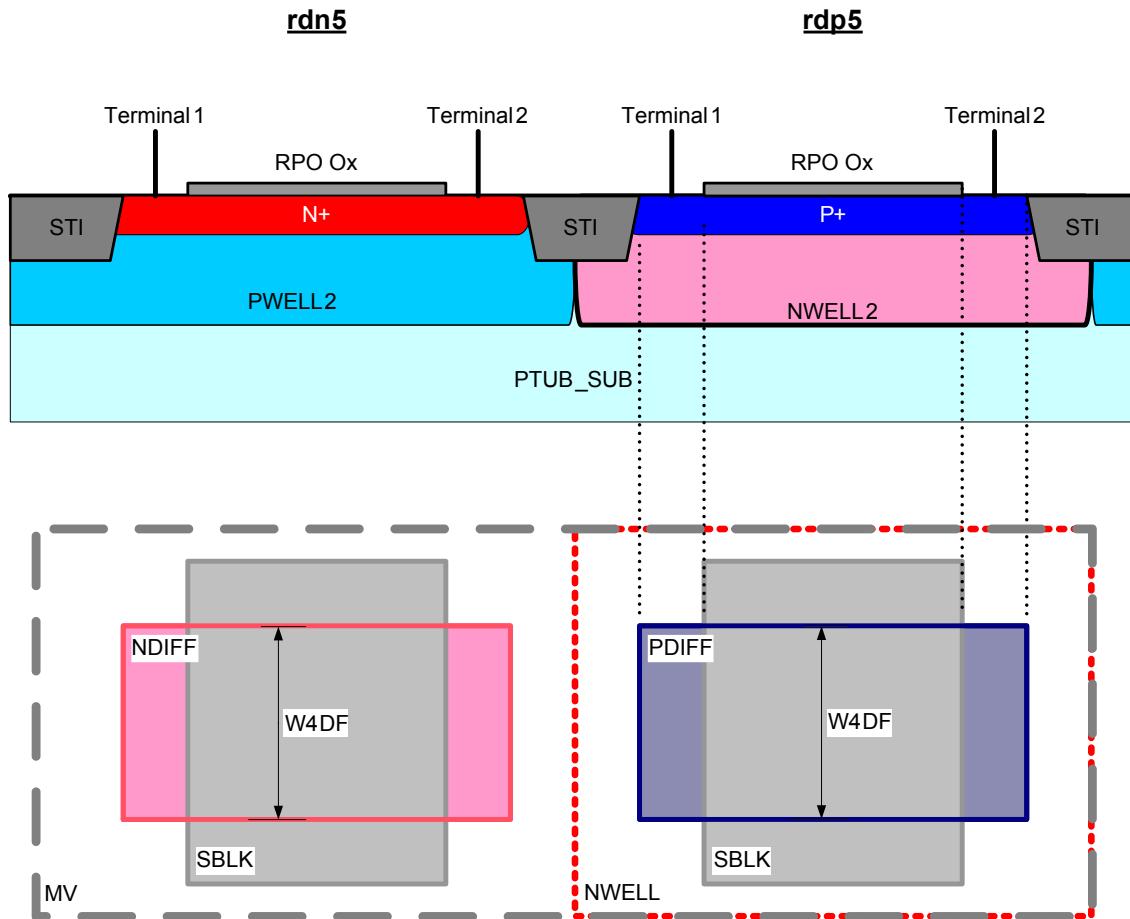
### **rdn5, rdp5**

Name	Description	Value	Unit
B1DN	rdn5 overlap of DEPL or HVDEPL is not allowed	-	-
W4DF	Minimum width	0.42	μm

**Note:** Recommended minimum number of squares is  $L/W \geq 5$ .

**Note:** MV is necessary for rdn5, rdp5

**Note:** rdn5 resistor definition: SBLK and not NWELL and NDIFF (except GATE)  
 rdp5 resistor definition: SBLK and NWELL and PDIFF (except GATE)



**Figure 3.68** rdn5, rdp5

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → rnw5

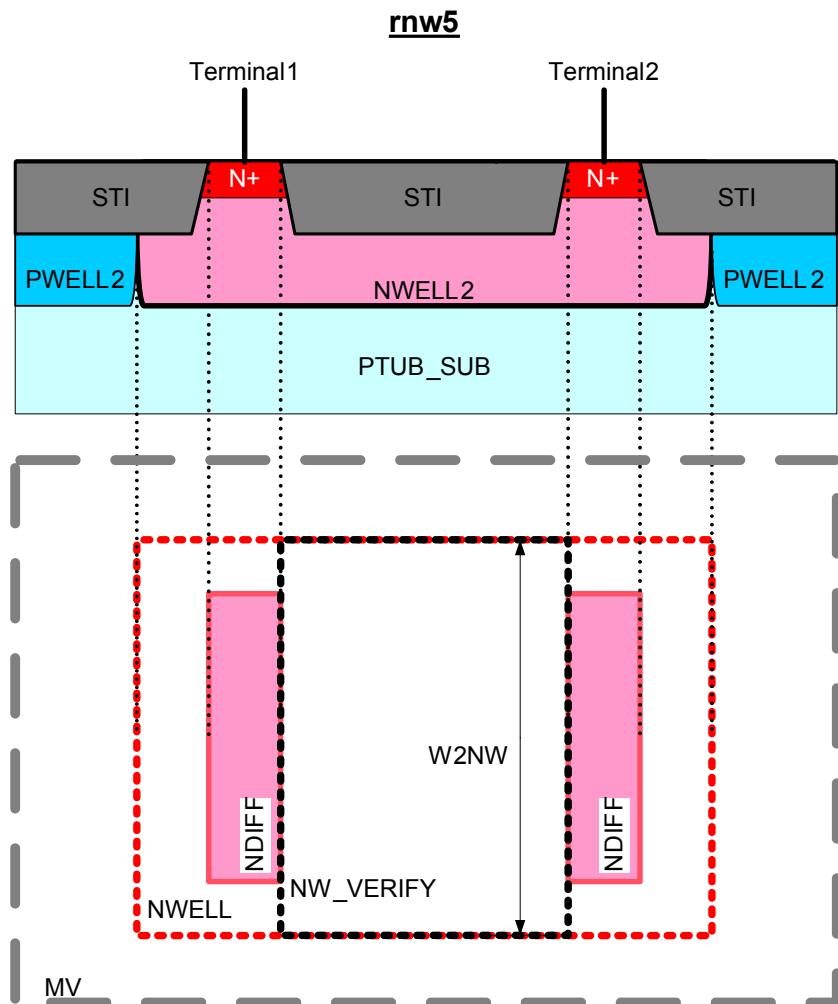
### **rnw5**

Name	Description	Value	Unit
W2NW	Minimum width	2.0	μm

**Note:** Recommended minimum number of squares is  $L/W \geq 5$ .

**Note:** rnw5 resistor definition: NWELL and NW\_VERIFY

**Note:** MV is necessary for rnw5



**Figure 3.69 rnw5**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → rnp1, rnp1\_3, rpp1, ...

### **rnp1, rnp1\_3, rpp1, rpp1\_3, rpp1nw\_3, rpp1s, rpp1s\_3**

Name	Description	Value	Unit
B16P1	rpp1#, rnp1#, rpp1s# overlap of DTI is not allowed	-	-
B22P1	(rnp1_3 NOT NWELL) without MV is not allowed	-	-
B24P1	rpp1nw_3 without NWELL is not allowed	-	-
B25P1	rpp1nw_3 overlap of rnw/rnw5 is not allowed	-	-
B2CT	CONT is not allowed within rpp1s#	-	-
B6P1	rnp1_3 overlap of rnw/rnw5 is not allowed	-	-
B7P1	rpp1_3 overlap of NWELL is not allowed	-	-
B8P1	rpp1s_3 overlap of rnw/rnw5 is not allowed	-	-
B4P1	rnp1_3 crossing NWELL edge is not allowed	-	-
B5P1	rpp1s_3 crossing NWELL edge is not allowed	-	-
W15P1	Minimum rnp1#, rpp1# width	0.42	μm
S1INP1	Minimum NIMP spacing to rpp1# or rpp1s#	0.26	μm
S1IPP1	Minimum PIMP spacing to rnp1#	0.26	μm
E1INP1	Minimum NIMP extension beyond rnp1#	0.18	μm
E1IPP1	Minimum PIMP extension beyond rpp1# or rpp1s#	0.18	μm

**Note:** Recommended minimum number of squares is L/W ≥ 5.

**Note:** Do not use dog-bone at the end of POLY1 resistor for CONT pickup.

**Note:** CONT array for POLY1 resistor should be a single column.

**Note:** rnp1# resistor definition: POLY1 and SBLK and NIMP (except GATE oversized by 0.22μm and except POLY1 nmvab oversized by 0.05μm (in the direction of GATE length)).

**Note:** rnp1\_3 device must be labeled "rnp1\_3" using POLY1 (VERIFICATION) layer

**Note:** rpp1# resistor definition: POLY1 and SBLK and PIMP (except GATE oversized by 0.22μm and except POLY1 of pmvab oversized by 0.05μm (in the direction of GATE length)).

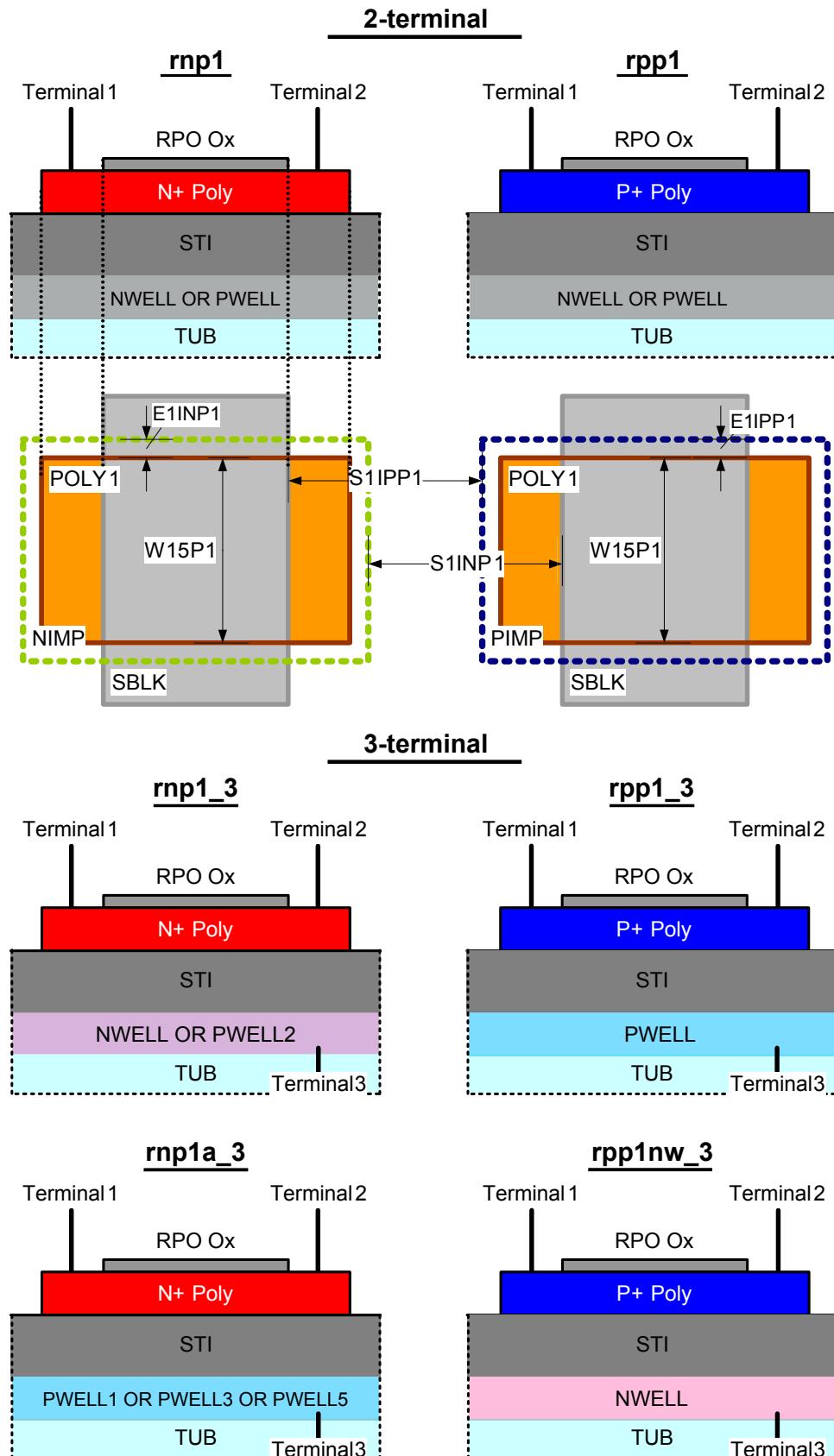
**Note:** rpp1\_3 device must be labeled "rpp1\_3" using POLY1 (VERIFICATION) layer.

**Note:** rpp1nw\_3 device must be labeled "rpp1nw\_3" using POLY1 (VERIFICATION) layer.

**Note:** rpp1s# resistor definition: POLY1 and POLY1\_VERIFY and PIMP. (except rpp1 oversized by 0.22 μm and not GATE)

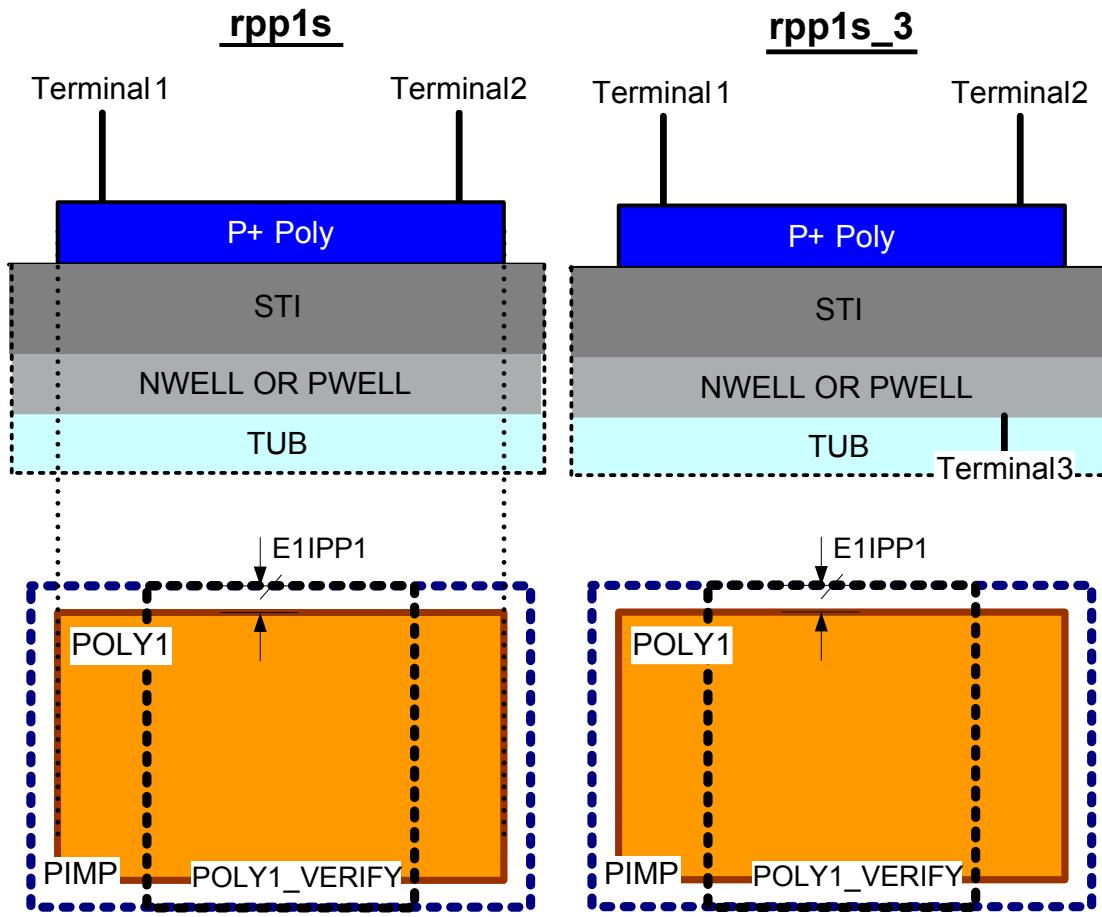
**Note:** rpp1s\_3 device must be labeled "rpp1s\_3" using POLY1 (VERIFICATION) layer.

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → rnp1, rnp1\_3, rpp1, ...



**Figure 3.70 rnp1# and rpp1#**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → rnp1, rnp1\_3, rpp1, ...



**Figure 3.71 rpp1s#**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → rm1, rm2

### **rm1, rm2**

Name	Description	Value	Unit
B2M1	CONT or VIA1 is not allowed within rm1	-	-
B2M2	VIA1 is not allowed within rm2	-	-
B3M2	VIATP is not allowed within rm2	-	-
	<b>Note:</b> valid if MET3 module is not selected		
B4M2	VIA2 is not allowed within rm2	-	-
	<b>Note:</b> Valid if MET3 module is selected.		

**Note:** rm1 resistor definition: MET1 and M1VERIFY.

**Note:** rm2 resistor definition: MET2 and M2VERIFY.



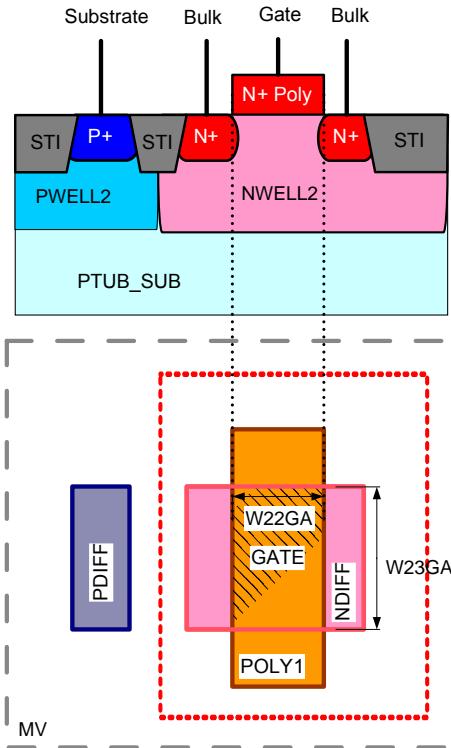
**Figure 3.72** rm1, rm2

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → mosvc5

### mosvc5

Name	Description	Value	Unit
B5GA	Only rectangular GATE is allowed	-	-
W22GA	Minimum GATE length	2.0	μm
W23GA	Minimum GATE width	2.0	μm

**Note:** MV is necessary for mosvc5



**Figure 3.73** mosvc5

### csf2p

The layout of the device csf2p is fixed and must not be changed. A single cell instance has an area of 4.48 μm x 10.80 μm.

Name	Description	Value	Unit
B20P1	csf2p overlap of DTI is not allowed	-	-

**Note:** CAPDEF is necessary for csf2p.

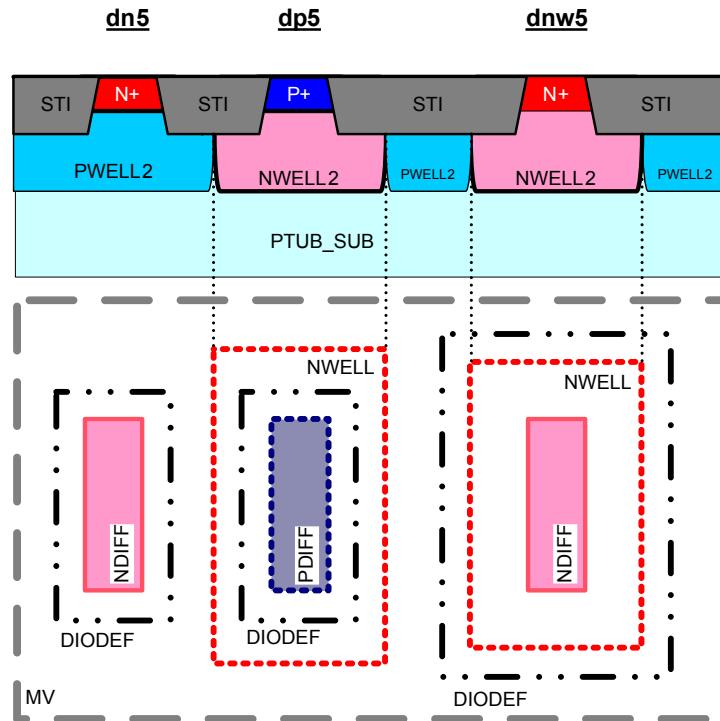
**Note:** Higher values may be achieved by the formation of arrays.

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → dn5, dp5, dnw5

### **dn5, dp5, dnw5**

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.

**Note:** MV is necessary for dn5, dp5 and dnw5.

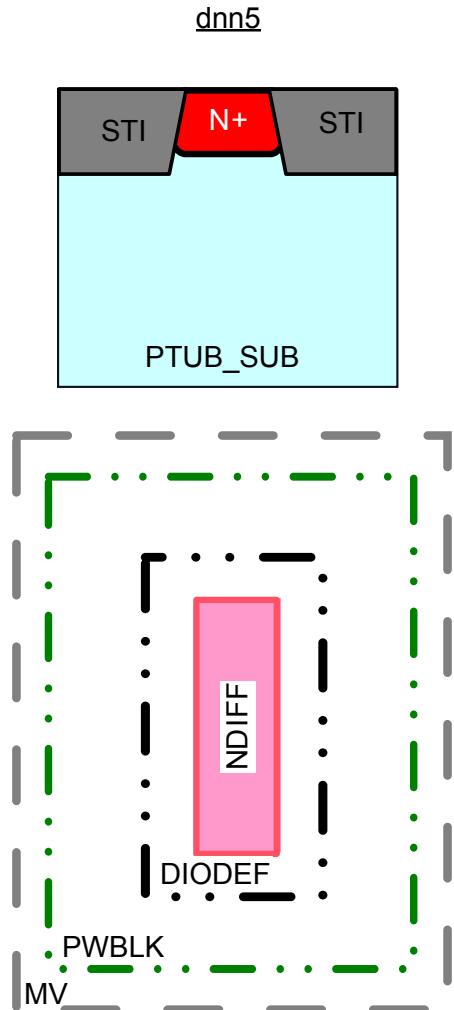


**Figure 3.74 dn5,dp5,dnw5**

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → dnn5

### dnn5

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.  
**Note:** MV is necessary for dnn5.



**Figure 3.75** dnn5

3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → pfuse

## pfuse

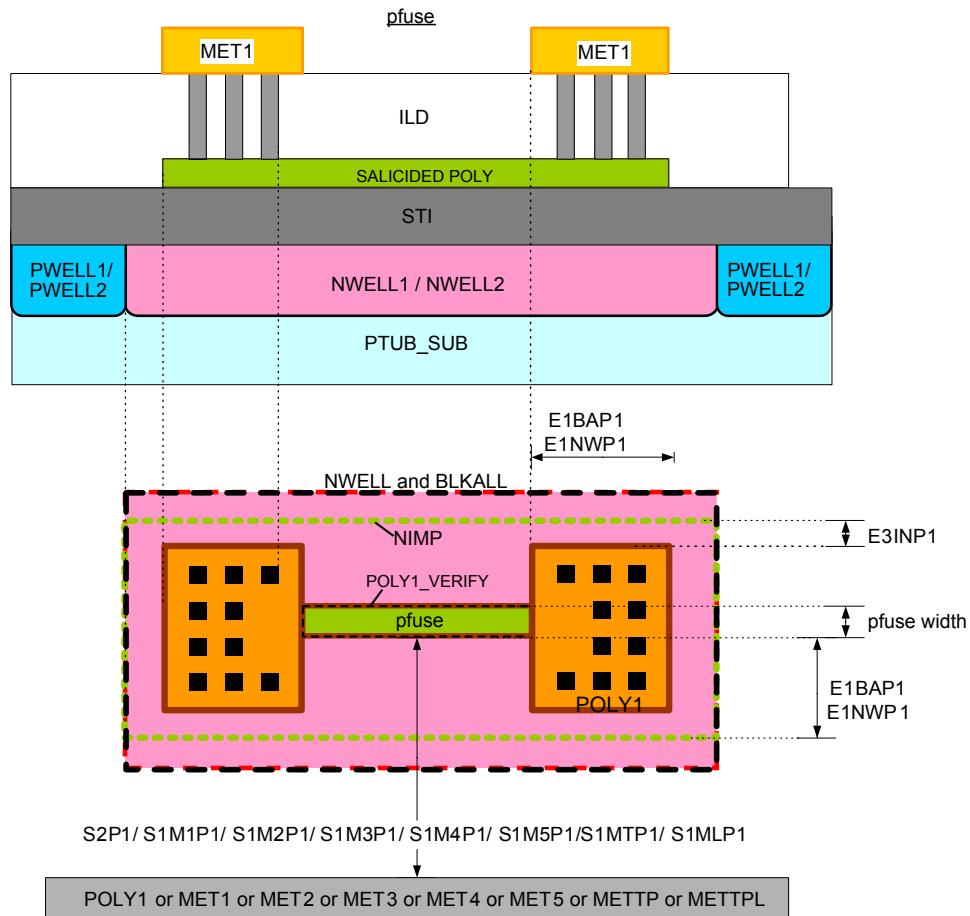
The layout of pfuse is predefined. It must not be changed. The other rules support the fixed dimensions of the layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B12P1	pfuse overlap of SBLK or DIFF is not allowed	-	-
B13P1	pfuse without NIMP and BLKALL is not allowed	-	-
B14P1	pfuse overlap of DTI is not allowed	-	-
B15P1	METCOP overlap of pfuse is not allowed	-	-
B2P1	pfuse overlap of MET1, MET2, MET3, MET4, MET5, METTP or METTPL is not allowed	-	-
S1DFP1	Minimum DIFF spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	2.0	μm
S1M1P1	Minimum MET1 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	0.8	μm
S1M2P1	Minimum MET2 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	0.8	μm
S1M3P1	Minimum MET3 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1M4P1	Minimum MET4 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1M5P1	Minimum MET5 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1MCP1	Minimum METCOP spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	10.0	μm
S1MLP1	Minimum METTPL spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1MTP1	Minimum METTP spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	1.7	μm
S1P1DT	Minimum pfuse spacing to DTI	1.7	μm
S2P1	Minimum POLY1 spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	2.0	μm
S2SBP1	Minimum SBLK spacing to pfuse <b>Note:</b> Valid in pfuse width direction only.	2.0	μm
E1BAP1	Minimum BLKALL enclosure of pfuse	1.7	μm
E1NWP1	Fixed NWELL enclosure of pfuse <b>Note:</b> NWELL is an electrically floating area without any connections.	1.7	μm
E3INP1	Minimum NIMP enclosure of POLY1	0.3	μm

**Note:** pfuse device must be marked with text "PFUSE" on layer POLY1\_VERIFY.

**Note:** pfuse device must have POLY1\_VERIFY layer.

## 3. Layer and Device rules → 3.2 MOS5 main module → 3.2.2 Device rules → pfuse

**Figure 3.76** pfuse

3. Layer and Device rules → 3.3 MET3 module

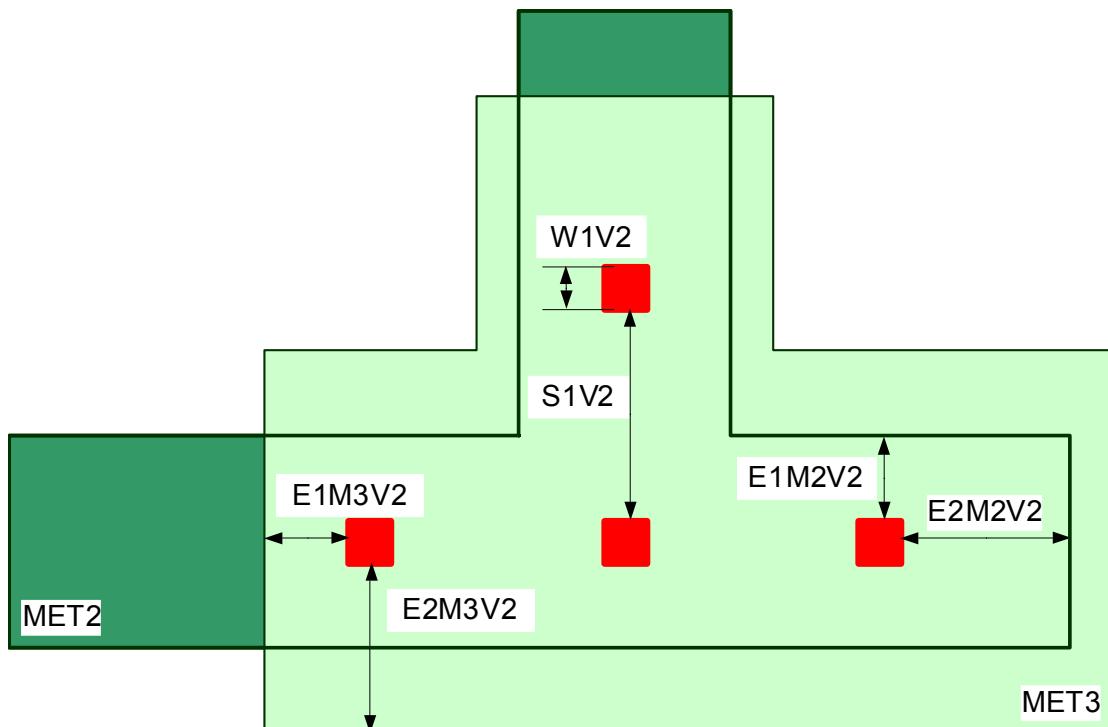
### 3.3 MET3 module

#### 3.3.1 Layer rules

##### VIA2

Name	Description	Value	Unit
B1V2	VIA2 must be covered by MET2 and MET3	-	-
W1V2	Fixed VIA2 size	0.26 x 0.26	μm x μm
S1V2	Minimum VIA2 spacing	0.26	μm
E1M2V2	Minimum MET2 enclosure of VIA2	0.01	μm
E1M3V2	Minimum MET3 enclosure of VIA2	0.01	μm
E2M2V2	Minimum MET2 enclosure of VIA2 (in one direction of VIA2 corner)	0.06	μm
E2M3V2	Minimum MET3 enclosure of VIA2 (in one direction of VIA2 corner)	0.06	μm
R1V2	Maximum ratio of VIA2 area to connected GATE area	20.0	-

**Note:** Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".



**Figure 3.77 VIA2**

## 3. Layer and Device rules → 3.3 MET3 module → 3.3.1 Layer rules → MET3

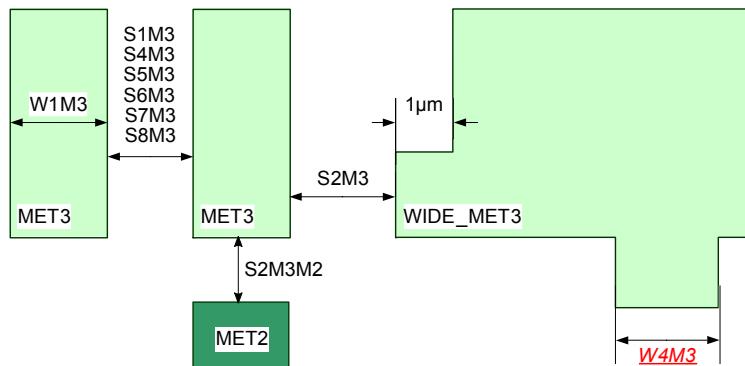
**MET3**

Name	Description	Value	Unit
B1M3M2	MET3 overlap of MET2 is not allowed (different net, tag_#, MET2, MET3 difference >300V)	-	-
W1M3	Minimum MET3 width	0.28	μm
<u>W4M3</u>	Minimum MET3 width joining wide MET3 track (> 35 μm)  <b>Note:</b> No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 μm from the main track prior to narrowing.	10.0	μm
<u>W5M3</u>	Maximum MET3 region size  <b>Note:</b> MET3 regions are defined as MET3 shapes (single MET3 shapes or a bundle of MET3 shapes, with width > 2.0 μm, inclusive of the spacing if the spacing is <= 1.0 μm) without any other metal layer above. For further information and design guidelines, please refer to the application note about <a href="#">IMD popping</a> on "my X-FAB".  <b>Note:</b> Not checked with standard DRC, option for check is available.	17.0 x 17.0	μm x μm
S1M3	Minimum MET3 spacing/notch	0.28	μm
<u>S4M3</u>	Minimum MET3 spacing (different net, tag_#, difference >25V ≤ 60V)  <b>Note:</b> Valid for spacing of all MET3 shapes with label tag_# to all MET3 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".	0.4	μm
<u>S5M3</u>	Minimum MET3 spacing (different net, tag_#, difference >60V ≤100V)  <b>Note:</b> Valid for spacing of all MET3 shapes with label tag_# to all MET3 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".	0.6	μm
<u>S6M3</u>	Minimum MET3 spacing (different net, tag_#, difference >100V ≤200V)  <b>Note:</b> Valid for spacing to all MET3 shapes with label tag_# to all MET3 shapes having other voltage classes and a difference between the numbers of the voltage class names of >100V ≤ 200V. Refer to the design related guideline "Voltage class definitions".	0.8	μm
<u>S7M3</u>	Minimum MET3 spacing (different net, tag_#, difference >200V ≤300V)  <b>Note:</b> Valid for spacing to all MET3 shapes with label tag_# to all MET3 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤ 300V. Refer to the design related guideline "Voltage class definitions".	1.2	μm
<u>S8M3</u>	Minimum MET3 spacing (different net, tag_#, difference >300V)  <b>Note:</b> Valid for spacing to all MET3 shapes with label tag_# to all MET3 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".	1.6	μm
S2M3	Minimum MET3 spacing to WIDE_MET3	0.6	μm
<u>S2M3M2</u>	Minimum MET3 spacing to MET2 (different net, tag_#, difference >300V)  <b>Note:</b> Valid if the voltage difference between MET2, MET3 voltage is >300V.  <b>Note:</b> Valid for spacing of all MET3/MET2 shapes with label tag_# to all MET2/MET3 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".	1.6	μm
A1M3	Minimum MET3 area	0.202	μm <sup>2</sup>
<u>R1M3</u>	Minimum ratio of MET3 area to EXTENT area  <b>Note:</b> Not checked with standard DRC, option for check is available.	30.0	%
<u>R2M3</u>	Maximum ratio of MET3 area to EXTENT area  <b>Note:</b> Not checked with standard DRC, option for check is available.	65.0	%
<u>R1M3P1</u>	Maximum ratio of MET3 area to connected GATE area  <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	400.0	-
<u>R2M3P1</u>	Maximum ratio of MET3 area to connected GATE area  <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	400.0	-



## 3. Layer and Device rules → 3.3 MET3 module → 3.3.1 Layer rules → MET3

Name	Description	Value	Unit
Q1M3	Resistor terminal net without VLABEL	-	-
<b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".			

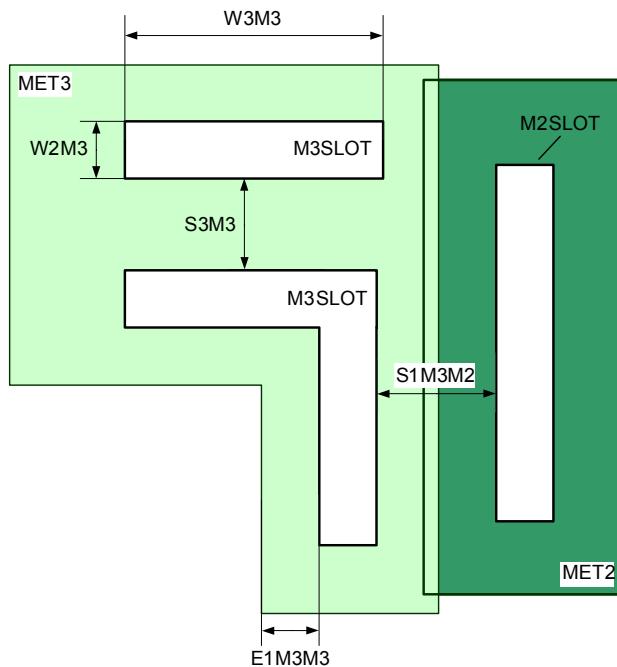
**Figure 3.78** MET3

3. Layer and Device rules → 3.3 MET3 module→ 3.3.1 Layer rules→ M3SLOT

### M3SLOT

Name	Description	Value	Unit
B1M3	All MET3 tracks > 35µm wide to be slotted (except Pads)	-	-
W2M3	Minimum M3SLOT width	0.6	µm
W3M3	Minimum M3SLOT length	20.0	µm
	<b>Note:</b> If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M3	Minimum M3SLOT spacing/notch	10.0	µm
S1M3M2	Minimum M3SLOT spacing to M2SLOT <b>Note:</b> M3SLOT is not allowed over M2SLOT.	2.0	µm
E1M3M3	Minimum MET3 enclosure of M3SLOT <b>Note:</b> M3SLOT without MET3 is not allowed.	10.0	µm

**Note:** Insert M3SLOTS in direction of current flow.



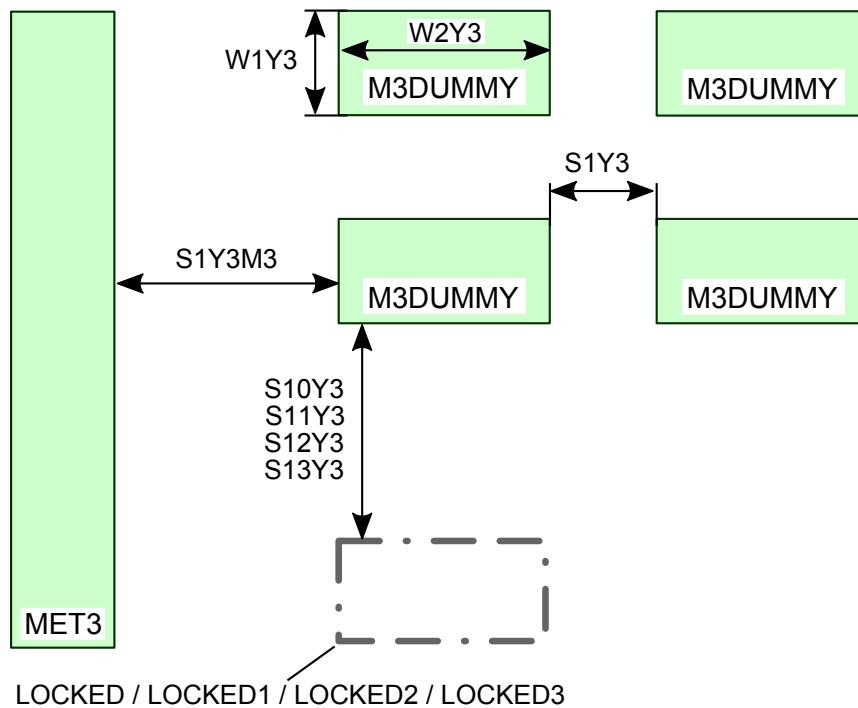
**Figure 3.79** M3SLOT

## 3. Layer and Device rules → 3.3 MET3 module → 3.3.1 Layer rules → M3DUMMY

**M3DUMMY**

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y3	Only rectangular M3DUMMY is allowed	-	-
B2Y3	M3DUMMY overlap of MET3 is not allowed	-	-
B3Y3V2	M3DUMMY overlap of VIA2 is not allowed	-	-
B3Y3V3	M3DUMMY overlap of VIA3 is not allowed	-	-
B3Y3VL	M3DUMMY overlap of VIATPL is not allowed  <b>Note:</b> Only valid if module MET4 is not selected.	-	-
B3Y3VT	M3DUMMY overlap of VIATP is not allowed  <b>Note:</b> Only valid if module MET4 is not selected.	-	-
W1Y3	Minimum M3DUMMY width	2.0	μm
W2Y3	Maximum M3DUMMY edge length	20.0	μm
S1Y3	Minimum M3DUMMY spacing	2.0	μm
S10Y3	Minimum M3DUMMY spacing to LOCKED	4.0	μm
S11Y3	Minimum M3DUMMY spacing to LOCKED1	4.0	μm
S12Y3	Minimum M3DUMMY spacing to LOCKED2	4.0	μm
S13Y3	Minimum M3DUMMY spacing to LOCKED3	4.0	μm
S1Y3M3	Minimum M3DUMMY spacing to MET3	4.0	μm

**Figure 3.80 M3DUMMY**

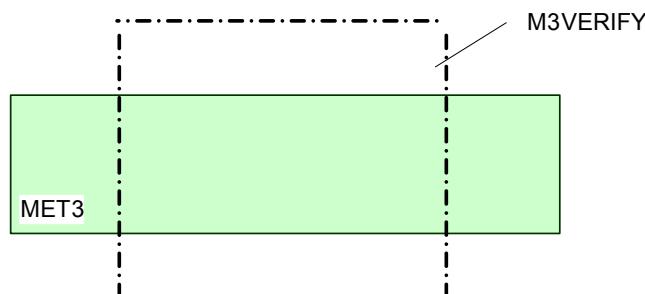
3. Layer and Device rules → 3.3 MET3 module → 3.3.2 Device rules → rm3

### 3.3.2 Device rules

#### rm3

Name	Description	Value	Unit
B2M3	VIA2 is not allowed within rm3	-	-
B3M3	VIATP is not allowed within rm3 <b>Note:</b> Valid if module METMID is selected and not MET4.	-	-
B4M3	VIA3 is not allowed within rm3 <b>Note:</b> Valid if MET4 module is selected.	-	-
B5M3	VIATPL is not allowed within rm3 <b>Note:</b> Valid if module METTHK is selected and not METMID	-	-

**Note:** rm3 resistor definition: MET3 and M3VERIFY.



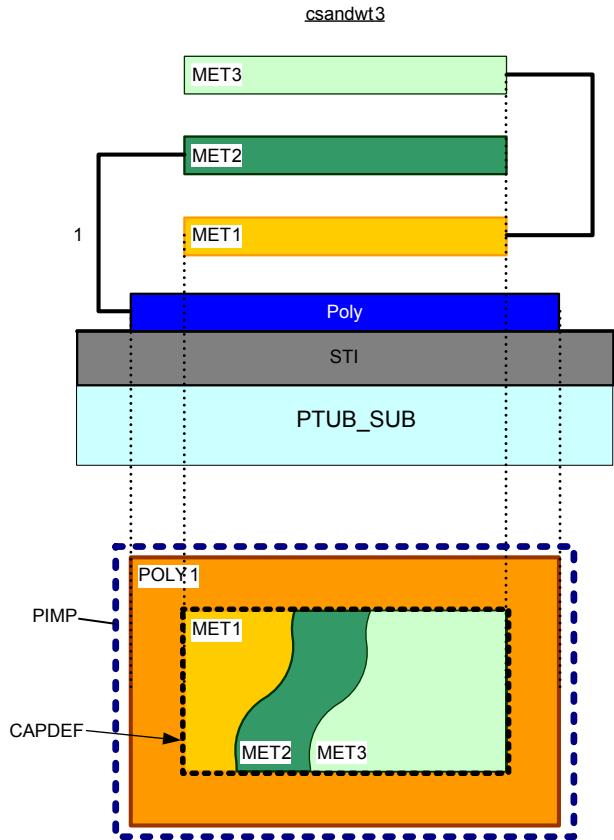
**Figure 3.81** rm3

3. Layer and Device rules → 3.3 MET3 module → 3.3.2 Device rules → csandwt3

### csandwt3

Name	Description	Value	Unit
B17P1	csandwt3 overlap of DTI is not allowed	-	-

**Note:** CAPDEF is necessary for csandwt3.



**Figure 3.82** csandwt3

### cif3

The layout of the device cif3 is fixed and must not be changed. A single cell instance has an area of  $7.04\mu\text{m} \times 25.00\mu\text{m}$ .

**Note:** CAPDEF is necessary for cif3.

**Note:** Higher values may be achieved by the formation of arrays.

### csf3p, csf3, csf3a

The layouts of the devices csf3p, csf3 and csf3a are fixed and must not be changed. For csf3p and csf3, a single cell instance has an area of  $4.48\mu\text{m} \times 10.80\mu\text{m}$ . For csf3a, a single cell instance has an area of  $5.76\mu\text{m} \times 11.10\mu\text{m}$ .

Name	Description	Value	Unit
B21P1	csf3p overlap of DTI is not allowed	-	-

**Note:** CAPDEF is necessary for csf3p, csf3 and csf3a.

**Note:** Higher values may be achieved by the formation of arrays.

### cif3a

The layout of the device cif3a is fixed and must not be changed. A single cell instance has an area of  $4.48\mu\text{m} \times 10.80\mu\text{m}$ .

**Note:** CAPDEF is necessary for cif3a.

3. Layer and Device rules → 3.3 MET3 module→ 3.3.2 Device rules→ cif3a

**Note:** Higher values may be achieved by the formation of arrays.

3. Layer and Device rules → 3.4 MET4 module

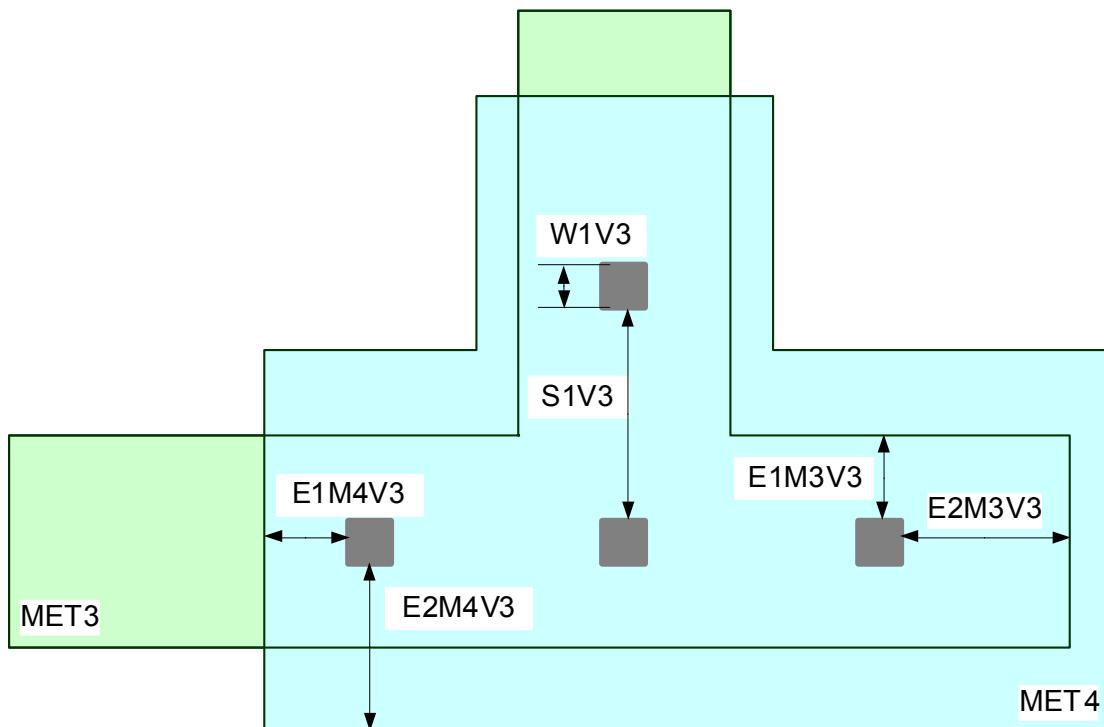
## 3.4 MET4 module

### 3.4.1 Layer rules

#### VIA3

Name	Description	Value	Unit
B1V3	VIA3 must be covered by MET3 and MET4	-	-
W1V3	Fixed VIA3 size	0.26 x 0.26	μm x μm
S1V3	Minimum VIA3 spacing	0.26	μm
E1M3V3	Minimum MET3 enclosure of VIA3	0.01	μm
E1M4V3	Minimum MET4 enclosure of VIA3	0.01	μm
E2M3V3	Minimum MET3 enclosure of VIA3 (in one direction of VIA3 corner)	0.06	μm
E2M4V3	Minimum MET4 enclosure of VIA3 (in one direction of VIA3 corner)	0.06	μm
R1V3	Maximum ratio of VIA3 area to connected GATE area	20.0	-

**Note:** Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".



**Figure 3.83 VIA3**

## 3. Layer and Device rules → 3.4 MET4 module → 3.4.1 Layer rules → MET4

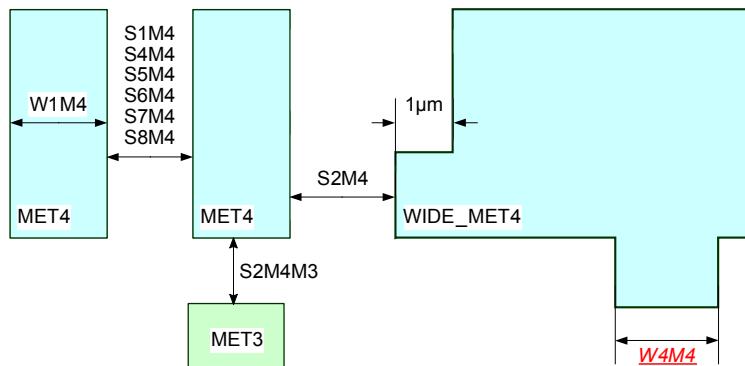
**MET4**

Name	Description	Value	Unit
B1M4M3	MET4 overlap of MET3 is not allowed (different net, tag_#, MET3, MET4 difference >300V)	-	-
W1M4	Minimum MET4 width	0.28	μm
<u>W4M4</u>	Minimum MET4 width joining wide MET4 track (> 35 μm)  <b>Note:</b> No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 μm from the main track prior to narrowing.	10.0	μm
<u>W5M4</u>	Maximum MET4 region size  <b>Note:</b> MET4 regions are defined as MET4 shapes (single MET4 shapes or a bundle of ME4 shapes, with width > 2.0μm, inclusive of the spacing if the spacing is <= 1.0μm) without any other metal layer above. For further information and design guidelines, please refer to the application note about <a href="#">IMD popping</a> on "my X-FAB".  <b>Note:</b> Not checked with standard DRC, option for check is available.	17.0 x 17.0	μm x μm
S1M4	Minimum MET4 spacing/notch	0.28	μm
<u>S4M4</u>	Minimum MET4 spacing (different net, tag_#, difference >25V ≤ 60V)  <b>Note:</b> Valid for spacing of all MET4 shapes with label tag_# to all MET4 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".	0.4	μm
<u>S5M4</u>	Minimum MET4 spacing (different net, tag_#, difference >60V ≤100V)  <b>Note:</b> Valid for spacing of all MET4 shapes with label tag_# to all MET4 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".	0.6	μm
<u>S6M4</u>	Minimum MET4 spacing (different net, tag_#, difference >100V ≤200V)  <b>Note:</b> Valid for spacing to all MET4 shapes with label tag_# to all MET4 shapes having other voltage classes and a difference between the numbers of the voltage class names of >100V ≤ 200V. Refer to the design related guideline "Voltage class definitions".	0.8	μm
<u>S7M4</u>	Minimum MET4 spacing (different net, tag_#, difference >200V ≤300V)  <b>Note:</b> Valid for spacing to all MET4 shapes with label tag_# to all MET4 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤ 300V. Refer to the design related guideline "Voltage class definitions".	1.2	μm
<u>S8M4</u>	Minimum MET4 spacing (different net, tag_#, difference >300V)  <b>Note:</b> Valid for spacing to all MET4 shapes with label tag_# to all MET4 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".	1.6	μm
S2M4	Minimum MET4 spacing to WIDE_MET4	0.6	μm
<u>S2M4M3</u>	Minimum MET4 spacing to MET3 (different net, tag_#, difference >300V)  <b>Note:</b> Valid if the voltage difference between MET3, MET4 voltage is >300V.  <b>Note:</b> Valid for spacing of all MET4/MET3 shapes with label tag_# to all MET3/MET4 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".	1.6	μm
A1M4	Minimum MET4 area	0.202	μm <sup>2</sup>
<u>R1M4</u>	Minimum ratio of MET4 area to EXTENT area  <b>Note:</b> Not checked with standard DRC, option for check is available.	30.0	%
<u>R2M4</u>	Maximum ratio of MET4 area to EXTENT area  <b>Note:</b> Not checked with standard DRC, option for check is available.	65.0	%
R1M4P1	Maximum ratio of MET4 area to connected GATE area  <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	400.0	-
R2M4P1	Maximum ratio of MET4 area to connected GATE area  <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	400.0	-



## 3. Layer and Device rules → 3.4 MET4 module→ 3.4.1 Layer rules→ MET4

Name	Description	Value	Unit
Q1M4	Resistor terminal net without VLABEL  <b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".	-	-

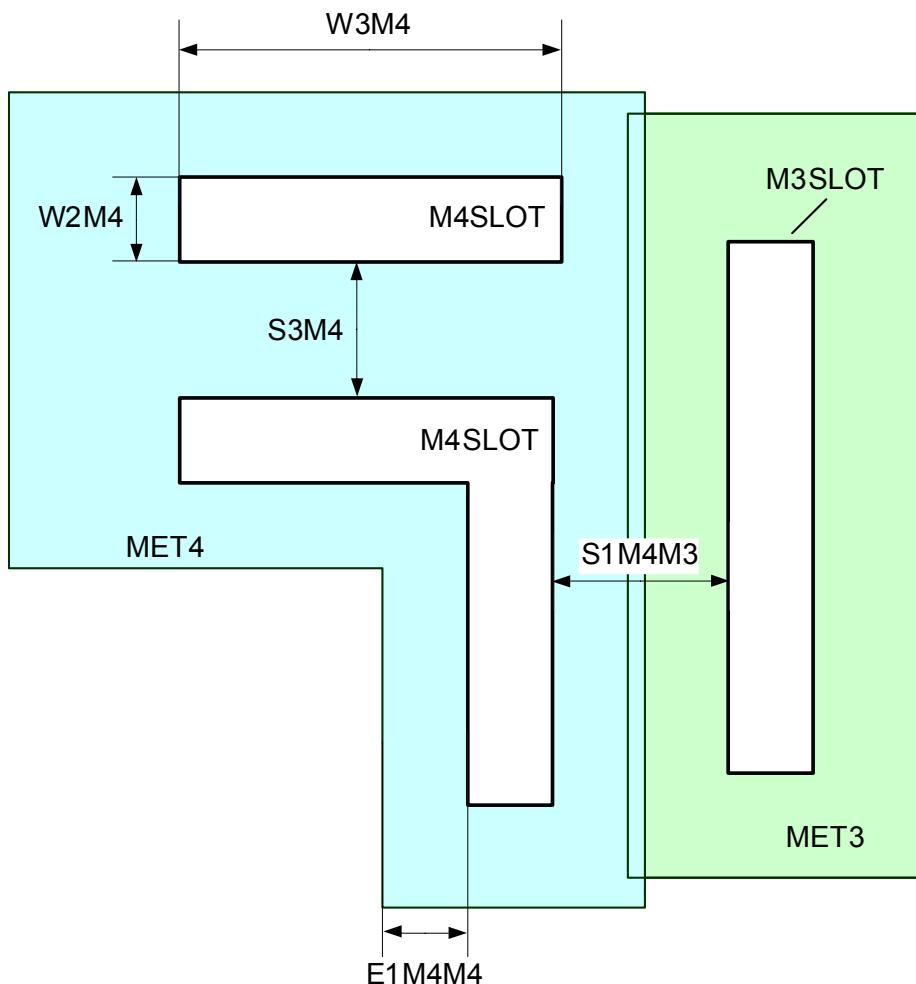
**Figure 3.84** MET4

3. Layer and Device rules → 3.4 MET4 module → 3.4.1 Layer rules → M4SLOT

## M4SLOT

Name	Description	Value	Unit
B1M4	All MET4 tracks > 35µm wide to be slotted (except Pads)	-	-
W2M4	Minimum M4SLOT width	0.6	µm
W3M4	Minimum M4SLOT length	20.0	µm
	<b>Note:</b> If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M4	Minimum M4SLOT spacing/notch	10.0	µm
S1M4M3	Minimum M4SLOT spacing to M3SLOT	2.0	µm
	<b>Note:</b> M4SLOT is not allowed over M3SLOT.		
E1M4M4	Minimum MET4 enclosure of M4SLOT	10.0	µm
	<b>Note:</b> M4SLOT without MET4 is not allowed.		

**Note:** Insert M4SLOTS in direction of current flow.



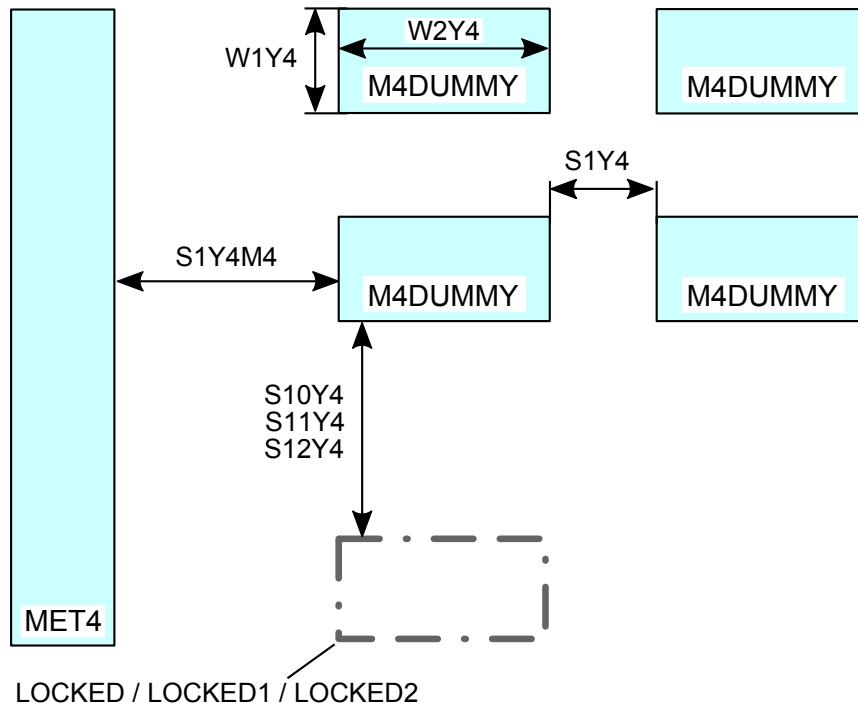
**Figure 3.85** M4SLOT

## 3. Layer and Device rules → 3.4 MET4 module → 3.4.1 Layer rules → M4DUMMY

**M4DUMMY**

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y4	Only rectangular M4DUMMY is allowed	-	-
B2Y4	M4DUMMY overlap of MET4 is not allowed	-	-
B3Y4V3	M4DUMMY overlap of VIA3 is not allowed	-	-
B3Y4V4	M4DUMMY overlap of VIA4 is not allowed	-	-
B3Y4VL	M4DUMMY overlap of VIATPL is not allowed	-	-
<b>Note:</b> Only valid if module METTHK is selected and not (MET5 or METMID).			
B3Y4VT	M4DUMMY overlap of VIATP is not allowed	-	-
<b>Note:</b> Only valid if module MET5 is not selected.			
W1Y4	Minimum M4DUMMY width	2.0	μm
W2Y4	Maximum M4DUMMY edge length	20.0	μm
S1Y4	Minimum M4DUMMY spacing	2.0	μm
S10Y4	Minimum M4DUMMY spacing to LOCKED	4.0	μm
S11Y4	Minimum M4DUMMY spacing to LOCKED1	4.0	μm
S12Y4	Minimum M4DUMMY spacing to LOCKED2	4.0	μm
S1Y4M4	Minimum M4DUMMY spacing to MET4	4.0	μm

**Figure 3.86 M4DUMMY**

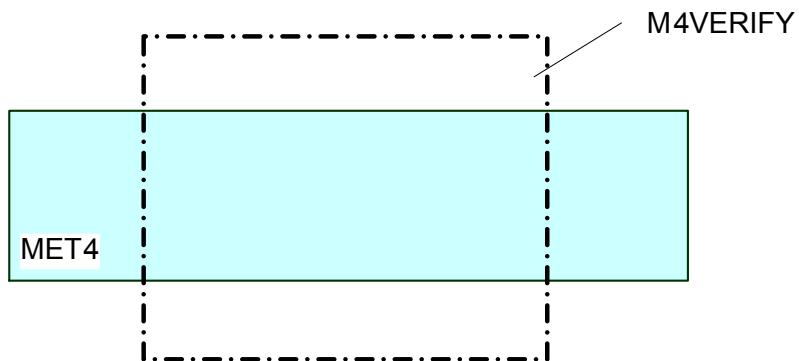
3. Layer and Device rules → 3.4 MET4 module → 3.4.2 Device rules → rm4

### 3.4.2 Device rules

#### rm4

Name	Description	Value	Unit
B2M4	VIA3 is not allowed within rm4	-	-
B3M4	VIATP is not allowed within rm4 <b>Note:</b> Valid if module METMID is selected and not MET5	-	-
B4M4	VIA4 is not allowed within rm4 <b>Note:</b> Valid if MET5 module is selected.	-	-
B5M4	VIATPL is not allowed within rm4 <b>Note:</b> Valid if module METTHK is selected and not METMID	-	-

**Note:** rm4 resistor definition: MET4 and M4VERIFY.



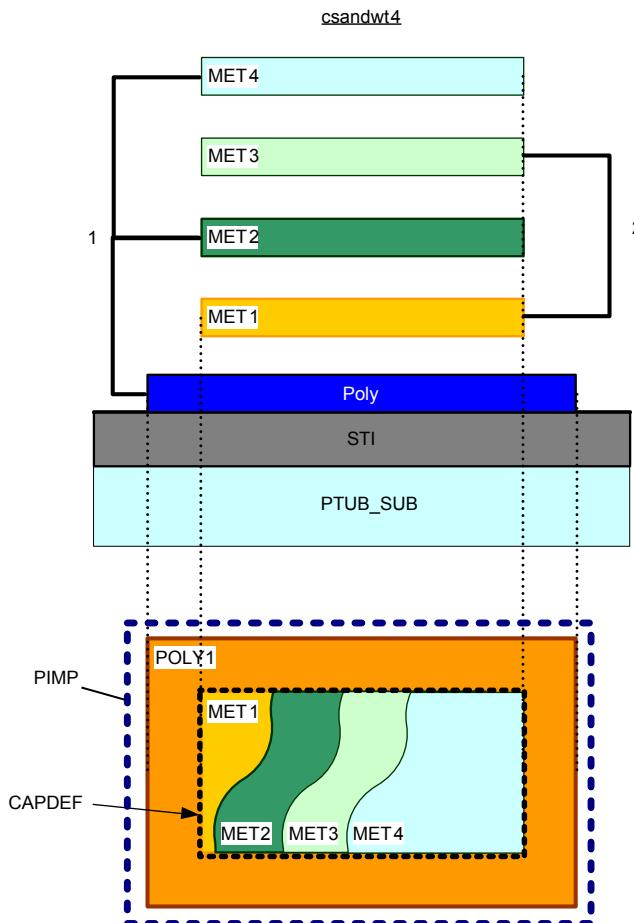
**Figure 3.87** rm4

3. Layer and Device rules → 3.4 MET4 module → 3.4.2 Device rules → csandwt4

### **csandwt4**

Name	Description	Value	Unit
B18P1	csandwt4 overlap of DTI is not allowed	-	-

**Note:** CAPDEF is necessary for csandwt4.



**Figure 3.88** csandwt4

### **cif4**

The layout of the device cif4 is fixed and must not be changed. A single cell instance has an area of  $7.04\mu\text{m} \times 25.00\mu\text{m}$ .

**Note:** CAPDEF is necessary for cif4.

**Note:** Higher values may be achieved by the formation of arrays.

### **cif4a**

The layout of the device cif4a is fixed and must not be changed. A single cell instance has an area of  $4.48\mu\text{m} \times 10.80\mu\text{m}$ .

**Note:** CAPDEF is necessary for cif4a.

**Note:** Higher values may be achieved by the formation of arrays.

### **csf4, csf4a**

The layouts of the devices csf4 and csf4a are fixed and must not be changed. For csf4, a single cell instance has an area of  $4.48\mu\text{m} \times 10.80\mu\text{m}$ . For csf4a, a single cell instance has an area of  $5.76\mu\text{m} \times 11.10\mu\text{m}$ .

**Note:** CAPDEF is necessary for csf4 and csf4a.

**Note:** Higher values may be achieved by the formation of arrays.

3. Layer and Device rules → 3.5 MET5 module

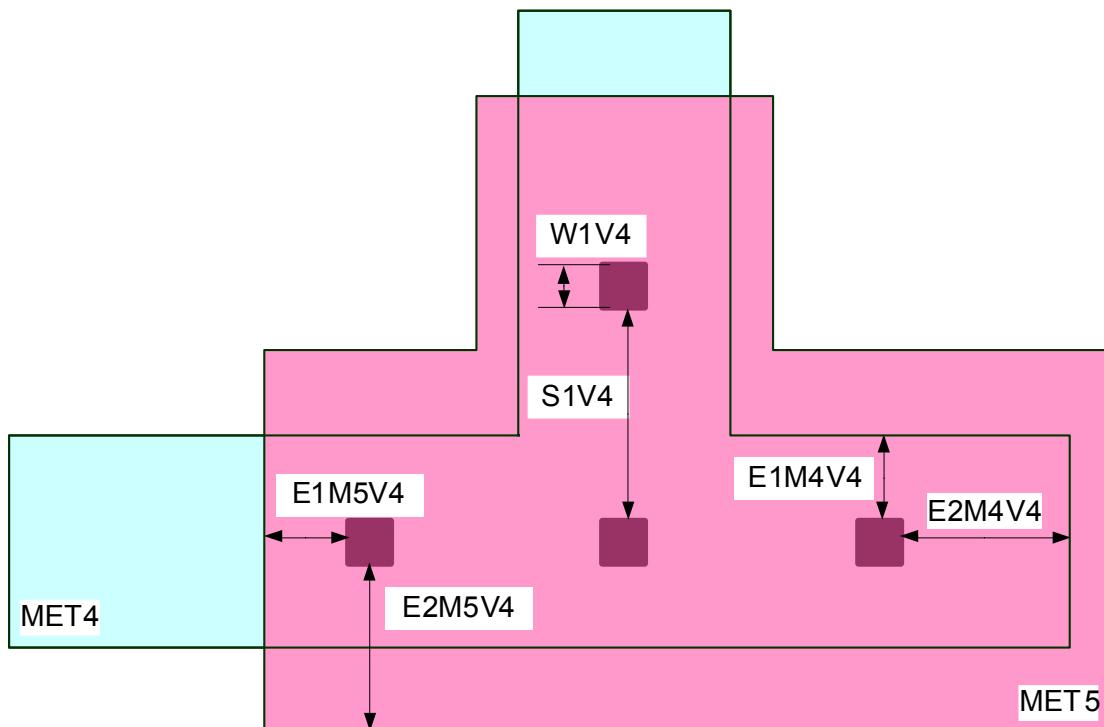
## 3.5 MET5 module

### 3.5.1 Layer rules

#### VIA4

Name	Description	Value	Unit
B1V4	VIA4 must be covered by MET4 and MET5	-	-
W1V4	Fixed VIA4 size	0.26 x 0.26	μm x μm
S1V4	Minimum VIA4 spacing	0.26	μm
E1M4V4	Minimum MET4 enclosure of VIA4	0.01	μm
E1M5V4	Minimum MET5 enclosure of VIA4	0.01	μm
E2M4V4	Minimum MET4 enclosure of VIA4 (in one direction of VIA4 corner)	0.06	μm
E2M5V4	Minimum MET5 enclosure of VIA4 (in one direction of VIA4 corner)	0.06	μm
R1V4	Maximum ratio of VIA4 area to connected GATE area	20.0	-

**Note:** Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".



**Figure 3.89 VIA4**

## 3. Layer and Device rules → 3.5 MET5 module → 3.5.1 Layer rules → MET5

**MET5**

Name	Description	Value	Unit
B1M5M4	MET5 overlap of MET4 is not allowed (different net, tag_#, MET4, MET5 difference >300V)	-	-
W1M5	Minimum MET5 width	0.28	μm
<b>W4M5</b>	Minimum MET5 width joining wide MET5 track (> 35 μm)  <b>Note:</b> No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 μm from the main track prior to narrowing.	10.0	μm
<b>W5M5</b>	Maximum MET5 region size  <b>Note:</b> MET5 regions are defined as MET5 shapes (single MET5 shapes or a bundle of MET5 shapes, with width > 2.0 μm, inclusive of the spacing if the spacing is <= 1.0 μm) without any other metal layer above. For further information and design guidelines, please refer to the application note about <a href="#">IMD popping</a> on "my X-FAB".  <b>Note:</b> Not checked with standard DRC, option for check is available.	17.0 x 17.0	μm x μm
S1M5	Minimum MET5 spacing/notch	0.28	μm
<b>S4M5</b>	Minimum MET5 spacing (different net, tag_#, difference >25V ≤ 60V)  <b>Note:</b> Valid for spacing of all MET5 shapes with label tag_# to all MET5 shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".	0.4	μm
<b>S5M5</b>	Minimum MET5 spacing (different net, tag_#, difference >60V ≤100V)  <b>Note:</b> Valid for spacing of all MET5 shapes with label tag_# to all MET5 shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".	0.6	μm
<b>S6M5</b>	Minimum MET5 spacing (different net, tag_#, difference >100V ≤200V)  <b>Note:</b> Valid for spacing to all MET5 shapes with label tag_# to all MET5 shapes having other voltage classes and a difference between the numbers of the voltage class names of >100V ≤ 200V. Refer to the design related guideline "Voltage class definitions".	0.8	μm
<b>S7M5</b>	Minimum MET5 spacing (different net, tag_#, difference >200V ≤300V)  <b>Note:</b> Valid for spacing to all MET5 shapes with label tag_# to all MET5 shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤ 300V. Refer to the design related guideline "Voltage class definitions".	1.2	μm
<b>S8M5</b>	Minimum MET5 spacing (different net, tag_#, difference >300V)  <b>Note:</b> Valid for spacing to all MET5 shapes with label tag_# to all MET5 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".	1.6	μm
<b>S1MLM5</b>	Minimum METTPL spacing to MET5 (different net, tag_#, difference >300V)  <b>Note:</b> Valid if the voltage difference between METTPL, MET5 voltage is >300V.  <b>Note:</b> Valid for spacing of all MET5/METTPL shapes with label tag_# to all METTPL /MET5 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".  <b>Note:</b> Valid if METMID module is not selected.	1.6	μm
S2M5	Minimum MET5 spacing to WIDE_MET5	0.6	μm
<b>S2M5M4</b>	Minimum MET5 spacing to MET4 (different net, tag_#, difference >300V)  <b>Note:</b> Valid if the voltage difference between MET4, MET5 voltage is >300V.  <b>Note:</b> Valid for spacing of all MET5/MET4 shapes with label tag_# to all MET4/MET5 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".	1.6	μm
A1M5	Minimum MET5 area	0.202	μm <sup>2</sup>
<b>R1M5</b>	Minimum ratio of MET5 area to EXTENT area  <b>Note:</b> Not checked with standard DRC, option for check is available.	30.0	%
<b>R2M5</b>	Maximum ratio of MET5 area to EXTENT area  <b>Note:</b> Not checked with standard DRC, option for check is available.	65.0	%

⇒

## 3. Layer and Device rules → 3.5 MET5 module → 3.5.1 Layer rules → MET5

Name	Description	Value	Unit
R1M5P1	Maximum ratio of MET5 area to connected GATE area <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	400.0	-
R2M5P1	Maximum ratio of MET5 area to connected GATE area <b>Note:</b> Refer to section "Antenna Rule definitions" as well.	400.0	-
Q1M5	Resistor terminal net without VLABEL <b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".	-	-

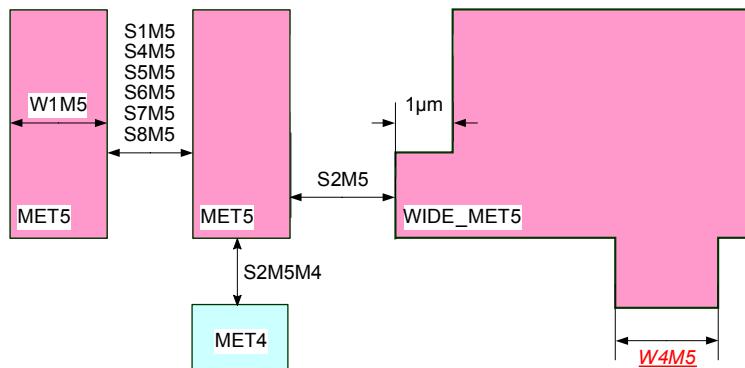


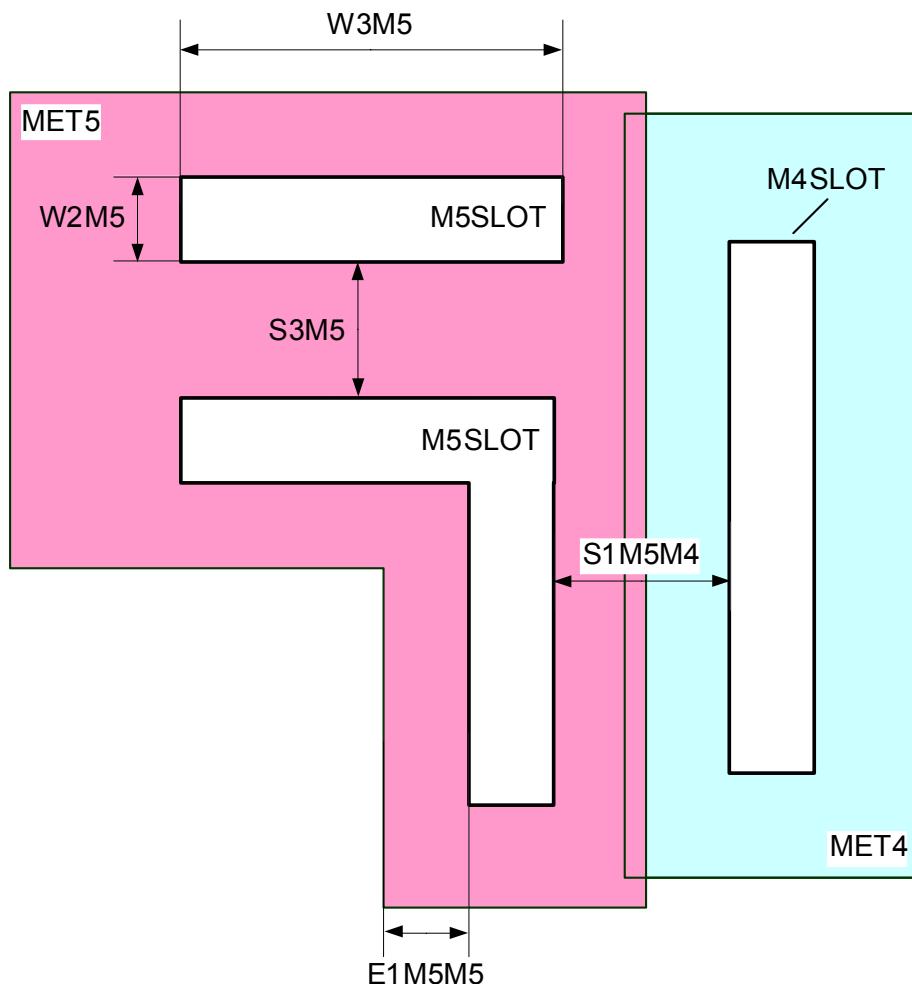
Figure 3.90 MET5

## 3. Layer and Device rules → 3.5 MET5 module → 3.5.1 Layer rules → M5SLOT

**M5SLOT**

Name	Description	Value	Unit
B1M5	All MET5 tracks > 35µm wide to be slotted (except Pads)	-	-
W2M5	Minimum M5SLOT width	0.6	µm
W3M5	Minimum M5SLOT length	20.0	µm
	<b>Note:</b> If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3M5	Minimum M5SLOT spacing/notch	10.0	µm
S1M5M4	Minimum M5SLOT spacing to M4SLOT	2.0	µm
	<b>Note:</b> M5SLOT is not allowed over M4SLOT.		
E1M5M5	Minimum MET5 enclosure of M5SLOT	10.0	µm
	<b>Note:</b> M5SLOT without MET5 is not allowed.		

**Note:** Insert M5SLOTS in direction of current flow.



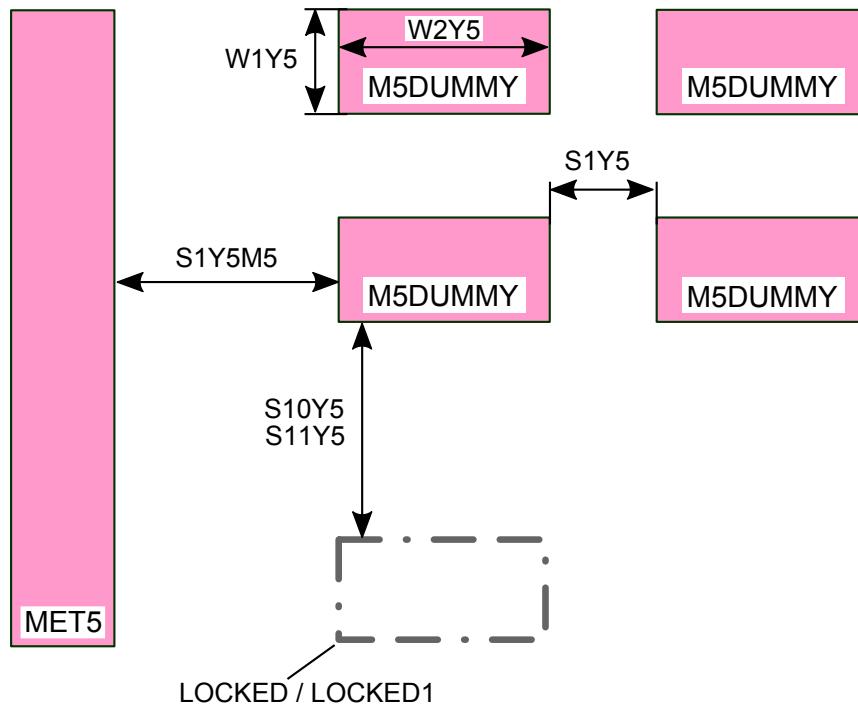
**Figure 3.91 M5SLOT**

## 3. Layer and Device rules → 3.5 MET5 module → 3.5.1 Layer rules → M5DUMMY

**M5DUMMY**

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1Y5	Only rectangular M5DUMMY is allowed	-	-
B2Y5	M5DUMMY overlap of MET5 is not allowed	-	-
B3Y5V4	M5DUMMY overlap of VIA4 is not allowed	-	-
B3Y5VT	M5DUMMY overlap of VIATP is not allowed	-	-
W1Y5	Minimum M5DUMMY width	2.0	µm
W2Y5	Maximum M5DUMMY edge length	20.0	µm
S1Y5	Minimum M5DUMMY spacing	2.0	µm
S10Y5	Minimum M5DUMMY spacing to LOCKED	4.0	µm
S11Y5	Minimum M5DUMMY spacing to LOCKED1	4.0	µm
S1Y5M5	Minimum M5DUMMY spacing to MET5	4.0	µm

**Figure 3.92 M5DUMMY****3.5.2 Device rules****rm5**

Name	Description	Value	Unit
B2M5	VIA4 is not allowed within rm5	-	-
B3M5	VIATP is not allowed within rm5 <b>Note:</b> Valid if module METMID is selected	-	-
B5M5	VIATPL is not allowed within rm5 <b>Note:</b> Valid if module METTHK is selected and not METMID	-	-

3. Layer and Device rules → 3.5 MET5 module → 3.5.2 Device rules → rm5

**Note:** rm5 resistor definition: MET5 and M5VERIFY.

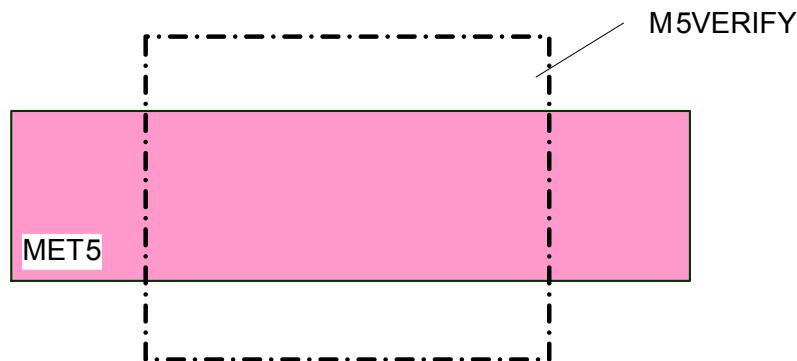


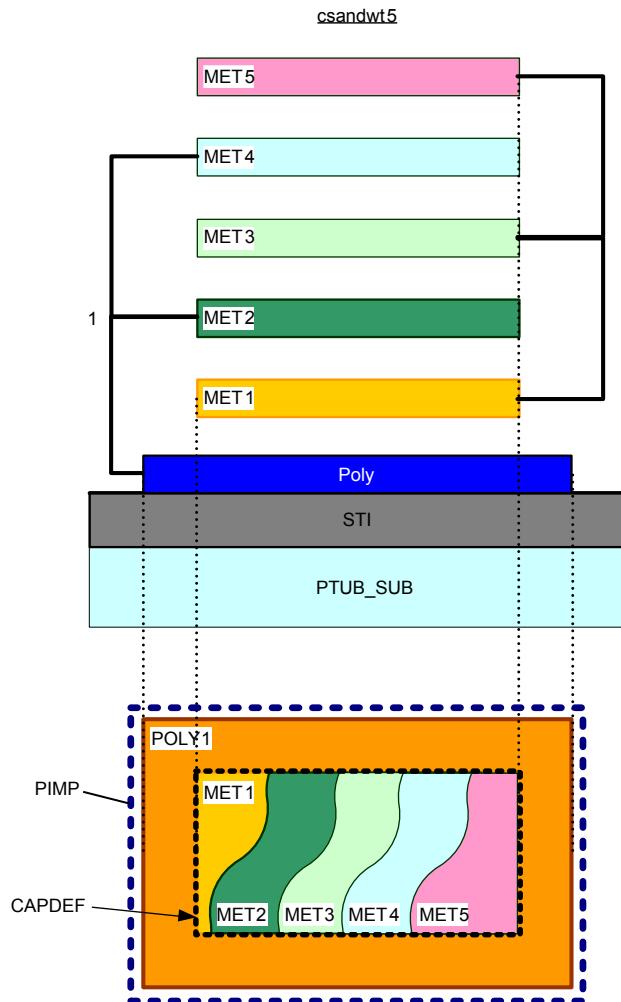
Figure 3.93 rm5

3. Layer and Device rules → 3.5 MET5 module → 3.5.2 Device rules → csandwt5

### csandwt5

Name	Description	Value	Unit
B19P1	csandwt5 overlap of DTI is not allowed	-	-

**Note:** CAPDEF is necessary for csandwt5.



**Figure 3.94** csandwt5

### cif5

The layout of the device cif5 is fixed and must not be changed. A single cell instance has an area of  $7.04\mu\text{m} \times 25.00\mu\text{m}$ .

**Note:** CAPDEF is necessary for cif5.

**Note:** Higher values may be achieved by the formation of arrays.

### cif5a

The layout of the device cif5a is fixed and must not be changed. A single cell instance has an area of  $4.48\mu\text{m} \times 10.80\mu\text{m}$ .

**Note:** CAPDEF is necessary for cif5a.

**Note:** Higher values may be achieved by the formation of arrays.

### csf5, csf5a

The layout of the devices csf5 and csf5a are fixed and must not be changed. For csf5, a single cell instance has an area of  $4.48\mu\text{m} \times 10.80\mu\text{m}$ . For csf5a, a single cell instance has an area of  $5.76\mu\text{m} \times 11.10\mu\text{m}$ .

3. Layer and Device rules → 3.5 MET5 module→ 3.5.2 Device rules→ csf5, csf5a

**Note:** CAPDEF is necessary for csf5 and csf5a .

**Note:** Higher values may be achieved by the formation of arrays.

3. Layer and Device rules → 3.6 METMID module

## 3.6 METMID module

### 3.6.1 Layer rules

#### VIATP

Name	Description	Value	Unit
B1VT	VIATP must be covered by METTP	-	-
B1VTM2	VIATP must be covered by MET2  <b>Note:</b> Valid if MET3 module is not selected	-	-
B1VTM3	VIATP must be covered by MET3  <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected	-	-
B1VTM4	VIATP must be covered by MET4  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	-	-
B1VTM5	VIATP must be covered by MET5  <b>Note:</b> Valid if MET5 module is selected	-	-
W1VT	Fixed VIATP size	0.36 x 0.36	μm x μm
S1VT	Minimum VIATP spacing	0.35	μm
E1M2VT	Minimum MET2 enclosure of VIATP  <b>Note:</b> Valid if MET3 module is not selected	0.01	μm
E1M3VT	Minimum MET3 enclosure of VIATP  <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected	0.01	μm
E1M4VT	Minimum MET4 enclosure of VIATP  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.01	μm
E1M5VT	Minimum MET5 enclosure of VIATP  <b>Note:</b> Valid if MET5 module is selected	0.01	μm
E1MTVT	Minimum METTP enclosure of VIATP	0.09	μm
E2M2VT	Minimum MET2 enclosure of VIATP (in one direction of VIATP corner)  <b>Note:</b> Valid if MET3 module is not selected	0.06	μm
E2M3VT	Minimum MET3 enclosure of VIATP (in one direction of VIATP corner)  <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected	0.06	μm
E2M4VT	Minimum MET4 enclosure of VIATP (in one direction of VIATP corner)  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.06	μm
E2M5VT	Minimum MET5 enclosure of VIATP (in one direction of VIATP corner)  <b>Note:</b> Valid if MET5 module is selected	0.06	μm
R1VT	Maximum ratio of VIATP area to connected GATE area	20.0	-

**Note:** Bond pads require interconnecting vias between the metal layers. See section "Bond Pad".

## 3. Layer and Device rules → 3.6 METMID module→ 3.6.1 Layer rules→ VIATP

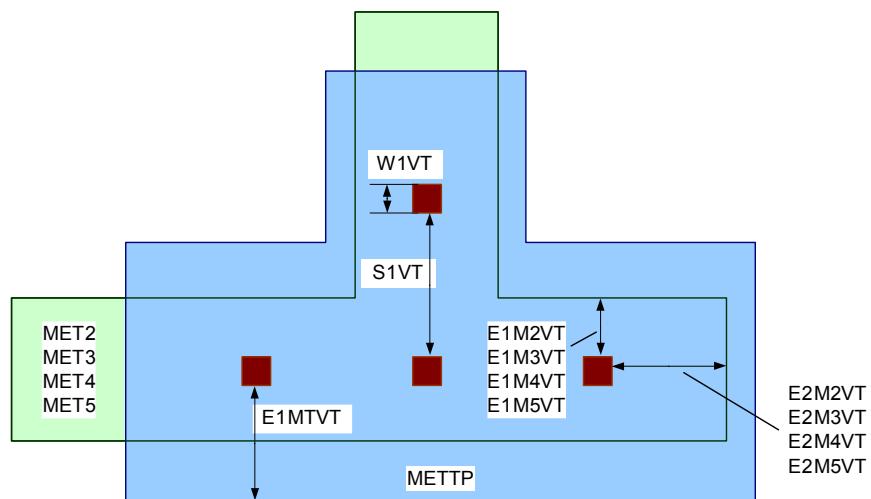


Figure 3.95 VIATP

## 3. Layer and Device rules → 3.6 METMID module→ 3.6.1 Layer rules→ METTP

**METTP**

Name	Description	Value	Unit
B1MTM2	METTP overlap of MET2 is not allowed (different net, tag_#, MET2, METTP difference >300V)  <b>Note:</b> Valid if MET3 module is not selected	-	-
B1MTM3	METTP overlap of MET3 is not allowed (different net, tag_#, MET3, METTP difference >300V)  <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected	-	-
B1MTM4	METTP overlap of MET4 is not allowed (different net, tag_#, MET4, METTP difference >300V)  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected	-	-
B1MTM5	METTP overlap of MET5 is not allowed (different net, tag_#, MET5, METTP difference >300V)  <b>Note:</b> Valid if MET5 module is selected	-	-
W1MT	Minimum METTP width	0.44	μm
<b><u>W4MT</u></b>	Minimum METTP width joining wide METTP track (> 35 μm)	10.0	μm
	<b>Note:</b> No slot is allowed opposite the join. It is recommended to maintain this width for at least 1 μm from the main track prior to narrowing.		
<b><u>W5MT</u></b>	Maximum METTP region size	17.0 x 17.0	μm x μm
	<b>Note:</b> METTP regions are defined as METTP shapes (single METTP shapes or a bundle of METTP shapes, with width > 2.0μm inclusive of the spacing if the spacing is <= 1.0μm) without any other metal layer above. For further information and design guidelines, please refer to the application note about <a href="#">IMD popping</a> on "my X-FAB".  <b>Note:</b> Not checked with standard DRC, option for check is available.		
S1MT	Minimum METTP spacing/notch	0.46	μm
S4MT	Minimum METTP spacing (different net, tag_#, difference >25V ≤ 60V)	0.5	μm
	<b>Note:</b> Valid for spacing of all METTP shapes with label tag_# to all METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of >25V ≤ 60V. Refer to the design related guideline "Voltage class definitions".		
S5MT	Minimum METTP spacing (different net, tag_#, difference >60V ≤100V)	0.6	μm
	<b>Note:</b> Valid for spacing of all METTP shapes with label tag_# to all METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of >60V ≤ 100V. Refer to the design related guideline "Voltage class definitions".		
S6MT	Minimum METTP spacing (different net, tag_#, difference >100V ≤200V)	0.8	μm
	<b>Note:</b> Valid for spacing to all METTP shapes with label tag_# to all METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of >100V ≤ 200V. Refer to the design related guideline "Voltage class definitions".		
S7MT	Minimum METTP spacing (different net, tag_#, difference >200V ≤300V)	1.2	μm
	<b>Note:</b> Valid for spacing to all METTP shapes with label tag_# to all METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of >200V ≤ 300V. Refer to the design related guideline "Voltage class definitions".		
S8MT	Minimum METTP spacing (different net, tag_#, difference >300V)	1.6	μm
	<b>Note:</b> Valid for spacing to all METTP shapes with label tag_# to all METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of > 300V. Refer to the design related guideline "Voltage class definitions".		
S2MT	Minimum METTP spacing to WIDE_METTP	0.6	μm
S2MTM2	Minimum METTP spacing to MET2 (different net, tag_#, difference >300V)	1.6	μm
	<b>Note:</b> Valid if MET3 module is not selected		
	<b>Note:</b> Valid if the voltage difference between MET2, METTP is >300V.		
	<b>Note:</b> Valid for spacing of all METTP/MET2 shapes with label tag_# to all MET2/METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		



## 3. Layer and Device rules → 3.6 METMID module→ 3.6.1 Layer rules→ METTP

Name	Description	Value	Unit
S2MTM3	Minimum METTP spacing to MET3 (different net, tag_#, difference >300V)	1.6	µm
	<b>Note:</b> Valid if the voltage difference between MET3, METTP is >300V.		
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected		
S2MTM4	<b>Note:</b> Valid for spacing of all METTP/MET3 shapes with label tag_# to all MET3/METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	Minimum METTP spacing to MET4 (different net, tag_#, difference >300V)	1.6	µm
	<b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected		
S2MTM5	<b>Note:</b> Valid if the voltage difference between MET4, METTP is >300V.		
	<b>Note:</b> Valid for spacing of all METTP/MET4 shapes with label tag_# to all MET4/METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	Minimum METTP spacing to MET5 (different net, tag_#, difference >300V)	1.6	µm
A1MT	<b>Note:</b> Valid if MET5 module is selected		
	<b>Note:</b> Valid if the voltage difference between MET5, METTP is >300V.		
	<b>Note:</b> Valid for spacing of all METTP/MET5 shapes with label tag_# to all MET5/METTP shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
R1MT	Minimum METTP area	0.562	µm <sup>2</sup>
R2MT	Minimum ratio of METTP area to EXTENT area	30.0	%
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
R1MTP1	Maximum ratio of METTP area to connected GATE area	400.0	-
	<b>Note:</b> Refer to section "Antenna Rule definitions" as well.		
R2MTP1	Maximum ratio of METTP area to connected GATE area	400.0	-
	<b>Note:</b> Refer to section "Antenna Rule definitions" as well.		
Q1MT	Resistor terminal net without VLABEL	-	-
	<b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".		

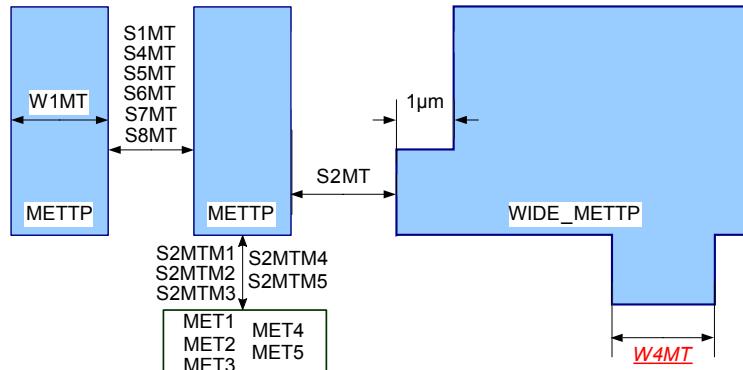


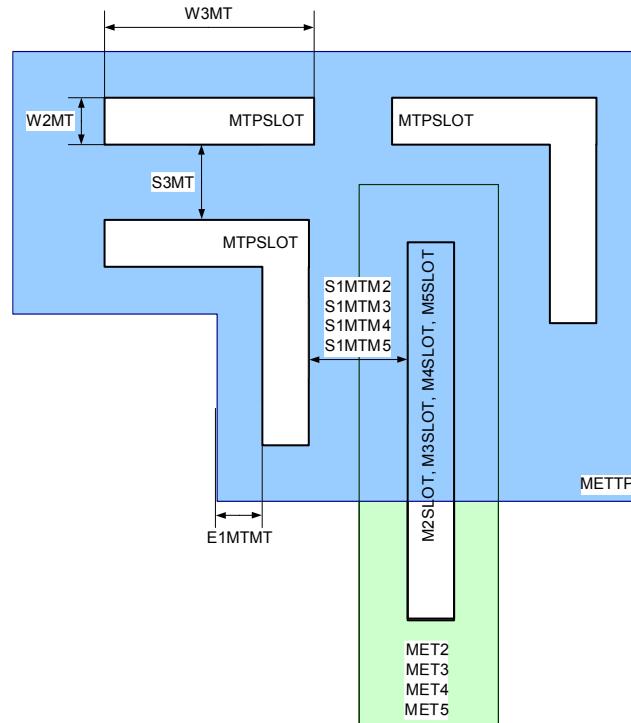
Figure 3.96 METTP

## 3. Layer and Device rules → 3.6 METMID module→ 3.6.1 Layer rules→ MTPSLOT

**MTPSLOT**

Name	Description	Value	Unit
B1MT	All METTP tracks > 35µm wide to be slotted (except Pads)	-	-
W2MT	Minimum MTPSLOT width	0.6	µm
W3MT	Minimum MTPSLOT length	20.0	µm
	<b>Note:</b> If this rule cannot be adhered to, it is suggested that the track in question is drawn as two narrow parallel tracks.		
S3MT	Minimum MTPSLOT spacing/notch	10.0	µm
S1MTM2	Minimum MTPSLOT spacing to M2SLOT <b>Note:</b> Valid if MET3 module is not selected <b>Note:</b> MTPSLOT is not allowed over M2SLOT.	2.0	µm
S1MTM3	Minimum MTPSLOT spacing to M3SLOT <b>Note:</b> MTPSLOT is not allowed over M3SLOT. <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected	2.0	µm
S1MTM4	Minimum MTPSLOT spacing to M4SLOT <b>Note:</b> MTPSLOT is not allowed over M4SLOT. <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected	2.0	µm
S1MTM5	Minimum MTPSLOT spacing to M5SLOT <b>Note:</b> MTPSLOT is not allowed over M5SLOT. <b>Note:</b> Valid if MET5 module is selected	2.0	µm
E1MTMT	Minimum METTP enclosure of MTPSLOT <b>Note:</b> MTPSLOT without METTP is not allowed.	10.0	µm

**Note:** Insert MTPSLOTs in direction of current flow.



**Figure 3.97 MTPSLOT**

3. Layer and Device rules → 3.6 METMID module→ 3.6.1 Layer rules→ MTPDUMMY

## MTPDUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1YT	Only rectangular MTPDUMMY is allowed	-	-
B2YT	MTPDUMMY overlap of METTP is not allowed	-	-
B3YTBD	MTPDUMMY overlap of BDO is not allowed  <b>Note:</b> Only valid if module METTHK is not selected.	-	-
B3YTVC	MTPDUMMY overlap of VIACOP is not allowed  <b>Note:</b> Only valid if module METTHK is not selected.	-	-
B3YTVL	MTPDUMMY overlap of VIATPL is not allowed	-	-
B3YTVT	MTPDUMMY overlap of VIATP is not allowed	-	-
W1YT	Minimum MTPDUMMY width	2.0	µm
W2YT	Maximum MTPDUMMY edge length	20.0	µm
S1YT	Minimum MTPDUMMY spacing	2.0	µm
S1YTMT	Minimum MTPDUMMY spacing to METTP	2.0	µm
S10YT	Minimum MTPDUMMY spacing to LOCKED	2.0	µm
S11YT	Minimum MTPDUMMY spacing to LOCKED1  <b>Note:</b> Only valid if module MET5 is not selected.	2.0	µm
S12YT	Minimum MTPDUMMY spacing to LOCKED2  <b>Note:</b> Only valid if module MET4 is not selected.	2.0	µm
S13YT	Minimum MTPDUMMY spacing to LOCKED3  <b>Note:</b> Only valid if module MET3 is not selected.	2.0	µm
S1YTBD	Minimum MTPDUMMY spacing to BDO  <b>Note:</b> Only valid if module METTHK is not selected.	5.0	µm
S1YTPA	Minimum MTPDUMMY spacing to PAD	5.0	µm

## 3. Layer and Device rules → 3.6 METMID module → 3.6.1 Layer rules → MTPDUMMY

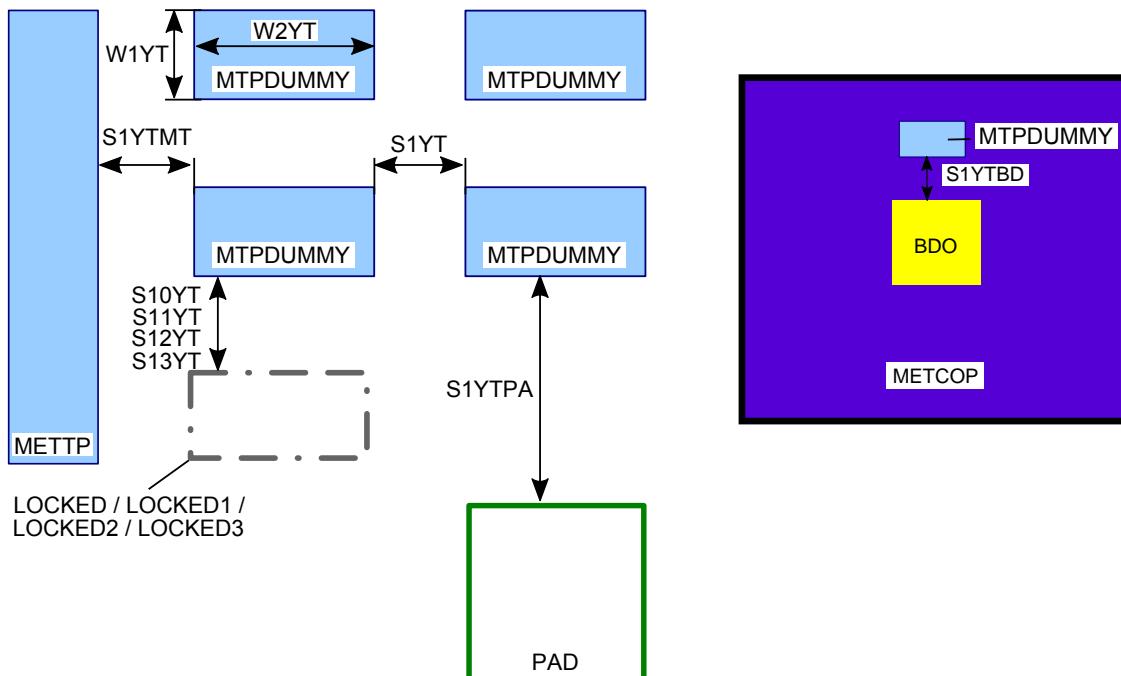


Figure 3.98 MTPDUMMY

## 3.6.2 Device rules

## rmtp

Name	Description	Value	Unit
B2MT	VIATP is not allowed within rmtp	-	-
B3MT	VIATPL is not allowed within rmtp <b>Note:</b> Valid if METTHK is selected.	-	-

**Note:** rmtp resistor definition: METTP and MTPVERIFY.

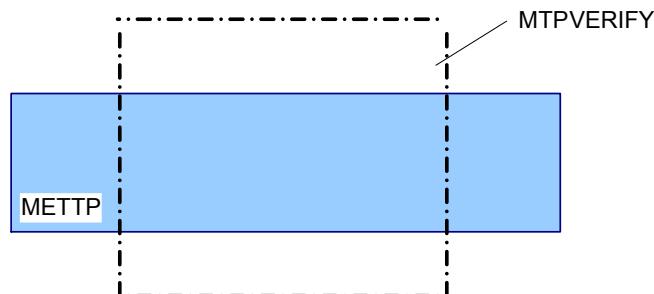


Figure 3.99 rmtp

## cift4, cift5, cift6

The layout of the devices cift4, cift5 and cift6 is fixed and must not be changed. A single cell instance has an area of 7.04µm x 25.84µm.

**Note:** Higher values may be achieved by the formation of arrays.

**Note:** CAPDEF is necessary for cift4, cift5 and cift6.

3. Layer and Device rules → 3.6 METMID module→ 3.6.2 Device rules→ cift4a, cift5a, cift...

### **cift4a, cift5a, cift6a**

The layouts of the devices cift4a, cift5a and cift6a are fixed and must not be changed. A single cell instance has an area of 4.48 µm x 11.04 µm.

**Note:** CAPDEF is necessary for cift4a, cift5a and cift6a.

**Note:** Higher values may be achieved by the formation of arrays.

### **csft4, csft4a, csft5, csft5a, csft6, csft6a**

The layouts of the devices csft4, csft4a, csft5, csft5a, csft6 and csft6a are fixed and must not be changed. For csft4, csft4b, csft5 and csft6, a single cell instance has an area of 4.48 µm x 10.80 µm. For csft4a, csft5a and csft6a, a single cell instance has an area of 5.76 µm x 11.10 µm.

**Note:** CAPDEF is necessary for csft4, csft4a, csft5, csft5a, csft6 and csft6a.

**Note:** Higher values may be achieved by the formation of arrays.

3. Layer and Device rules → 3.7 METTHK module

## 3.7 METTHK module

### 3.7.1 Layer rules

#### VIATPL

Name	Description	Value	Unit
B1VL	VIATPL must be covered by METTPL	-	-
B1VLM3	VIATPL must be covered by MET3  <b>Note:</b> Valid if module MET3 and METTHK are selected and not (MET4 or METMID)	-	-
B1VLM4	VIATPL must be covered by MET4  <b>Note:</b> Valid if module MET4 is selected and not MET5 or METMID	-	-
B1VLM5	VIATPL must be covered by MET5  <b>Note:</b> Valid if module MET5 is selected and not METMID	-	-
B1VLMT	VIATPL must be covered by METTP  <b>Note:</b> Valid if METMID module is selected.	-	-
W1VL	Fixed VIATPL size	0.5 x 0.5	μm x μm
S1VL	Minimum VIATPL spacing	0.45	μm
E1M3VL	Minimum MET3 enclosure of VIATPL  <b>Note:</b> Valid if module MET3 and METTHK are selected and not (MET4 or METMID)	0.5	μm
E1M4VL	Minimum MET4 enclosure of VIATPL  <b>Note:</b> Valid if module MET4 is selected and not MET5 or METMID	0.5	μm
E1M5VL	Minimum MET5 enclosure of VIATPL  <b>Note:</b> Valid if module MET5 is selected and not METMID	0.5	μm
E1MLVL	Minimum METTPL enclosure of VIATPL	0.5	μm
E1MTVL	Minimum METTP enclosure of VIATPL  <b>Note:</b> Valid if METMID module is selected.	0.5	μm
R1VL	Maximum ratio of VIATPL area to connected GATE area	20.0	-
R1VLVT	Maximum local VIATPL density  <b>Note:</b> Valid in any 200μm x 200μm window, step size 100μm.  <b>Note:</b> It is recommended to increase VIATPL spacing to at least 0.90μm (2X the minimum spacing rule S1VL)  <b>Note:</b> It is recommended to increase VIATPL spacing to at least 0.70μm (2X the minimum spacing rule S1VT)  <b>Note:</b> Valid only if maximum local VIATPL density > 21.0% in the same window.	19.0	%

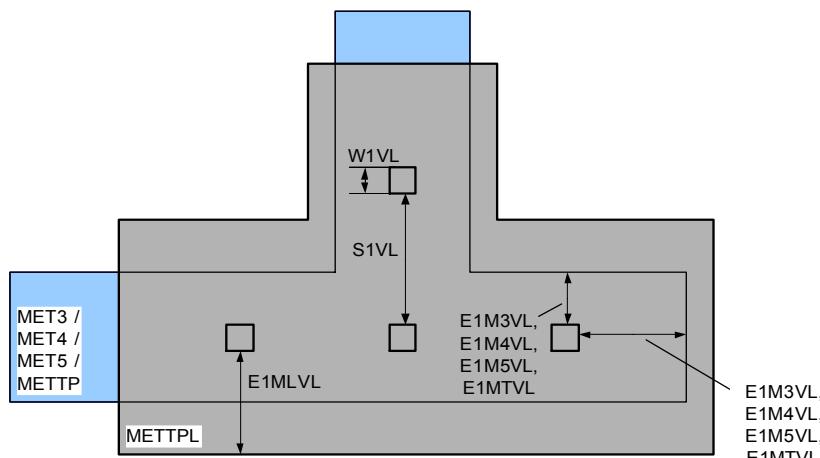


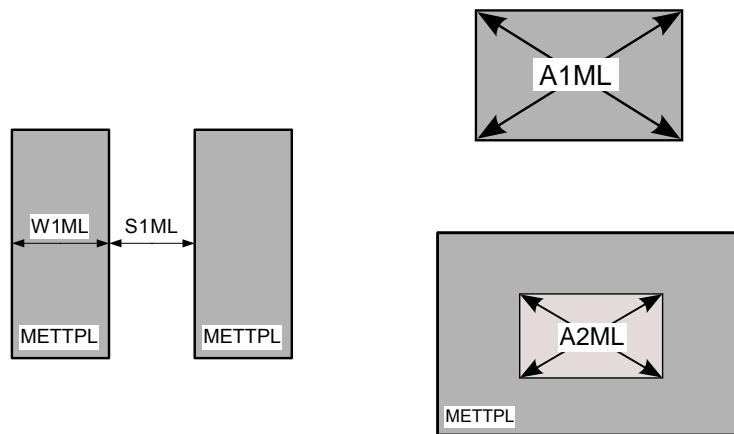
Figure 3.100 VIATPL

3. Layer and Device rules → 3.7 METTHK module→ 3.7.1 Layer rules→ METTPL

**METTPL**

Name	Description	Value	Unit
B1ML	METTPL tracks >35.0µm are not allowed (except Pads)	-	-
	<b>Note:</b> Dimensions greater than the limit above should be divided into parallel tracks.		
B1MLM3	METTPL overlap of MET3 is not allowed (different net, tag_#, MET3, METTPL difference >300V)	-	-
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected		
B1MLM4	METTPL overlap of MET4 is not allowed (different net, tag_#, MET4, METTPL difference >300V)	-	-
	<b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected		
B1MLM5	METTPL overlap of MET5 is not allowed (different net, tag_#, MET5, METTPL difference >300V)	-	-
	<b>Note:</b> Valid if MET5 module is selected		
W1ML	Minimum METTPL width	3.0	µm
S1ML	Minimum METTPL spacing/notch	2.5	µm
	Minimum METTPL spacing to MET3 (different net, tag_#, difference >300V)	1.6	µm
	<b>Note:</b> Valid if the voltage difference between METTPL, MET3 voltage is >300V.		
S1MLM3	<b>Note:</b> Valid for spacing of all MET3/METTPL shapes with label tag_# to all METTPL /MET3 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Valid if MET4 or METMID module is not selected.		
	Minimum METTPL spacing to MET4 (different net, tag_#, difference >300V)	1.6	µm
	<b>Note:</b> Valid if the voltage difference between METTPL, MET4 voltage is >300V.		
S1MLM4	<b>Note:</b> Valid for spacing of all MET4/METTPL shapes with label tag_# to all METTPL /MET4 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Valid if MET5 or METMID module is not selected.		
	Minimum METTPL spacing to MET5 (different net, tag_#, difference >300V)	1.6	µm
	<b>Note:</b> Valid if the voltage difference between METTPL, MET5 voltage is >300V.		
S1MLM5	<b>Note:</b> Valid for spacing of all MET5/METTPL shapes with label tag_# to all METTPL /MET5 shapes having other voltage classes and a difference between the numbers of the voltage class names of >300V. Refer to the design related guideline "Voltage class definitions".		
	<b>Note:</b> Valid if METMID module is not selected.		
A1ML	Minimum METTPL area	10.0	µm <sup>2</sup>
A2ML	Minimum METTPL enclosed area	18.0	µm <sup>2</sup>
<i>R1ML</i>	Minimum ratio of METTPL area to EXTENT area	30.0	%
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
<i>R2ML</i>	Maximum ratio of METTPL area to EXTENT area	65.0	%
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
R1MLP1	Maximum ratio of METTPL area to connected GATE area	200.0	-
	<b>Note:</b> Refer to section "Antenna Rule definitions" as well.		
R2MLP1	Maximum ratio of METTPL area to connected GATE area	200.0	-
	<b>Note:</b> Refer to section "Antenna Rule definitions" as well.		
Q1ML	Resistor terminal net without VLABEL	-	-
	<b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".		

3. Layer and Device rules → 3.7 METTHK module→ 3.7.1 Layer rules→ METTPL



**Figure 3.101** METTPL

3. Layer and Device rules → 3.7 METTHK module→ 3.7.1 Layer rules→ MTPLDUMMY

## MTPLDUMMY

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPLDUMMY and MTPLDUMMY). For further information, refer to the design related guideline "Dummy Pattern Generation".

Name	Description	Value	Unit
B1YL	Only rectangular MTPLDUMMY is allowed	-	-
B2YL	MTPLDUMMY overlap of METTPL is not allowed	-	-
B3YLB	MTPLDUMMY overlap of BDO is not allowed	-	-
B3YLV	MTPLDUMMY overlap of VIACOP is not allowed	-	-
B3YLV	MTPLDUMMY overlap of VIATPL is not allowed	-	-
W1YL	Minimum MTPLDUMMY width	5.0	μm
W2YL	Maximum MTPLDUMMY edge length	20.0	μm
S1YL	Minimum MTPLDUMMY spacing	5.0	μm
S10YL	Minimum MTPLDUMMY spacing to LOCKED	5.0	μm
S11YL	Minimum MTPLDUMMY spacing to LOCKED1	5.0	μm
	<b>Note:</b> Not valid if (MET4 and METMID) modules are selected or MET5 module is selected.		
S12YL	Minimum MTPLDUMMY spacing to LOCKED2	5.0	μm
	<b>Note:</b> Not valid if (MET3 and METMID) modules are selected or MET4 module is selected.		
S1YLB	Minimum MTPLDUMMY spacing to BDO	5.0	μm
S1YML	Minimum MTPLDUMMY spacing to METTPL	5.0	μm

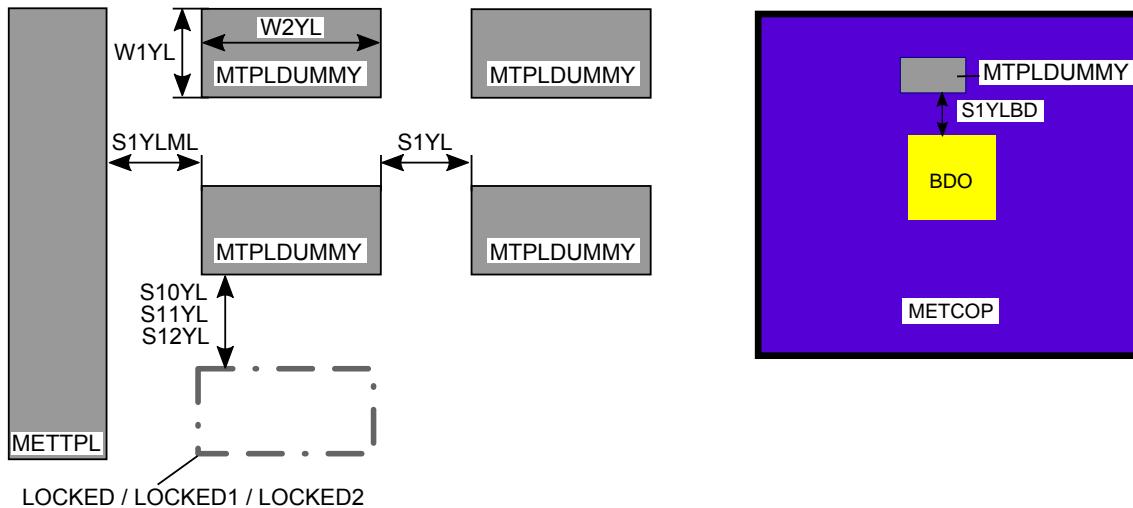


Figure 3.102 MTPLDUMMY

## 3.7.2 Device rules

### rmtpl

Name	Description	Value	Unit
B2ML	VIATPL is not allowed within rmtpl	-	-

**Note:** rmtpl resistor definition: METTPL and MLVERIFY.

3. Layer and Device rules → 3.7 METTHK module→ 3.7.2 Device rules→ rmtpl



**Figure 3.103** rmtpl

3. Layer and Device rules → 3.8 THKCOP module

## 3.8 THKCOP module

### 3.8.1 Layer rules

#### VIACOP

Name	Description	Value	Unit
B1VC	VIACOP must be covered by BDO	-	-
B1VCM <sub>L</sub>	VIACOP without METTPL is not allowed  <b>Note:</b> Valid if METTHK module is selected.	-	-
B1VCMT	VIACOP without METTP is not allowed  <b>Note:</b> Valid if METMID module is selected and not METTHK	-	-
B2VC	VIACOP must be a rectangle	-	-
B3ML	VIACOP is not allowed within rmtpl  <b>Note:</b> Valid if METTHK module is selected.	-	-
B4MT	VIACOP is not allowed within rmtpl  <b>Note:</b> Valid if METMID module is selected and not METTHK	-	-
W1VC	Minimum VIACOP width	7.0	μm
S1VC	Minimum VIACOP spacing	7.0	μm
E1MLVC	Minimum METTPL enclosure of VIACOP  <b>Note:</b> Valid if METTHK module is selected.	2.0	μm
E1MTVC	Minimum METTP enclosure of VIACOP  <b>Note:</b> Valid if METMID module is selected and not METTHK	2.0	μm

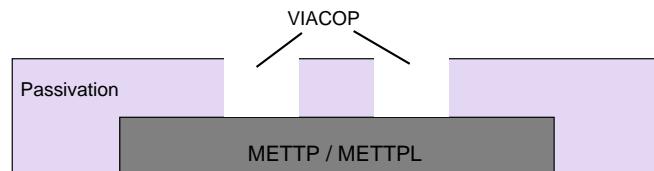
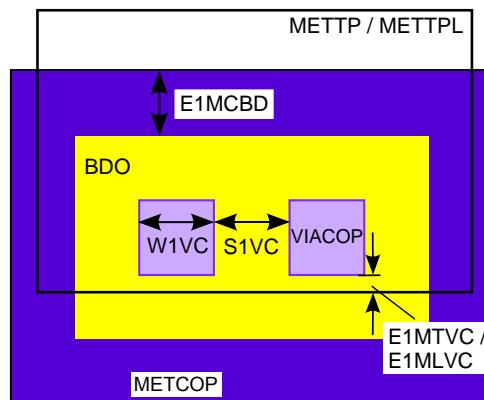


Figure 3.104 VIACOP

3. Layer and Device rules → 3.8 THKCOP module→ 3.8.1 Layer rules→ METCOP

## METCOP

Name	Description	Value	Unit
B1IBMC	NOPIM or PIMIDE marker are not allowed when METCOP is present	-	-
W1MC	Minimum METCOP width	10.0	μm
<u>W2MC</u>	Maximum METCOP trace length for width < 20μm	width x 100.0	μm
<u>W3MC</u>	Maximum METCOP trace length for width >= 20μm	width x 200.0	μm
S1MC	Minimum METCOP spacing / notch	10.0	μm
E1MCBD	Minimum METCOP enclosure of BDO	8.0	μm
<u>E1MCCE</u>	Minimum customer chip edge enclosure of METCOP	5.0	μm
<b>Note:</b> Customer chip is the polygon that represents the least enclosing rectangle of the database.			
A1MC	Maximum METCOP area	19.0	mm <sup>2</sup>
<u>R1MC</u>	Maximum ratio of METCOP area to EXTENT area	70.0	%
<b>Note:</b> Not checked with standard DRC, option for check is available.			
Q1MC	Resistor terminal net without VLABEL	-	-
<b>Note:</b> Resistor having VLABEL at one terminal only is not allowed. Refer to the design related guideline "Voltage class definitions".			

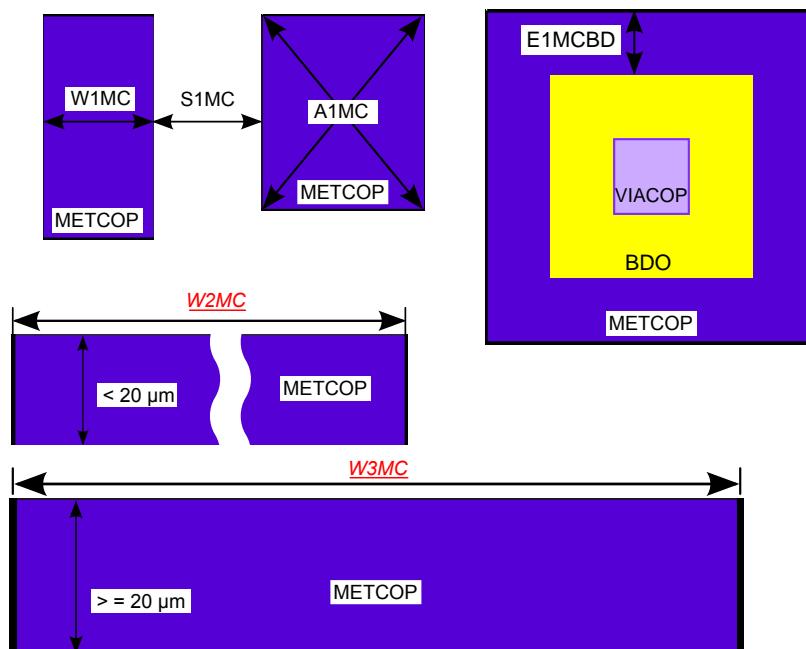
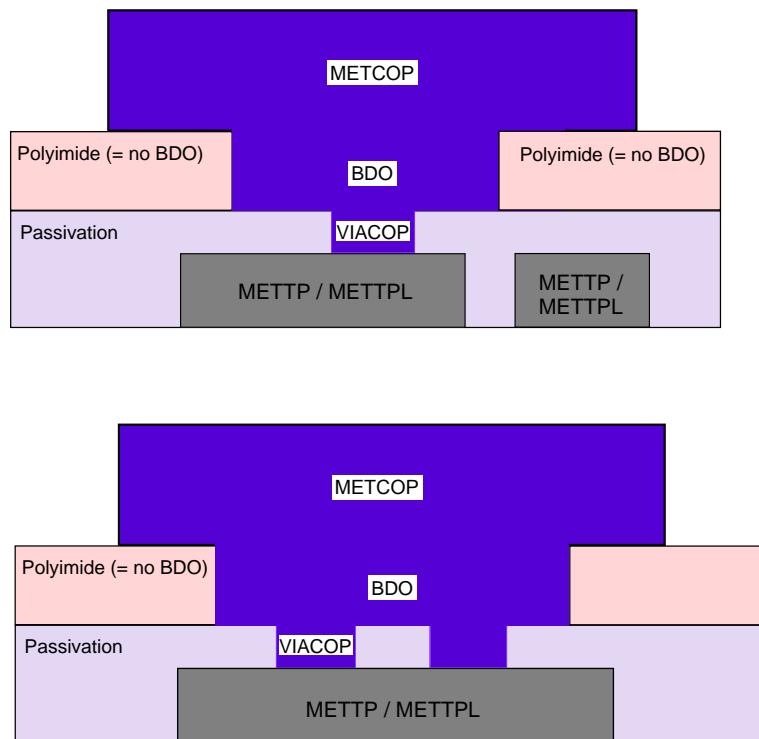


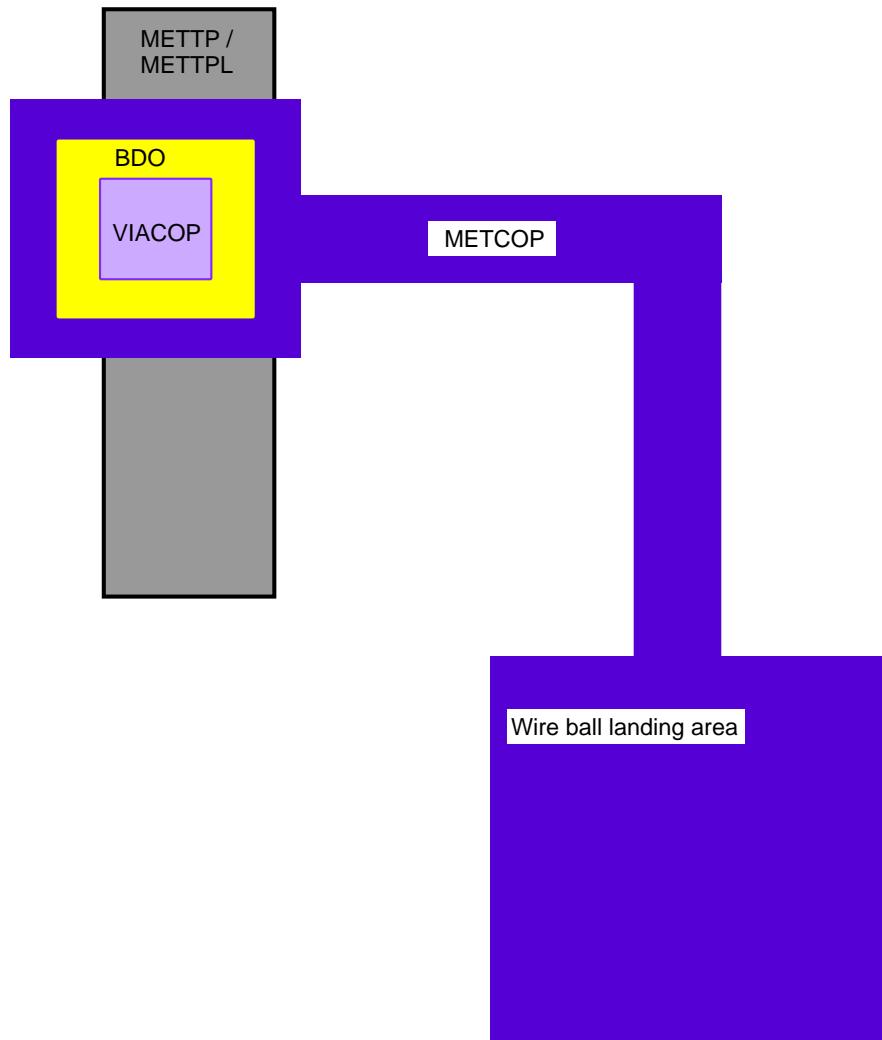
Figure 3.105 METCOP

## 3. Layer and Device rules → 3.8 THKCOP module→ 3.8.1 Layer rules→ METCOP



**Figure 3.106** METCOP related cross sectional diagram

3. Layer and Device rules → 3.8 THKCOP module→ 3.8.1 Layer rules→ METCOP



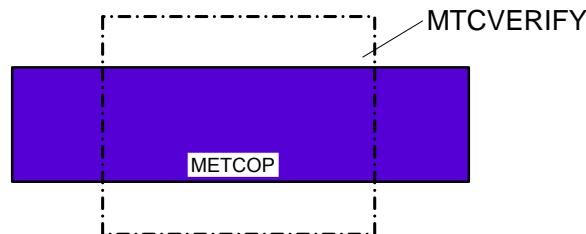
**Figure 3.107** METCOP wiring

### 3.8.2 Device rules

#### rmrdl

Name	Description	Value	Unit
B2MC	VIACOP is not allowed within rmrdl	-	-

**Note:** rmrdl resistor definition: METCOP and MTCVERIFY



**Figure 3.108** rmrdl

3. Layer and Device rules → 3.9 HRPOLY module

## 3.9 HRPOLY module

### 3.9.1 Layer rules

#### HRES

Name	Description	Value	Unit
B12HR	HRES overlap of DTI is not allowed	-	-
B1HR	HRES overlap of DIFF is not allowed	-	-
B3HR	PIMP overlap of HRES is not allowed	-	-
B4HR	POLY1 crossing HRES edge is not allowed	-	-
B6HR	NIMP crossing HRES edge is not allowed	-	-
W1HR	Minimum HRES width	0.44	μm
S1HR	Minimum HRES spacing/notch	0.44	μm
S1HRDF	Minimum HRES spacing to DIFF	0.32	μm
S1HRIN	Minimum HRES spacing to NIMP	0.44	μm
S1HRIP	Minimum HRES spacing to PIMP	0.44	μm
S1HRP1	Minimum HRES spacing to POLY1	0.32	μm
E1HRP1	Minimum HRES enclosure of POLY1	0.18	μm
A1HR	Minimum HRES area	5.0	μm <sup>2</sup>

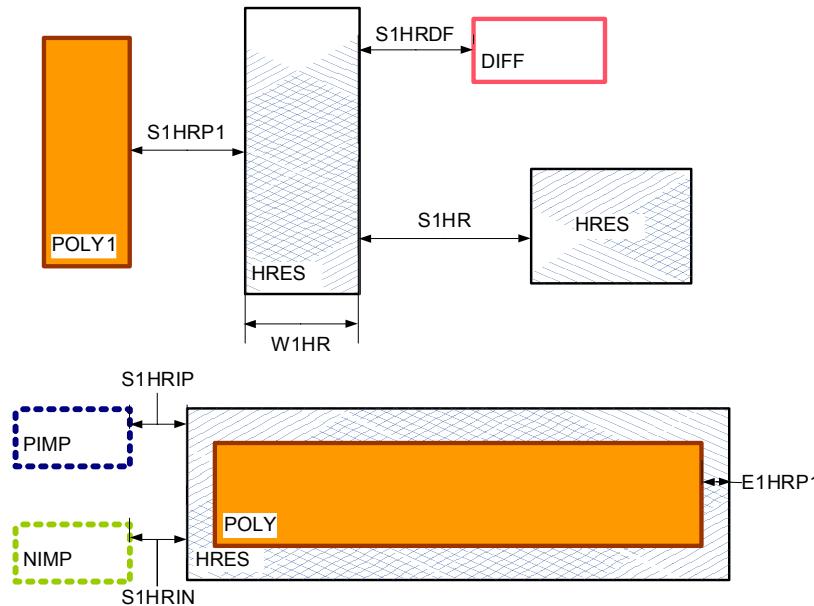


Figure 3.109 HRRES

### 3.9.2 Device rules

#### rnp1h, rnp1h\_3

Name	Description	Value	Unit
B11HR	rnp1h_3 overlap of rnw/rnw5 is not allowed	-	-
B2HR	NIMP overlap of rnp1h# (resistor body) is not allowed	-	-
B5HR	rnp1h# terminal without NIMP is not allowed	-	-
B7HR	MET1 overlap of rnp1h# (resistor body) is not allowed	-	-
B10HR	rnp1h_3 crossing NWELL edge is not allowed	-	-

## 3. Layer and Device rules → 3.9 HRPOLY module→ 3.9.2 Device rules→ rnp1h, rnp1h\_3

Name	Description	Value	Unit
W2HR	Minimum rnp1h# width	0.42	μm
W3HR	Minimum rnp1h# length	5.0	μm
S2INP1	Minimum NIMP (in SBLK) spacing to rnp1h#	0.18	μm
E2INP1	Minimum NIMP extension beyond POLY1	0.18	μm

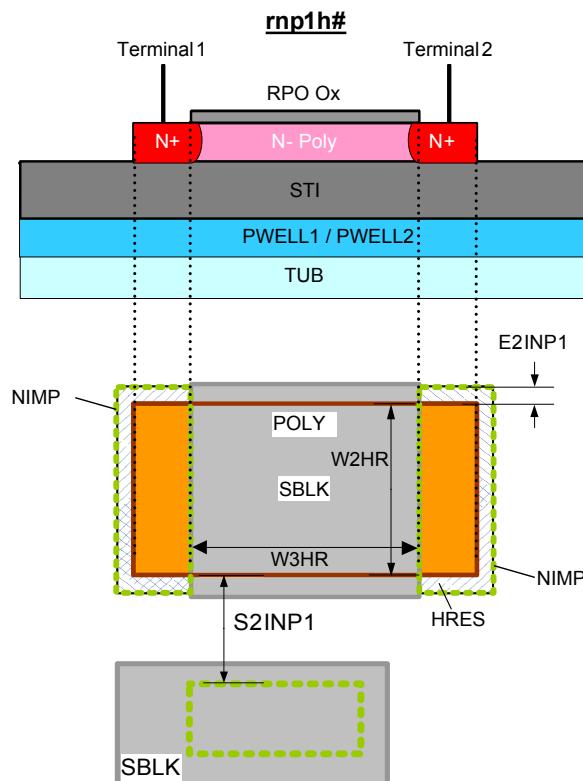
**Note:** Recommended minimum number of squares is L/W ≥ 5.

**Note:** Do not use dog-bone at the end of POLY1 resistor for CONT pickup.

**Note:** CONT array for POLY1 resistor should be a single column.

**Note:** For good matching or precise resistance value, it is strongly recommended to use larger HRES extension beyond POLY1 in resistor width direction (>=0.6μm).

**Note:** rnp1h\_3 device must be labeled "rnp1h\_3" using POLY1 (VERIFICATION) layer.



**Figure 3.110 rnp1h, rnp1h\_3**

3. Layer and Device rules → 3.10 MRPOLY module

## 3.10 MRPOLY module

### 3.10.1 Layer rules

#### MRES

Name	Description	Value	Unit
B10MR	MRES overlap of DTI is not allowed	-	-
B1MR	MRES overlap of DIFF is not allowed	-	-
B2MR	MRES without SBLK is not allowed	-	-
B3MR	MRES overlap of NIMP or PIMP is not allowed	-	-
B4MR	HRES overlap of MRES is not allowed	-	-
W1MR	Minimum MRES width	0.44	µm
S1MR	Minimum MRES spacing/notch	0.44	µm
S1MRDF	Minimum MRES spacing to DIFF	0.32	µm
S1MRP1	Minimum MRES spacing to POLY1	0.32	µm
A1MR	Minimum MRES area	0.3844	µm <sup>2</sup>

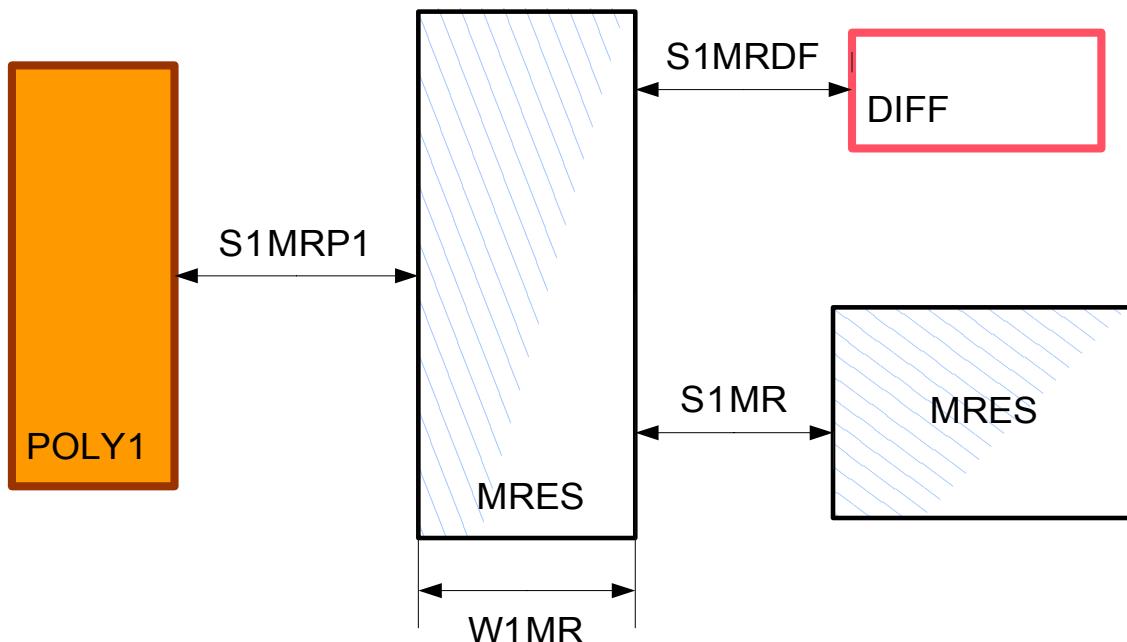


Figure 3.111 MRES

### 3.10.2 Device rules

#### rpp1k1, rpp1k1\_3

Name	Description	Value	Unit
B7MR	rpp1k1_3 overlap of rnw/rnw5 is not allowed	-	-
B6MR	rpp1k1_3 crossing NWELL edge is not allowed	-	-
W16P1	Minimum rpp1k1# width	0.42	µm
S3INP1	Minimum NIMP spacing to rpp1k1 or rpp1k1_ext	0.26	µm
<b>Note:</b> The rpp1k1_ext area is defined as the (POLY1 and SBLK) area outside the resistor at the resistor terminals (see drawing).			
E1MRP1	Minimum MRES extension beyond rpp1k1#	0.18	µm
E1SBMR	Fixed SBLK extension beyond MRES in direction of POLY1	0.22	µm



## 3. Layer and Device rules → 3.10 MRPOLY module→ 3.10.2 Device rules→ rpp1k1, rpp1k1\_3

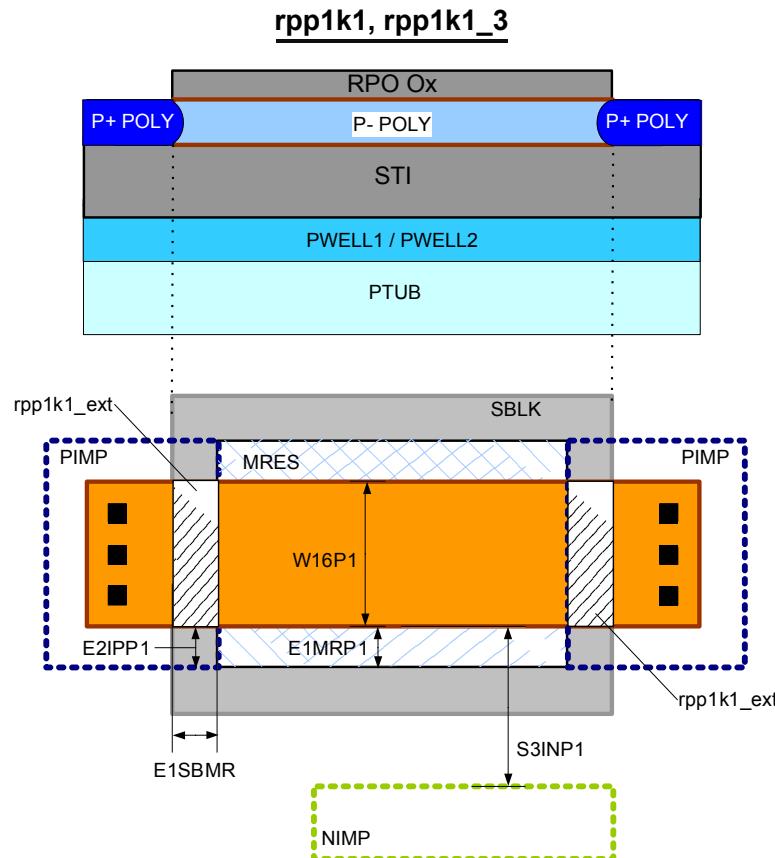
Name	Description	Value	Unit
E2IPP1	Minimum PIMP extension beyond rpp1k1_ext  <b>Note:</b> The rpp1k1_ext area is defined as the (POLY1 and SBLK) area outside the resistor at the resistor terminals (see drawing).	0.18	μm

**Note:** CONT array for rpp1k1 and rpp1k1\_3 resistors should be a single column.

**Note:** Do not use dog-bone at the end of rpp1k1 and rpp1k1\_3 resistors for CONT pickup.

**Note:** Recommended minimum number of squares is L/W ≥ 5.

**Note:** rpp1k1, rpp1k1\_3 resistor definition: POLY1 and MRES



**Figure 3.112 rpp1k1, rpp1k1\_3**

3. Layer and Device rules → 3.10 MRPOLY module→ 3.10.2 Device rules→ rpp1k1a, rpp1k1a\_3

### rpp1k1a, rpp1k1a\_3

Name	Description	Value	Unit
B9MR	rpp1k1a_3 overlap of rnw/rnw5 is not allowed	-	-
B8MR	rpp1k1a_3 crossing NWELL edge is not allowed	-	-
W16P1	Minimum rpp1k1# width	0.42	μm
S4INP1	Minimum NIMP spacing to rpp1k1a or rpp1k1a_ext <b>Note:</b> The rpp1k1a_ext area is defined as the (POLY1 and SBLK) area outside the resistor at the resistor terminals (see drawing).	0.26	μm
S6P1DF	Minimum POLY1 spacing to DIFF	1.3	μm
E1MRP1	Minimum MRES extension beyond rpp1k1#	0.18	μm
E1SBMR	Fixed SBLK extension beyond MRES in direction of POLY1	0.22	μm
E3IPP1	Minimum PIMP extension beyond rpp1k1a_ext <b>Note:</b> The rpp1k1a_ext area is defined as the (POLY1 and SBLK) area outside the resistor at the resistor terminals (see drawing).	0.18	μm

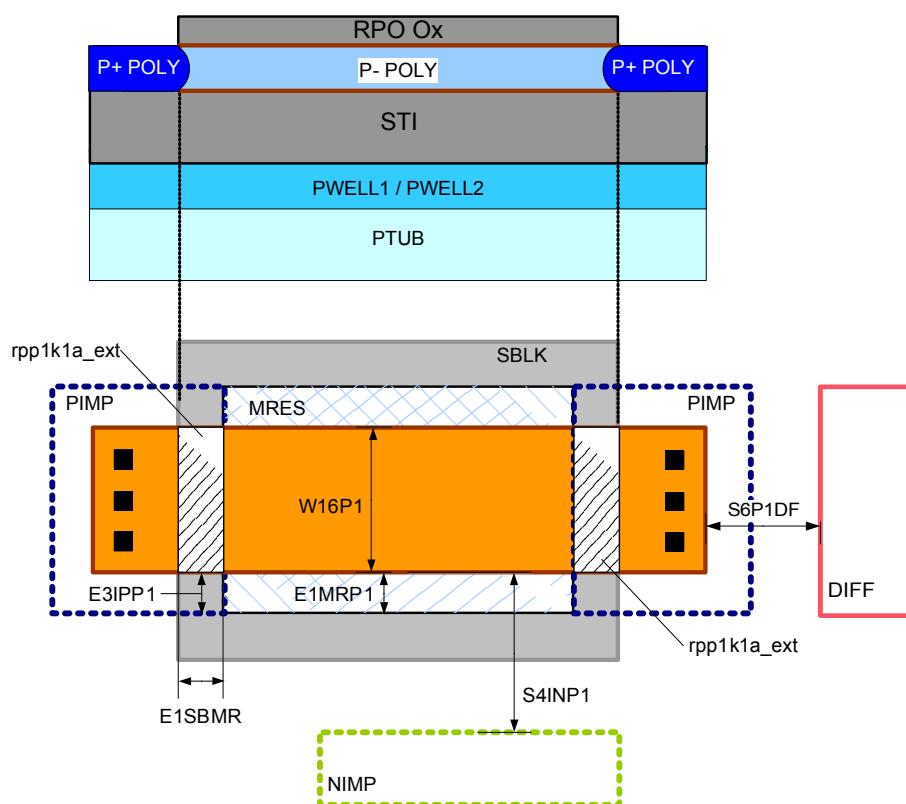
**Note:** Recommended minimum number of squares is L/W ≥ 5.

**Note:** CONT array for rpp1k1a and rpp1k1a\_3 resistors should be a single column.

**Note:** Do not use dog-bone at the end of rpp1k1a and rpp1k1a\_3 resistors for CONT pickup.

**Note:** rpp1k1a, rpp1k1a\_3 resistor definition: POLY1 and MRES

### rpp1k1a, rpp1k1a\_3



**Figure 3.113 rpp1k1a, rpp1k1a\_3**

3. Layer and Device rules → 3.11 DTI module

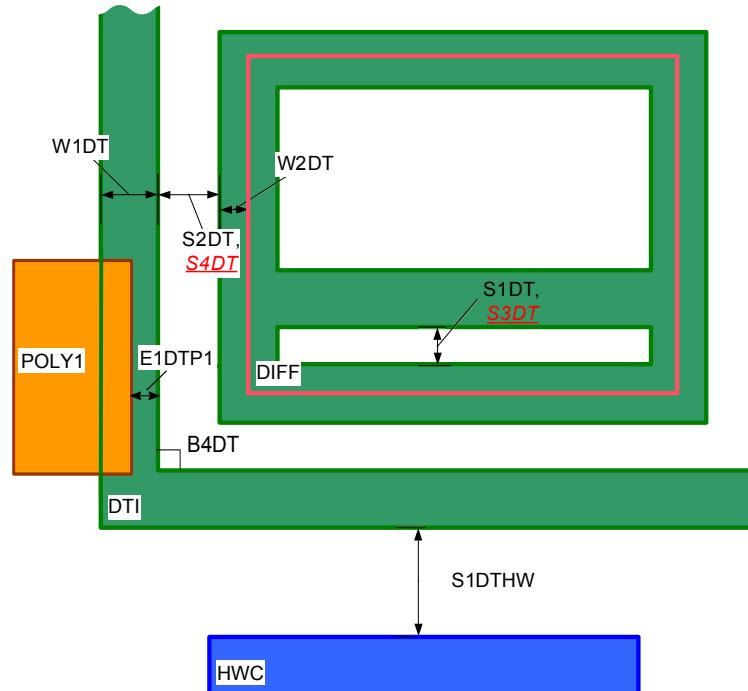
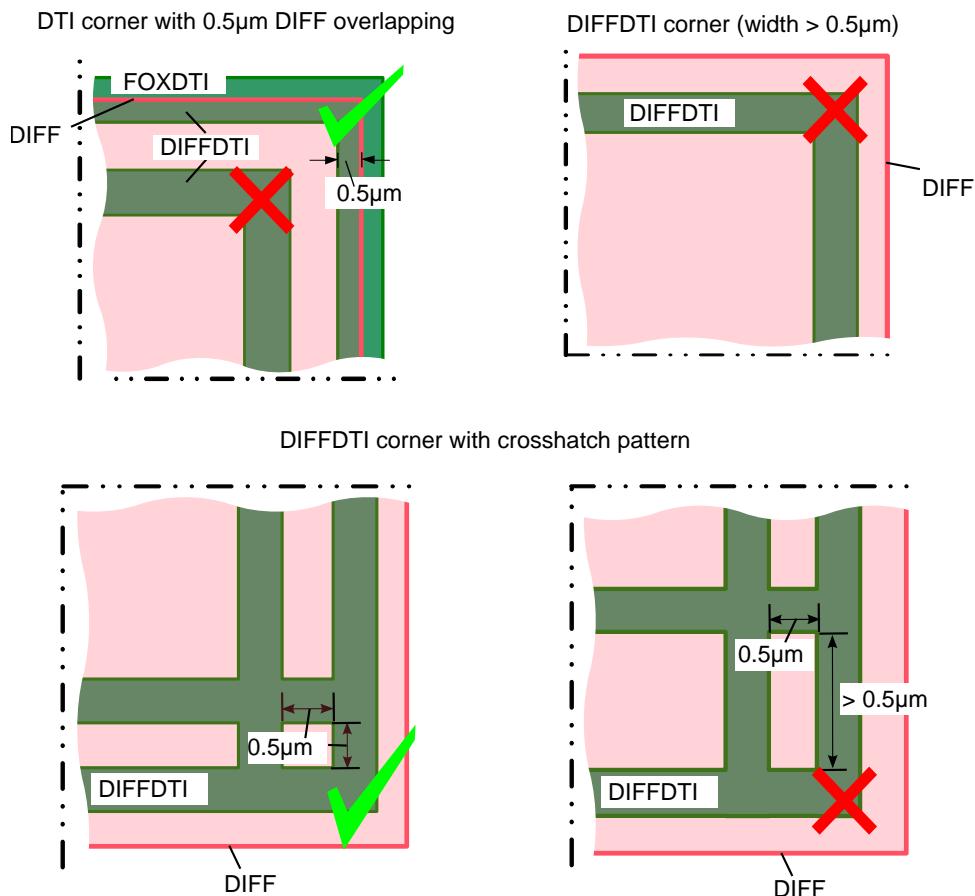
## 3.11 DTI module

### 3.11.1 Layer rules

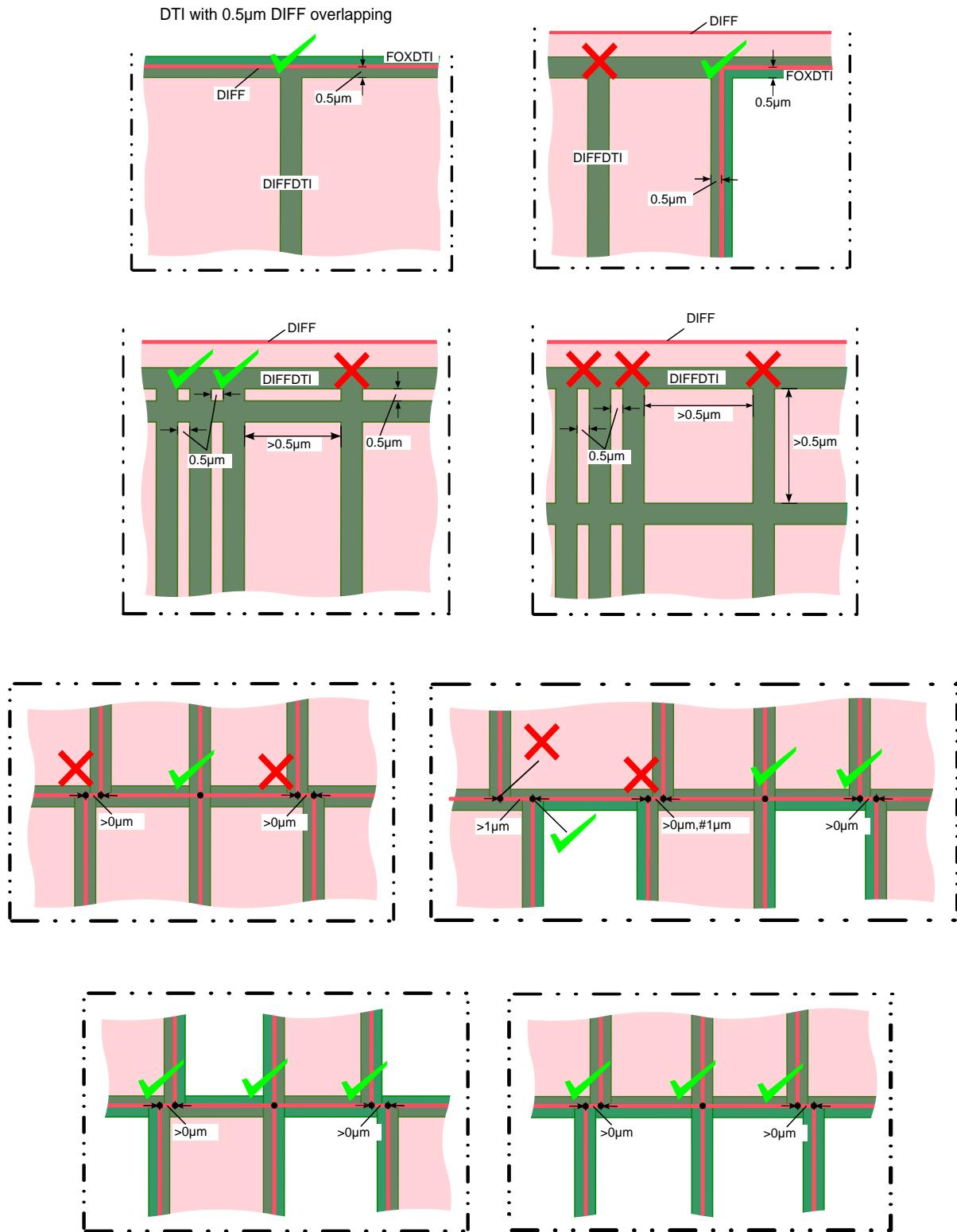
#### DTI

Name	Description	Value	Unit
B1DI	90 degree DIFFDTI corner (width > 0.5μm) is not allowed  <b>Note:</b> Multiple DIFFDTI corners with crosshatch pattern are allowed.	-	-
B1DT	DTI must form closed rings. Spurs are not allowed.	-	-
B2DI	T-junction DIFFDTI (width > 0.5μm) is not allowed (except nhsj1_7, phsj1_7, dfwnsj1_7, phsj2b_7)  <b>Note:</b> Multiple DIFFDTIs with intersectional pattern are allowed.	-	-
B4DT	DTI corner is 90° (except for dhw4c, dhw4d and dhw5d the corners are 135°)	-	-
W17P1	Minimum POLY1 width in dense DTI area  <b>Note:</b> Valid only in local DTI density > 40.0% window.  <b>Note:</b> DTI density is valid in any 100x100μm window using a step size of 10μm.	0.25	μm
W1DT	Fixed DTI width	1.0	μm
W2DT	Minimum FOXDTI width	0.5	μm
S1DTLOCK	Minimum dense DTI area spacing to LOCKED, LOCKED1, LOCKED2, LOCKED3 and LOCKED4  <b>Note:</b> Valid only in local DTI density > 40.0% window.  <b>Note:</b> DTI density is valid in any 100x100μm window using a step size of 10μm.	1.0	μm
<i>S3DT</i>	Fixed DIFFDTI spacing between multiple DIFFDTI rings	0.5	μm
<i>S4DT</i>	Fixed FOXDTI spacing between multiple FOXDTI rings (except dhw3c, dhw4c, dhw4d, dhw5d)	1.0	μm
S1DT	Minimum DIFFDTI spacing to DTI	0.5	μm
S1DTHW	Minimum DTI spacing to HWC	4.0	μm
S2DT	Minimum FOXDTI spacing to DTI	1.0	μm
E1DTP1	Minimum DTI enclosure of POLY1	0.5	μm
O1SBDT	Minimum SBLK overlap of DTI	0.5	μm
<i>R1DT</i>	Maximum ratio of DTI area to EXTENT AREA  <b>Note:</b> Not checked with standard DRC, option for check is available.	20.0	%

## 3. Layer and Device rules → 3.11 DTI module → 3.11.1 Layer rules → DTI

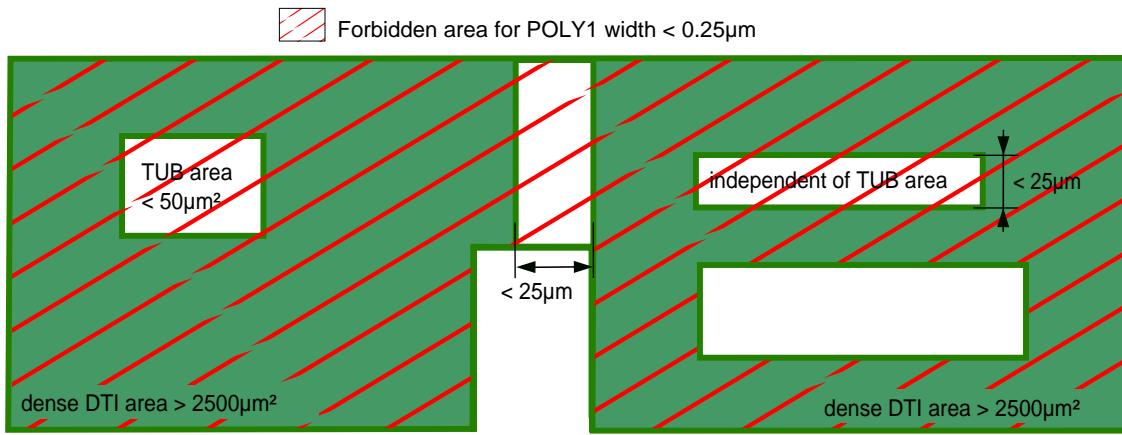
**Figure 3.114** DTI**Figure 3.115** DIFFDTI: B1DI

3. Layer and Device rules → 3.11 DTI module → 3.11.1 Layer rules → DTI



**Figure 3.116** DIFFDTI: B2DI

## 3. Layer and Device rules → 3.11 DTI module→ 3.11.1 Layer rules→ DTI

**Figure 3.117** DTI: W17P1**3.11.2 Device rules****nmva**

The device nmva is superseded by nmvaa. nmva must not be used for any new designs.

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5DF	Check for nmva usage	-	-
<b>Note:</b> The device nmva is superseded by nmvaa. It is strongly recommended to use nmvaa.			
B5MV	nmva without MV is not allowed	-	-
W3GA	Fixed CHANNEL length	0.5	$\mu\text{m}$
W4GA	Minimum CHANNEL width	1.0	$\mu\text{m}$
S3DF	Fixed DRAIN-EDGE-STI length	0.4	$\mu\text{m}$
S1P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.2	$\mu\text{m}$
S4GADT	Fixed GATE spacing to DTI (in direction of GATE width)	0.5	$\mu\text{m}$
E3NWDN	Minimum NWELL enclosure of DRAIN NDIFF	0.5	$\mu\text{m}$
E10P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE width)	1.0	$\mu\text{m}$
E2P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.2	$\mu\text{m}$
O1NWGA	Fixed NWELL overlap of GATE	0.3	$\mu\text{m}$

**Note:** Each nmva transistor must be surrounded by DTI

3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ nmvaa

### **nmvaa**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5DF	Check for nmva usage  <b>Note:</b> The device nmva is superseded by nmvaa. It is strongly recommended to use nmvaa.	-	-
W30GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not NWELL.	0.5	μm
W31GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	1.0	μm
S3DF	Fixed DRAIN-EDGE-STI length	0.4	μm
S1P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.2	μm
S4GADT	Fixed GATE spacing to DTI (in direction of GATE width)	0.5	μm
E10P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E2P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.2	μm
O1NWGA	Fixed NWELL overlap of GATE	0.3	μm

**Note:** MV is necessary for this device.

**Note:** Each nmvaa transistor must be surrounded by DTI.

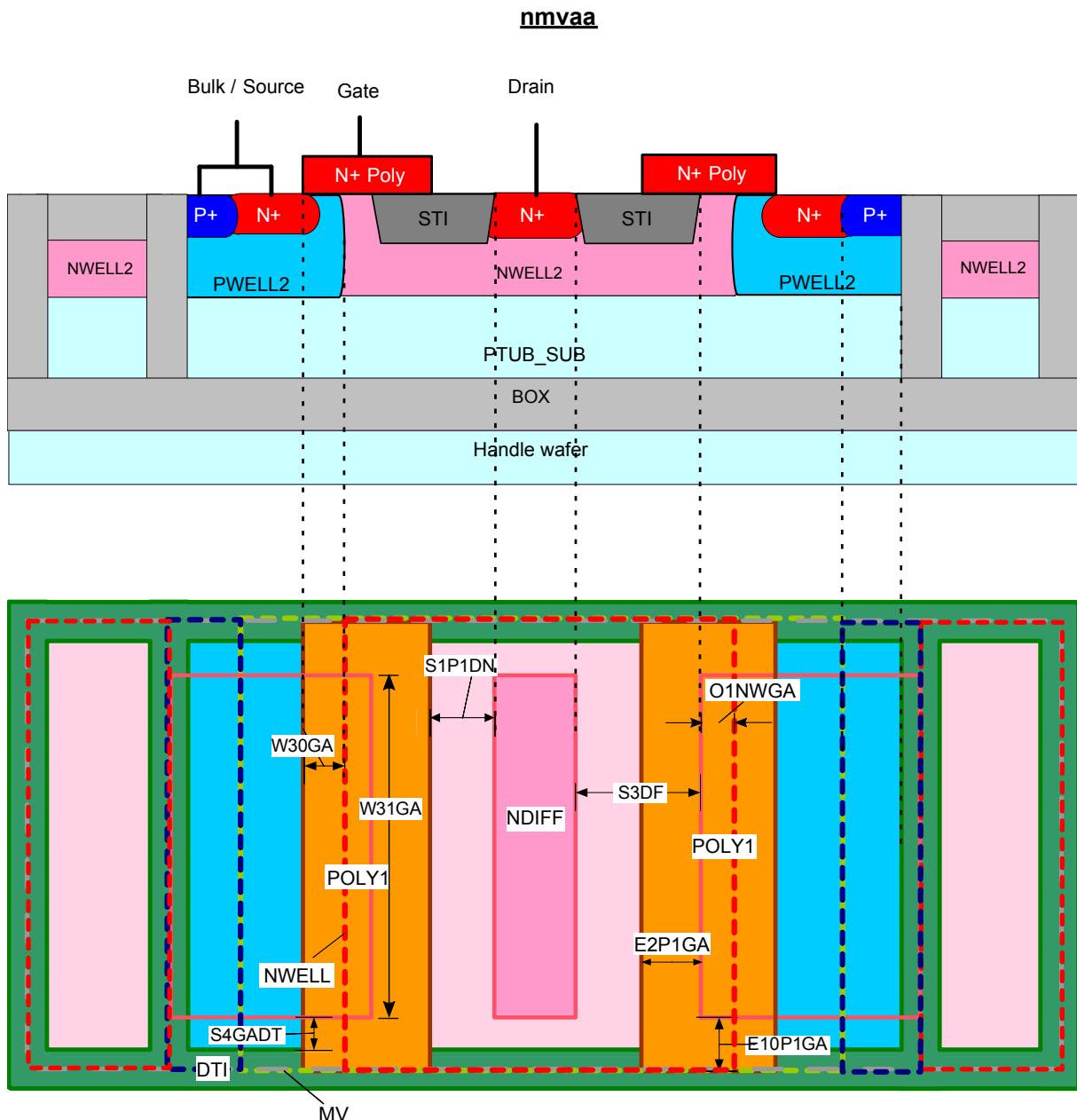
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The device nmvaa must be labeled "nmvaa" using POLY1 (VERIFICATION) layer over GATE.

**Note:** The DTI edge termination is predefined and must not be changed.

## 3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ nmvaa

**Figure 3.118 nmvaa**

3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ nmvab

### **nmvab**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

The device nmvab must be labeled "nmvab" using POLY1 (VERIFICATION) layer over GATE.

Each nmvab transistor must be surrounded by DTI.

Name	Description	Value	Unit
W30GA	Minimum CHANNEL length	0.5	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NWELL.		
W31GA	Minimum GATE width	1.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
S3DF	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
	Fixed DRAIN-EDGE-STI length	0.4	μm
S1P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.2	μm
S4GADT	Fixed GATE spacing to DTI (in direction of GATE width)	0.5	μm
E10P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E2P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.2	μm
O1NWGA	Fixed NWELL overlap of GATE	0.3	μm

**Note:** MV is necessary for this device.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

## 3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ nmvab

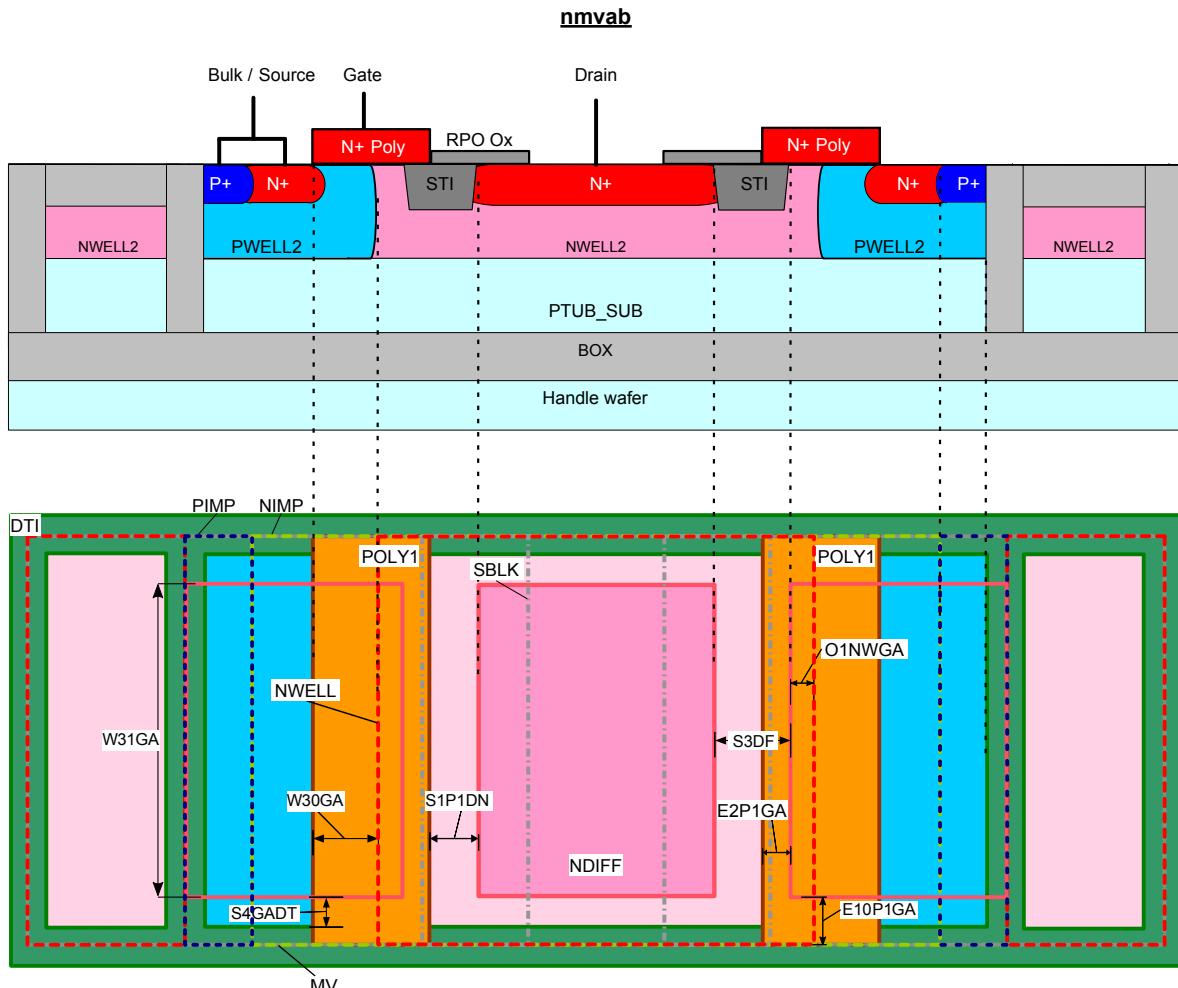


Figure 3.119 nmvab

3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ pmva

### **pmva**

The device pmva is superseded by pmvaa. pmva must not be used for any new designs.

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B6DF	Check for pmva usage	-	-
	<b>Note:</b> The device pmva is superseded by pmvaa. It is strongly recommended to use pmvaa.		
B8MV	pmva without MV is not allowed	-	-
W10GA	Minimum CHANNEL width	1.0	µm
W9GA	Fixed CHANNEL length	0.5	µm
S8DF	Fixed DRAIN-EDGE-STI length	0.4	µm
S3P1DP	Minimum POLY1 spacing to DRAIN PDIFF	0.2	µm
S4GADT	Fixed GATE spacing to DTI (in direction of GATE width)	0.5	µm
E3NWDP	Minimum NWELL enclosure of SOURCE PDIFF	0.5	µm
E11P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E9P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.2	µm
O2PWGA	Fixed PWELL overlap of GATE	0.3	µm

**Note:** Each pmva transistor must be surrounded by DTI

3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ pmvaa

### **pmvaa**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B6DF	Check for pmva usage  <b>Note:</b> The device pmva is superseded by pmvaa. It is strongly recommended to use pmvaa.	-	-
W66GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not PWELL.	0.5	μm
W67GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	1.0	μm
S8DF	Fixed DRAIN-EDGE-STI length	0.4	μm
S3P1DP	Minimum POLY1 spacing to DRAIN PDIFF	0.2	μm
S4GADT	Fixed GATE spacing to DTI (in direction of GATE width)	0.5	μm
E11P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E9P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.2	μm
O2PWGA	Fixed PWELL overlap of GATE	0.3	μm

**Note:** MV is necessary for this device.

**Note:** Each pmvaa transistor must be surrounded by DTI.

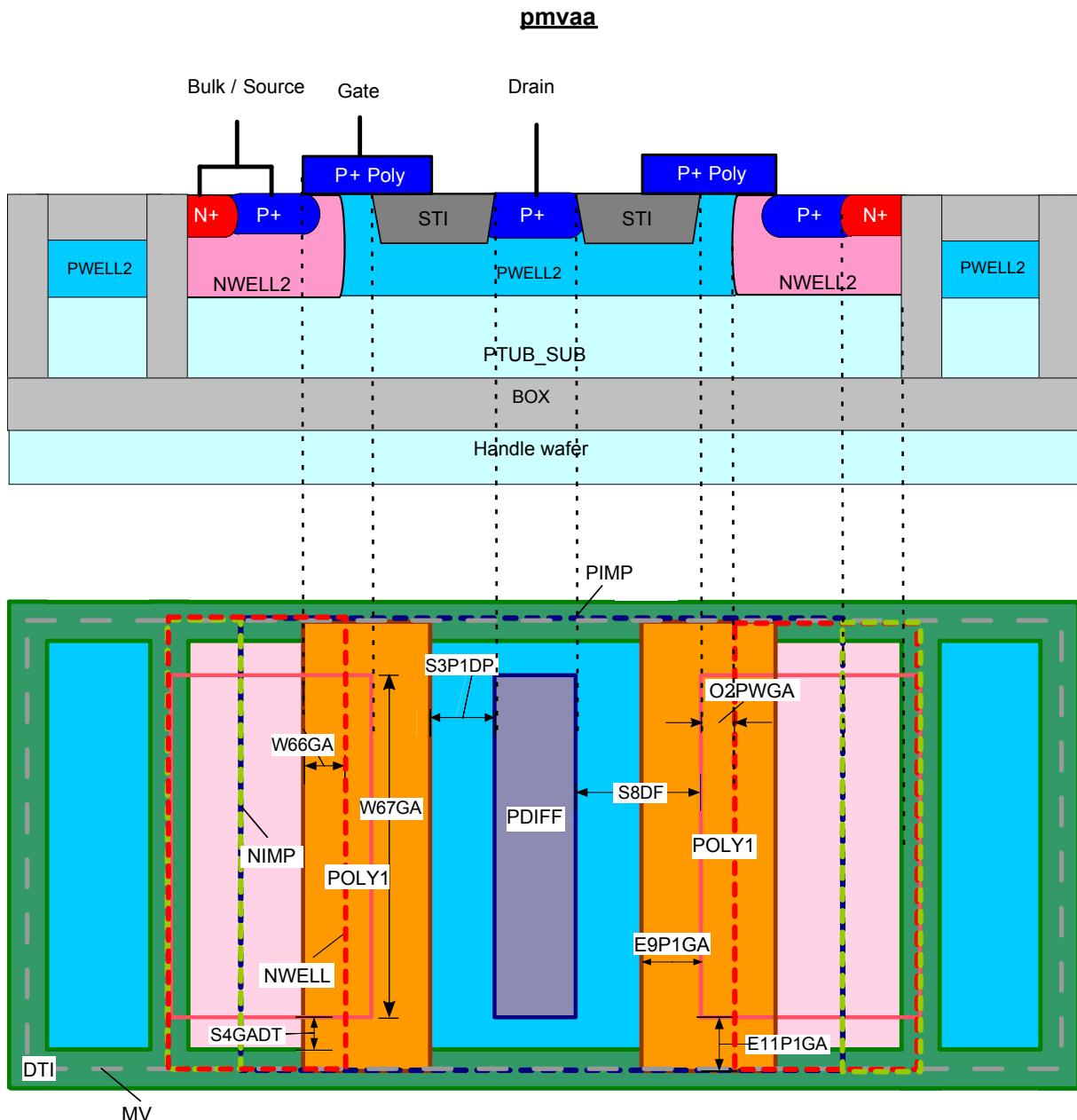
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The device pmvaa must be labeled "pmvaa" using POLY1 (VERIFICATION) layer over GATE.

**Note:** The DTI edge termination is predefined and must not be changed.

## 3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ pmvaa

**Figure 3.120 pmvaa**

3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ pmvab

### **pmvab**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W66GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not PWELL.	0.5	μm
W67GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	1.0	μm
S8DF	Fixed DRAIN-EDGE-STI length	0.4	μm
S3P1DP	Minimum POLY1 spacing to DRAIN PDIFF	0.2	μm
S4GADT	Fixed GATE spacing to DTI (in direction of GATE width)	0.5	μm
E11P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E9P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.2	μm
O2PWGA	Fixed PWELL overlap of GATE	0.3	μm

**Note:** MV is necessary for this device.

**Note:** The device pmvab must be labeled "pmvab" using POLY1 (VERIFICATION) layer over GATE.

**Note:** Each pmvab transistor must be surrounded by DTI.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

## 3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ pmvab

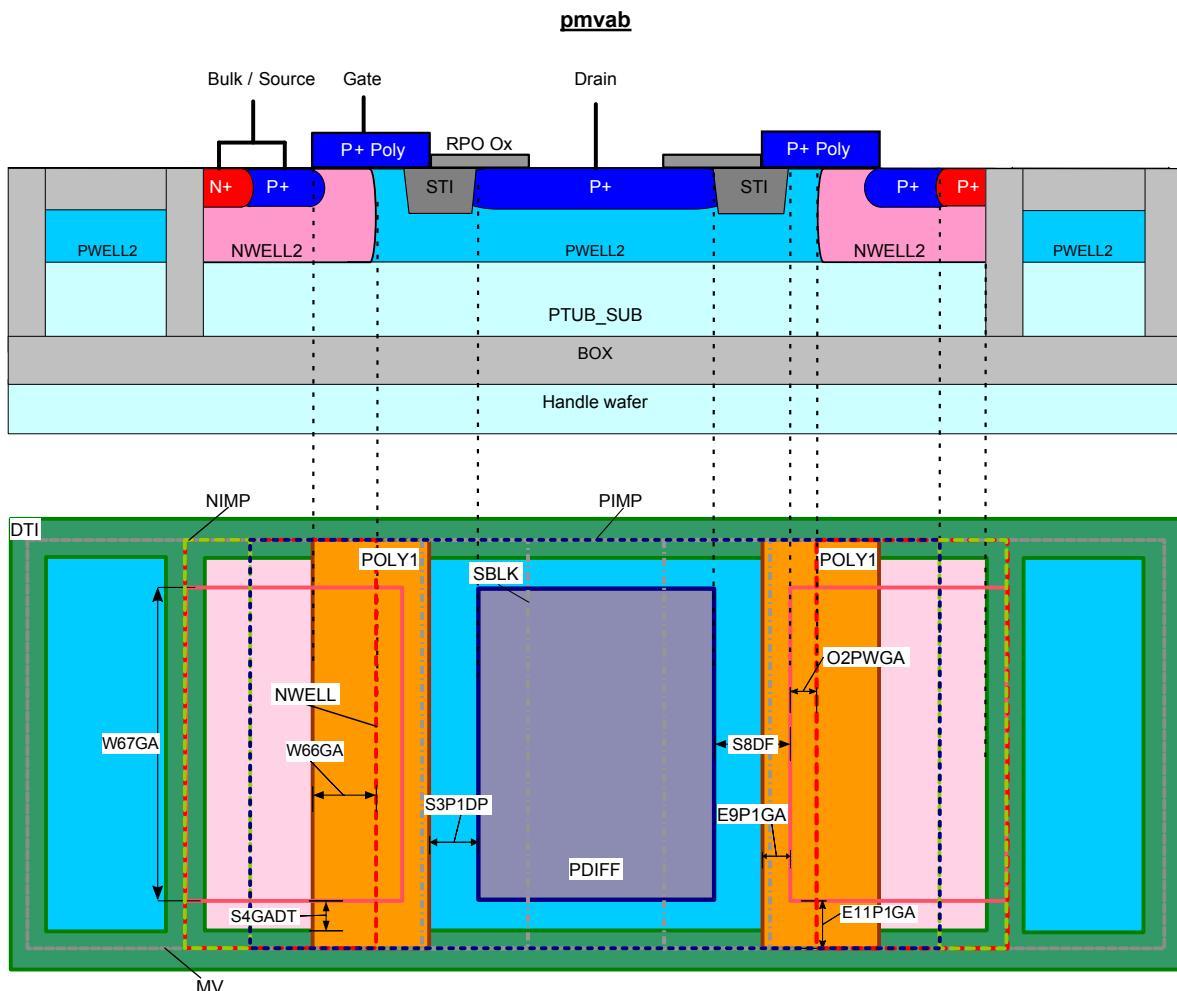


Figure 3.121 pmvab

3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ rxw2ti

### **rxw2ti**

The layout of rxw2ti is predefined and scalable concerning width and length only. All other dimensions of resistor body must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

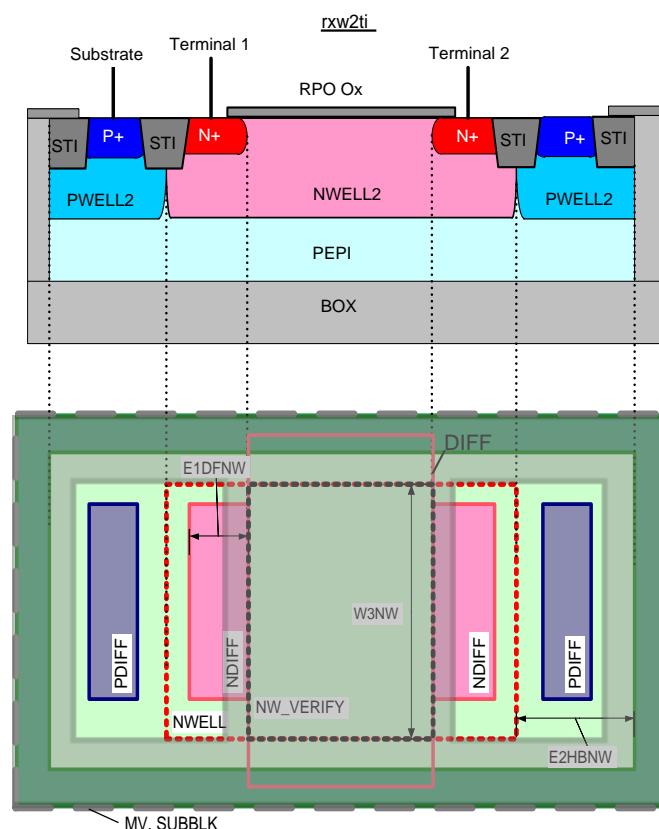
Name	Description	Value	Unit
B2NW	DTI ring is required for rxw2ti	-	-
B3NW	NIMP or PIMP overlap of rxw2ti (resistor body) is not allowed	-	-
B4NW	rxw2ti terminal without NIMP is not allowed	-	-
B5NW	MET1 or MET2 overlap of rxw2ti (resistor body) is not allowed	-	-
B6MV	rxw2ti without MV is not allowed	-	-
B7NW	rxw2ti (resistor body) without MET1BLK and MET2BLK is not allowed	-	-
W3NW	Minimum width	2.0	μm
E2HBNW	Minimum SUBBLK enclosure of NWELL	1.0	μm
E1DFNW	Fixed DIFF extension beyond NW_VERIFY in the direction of resistor terminal	0.76	μm

**Note:** Recommended minimum number of squares is  $L/W \geq 5$ .

**Note:** rxw2ti device must be labeled "rxw2ti " using NWELL (VERIFICATION).

**Note:** SUBBLK is necessary for this device.

**Note:** rxw2ti resistor definition: NWELL and NW\_VERIFY and DIFF and SBLK



**Figure 3.122 rxw2ti**

3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ mosvcti

### mosvcti

Name	Description	Value	Unit
B5GA	Only rectangular GATE is allowed	-	-
W22GA	Minimum GATE length	2.0	μm
W23GA	Minimum GATE width	2.0	μm

**Note:** DTI ring is required for mosvcti

**Note:** If the module MOS5 is selected, mosvcti is not available

**Note:** There is a limit to the tub size, please refer to R3DF design rule.

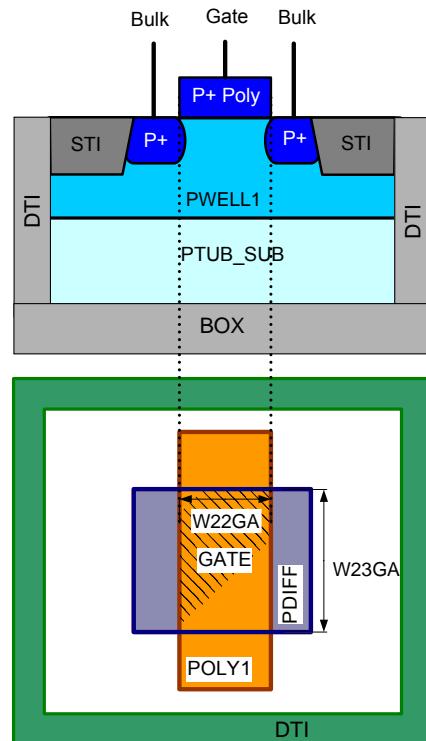


Figure 3.123 mosvcti

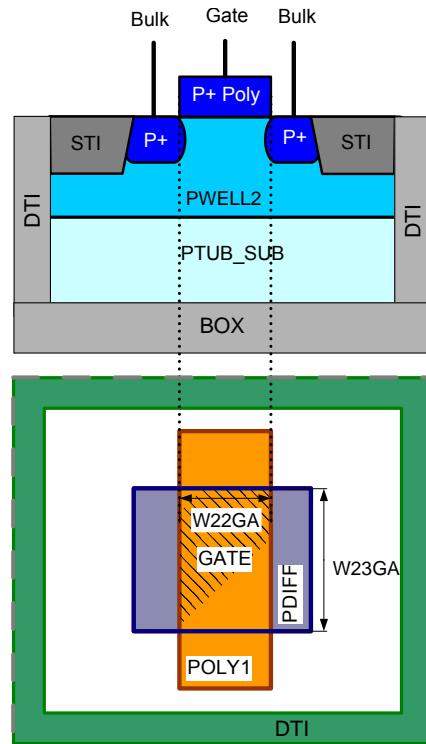
3. Layer and Device rules → 3.11 DTI module→ 3.11.2 Device rules→ mosvc5ti

### **mosvc5ti**

Name	Description	Value	Unit
B5GA	Only rectangular GATE is allowed	-	-
W22GA	Minimum GATE length	2.0	μm
W23GA	Minimum GATE width	2.0	μm

**Note:** DTI ring is required for mosvc5ti

**Note:** MV is necessary for mosvc5ti



**Figure 3.124** mosvc5ti

3. Layer and Device rules → 3.12 PSUB module

## 3.12 PSUB module

### 3.12.1 Layer rules

#### SUBBLK

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B13HB	NWELL in SUBBLK must have same net (except DTI, rxw2ti)	-	-
B1HB	SUBBLK overlap of HVNWELL is not allowed	-	-
<b>B2HB</b>	SUBBLK overlap of NWELL, NDIFF, PWBLK is not allowed (except nhsj1_#, phsj1_#, dfwnsj1_#, dhw#, nisj1_16, nhv#, phv#, ndhv#, dfwdn#, dfwdn5, ds5b, dnpa, dnpati, dza, dzati, dzbt, dzct, qpv#, qnv5, qnvha, qpv5, qpvha, rxw2ti, pmv#, nhvr#, phvr#, ndhvr#, dfwdnh#, nhsj1a_#, phsj1a_#, nhsj1b_#, phsj2b_#, dfwnsj1a_#, dfwnsj1b_#, dhw#c, dhw#d)	-	-
W1HB	Minimum SUBBLK width	2.0	μm
S1HB	Minimum SUBBLK spacing/notch	1.5	μm
S1HBDN	Minimum SUBBLK spacing to NDIFF (except DTI, nhsj1_#, phsj1_#, dfwnsj1_#, dhw# and nisj1_16, nhsj1a_#, dfwnsj1a_#)	0.5	μm
S1HBNW	Minimum SUBBLK spacing to NWELL (except DTI, nhsj1_#, phsj1_#, dfwnsj1_#, dhw#)	0.6	μm
S1HBPB	Minimum SUBBLK spacing to PWBLK (except DTI)	0.5	μm

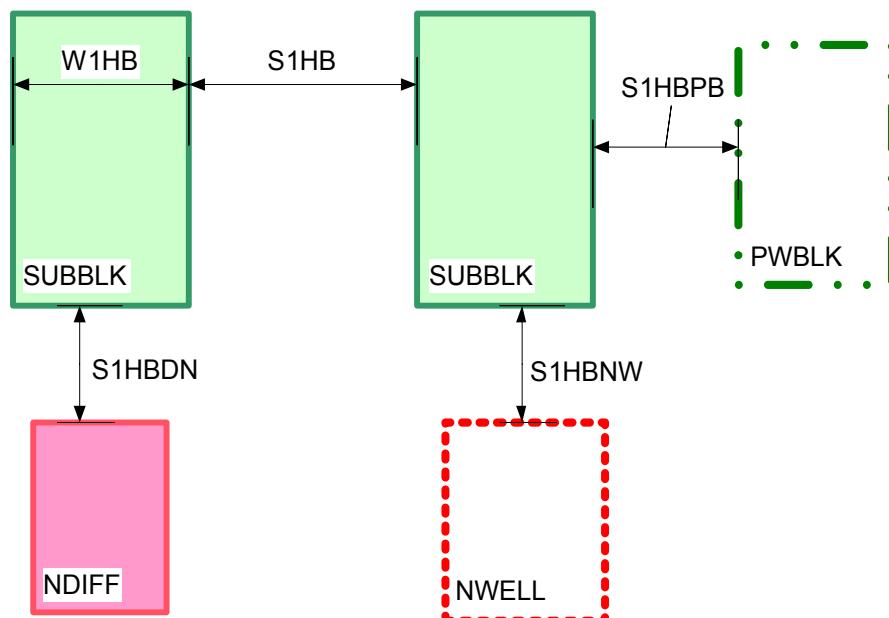


Figure 3.125 SUBBLK

#### SUB, SUB\_E

Name	Description	Value	Unit
W1BS	Minimum SUB width	1.5	μm
W2BS	Minimum SUB_E width	0.5	μm
S1BS	Minimum SUB spacing/notch	2.0	μm
A1BS	Minimum SUB area	9.5	μm <sup>2</sup>

3. Layer and Device rules → 3.12 PSUB module → 3.12.2 Device rules → qpva, qpvb, qpvc

### 3.12.2 Device rules

#### **qpva, qpvb, qpvc**

The devices qpva, qpvb and qpvc use PDIFF as emitter, NWELL1 as base and PWELL1 as collector.

The layouts of qpva, qpvb and qpvc are predefined. They must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

##### **qpva**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $2 \times 2 \mu\text{m}^2$

##### **qpvb**

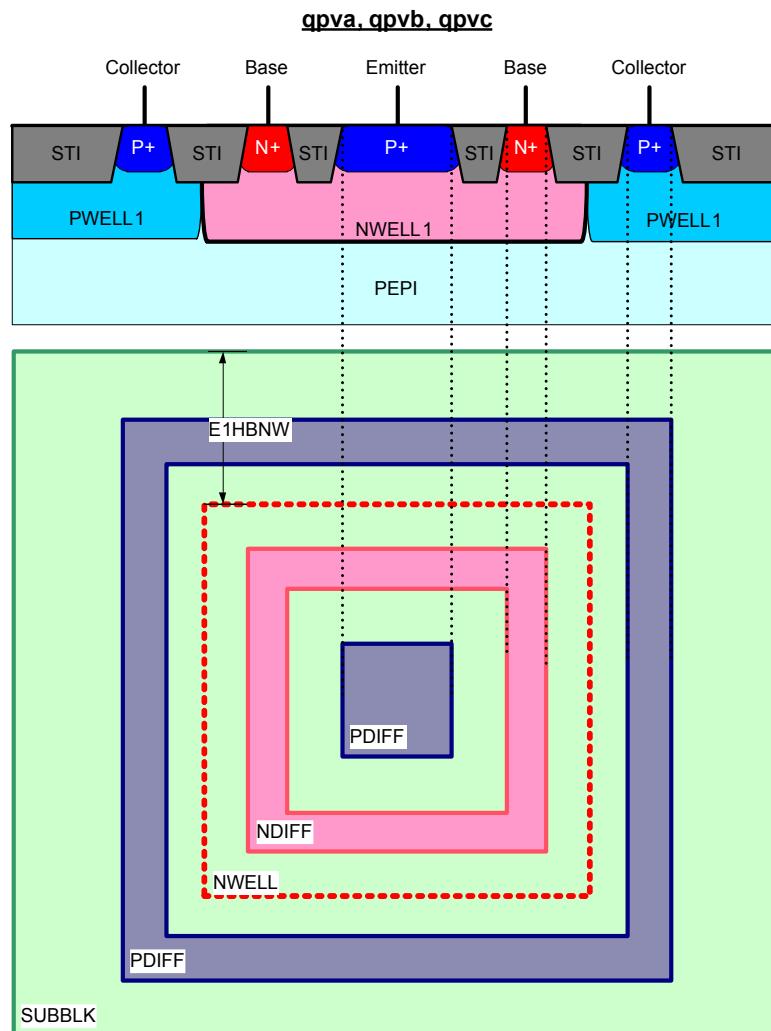
NDIFF base surrounding PDIFF emitter contact, emitter area:  $5 \times 5 \mu\text{m}^2$

##### **qpvc**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $10 \times 10 \mu\text{m}^2$

Name	Description	Value	Unit
E1HBNW	Fixed SUBBLK enclosure of NWELL	1.33	$\mu\text{m}$

**Note:** If the module MOS5 is selected, qpva, qpvb, qpvc are not available



**Figure 3.126** qpva, qpvb, qpvc

3. Layer and Device rules → 3.12 PSUB module → 3.12.2 Device rules → qpva5, qpvb5, qpvc5

### **qpva5, qpvb5, qpvc5**

This section describes the vertical PNP transistors qpva5, qpvb5, and qpvc5.

These transistors use PDIFF as emitter, NWELL2 as base and PWELL2 as collector. Their layouts are predefined. They must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

#### **qpva5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $2 \times 2 \mu\text{m}^2$

#### **qpvb5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $5 \times 5 \mu\text{m}^2$

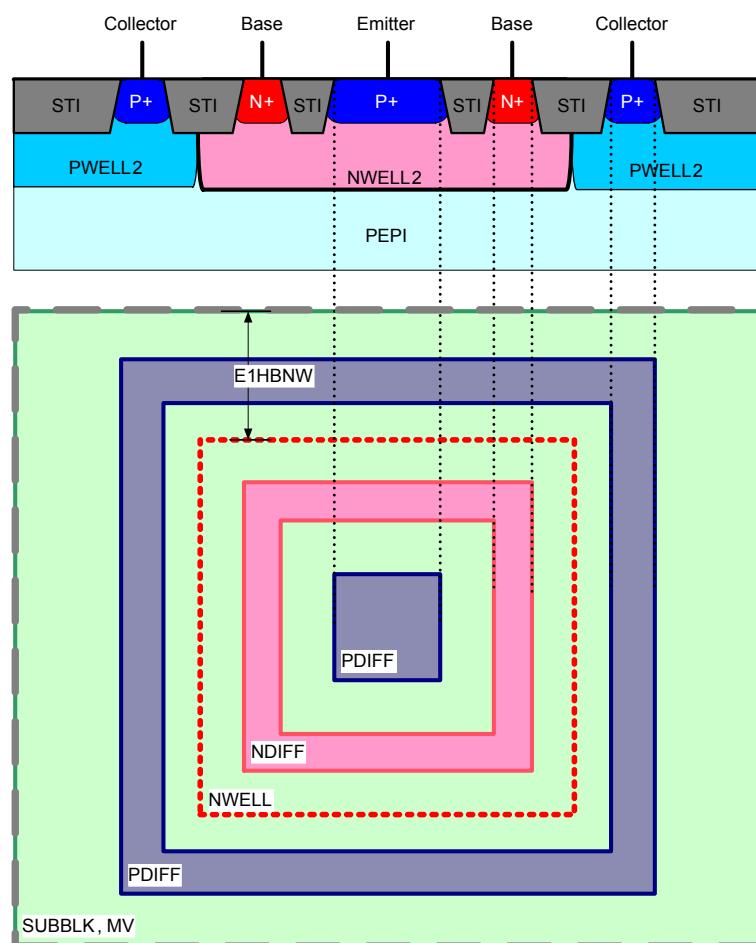
#### **qpvc5**

NDIFF base surrounding PDIFF emitter contact, emitter area:  $10 \times 10 \mu\text{m}^2$

Name	Description	Value	Unit
E1HBNW	Fixed SUBBLK enclosure of NWELL	1.33	μm

**Note:** MV is necessary for qpva5, qpvb5 and qpvc5.

#### **qpva5, qpvb5, qpvc5**



**Figure 3.127** qpva5, qpvb5, qpvc5

3. Layer and Device rules → 3.12 PSUB module→ 3.12.2 Device rules→ dfwdn5

### dfwdn5

The layout of the dfwdn5 diode is predefined and only the cathode width can be changed in the range of 2.0  $\mu\text{m}$  to 200.0  $\mu\text{m}$ . Fixed cathode length is 1.0  $\mu\text{m}$ .

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.

**Note:** DTI ring is required for this device.

**Note:** MV is necessary for dfwdn5

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

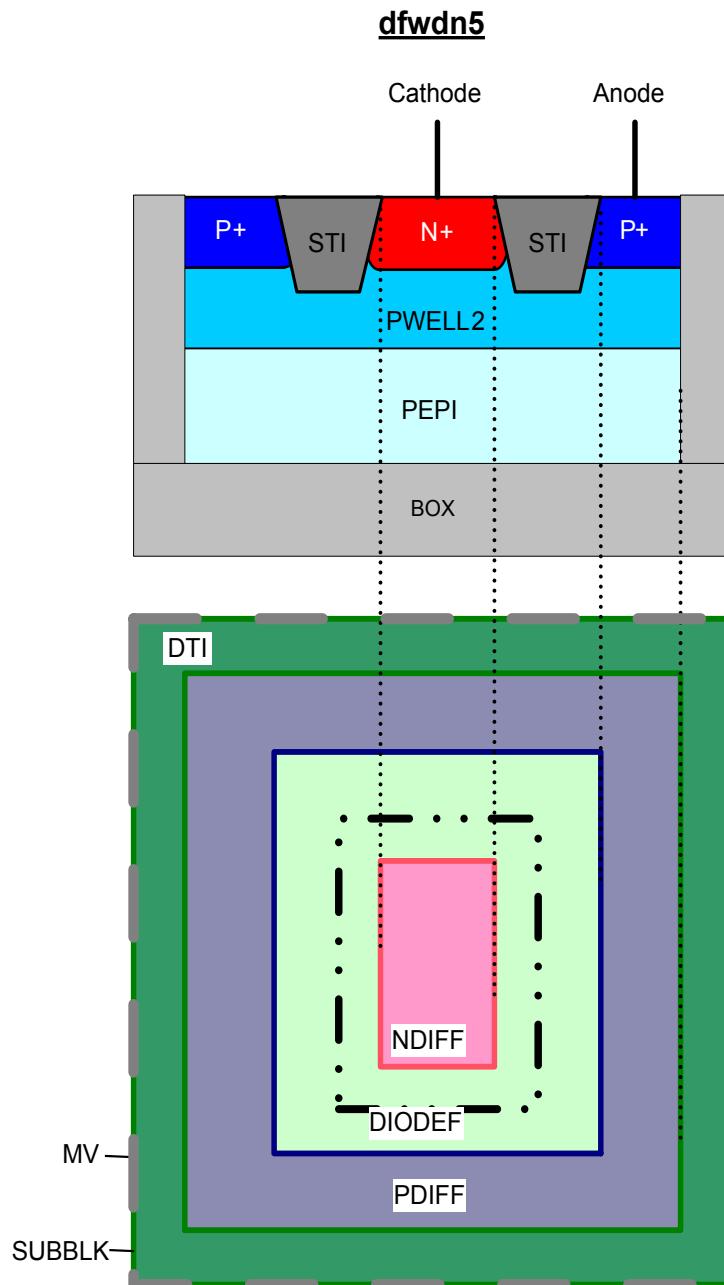


Figure 3.128 dfwdn5

3. Layer and Device rules → 3.12 PSUB module→ 3.12.2 Device rules→ ds5b

### ds5b

The layout of the ds5b Schottky diode is predefined and only the width can be changed in the range of 2.4  $\mu\text{m}$  up to 50  $\mu\text{m}$ . Fixed length is 0.94  $\mu\text{m}$ .

Name	Description	Value	Unit
B2DF	ds5 is not allowed	-	-

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

**Note:** DTI ring is required for ds5b.

**Note:** MV is necessary for ds5b.

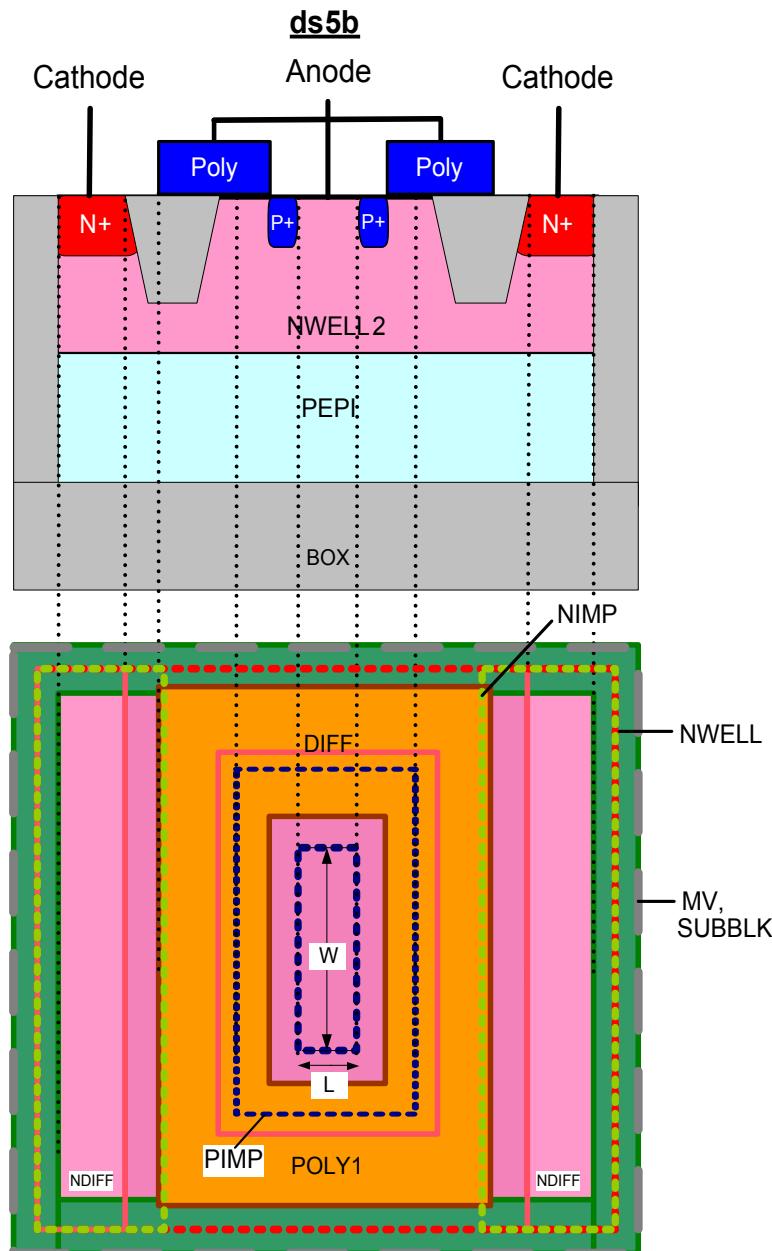


Figure 3.129 ds5b

3. Layer and Device rules → 3.13 LVT module

## 3.13 LVT module

### 3.13.1 Layer rules

#### LVT

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1LV	LVT overlap of MV, DNC, DPC, PWBLK, SUBBLK, HVNWELL or HVPWELL is not allowed	-	-
B2LV	LVT overlap of rnw, rdn, rdp, qpve, qpvf, qpvg is not allowed	-	-
S1LVHN	Minimum LVT spacing to HVNWELL	1.0	μm
S1LVHP	Minimum LVT spacing to HVPWELL	1.0	μm
S1LVGA	Minimum LVT spacing to GATE	0.35	μm
S2LVGA	Minimum LVT spacing to GATE (in the direction of GATE length)	0.46	μm
E1LVGA	Minimum LVT enclosure of GATE	0.35	μm
E2LVGA	Minimum LVT enclosure of GATE (in the direction of GATE length)	0.46	μm

**Note:** Because of the well proximity effect it is not recommended to use the minimum design rules E1LVGA, E2LVGA, S1LVGA and S2LVGA for critical and precise designs.

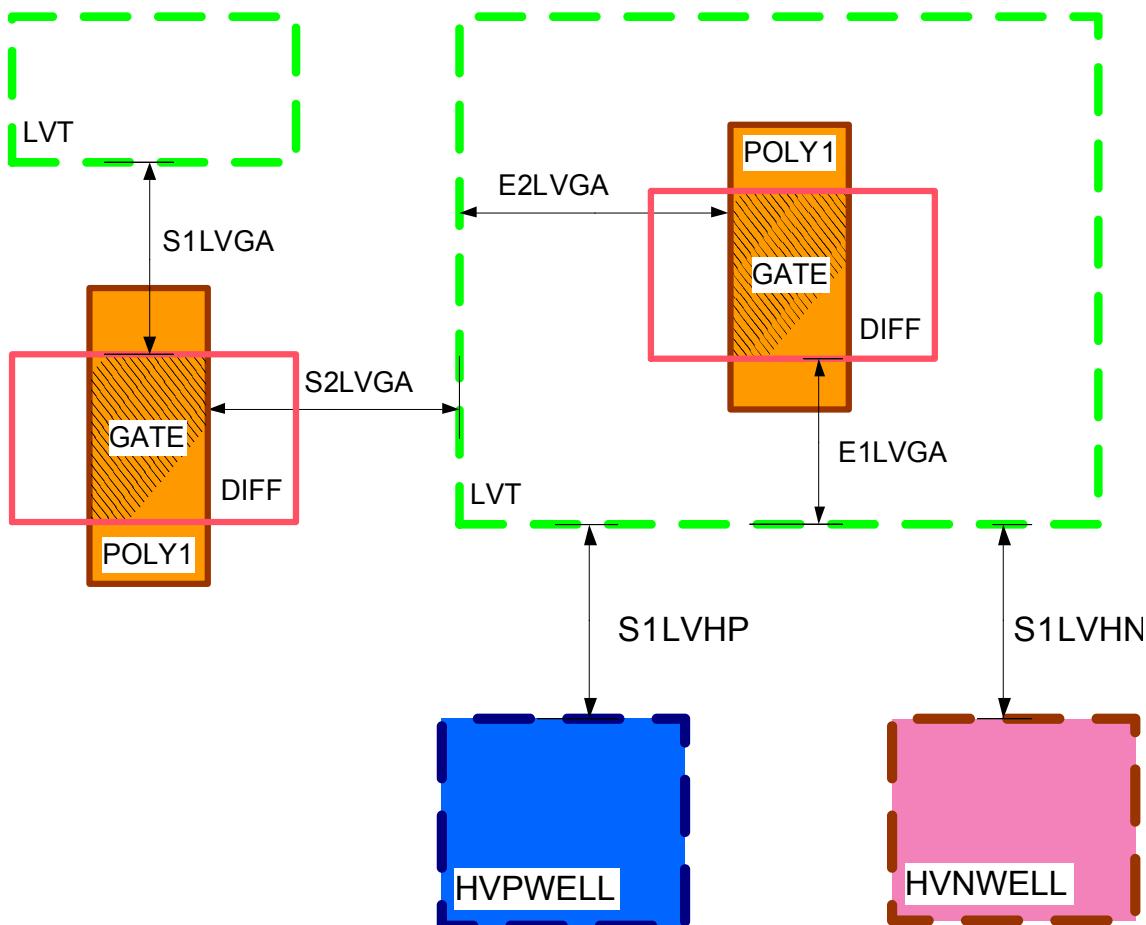


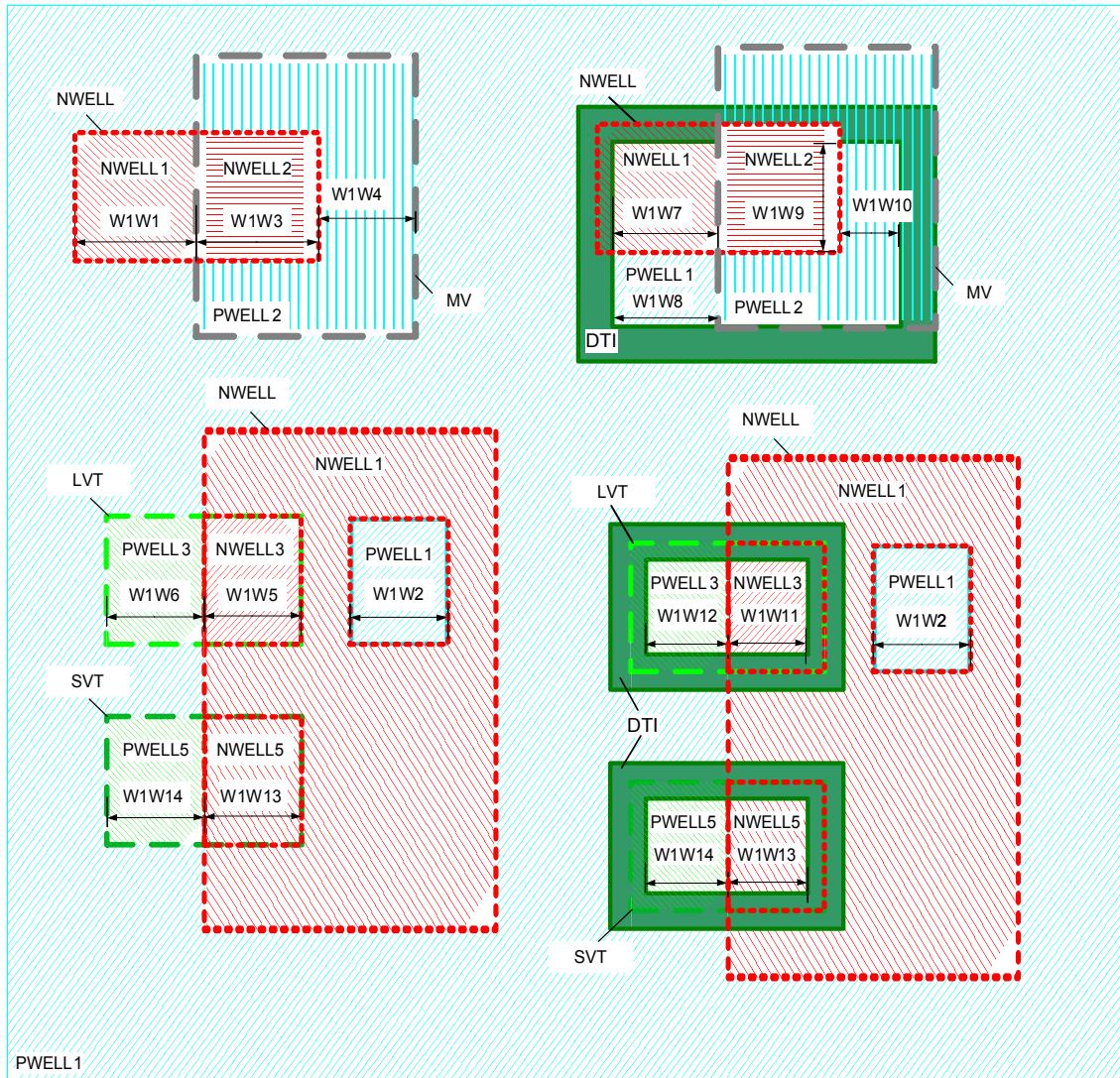
Figure 3.130 LVT

3. Layer and Device rules → 3.13 LVT module → 3.13.1 Layer rules → NWELL3, PWELL3, NWELL3\_E, PWELL3\_E

### NWELL3, PWELL3, NWELL3\_E, PWELL3\_E

These rules are related to a combination of design layers (refer to section "2.4 Definitions").

Name	Description	Value	Unit
W1W5	Minimum NWELL3 width	0.86	μm
W1W6	Minimum PWELL3 width	0.6	μm
W1W11	Minimum NWELL3_E width	0.5	μm
W1W12	Minimum PWELL3_E width	0.5	μm
A1W5	Minimum NWELL3 area	2.25	μm <sup>2</sup>
A1W6	Minimum PWELL3 area	0.8	μm <sup>2</sup>



**Figure 3.131 NWELL, PWELL**

### 3.13.2 Device rules

#### nel, pel

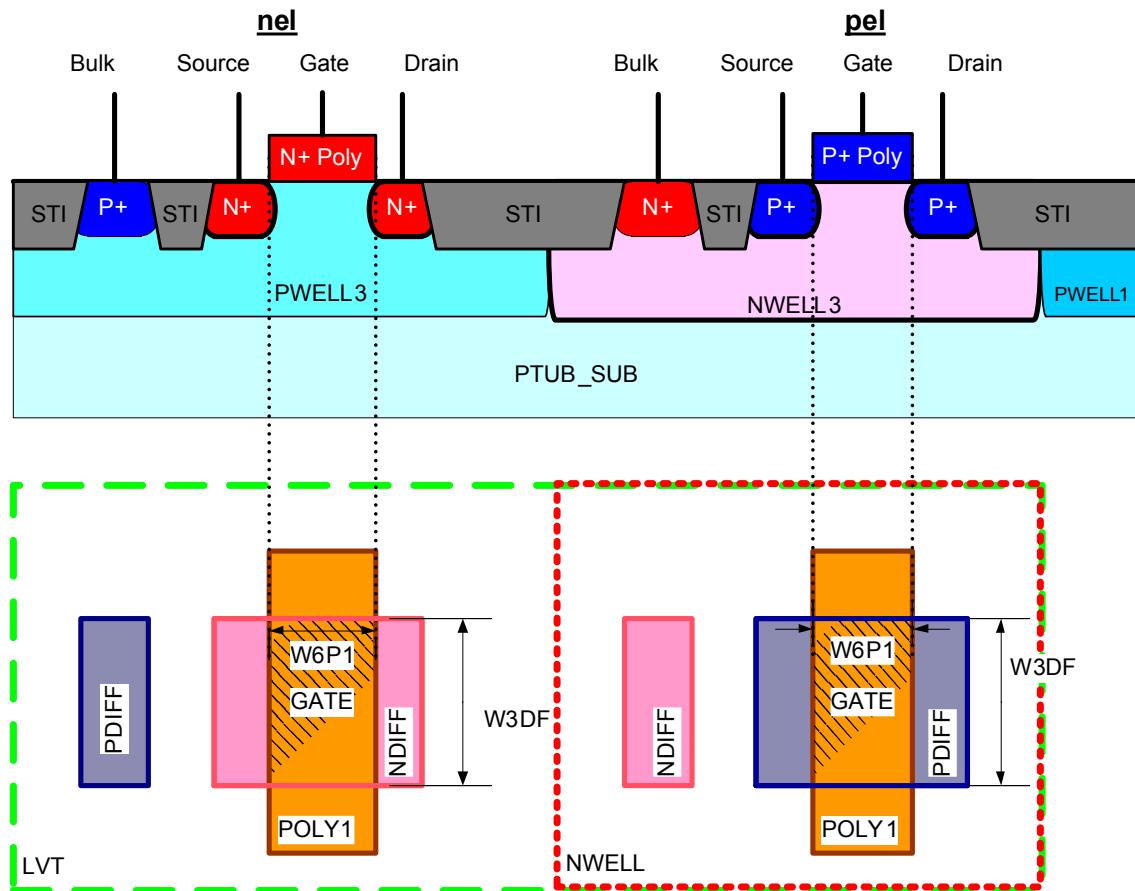
Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.			⇒

## 3. Layer and Device rules → 3.13 LVT module→ 3.13.2 Device rules→ nel, pel

Name	Description	Value	Unit
W6P1	Minimum GATE length	0.22	μm

**Note:** If the module MOS5 is selected, nel, pel are not available

**Note:** For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.



**Figure 3.132** nel, pel

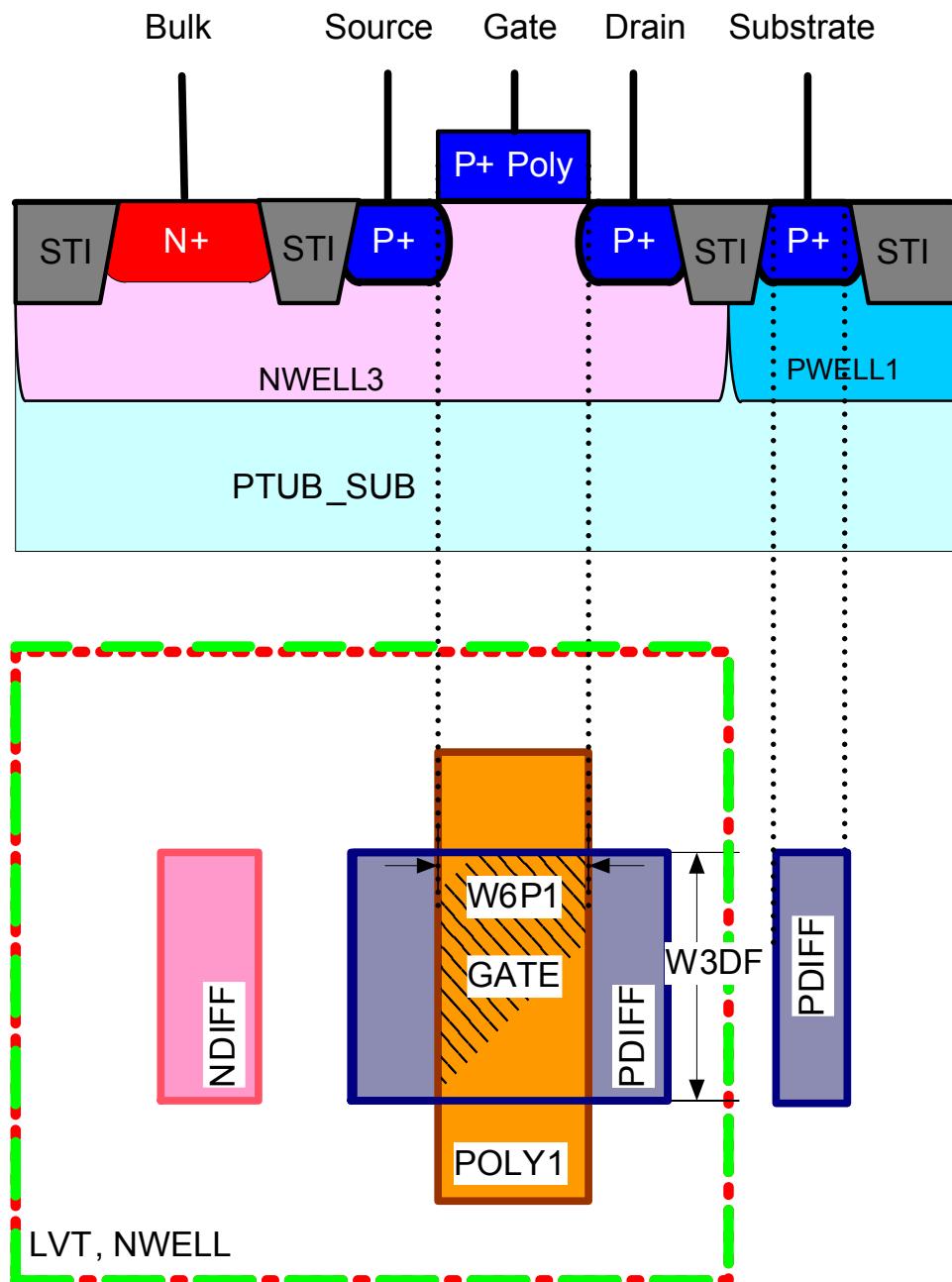
3. Layer and Device rules → 3.13 LVT module → 3.13.2 Device rules → pel\_5

### **pel\_5**

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.		
W6P1	Minimum GATE length	0.22	μm

**Note:** If the module MOS5 is selected, pel\_5 is not available

### **pel\_5**



**Figure 3.133 pel\_5**

3. Layer and Device rules → 3.14 SVT module

## 3.14 SVT module

### 3.14.1 Layer rules

#### SVT

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1SV	SVT overlap of LVT, MV, DNC, DPC, PWBLK, SUBBLK, HVNWELL or HVPWELL is not allowed	-	-
B2SV	SVT overlap of rnw, rdn, rdp, qpve, qpvf, qpvg is not allowed	-	-
S1SVHN	Minimum SVT spacing to HVNWELL	1.0	μm
S1SVHP	Minimum SVT spacing to HVPWELL	1.0	μm
S1SVGA	Minimum SVT spacing to GATE	0.35	μm
S2SVGA	Minimum SVT spacing to GATE (in the direction of GATE length)	0.46	μm
E1SVGA	Minimum SVT enclosure of GATE	0.35	μm
E2SVGA	Minimum SVT enclosure of GATE (in the direction of GATE length)	0.46	μm

**Note:** Because of the well proximity effect it is not recommended to use the minimum design rules E1SVGA, E2SVGA, S1SVGA and S2SVGA for critical and precise designs.

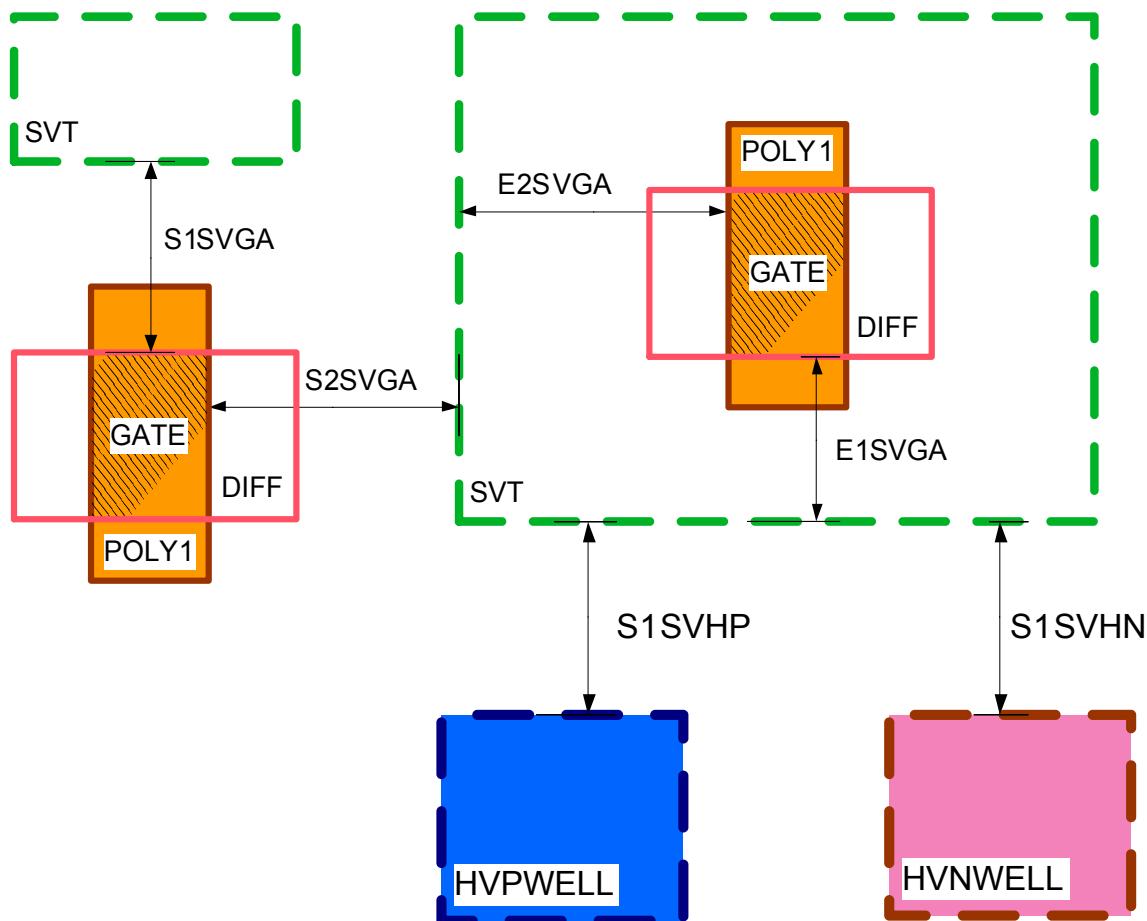
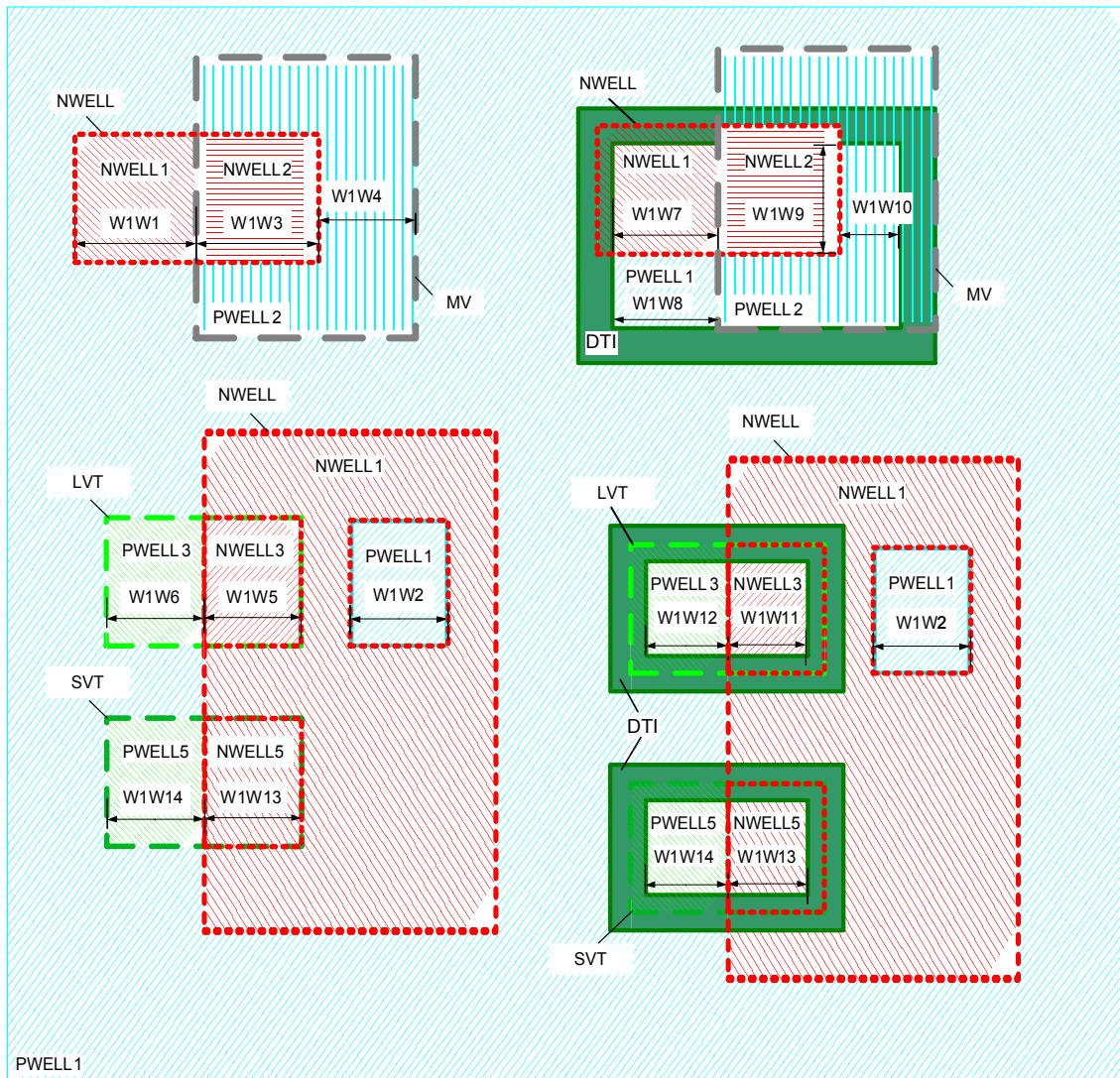


Figure 3.134 SVT

3. Layer and Device rules → 3.14 SVT module→ 3.14.1 Layer rules→ NWELL5, NWELL5\_E, PW...

### NWELL5, NWELL5\_E, PWELL5, PWELL5\_E

Name	Description	Value	Unit
W1W13	Minimum NWELL5 width	0.86	μm
	<b>Note:</b> Not valid between adjacent corners if the virtual line which joins them is orthogonal with respect to the coordinate system axes. The minimum length of this line is 0.56μm.		
W1W14	Minimum PWELL5 width	0.6	μm
	<b>Note:</b> Not valid between adjacent corners if the virtual line which joins them is orthogonal with respect to the coordinate system axes. The minimum length of this line is 0.56μm.		
W1W15	Minimum NWELL5_E width	0.5	μm
W1W16	Minimum PWELL5_E width	0.5	μm
A1W13	Minimum NWELL5 area	2.25	μm <sup>2</sup>
A1W14	Minimum PWELL5 area	0.8	μm <sup>2</sup>



**Figure 3.135 NWELL, PWELL**

3. Layer and Device rules → 3.14 SVT module → 3.14.2 Device rules → nesvt, pesvt

### 3.14.2 Device rules

#### nesvt, pesvt

Name	Description	Value	Unit
W10P1	Minimum GATE length	0.21	μm
W3DF	Minimum GATE width <b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.	0.22	μm

**Note:** If the module MOS5 is selected, nesvt, pesvt are not available

**Note:** For more extensive LVS, it is recommended to use the related 5 or 6 terminal device.

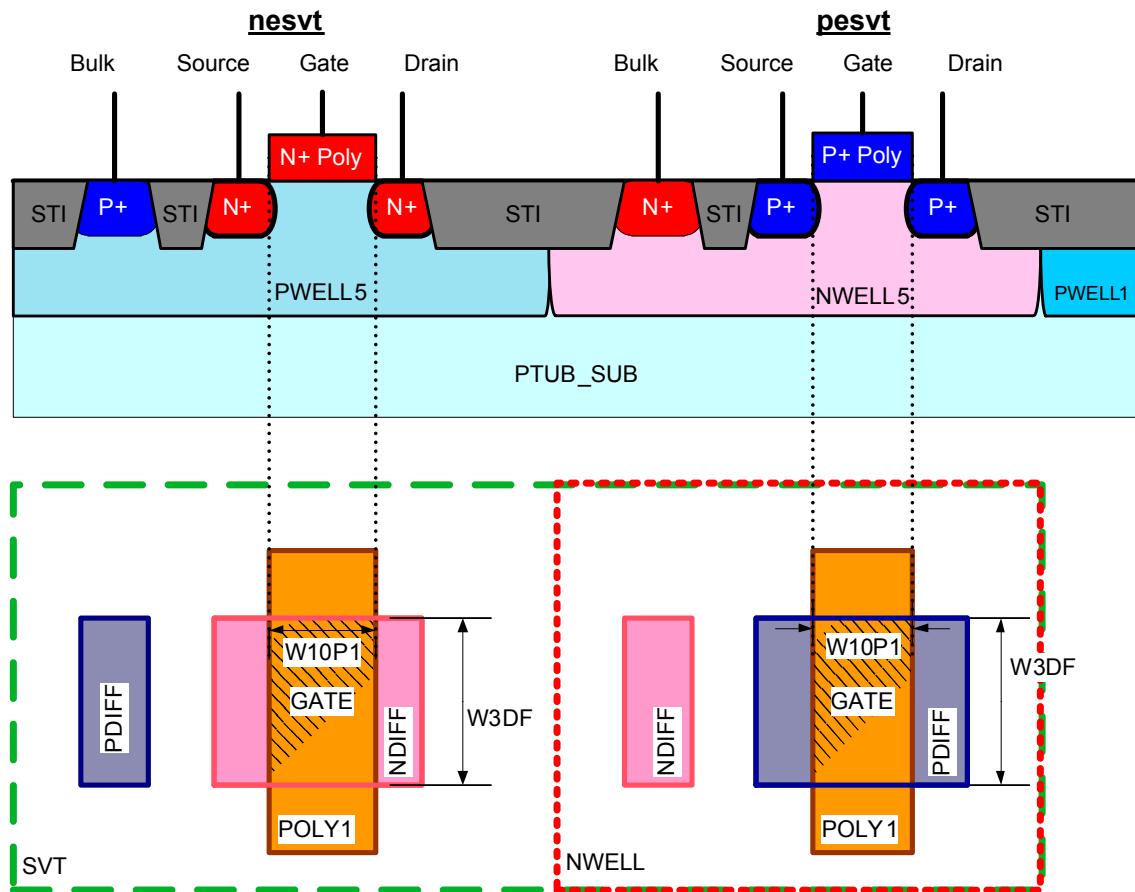


Figure 3.136 nesvt, pesvt

3. Layer and Device rules → 3.14 SVT module → 3.14.2 Device rules → pesvt\_5

### **pesvt\_5**

Name	Description	Value	Unit
W10P1	Minimum GATE length	0.21	μm
W3DF	Minimum GATE width	0.22	μm
<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.			

**Note:** If the module MOS5 is selected, pesvt\_5 is not available

### **pesvt\_5**

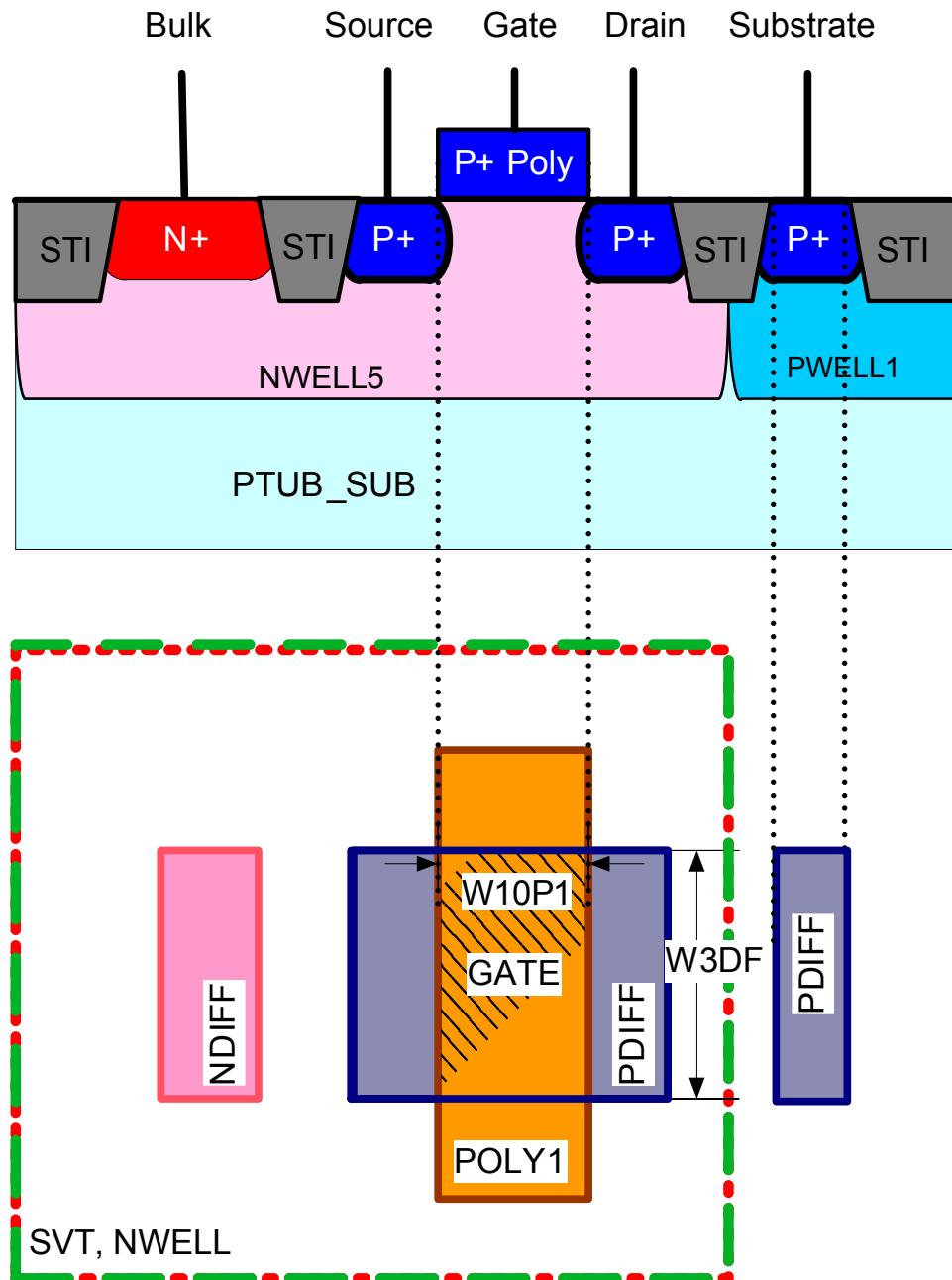


Figure 3.137 pesvt\_5

3. Layer and Device rules → 3.15 BJTA module

## 3.15 BJTA module

### 3.15.1 Layer rules

#### NBASE

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1QN	NBASE is only allowed for qpv5, qpvha	-	-
B2QN	NBASE overlap of DPC, PWBLK, NWELL, PBASE, PZENER, NDF, PDF, PWELL4 or POLY1 is not allowed	-	-
B3QN	NBASE without MV and SUBBLK is not allowed	-	-
W1QN	Minimum NBASE width	1.0	μm
S1QN	Minimum NBASE spacing/notch	1.0	μm
A1QN	Minimum NBASE area	4.0	μm <sup>2</sup>

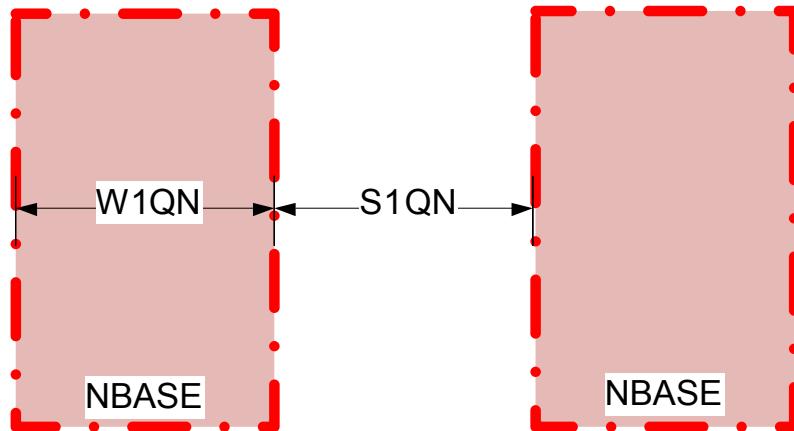


Figure 3.138 NBASE

#### NBASE\_E

Name	Description	Value	Unit
W2QN	Minimum NBASE_E width	0.5	μm

### 3.15.2 Device rules

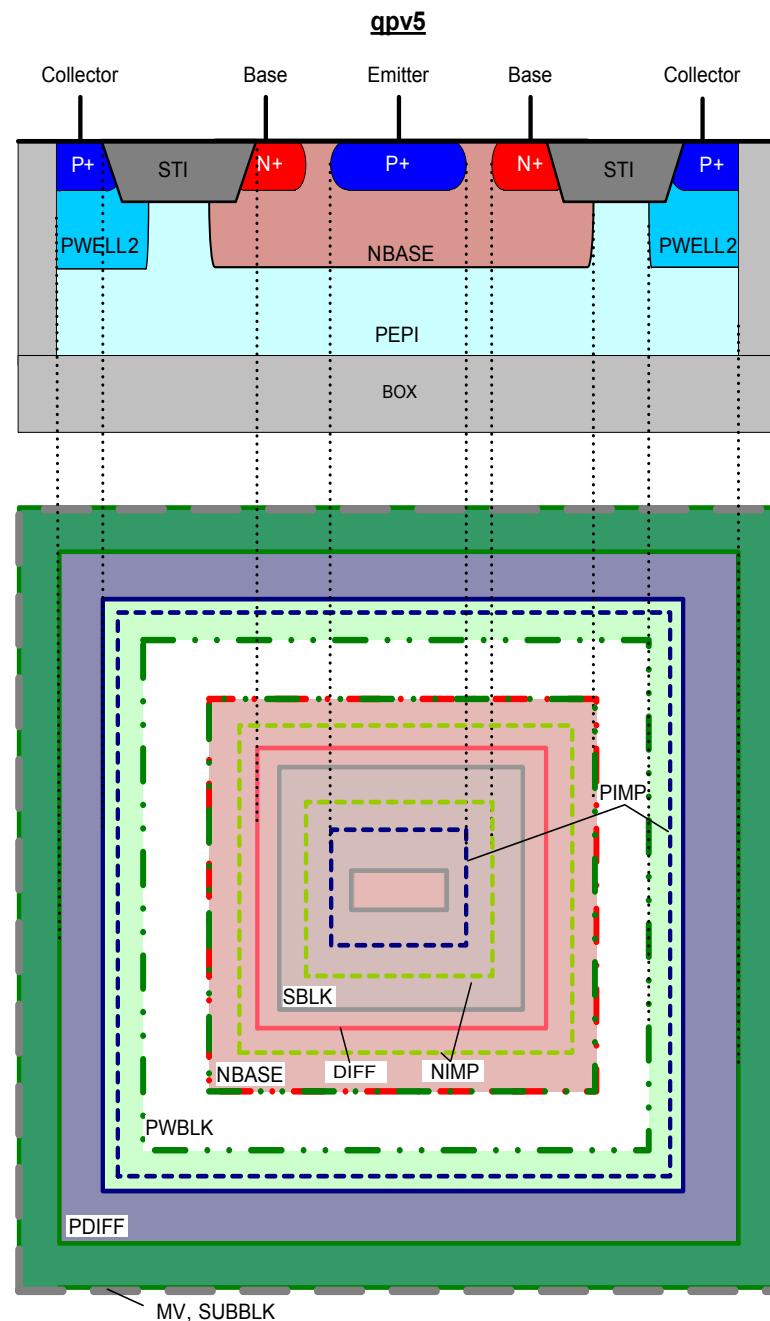
#### qpv5

The layout of the qpv5 bipolar PNP transistor is predefined and only the emitter length can be changed in the range of 10.0 μm to 100.0 μm. The emitter width is fixed at 2.0 μm.

**Note:** MV and SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

3. Layer and Device rules → 3.15 BJTA module→ 3.15.2 Device rules→ qpv5



**Figure 3.139** qpv5

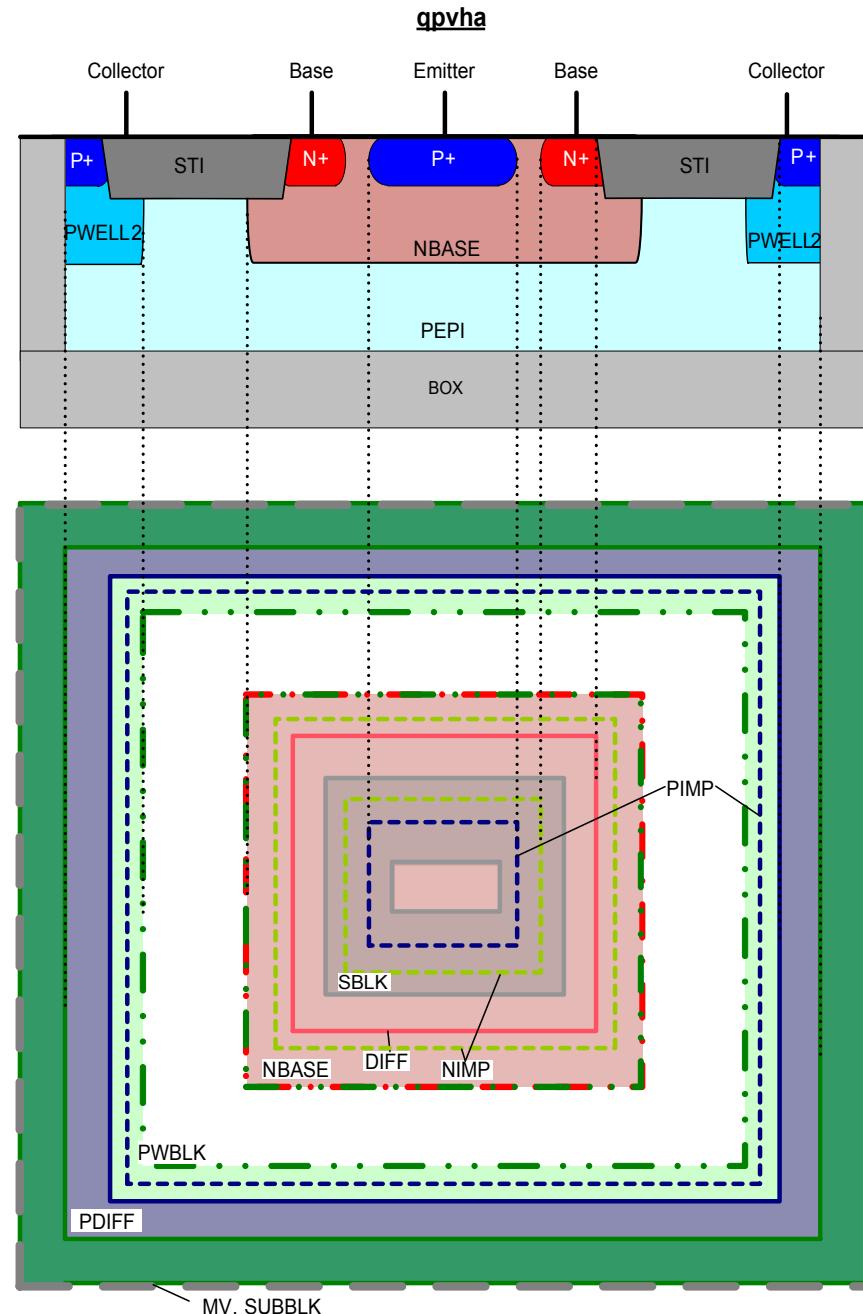
3. Layer and Device rules → 3.15 BJTA module→ 3.15.2 Device rules→ qpvha

### **qpvha**

The layout of the qpvha bipolar PNP transistor is predefined and only the emitter length can be changed in the range of 10.0  $\mu\text{m}$  to 100.0  $\mu\text{m}$ . The emitter width is fixed at 2.0  $\mu\text{m}$ .

**Note:** MV and SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.



**Figure 3.140** qpvha

3. Layer and Device rules → 3.16 BJTC module

## 3.16 BJTC module

### 3.16.1 Layer rules

#### PBASE

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1QP	PBASE is only allowed for qnv5, qnvhā	-	-
B2QP	PBASE overlap of DPC, PWBLK, NWELL, PZENER, NDF, PDF, PWELL4 or POLY1 is not allowed	-	-
B3QP	PBASE without MV and SUBBLK is not allowed	-	-
W1QP	Minimum PBASE width	1.0	μm
S1QP	Minimum PBASE spacing/notch	1.0	μm
A1QP	Minimum PBASE area	4.0	μm <sup>2</sup>

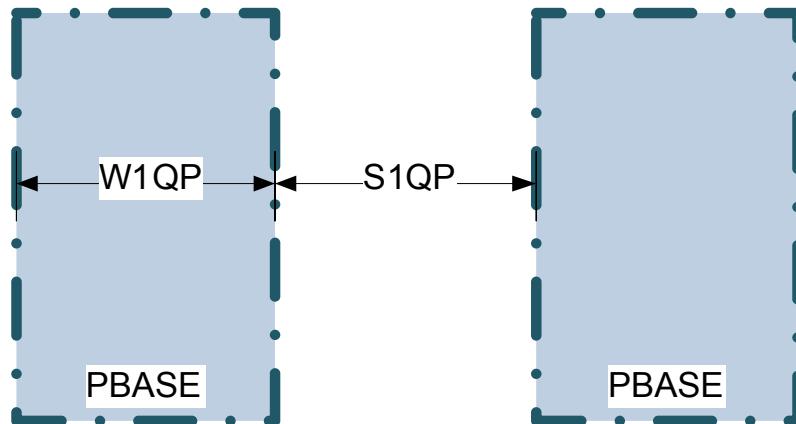


Figure 3.141 PBASE

#### PBASE\_E

Name	Description	Value	Unit
W2QP	Minimum PBASE_E width	0.5	μm

### 3.16.2 Device rules

#### qnv5

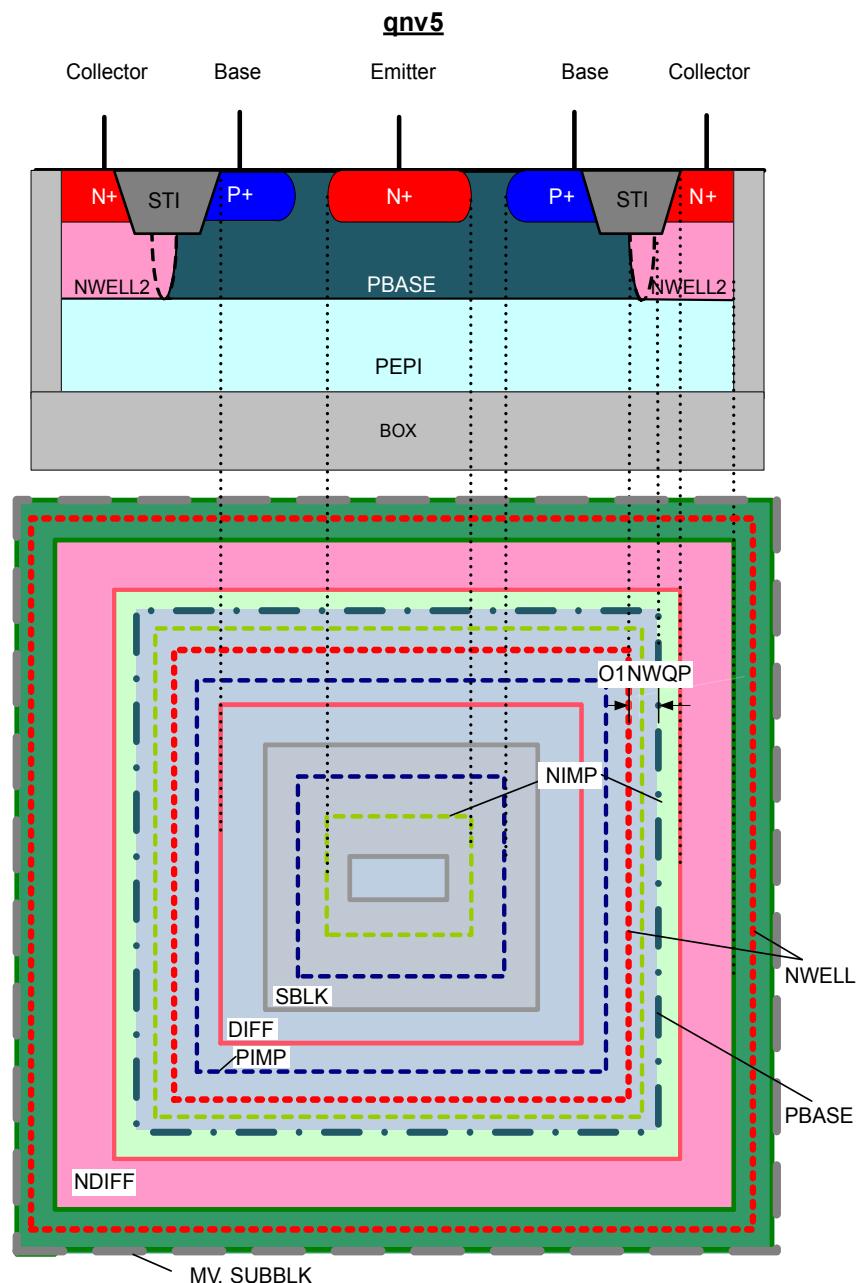
The layout of the qnv5 bipolar NPN transistor is predefined and only the emitter length can be changed in the range of 3.0 μm to 100.0 μm. The emitter width is fixed at 2.0 μm.

Name	Description	Value	Unit
O1NWQP	Fixed NWELL overlap of PBASE	0.1	μm

**Note:** MV and SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

3. Layer and Device rules → 3.16 BJTC module→ 3.16.2 Device rules→ qnv5



**Figure 3.142 qnv5**

3. Layer and Device rules → 3.16 BJTC module→ 3.16.2 Device rules→ qnvha

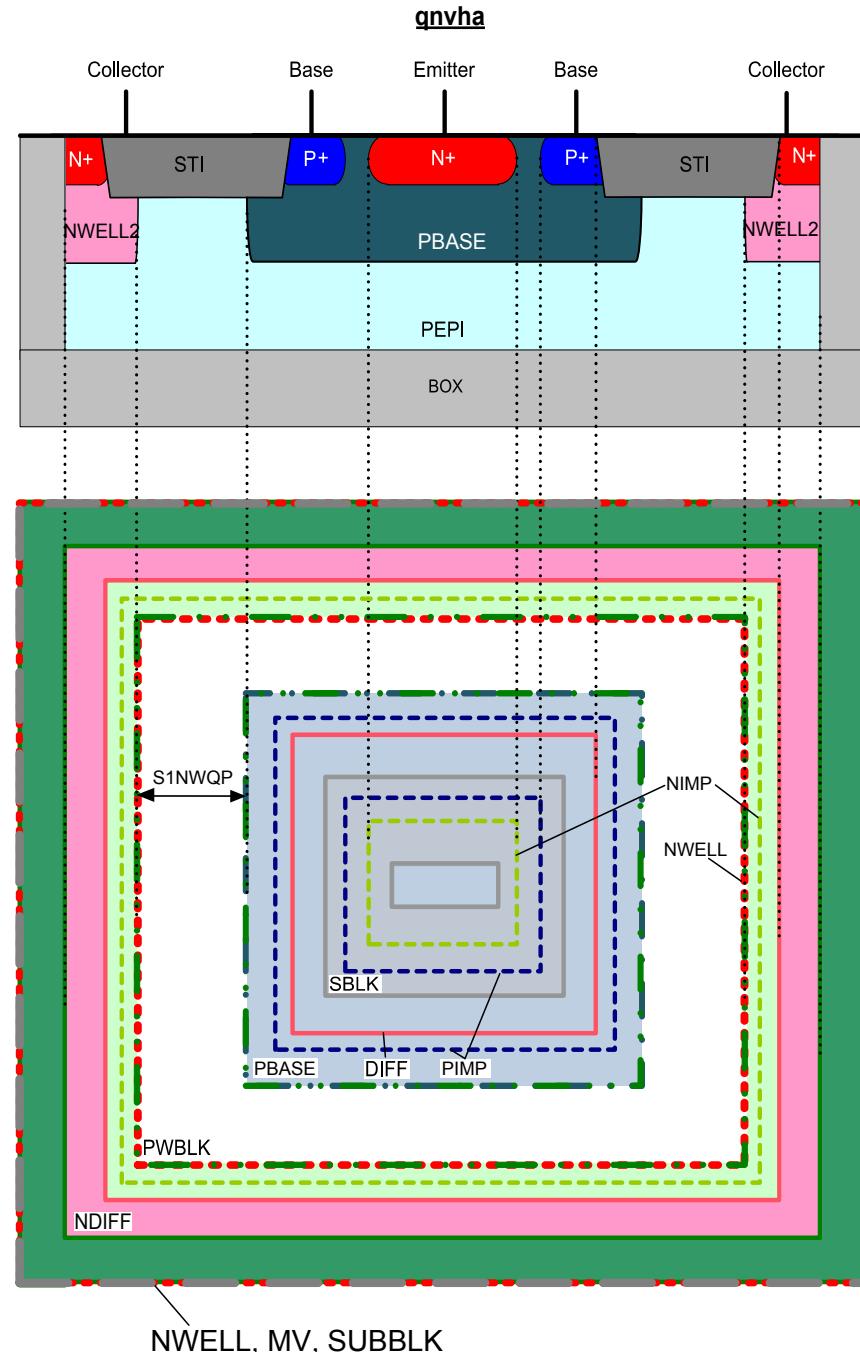
### qnvha

The layout of the qnvha bipolar NPN transistor is predefined and only the emitter length can be changed in the range of 3.0  $\mu\text{m}$  to 100.0  $\mu\text{m}$ . The emitter width is fixed at 2.0  $\mu\text{m}$ .

Name	Description	Value	Unit
S1NWQP	Fixed NWELL spacing to PBASE	3.0	$\mu\text{m}$

**Note:** MV and SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.



**Figure 3.143** qnvha

3. Layer and Device rules → 3.17 DEPL module

## 3.17 DEPL module

### 3.17.1 Layer rules

#### DEPL

Name	Description	Value	Unit
B1DL	DEPL is only allowed in PWELL2, PWELL4, NDF or NDFMV	-	-
B2DL	DEPL overlap of DPC, DFN, HVPWELL, NBASE, PBASE, PZENER, SJNP or SJPN is not allowed	-	-
W1DL	Minimum DEPL width	0.6	μm
S1DL	Minimum DEPL spacing/notch	0.42	μm
S1DLGA	Minimum DEPL spacing to GATE	0.2	μm
E1DLGA	Minimum DEPL enclosure of GATE (except ndhv#, ndmv#)	0.32	μm
A1DL	Minimum DEPL area	0.3844	μm <sup>2</sup>

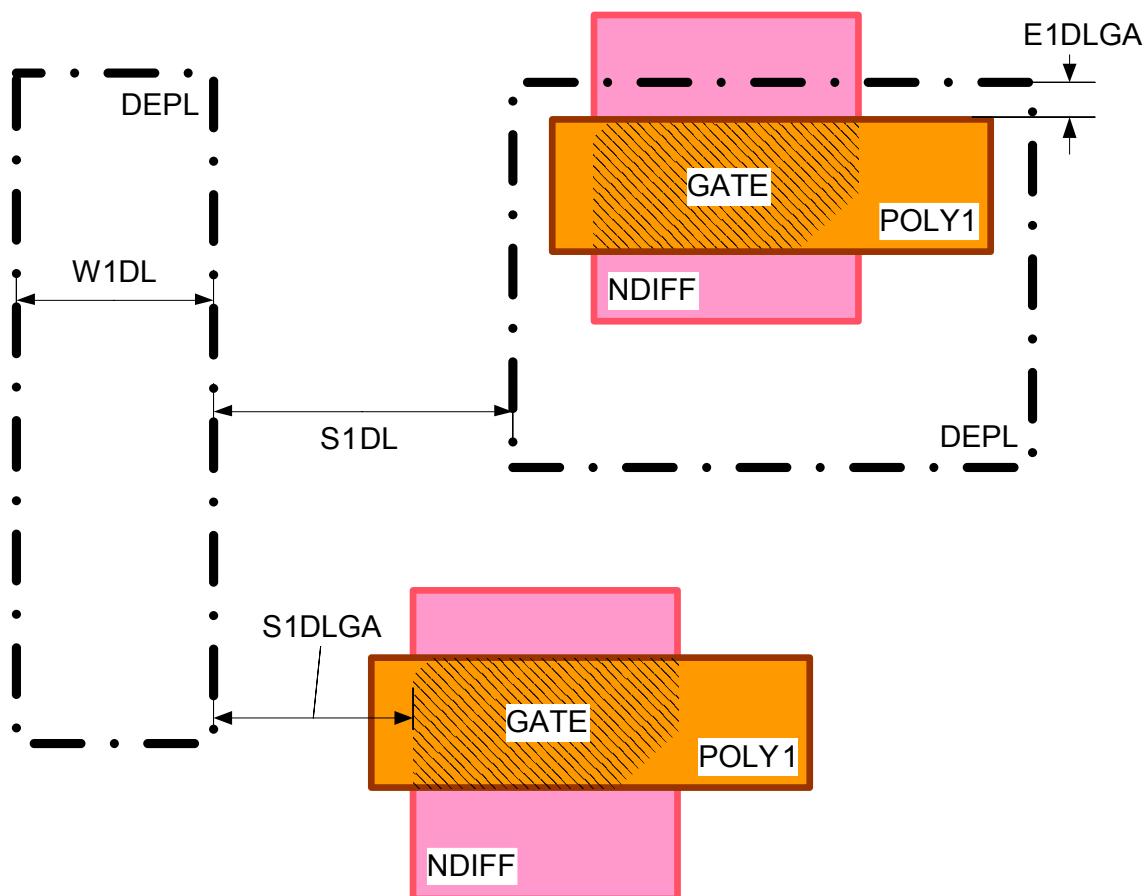


Figure 3.144 DEPL

### 3.17.2 Device rules

#### nd5

Name	Description	Value	Unit
W18GA	Minimum GATE length	0.7	μm
W19GA	Minimum GATE width	0.44	μm

Note: MV is necessary for nd5

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ nd5

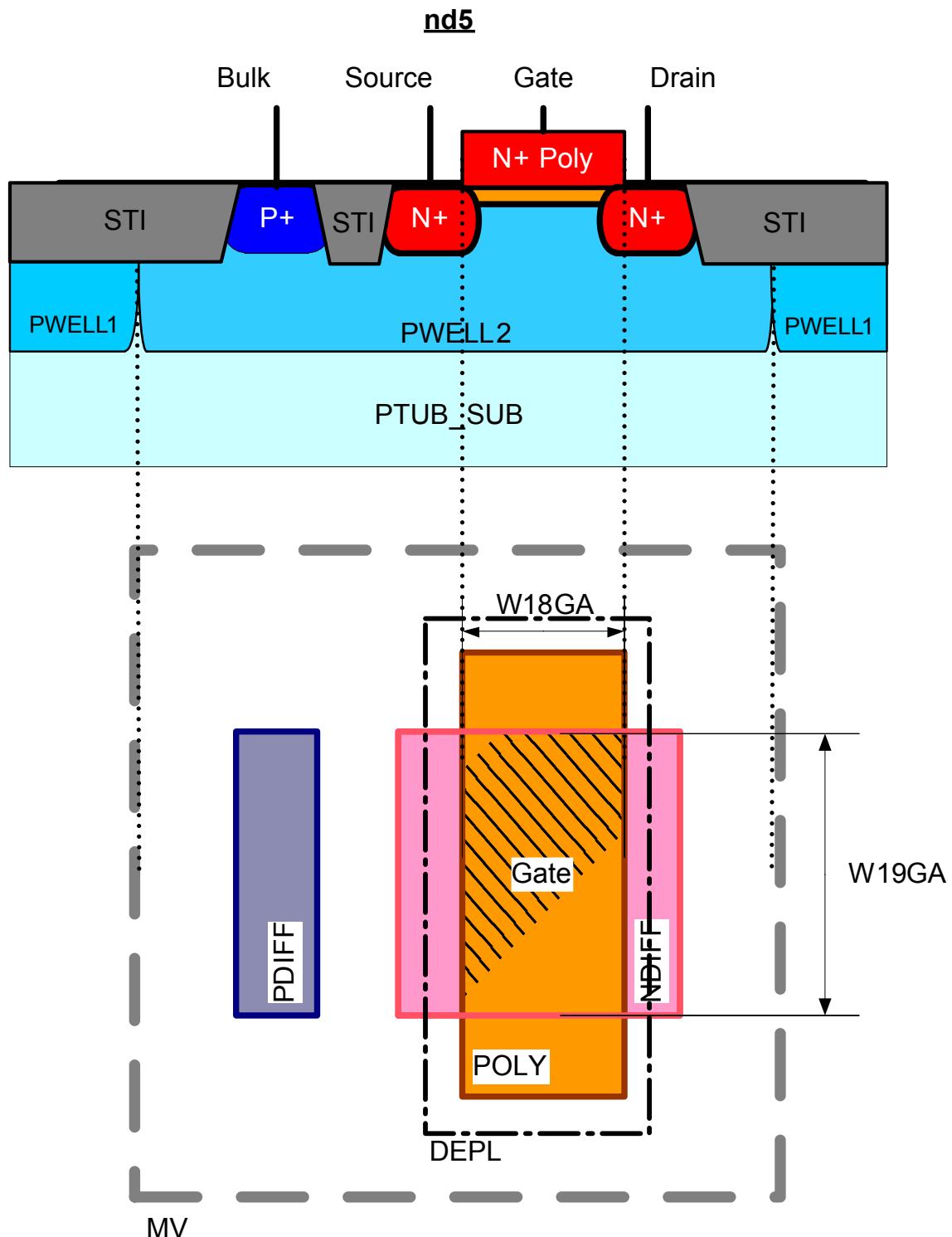


Figure 3.145 nd5

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ ndmvd

## ndmvd

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W33GA	Minimum GATE width	3.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W34GA	Minimum CHANNEL length	0.7	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
W35GA	Maximum CHANNEL length	5.0	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
W5IP	Minimum PIMP width	0.42	µm
S4IN	Minimum NIMP spacing / notch	0.42	µm
S13P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.15	µm
S20DF	Fixed DRAIN-EDGE-STI length	0.45	µm
S3ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.18	µm
S6GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E13P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E5DNP1	Minimum NDIFF extension beyond POLY1	0.27	µm
E9P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.3	µm
O4NDGA	Fixed NDFMV overlap of GATE	0.4	µm

**Note:** MV is necessary for ndmvd

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

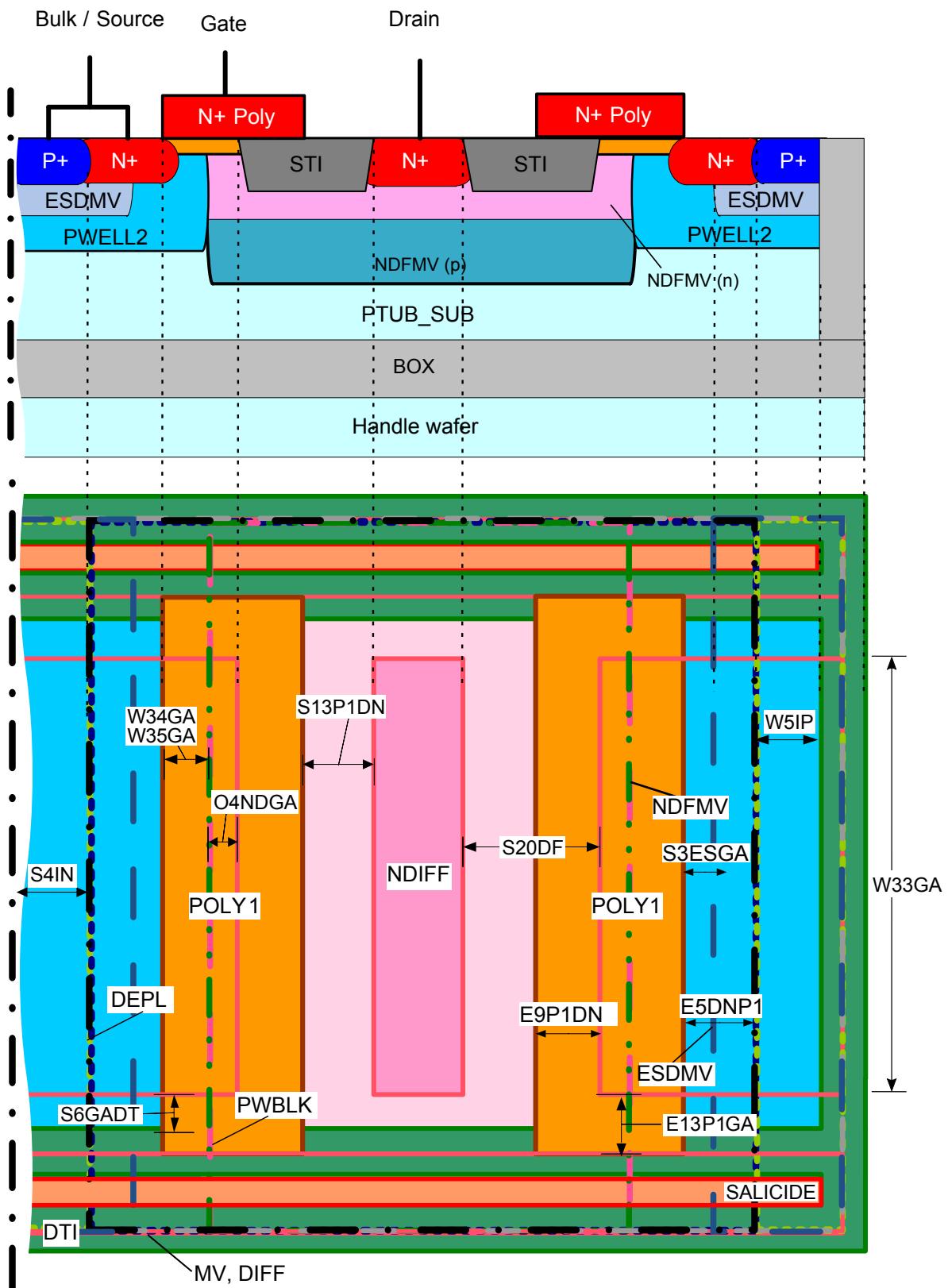
**Note:** ndmvd device must be labeled "ndmvd" using POLY1 (VERIFICATION) layer over GATE

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ ndmvd

### ndmvd



**Figure 3.146** ndmvd

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ ndmvf

## ndmvf

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W33GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.	3.0	µm
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
W34GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.	0.7	µm
W35GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.	5.0	µm
W5IP	Minimum PIMP width	0.42	µm
S4IN	Minimum NIMP spacing / notch	0.42	µm
S3ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.18	µm
S45DF	Fixed DRAIN-EDGE-STI length	1.27	µm
S6GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
S8P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.5	µm
E11P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.77	µm
E13P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E5DNP1	Minimum NDIFF extension beyond POLY1	0.27	µm
O4NDGA	Fixed NDFMV overlap of GATE	0.4	µm

**Note:** MV is necessary for ndmvf

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

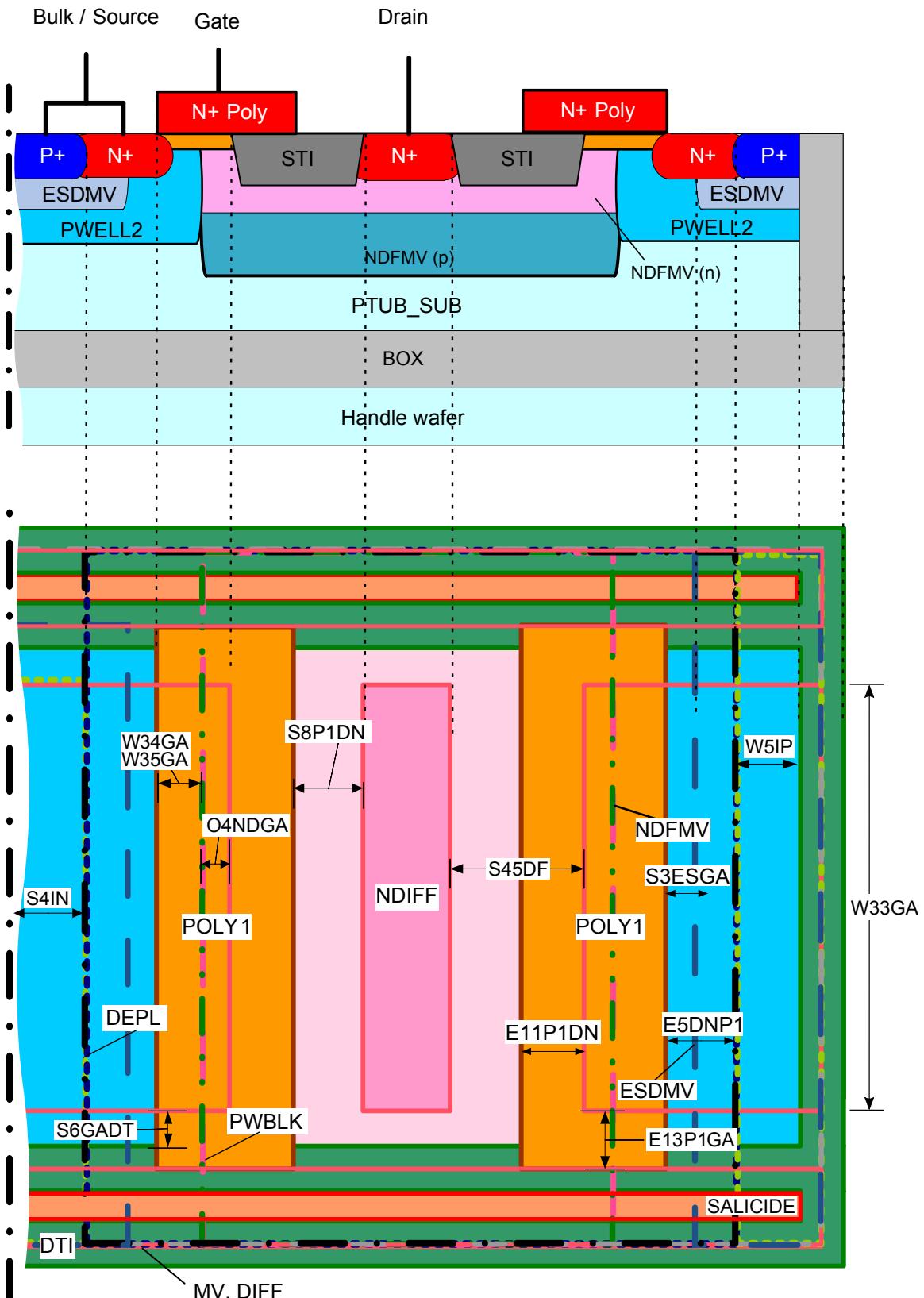
**Note:** ndmvf device must be labeled "ndmvf" using POLY1 (VERIFICATION) layer over GATE

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ ndmvf

### ndmvf



**Figure 3.147** ndmvf

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ ndhvt

## ndhvt

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10HB	ndhvt without SUBBLK is not allowed	-	-
B18MV	ndhvt without MV is not allowed	-	-
B5NX	MET1 is not allowed over NDF (except predefined POLY1 GATE connection, predefined MET1 device terminal connections)	-	-
W21GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	5.0	µm
W3IP	Minimum PIMP width	0.42	µm
W5GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.5	µm
W6GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The GATE fingers must be even number.	3.0	µm
S2PB	Minimum PWBLK spacing/notch	0.6	µm
S3IN	Minimum NIMP spacing/notch	0.42	µm
S10P1DN	Minimum POLY1 spacing to DRAIN NDIFF	1.55	µm
S17DF	Fixed DRAIN-EDGE-STI length	2.4	µm
S5GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E1M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	µm
E2M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	µm
E2NXDN	Minimum NDF enclosure of DRAIN NDIFF	2.5	µm
E2PBP1	Fixed PWBLK enclosure POLY1 in SOURCE region	0.23	µm
E12P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E2P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.85	µm
O1NXP4	Fixed NDF overlap of PWELL4	0.1	µm
O2NXGA	Fixed NDF overlap of GATE	0.65	µm

**Note:** ndhvt device must be labeled "ndhvt" using POLY1 (VERIFICATION) layer over GATE

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** Each transistor must be surrounded by DTI ring.

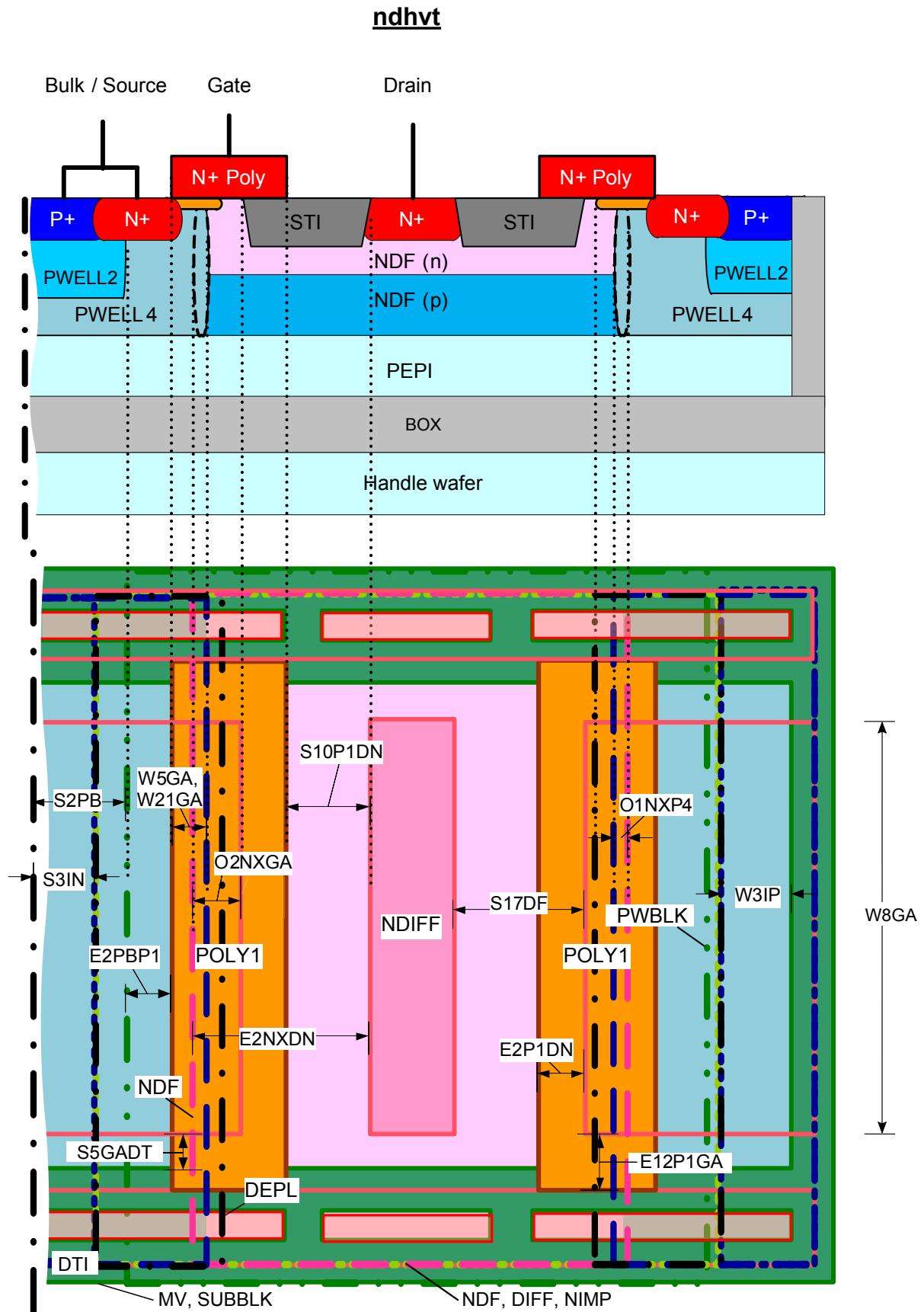
**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.17 DEPL module → 3.17.2 Device rules → ndhvt



**Figure 3.148** ndhvt

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ ndhvta

## ndhvta

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B12HB	ndhvta without SUBBLK is not allowed	-	-
B19MV	ndhvta without MV is not allowed	-	-
W15GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	1.5	μm
W20GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.4	μm
W3IP	Minimum PIMP width	0.42	μm
W6GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The GATE fingers must be even number.	3.0	μm
S2PB	Minimum PWBLK spacing/notch	0.6	μm
S3IN	Minimum NIMP spacing/notch	0.42	μm
S7DF	Fixed DRAIN-EDGE-STI length	1.25	μm
S5GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S7M1	Minimum MET1 of DRAIN NDIFF spacing to MET1	0.28	μm
S7P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.65	μm
E1M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	μm
E1NXDN	Minimum NDF enclosure of DRAIN NDIFF	1.8	μm
E1PBP1	Fixed PWBLK enclosure of POLY1 in SOURCE region	0.18	μm
E2M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	μm
E12P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E2DNP1	Minimum NDIFF extension beyond POLY1	0.27	μm
E6P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.6	μm
O1NXGA	Fixed NDF overlap of GATE	0.55	μm

**Note:** ndhvta device must be labeled "ndhvta" using POLY1 (VERIFICATION) layer over GATE

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** Each transistor must be surrounded by DTI ring.

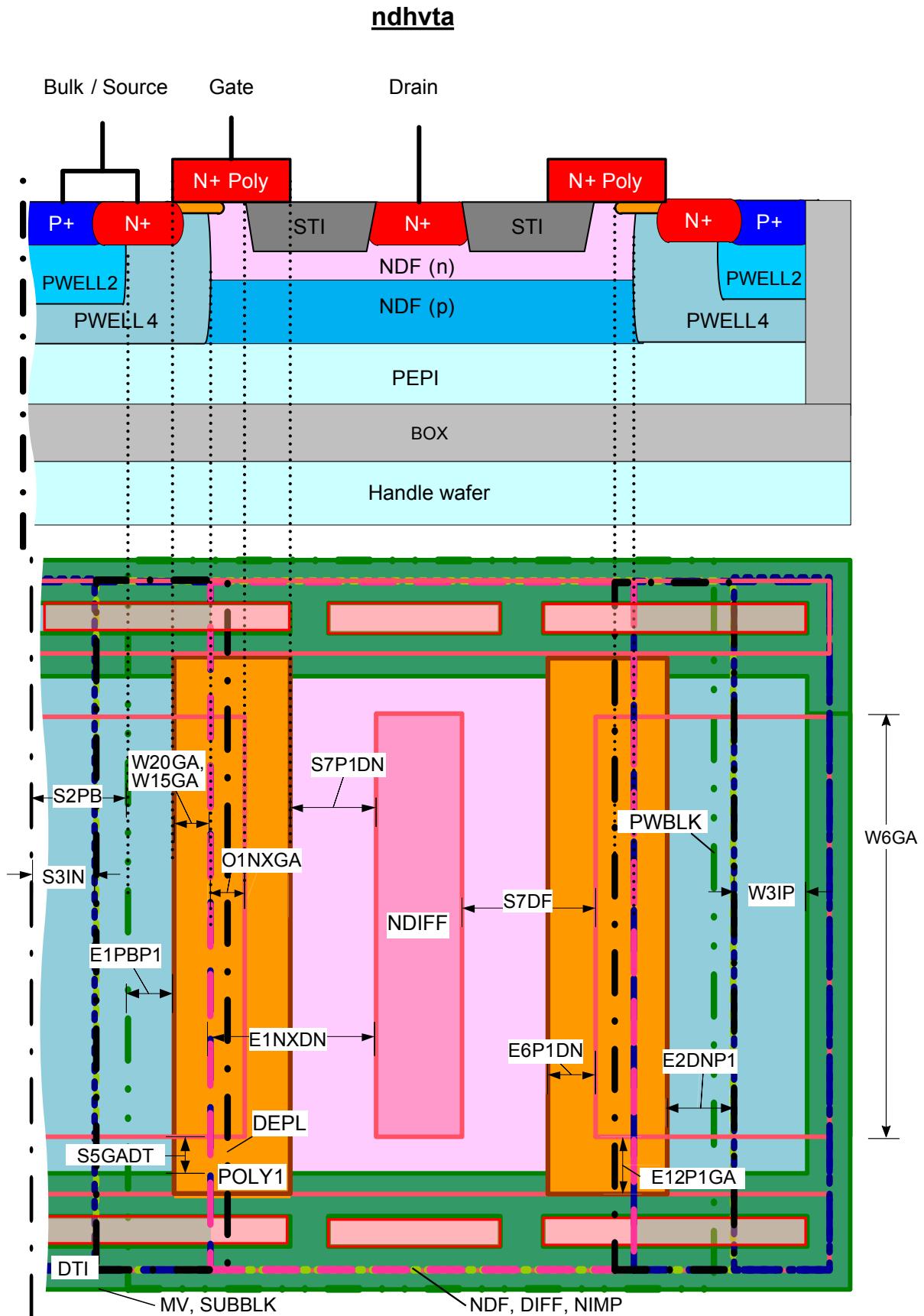
**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.17 DEPL module → 3.17.2 Device rules → ndhvta



**Figure 3.149** ndhvta

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ ndhvtaa

## ndhvtaa

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B15HB	ndhvtaa without SUBBLK is not allowed	-	-
B21MV	ndhvtaa without MV is not allowed	-	-
W15GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	1.5	μm
W20GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.4	μm
W3IP	Minimum PIMP width	0.42	μm
W6GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The GATE fingers must be even number.	3.0	μm
S2PB	Minimum PWBLK spacing/notch	0.6	μm
S3IN	Minimum NIMP spacing/notch	0.42	μm
S49DF	Fixed DRAIN-EDGE-STI length	1.35	μm
S11GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	2.5	μm
S7M1	Minimum MET1 of DRAIN NDIFF spacing to MET1	0.28	μm
S7P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.65	μm
E17M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	4.0	μm
E1M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	μm
E1NXDN	Minimum NDF enclosure of DRAIN NDIFF	1.8	μm
E1PBP1	Fixed PWBLK enclosure of POLY1 in SOURCE region	0.18	μm
E17P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	3.0	μm
E27P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.7	μm
E2DNP1	Minimum NDIFF extension beyond POLY1	0.27	μm
O4NXGA	Fixed NDF overlap of GATE	0.45	μm

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** ndhvtaa device must be labeled "ndhvtaa" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.17 DEPL module→ 3.17.2 Device rules→ ndhvtaa

### ndhvtaa

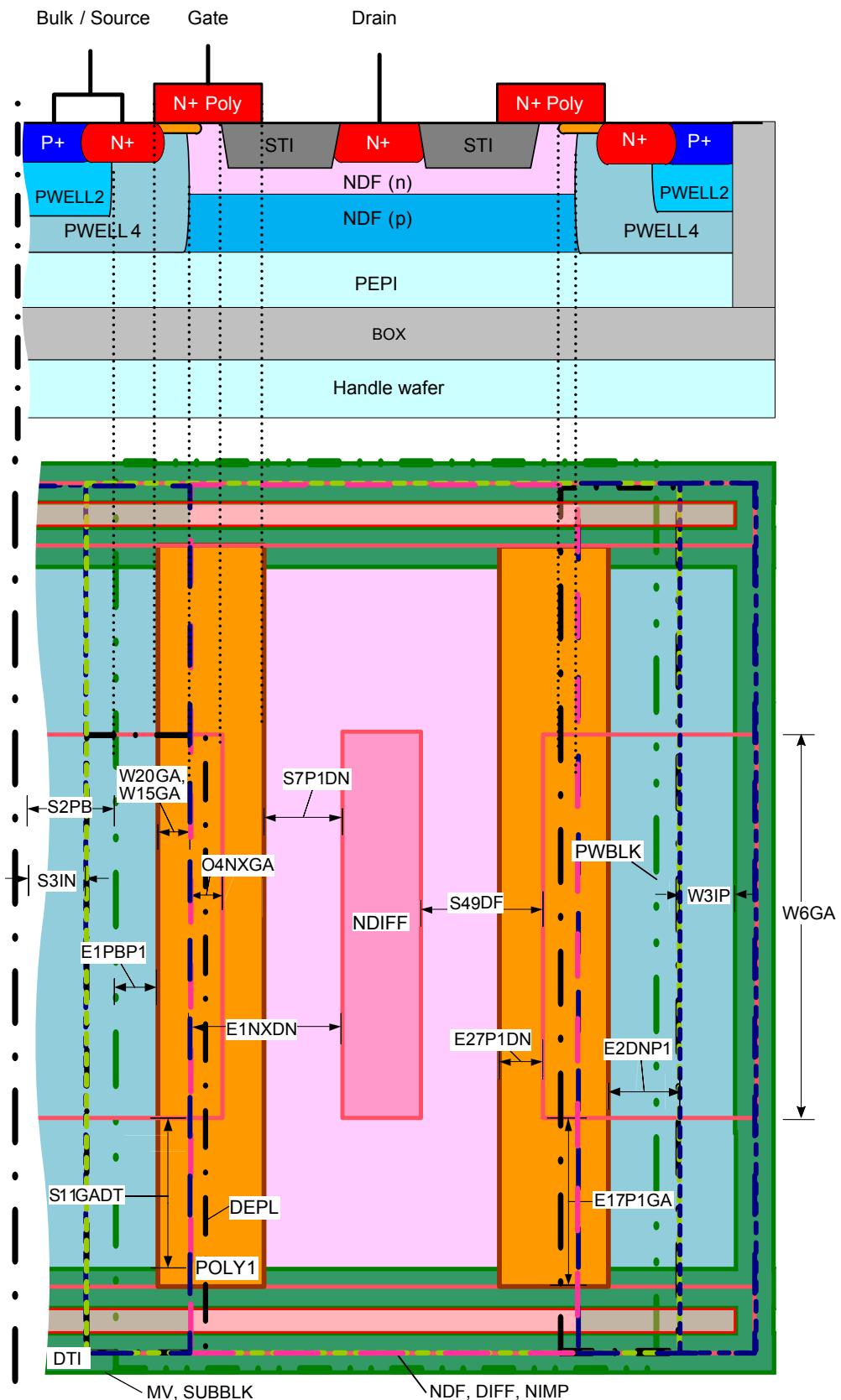


Figure 3.150 ndhvtaa

3. Layer and Device rules → 3.18 HVDEPL module

## 3.18 HVDEPL module

### 3.18.1 Layer rules

#### HVDEPL

Name	Description	Value	Unit
B1HL	HVDEPL is only allowed in PWELL2, PWELL4 or DFN	-	-
B2HL	HVDEPL overlap of DPC, NDF, NDFMV, PDFMV, HVPWELL, NBASE, PBASE, PZENER, SJNP or SJPN is not allowed	-	-
B3HL	HVDEPL overlap of DEPL is not allowed	-	-
W1HL	Minimum HVDEPL width	0.6	μm
S1HL	Minimum HVDEPL spacing / notch	0.42	μm
S1HLGA	Minimum HVDEPL spacing to GATE	0.2	μm
E1HLGA	Minimum HVDEPL enclosure of GATE	0.32	μm
A1HL	Minimum HVDEPL area	0.3844	μm <sup>2</sup>

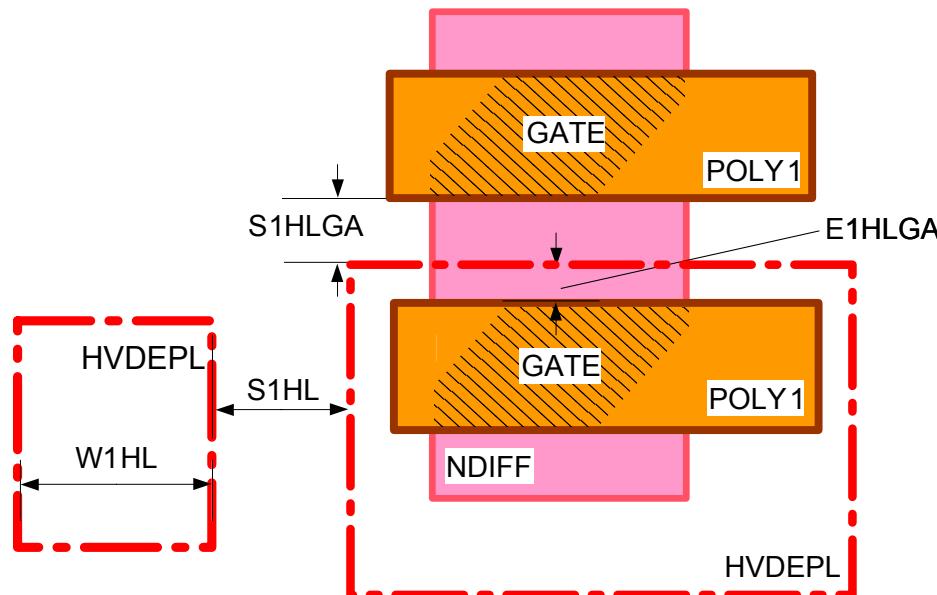


Figure 3.151 HVDEPL

### 3.18.2 Device rules

#### ndhvrd

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W56GA	Minimum CHANNEL length  Note: CHANNEL for this device is defined as GATE AND PWELL4.	0.5	μm
W57GA	Minimum GATE width  Note: Minimum GATE width is defined as single GATE finger width.  Note: Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  Note: Minimum GATE width is defined as minimum GATE finger width.	3.0	μm
W59GA	Maximum CHANNEL length  Note: CHANNEL for this device is defined as GATE AND PWELL4.	5.0	μm



## 3. Layer and Device rules → 3.18 HVDEPL module→ 3.18.2 Device rules→ ndhvr

Name	Description	Value	Unit
S22P1DN	Minimum POLY1 spacing to DRAIN NDIFF (in the direction of GATE length)	3.1	µm
S40DF	Fixed DRAIN-EDGE-STI length	4.1	µm
S8GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E2M2DN	Minimum MET2 enclosure of DRAIN NDIFF (in the direction of GATE width)	3.0	µm
E4M2DN	Fixed MET2 enclosure of DRAIN NDIFF (in the direction of GATE length)	1.1	µm
E6M1DN	Minimum MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	µm
E8M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	1.0	µm
E12DNP1	Minimum NDIFF extension beyond POLY1	0.32	µm
E15P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E18P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	1.0	µm
O1FNGA	Fixed DFN overlap of GATE	0.95	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** ndhvr device must be labeled "ndhvr" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

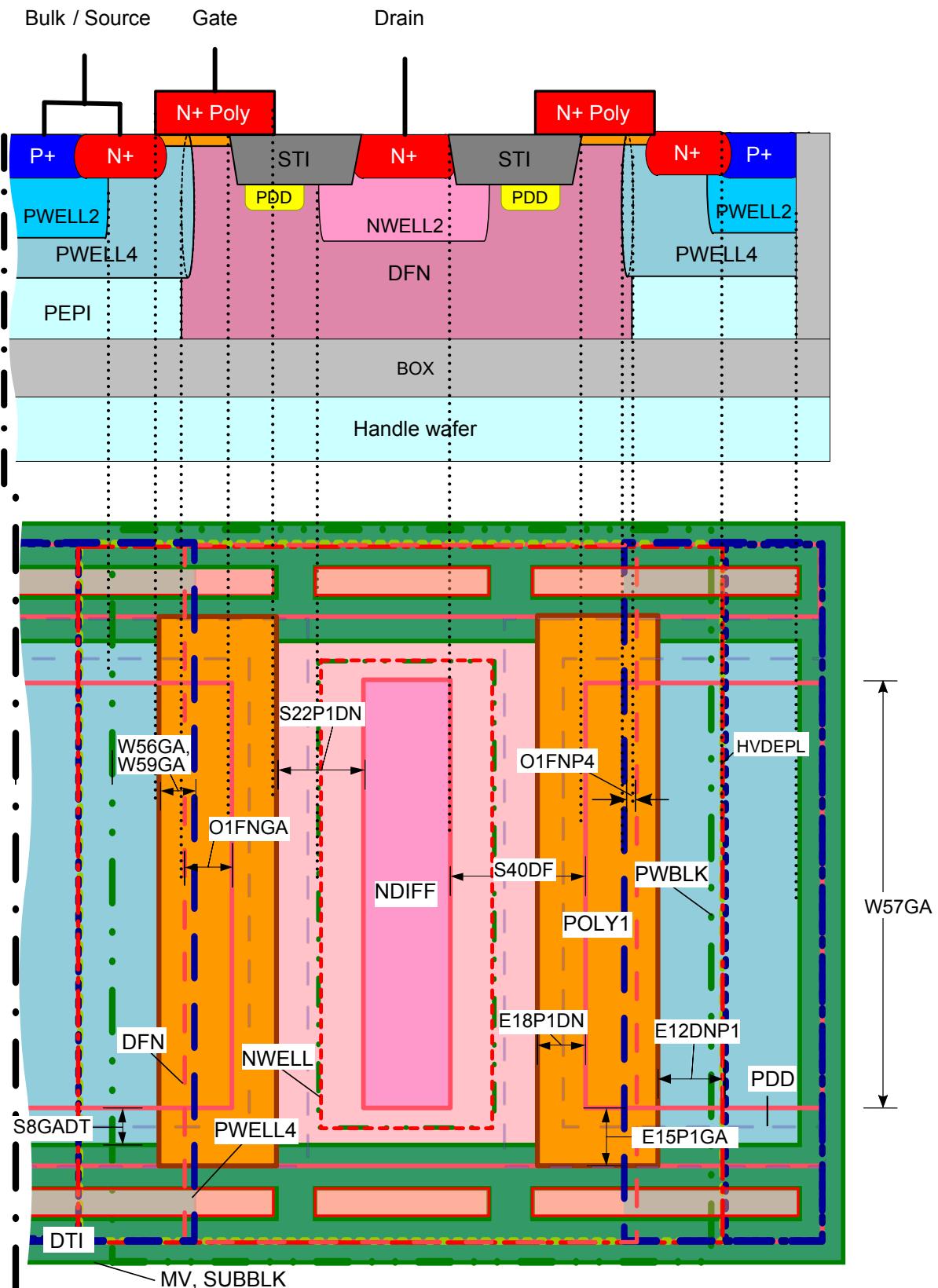
**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.18 HVDEPL module → 3.18.2 Device rules → ndhvrd

### ndhvrd



**Figure 3.152** ndhvrd

3. Layer and Device rules → 3.18 HVDEPL module → 3.18.2 Device rules → ndhvrf

## ndhvrf

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W56GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.5	µm
W57GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	µm
W59GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	5.0	µm
S21P1DN	Minimum POLY1 spacing to DRAIN NDIFF (in the direction of GATE length)	5.95	µm
S33DF	Fixed DRAIN-EDGE-STI length	7.0	µm
S8GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E2M2DN	Minimum MET2 enclosure of DRAIN NDIFF (in the direction of GATE width)	3.0	µm
E3M2DN	Fixed MET2 enclosure of DRAIN NDIFF (in the direction of GATE length)	2.1	µm
E6M1DN	Minimum MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	µm
E7M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	2.0	µm
E12DNP1	Minimum NDIFF extension beyond POLY1	0.32	µm
E15P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E17P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	1.05	µm
O1FNGA	Fixed DFN overlap of GATE	0.95	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** ndhvrf device must be labeled "ndhvrf" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

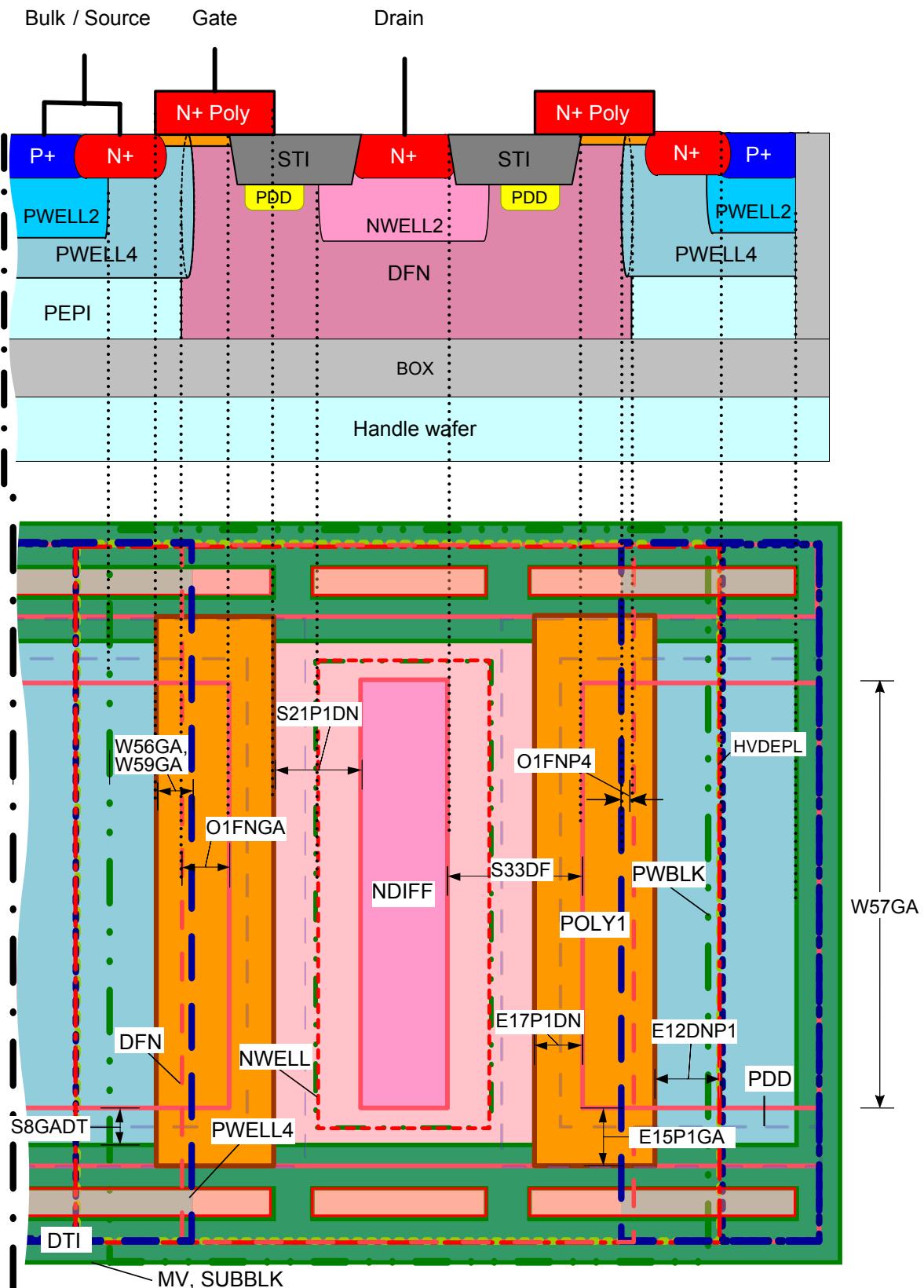
**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.18 HVDEPL module → 3.18.2 Device rules → ndhvrf

### ndhvrf



**Figure 3.153** ndhvrf

3. Layer and Device rules → 3.19 1XN module

## 3.19 1XN module

### 3.19.1 Layer rules

#### SJNP

Name	Description	Value	Unit
B10NT	SJNP overlap of NDF, PDF, NDFMV, PDFMV, DFN, DFP, PWELL4, NBASE, PBASE is not allowed	-	-
B1NT	SJNP without PWBLK, SUBBLK and MV is not allowed	-	-
B2NT	SJNP overlap of HWTUB, NWELL, HVNWELL, HVPWELL, PIMP, HRES or MRES is not allowed	-	-
B3NT	SJNP overlap of POLY1 or NIMP is not allowed (except nhsj1_# CHANNEL region and nisj1_16)	-	-
B4NT	SJNP overlap of SJPN is not allowed	-	-
B8NT	SJNP without DIFF is not allowed (except nhsj1_# CHANNEL region and nisj1_16)	-	-
W1NT	Minimum SJNP width	2.0	μm
S1NT	Minimum SJNP spacing/notch	1.5	μm
S1NTPT	Minimum SJNP spacing to SJPN	2.0	μm
A1NT	Minimum SJNP area	9.5	μm <sup>2</sup>

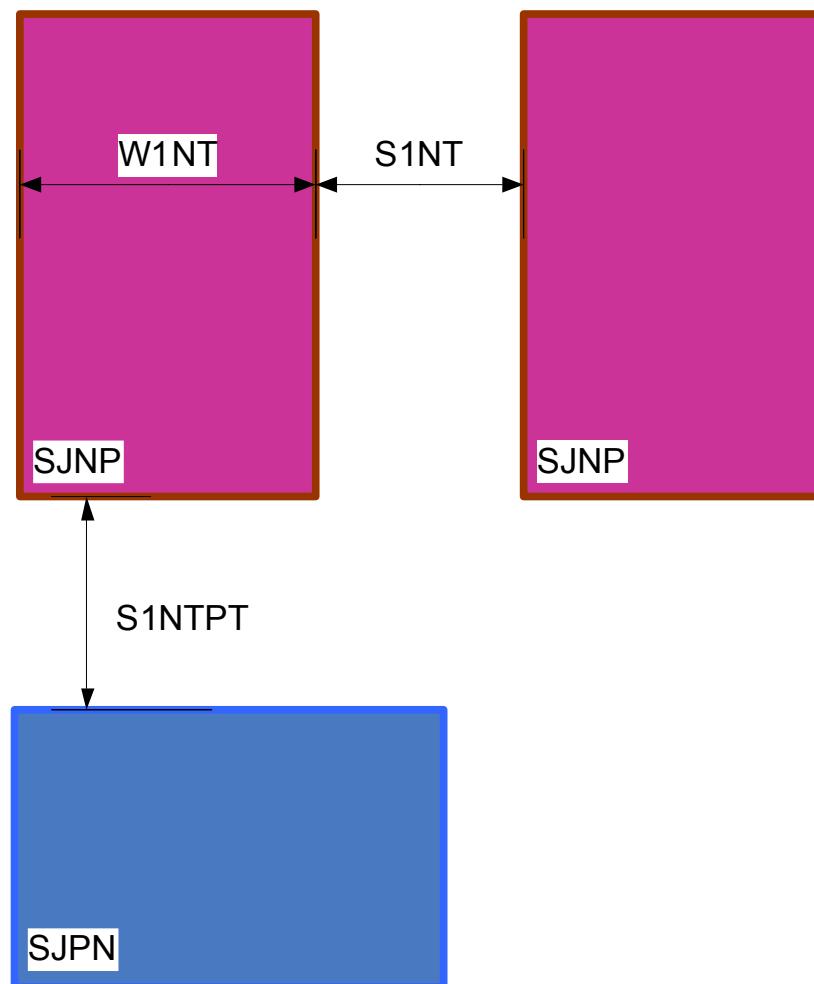


Figure 3.154 SJNP

3. Layer and Device rules → 3.19 1XN module→ 3.19.1 Layer rules→ SJNP\_E

## SJNP\_E

Name	Description	Value	Unit
W2NT	Minimum SJNP_E width	0.5	μm

### 3.19.2 Device rules

#### nhsj1\_7

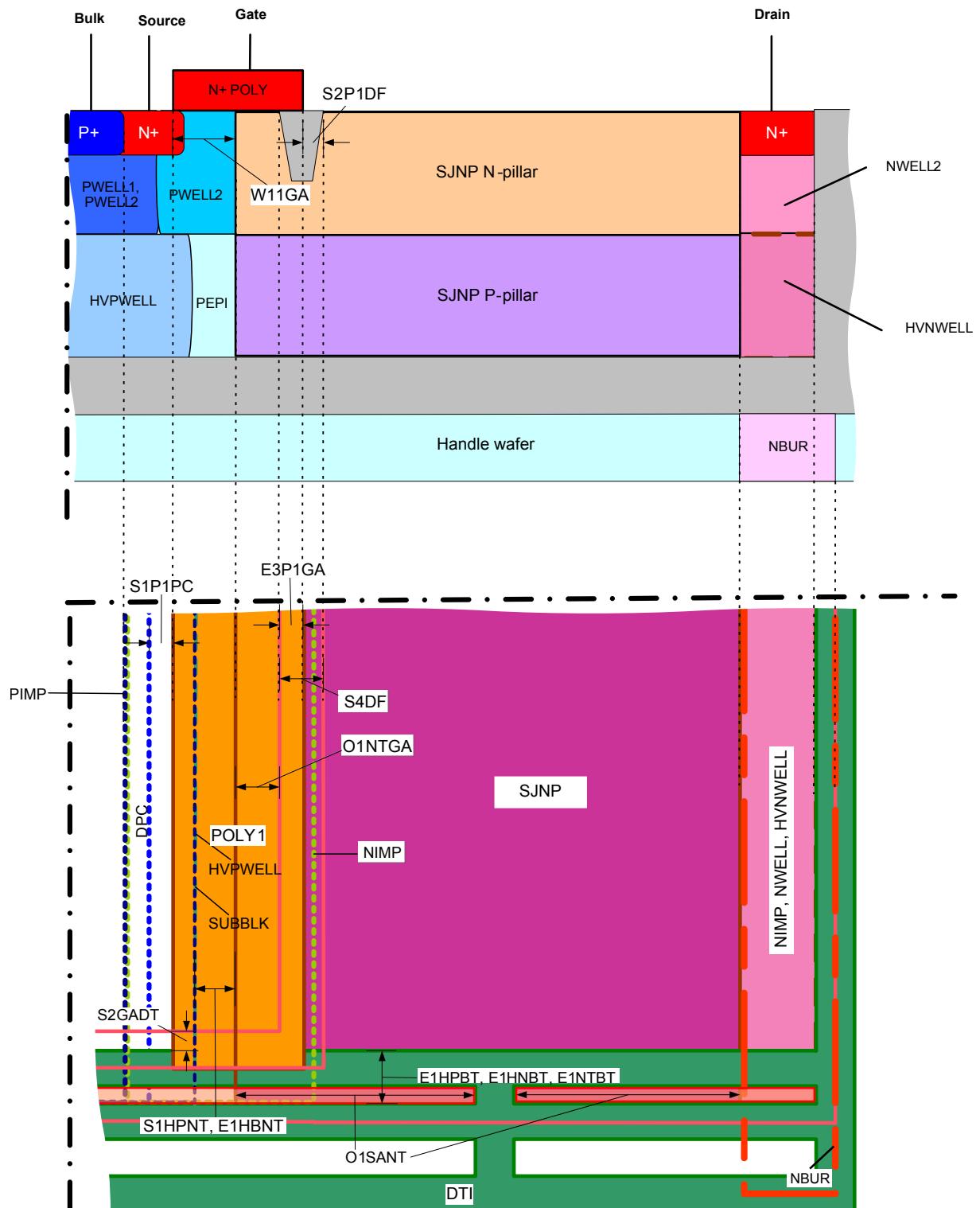
The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11NT	This device must be used together with a dhw2a, dhw2 or dhw3	-	-
B3MV	nhsj1_# without MV is not allowed	-	-
B5NT	DRAIN NBUR must connect to HWNTUB	-	-
B6NT	Fixed orientation is 0 degree or 180 degree	-	-
W11GA	Minimum CHANNEL length	0.5	μm
	Minimum GATE width	10.0	μm
W1GA	<b>Note:</b> Device finger width of nhsj1_# is defined as GATE finger width + 1 μm		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
S4DF	Fixed DRAIN-EDGE-STI length	1.0	μm
S1HPNT	Fixed HVPWELL spacing to SJNP (in CHANNEL region)	0.5	μm
S1P1PC	Fixed POLY1 spacing to DPC (in the direction of GATE length)	0.2	μm
S2GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S2P1DF	Minimum POLY1 spacing to DRAIN DIFF	0.48	μm
S4IPDN	Minimum PIMP spacing to NDIFF	0.14	μm
E1HBNT	Fixed SUBBLK enclosure of SJNP (in CHANNEL region)	0.5	μm
E1HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	1.5	μm
E1HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	1.5	μm
E1NTBT	Fixed extension of SJNP beyond TUB (in the direction of device width)	1.5	μm
E3INDF	Minimum NIMP extension beyond SOURCE NDIFF	0.14	μm
E3IPDF	Minimum PIMP extension beyond PDIF	0.14	μm
E3P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.52	μm
O1NTGA	Fixed SJNP overlap of GATE	1.5	μm
O1SANT	Fixed SALICIDE overlap of SJNP	3.0	μm
O1F1NT	Fixed M1_FPLATE overlap of SJNP	3.0	μm

**Note:** Maximum CHANNEL length is 5 μm

**Note:** NBUR connection to dhw# is not shown in the diagram.

## 3. Layer and Device rules → 3.19 1XN module→ 3.19.2 Device rules→ nhsj1\_7

**Figure 3.155 nhsj1\_7**

3. Layer and Device rules → 3.19 1XN module→ 3.19.2 Device rules→ nhsj1\_10

## nhsj1\_10

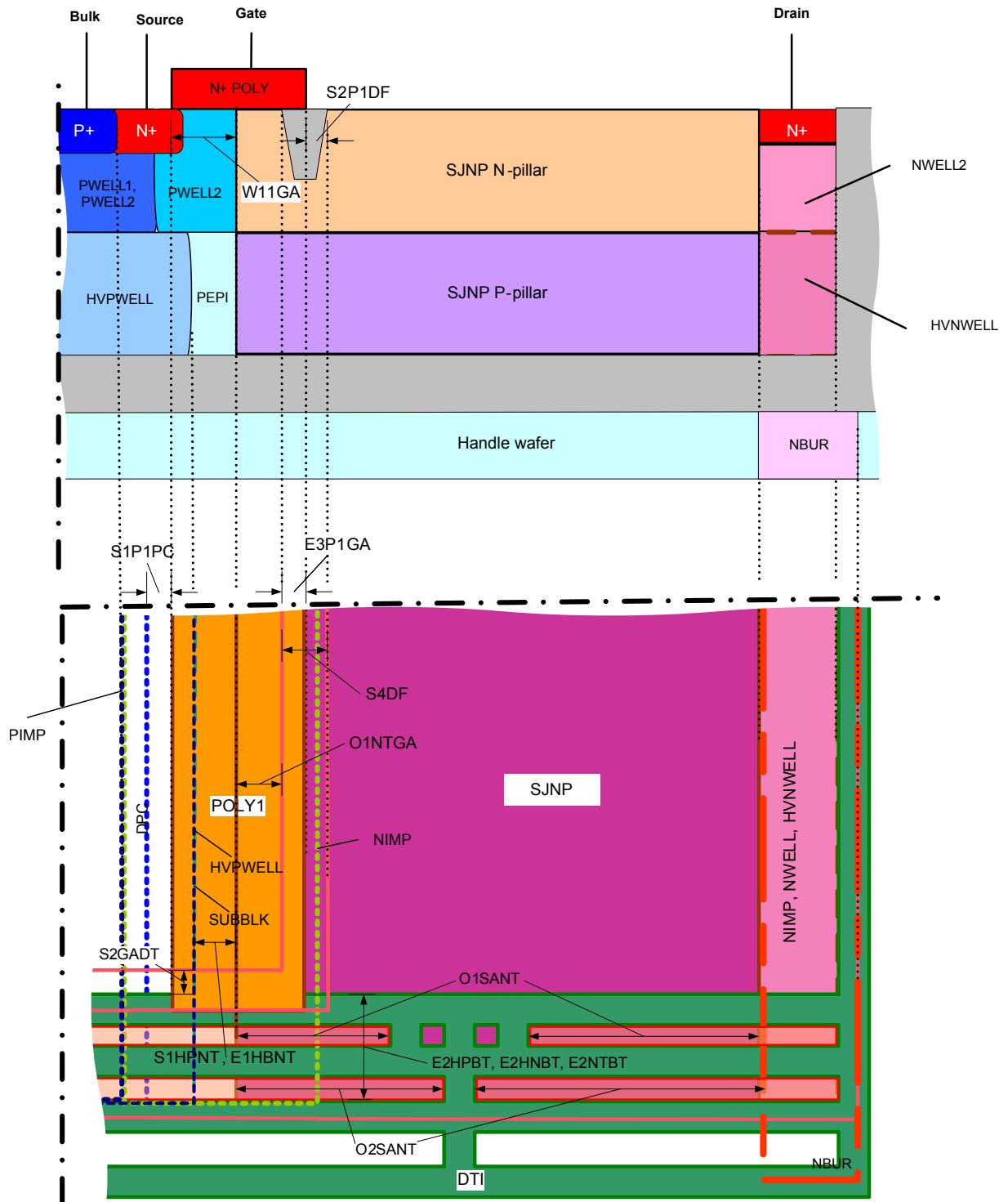
The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B12NT	This device must be used together with a dhw2 or dhw3	-	-
B3MV	nhsj1_# without MV is not allowed	-	-
B5NT	DRAIN NBUR must connect to HWNTUB	-	-
B6NT	Fixed orientation is 0 degree or 180 degree	-	-
W11GA	Minimum CHANNEL length	0.5	μm
W1GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Device finger width of nhsj1_# is defined as GATE finger width + 1 μm		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
S4DF	Fixed DRAIN-EDGE-STI length	1.0	μm
S1HPNT	Fixed HVPWELL spacing to SJNP (in CHANNEL region)	0.5	μm
S1P1PC	Fixed POLY1 spacing to DPC (in the direction of GATE length)	0.2	μm
S2GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S2P1DF	Minimum POLY1 spacing to DRAIN DIFF	0.48	μm
S4IPDN	Minimum PIMP spacing to NDIFF	0.14	μm
E1HBNT	Fixed SUBBLK enclosure of SJNP (in CHANNEL region)	0.5	μm
E2HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	3.0	μm
E2HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	3.0	μm
E2NTBT	Fixed extension of SJNP beyond TUB (in the direction of device width)	3.0	μm
E3INDF	Minimum NIMP extension beyond SOURCE NDIFF	0.14	μm
E3IPDF	Minimum PIMP extension beyond PDIFF	0.14	μm
E3P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.52	μm
O1NTGA	Fixed SJNP overlap of GATE	1.5	μm
O1SANT	Fixed SALICIDE overlap of SJNP	3.0	μm
O2SANT	Fixed SALICIDE overlap of SJNP	4.5	μm
O1F1NT	Fixed M1_FPLATE overlap of SJNP	3.0	μm
O4F2NT	Fixed M2_FPLATE overlap of SJNP	4.5	μm

**Note:** Maximum CHANNEL length is 5 μm

**Note:** NBUR connection to dhw# is not shown in the diagram.

## 3. Layer and Device rules → 3.19 1XN module→ 3.19.2 Device rules→ nhsj1\_10

**Figure 3.156 nhsj1\_10**

3. Layer and Device rules → 3.19 1XN module→ 3.19.2 Device rules→ nhsj1\_16c

### **nhsj1\_16c**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13NT	This device must be used together with dhw3	-	-
B3MV	nhsj1_# without MV is not allowed	-	-
B5NT	DRAIN NBUR must connect to HWNTUB	-	-
B6NT	Fixed orientation is 0 degree or 180 degree	-	-
W11GA	Minimum CHANNEL length	0.5	μm
W26GA	Minimum GATE width	20.0	μm
	<b>Note:</b> Device finger width of nhsj1_# is defined as GATE finger width + 1 μm		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
S4DF	Fixed DRAIN-EDGE-STI length	1.0	μm
S1HPNT	Fixed HVPWELL spacing to SJNP (in CHANNEL region)	0.5	μm
S1P1PC	Fixed POLY1 spacing to DPC (in the direction of GATE length)	0.2	μm
S2GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S2P1DF	Minimum POLY1 spacing to DRAIN DIFF	0.48	μm
S4IPDN	Minimum PIMP spacing to NDIFF	0.14	μm
E1HBNT	Fixed SUBBLK enclosure of SJNP (in CHANNEL region)	0.5	μm
E2HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	3.0	μm
E2HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	3.0	μm
E2NTBT	Fixed extension of SJNP beyond TUB (in the direction of device width)	3.0	μm
E3INDF	Minimum NIMP extension beyond SOURCE NDIFF	0.14	μm
E3IPDF	Minimum PIMP extension beyond PDIFF	0.14	μm
E3P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.52	μm
O1NTGA	Fixed SJNP overlap of GATE	1.5	μm
O1SANT	Fixed SALICIDE overlap of SJNP	3.0	μm
O3SANT	Fixed SALICIDE overlap of SJNP	6.0	μm
O1F1NT	Fixed M1_FPLATE overlap of SJNP	3.0	μm
O4F2NT	Fixed M2_FPLATE overlap of SJNP	4.5	μm
O1F3NT	Fixed M3_FPLATE overlap of SJNP	6.0	μm

**Note:** nhsj1\_16c device must be labeled "nhsj1\_16c" using POLY1 (VERIFICATION) layer over the GATE

**Note:** Maximum CHANNEL length is 5 μm

**Note:** NBUR connection to dhw# is not shown in the diagram.

## 3. Layer and Device rules → 3.19 1XN module → 3.19.2 Device rules → nhsj1\_16c

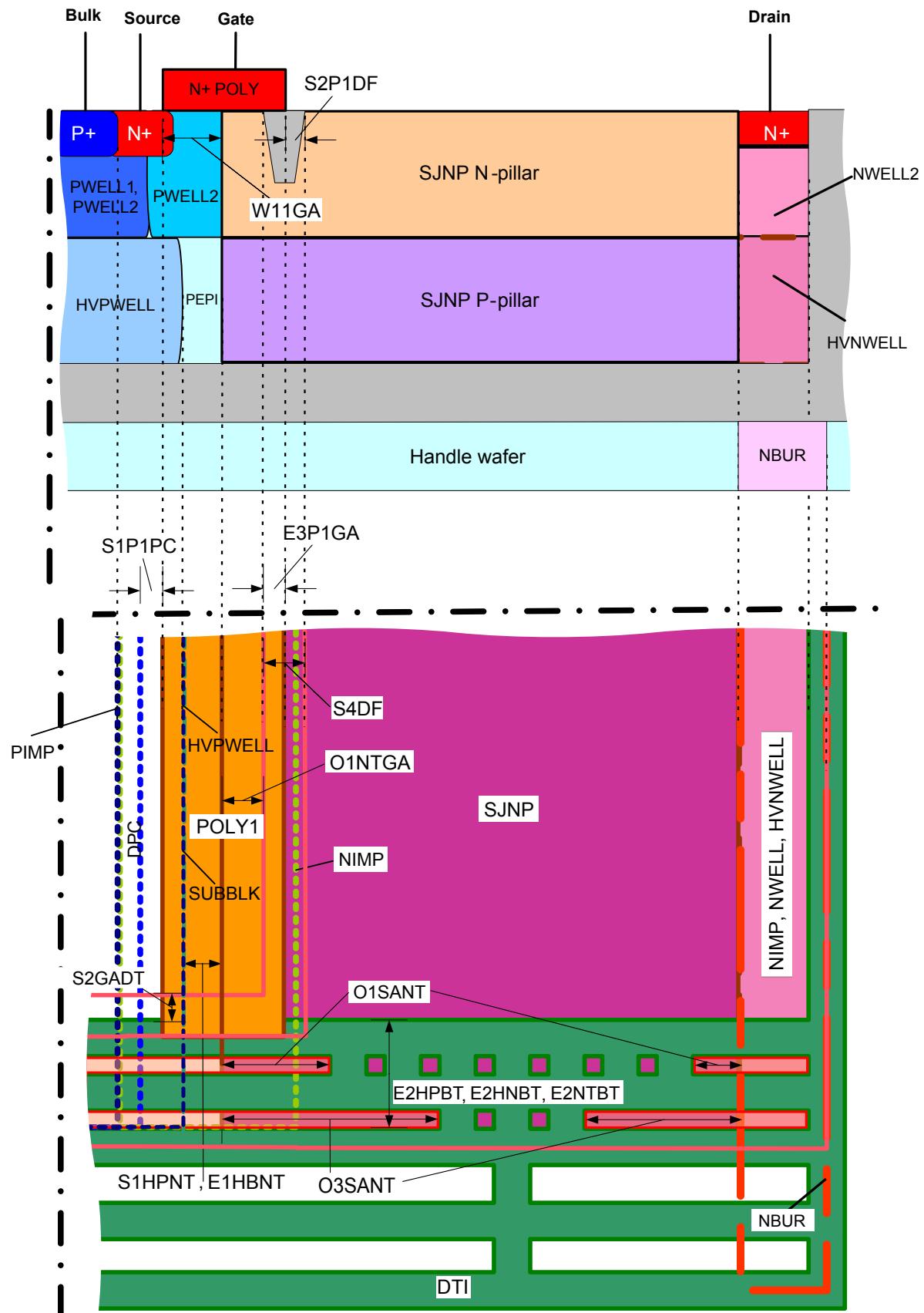


Figure 3.157 nhsj1\_16c

3. Layer and Device rules → 3.19 1XN module→ 3.19.2 Device rules→ dfwnsj1\_7

### **dfwnsj1\_7**

The layout is predefined and scalable concerning width. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11NT	This device must be used together with a dhw2a, dhw2 or dhw3	-	-
B4MV	dfwnsj1_# without MV is not allowed	-	-
B6NT	Fixed orientation is 0 degree or 180 degree	-	-
B7NT	Cathode dfwnsj1_# NBUR must connect to HWNTUB	-	-
E1HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	1.5	µm
E1HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	1.5	µm
E1NTBT	Fixed extension of SJNP beyond TUB (in the direction of device width)	1.5	µm
O1SANT	Fixed SALICIDE overlap of SJNP	3.0	µm
O1F1NT	Fixed M1_FPLATE overlap of SJNP	3.0	µm

**Note:** Minimum drawn finger width is 10 µm

**Note:** NBUR connection to dhw# is not shown in the diagram.

3. Layer and Device rules → 3.19 1XN module → 3.19.2 Device rules → dwnsj1\_7

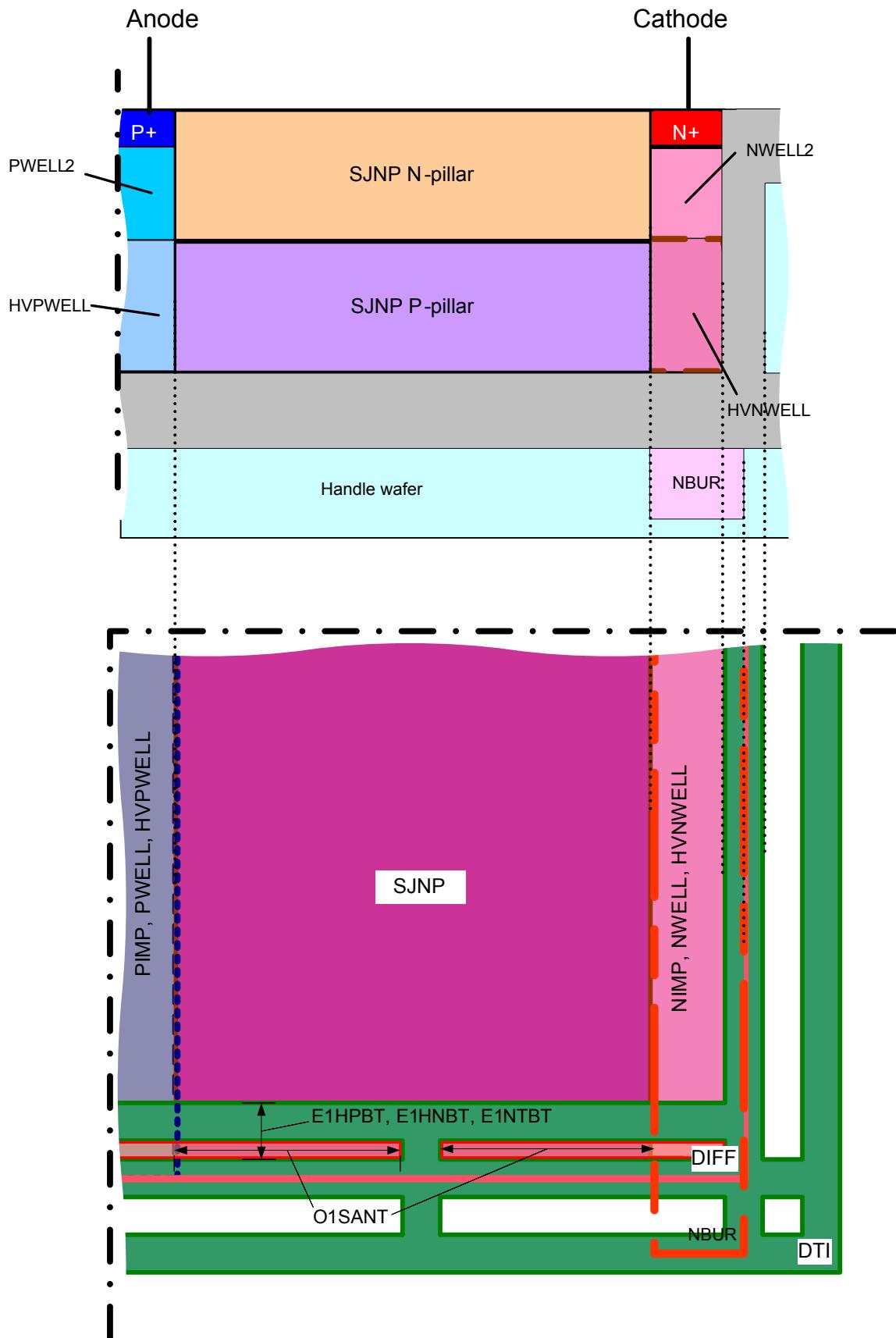


Figure 3.158 dwnsj1\_7

3. Layer and Device rules → 3.19 1XN module→ 3.19.2 Device rules→ dfwnsj1\_10

### **dfwnsj1\_10**

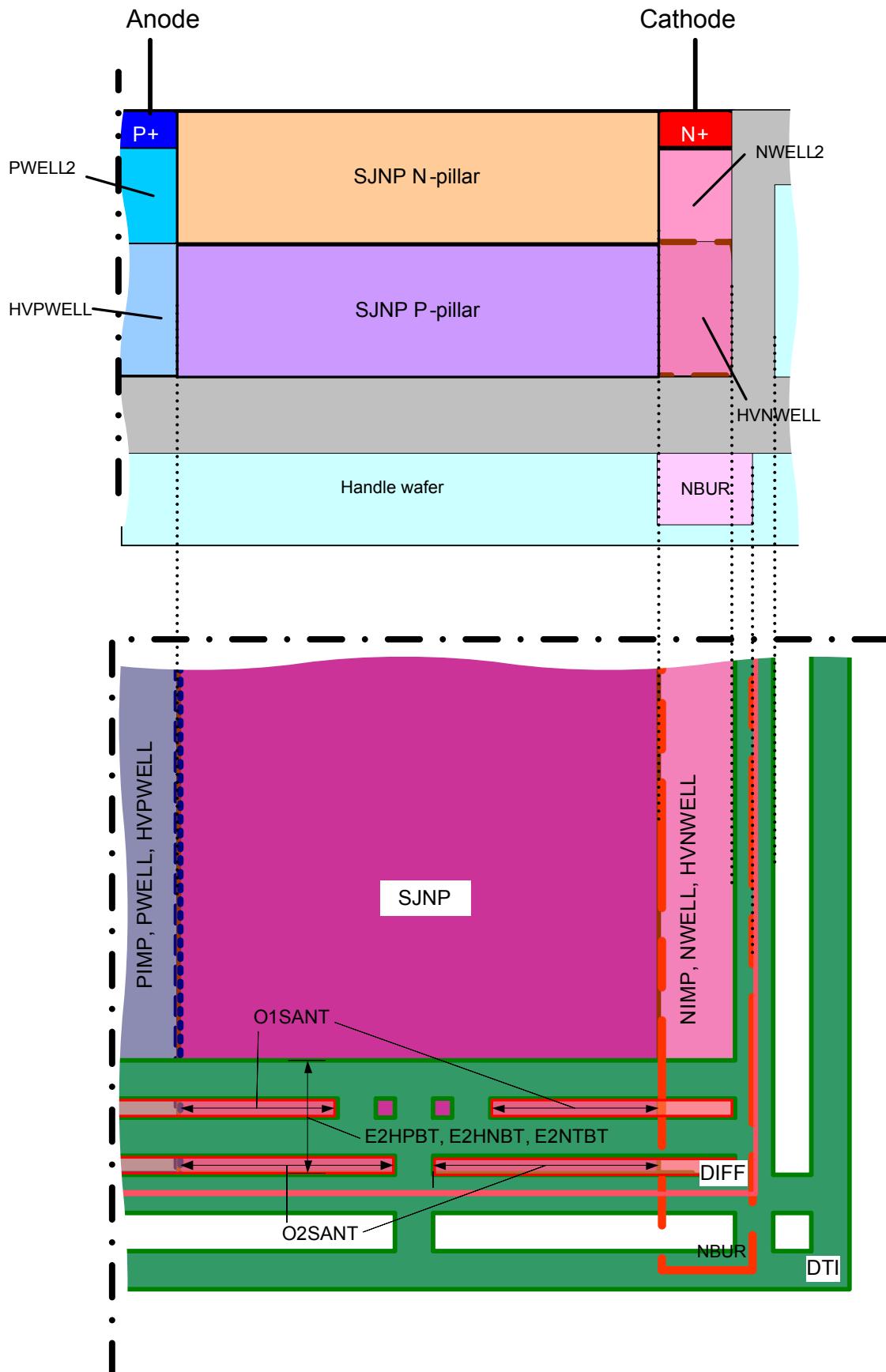
The layout is predefined and scalable concerning width. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B4MV	dfwnsj1_# without MV is not allowed	-	-
B6NT	Fixed orientation is 0 degree or 180 degree	-	-
B7NT	Cathode dfwnsj1_# NBUR must connect to HWNTUB	-	-
E2HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	3.0	µm
E2HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	3.0	µm
E2NTBT	Fixed extension of SJNP beyond TUB (in the direction of device width)	3.0	µm
O1SANT	Fixed SALICIDE overlap of SJNP	3.0	µm
O2SANT	Fixed SALICIDE overlap of SJNP	4.5	µm
O1F1NT	Fixed M1_FPLATE overlap of SJNP	3.0	µm
O4F2NT	Fixed M2_FPLATE overlap of SJNP	4.5	µm

**Note:** Minimum drawn finger width is 10 µm

**Note:** NBUR connection to dhw# is not shown in the diagram.

## 3. Layer and Device rules → 3.19 1XN module→ 3.19.2 Device rules→ dfwnsj1\_10

**Figure 3.159** dfwnsj1\_10

3. Layer and Device rules → 3.19 1XN module→ 3.19.2 Device rules→ dfwnsj1\_16c

### **dfwnsj1\_16c**

The layout is predefined and scalable concerning width. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B4MV	dfwnsj1_# without MV is not allowed	-	-
B6NT	Fixed orientation is 0 degree or 180 degree	-	-
B7NT	Cathode dfwnsj1_# NBUR must connect to HWNTUB	-	-
E2HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	3.0	µm
E2HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	3.0	µm
E2NTBT	Fixed extension of SJNP beyond TUB (in the direction of device width)	3.0	µm
O1SANT	Fixed SALICIDE overlap of SJNP	3.0	µm
O3SANT	Fixed SALICIDE overlap of SJNP	6.0	µm
O1F1NT	Fixed M1_FPLATE overlap of SJNP	3.0	µm
O4F2NT	Fixed M2_FPLATE overlap of SJNP	4.5	µm
O1F3NT	Fixed M3_FPLATE overlap of SJNP	6.0	µm

**Note:** dfwnsj1\_16c device must be labeled "dfwnsj1\_16c" using DIODEF layer

**Note:** Minimum drawn finger width is 20 µm

**Note:** NBUR connection to dhw# is not shown in the diagram.

3. Layer and Device rules → 3.19 1XN module → 3.19.2 Device rules → dfwnsj1\_16c

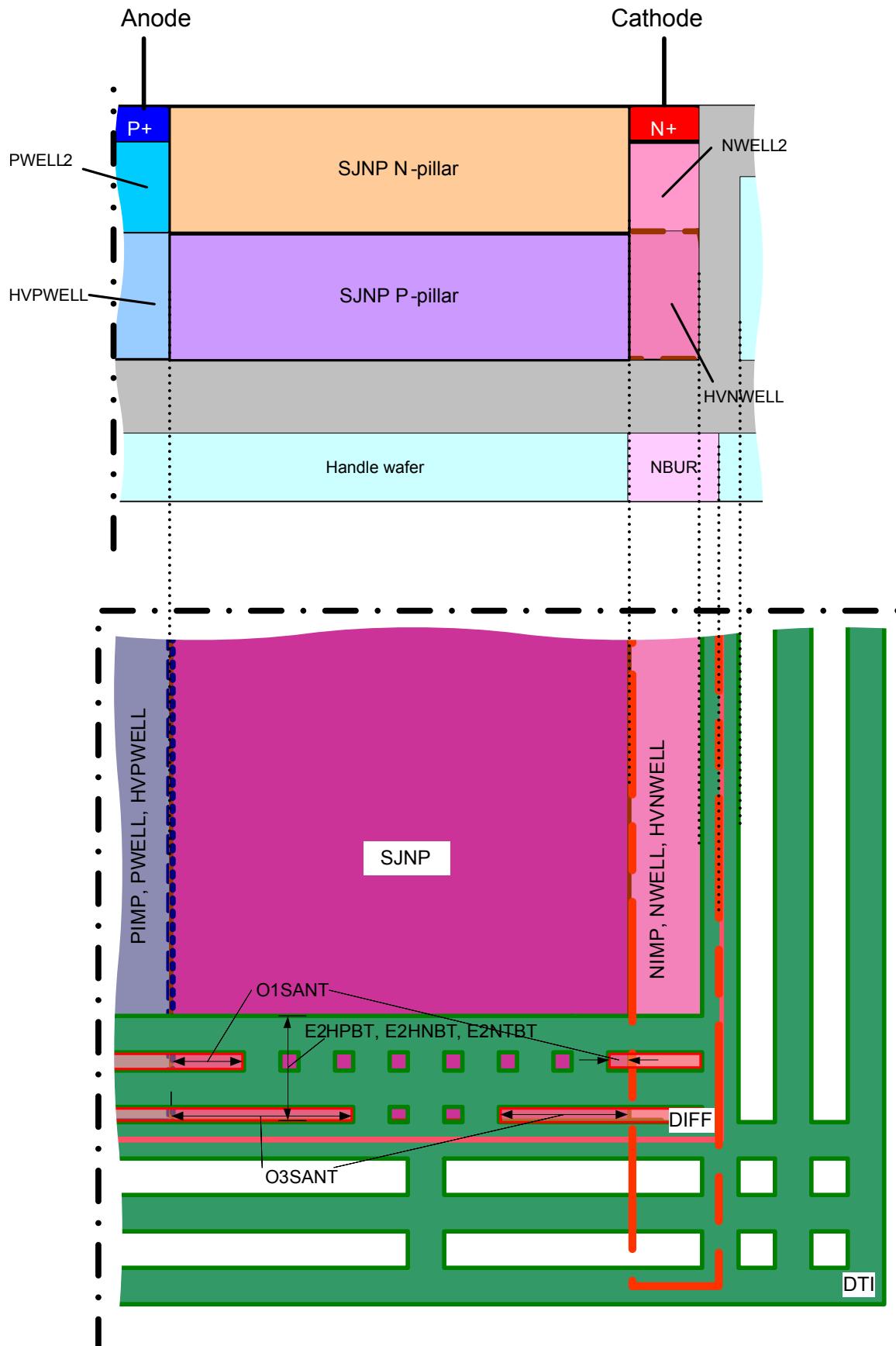


Figure 3.160 dfwnsj1\_16c

3. Layer and Device rules → 3.20 1XP module

## 3.20 1XP module

### 3.20.1 Layer rules

#### SJPN

Name	Description	Value	Unit
B1PT	SJPN without PWBLK, SUBBLK and MV is not allowed	-	-
B2PT	SJPN overlap of HWTUB, NWELL, HVNWELL, HVPWELL, NIMP, HRES or MRES is not allowed	-	-
B3PT	SJPN overlap of POLY1 or PIMP is not allowed (except phsj1_# CHANNEL region)	-	-
B4PT	SJPN overlap of NDF, PDF, PWELL4, NDFMV, PDFMV, DFN, DFP, NBASE, PBASE is not allowed	-	-
B6PT	SJPN without DIFF is not allowed (except phsj1_# CHANNEL region)	-	-
W1PT	Minimum SJPN width	2.0	μm
S1PT	Minimum SJPN spacing/notch	1.5	μm
A1PT	Minimum SJPN area	9.5	μm <sup>2</sup>

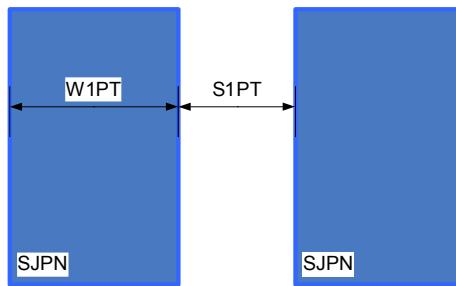


Figure 3.161 SJPN

#### SJPN\_E

Name	Description	Value	Unit
W2PT	Minimum SJPN_E width	0.5	μm

### 3.20.2 Device rules

#### phsj1\_7

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10PT	This device must be used together with a dhw2a, dhw2 or dhw3	-	-
B5PT	SOURCE NBUR must connect to HWNTUB	-	-
B8PT	Fixed orientation is 0 degree or 180 degree	-	-
B9MV	phsj1_# without MV is not allowed	-	-
W12GA	Minimum CHANNEL length	0.5	μm
W2GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Device finger width of phsj1_# is defined as GATE finger width + 1 μm		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

⇒

## 3. Layer and Device rules → 3.20 1XP module→ 3.20.2 Device rules→ phsj1\_7

Name	Description	Value	Unit
S5DF	Fixed DRAIN-EDGE-STI length	1.0	µm
S1HNPT	Fixed HVNWELL spacing to SJPN (in CHANNEL direction)	0.5	µm
S1P1NC	Fixed POLY1 spacing to DNC (in the direction of GATE length)	0.2	µm
S3GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
S3P1DF	Minimum POLY1 spacing to DRAIN DIFF	0.48	µm
S4INDP	Minimum NIMP spacing to PDIFF	0.14	µm
E1HBPT	Fixed SUBBLK enclosure of SJPN (in CHANNEL region)	0.5	µm
E1HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	1.5	µm
E1HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	1.5	µm
E1PTBT	Fixed extension of SJPN beyond TUB (in the direction of device width)	1.5	µm
E4INDF	Minimum NIMP extension beyond NDIFF	0.14	µm
E4IPDF	Minimum PIMP extension beyond SOURCE PDIFF	0.14	µm
E4P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.52	µm
O1PTGA	Fixed SJPN overlap of GATE	1.5	µm
O1SAPT	Fixed SALICIDE overlap of SJPN	3.0	µm
O1F1PT	Fixed M1_FPLATE overlap of SJPN	3.0	µm

**Note:** Maximum CHANNEL length is 5 µm

**Note:** NBUR connection to dhw# is not shown in the diagram.

## 3. Layer and Device rules → 3.20 1XP module → 3.20.2 Device rules → phsj1\_7

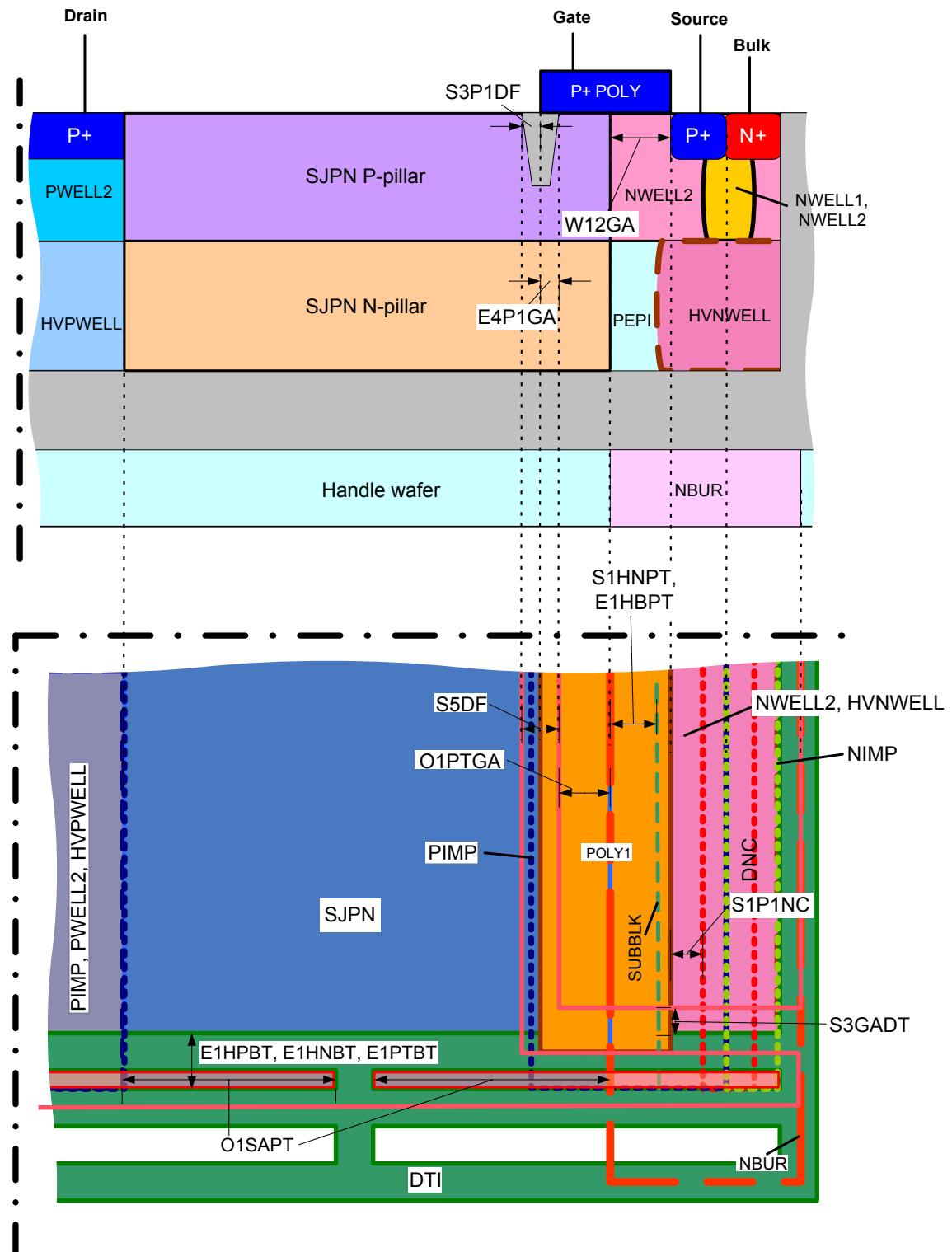


Figure 3.162 phsj1\_7

3. Layer and Device rules → 3.20 1XP module→ 3.20.2 Device rules→ phsj1\_10

## **phsj1\_10**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11PT	This device must be used together with a dhw2 or dhw3	-	-
B5PT	SOURCE NBUR must connect to HWNTUB	-	-
B8PT	Fixed orientation is 0 degree or 180 degree	-	-
B9MV	phsj1_# without MV is not allowed	-	-
W12GA	Minimum CHANNEL length	0.5	μm
W2GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Device finger width of phsj1_# is defined as GATE finger width + 1 μm		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
S5DF	Fixed DRAIN-EDGE-STI length	1.0	μm
S1HNPT	Fixed HVNWELL spacing to SJPN (in CHANNEL direction)	0.5	μm
S1P1NC	Fixed POLY1 spacing to DNC (in the direction of GATE length)	0.2	μm
S3GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S3P1DF	Minimum POLY1 spacing to DRAIN DIFF	0.48	μm
S4INDP	Minimum NIMP spacing to PDIFF	0.14	μm
E1HBPT	Fixed SUBBLK enclosure of SJPN (in CHANNEL region)	0.5	μm
E2HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	3.0	μm
E2HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	3.0	μm
E2PTBT	Fixed extension of SJPN beyond TUB (in the direction of device width)	3.0	μm
E4INDF	Minimum NIMP extension beyond NDIFF	0.14	μm
E4IPDF	Minimum PIMP extension beyond SOURCE PDIFF	0.14	μm
E4P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.52	μm
O1PTGA	Fixed SJPN overlap of GATE	1.5	μm
O1SAPT	Fixed SALICIDE overlap of SJPN	3.0	μm
O2SAPT	Fixed SALICIDE overlap of SJPN	4.5	μm
O1F1PT	Fixed M1_FPLATE overlap of SJPN	3.0	μm
O4F2PT	Fixed M2_FPLATE overlap of SJPN	4.5	μm

**Note:** Maximum CHANNEL length is 5 μm

**Note:** NBUR connection to dhw# is not shown in the diagram.

## 3. Layer and Device rules → 3.20 1XP module → 3.20.2 Device rules → phsj1\_10

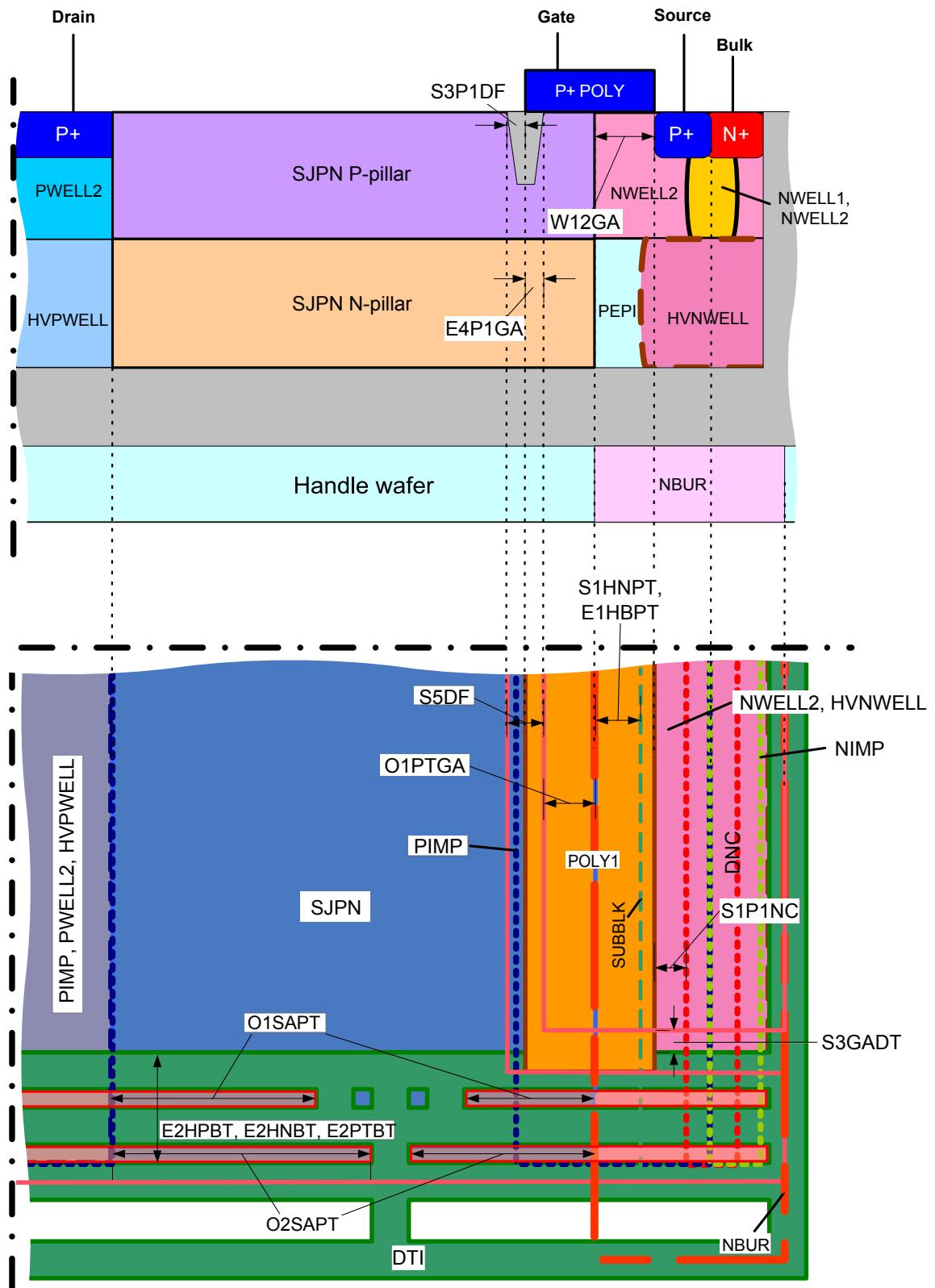


Figure 3.163 phsj1\_10

3. Layer and Device rules → 3.20 1XP module→ 3.20.2 Device rules→ phsj1\_16c

### **phsj1\_16c**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

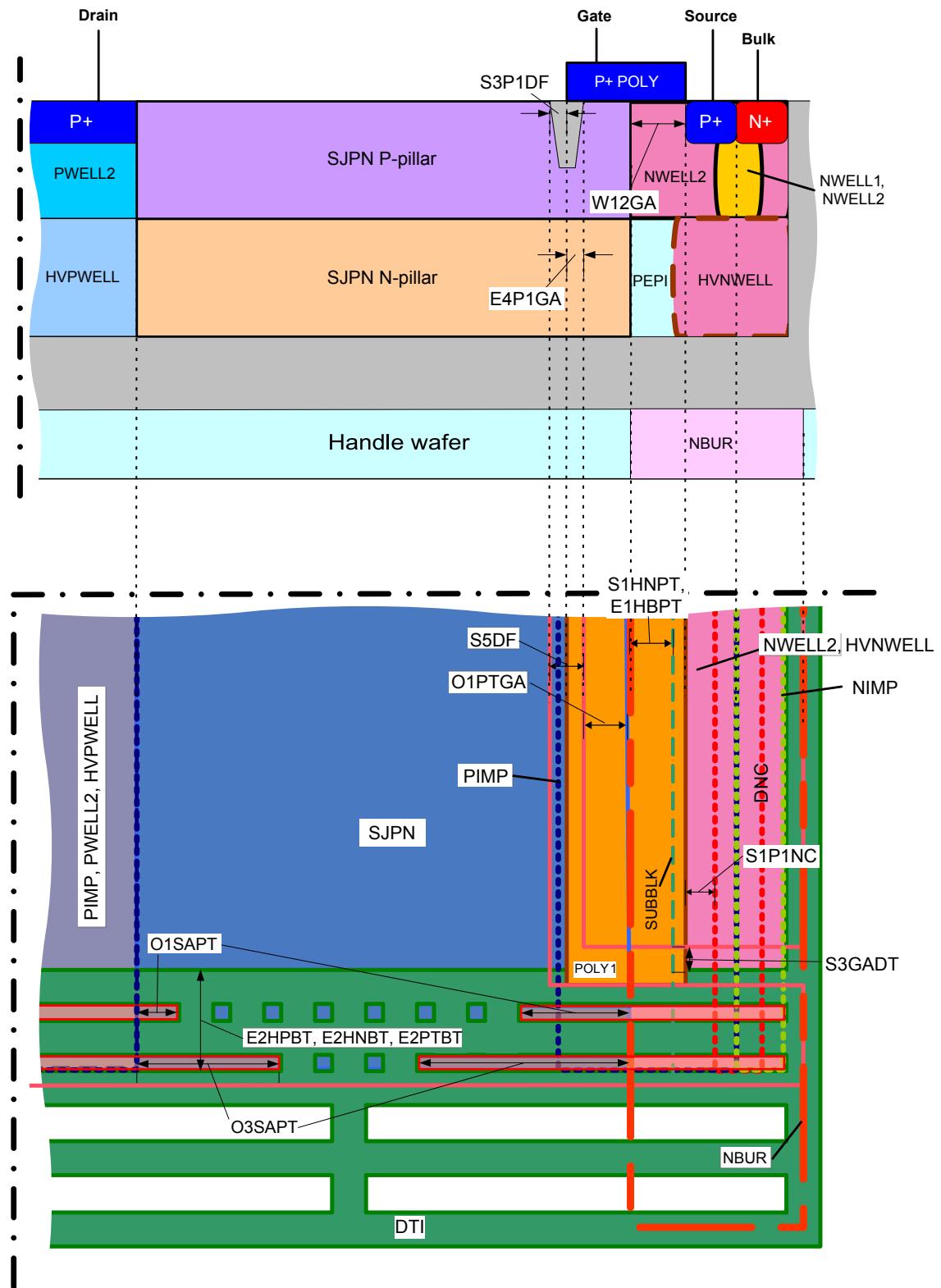
Name	Description	Value	Unit
B12PT	This device must be used together with dhw3	-	-
B5PT	SOURCE NBUR must connect to HWNTUB	-	-
B8PT	Fixed orientation is 0 degree or 180 degree	-	-
B9MV	phsj1_# without MV is not allowed	-	-
W12GA	Minimum CHANNEL length	0.5	μm
W26GA	Minimum GATE width	20.0	μm
	<b>Note:</b> Device finger width of nhsj1_# is defined as GATE finger width + 1 μm		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
S5DF	Fixed DRAIN-EDGE-STI length	1.0	μm
S1HNPT	Fixed HVNWELL spacing to SJPN (in CHANNEL direction)	0.5	μm
S1P1NC	Fixed POLY1 spacing to DNC (in the direction of GATE length)	0.2	μm
S3GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S3P1DF	Minimum POLY1 spacing to DRAIN DIFF	0.48	μm
S4INDP	Minimum NIMP spacing to PDIFF	0.14	μm
E1HBPT	Fixed SUBBLK enclosure of SJPN (in CHANNEL region)	0.5	μm
E2HNBT	Fixed extension of HVNWELL beyond TUB (in the direction of device width)	3.0	μm
E2HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	3.0	μm
E2PTBT	Fixed extension of SJPN beyond TUB (in the direction of device width)	3.0	μm
E4INDF	Minimum NIMP extension beyond NDIFF	0.14	μm
E4IPDF	Minimum PIMP extension beyond SOURCE PDIFF	0.14	μm
E4P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.52	μm
O1PTGA	Fixed SJPN overlap of GATE	1.5	μm
O1SAPT	Fixed SALICIDE overlap of SJPN	3.0	μm
O3SAPT	Fixed SALICIDE overlap of SJPN	6.0	μm
O1F1PT	Fixed M1_FPLATE overlap of SJPN	3.0	μm
O4F2PT	Fixed M2_FPLATE overlap of SJPN	4.5	μm
O1F3PT	Fixed M3_FPLATE overlap of SJPN	6.0	μm

**Note:** phsj1\_16c device must be labeled "phsj1\_16c" using POLY1 (VERIFICATION) layer over the GATE

**Note:** Maximum CHANNEL length is 5 μm

**Note:** NBUR connection to dhw# is not shown in the diagram.

## 3. Layer and Device rules → 3.20 1XP module → 3.20.2 Device rules → phsj1\_16c

**Figure 3.164 phsj1\_16c**

3. Layer and Device rules → 3.21 2XP module

## 3.21 2XP module

### 3.21.1 Layer rules

#### SJ2XP

Name	Description	Value	Unit
B12X4	MET1 is not allowed over SJ2XP (except predefined MET1 device terminal connections)	-	-
B1X4	SJ2XP without PWBLK, SUBBLK and MV is not allowed	-	-
B2X4	SJ2XP overlap of HWTUB, DNC, DPC, NWELL, HVNWELL, HVPWELL, NIMP, HRES, MRES, DEPL, PWELL4 is not allowed	-	-
B3X4	SJ2XP overlap of POLY1 or PIMP is not allowed (except phsj2b_# CHANNEL region)	-	-
B4X4	SJ2XP without DIFF is not allowed (except phsj2b_# CHANNEL region)	-	-
B5X4	SJ2XP overlap of SJNP, SJPN, NBUF, SJ1XN, SJ1XP is not allowed	-	-
B6X4	SJ2XP overlap of NDF, PDF, NDFMV, PDFMV, DFN, DFP, NBASE, PBASE is not allowed	-	-
W1X4	Minimum SJ2XP width	2.0	μm
S1X4	Minimum SJ2XP spacing / notch	1.5	μm
S1X4NF	Minimum SJ2XP spacing to NBUF	2.0	μm
S1X4NT	Minimum SJ2XP spacing to SJNP	2.0	μm
S1X4PT	Minimum SJ2XP spacing to SJPN	2.0	μm
A1X4	Minimum SJ2XP area	9.5	μm <sup>2</sup>

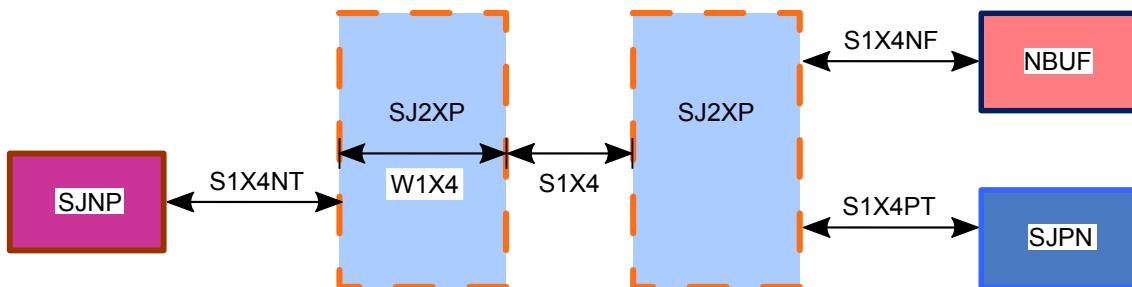


Figure 3.165 SJ2XP

3. Layer and Device rules → 3.21 2XP module → 3.21.1 Layer rules → SJNTOP

## SJNTOP

Name	Description	Value	Unit
B1NS	SJNTOP without SJ2XP is not allowed	-	-
W1NS	Minimum SJNTOP width	1.0	µm
S1NS	Minimum SJNTOP spacing / notch	1.0	µm
A1NS	Minimum SJNTOP area	2.25	µm <sup>2</sup>

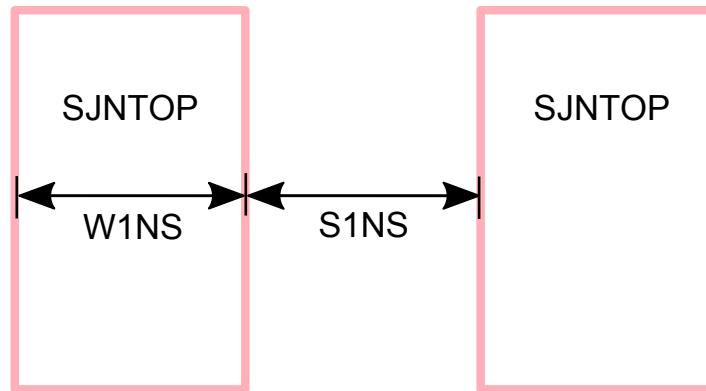


Figure 3.166 SJNTOP

## SJ2XP\_E

Name	Description	Value	Unit
W2X4	Minimum SJ2XP_E width	0.5	µm

## SJNTOP\_E

Name	Description	Value	Unit
W2NS	Minimum SJNTOP_E width	0.5	µm

## 3.21.2 Device rules

### phsj2b\_7

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
B8X4	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W61GA	Fixed CHANNEL length	0.5	µm
W63GA	Minimum GATE width	10.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj2b\_7 device must be labeled "phsj2b\_7" using POLY1 (VERIFICATION) layer over GATE

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_7

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_7

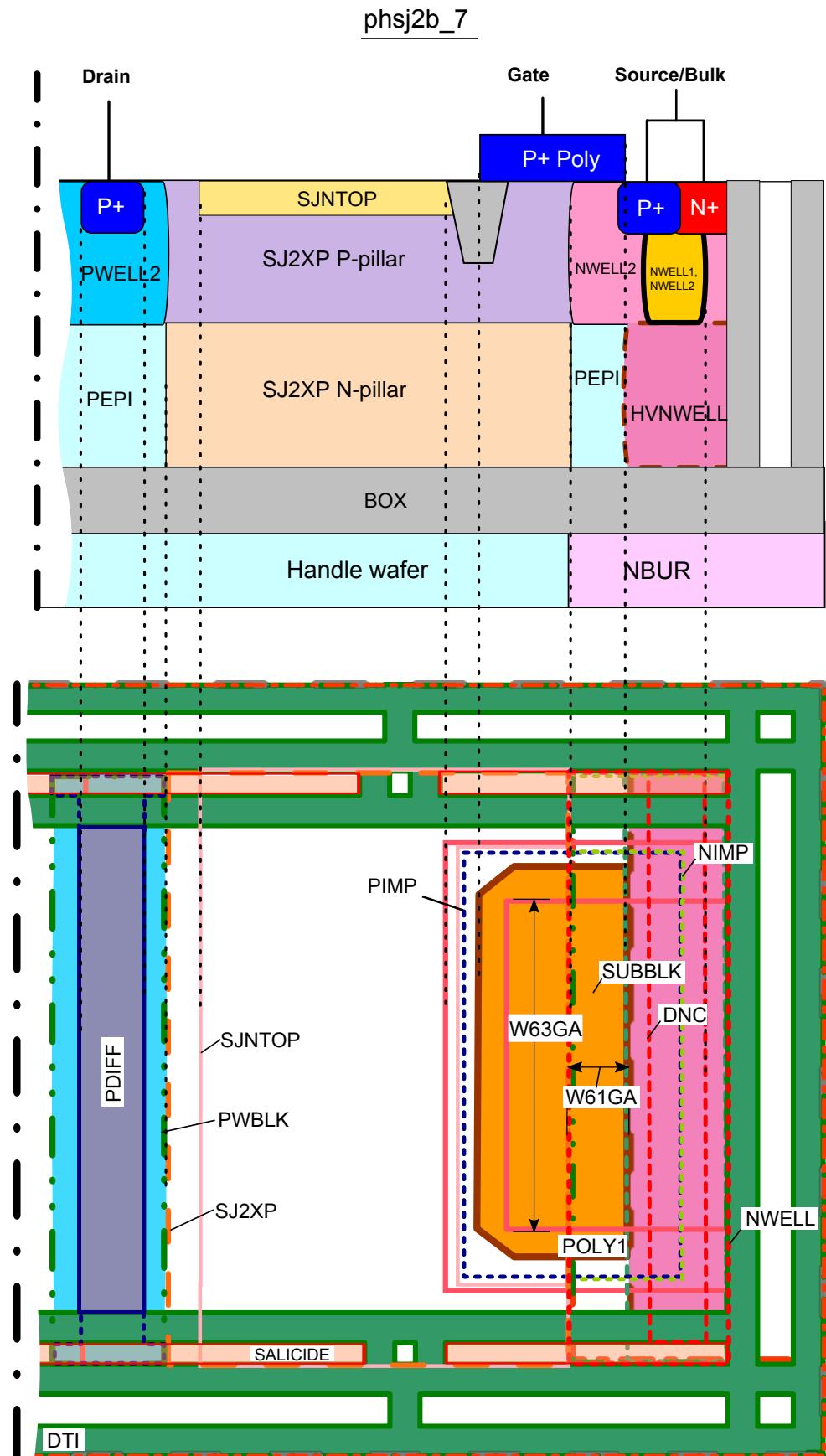


Figure 3.167 phsj2b\_7

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_8

### **phsj2b\_8**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B15X4	METTP, METTPL are not allowed over SJ2XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X4	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ2XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
B9X4	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W61GA	Fixed CHANNEL length	0.5	μm
W63GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	μm

**Note:** phsj2b\_8 device must be labeled "phsj2b\_8" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj2b\_8m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.21 2XP module → 3.21.2 Device rules → phsj2b\_8

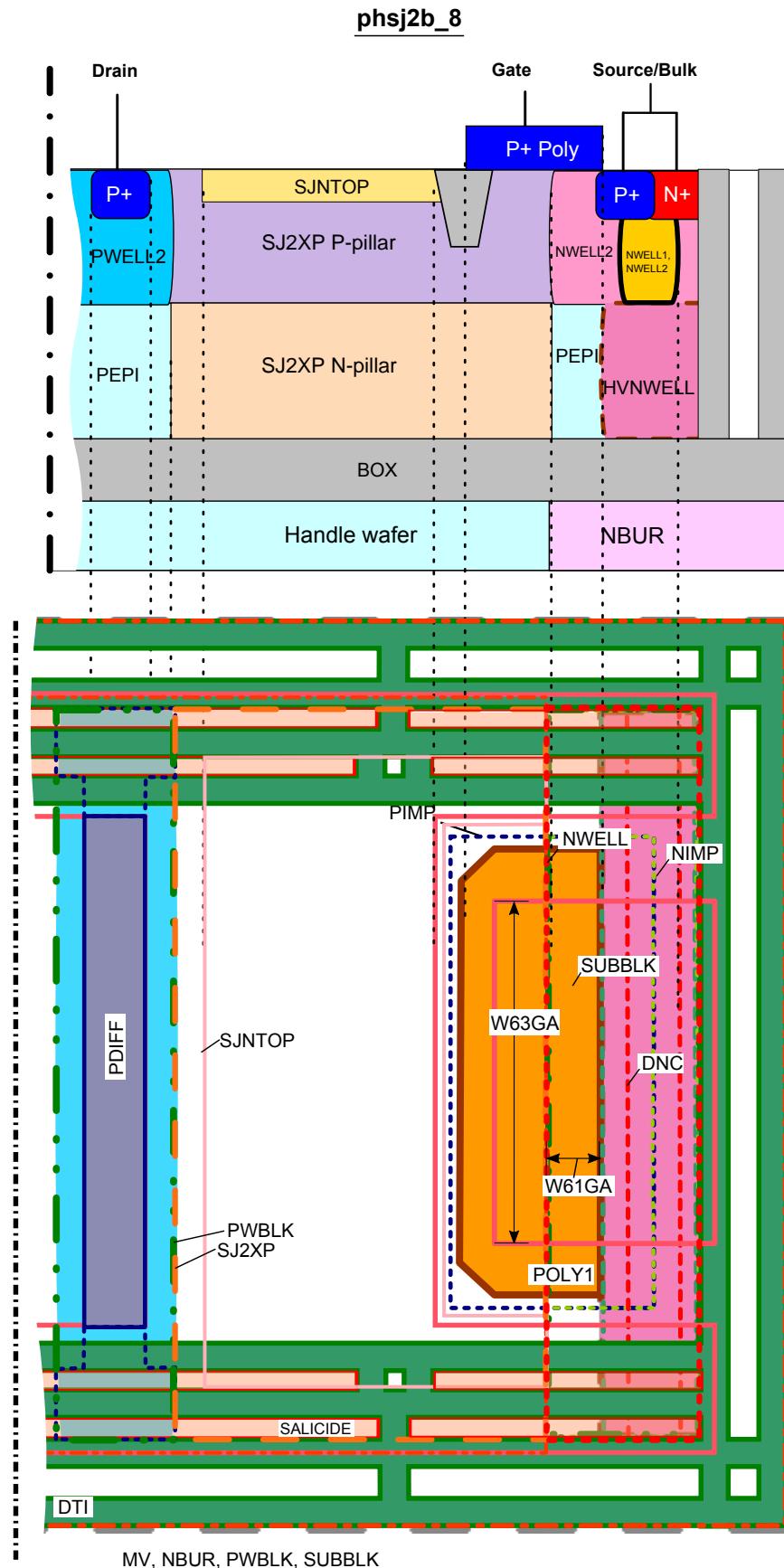


Figure 3.168 phsj2b\_8

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_10

## **phsj2b\_10**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B15X4	METTP, METTPL are not allowed over SJ2XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X4	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ2XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
B9X4	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W61GA	Fixed CHANNEL length	0.5	μm
W63GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	μm

**Note:** phsj2b\_10 device must be labeled "phsj2b\_10" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

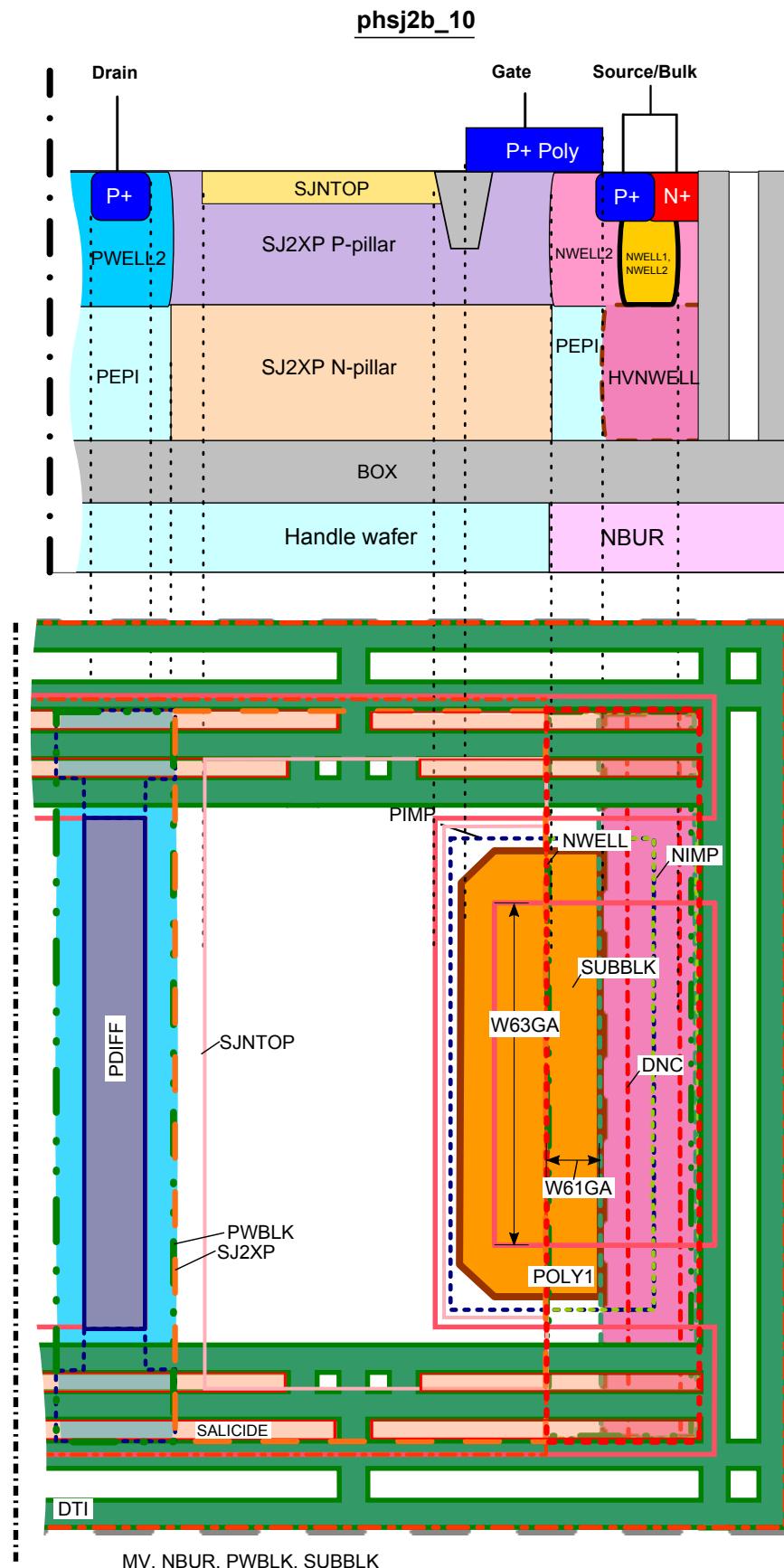
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj2b\_10m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_10



**Figure 3.169** phsj2b\_10

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_13

### **phsj2b\_13**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10X4	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B15X4	METTP, METTPL are not allowed over SJ2XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X4	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ2XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
W61GA	Fixed CHANNEL length	0.5	µm
W64GA	Minimum GATE width	25.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj2b\_13 device must be labeled "phsj2b\_13" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

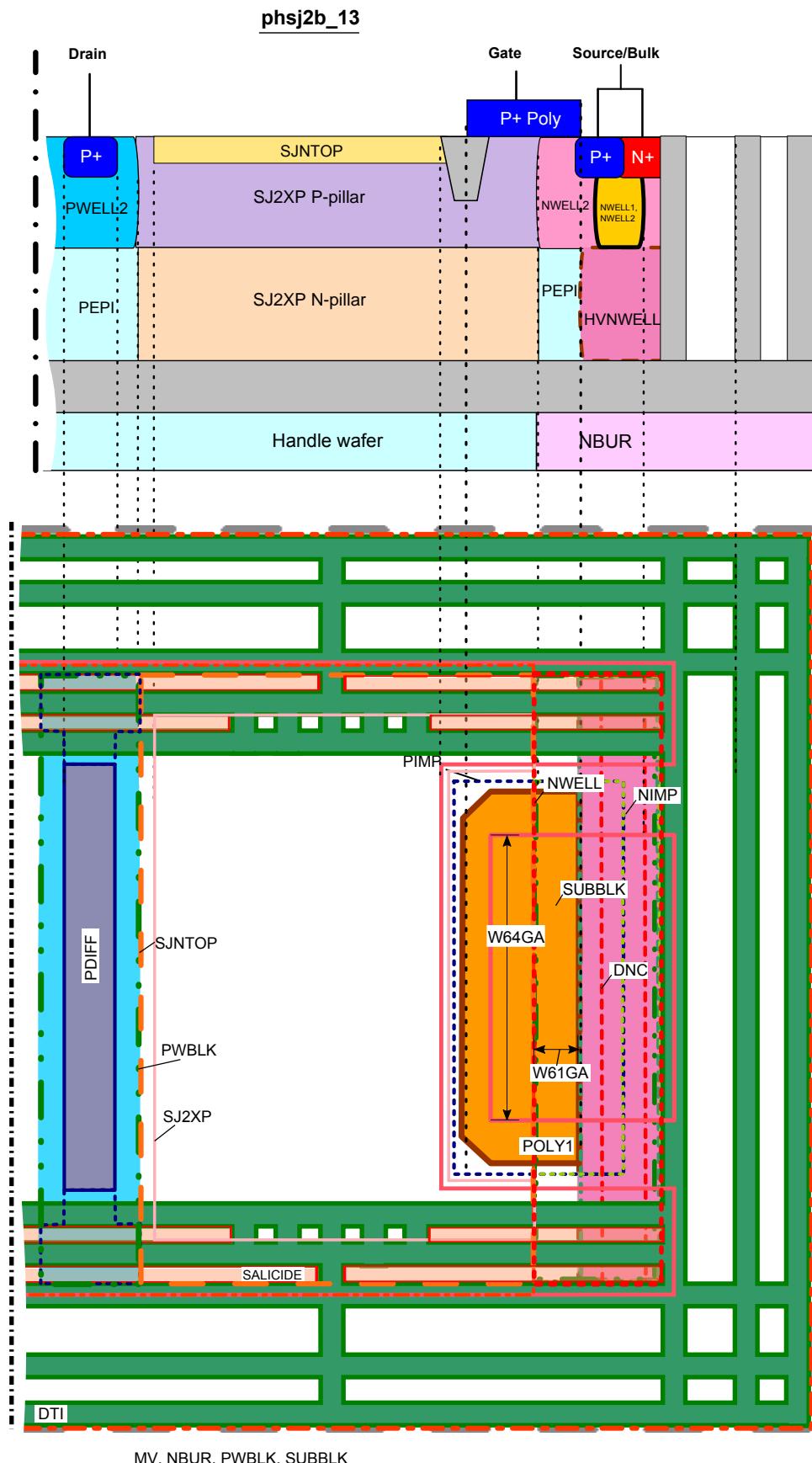
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj2b\_13m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_13



MV, NBUR, PWBLK, SUBBLK

**Figure 3.170 phsj2b\_13**

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_16

### **phsj2b\_16**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11X4	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B15X4	METTP, METTPL are not allowed over SJ2XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X4	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ2XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
W61GA	Fixed CHANNEL length	0.5	µm
W65GA	Minimum GATE width	30.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj2b\_16 device must be labeled "phsj2b\_16" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

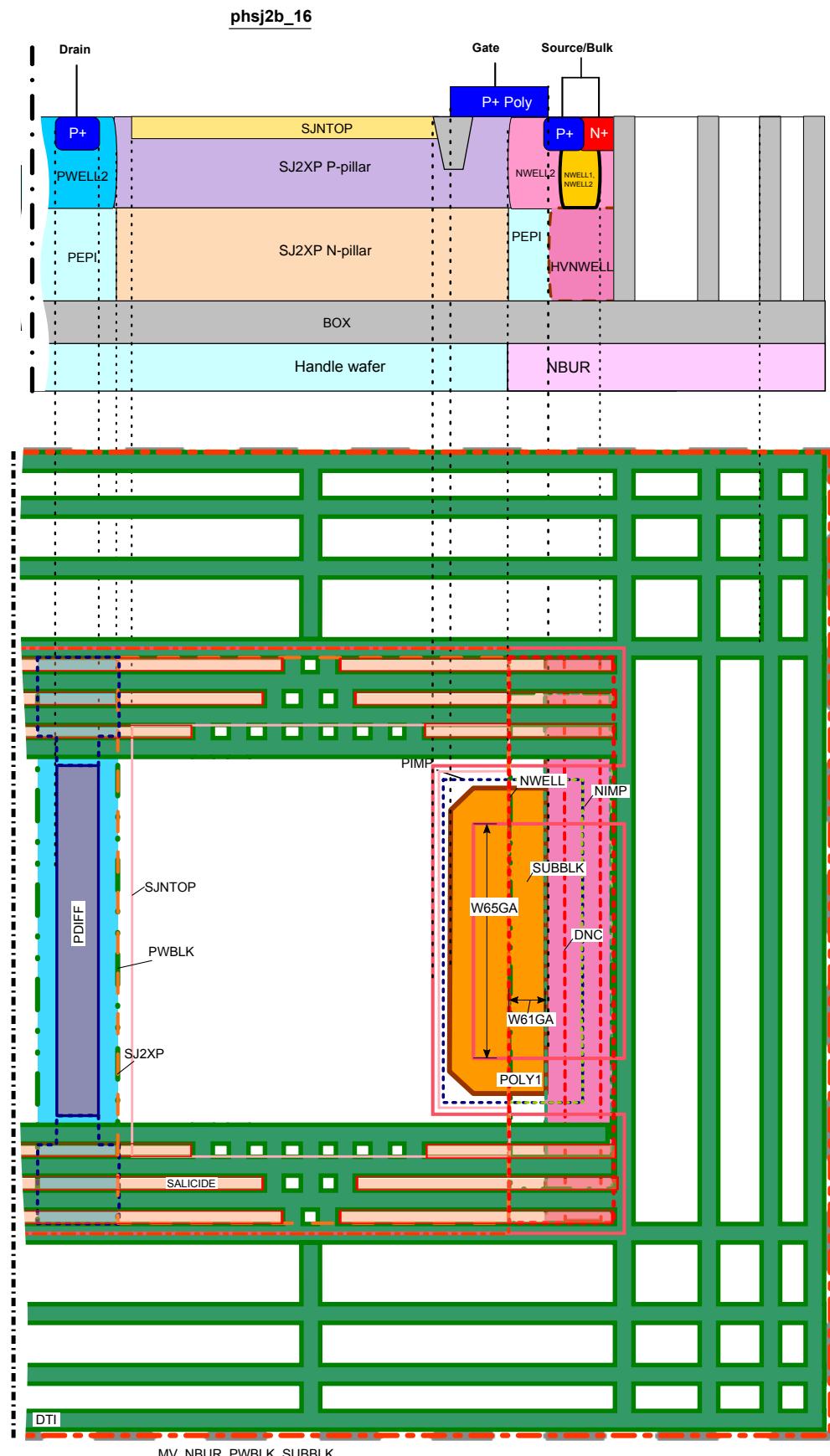
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj2b\_16m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.21 2XP module→ 3.21.2 Device rules→ phsj2b\_16



**Figure 3.171 phsj2b\_16**

3. Layer and Device rules → 3.22 DNC module

## 3.22 DNC module

### 3.22.1 Layer rules

#### DNC

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1NC	DNC is only allowed for dfwdpa, phsj1_#, dpp6, dpp7, phsj1a_#, phsj2b_#	-	-
B2NC	DNC without NWELL is not allowed	-	-
B3NC	NW_VERIFY overlap of DNC is not allowed	-	-
W1NC	Minimum DNC width	0.86	µm
S1NC	Minimum DNC spacing/notch	0.6	µm

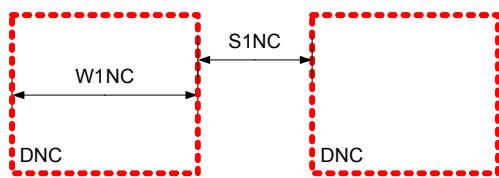


Figure 3.172 DNC

3. Layer and Device rules → 3.23 DPC module

## 3.23 DPC module

### 3.23.1 Layer rules

#### DPC

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1PC	DPC is only allowed for nhsj1_#, dnp7, nisj1_16, nhsj1a_#, nhsj1b_#	-	-
B3PC	DPC overlap of NWELL or PWBLK is not allowed	-	-
B2PC	DPC crossing MV edge is not allowed	-	-
W1PC	Minimum DPC width	0.6	μm
S1PC	Minimum DPC spacing/notch	0.6	μm
S1PCNW	Minimum DPC spacing to NWELL	1.0	μm

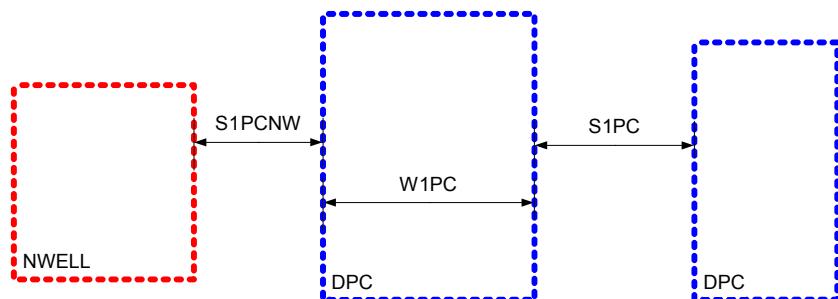


Figure 3.173 DPC

### 3.23.2 Device rules

#### dnp7

The layout of the dnp7 protection diode is predefined and only the cathode width can be changed in the range of 1μm to 100μm. Fixed cathode length is 1μm.

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.

**Note:** MV is necessary for dnp7.

**Note:** DTI ring is required for dnp7.

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

3. Layer and Device rules → 3.23 DPC module→ 3.23.2 Device rules→ dnp7

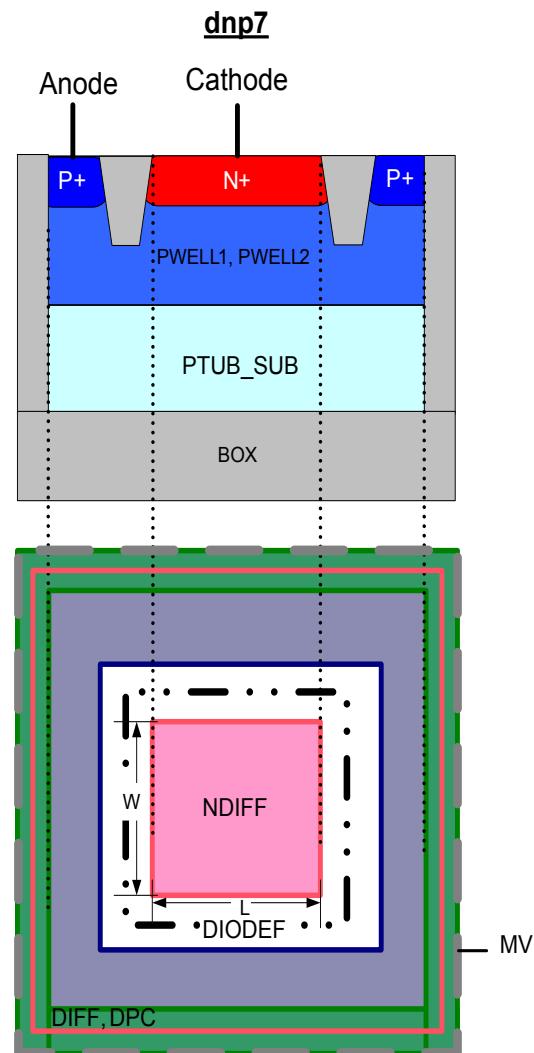


Figure 3.174 dnp7

3. Layer and Device rules → 3.24 HVN module

## 3.24 HVN module

### 3.24.1 Layer rules

#### HVNWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HN	HVNWELL must be surrounded by DTI (except nhsj1_#, phsj1_# and dfwnsj1_#, nhsj1a_#, phsj1a_#, dfwnsj1a_#, phsj2b_#)	-	-
B2HN	HVNWELL without NWELL is not allowed	-	-
B3HN	HVNWELL overlap of NDF, PDF, PWELL4, NDFMV, PDFMV, DFN, DFP is not allowed	-	-
W1HN	Minimum HVNWELL width	1.5	μm
W1TN	Minimum HWNTUB width	2.0	μm
S1HN	Minimum HVNWELL spacing/notch	2.0	μm
A1HN	Minimum HVNWELL area	9.5	μm <sup>2</sup>

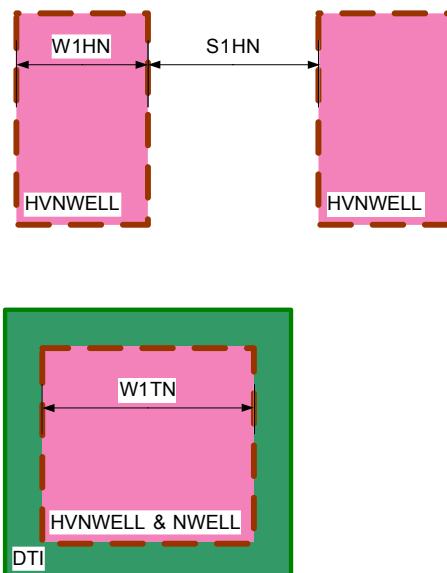


Figure 3.175 HVNWELL

#### HVNWELL\_E

Name	Description	Value	Unit
W2HN	Minimum HVNWELL_E width	0.5	μm

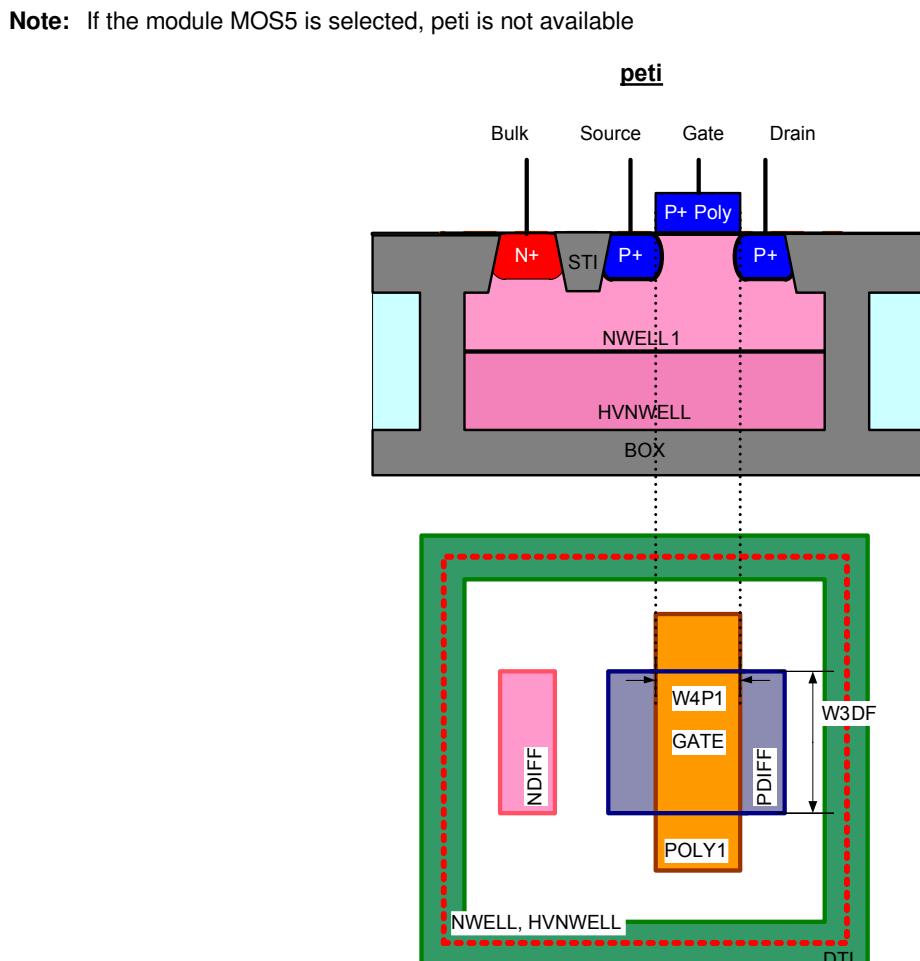
### 3.24.2 Device rules

peti

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.			⇒

## 3. Layer and Device rules → 3.24 HVN module→ 3.24.2 Device rules→ peti

Name	Description	Value	Unit
W4P1	Minimum GATE length <b>Note:</b> The design rule check error message W4P1 is also used generally for GATE areas (of any devices or shapes) being smaller than 0.18µm at any dimension.	0.18	µm
<b>Note:</b> If the module MOS5 is selected, peti is not available			

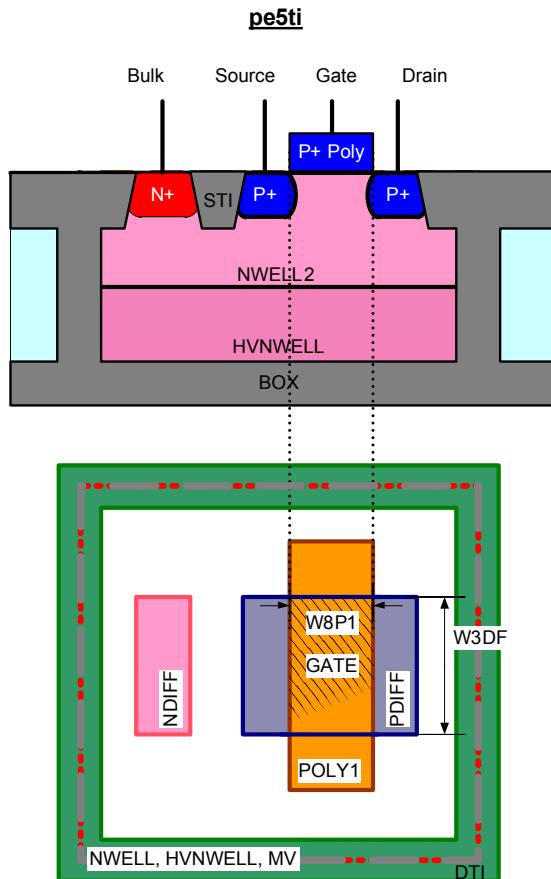
**Figure 3.176 peti**

3. Layer and Device rules → 3.24 HVN module → 3.24.2 Device rules → pe5ti

### pe5ti

Name	Description	Value	Unit
W3DF	Minimum GATE width	0.22	μm
	<b>Note:</b> The design rule check error message W3DF is also used generally for GATE areas (of any devices or shapes) being smaller GATE width than 0.22μm.		
W8P1	Minimum GATE length	0.5	μm

**Note:** MV is necessary for pe5ti



**Figure 3.177** pe5ti

3. Layer and Device rules → 3.24 HVN module → 3.24.2 Device rules → dfwdpa

### **dfwdpa**

The layout of dfwdpa is predefined and scalable concerning width only. All other dimensions must not be changed.

Name	Description	Value	Unit
E5INDF	Minimum NIMP enclosure of ACTIVE	0.14	μm
E5IPDF	Minimum PIMP enclosure of ACTIVE	0.14	μm

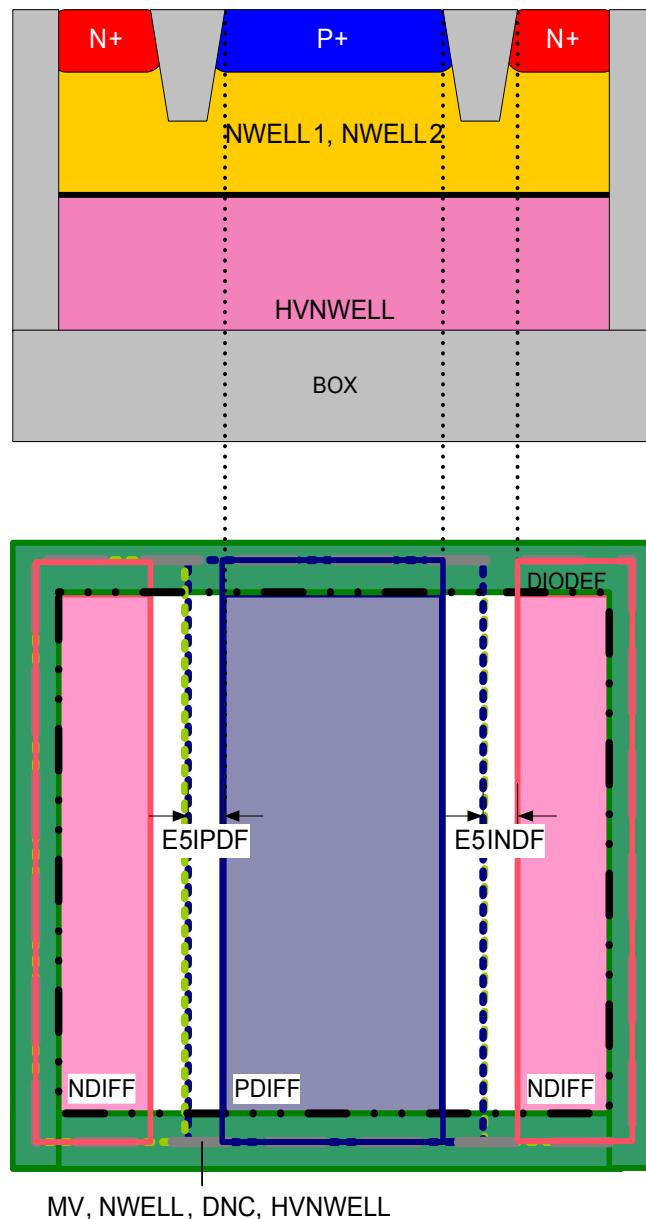
**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.

**Note:** Minimum drawn finger width is 2 μm.

**Note:** DTI ring is required for dfwdpa.

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

### dfwdpa



**Figure 3.178 dfwdpa**

3. Layer and Device rules → 3.24 HVN module→ 3.24.2 Device rules→ ds5a

### ds5a

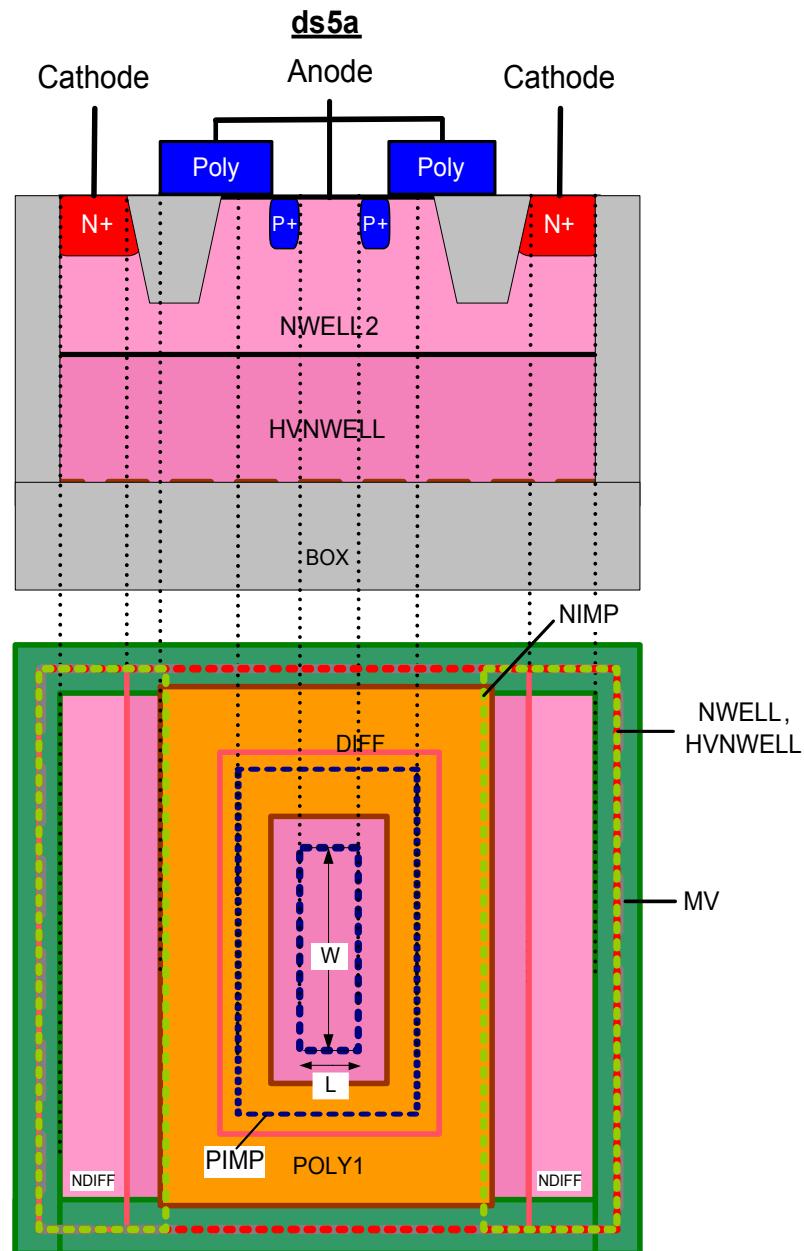
The layout of the ds5a Schottky diode is predefined and only the width can be changed in the range of 2.4  $\mu\text{m}$  up to 50  $\mu\text{m}$ . Fixed length is 0.94  $\mu\text{m}$ .

Name	Description	Value	Unit
B2DF	ds5 is not allowed	-	-

**Note:** DTI ring is required for ds5a.

**Note:** MV is necessary for ds5a.

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.



**Figure 3.179** ds5a

3. Layer and Device rules → 3.24 HVN module→ 3.24.2 Device rules→ dpp6

### dpp6

The layout of the dpp6 protection diode is predefined and only the anode and cathode width can be changed in the range of 5 $\mu\text{m}$  to 200 $\mu\text{m}$ . Fixed anode length is 0.82 $\mu\text{m}$ .

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.

**Note:** MV is necessary for dpp6.

**Note:** DTI ring is required for dpp6.

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

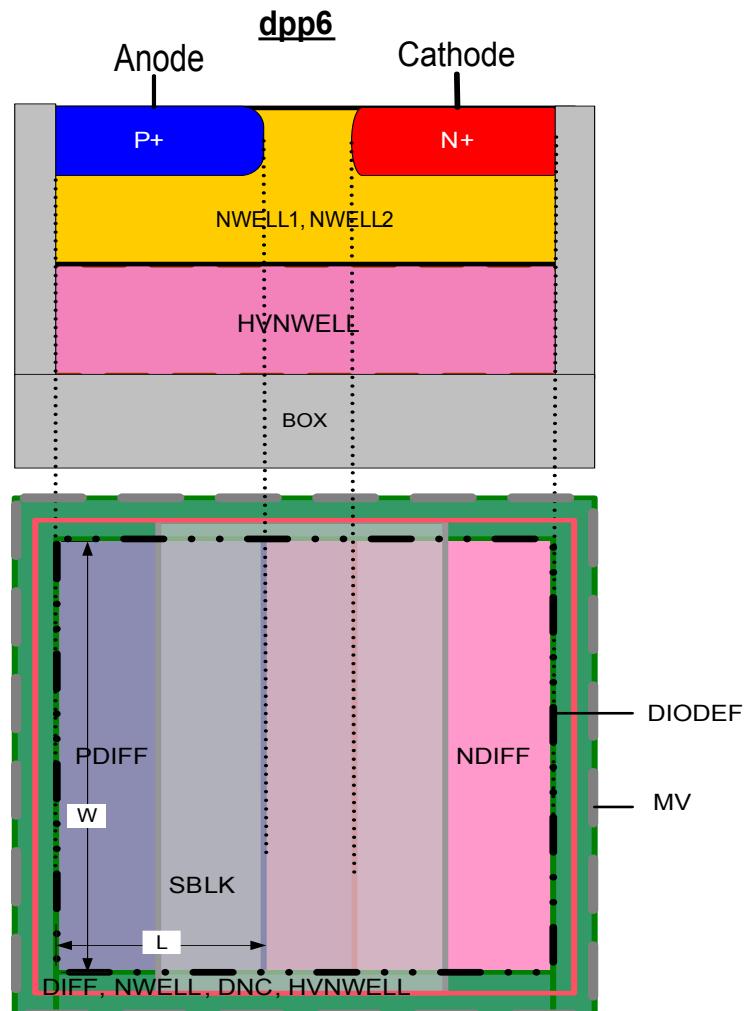


Figure 3.180 dpp6

3. Layer and Device rules → 3.24 HVN module → 3.24.2 Device rules → dpp7

### dpp7

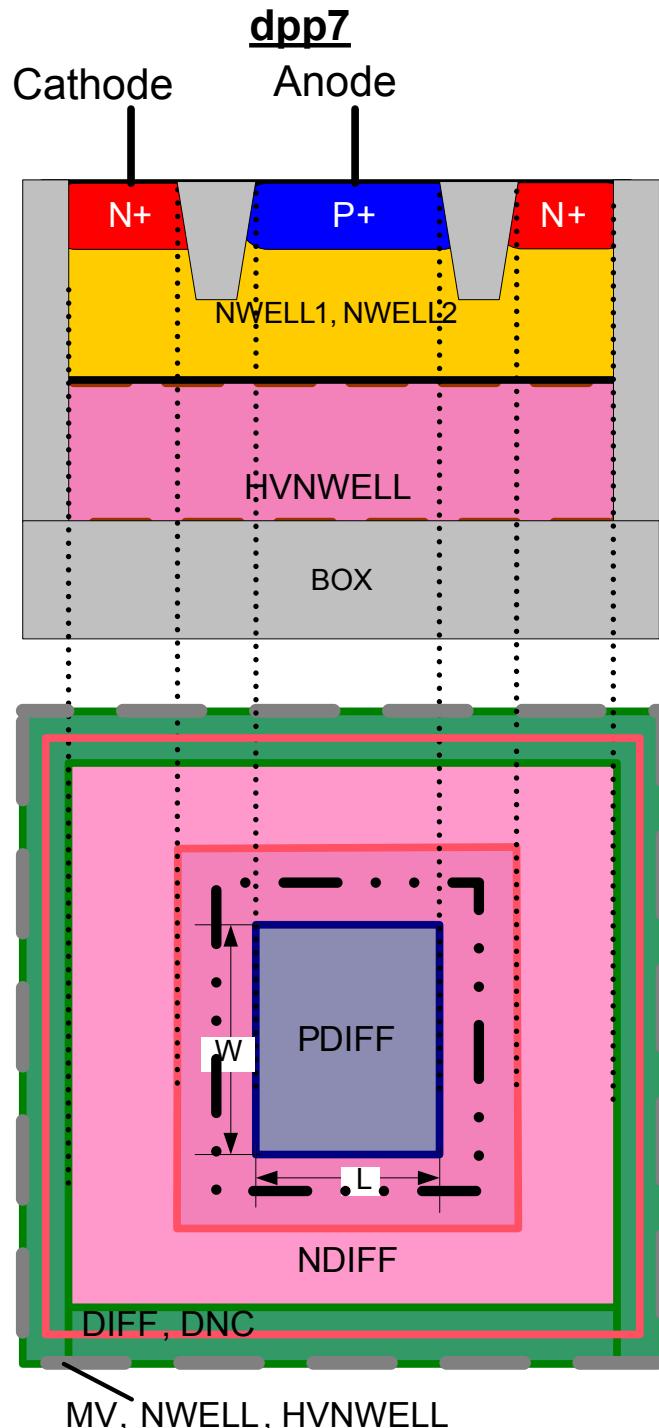
The layout of the dpp7 protection diode is predefined and only the anode width can be changed in the range of  $1\mu\text{m}$  to  $100\mu\text{m}$ . Fixed anode length is  $1\mu\text{m}$ .

**Note:** The layer DIODEF must enclose the pn junction and must not cross the pn junction.

**Note:** MV is necessary for dpp7.

**Note:** DTI ring is required for dpp7.

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.



**Figure 3.181** dpp7

3. Layer and Device rules → 3.25 HVP module

## 3.25 HVP module

### 3.25.1 Layer rules

#### HVPWELL

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1HP	HVPWELL overlap of NWELL, PWBLK is not allowed	-	-
B2HP	HVPWELL overlap of HVNWELL, SUBBLK, HRES or MRES is not allowed	-	-
B3HP	HVPWELL overlap of ne, ne5, dn, dn5, rdn, rdn5, rmp1#, rpp1#, rpp1s# or rpp1k1# is not allowed	-	-
B4HP	HVPWELL overlap of NDF, PDF, NDFMV, PDFMV, DFN, DFP, PWELL4 is not allowed	-	-
BDHP	HVPWELL(DUMMY) is not allowed to be used by customers (except predefined area)	-	-
W1HP	Minimum HVPWELL width	1.5	μm
S1HP	Minimum HVPWELL spacing/notch	2.0	μm
S1PHN	Minimum HVPWELL spacing to HVNWELL	1.5	μm
S1HPNW	Minimum HVPWELL spacing to NWELL	1.0	μm
A1HP	Minimum HVPWELL area	9.5	μm <sup>2</sup>

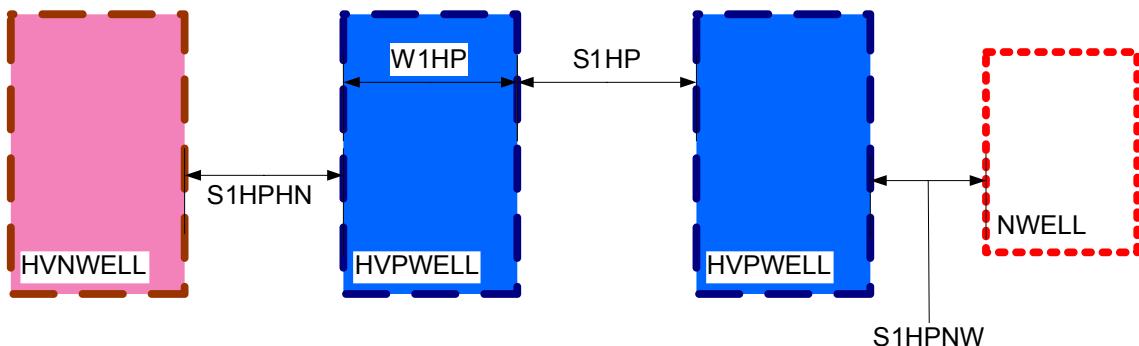


Figure 3.182 HVPWELL

#### HVPWELL\_E

Name	Description	Value	Unit
W2HP	Minimum HVPWELL_E width	0.5	μm

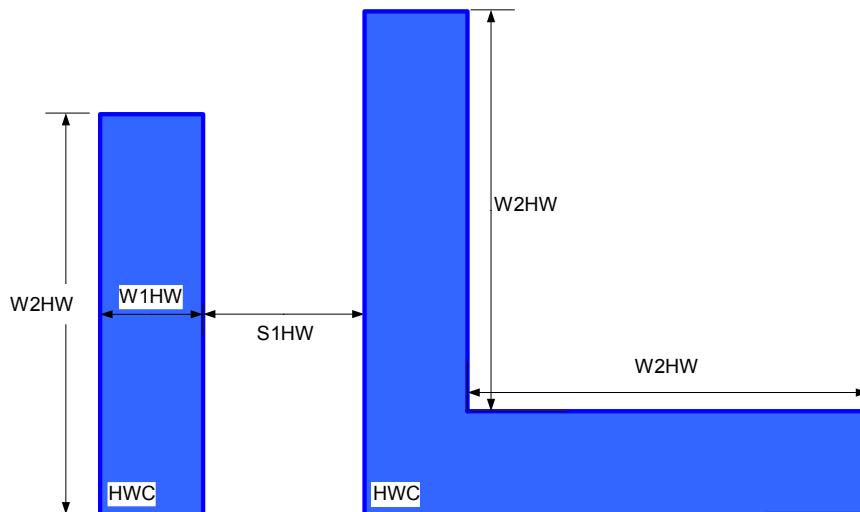
3. Layer and Device rules → 3.26 HWC module

## 3.26 HWC module

### 3.26.1 Layer rules

#### HWC

Name	Description	Value	Unit
B1HW	HWTUB overlap of SUBBLK is not allowed	-	-
B2HW	NWELL overlap of HWPTUB is not allowed	-	-
B3HW	HWNTUB and HWPTUB in one HWTUB is not allowed	-	-
B4HW	HWNTUB without NIMP is not allowed	-	-
B5HW	HWPTUB without PIMP is not allowed	-	-
B6HW	HWC overlap of CONT, PWBLK, POLY1, DTI, NBUF, DEPL, HVDEPL, LVT or SVT is not allowed	-	-
B7HW	HWC without DIFF is not allowed	-	-
B8HW	HWC without TUB is not allowed	-	-
B9HW	HWC overlap of handle wafer contact marked by HWC (VERIFICATION) is not allowed	-	-
W1HW	Fixed HWC width	1.5	μm
W2HW	Minimum HWC edge length	5.0	μm
S1HW	Minimum HWC spacing/notch	6.5	μm



**Figure 3.183 HWC**

3. Layer and Device rules → 3.27 NBUF module

## 3.27 NBUF module

### 3.27.1 Layer rules

#### NBUF

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1NF	NBUF without PWBLK, DIFF, SUBBLK, MV is not allowed	-	-
B2NF	NBUF overlap of HWTUB, POLY1, NIMP, SJNP, SJPN, DEPL, PWELL4 is not allowed	-	-
B3NF	NBUF is only allowed for nisj1_16	-	-
B6NF	NBUF overlap of NDF, PDF, NDFMV, PDFMV, DFN, DFP, NBASE, PBASE is not allowed	-	-
W1NF	Minimum NBUF width	2.0	μm
S1NF	Minimum NBUF spacing/notch	1.5	μm
A1NF	Minimum NBUF area	9.5	μm <sup>2</sup>

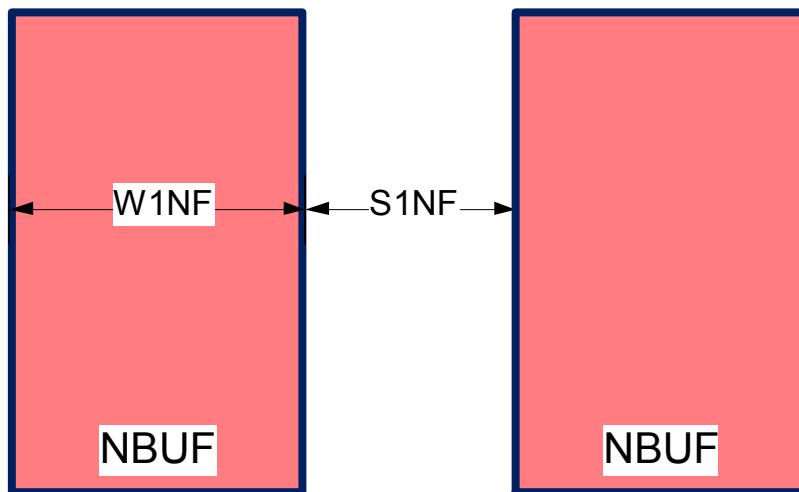


Figure 3.184 NBUF

#### NBUF\_E

Name	Description	Value	Unit
W2NF	Minimum NBUF_E width	0.5	μm

### 3.27.2 Device rules

#### nisj1\_16

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13NT	This device must be used together with dhw3	-	-

⇒

## 3. Layer and Device rules → 3.27 NBUF module→ 3.27.2 Device rules→ nisj1\_16

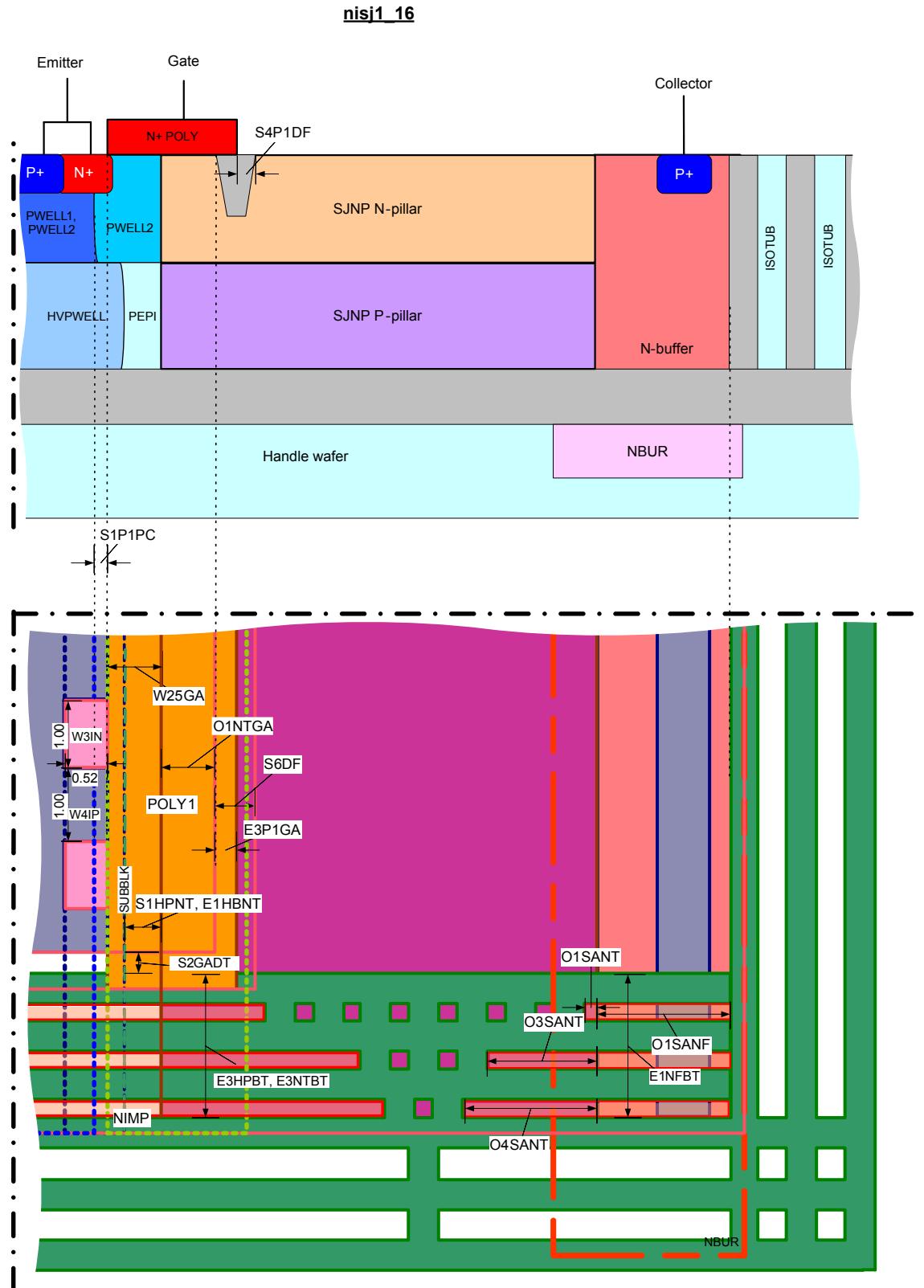
Name	Description	Value	Unit
B4NF	Fixed orientation is 0 degree or 180 degree	-	-
B5NF	NBUF without MET1, MET2, M3_FPLATE is not allowed	-	-
B7MV	nisj1_16 without MV is not allowed	-	-
B9NT	Collector NBUR must connect to HWNTUB	-	-
W25GA	Fixed CHANNEL length	1.0	μm
W27GA	Minimum GATE width	20.0	μm
W3IN	Fixed Emitter NDIFF segment size	1.0 x 0.52	μm x μm
W4IP	Fixed Emitter PDIFF segment size	1.0 x 0.52	μm x μm
S6DF	Fixed Collector-EDGE-STI length	1.0	μm
S1HPNT	Fixed HVPWELL spacing to SJNP (in CHANNEL region)	0.5	μm
S1P1PC	Fixed POLY1 spacing to DPC (in the direction of GATE length)	0.2	μm
S2GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S4P1DF	Minimum POLY1 spacing to Collector DIFF	0.48	μm
E1HBNT	Fixed SUBBLK enclosure of SJNP (in CHANNEL region)	0.5	μm
E1NFBT	Fixed extension of NBUF beyond TUB (in the direction of device width)	4.5	μm
E3HPBT	Fixed extension of HVPWELL beyond TUB (in the direction of device width)	4.5	μm
E3NTBT	Fixed extension of SJNP beyond TUB (in the direction of device width)	4.5	μm
E3P1GA	Minimum POLY1 extension beyond GATE (in the direction of GATE length)	0.52	μm
O1NTGA	Fixed SJNP overlap of GATE	1.5	μm
O1SANF	Fixed SALICIDE overlap of NBUF	7.0	μm
O1SANT	Fixed SALICIDE overlap of SJNP	3.0	μm
O3SANT	Fixed SALICIDE overlap of SJNP	6.0	μm
O4SANT	Fixed SALICIDE overlap of SJNP	6.75	μm
O1F1NT	Fixed M1_FPLATE overlap of SJNP	3.0	μm
O8F2NT	Fixed M2_FPLATE overlap of SJNP	6.0	μm
O4F3NT	Fixed M3_FPLATE overlap of SJNP	6.75	μm

**Note:** Width scaling is in the fixed increment of 2μm.

**Note:** NDIFF and PDIFF segments are arranged alternatively.

**Note:** NBUR connection to dhw# is not shown in the diagram.

## 3. Layer and Device rules → 3.27 NBUF module→ 3.27.2 Device rules→ nisj1\_16

**Figure 3.185 nisj1\_16**

3. Layer and Device rules → 3.28 NBUR module

## 3.28 NBUR module

### 3.28.1 Layer rules

#### NBUR

Name	Description	Value	Unit
B1NB	HWNTUB without NBUR is not allowed	-	-
B3NB	NBUR must connect to HWNTUB	-	-
B5NB	NBUR overlap of NBASE, PBASE is not allowed	-	-
B6NB	nhv#, ndhv#, dfwdn#, phv#, nhvr#, phvr#, ndhvr#, dfwdnh#, nmv#, pmv#, ndmv#, dfwd# in dhw# is not allowed	-	-
B7NB	qnv5, qnwha, qpv5, qpwha in dhw# is not allowed	-	-
B8NB	nhv#, ndhv#, dfwdn#, phv#, nhvr#, phvr#, ndhvr#, dfwdnh#, nmv#, pmv#, ndmv#, dfwd# in dhw#c or dhw#d are not allowed	-	-
B9NB	qnv5, qnwha, qpv5, qpwha in dhw#c or dhw#d are not allowed	-	-
W1NB	Minimum NBUR width	1.0	μm
S1NB	Minimum NBUR spacing/notch	2.0	μm
A1NB	Minimum NBUR area	4.0	μm <sup>2</sup>

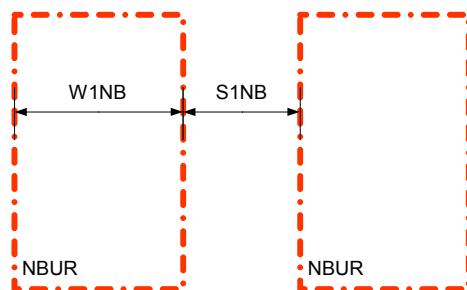


Figure 3.186 NBUR

### 3.28.2 Device rules

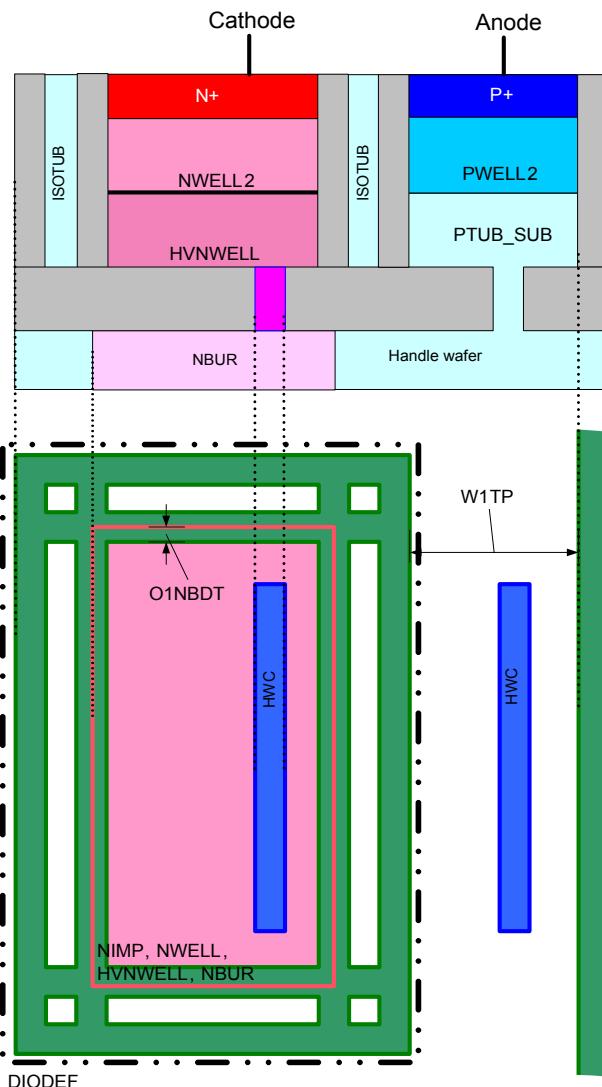
#### dhw2a

Name	Description	Value	Unit
B2DT	FOXDTI without PWBLK and SUBBLK is not allowed	-	-
B2NB	dhw# terminal (Cathode/Anode) short is not allowed	-	-
B3DT	NWELL, DNC, DPC, NIMP, PIMP, HRES, MRES, HVNWELL, HVPWELL, SJNP, SJPN, NBUR over FOXDTI surrounding dhw# is not allowed	-	-
	<b>Note:</b> except NBUR stripes in dhw#		
B4HN	dhw# must be surrounded by HWPTUB	-	-
B5HN	dhw2a must be surrounded by 2FOXDTI	-	-
W1TP	Minimum HWPTUB width	7.0	μm
S2NB	Minimum NBUR spacing (different net)	23.0	μm
S1NBHB	Minimum NBUR spacing to SUBBLK	19.5	μm
S1NBHW	Minimum NBUR spacing to HWC	19.5	μm
O1NBBDT	Fixed NBUR overlap of DIFFDTI (except nhsj1_# DRAIN, phsj1_# Body, dfwnsj1_# Cathode)	0.5	μm

**Note:** Handle-wafer connection is not completely shown in the diagram

**Note:** dhw2a device must be labeled "dhw2a" using DIODEF (VERIFICATION) layer.

3. Layer and Device rules → 3.28 NBUR module → 3.28.2 Device rules → dhw2a



**Figure 3.187 dhw2a**

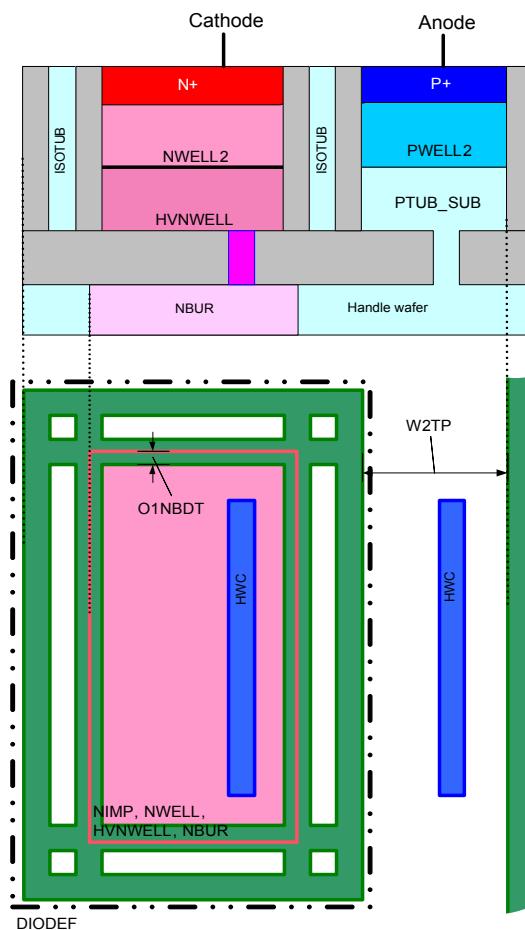
3. Layer and Device rules → 3.28 NBUR module→ 3.28.2 Device rules→ dhw2

## dhw2

Name	Description	Value	Unit
B12HN	dhw2 must be surrounded by 2FOXTDI	-	-
B2DT	FOXTDI without PWBLK and SUBBLK is not allowed	-	-
B2NB	dhw# terminal (Cathode/Anode) short is not allowed	-	-
B3DT	NWELL, DNC, DPC, NIMP, PIMP, HRES, MRES, HVNWELL, HVPWELL, SJNP, SJPN, NBUR over FOXDTI surrounding dhw# is not allowed  <b>Note:</b> except NBUR stripes in dhw#	-	-
B4HN	dhw# must be surrounded by HWPTUB	-	-
W2TP	Minimum HWPTUB width	9.0	μm
S3NB	Minimum NBUR spacing (different net)	27.0	μm
S2NBHB	Minimum NBUR spacing to SUBBLK	23.5	μm
S2NBHW	Minimum NBUR spacing to HWC	23.5	μm
S6NB	Minimum NBUR spacing to NBUR (dhw2a)	27.0	μm
O1NBDT	Fixed NBUR overlap of DIFFDTI (except nhsj1_# DRAIN, phsj1_# Body, dfwnsj1_# Cathode)	0.5	μm

**Note:** Handle-wafer connection is not completely shown in the diagram

**Note:** dhw2 device must be labeled "dhw2" using DIODEF (VERIFICATION) layer.



**Figure 3.188 dhw2**

3. Layer and Device rules → 3.28 NBUR module→ 3.28.2 Device rules→ dhw3

### dhw3

Name	Description	Value	Unit
B2DT	FOXDTI without PWBLK and SUBBLK is not allowed	-	-
B2NB	dhw# terminal (Cathode/Anode) short is not allowed	-	-
B3DT	NWELL, DNC, DPC, NIMP, PIMP, HRES, MRES, HVNWELL, HVPWELL, SJNP, SJPN, NBUR over FOXDTI surrounding dhw# is not allowed	-	-
	<b>Note:</b> except NBUR stripes in dhw#		
B4HN	dhw# must be surrounded by HWPTUB	-	-
B9HN	dhw3 must be surrounded by 3FOXDTI	-	-
W2TP	Minimum HWPTUB width	9.0	μm
W3TN	Minimum HWNTUB width	5.0	μm
S4NB	Minimum NBUR spacing (different net)	33.0	μm
S3DTHW	Minimum DTI spacing to HWC	5.0	μm
S3NBHB	Minimum NBUR spacing to SUBBLK	29.5	μm
S3NBHW	Minimum NBUR spacing to HWC	29.5	μm
S7NB	Minimum NBUR spacing to NBUR (dhw2a or dhw2)	33.0	μm
O1NBDT	Fixed NBUR overlap of DIFFDTI (except nhsj1_# DRAIN, phsj1_# Body, dfwnsj1_# Cathode)	0.5	μm

**Note:** Handle-wafer connection is not completely shown in the diagram

**Note:** dhw3 device must be labeled "dhw3" using DIODEF (VERIFICATION) layer.

3. Layer and Device rules → 3.28 NBUR module → 3.28.2 Device rules → dhw3

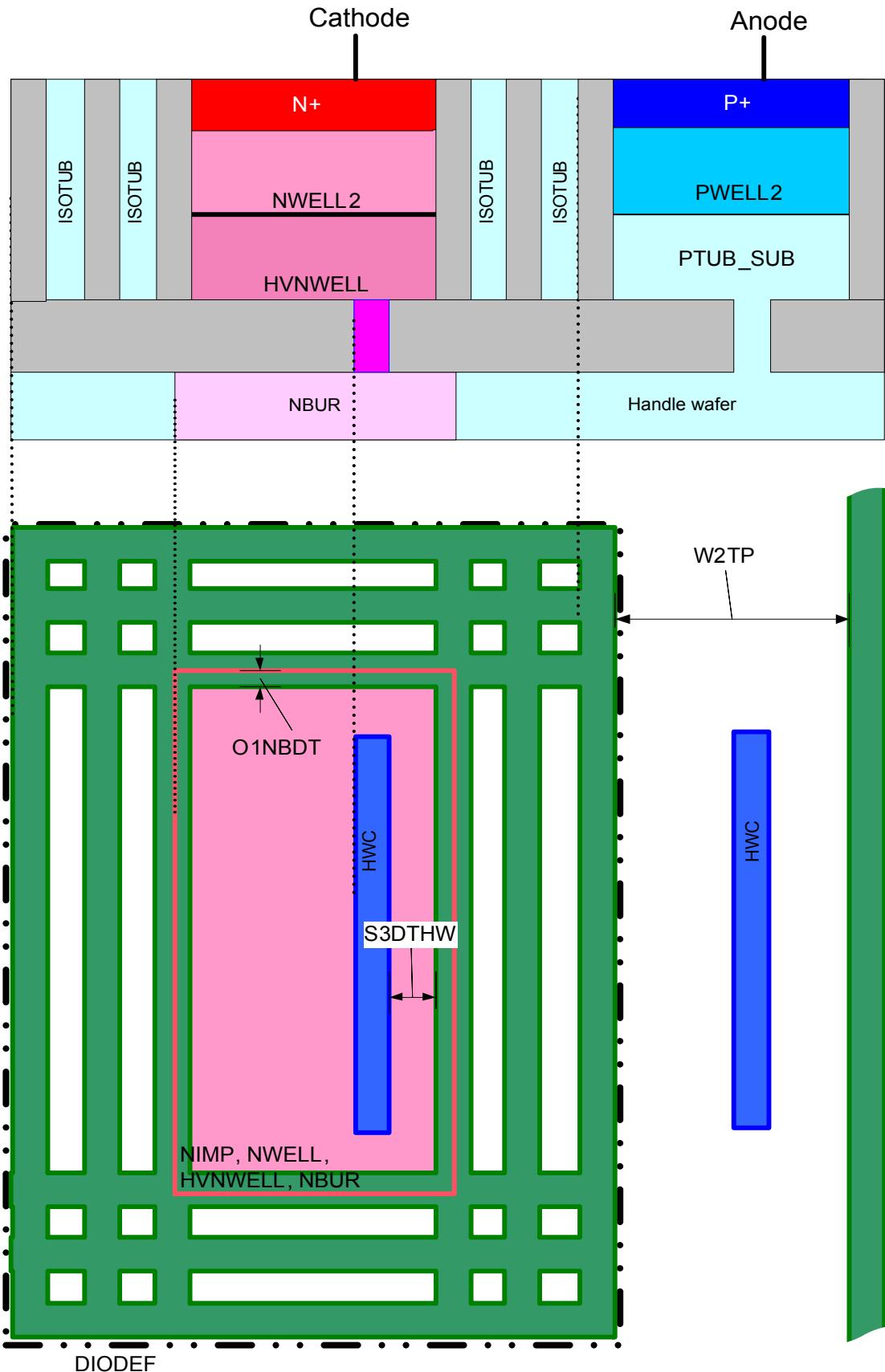


Figure 3.189 dhw3

3. Layer and Device rules → 3.28 NBUR module→ 3.28.2 Device rules→ dhw2b

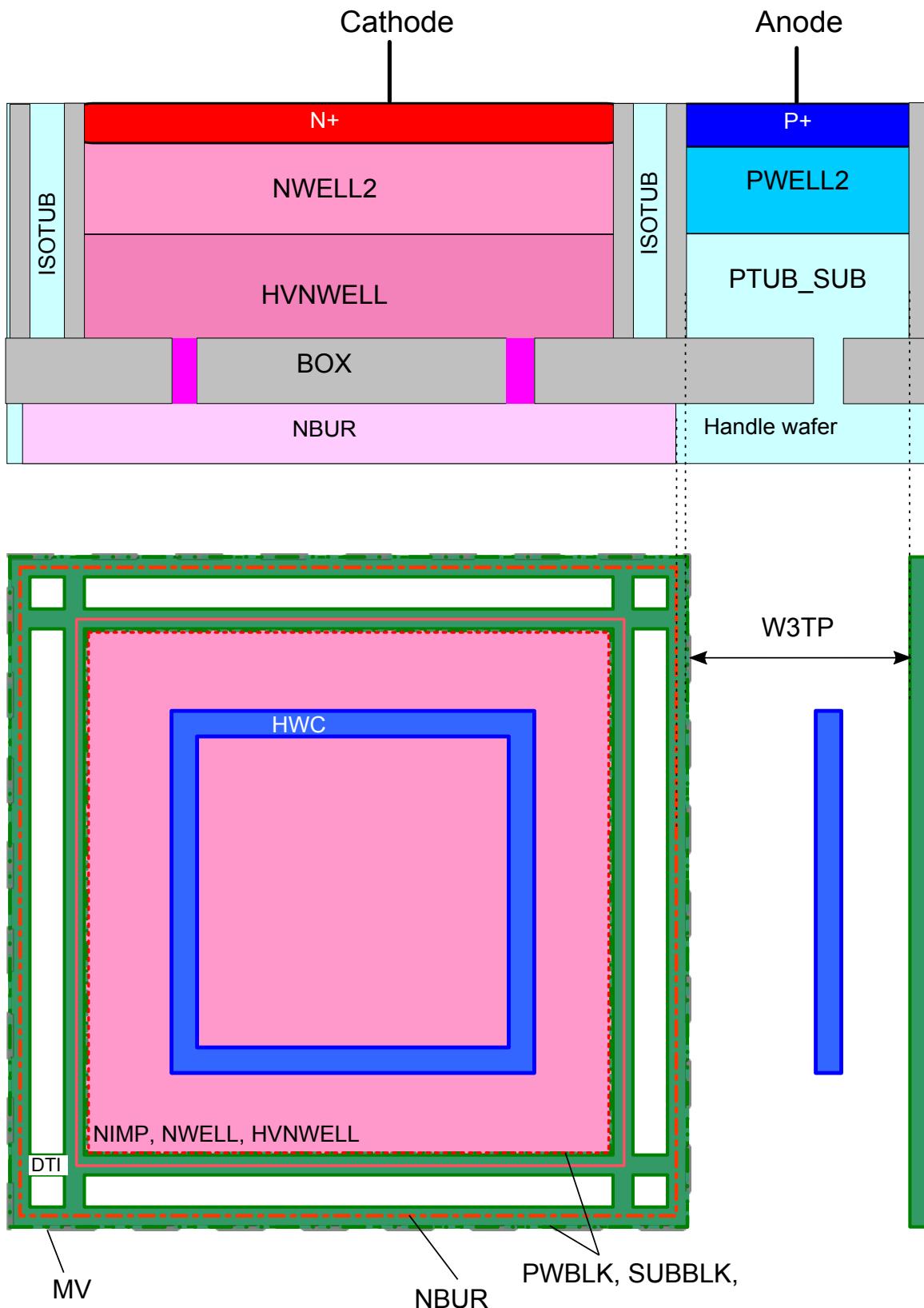
## dhw2b

Name	Description	Value	Unit
B10NB	TUB inside dhw#c, dhw#d must be surrounded by HWNTUB (except ISOTUB or TIEDTUB)	-	-
<u>B11HW</u>	TUB inside dhw#c, dhw#d must have HWC on each side (except ISOTUB or TIEDTUB)	-	-
B3M1	MET1 overlap of ISOTUB is not allowed	-	-
B4NB	dhw#c, dhw#d terminal (Cathode/Anode) short is not allowed	-	-
B6HN	dhw#c, dhw#d must be surrounded by HWPTUB	-	-
W3TP	Minimum HWPTUB width	9.0	µm
W5TN	Minimum HWNTUB width	9.5	µm
W6M2	Maximum (MET2 inside ISOTUB) width	0.5	µm
S5NB	Minimum NBUR spacing (different net)	16.5	µm
S18NB	Minimum NBUR spacing to NBUR (dhw#)	16.5	µm
S9NBHB	Minimum NBUR spacing to SUBBLK	15.0	µm
S9NBHW	Minimum NBUR spacing to HWC	15.0	µm

**Note:** dhw2b device must be labeled "dhw2b" using DIODEF (VERIFICATION) layer.

3. Layer and Device rules → 3.28 NBUR module → 3.28.2 Device rules → dhw2b

### dhw2b, dhw2c



**Figure 3.190** dhw2b

3. Layer and Device rules → 3.28 NBUR module→ 3.28.2 Device rules→ dhw2c

## dhw2c

Name	Description	Value	Unit
B10NB	TUB inside dhw#c, dhw#d must be surrounded by HWNTUB (except ISOTUB or TIEDTUB)	-	-
<u>B11HW</u>	TUB inside dhw#c, dhw#d must have HWC on each side (except ISOTUB or TIEDTUB)	-	-
B3M1	MET1 overlap of ISOTUB is not allowed	-	-
B4NB	dhw#c, dhw#d terminal (Cathode/Anode) short is not allowed	-	-
B6HN	dhw#c, dhw#d must be surrounded by HWPTUB	-	-
W3TP	Minimum HWPTUB width	9.0	µm
W5TN	Minimum HWNTUB width	9.5	µm
W6M2	Maximum (MET2 inside ISOTUB) width	0.5	µm
S8NB	Minimum NBUR spacing (different net)	18.5	µm
S4NBHB	Minimum NBUR spacing to SUBBLK	17.0	µm
S4NBHW	Minimum NBUR spacing to HWC	17.0	µm
S9NB	Minimum NBUR spacing to NBUR (dhw#, dhw2b)	18.5	µm

**Note:** dhw2c device must be labeled "dhw2c" using DIODEF (VERIFICATION) layer.

3. Layer and Device rules → 3.28 NBUR module → 3.28.2 Device rules → dhw2c

### dhw2b, dhw2c

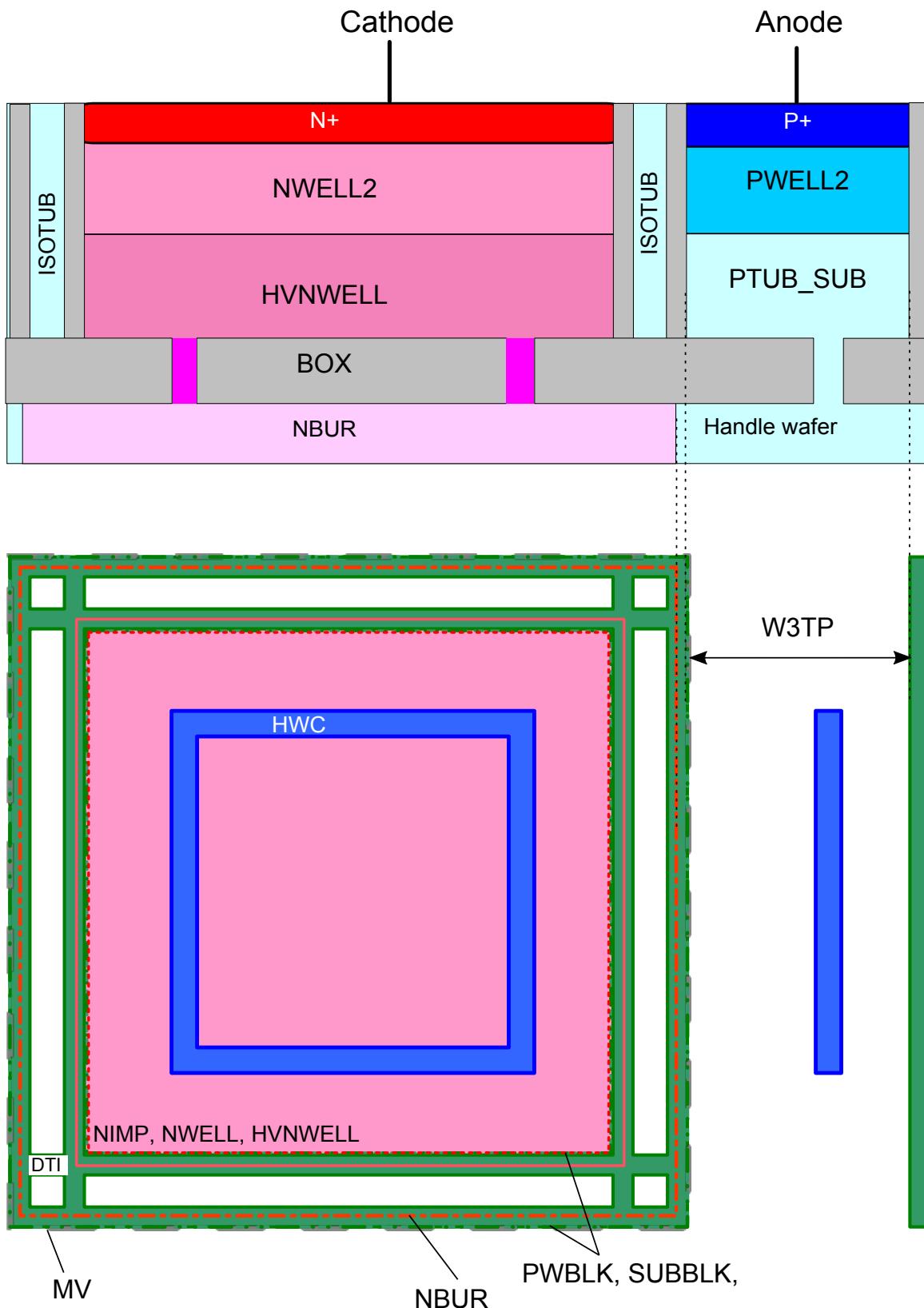


Figure 3.191 dhw2b

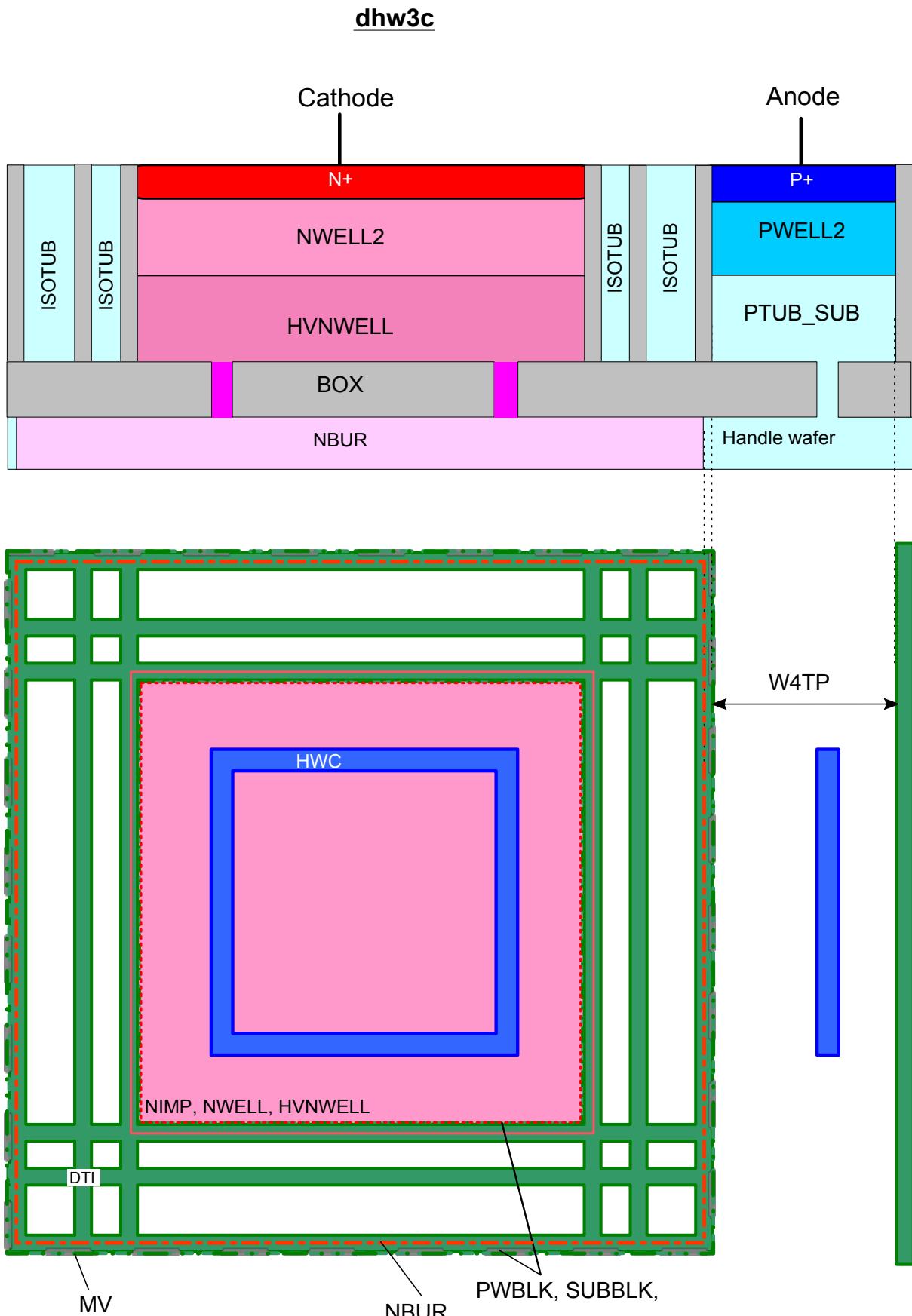
3. Layer and Device rules → 3.28 NBUR module→ 3.28.2 Device rules→ dhw3c

### dhw3c

Name	Description	Value	Unit
B10NB	TUB inside dhw#c, dhw#d must be surrounded by HWNTUB (except ISOTUB or TIEDTUB)	-	-
<u>B11HW</u>	TUB inside dhw#c, dhw#d must have HWC on each side (except ISOTUB or TIEDTUB)	-	-
B3M1	MET1 overlap of ISOTUB is not allowed	-	-
B4NB	dhw#c, dhw#d terminal (Cathode/Anode) short is not allowed	-	-
B6HN	dhw#c, dhw#d must be surrounded by HWPTUB	-	-
W4TP	Minimum HWPTUB width	10.0	µm
W5TN	Minimum HWNTUB width	9.5	µm
W6M2	Maximum (MET2 inside ISOTUB) width	0.5	µm
S10NB	Minimum NBUR spacing (different net)	20.0	µm
S11NB	Minimum NBUR spacing to NBUR (dhw#, dhw2b, dhw2c)	20.0	µm
S5NBHB	Minimum NBUR spacing to SUBBLK	18.5	µm
S5NBHW	Minimum NBUR spacing to HWC	18.5	µm

**Note:** dhw3c device must be labeled "dhw3c" using DIODEF (VERIFICATION) layer.

3. Layer and Device rules → 3.28 NBUR module → 3.28.2 Device rules → dhw3c



**Figure 3.192 dhw3c**

3. Layer and Device rules → 3.28 NBUR module→ 3.28.2 Device rules→ dhw4c

### dhw4c

Name	Description	Value	Unit
B10NB	TUB inside dhw#c, dhw#d must be surrounded by HWNTUB (except ISOTUB or TIEDTUB)	-	-
<u>B11HW</u>	TUB inside dhw#c, dhw#d must have HWC on each side (except ISOTUB or TIEDTUB)	-	-
B3M1	MET1 overlap of ISOTUB is not allowed	-	-
B4NB	dhw#c, dhw#d terminal (Cathode/Anode) short is not allowed	-	-
B6HN	dhw#c, dhw#d must be surrounded by HWPTUB	-	-
W5TN	Minimum HWNTUB width	9.5	µm
W5TP	Minimum HWPTUB width	15.0	µm
W6M2	Maximum (MET2 inside ISOTUB) width	0.5	µm
S12NB	Minimum NBUR spacing (different net)	21.0	µm
S13NB	Minimum NBUR spacing to NBUR (dhw#, dhw2b, dhw2c, dhw3c)	21.0	µm
S6NBHB	Minimum NBUR spacing to SUBBLK	19.5	µm
S6NBHW	Minimum NBUR spacing to HWC	19.5	µm

**Note:** dhw4c device must be labeled "dhw4c" using DIODEF (VERIFICATION) layer.

3. Layer and Device rules → 3.28 NBUR module → 3.28.2 Device rules → dhw4c

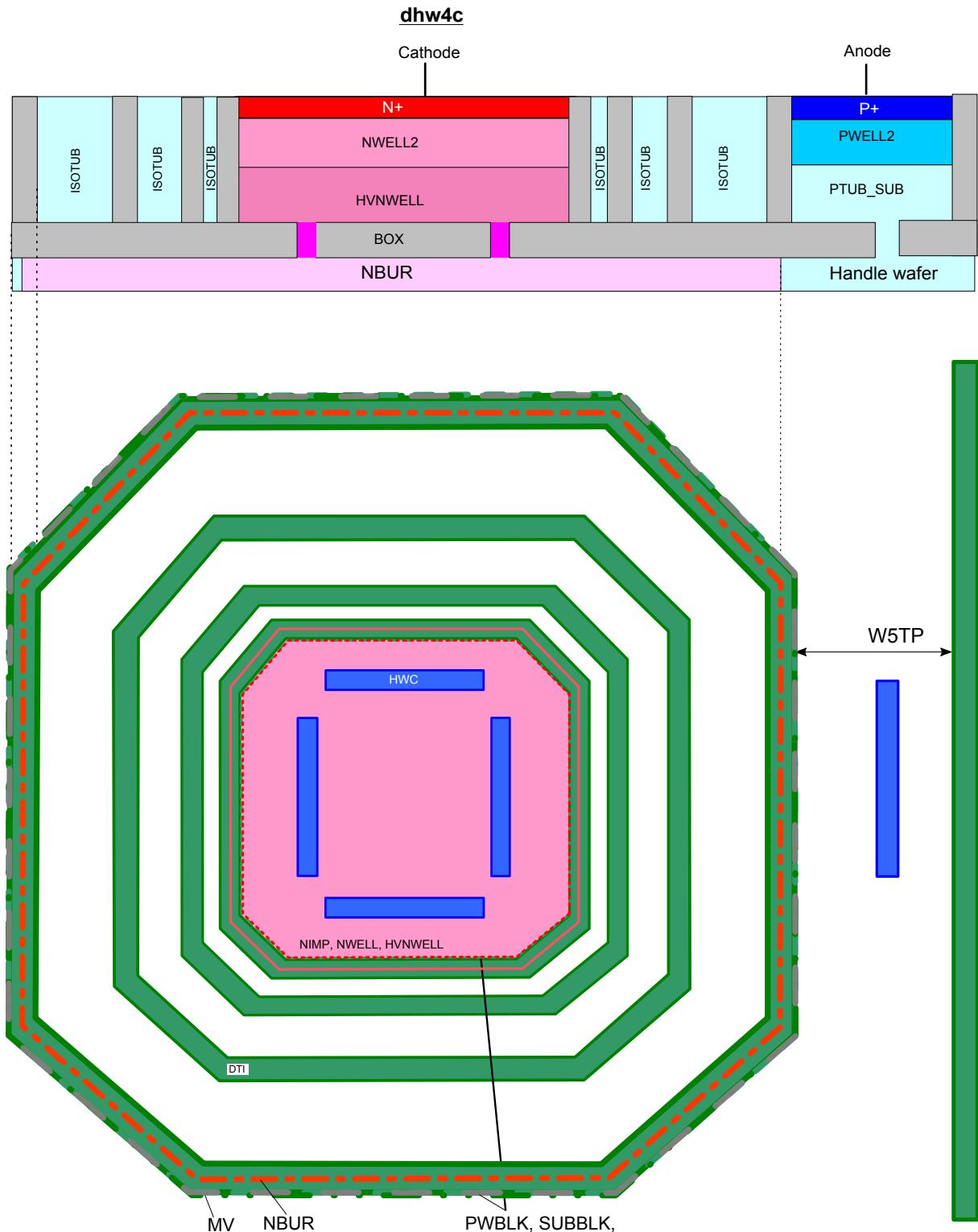


Figure 3.193 dhw4c

3. Layer and Device rules → 3.28 NBUR module→ 3.28.2 Device rules→ dhw4d

### dhw4d

Name	Description	Value	Unit
B10NB	TUB inside dhw#c, dhw#d must be surrounded by HWNTUB (except ISOTUB or TIEDTUB)	-	-
<u>B11HW</u>	TUB inside dhw#c, dhw#d must have HWC on each side (except ISOTUB or TIEDTUB)	-	-
B3M1	MET1 overlap of ISOTUB is not allowed	-	-
B4NB	dhw#c, dhw#d terminal (Cathode/Anode) short is not allowed	-	-
B6HN	dhw#c, dhw#d must be surrounded by HWPTUB	-	-
W5TP	Minimum HWPTUB width	15.0	µm
W6M2	Maximum (MET2 inside ISOTUB) width	0.5	µm
W6TN	Minimum HWNTUB width	17.5	µm
S16NB	Minimum NBUR spacing (different net)	23.0	µm
S14NB	Minimum NBUR spacing to NBUR (dhw#, dhw#c)	23.0	µm
S5DTHW	Minimum DTI spacing to HWC	8.0	µm
<u>S6DTHW</u>	Maximum DTI spacing to HWC	16.0	µm
S7NBHB	Minimum NBUR spacing to SUBBLK	21.5	µm
S7NBHW	Minimum NBUR spacing to HWC	21.5	µm

**Note:** dhw4d device must be labeled "dhw4d" using DIODEF (VERIFICATION) layer.

3. Layer and Device rules → 3.28 NBUR module → 3.28.2 Device rules → dhw4d

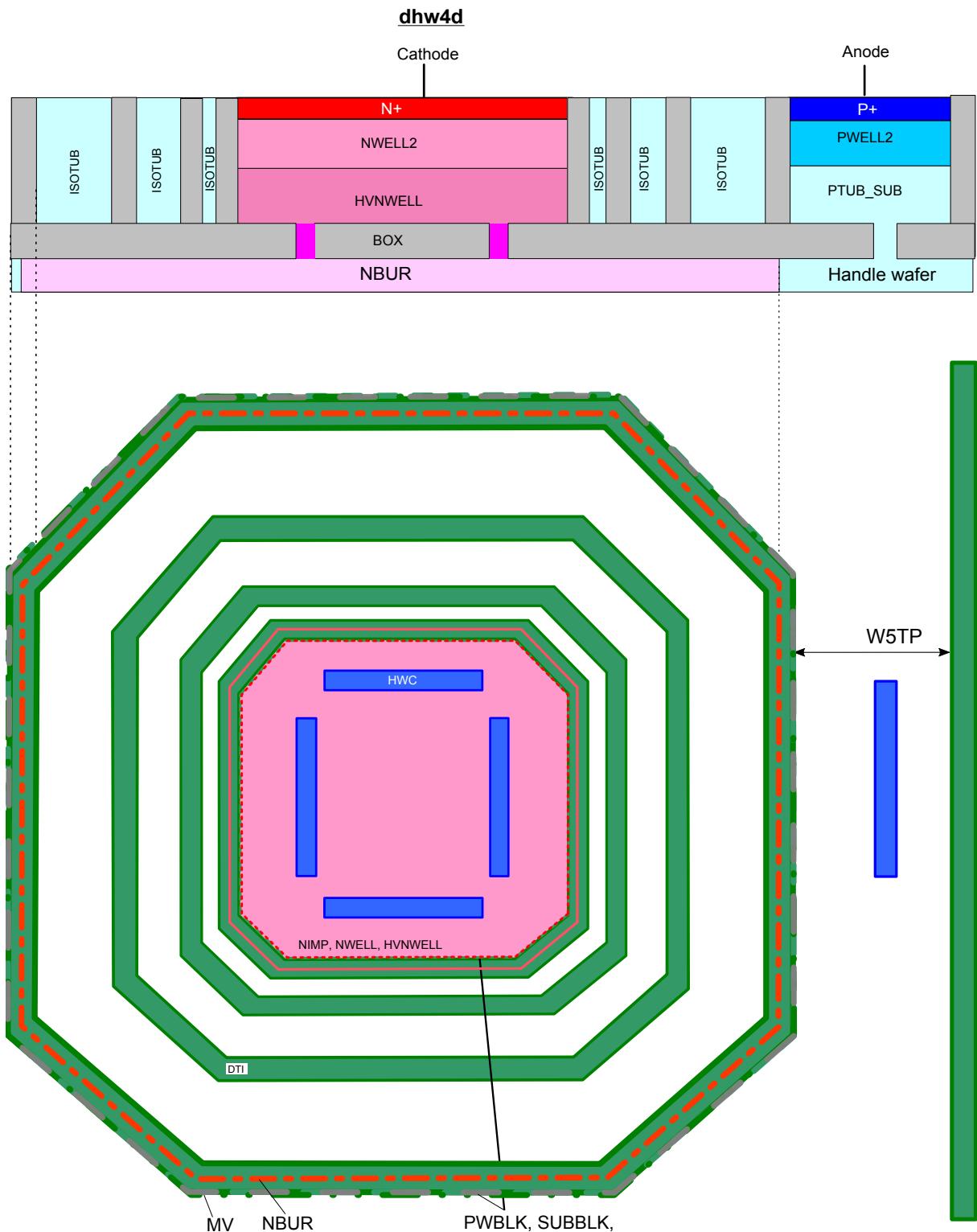


Figure 3.194 dhw4d

3. Layer and Device rules → 3.28 NBUR module→ 3.28.2 Device rules→ dhw5d

## dhw5d

Name	Description	Value	Unit
B10NB	TUB inside dhw#c, dhw#d must be surrounded by HWNTUB (except ISOTUB or TIEDTUB)	-	-
<u>B11HW</u>	TUB inside dhw#c, dhw#d must have HWC on each side (except ISOTUB or TIEDTUB)	-	-
B3M1	MET1 overlap of ISOTUB is not allowed	-	-
B4NB	dhw#c, dhw#d terminal (Cathode/Anode) short is not allowed	-	-
B6HN	dhw#c, dhw#d must be surrounded by HWPTUB	-	-
W5TP	Minimum HWPTUB width	15.0	µm
W6M2	Maximum (MET2 inside ISOTUB) width	0.5	µm
W6TN	Minimum HWNTUB width	17.5	µm
S17NB	Minimum NBUR spacing (different net)	24.0	µm
S15NB	Minimum NBUR spacing to NBUR (dhw#, dhw#c, dhw4d)	24.0	µm
S5DTHW	Minimum DTI spacing to HWC	8.0	µm
<u>S6DTHW</u>	Maximum DTI spacing to HWC	16.0	µm
S8NBHB	Minimum NBUR spacing to SUBBLK	22.5	µm
S8NBHW	Minimum NBUR spacing to HWC	22.5	µm

**Note:** dhw5d device must be labeled "dhw5d" using DIODEF (VERIFICATION) layer.

## 3. Layer and Device rules → 3.28 NBUR module → 3.28.2 Device rules → dhw5d

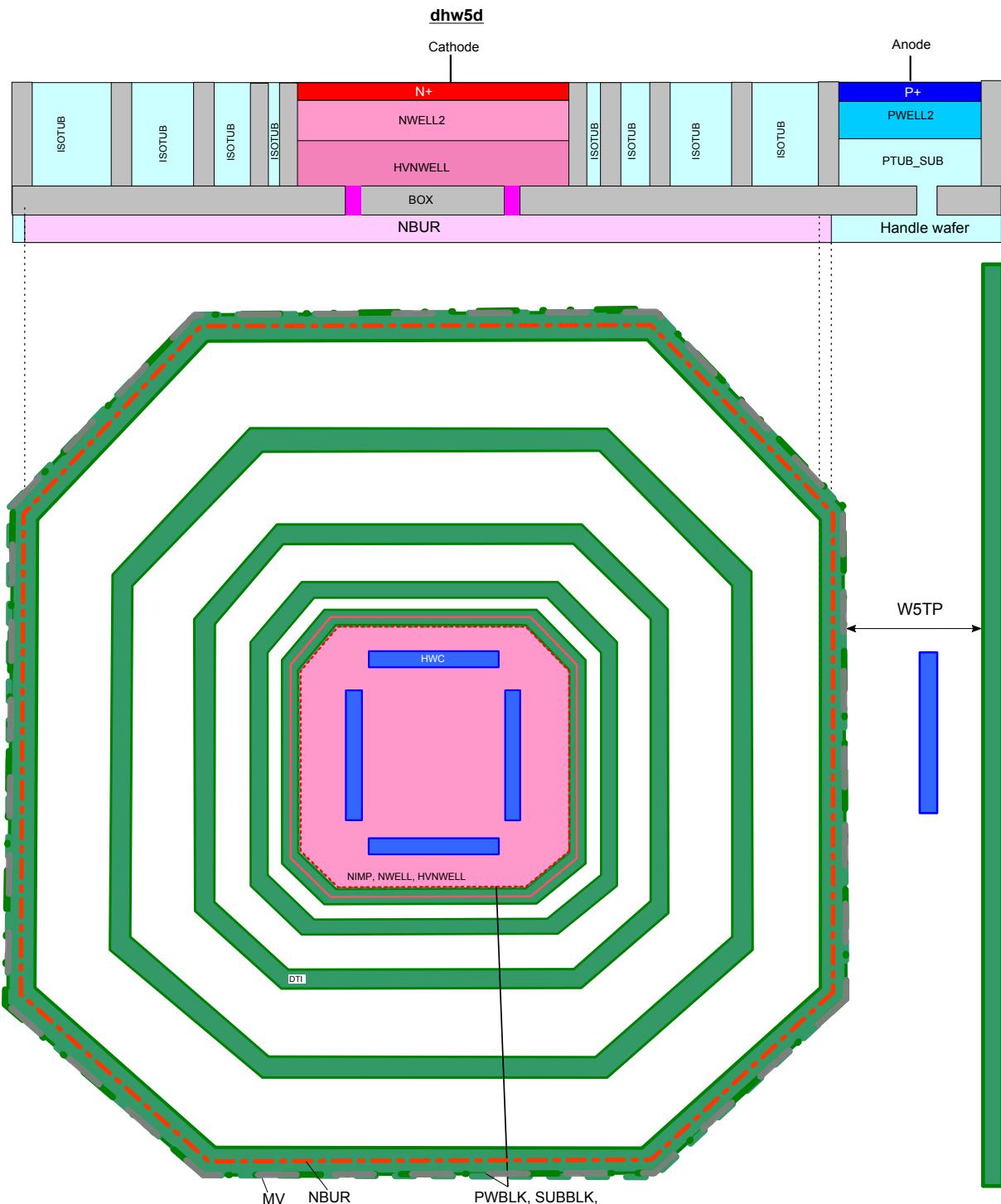


Figure 3.195 dhw5d

3. Layer and Device rules → 3.29 NHVA module

## 3.29 NHVA module

### 3.29.1 Layer rules

#### NDF

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1NX	NDF is only allowed for nhv#, ndhv#, dfwdn#	-	-
B2NX	NDF overlap of PDF or PZENER is not allowed	-	-
B3NX	NDF overlap of DEPL is not allowed (except ndhv#)	-	-
B4NX	NDF without PWBLK, MV and SUBBLK is not allowed	-	-
W1NX	Minimum NDF width	2.0	μm
S1NX	Minimum NDF spacing/notch	1.0	μm
A1NX	Minimum NDF area	4.0	μm <sup>2</sup>

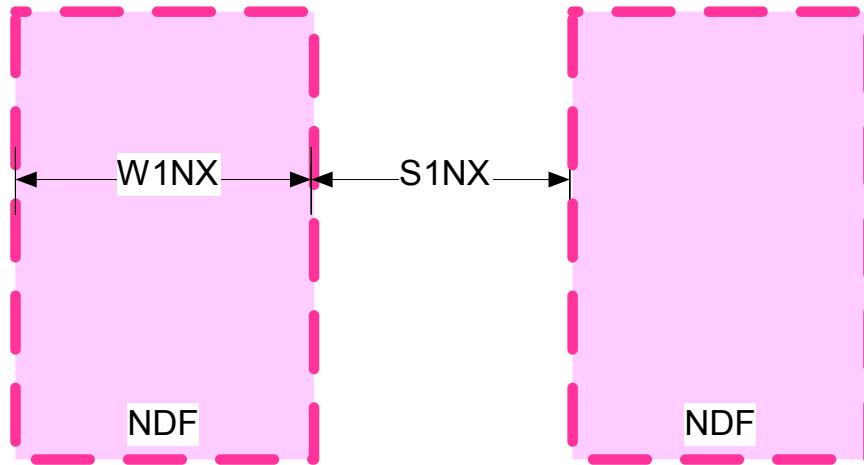


Figure 3.196 NDF

#### NDF\_E

Name	Description	Value	Unit
W2NX	Minimum NDF_E width	0.5	μm

3. Layer and Device rules → 3.29 NHVA module → 3.29.1 Layer rules → PWELL4

## PWELL4

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1P4	PWELL4 is only allowed for nhv#, ndhv#, dfwdn#, dnpa, dnpati, nhvr#, ndhvr# or dfwdnh#	-	-
B2P4	PWELL4 overlap of NWELL, DPC, HVPWELL, SJNP or SJPN is not allowed	-	-
B4P4	PWELL4 without MV and SUBBLK is not allowed	-	-
W1P4	Minimum PWELL4 width	1.0	μm
S1P4	Minimum PWELL4 spacing/notch	1.0	μm
S1P4DN	Minimum PWELL4 spacing to NDIFF	0.25	μm
E1P4DN	Minimum PWELL4 enclosure of NDIFF	0.43	μm
E1P4DP	Minimum PWELL4 enclosure of PDIFF (except dfwdn#, dfwdnh#)	0.25	μm
A1P4	Minimum PWELL4 area	2.25	μm <sup>2</sup>

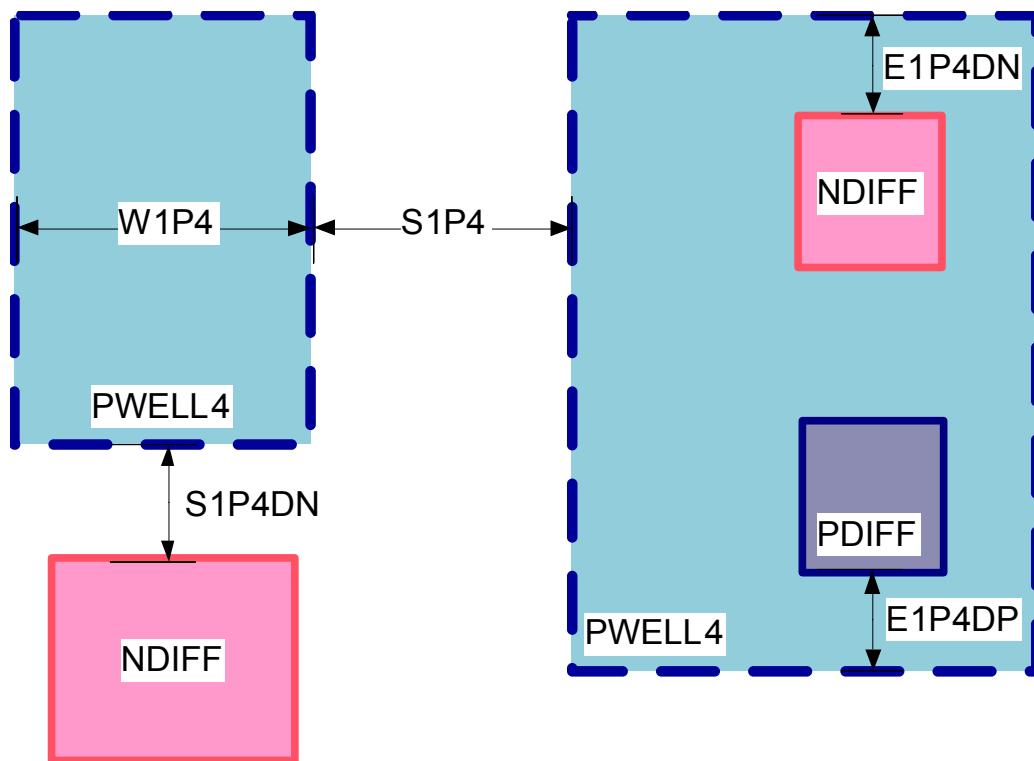


Figure 3.197 PWELL4

## PWELL4\_E

Name	Description	Value	Unit
W2P4	Minimum PWELL4_E width	0.5	μm

## 3.29.2 Device rules

### nhvta

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

## 3. Layer and Device rules → 3.29 NHVA module→ 3.29.2 Device rules→ nhvta

Name	Description	Value	Unit
B10MV	nhvta without MV is not allowed	-	-
B11HB	nhvta without SUBBLK is not allowed	-	-
W15GA	Maximum CHANNEL length <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	1.5	μm
W17GA	Minimum CHANNEL length <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.4	μm
W2IP	Minimum PIMP width	0.42	μm
	Minimum GATE width	3.0	μm
W8GA	<b>Note:</b> Minimum GATE width is defined as single GATE finger width. <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
S2IN	Minimum NIMP spacing/notch	0.42	μm
S2PB	Minimum PWBLK spacing/notch	0.6	μm
S9DF	Fixed DRAIN-EDGE-STI length	1.25	μm
S2P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.65	μm
S5GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S7M1	Minimum MET1 of DRAIN NDIFF spacing to MET1	0.28	μm
E1M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	μm
E1NXDN	Minimum NDF enclosure of DRAIN NDIFF	1.8	μm
E1PBP1	Fixed PWBLK enclosure of POLY1 in SOURCE region	0.18	μm
E2M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	μm
E12P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E1P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.6	μm
E2DNP1	Minimum NDIFF extension beyond POLY1	0.27	μm
O1NXGA	Fixed NDF overlap of GATE	0.55	μm

**Note:** nhvta device must be labeled "nhvta" using POLY1 (VERIFICATION) layer over GATE

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** Each transistor must be surrounded by DTI ring.

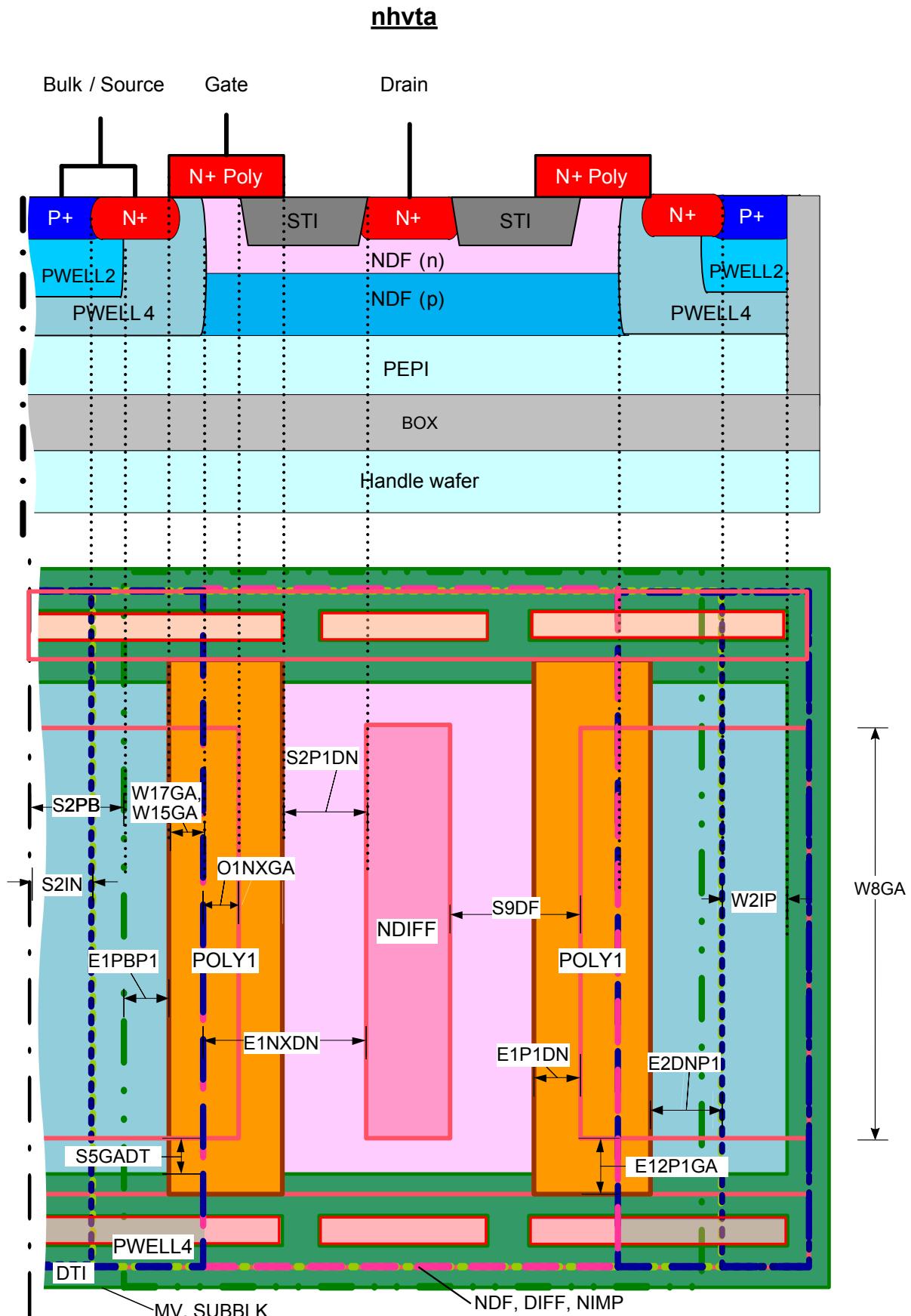
**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → nhvta



**Figure 3.198 nhvta**

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → nhvtaa

## nhvtaa

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B14HB	nhvtaa without SUBBLK is not allowed	-	-
B20MV	nhvtaa without MV is not allowed	-	-
W15GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	1.5	μm
W17GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.4	μm
W2IP	Minimum PIMP width	0.42	μm
W8GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.	3.0	μm
S2IN	Minimum NIMP spacing/notch	0.42	μm
S2PB	Minimum PWBLK spacing/notch	0.6	μm
S9DF	Fixed DRAIN-EDGE-STI length	1.25	μm
S11GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	2.5	μm
S2P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.65	μm
S7M1	Minimum MET1 of DRAIN NDIFF spacing to MET1	0.28	μm
E17M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	4.0	μm
E1M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	μm
E1NXDN	Minimum NDF enclosure of DRAIN NDIFF	1.8	μm
E1PBP1	Fixed PWBLK enclosure of POLY1 in SOURCE region	0.18	μm
E17P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	3.0	μm
E1P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.6	μm
E2DNP1	Minimum NDIFF extension beyond POLY1	0.27	μm
O1NXGA	Fixed NDF overlap of GATE	0.55	μm

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** nhvtaa device must be labeled "nhvtaa" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → nhvtaa

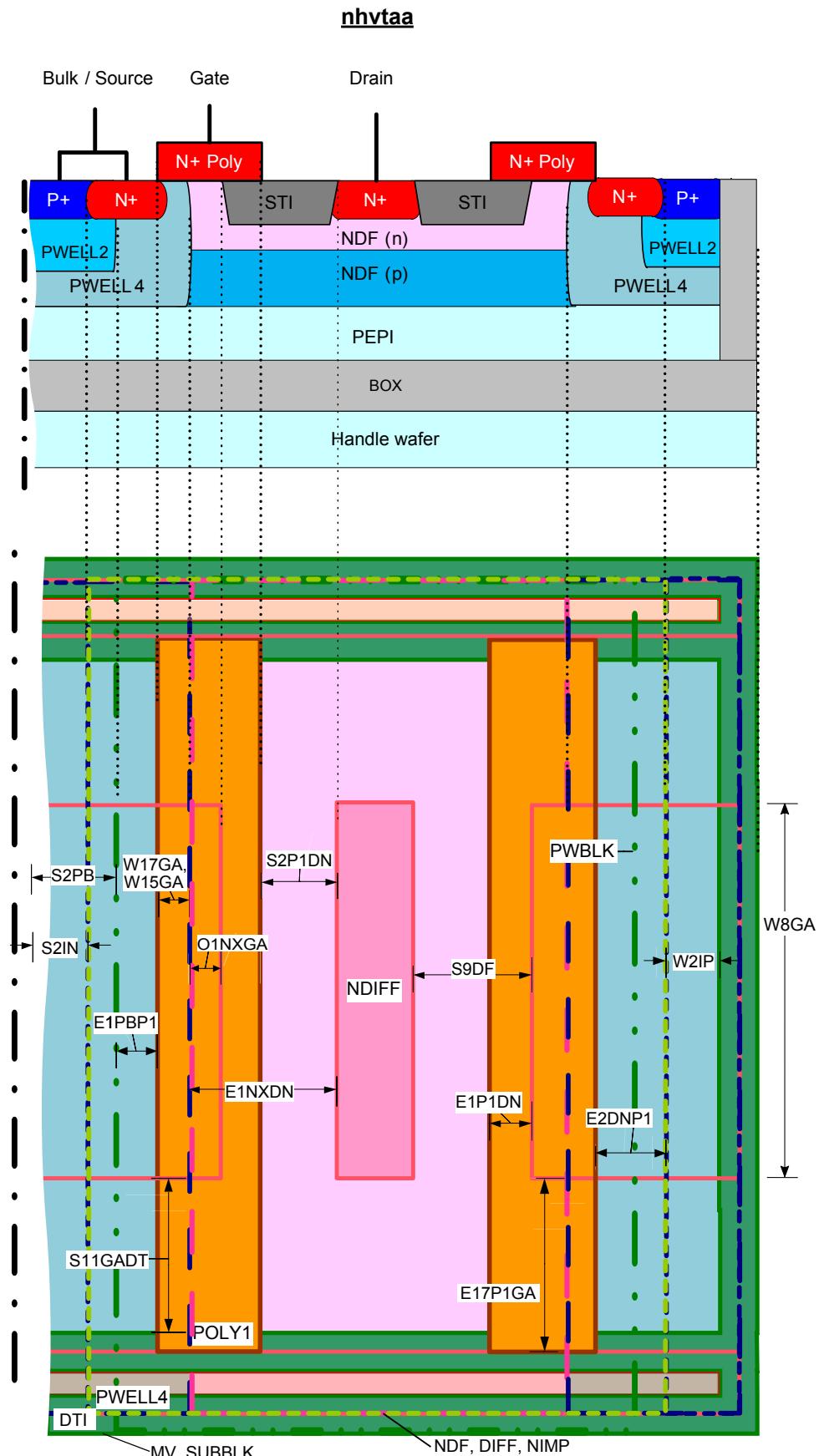


Figure 3.199 nhvtaa

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → nhvtb

## **nhvtb**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11MV	nhvtb without MV is not allowed	-	-
B3HB	nhvtb without SUBBLK is not allowed	-	-
B5NX	MET1 is not allowed over NDF (except predefined POLY1 GATE connection, predefined MET1 device terminal connections)	-	-
W16GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	25.0	μm
W2IP	Minimum PIMP width	0.42	μm
W7GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.5	μm
W8GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.	3.0	μm
S2IN	Minimum NIMP spacing/notch	0.42	μm
S2PB	Minimum PWBLK spacing/notch	0.6	μm
S10DF	Fixed DRAIN-EDGE-STI length	2.4	μm
S3P1DN	Minimum POLY1 spacing to DRAIN NDIFF	1.55	μm
S5GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
E1M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	μm
E2M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	μm
E2NXDN	Minimum NDF enclosure of DRAIN NDIFF	2.5	μm
E2PBP1	Fixed PWBLK enclosure POLY1 in SOURCE region	0.23	μm
E12P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E2P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.85	μm
O1NXP4	Fixed NDF overlap of PWELL4	0.1	μm
O2NXGA	Fixed NDF overlap of GATE	0.65	μm

**Note:** nhvtb device must be labeled "nhvtb" using POLY1 (VERIFICATION) layer over GATE

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

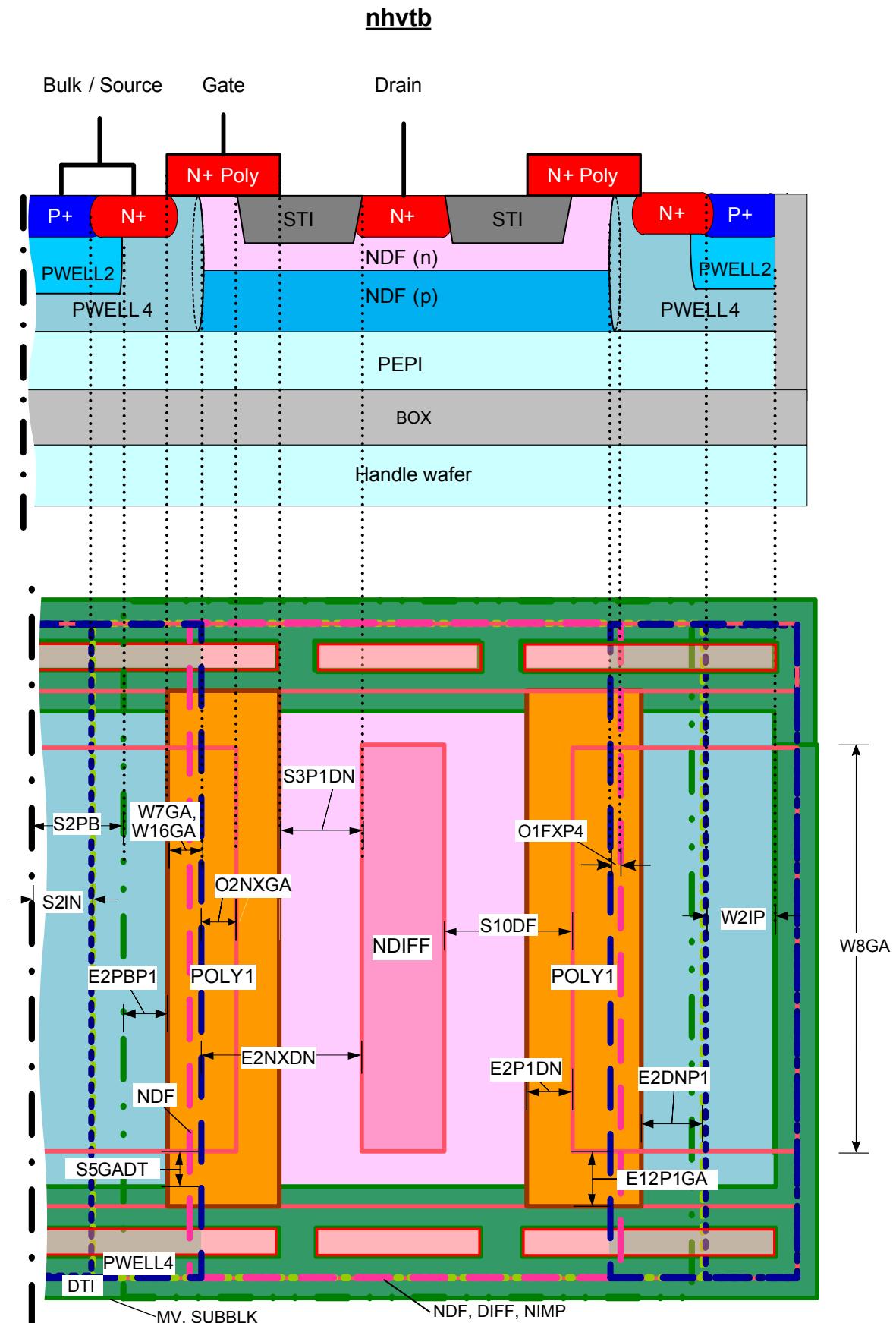
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer.

Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → nhvtb



**Figure 3.200 nhvtb**

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → nhvu

## **nhvu**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B12MV	nhvu without MV is not allowed	-	-
B4HB	nhvu without SUBBLK is not allowed	-	-
B5NX	MET1 is not allowed over NDF (except predefined POLY1 GATE connection, predefined MET1 device terminal connections)	-	-
W16GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	25.0	µm
W2IP	Minimum PIMP width	0.42	µm
W7GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.5	µm
W8GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.	3.0	µm
S2IN	Minimum NIMP spacing/notch	0.42	µm
S2PB	Minimum PWBLK spacing/notch	0.6	µm
S11DF	Fixed DRAIN-EDGE-STI length	4.45	µm
S4P1DN	Minimum POLY1 spacing to DRAIN NDIFF	2.6	µm
S5GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E1M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	µm
E2M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	µm
E2NXDN	Minimum NDF enclosure of DRAIN NDIFF	2.5	µm
E2PBP1	Fixed PWBLK enclosure POLY1 in SOURCE region	0.23	µm
E12P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E3P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	1.85	µm
O1NXP4	Fixed NDF overlap of PWELL4	0.1	µm
O2NXGA	Fixed NDF overlap of GATE	0.65	µm

**Note:** nhvu device must be labeled "nhvu" using POLY1 (VERIFICATION) layer over GATE

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

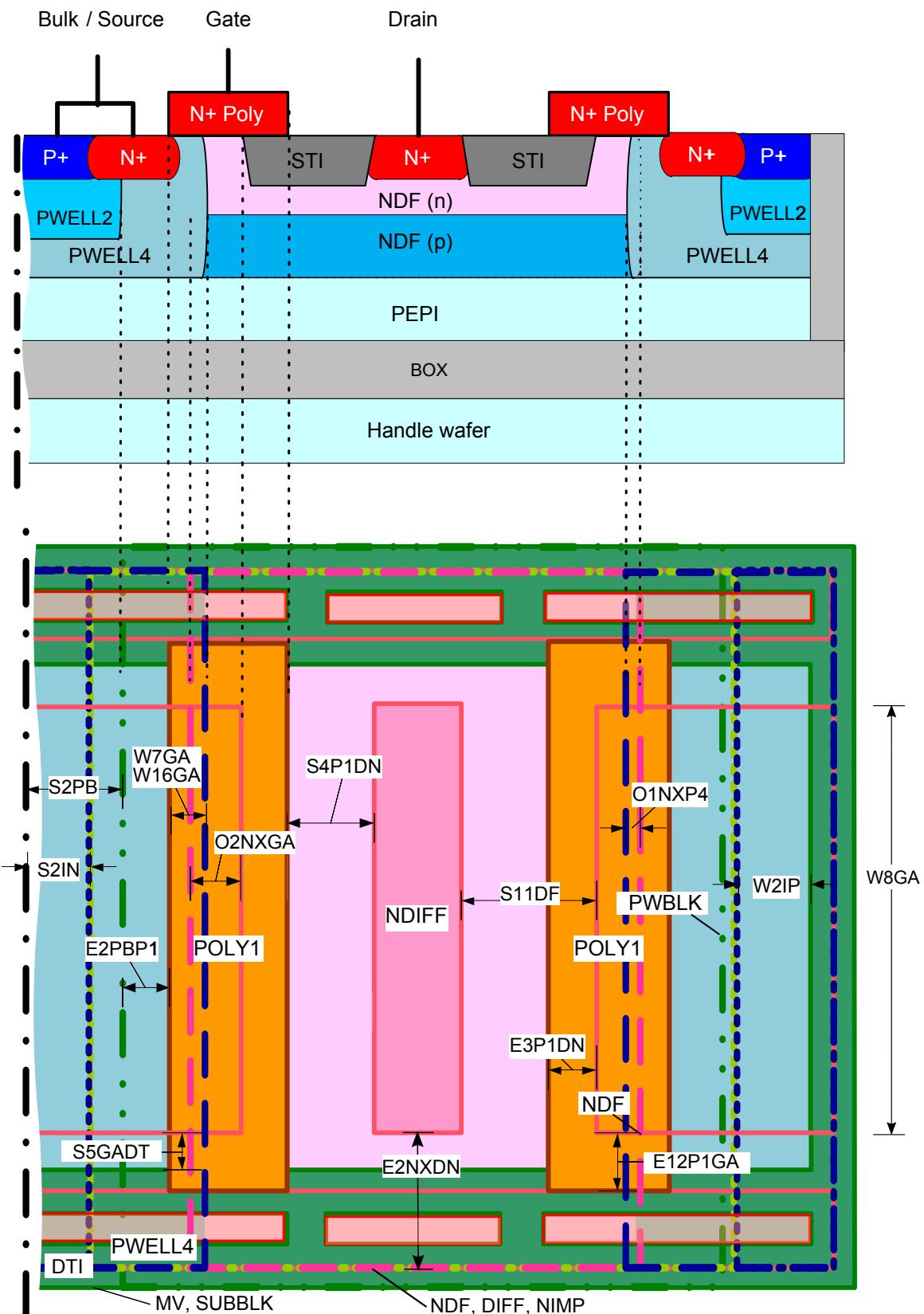
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → nhvu

### nhvu



**Figure 3.201 nhvu**

3. Layer and Device rules → 3.29 NHVA module→ 3.29.2 Device rules→ dfwdnt

### **dfwdnt**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13MV	dfwdnt without MV is not allowed	-	-
B5HB	dfwdnt without SUBBLK is not allowed	-	-
B5NX	MET1 is not allowed over NDF (except predefined POLY1 GATE connection, predefined MET1 device terminal connections)	-	-
W2IP	Minimum PIMP width	0.42	μm
S2IN	Minimum NIMP spacing/notch	0.42	μm
S2PB	Minimum PWBLK spacing/notch	0.6	μm
S12DF	Fixed CATHODE-EDGE-STI length	2.4	μm
S5P1DN	Minimum POLY1 spacing to Cathode NDIFF	1.55	μm
E1INNX	Fixed NIMP enclosure of NDF (in the direction of device length)	0.1	μm
E2P4DP	Minimum PWELL4 enclosure of PDIFF	0.2	μm
E3M1DN	Fixed MET1 enclosure of Cathode NDIFF (in the direction of device length)	0.5	μm
E3PBP1	Fixed PWBLK enclosure of POLY1 in Anode region	0.23	μm
E4M1DN	Fixed MET1 enclosure of Cathode NDIFF (in the direction of device width)	2.0	μm
E4NXDN	Minimum NDF enclosure of Cathode NDIFF	2.5	μm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	μm
E4P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	0.85	μm
O1P1DP	Minimum POLY1 overlap PDIFF	0.3	μm
O2NXP4	Fixed NDF overlap of PWELL4	0.1	μm
O3NXGA	Fixed NDF overlap of GATE Anode	0.65	μm

**Note:** Minimum drawn finger width is 5 μm

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

**Note:** Each diode must be surrounded by DTI ring

**Note:** Device finger width is defined as Cathode NDIFF width

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → dfwdnt

### dfwdnt

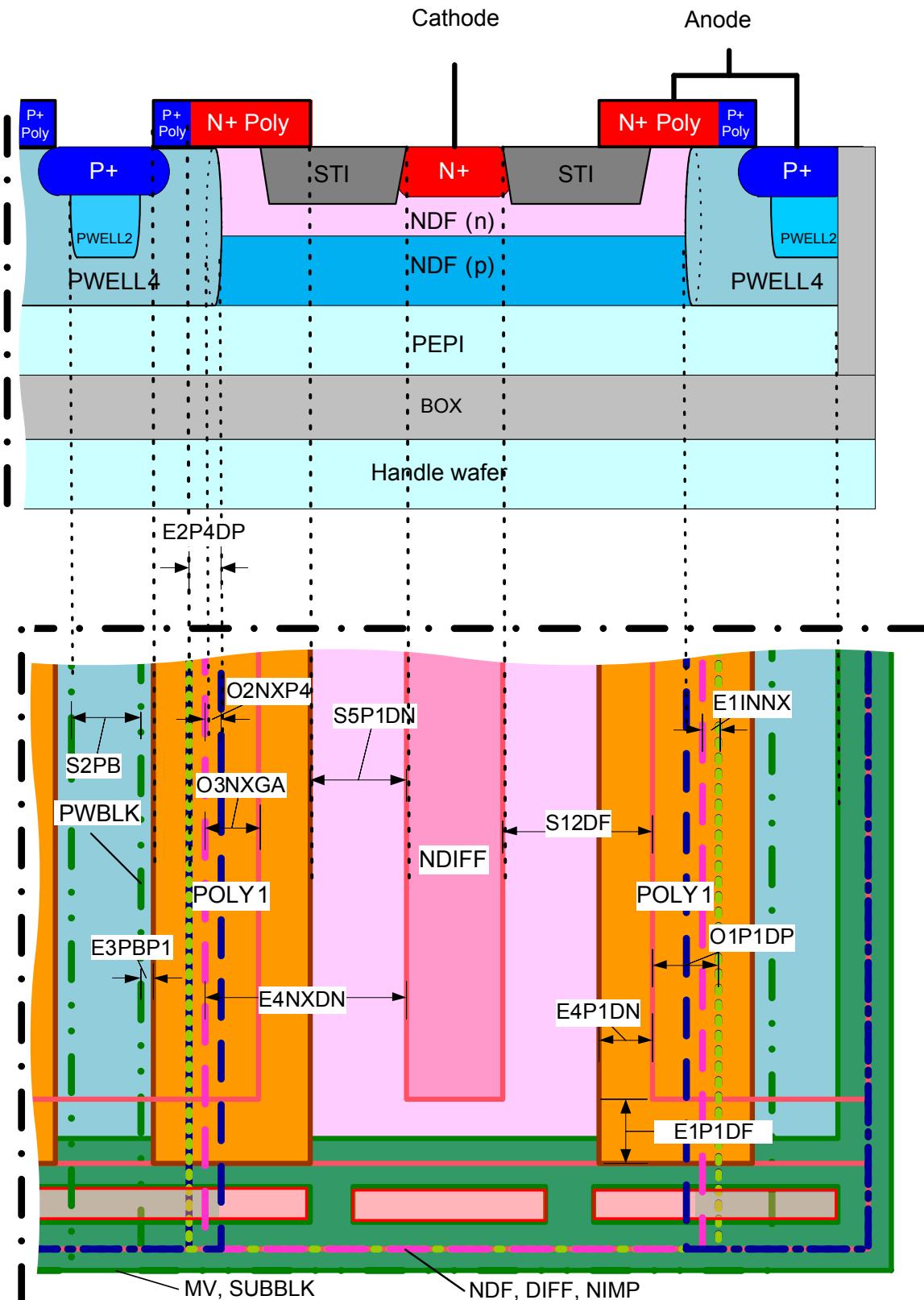


Figure 3.202 dfwdnt

3. Layer and Device rules → 3.29 NHVA module→ 3.29.2 Device rules→ dfwdnru

### **dfwdnru**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B14MV	dfwdnru without MV is not allowed	-	-
B5NX	MET1 is not allowed over NDF (except predefined POLY1 GATE connection, predefined MET1 device terminal connections)	-	-
B6HB	dfwdnru without SUBBLK is not allowed	-	-
W2IP	Minimum PIMP width	0.42	μm
S2IN	Minimum NIMP spacing/notch	0.42	μm
S2PB	Minimum PWBLK spacing/notch	0.6	μm
S13DF	Fixed CATHODE-EDGE-STI length	4.45	μm
S6P1DN	Minimum POLY1 spacing to Cathode NDIFF	2.6	μm
E1INNX	Fixed NIMP enclosure of NDF (in the direction of device length)	0.1	μm
E2P4DP	Minimum PWELL4 enclosure of PDIFF	0.2	μm
E3M1DN	Fixed MET1 enclosure of Cathode NDIFF (in the direction of device length)	0.5	μm
E3PBP1	Fixed PWBLK enclosure of POLY1 in Anode region	0.23	μm
E4M1DN	Fixed MET1 enclosure of Cathode NDIFF (in the direction of device width)	2.0	μm
E4NXDN	Minimum NDF enclosure of Cathode NDIFF	2.5	μm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	μm
E5P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	1.85	μm
O1P1DP	Minimum POLY1 overlap PDIFF	0.3	μm
O2NXP4	Fixed NDF overlap of PWELL4	0.1	μm
O3NXGA	Fixed NDF overlap of GATE Anode	0.65	μm

**Note:** Minimum drawn finger width is 5 μm

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** One additional DTI ring is necessary if the device is placed inside HWTUB.

**Note:** Each diode must be surrounded by DTI ring

**Note:** Device finger width is defined as Cathode NDIFF width

3. Layer and Device rules → 3.29 NHVA module → 3.29.2 Device rules → dfwdnu

### dfwdnu

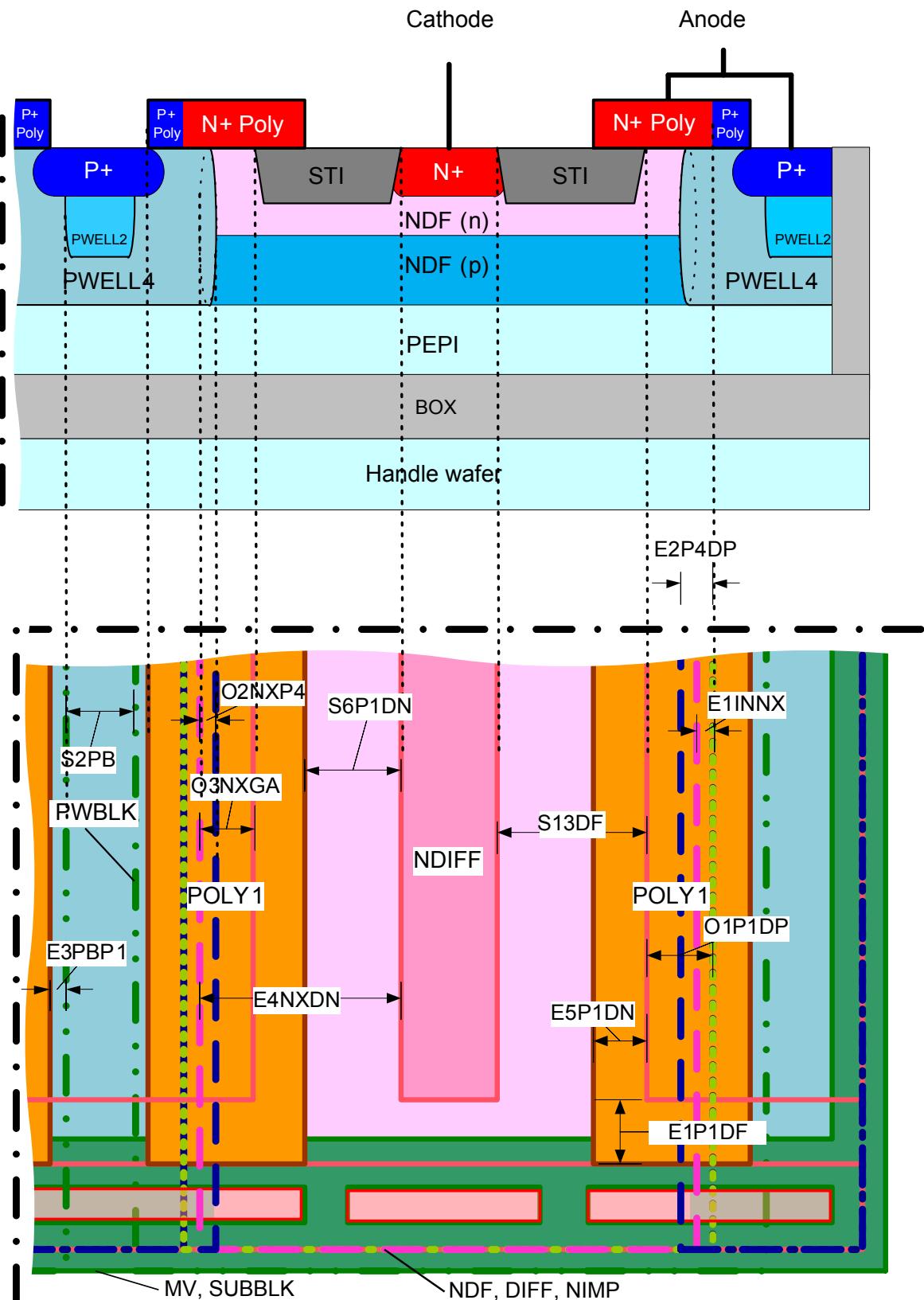


Figure 3.203 dfwdnu

3. Layer and Device rules → 3.29 NHVA module→ 3.29.2 Device rules→ dnpa

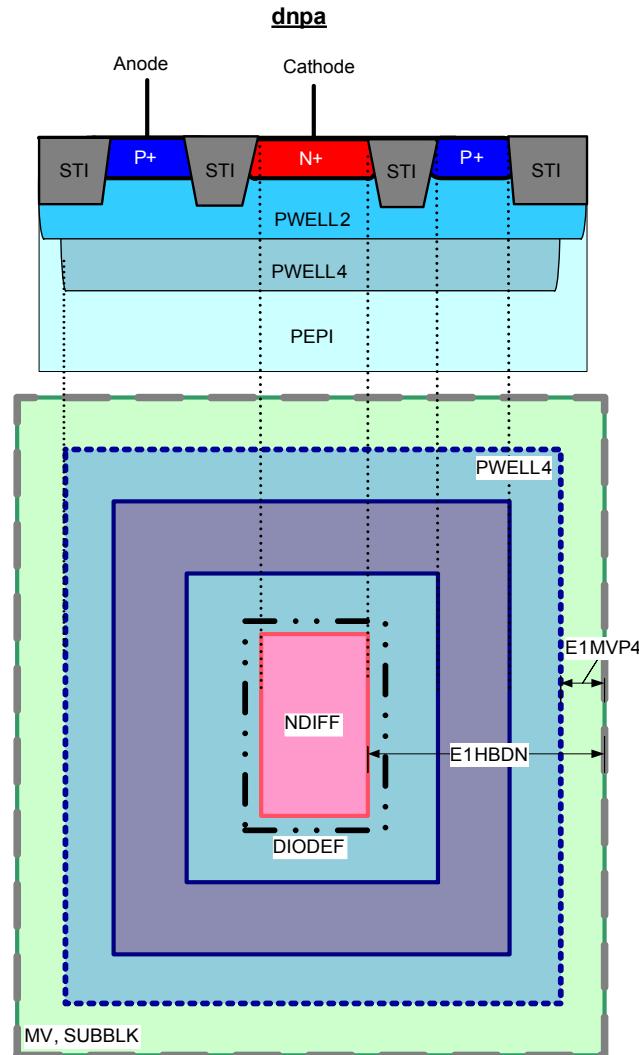
### **dnpa**

The layout of the dnpa protection diode is predefined and only the cathode width can be changed in the range of 2.0  $\mu\text{m}$  to 200.0  $\mu\text{m}$ . Fixed cathode length is 1.0  $\mu\text{m}$ .

Name	Description	Value	Unit
E1HBDN	Minimum SUBBLK enclosure of NDIFF	1.68	$\mu\text{m}$
E1MVP4	Minimum MV enclosure of PWELL4	0.5	$\mu\text{m}$

**Note:** A DTI ring is necessary, valid if Vanode is higher than the handle wafer voltage.

**Note:** MV, PWELL4, SUBBLK are necessary for this device



**Figure 3.204 dnpa**

3. Layer and Device rules → 3.29 NHVA module→ 3.29.2 Device rules→ dnpati

### dnpati

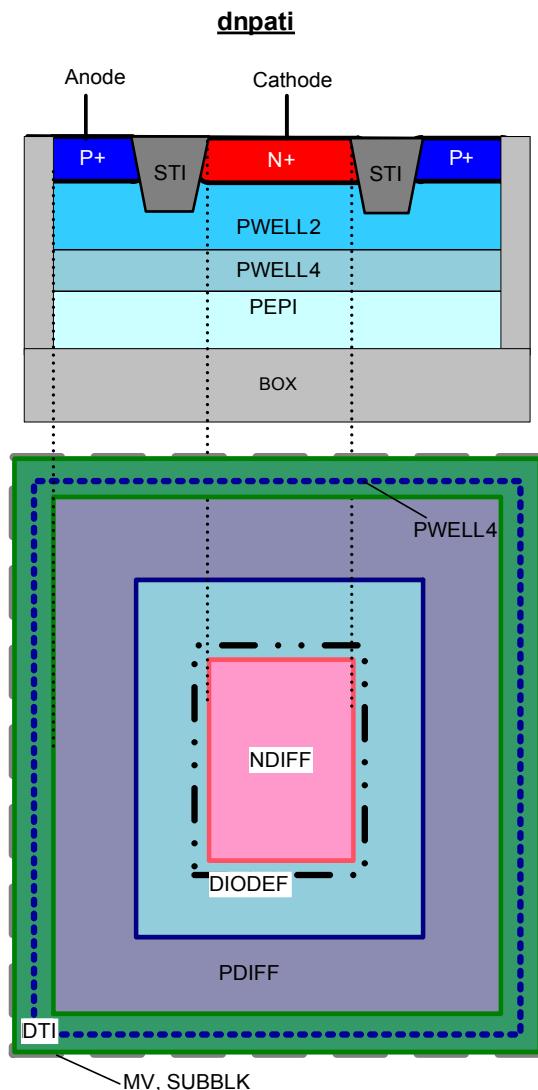
The layout of the dnpati protection diode is predefined and only the cathode width can be changed in the range of 2.0  $\mu\text{m}$  to 200.0  $\mu\text{m}$ . Fixed cathode length is 1.0  $\mu\text{m}$ .

**Note:** DTI ring is required for this device.

**Note:** dnpati device must be labeled "dnpati " using DIODEF (VERIFICATION).

**Note:** MV, PWELL4, SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.



**Figure 3.205** dnpati

3. Layer and Device rules → 3.30 NHVR module

## 3.30 NHVR module

### 3.30.1 Layer rules

#### DFN

Name	Description	Value	Unit
B1FN	DFN is only allowed for nhvr#, phvr#, ndhvr# or dfwdnh#	-	-
B2FN	DFN overlap of DNC, NDF, PDF, DFP, NDFMV, PDFMV or NZENER is not allowed	-	-
B3FN	DFN without PWBLK or NWELL is not allowed	-	-
B4FN	DFN without SUBBLK and MV is not allowed	-	-
W1FN	Minimum DFN width	1.5	μm
S1FN	Minimum DFN spacing / notch	1.5	μm
A1FN	Minimum DFN area	9.0	μm <sup>2</sup>

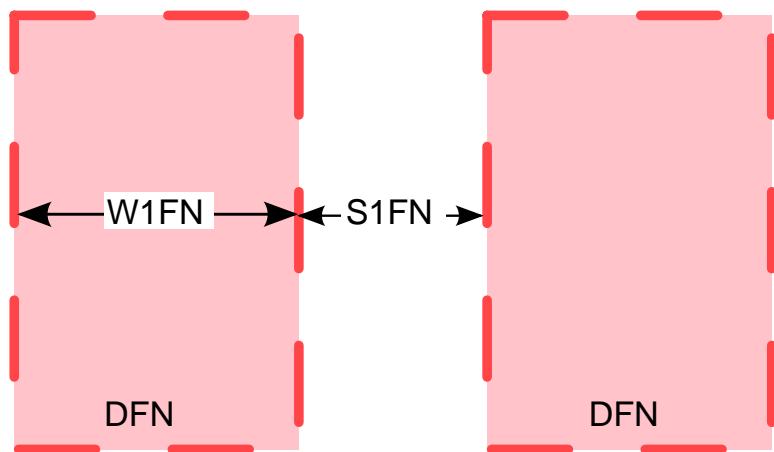


Figure 3.206 DFN

#### DFN\_E

Name	Description	Value	Unit
W2FN	Minimum DFN_E width	0.5	μm

3. Layer and Device rules → 3.30 NHVR module→ 3.30.1 Layer rules→ PDD

## PDD

Name	Description	Value	Unit
B1PF	PDD is only allowed for nhvr#, ndhvr# or dfwdnh#	-	-
B2PF	PDD without DFN or PWELL4 is not allowed	-	-
B3PF	PDD without MV and SUBBLK is not allowed	-	-
B4PF	PDD overlap of DPC or NWELL is not allowed	-	-
W1PF	Minimum PDD width	0.8	μm
S1PF	Minimum PDD spacing / notch	0.6	μm
A1PF	Minimum PDD area	0.8	μm <sup>2</sup>

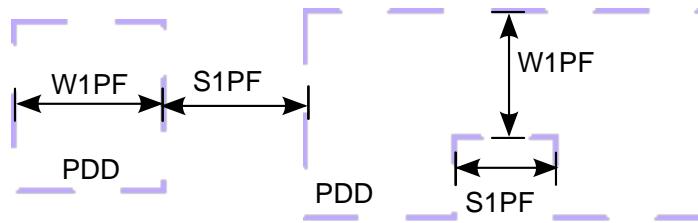


Figure 3.207 PDD

## PDD\_E

Name	Description	Value	Unit
W2PF	Minimum PDD_E width	0.3	μm

3. Layer and Device rules → 3.30 NHVR module → 3.30.1 Layer rules → PWELL4

### PWELL4

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1P4	PWELL4 is only allowed for nhv#, ndhv#, dfwdn#, dnpa, dnpati, nhvr#, ndhvr# or dfwdnh#	-	-
B2P4	PWELL4 overlap of NWELL, DPC, HVPWELL, SJNP or SJPN is not allowed	-	-
B4P4	PWELL4 without MV and SUBBLK is not allowed	-	-
W1P4	Minimum PWELL4 width	1.0	μm
S1P4	Minimum PWELL4 spacing/notch	1.0	μm
S1P4DN	Minimum PWELL4 spacing to NDIFF	0.25	μm
E1P4DN	Minimum PWELL4 enclosure of NDIFF	0.43	μm
E1P4DP	Minimum PWELL4 enclosure of PDIFF (except dfwdn#, dfwdnh#)	0.25	μm
A1P4	Minimum PWELL4 area	2.25	μm <sup>2</sup>

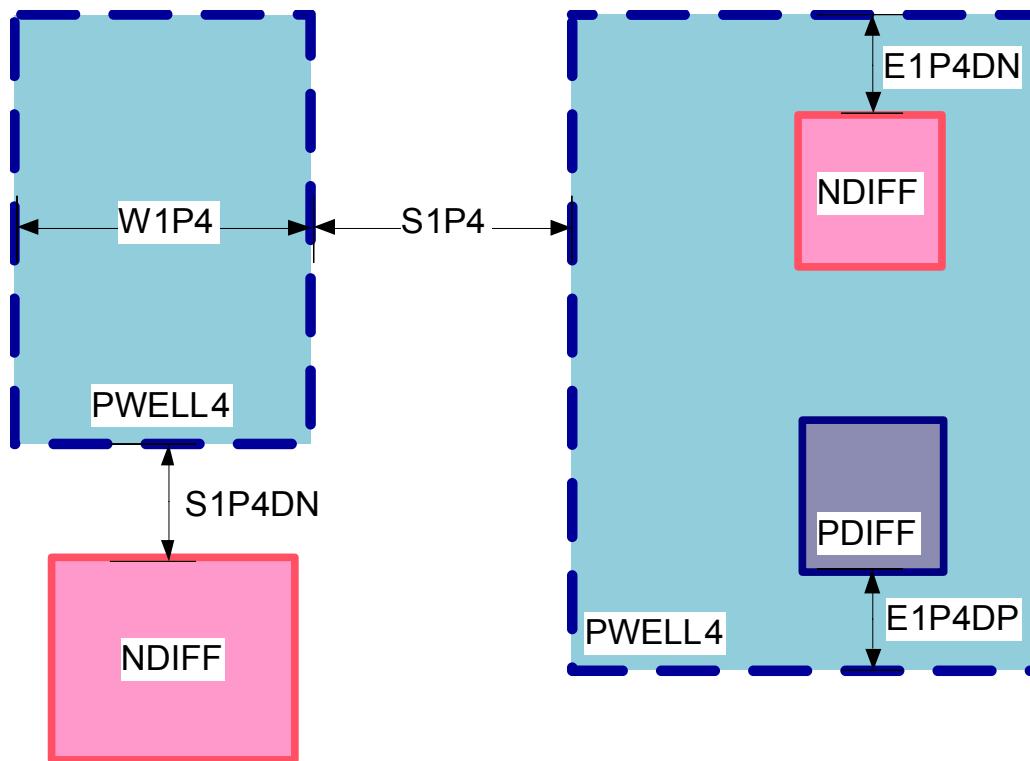


Figure 3.208 PWELL4

### 3.30.2 Device rules

#### nhvra

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W48GA	Minimum CHANNEL length <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.4	μm

## 3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ nhvra

Name	Description	Value	Unit
W57GA	Minimum GATE width	3.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W58GA	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
	Maximum CHANNEL length	25.0	µm
<b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.			
S16P1DN	Minimum POLY1 spacing to DRAIN NDIFF (in the direction of GATE length)	0.88	µm
S28DF	Fixed DRAIN-EDGE-STI length	1.4	µm
S8GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E2M2DN	Minimum MET2 enclosure of DRAIN NDIFF (in the direction of GATE width)	3.0	µm
E5M2DN	Fixed MET2 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	µm
E6M1DN	Minimum MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	µm
E9M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.2	µm
E12DNP1	Minimum NDIFF extension beyond POLY1	0.32	µm
E12P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.52	µm
E15P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1FNGA	Fixed DFN overlap of GATE	0.95	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** nhvra device must be labeled "nhvra" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

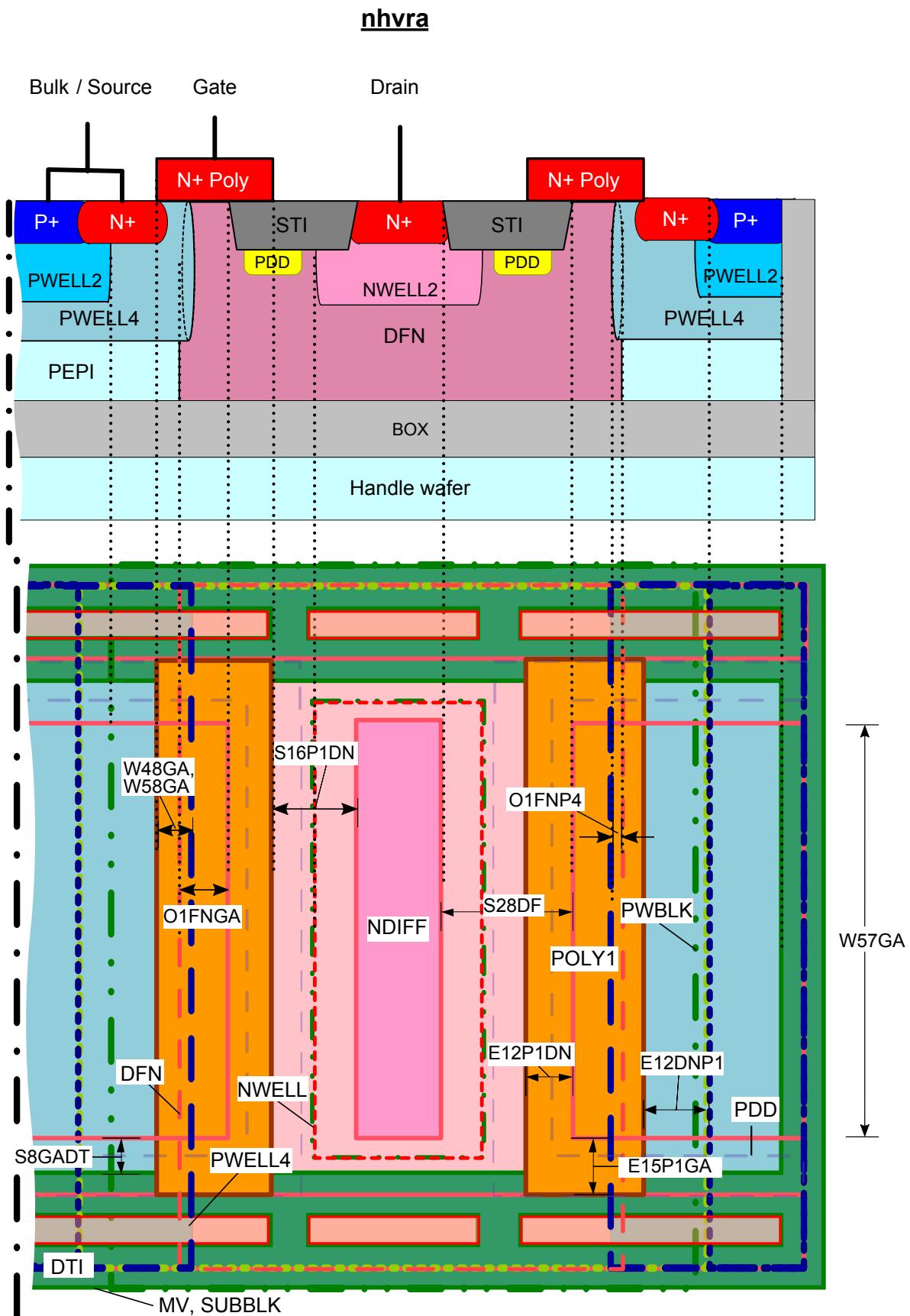
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → nhvra



**Figure 3.209 nhvra**

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ nhvrb

## **nhvrb**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W48GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.4	µm
W57GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	µm
W58GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	25.0	µm
S17P1DN	Minimum POLY1 spacing to DRAIN NDIFF (in the direction of GATE length)	1.98	µm
S29DF	Fixed DRAIN-EDGE-STI length	2.5	µm
S8GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E10M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.4	µm
E2M2DN	Minimum MET2 enclosure of DRAIN NDIFF (in the direction of GATE width)	3.0	µm
E5M2DN	Fixed MET2 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	µm
E6M1DN	Minimum MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	µm
E12DNP1	Minimum NDIFF extension beyond POLY1	0.32	µm
E13P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.52	µm
E15P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1FNGA	Fixed DFN overlap of GATE	0.95	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** nhvrb device must be labeled "nhvrb" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

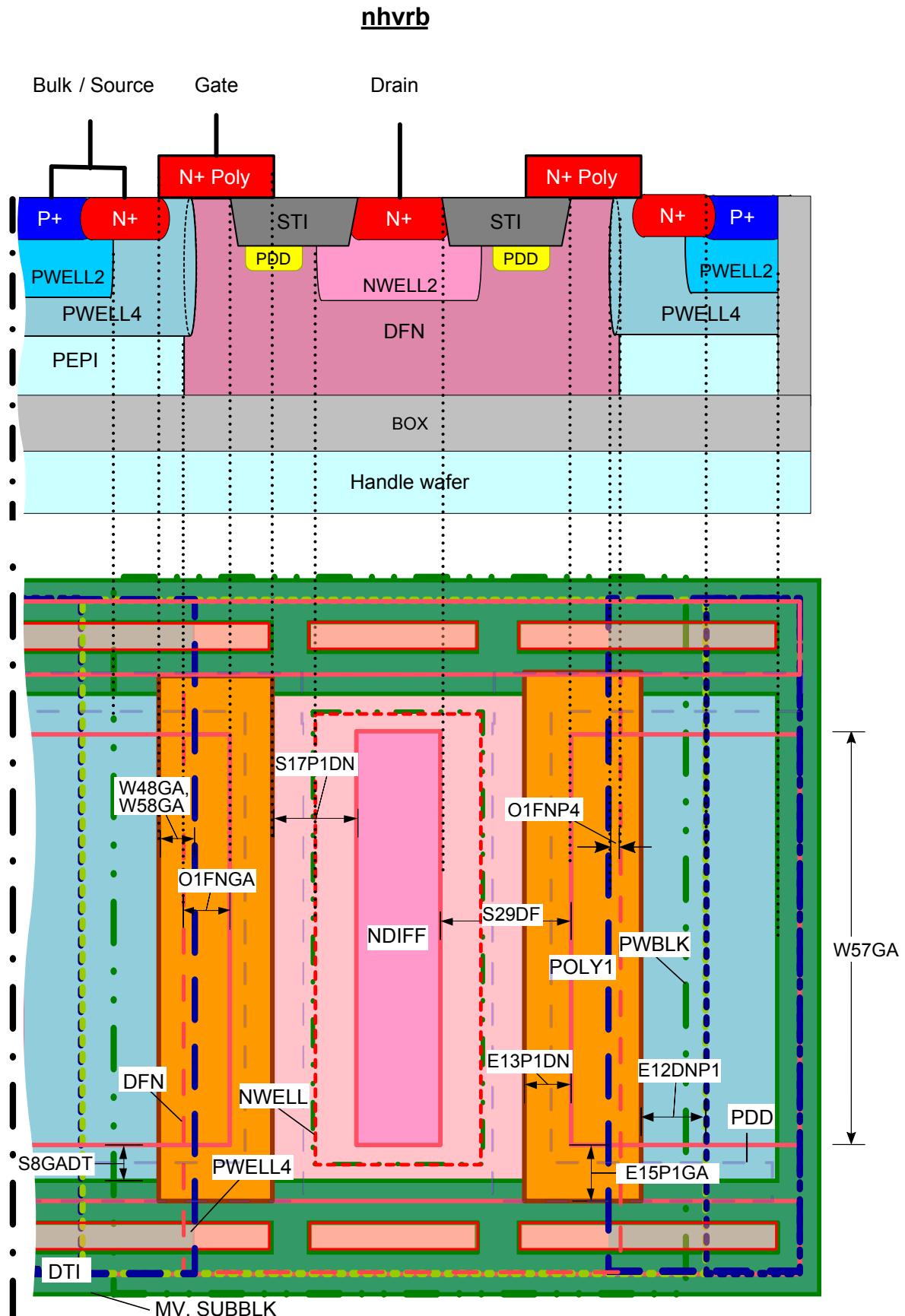
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → nhvrb



**Figure 3.210 nhvrb**

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ nhvrc

## nhvrc

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W48GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.4	µm
W57GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	µm
W58GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	25.0	µm
S18P1DN	Minimum POLY1 spacing to DRAIN NDIFF (in the direction of GATE length)	2.33	µm
S30DF	Fixed DRAIN-EDGE-STI length	3.0	µm
S8GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E11M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.5	µm
E2M2DN	Minimum MET2 enclosure of DRAIN NDIFF (in the direction of GATE width)	3.0	µm
E6M1DN	Minimum MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	µm
E6M2DN	Fixed MET2 enclosure of DRAIN NDIFF (in the direction of GATE length)	0.6	µm
E12DNP1	Minimum NDIFF extension beyond POLY1	0.32	µm
E14P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.67	µm
E15P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1FNGA	Fixed DFN overlap of GATE	0.95	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** nhvrc device must be labeled "nhvrc" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → nhvrc

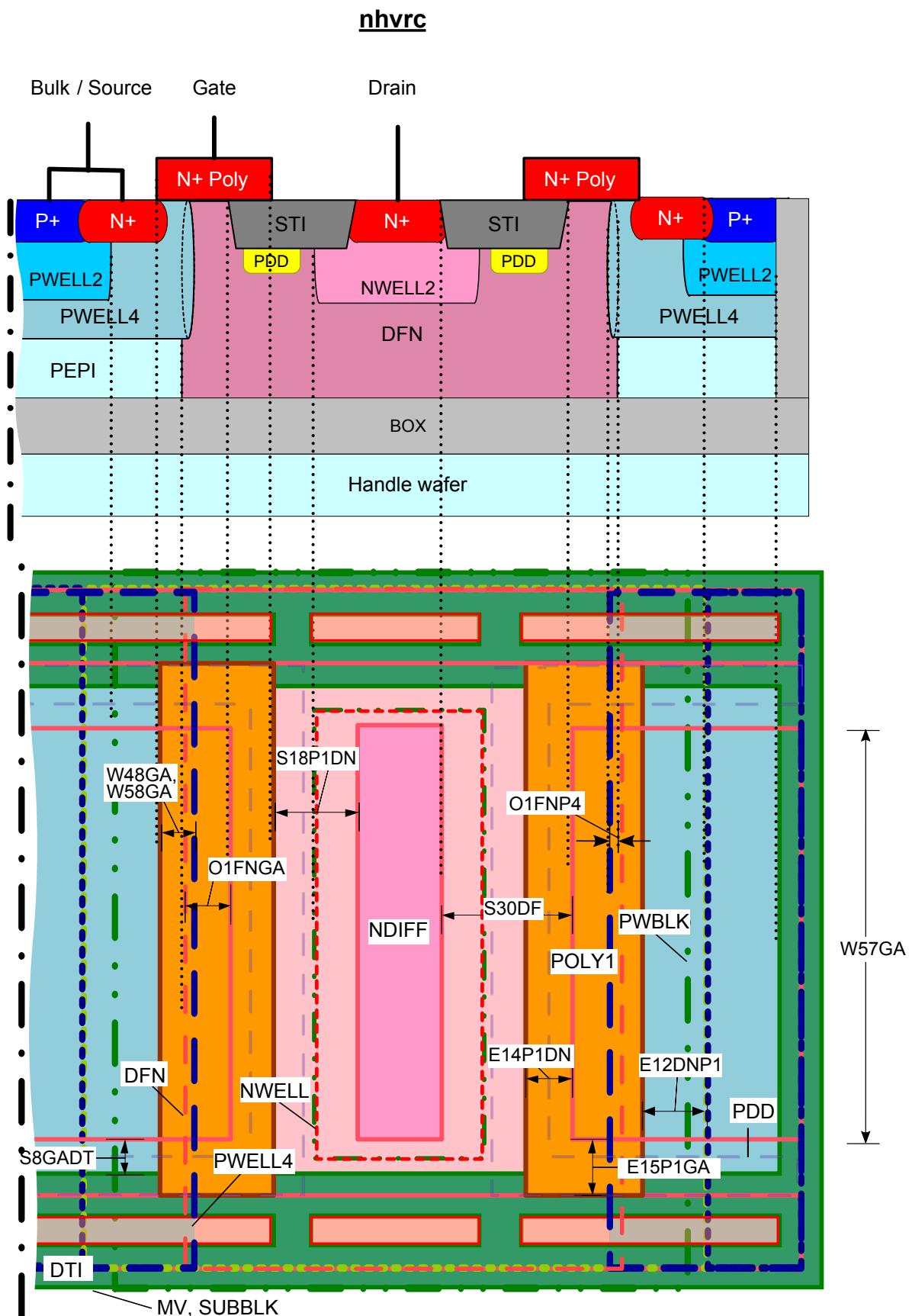


Figure 3.211 nhvrc

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ nhvrd

## **nhvrd**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W56GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.5	µm
W57GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	µm
W58GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	25.0	µm
S19P1DN	Minimum POLY1 spacing to DRAIN NDIFF (in the direction of GATE length)	3.04	µm
S31DF	Fixed DRAIN-EDGE-STI length	3.8	µm
S8GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E2M2DN	Minimum MET2 enclosure of DRAIN NDIFF (in the direction of GATE width)	3.0	µm
E4M2DN	Fixed MET2 enclosure of DRAIN NDIFF (in the direction of GATE length)	1.1	µm
E6M1DN	Minimum MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	µm
E8M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	1.0	µm
E12DNP1	Minimum NDIFF extension beyond POLY1	0.32	µm
E15P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.76	µm
E15P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1FNGA	Fixed DFN overlap of GATE	0.95	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** nhvrd device must be labeled "nhvrd" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

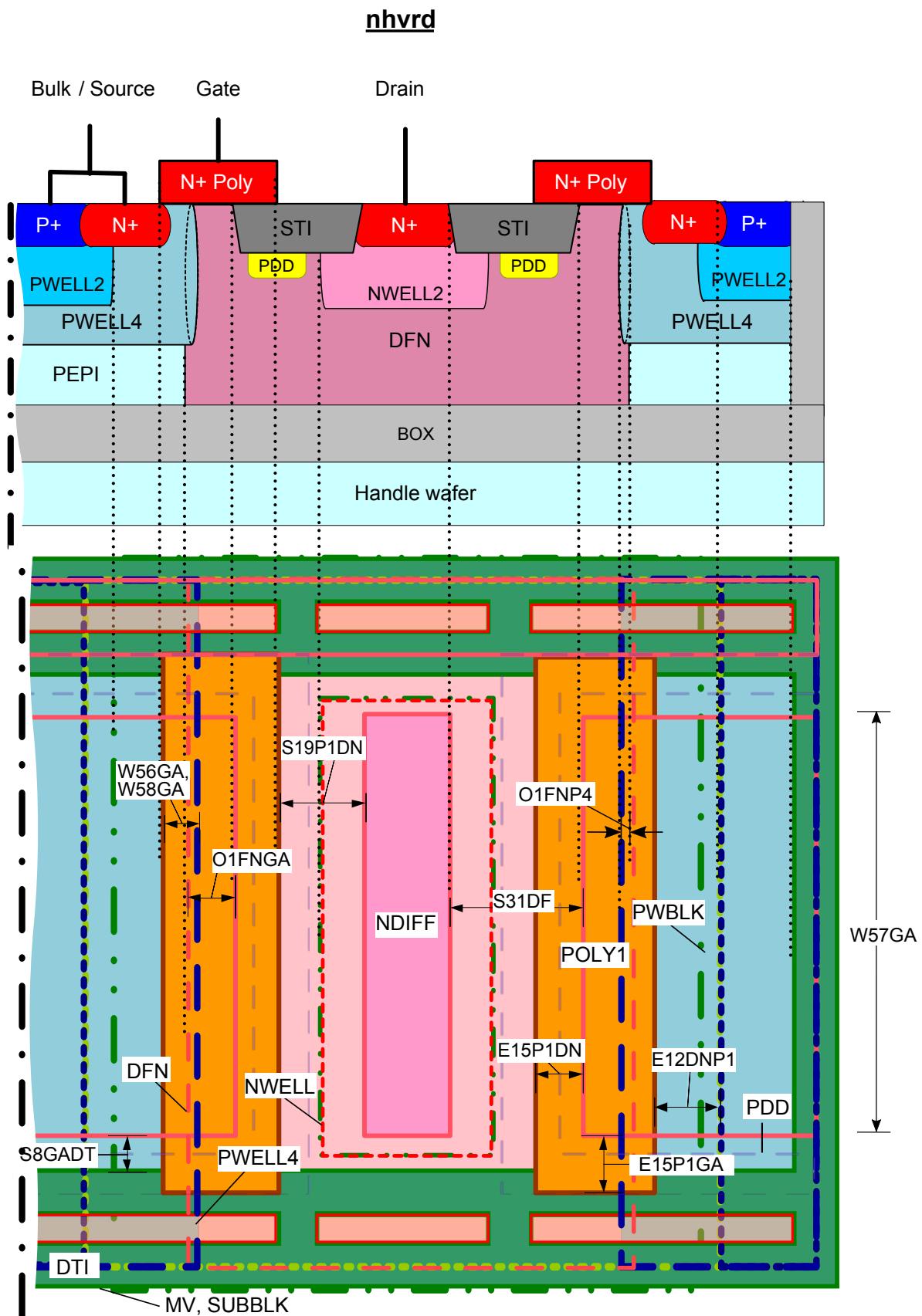
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → nhvrd



**Figure 3.212 nhvrd**

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ nhvre

## **nhvre**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W56GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.5	μm
W57GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	μm
W58GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	25.0	μm
S20P1DN	Minimum POLY1 spacing to DRAIN NDIFF (in the direction of GATE length)	4.25	μm
S32DF	Fixed DRAIN-EDGE-STI length	5.0	μm
S8GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
E1M2DN	Fixed MET2 enclosure of DRAIN NDIFF (in the direction of GATE length)	1.6	μm
E2M2DN	Minimum MET2 enclosure of DRAIN NDIFF (in the direction of GATE width)	3.0	μm
E5M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	1.5	μm
E6M1DN	Minimum MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	μm
E12DNP1	Minimum NDIFF extension beyond POLY1	0.32	μm
E15P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E16P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.75	μm
O1FNGA	Fixed DFN overlap of GATE	0.95	μm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	μm

**Note:** MV and SUBBLK are necessary for this device

**Note:** nhvre device must be labeled "nhvre" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

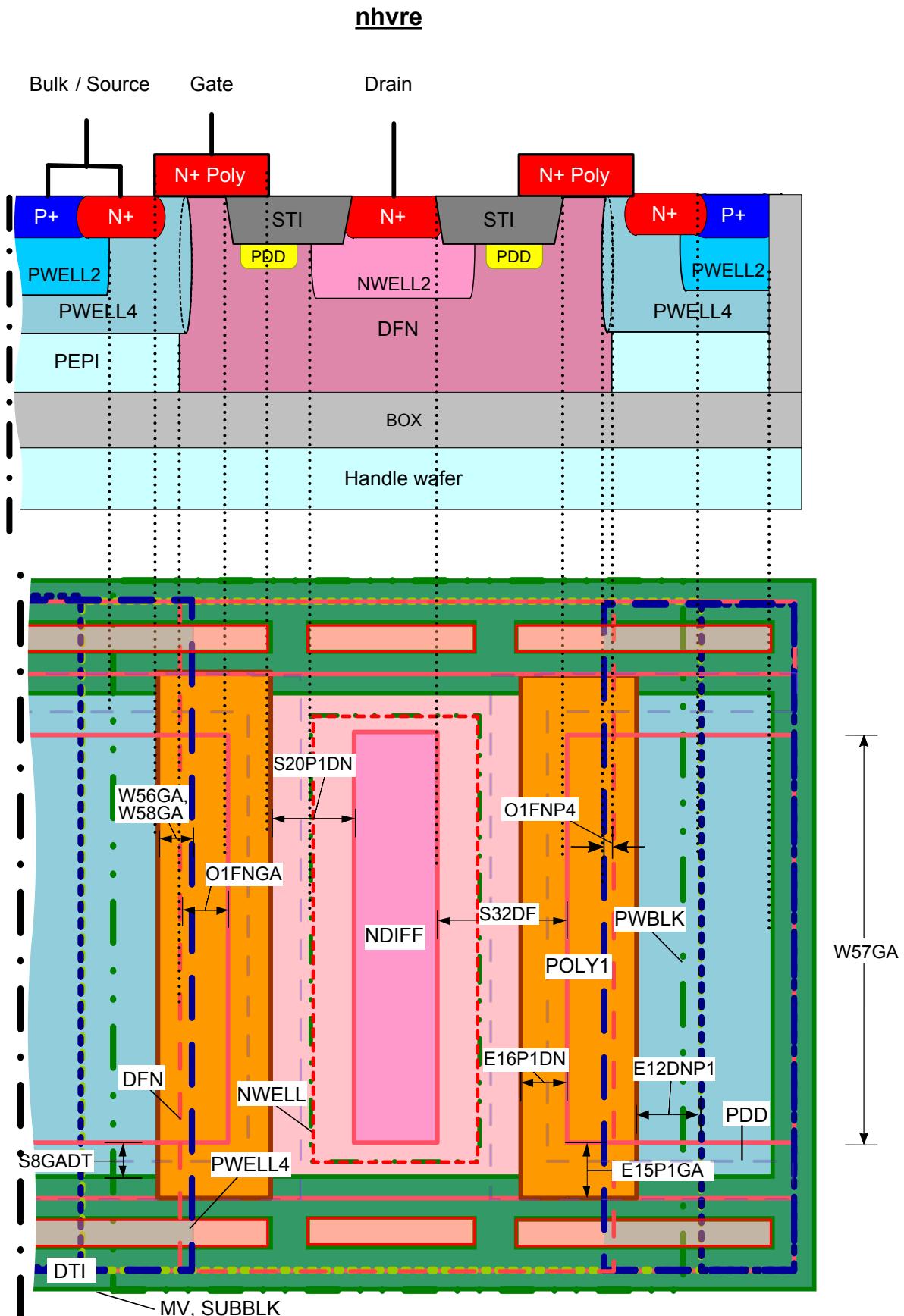
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → nhvre



**Figure 3.213 nhvre**

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ nhvrf

## nhvrf

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W56GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	0.5	μm
W57GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	μm
W58GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE AND PWELL4.	25.0	μm
S21P1DN	Minimum POLY1 spacing to DRAIN NDIFF (in the direction of GATE length)	5.95	μm
S33DF	Fixed DRAIN-EDGE-STI length	7.0	μm
S8GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
E2M2DN	Minimum MET2 enclosure of DRAIN NDIFF (in the direction of GATE width)	3.0	μm
E3M2DN	Fixed MET2 enclosure of DRAIN NDIFF (in the direction of GATE length)	2.1	μm
E6M1DN	Minimum MET1 enclosure of DRAIN NDIFF (in the direction of GATE width)	2.0	μm
E7M1DN	Fixed MET1 enclosure of DRAIN NDIFF (in the direction of GATE length)	2.0	μm
E12DNP1	Minimum NDIFF extension beyond POLY1	0.32	μm
E15P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E17P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	1.05	μm
O1FNGA	Fixed DFN overlap of GATE	0.95	μm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	μm

**Note:** MV and SUBBLK are necessary for this device

**Note:** nhvrf device must be labeled "nhvrf" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

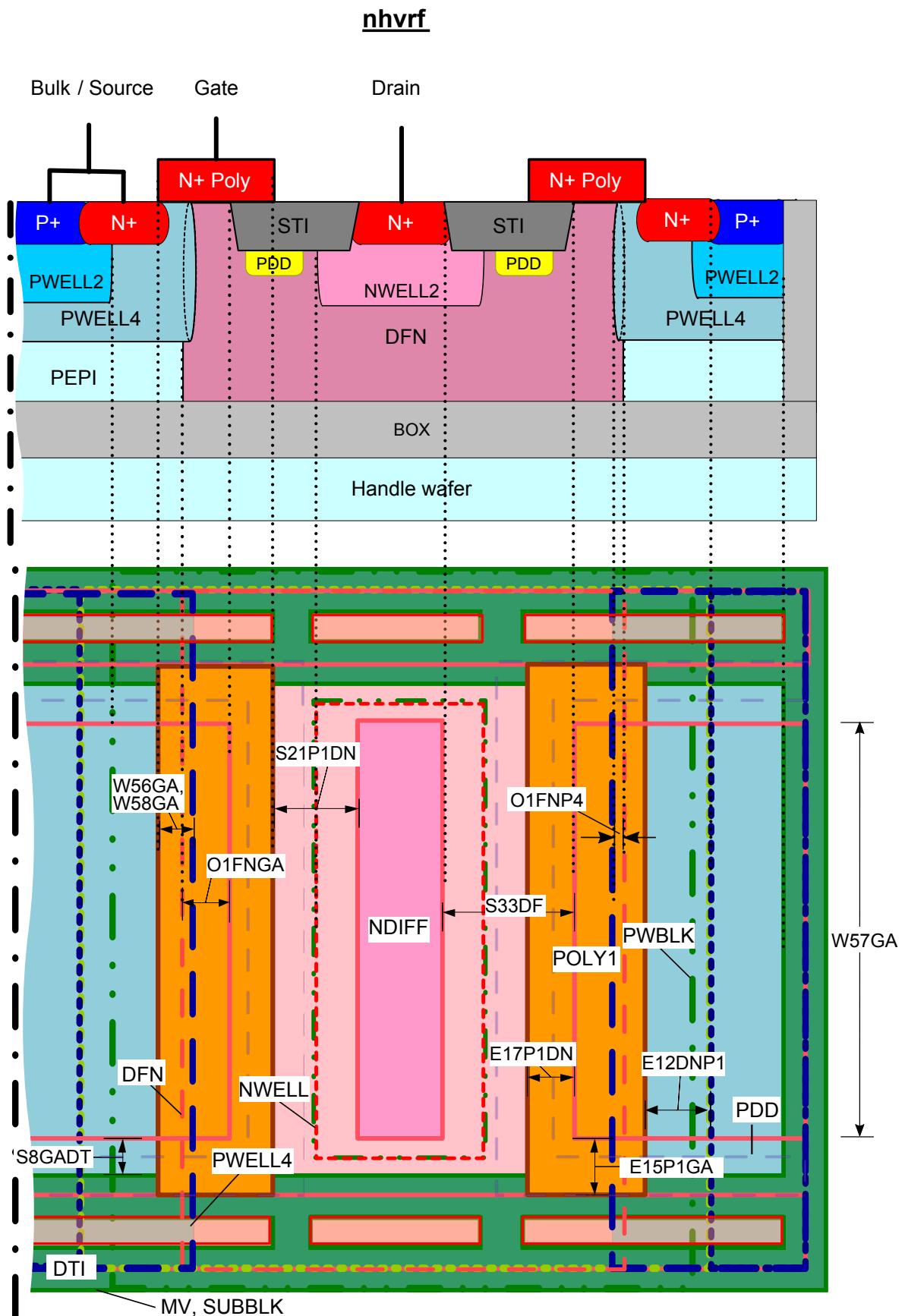
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → nhvrf



**Figure 3.214 nhvrf**

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ dfwdnhc

### **dfwdnhc**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
S24P1DN	Minimum POLY1 spacing to Cathode NDIFF (in the direction of device length)	2.33	µm
S41DF	Fixed CATHODE-EDGE-STI length	3.0	µm
E12M1DN	Fixed MET1 enclosure of Cathode NDIFF (in the direction of device length)	0.5	µm
E13M1DN	Minimum MET1 enclosure of Cathode NDIFF (in the direction of device width)	2.0	µm
E7M2DN	Fixed MET2 enclosure of Cathode NDIFF (in the direction of device length)	0.6	µm
E8M2DN	Minimum MET2 enclosure of Cathode NDIFF (in the direction of device width)	3.0	µm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	µm
E20P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	0.67	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm
O1P1DP	Minimum POLY1 overlap PDIFF	0.3	µm
O2FNGA	Fixed DFN overlap of GATE Anode	0.95	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** dfwdnhc device must be labeled "dfwdnhc" using DIODEF (VERIFICATION) layer over DFN inside the innermost DTI hole.

**Note:** Each diode must be surrounded by DTI ring

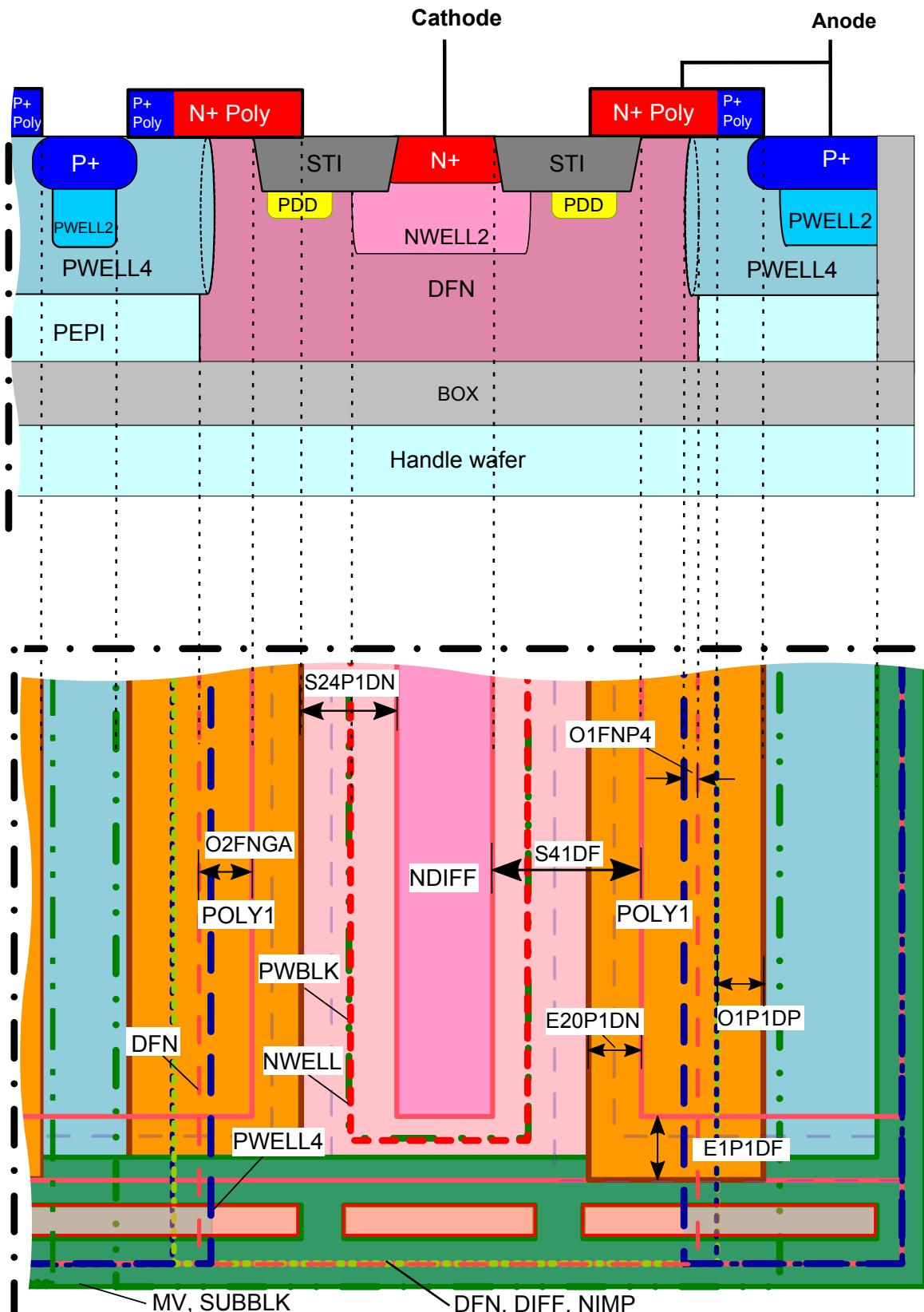
**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** Device finger width is defined as Cathode NDIFF width

**Note:** Minimum drawn finger width is 3 µm

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → dfwdnhc

### dfwdnhc



**Figure 3.215 dfwdnhc**

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ dfwdnhd

### **dfwdnhd**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
S25P1DN	Minimum POLY1 spacing to Cathode NDIFF (in the direction of device length)	3.04	µm
S42DF	Fixed CATHODE-EDGE-STI length	3.8	µm
E13M1DN	Minimum MET1 enclosure of Cathode NDIFF (in the direction of device width)	2.0	µm
E14M1DN	Fixed MET1 enclosure of Cathode NDIFF (in the direction of device length)	1.0	µm
E8M2DN	Minimum MET2 enclosure of Cathode NDIFF (in the direction of device width)	3.0	µm
E9M2DN	Fixed MET2 enclosure of Cathode NDIFF (in the direction of device length)	1.1	µm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	µm
E21P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	0.76	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm
O1P1DP	Minimum POLY1 overlap PDIFF	0.3	µm
O2FNGA	Fixed DFN overlap of GATE Anode	0.95	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** dfwdnhd device must be labeled "dfwdnhd" using DIODEF (VERIFICATION) layer over DFN inside the innermost DTI hole.

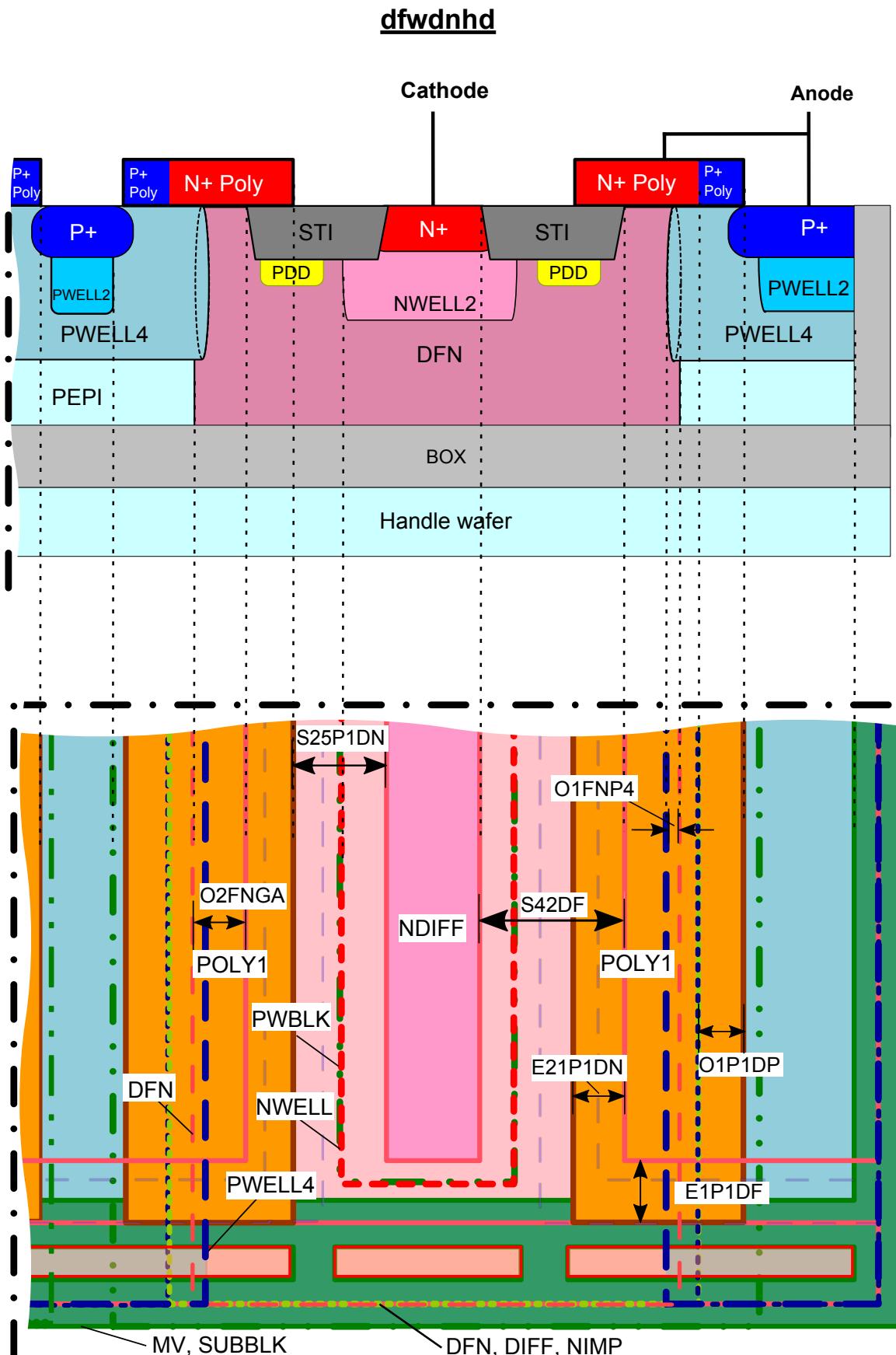
**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** Device finger width is defined as Cathode NDIFF width

**Note:** Minimum drawn finger width is 3 µm

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → dfwdnhd



**Figure 3.216** dfwdnhd

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ dfwdnhe

### **dfwdnhe**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
S26P1DN	Minimum POLY1 spacing to Cathode NDIFF (in the direction of device length)	4.25	µm
S43DF	Fixed CATHODE-EDGE-STI length	5.0	µm
E10M2DN	Fixed MET2 enclosure of Cathode NDIFF (in the direction of device length)	1.6	µm
E13M1DN	Minimum MET1 enclosure of Cathode NDIFF (in the direction of device width)	2.0	µm
E15M1DN	Fixed MET1 enclosure of Cathode NDIFF (in the direction of device length)	1.5	µm
E8M2DN	Minimum MET2 enclosure of Cathode NDIFF (in the direction of device width)	3.0	µm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	µm
E22P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	0.75	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm
O1P1DP	Minimum POLY1 overlap PDIFF	0.3	µm
O2FNGA	Fixed DFN overlap of GATE Anode	0.95	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** dfwdnhe device must be labeled "dfwdnhe" using DIODEF (VERIFICATION) layer over DFN inside the innermost DTI hole.

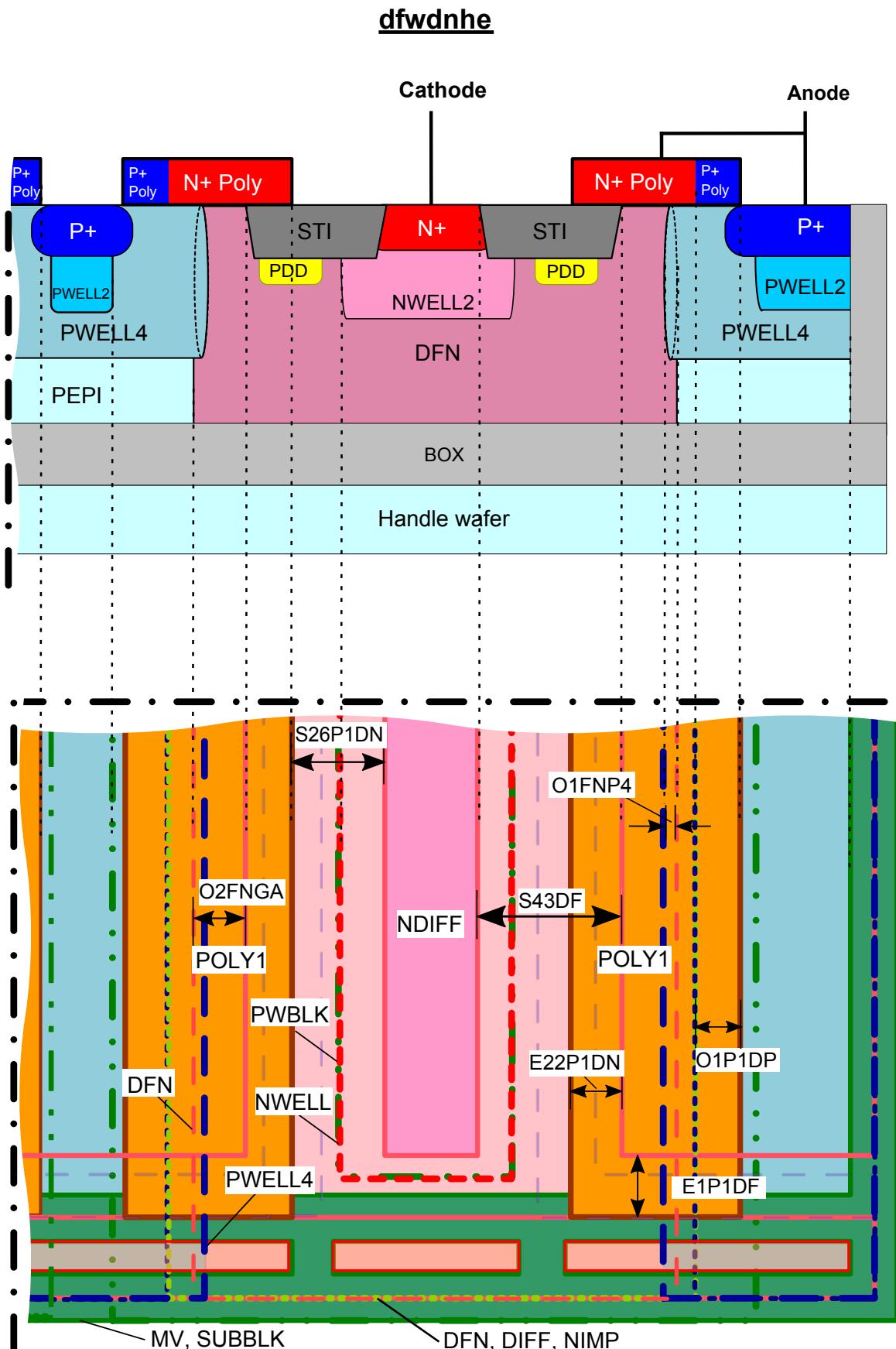
**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** Device finger width is defined as Cathode NDIFF width

**Note:** Minimum drawn finger width is 3 µm

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → dfwdnhe



**Figure 3.217 dfwdnhe**

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ dfwdnhf

### **dfwdnhf**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
S27P1DN	Minimum POLY1 spacing to Cathode NDIFF (in the direction of device length)	5.95	µm
S44DF	Fixed CATHODE-EDGE-STI length	7.0	µm
E11M2DN	Fixed MET2 enclosure of Cathode NDIFF (in the direction of device length)	2.1	µm
E13M1DN	Minimum MET1 enclosure of Cathode NDIFF (in the direction of device width)	2.0	µm
E16M1DN	Fixed MET1 enclosure of Cathode NDIFF (in the direction of device length)	2.0	µm
E8M2DN	Minimum MET2 enclosure of Cathode NDIFF (in the direction of device width)	3.0	µm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	µm
E23P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	1.05	µm
O1FNP4	Fixed DFN overlap of PWELL4	0.1	µm
O1P1DP	Minimum POLY1 overlap PDIFF	0.3	µm
O2FNGA	Fixed DFN overlap of GATE Anode	0.95	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** dfwdnhf device must be labeled "dfwdnhf" using DIODEF (VERIFICATION) layer over DFN inside the innermost DTI hole.

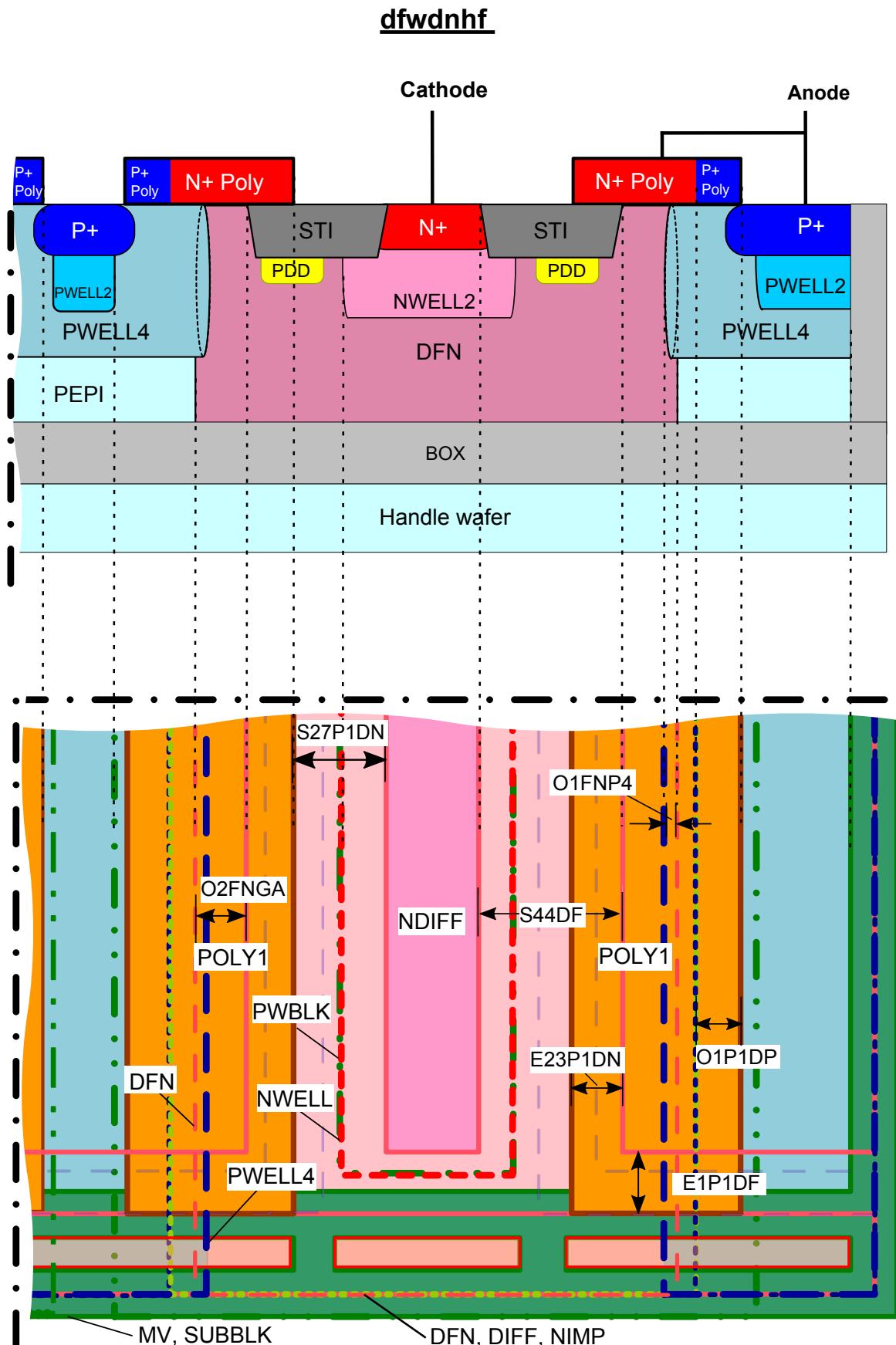
**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** Device finger width is defined as Cathode NDIFF width

**Note:** Minimum drawn finger width is 3 µm

3. Layer and Device rules → 3.30 NHVR module → 3.30.2 Device rules → dfwdnhf



**Figure 3.218 dfwdnhf**

3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ dnpa

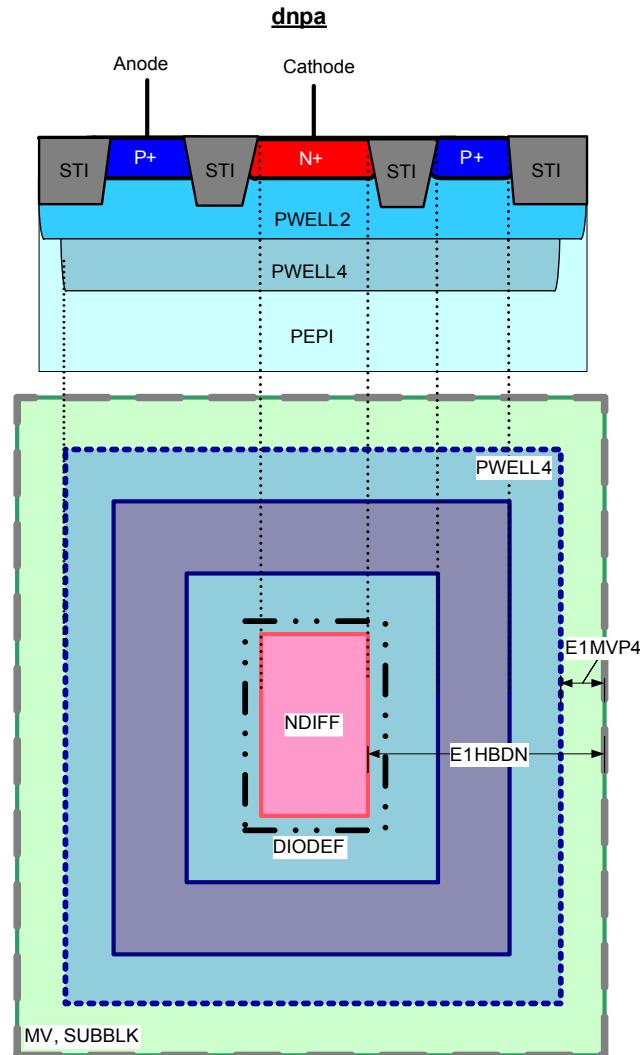
### **dnpa**

The layout of the dnpa protection diode is predefined and only the cathode width can be changed in the range of 2.0  $\mu\text{m}$  to 200.0  $\mu\text{m}$ . Fixed cathode length is 1.0  $\mu\text{m}$ .

Name	Description	Value	Unit
E1HBDN	Minimum SUBBLK enclosure of NDIFF	1.68	$\mu\text{m}$
E1MVP4	Minimum MV enclosure of PWELL4	0.5	$\mu\text{m}$

**Note:** A DTI ring is necessary, valid if Vanode is higher than the handle wafer voltage.

**Note:** MV, PWELL4, SUBBLK are necessary for this device



**Figure 3.219 dnpa**

## 3. Layer and Device rules → 3.30 NHVR module→ 3.30.2 Device rules→ dnpati

**dnpati**

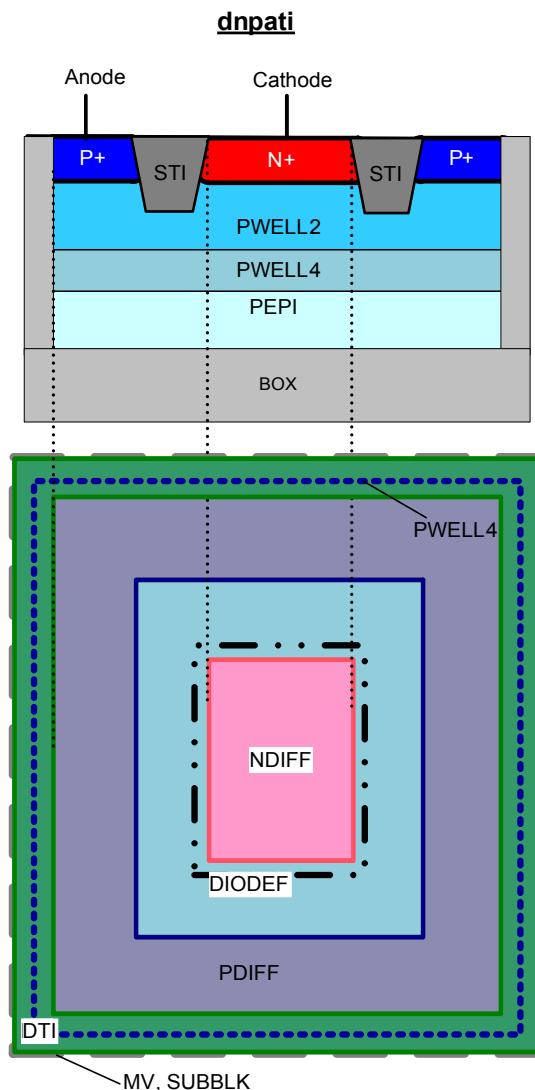
The layout of the dnpati protection diode is predefined and only the cathode width can be changed in the range of 2.0  $\mu\text{m}$  to 200.0  $\mu\text{m}$ . Fixed cathode length is 1.0  $\mu\text{m}$ .

**Note:** DTI ring is required for this device.

**Note:** dnpati device must be labeled "dnpati " using DIODEF (VERIFICATION).

**Note:** MV, PWELL4, SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.



**Figure 3.220** dnpati

3. Layer and Device rules → 3.31 NMV module

## 3.31 NMV module

### 3.31.1 Layer rules

#### ESDMV

Name	Description	Value	Unit
B1ES	ESDMV is only allowed for nmv#, ndmv#, dfwd#	-	-
B2ES	ESDMV overlap of NWELL, PWBLK, SUBBLK, DPC, PWELL4, NDF or PDF is not allowed	-	-
B3ES	ESDMV without MV is not allowed	-	-
W1ES	Minimum ESDMV width	0.6	μm
S1ES	Minimum ESDMV spacing / notch	0.6	μm
A1ES	Minimum ESDMV area	0.8	μm <sup>2</sup>

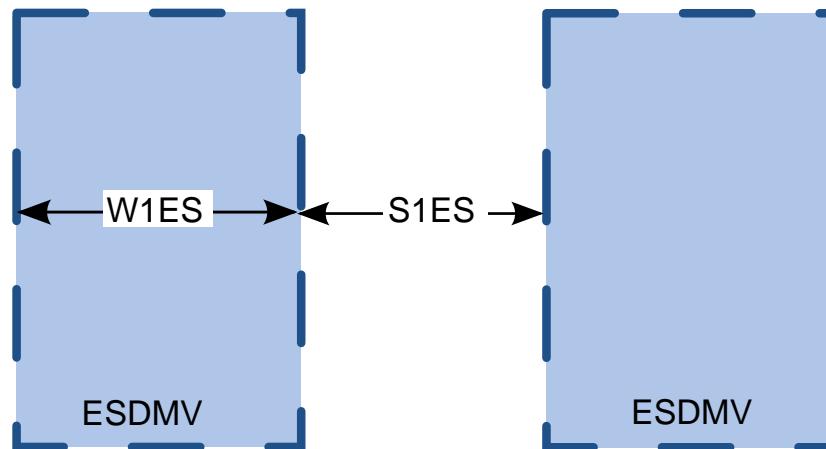


Figure 3.221 ESDMV

#### ESDMV\_E

Name	Description	Value	Unit
W2ES	Minimum ESDMV_E width	0.5	μm

3. Layer and Device rules → 3.31 NMV module → 3.31.1 Layer rules → NDFMV

## NDFMV

Name	Description	Value	Unit
B1ND	NDFMV is only allowed for nmv#, ndmv#, dfwd#	-	-
B2ND	NDFMV overlap of NDF, PDF or PDFMV is not allowed	-	-
B3ND	NDFMV overlap of SUBBLK is not allowed	-	-
B4ND	NDFMV without PWBLK or NWELL is not allowed	-	-
B5ND	NDFMV without MV is not allowed	-	-
W1ND	Minimum NDFMV width	1.0	μm
S1ND	Minimum NDFMV spacing / notch	1.0	μm
A1ND	Minimum NDFMV area	2.25	μm <sup>2</sup>

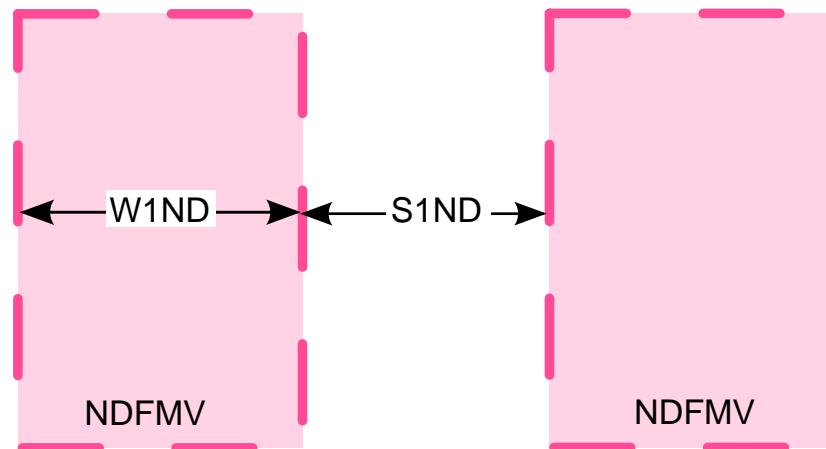


Figure 3.222 NDFMV

## NDFMV\_E

Name	Description	Value	Unit
W2ND	Minimum NDFMV_E width	0.5	μm

### 3.31.2 Device rules

#### nmvb

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W32GA	Minimum CHANNEL length	0.4	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
W33GA	<b>Note:</b> Number of GATE fingers is 2 for CHANNEL length $\geq 5\mu\text{m}$		
	Minimum GATE width	3.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
W36GA	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
W36GA	Maximum CHANNEL length	25.0	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		

⇒

## 3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ nmvb

Name	Description	Value	Unit
W5IP	Minimum PIMP width	0.42	µm
S4IN	Minimum NIMP spacing / notch	0.42	µm
S11P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.1	µm
S18DF	Fixed DRAIN-EDGE-STI length	0.32	µm
S6GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
S1ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.18	µm
	<b>Note:</b> Valid for CHANNEL length < 5µm		
S2ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.28	µm
	<b>Note:</b> Valid for CHANNEL length ≥ 5µm		
E13P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E5DNP1	Minimum NDIFF extension beyond POLY1	0.27	µm
E7P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.22	µm
O1NDGA	Fixed NDFMV overlap of GATE	0.45	µm

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

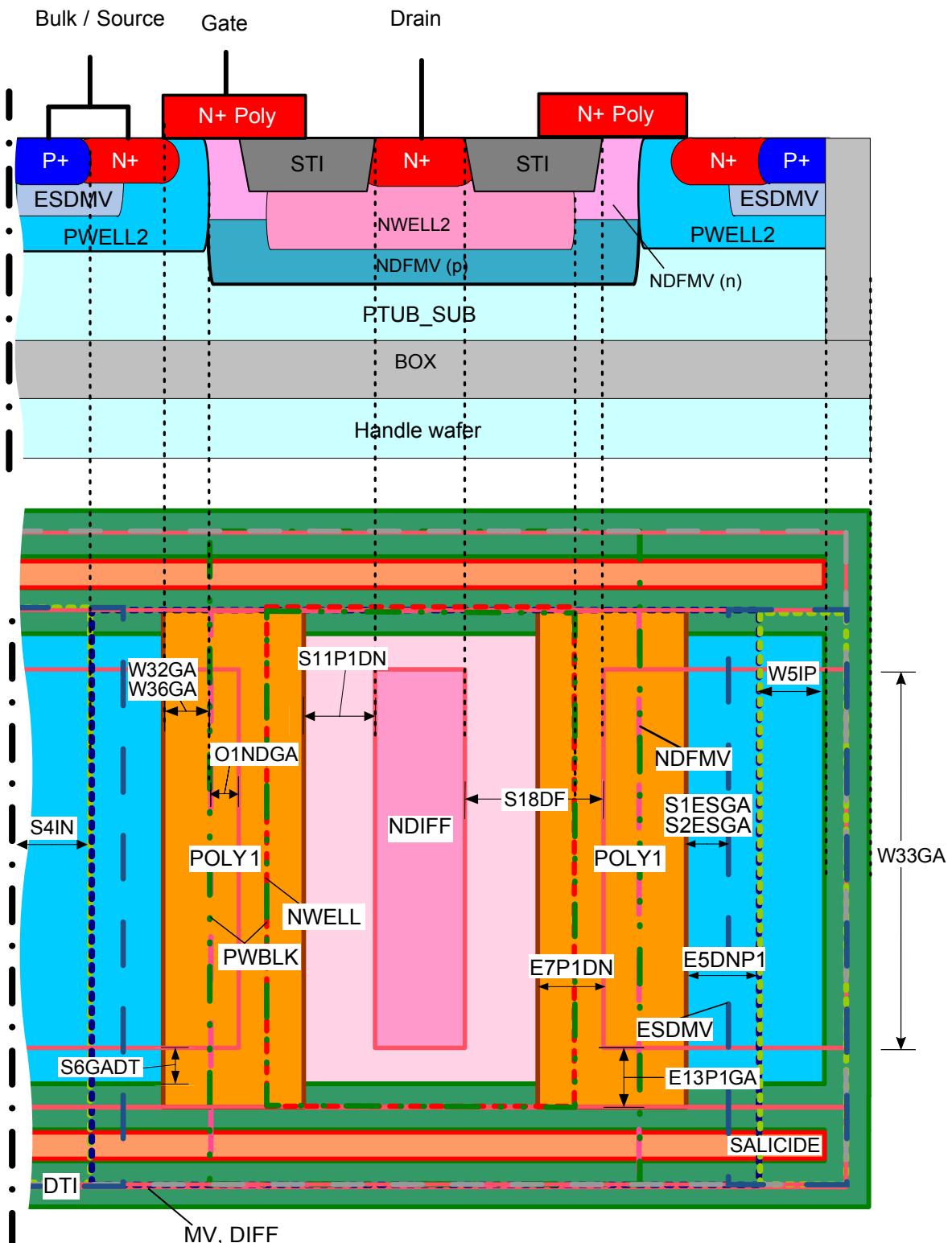
**Note:** nmvb device must be labeled "nmvb" using POLY1 (VERIFICATION) layer over GATE

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.31 NMV module → 3.31.2 Device rules→ nmvb

### nmvb



**Figure 3.223 nmvb**

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ nmvc

### **nmvc**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W32GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.  <b>Note:</b> Number of GATE fingers is 2 for CHANNEL length $\geq 5\mu\text{m}$	0.4	$\mu\text{m}$
	Minimum GATE width	3.0	$\mu\text{m}$
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
W36GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.	25.0	$\mu\text{m}$
	Minimum PIMP width	0.42	$\mu\text{m}$
S4IN	Minimum NIMP spacing / notch	0.42	$\mu\text{m}$
S12P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.1	$\mu\text{m}$
S19DF	Fixed DRAIN-EDGE-STI length	0.42	$\mu\text{m}$
S6GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	$\mu\text{m}$
S1ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)  <b>Note:</b> Valid for CHANNEL length $< 5\mu\text{m}$	0.18	$\mu\text{m}$
	Fixed ESDMV spacing to GATE (in the direction of GATE length)  <b>Note:</b> Valid for CHANNEL length $\geq 5\mu\text{m}$	0.28	$\mu\text{m}$
E13P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	$\mu\text{m}$
E5DNP1	Minimum NDIFF extension beyond POLY1	0.27	$\mu\text{m}$
E8P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.32	$\mu\text{m}$
O1NDGA	Fixed NDFMV overlap of GATE	0.45	$\mu\text{m}$

**Note:** MV is necessary for nmvc

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

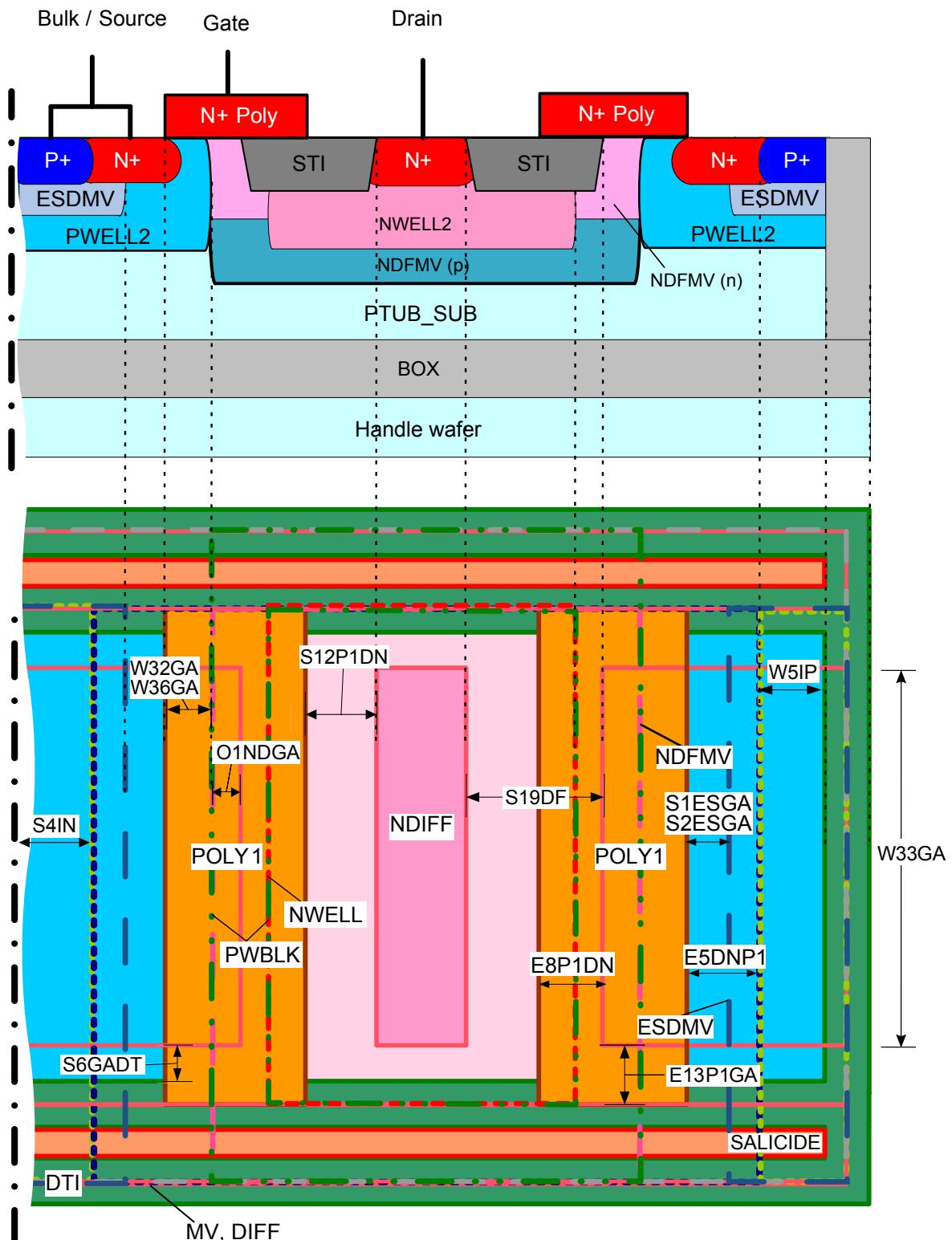
**Note:** nmvc device must be labeled "nmvc" using POLY1 (VERIFICATION) layer over GATE

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.31 NMV module → 3.31.2 Device rules → nmvc

### nmvc



**Figure 3.224 nmvc**

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ nmvd

## nmvd

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W32GA	Minimum CHANNEL length	0.4	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
	<b>Note:</b> Number of GATE fingers is 2 for CHANNEL length $\geq 5\mu\text{m}$		
W33GA	Minimum GATE width	3.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W36GA	Minimum GATE width is defined as minimum GATE finger width.		
	Maximum CHANNEL length	25.0	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
W5IP	Minimum PIMP width	0.42	μm
S4IN	Minimum NIMP spacing / notch	0.42	μm
S13P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.15	μm
S20DF	Fixed DRAIN-EDGE-STI length	0.45	μm
S6GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S1ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.18	μm
	<b>Note:</b> Valid for CHANNEL length $< 5\mu\text{m}$		
S2ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.28	μm
	<b>Note:</b> Valid for CHANNEL length $\geq 5\mu\text{m}$		
E13P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E5DNP1	Minimum NDIFF extension beyond POLY1	0.27	μm
E9P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.3	μm
O1NDGA	Fixed NDFMV overlap of GATE	0.45	μm

**Note:** MV is necessary for nmvd

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

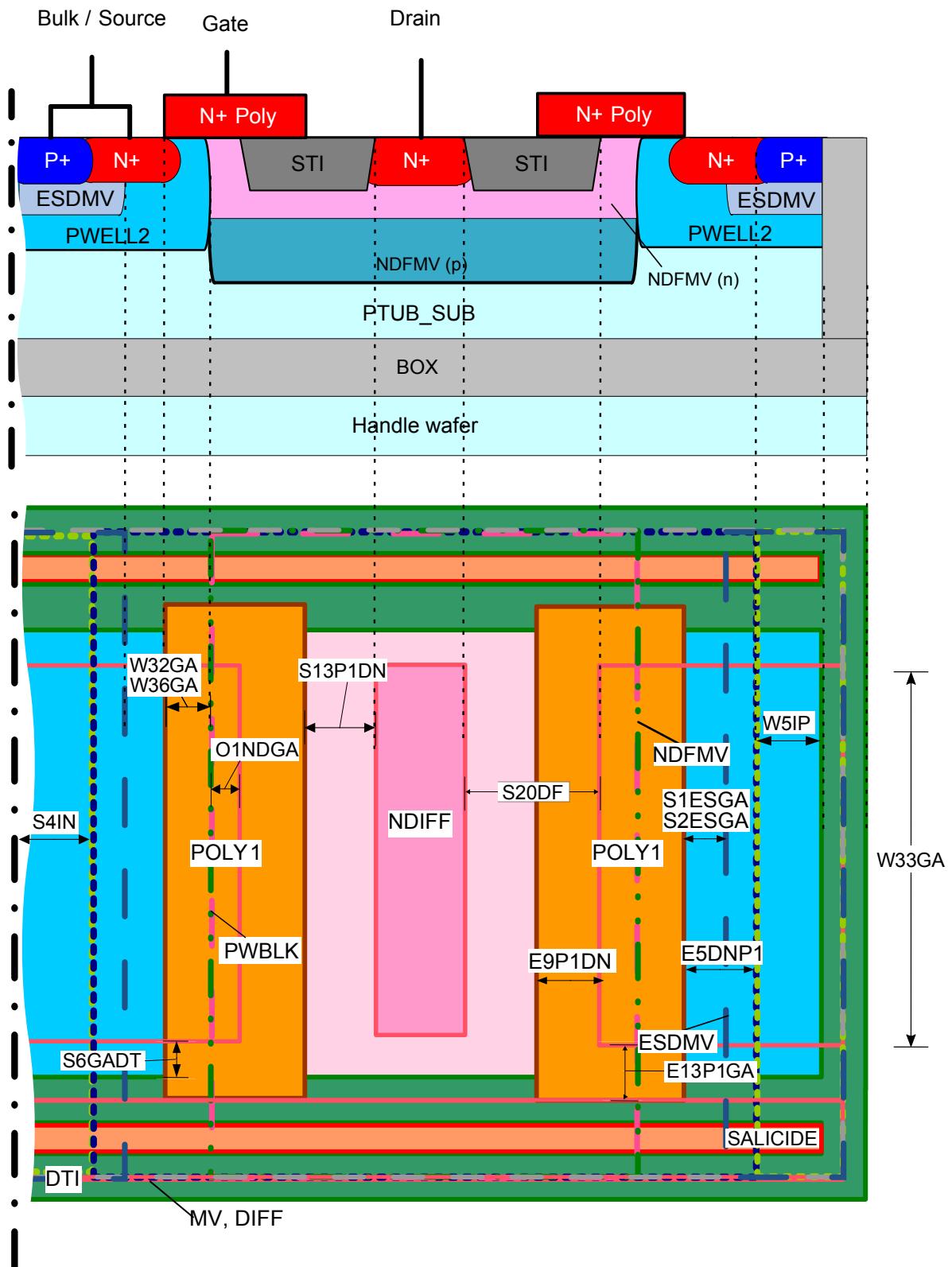
**Note:** nmvd device must be labeled "nmvd" using POLY1 (VERIFICATION) layer over GATE

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ nmvd

### nmvd



**Figure 3.225 nmvd**

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ nmve

## nmve

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W32GA	Minimum CHANNEL length	0.4	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
	<b>Note:</b> Number of GATE fingers is 2 for CHANNEL length $\geq$ 5μm		
W33GA	Minimum GATE width	3.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W36GA	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
	Maximum CHANNEL length	25.0	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
W5IP	Minimum PIMP width	0.42	μm
S4IN	Minimum NIMP spacing / notch	0.42	μm
S14P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.15	μm
S21DF	Fixed DRAIN-EDGE-STI length	0.7	μm
S6GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S1ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.18	μm
	<b>Note:</b> Valid for CHANNEL length < 5μm		
S2ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.28	μm
	<b>Note:</b> Valid for CHANNEL length $\geq$ 5μm		
E10P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.55	μm
E13P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E5DNP1	Minimum NDIFF extension beyond POLY1	0.27	μm
O1NDGA	Fixed NDFMV overlap of GATE	0.45	μm

**Note:** MV is necessary for nmve

**Note:** Each transistor must be surrounded by DTI ring.

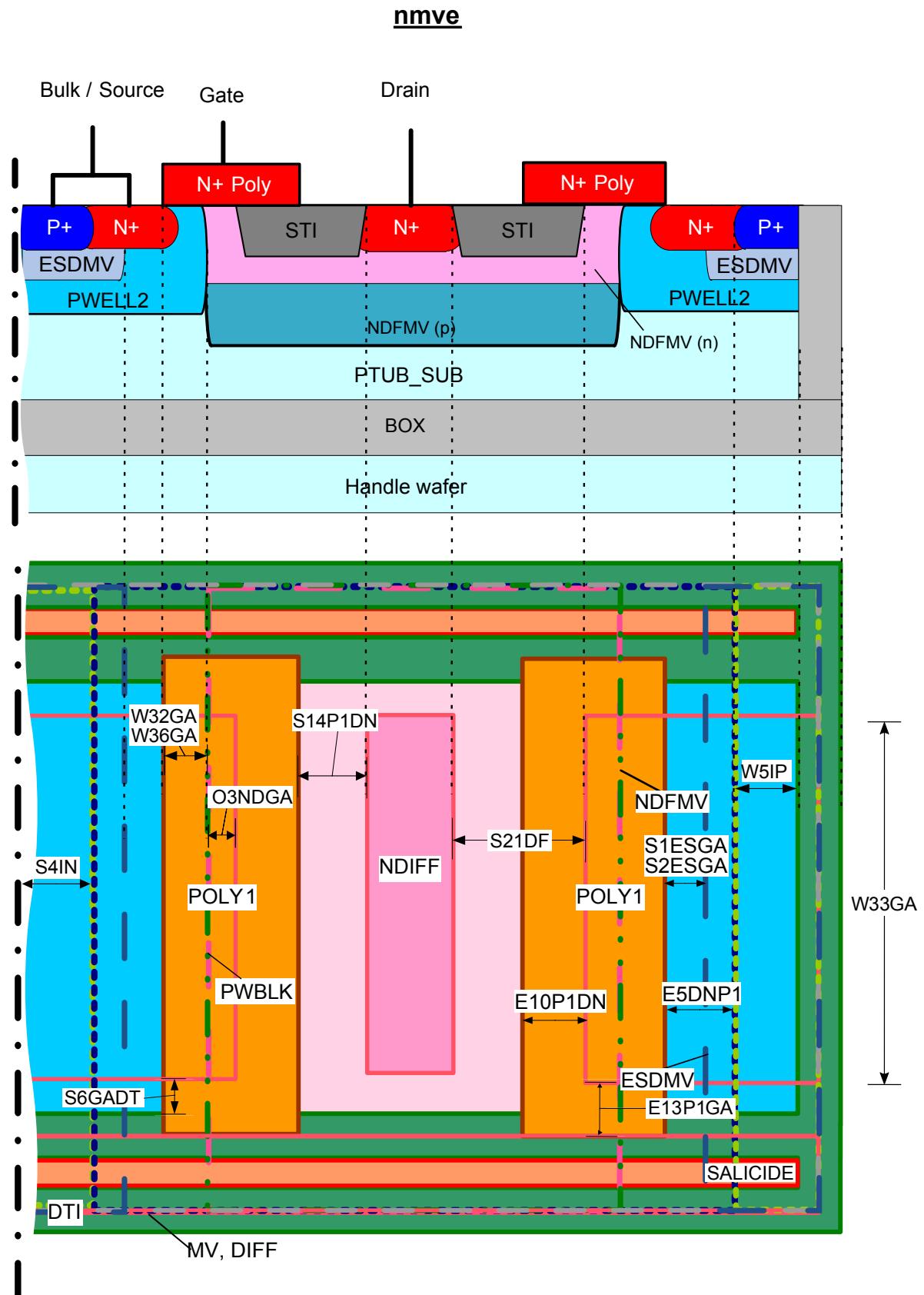
**Note:** nmve device must be labeled "nmve" using POLY1 (VERIFICATION) layer over GATE

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.31 NMV module → 3.31.2 Device rules→ nmve



**Figure 3.226 nmve**

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ nmvf

## nmvf

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W32GA	Minimum CHANNEL length	0.4	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
	<b>Note:</b> Number of GATE fingers is 2 for CHANNEL length $\geq 5\mu\text{m}$		
W33GA	Minimum GATE width	3.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W36GA	Minimum GATE width is defined as minimum GATE finger width.		
	Maximum CHANNEL length	25.0	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not NDFMV.		
W5IP	Minimum PIMP width	0.42	μm
S4IN	Minimum NIMP spacing / notch	0.42	μm
S15P1DN	Minimum POLY1 spacing to DRAIN NDIFF	0.5	μm
S22DF	Fixed DRAIN-EDGE-STI length	1.27	μm
S6GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S1ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.18	μm
	<b>Note:</b> Valid for CHANNEL length $< 5\mu\text{m}$		
S2ESGA	Fixed ESDMV spacing to GATE (in the direction of GATE length)	0.28	μm
	<b>Note:</b> Valid for CHANNEL length $\geq 5\mu\text{m}$		
E11P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of GATE length)	0.77	μm
E13P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E5DNP1	Minimum NDIFF extension beyond POLY1	0.27	μm
O1NDGA	Fixed NDFMV overlap of GATE	0.45	μm

**Note:** MV is necessary for nmvf

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

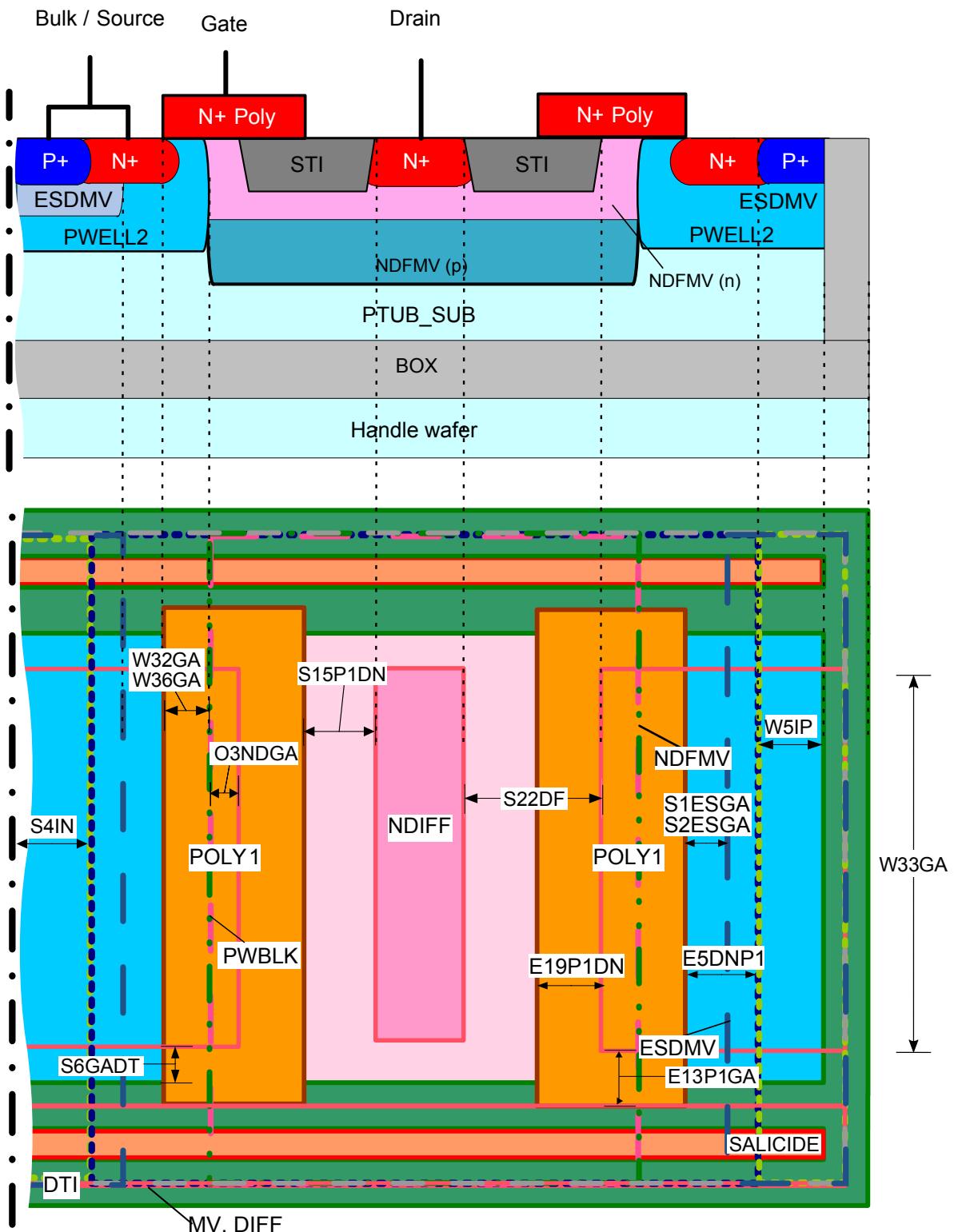
**Note:** nmvf device must be labeled "nmvf" using POLY1 (VERIFICATION) layer over GATE

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.31 NMV module → 3.31.2 Device rules → nmvf

### nmvf



**Figure 3.227 nmvf**

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ dfwdnb

### **dfwdnb**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
S28P1DN	Minimum POLY1 spacing to Cathode NDIFF (in the direction of device length)	0.1	µm
S46DF	Fixed CATHODE-EDGE-STI length	0.32	µm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	µm
E24P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	0.22	µm
O2NDGA	Fixed NDFMV overlap of GATE Anode	0.45	µm
O2P1DP	Minimum POLY1 overlap PDIFF	0.35	µm

**Note:** MV is necessary for dfwdnb

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** Device finger width is defined as Cathode NDIFF width

**Note:** Minimum drawn finger width is 3 µm

**Note:** dfwdnb device must be labeled "dfwdnb" using DIODEF (VERIFICATION) layer over NDFMV inside the innermost DTI hole.

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ dfwdnb

### dfwdnb

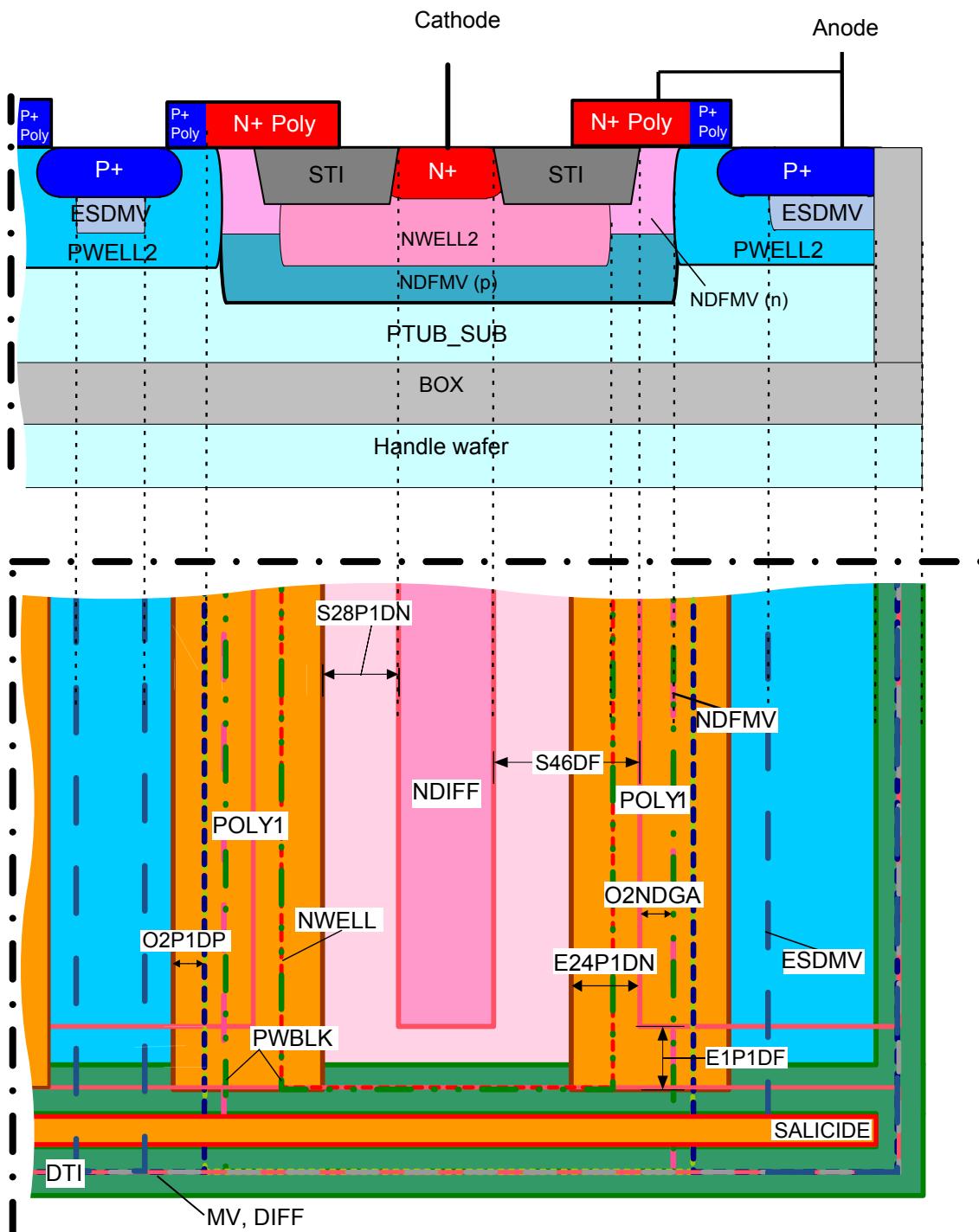


Figure 3.228 dfwdnb

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ dfwdnc

### **dfwdnc**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
S28P1DN	Minimum POLY1 spacing to Cathode NDIFF (in the direction of device length)	0.1	µm
S47DF	Fixed CATHODE-EDGE-STI length	0.42	µm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	µm
E25P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	0.32	µm
O2NDGA	Fixed NDFMV overlap of GATE Anode	0.45	µm
O2P1DP	Minimum POLY1 overlap PDIFF	0.35	µm

**Note:** MV is necessary for dfwdnc

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** Device finger width is defined as Cathode NDIFF width

**Note:** Minimum drawn finger width is 3 µm

**Note:** dfwdnc device must be labeled "dfwdnc" using DIODEF (VERIFICATION) layer over NDFMV inside the innermost DTI hole.

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ dfwdnc

### dfwdnc

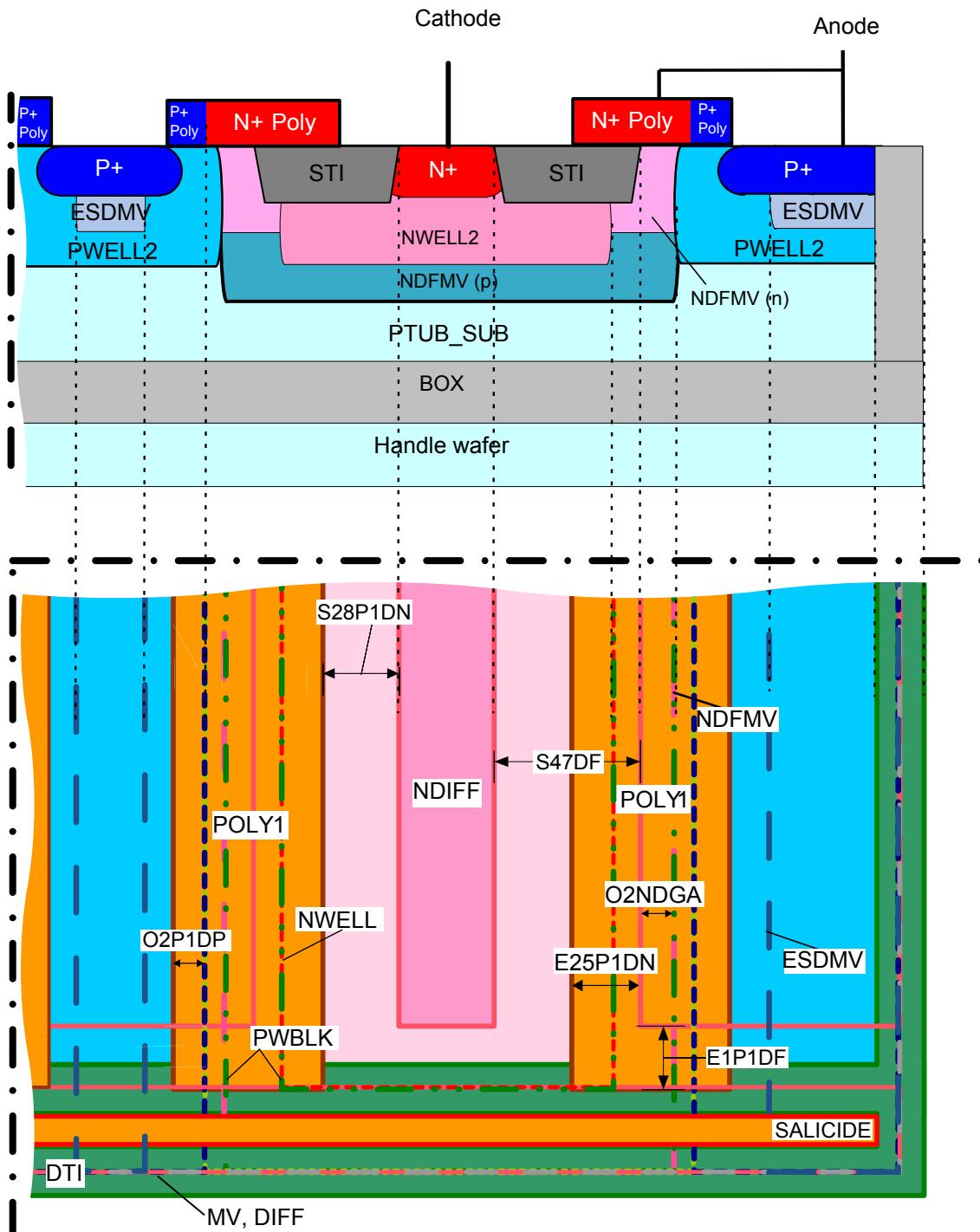


Figure 3.229 dfwdnc

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ dfwdnd

### **dfwdnd**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
S29P1DN	Minimum POLY1 spacing to Cathode NDIFF (in the direction of device length)	0.15	µm
S48DF	Fixed CATHODE-EDGE-STI length	0.45	µm
E1P1DF	Fixed POLY1 extension beyond ACTIVE (in the direction of device width)	1.0	µm
E26P1DN	Minimum POLY1 extension beyond NDIFF (in the direction of device length)	0.3	µm
O2NDGA	Fixed NDFMV overlap of GATE Anode	0.45	µm
O2P1DP	Minimum POLY1 overlap PDIFF	0.35	µm

**Note:** MV is necessary for dfwdnd

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** Device finger width is defined as Cathode NDIFF width

**Note:** Minimum drawn finger width is 3 µm

**Note:** dfwdnd device must be labeled "dfwdnd" using DIODEF (VERIFICATION) layer over NDFMV inside the innermost DTI hole.

3. Layer and Device rules → 3.31 NMV module→ 3.31.2 Device rules→ dfwdnd

### dfwdnd

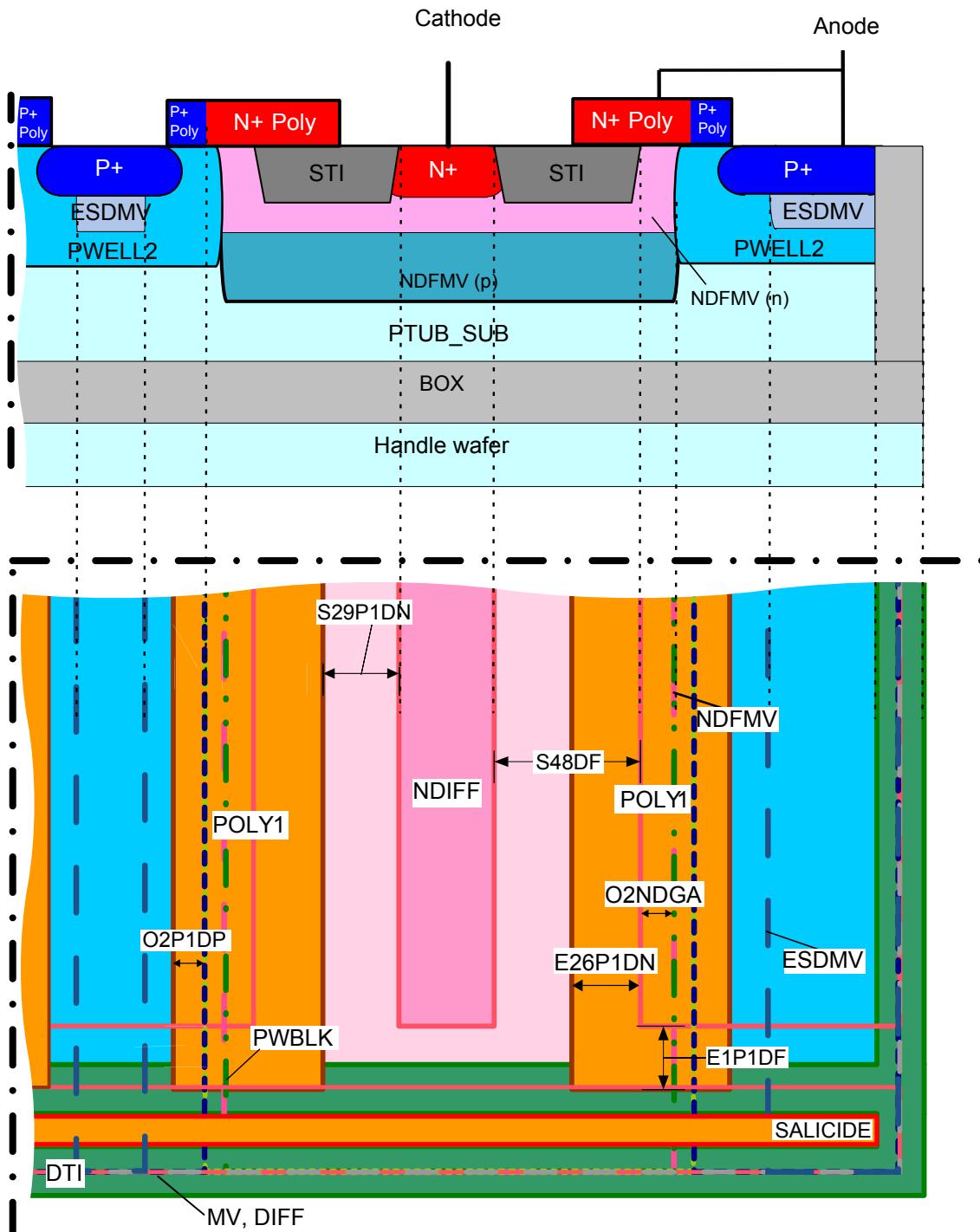


Figure 3.230 dfwdnd

3. Layer and Device rules → 3.32 PHVA module

## 3.32 PHVA module

### 3.32.1 Layer rules

#### PDF

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1PX	PDF is only allowed for phv#	-	-
B2PX	PDF overlap of DNC, NZENER or PWELL4 is not allowed	-	-
B3PX	PDF without PWBLK or NWELL is not allowed	-	-
B4PX	PDF without MV and SUBBLK is not allowed	-	-
W1PX	Minimum PDF width	2.0	μm
S1PX	Minimum PDF spacing/notch	1.5	μm
A1PX	Minimum PDF area	9.5	μm <sup>2</sup>

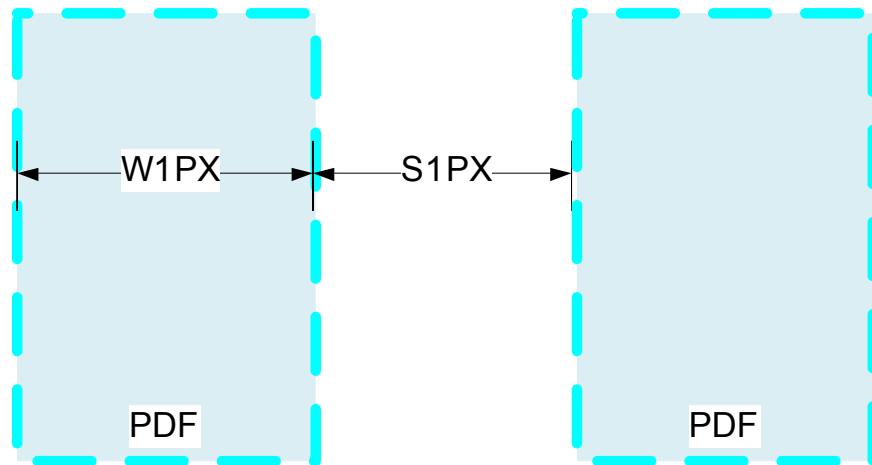


Figure 3.231 PDF

#### PDF\_E

Name	Description	Value	Unit
W2PX	Minimum PDF_E width	0.5	μm

### 3.32.2 Device rules

#### phvta

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B15MV	phvta without MV is not allowed	-	-
B7HB	phvta without SUBBLK is not allowed	-	-
W13GA	Minimum CHANNEL length <b>Note:</b> CHANNEL for this device is defined as GATE AND NWELL	0.5	μm

⇒

## 3. Layer and Device rules → 3.32 PHVA module→ 3.32.2 Device rules→ phvta

Name	Description	Value	Unit
W14GA	Minimum GATE width	3.0	µm
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number		
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
W24GA	Maximum CHANNEL length	1.5	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE AND NWELL		
W2IN	Minimum NIMP width	0.42	µm
S2IP	Minimum PIMP spacing/notch	0.42	µm
S14DF	Fixed DRAIN-EDGE-STI length	1.6	µm
S1P1DP	Minimum POLY1 spacing to DRAIN PDIFF	0.7	µm
S5GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E1M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.5	µm
E1PXDP	Minimum PDF enclosure of DRAIN PDIFF	2.35	µm
E2M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	µm
E12P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E1P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	0.9	µm
O1PXGA	Fixed PDF overlap of GATE	0.75	µm
O1PXNW	Fixed PDF overlap of NWELL	0.1	µm

**Note:** phvta device must be labeled "phvta" using POLY1 (VERIFICATION) layer over GATE

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

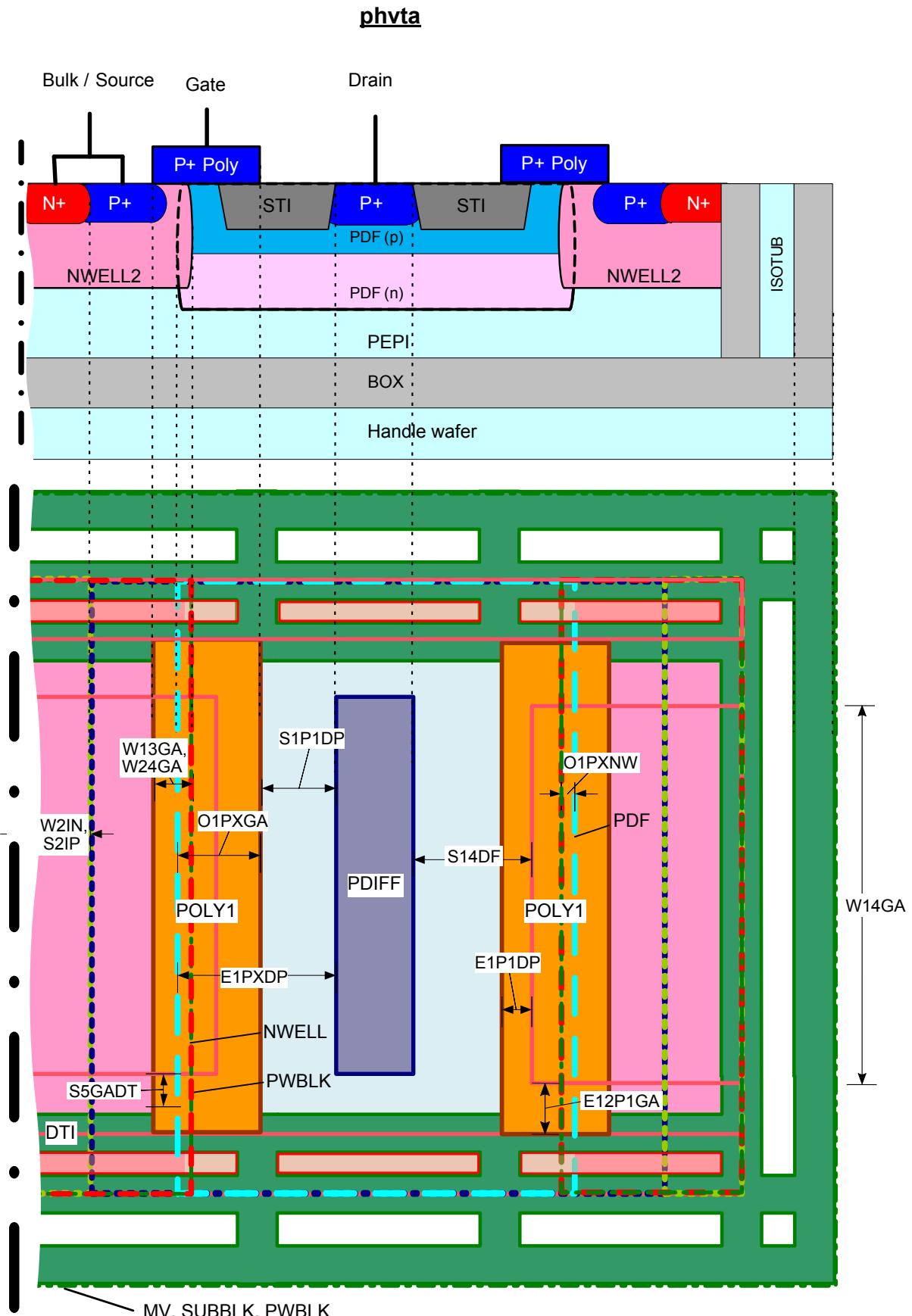
**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.32 PHVA module → 3.32.2 Device rules → phvta



**Figure 3.232 phvta**

3. Layer and Device rules → 3.32 PHVA module→ 3.32.2 Device rules→ phvtb

## phvtb

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B16MV	phvtb without MV is not allowed	-	-
B5PX	MET1 is not allowed over PDF (except predefined POLY1 GATE connection, predefined MET1 device terminal connections)	-	-
B8HB	phvtb without SUBBLK is not allowed	-	-
W13GA	Minimum CHANNEL length	0.5	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE AND NWELL		
W14GA	Minimum GATE width	3.0	μm
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number		
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
W28GA	Maximum CHANNEL length	25.0	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE AND NWELL		
W2IN	Minimum NIMP width	0.42	μm
S2IP	Minimum PIMP spacing/notch	0.42	μm
S15DF	Fixed DRAIN-EDGE-STI length	2.5	μm
S2P1DP	Minimum POLY1 spacing to DRAIN PDIFF	1.4	μm
S5GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
E1M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.5	μm
E2M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	μm
E2PXDP	Minimum PDF enclosure of DRAIN PDIFF	2.5	μm
E12P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E2P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	1.1	μm
O1PXGA	Fixed PDF overlap of GATE	0.75	μm
O1PXNW	Fixed PDF overlap of NWELL	0.1	μm

**Note:** phvtb device must be labeled "phvtb" using POLY1 (VERIFICATION) layer over GATE

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** Each transistor must be surrounded by DTI ring.

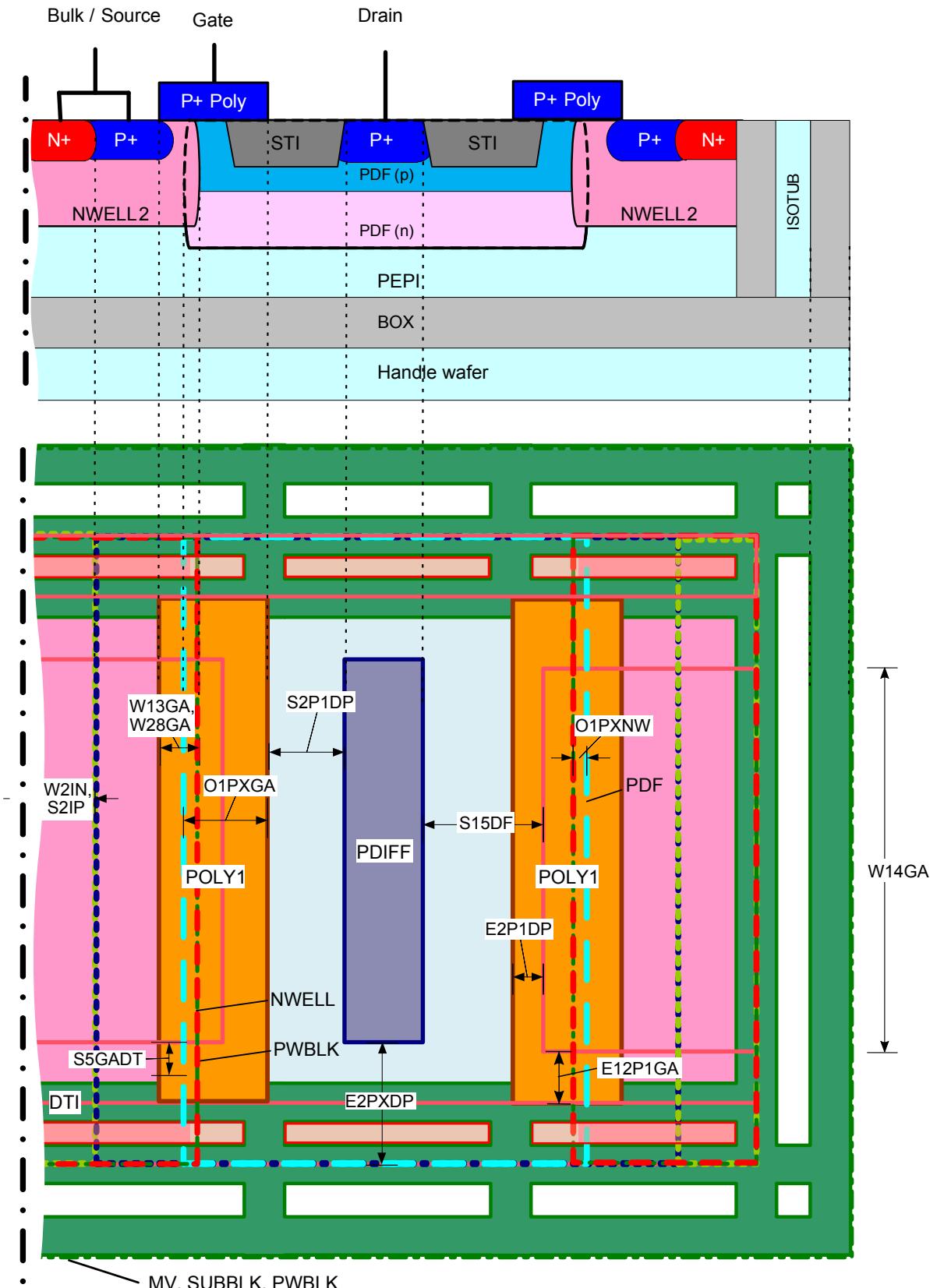
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.32 PHVA module → 3.32.2 Device rules → phvtb

### phvtb



**Figure 3.233 phvtb**

3. Layer and Device rules → 3.32 PHVA module→ 3.32.2 Device rules→ phvu

## phvu

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B17MV	phvu without MV is not allowed	-	-
B5PX	MET1 is not allowed over PDF (except predefined POLY1 GATE connection, predefined MET1 device terminal connections)	-	-
B9HB	phvu without SUBBLK is not allowed	-	-
W13GA	Minimum CHANNEL length	0.5	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE AND NWELL		
W14GA	Minimum GATE width	3.0	μm
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number		
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
W28GA	Maximum CHANNEL length	25.0	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE AND NWELL		
W2IN	Minimum NIMP width	0.42	μm
S2IP	Minimum PIMP spacing/notch	0.42	μm
S16DF	Fixed DRAIN-EDGE-STI length	3.85	μm
S4P1DP	Minimum POLY1 spacing to DRAIN PDIFF	2.05	μm
S5GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
E1M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.5	μm
E2M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	μm
E2PXDP	Minimum PDF enclosure of DRAIN PDIFF	2.5	μm
E12P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
E3P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	1.8	μm
O1PXGA	Fixed PDF overlap of GATE	0.75	μm
O1PXNW	Fixed PDF overlap of NWELL	0.1	μm

**Note:** phvu device must be labeled "phvu" using POLY1 (VERIFICATION) layer over GATE

**Note:** If the potential difference between TUB of device to the surrounding TUB is >100V, it is strongly recommended to use > 1 DTI to the device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.32 PHVA module → 3.32.2 Device rules → phvu

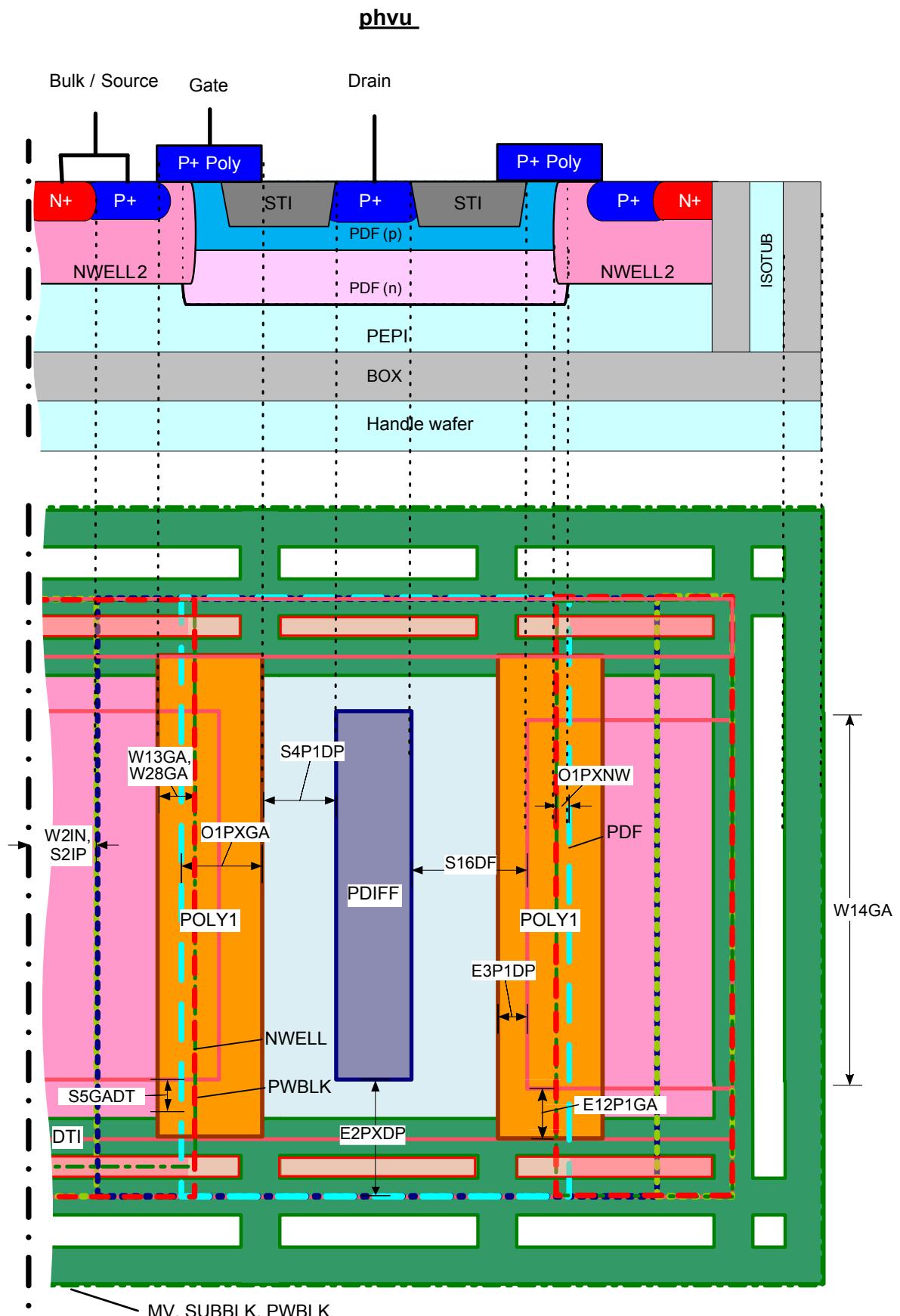


Figure 3.234 phvu

3. Layer and Device rules → 3.33 PHVR module

## 3.33 PHVR module

### 3.33.1 Layer rules

#### DFN

Name	Description	Value	Unit
B1FN	DFN is only allowed for nhvr#, phvr#, ndhvr# or dfwdnh#	-	-
B2FN	DFN overlap of DNC, NDF, PDF, DFP, NDFMV, PDFMV or NZENER is not allowed	-	-
B3FN	DFN without PWBLK or NWELL is not allowed	-	-
B4FN	DFN without SUBBLK and MV is not allowed	-	-
W1FN	Minimum DFN width	1.5	μm
S1FN	Minimum DFN spacing / notch	1.5	μm
A1FN	Minimum DFN area	9.0	μm <sup>2</sup>

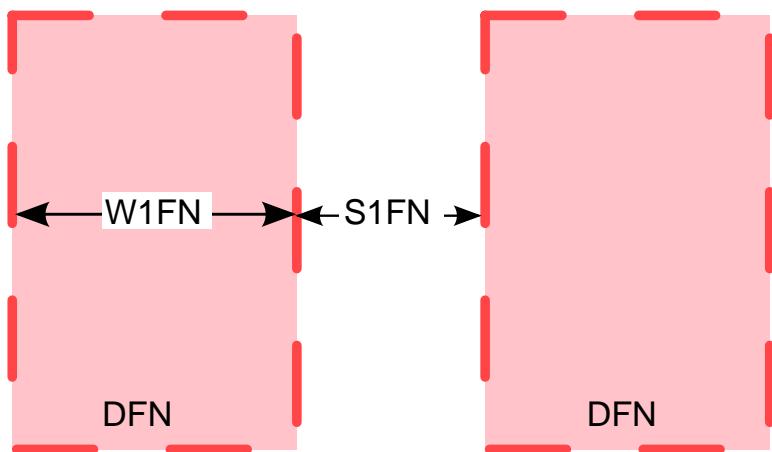


Figure 3.235 DFN

3. Layer and Device rules → 3.33 PHVR module → 3.33.1 Layer rules → DFP

## DFP

Name	Description	Value	Unit
B1FP	DFP is only allowed for phvr#	-	-
B2FP	DFP overlap of DNC, NDF, PDF, NDFMV, PDFMV, NZENER, PZENER or PWELL4 is not allowed	-	-
B3FP	DFP without PWBLK is not allowed	-	-
B4FP	DFP without MV and SUBBLK is not allowed	-	-
W1FP	Minimum DFP width	2.0	μm
S1FP	Minimum DFP spacing / notch	2.0	μm
A1FP	Minimum DFP area	9.5	μm <sup>2</sup>

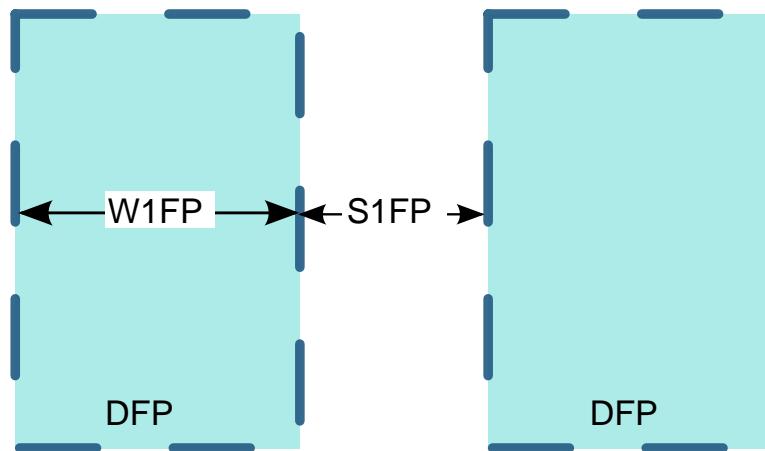


Figure 3.236 DFP

## DFP\_E

Name	Description	Value	Unit
W2FP	Minimum DFP_E width	0.5	μm

## 3.33.2 Device rules

### phvra

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W57GA	Minimum GATE width	3.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
W68GA	Minimum CHANNEL length	0.5	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
W69GA	Maximum CHANNEL length	25.0	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
S10P1DP	Minimum POLY1 spacing to DRAIN PDIFF (in the direction of GATE length)	0.58	μm
S1FPNW	Fixed DFP spacing to NWELL (in CHANNEL region)	0.1	μm
S34DF	Fixed DRAIN-EDGE-STI length	1.1	μm

⇒

## 3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvra

Name	Description	Value	Unit
S9GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E2M2DP	Minimum MET2 enclosure of DRAIN PDIFF (in the direction of GATE width)	3.0	µm
E4M2DP	Fixed MET2 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.45	µm
E6M1DP	Minimum MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	µm
E8M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.25	µm
E16P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
E9P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	0.52	µm
O1FPGA	Fixed DFP overlap of GATE	0.75	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** phvra device must be labeled "phvra" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

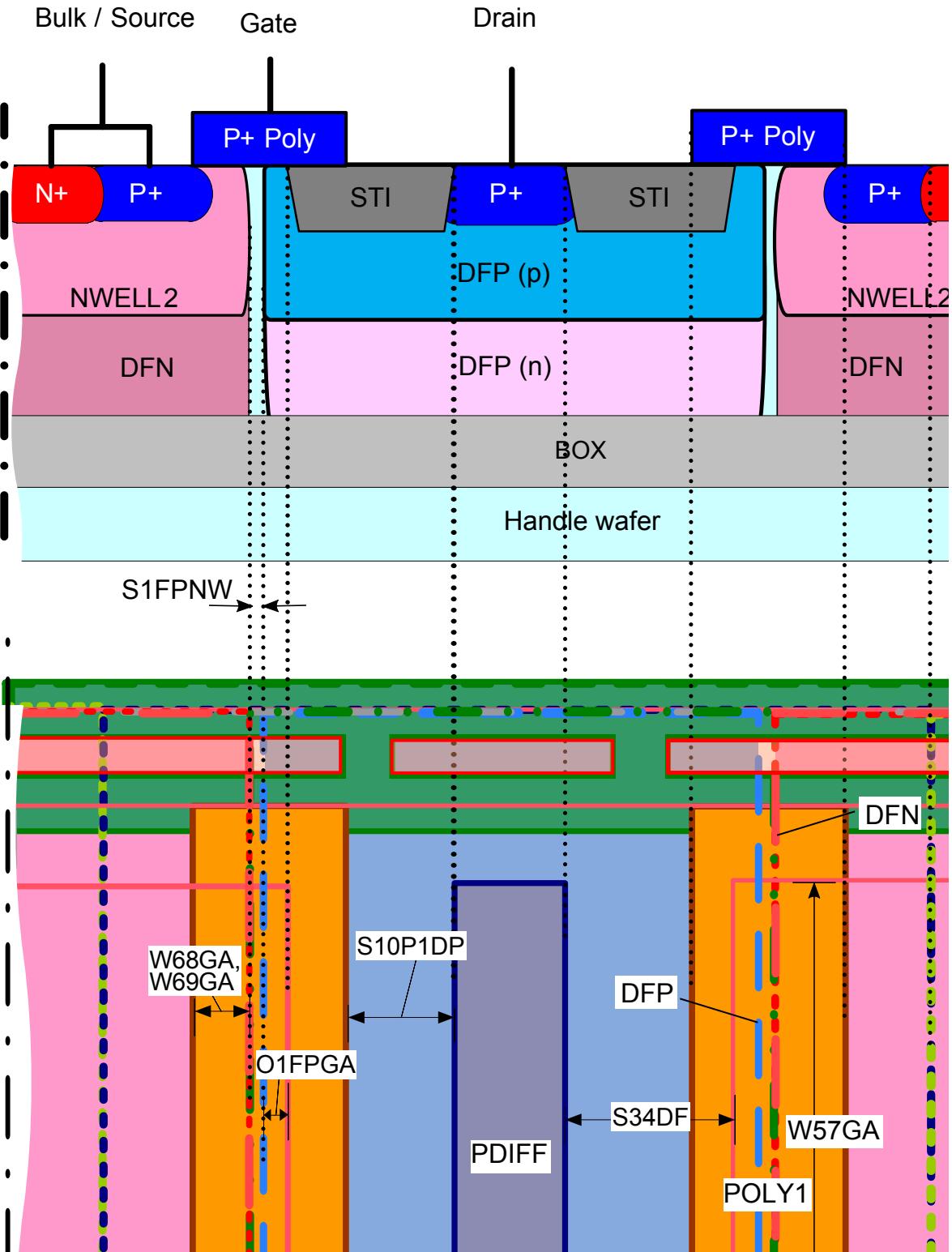
**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvra

### phvra



**Figure 3.237 phvra**

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvrb

## phvrb

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W57GA	Minimum GATE width	3.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W68GA	Minimum CHANNEL length	0.5	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
W69GA	Maximum CHANNEL length	25.0	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
S11P1DP	Minimum POLY1 spacing to DRAIN PDIFF (in the direction of GATE length)	1.35	µm
S1FPNW	Fixed DFP spacing to NWELL (in CHANNEL region)	0.1	µm
S35DF	Fixed DRAIN-EDGE-STI length	2.5	µm
S9GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E1M2DP	Fixed MET2 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.5	µm
E2M2DP	Minimum MET2 enclosure of DRAIN PDIFF (in the direction of GATE width)	3.0	µm
E5M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.4	µm
E6M1DP	Minimum MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	µm
E10P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	1.15	µm
E16P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1FPGA	Fixed DFP overlap of GATE	0.75	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** phvrb device must be labeled "phvrb" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

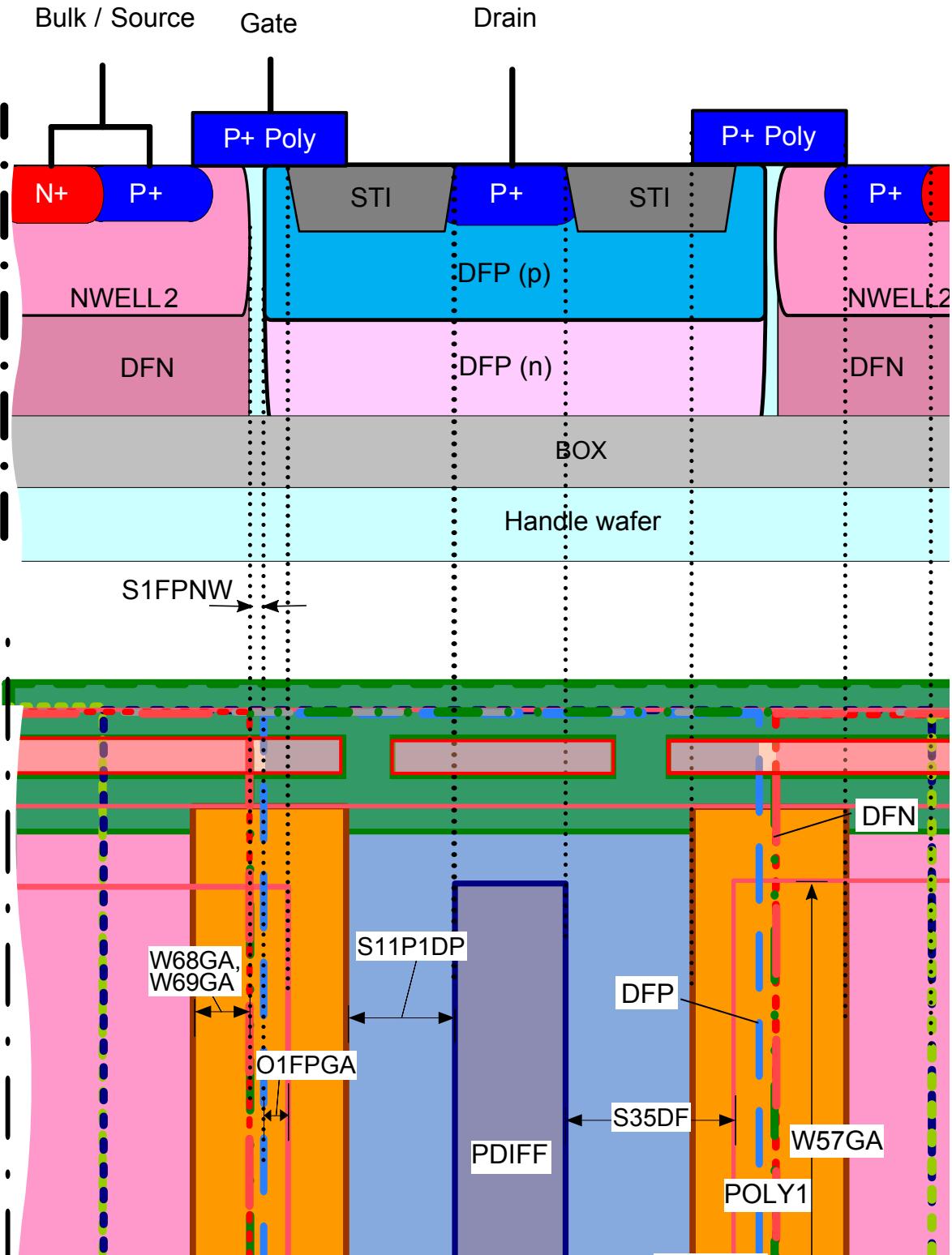
**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvrb

### **phvrb**



**Figure 3.238 phvrb**

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvrc

## phvrc

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W57GA	Minimum GATE width	3.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W68GA	Minimum CHANNEL length	0.5	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
W69GA	Maximum CHANNEL length	25.0	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
S12P1DP	Minimum POLY1 spacing to DRAIN PDIFF (in the direction of GATE length)	1.8	µm
S1FPNW	Fixed DFP spacing to NWELL (in CHANNEL region)	0.1	µm
S36DF	Fixed DRAIN-EDGE-STI length	3.0	µm
S9GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E2M2DP	Minimum MET2 enclosure of DRAIN PDIFF (in the direction of GATE width)	3.0	µm
E5M2DP	Fixed MET2 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.85	µm
E6M1DP	Minimum MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	µm
E9M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.75	µm
E11P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	1.2	µm
E16P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O2FPGA	Fixed DFP overlap of GATE	0.85	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** phvrc device must be labeled "phvrc" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

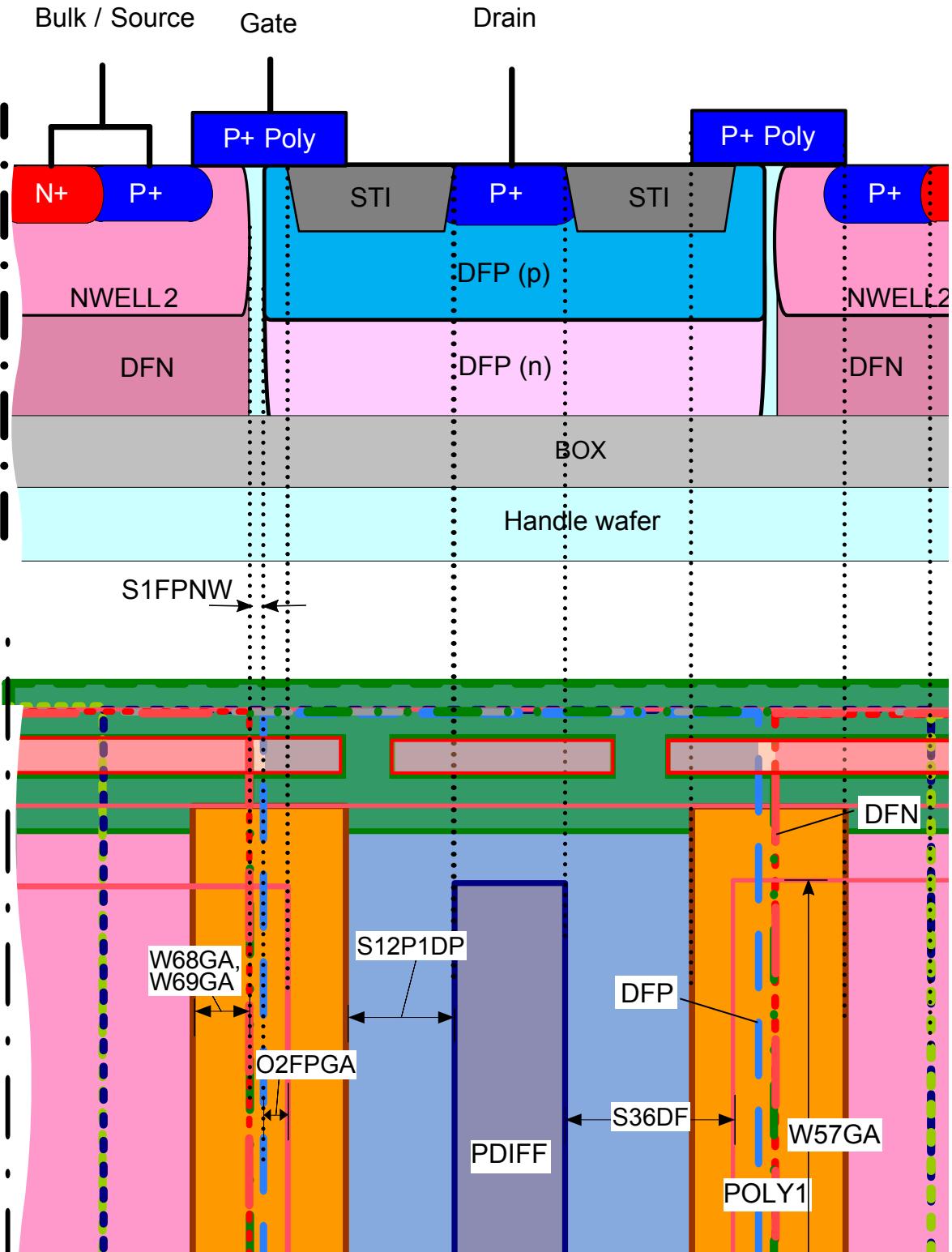
**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvrc

### phvrc



**Figure 3.239** phvrc

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvrd

## **phvrd**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W57GA	Minimum GATE width	3.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W68GA	Minimum CHANNEL length	0.5	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
W69GA	Maximum CHANNEL length	25.0	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
S13P1DP	Minimum POLY1 spacing to DRAIN PDIFF (in the direction of GATE length)	2.28	µm
S1FPNW	Fixed DFP spacing to NWELL (in CHANNEL region)	0.1	µm
S37DF	Fixed DRAIN-EDGE-STI length	3.8	µm
S9GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E2M2DP	Minimum MET2 enclosure of DRAIN PDIFF (in the direction of GATE width)	3.0	µm
E3M2DP	Fixed MET2 enclosure of DRAIN PDIFF (in the direction of GATE length)	1.1	µm
E6M1DP	Minimum MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	µm
E7M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	1.0	µm
E12P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	1.52	µm
E16P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O2FPGA	Fixed DFP overlap of GATE	0.85	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** phvrd device must be labeled "phvrd" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

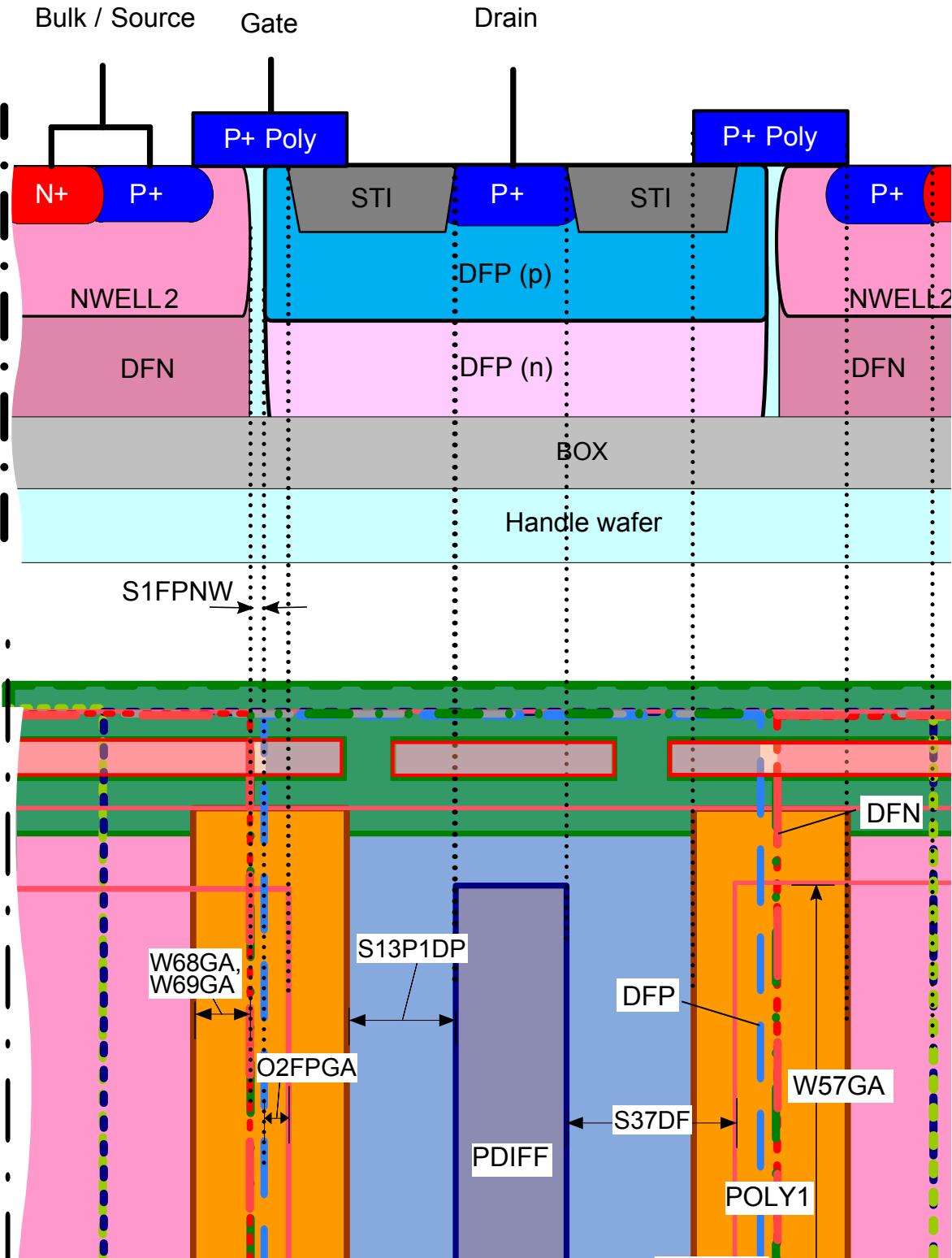
**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvrd

### phvrd



**Figure 3.240** phvrd

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvre

### **phvre**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W57GA	Minimum GATE width	3.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W68GA	Minimum CHANNEL length	0.5	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
W69GA	Maximum CHANNEL length	25.0	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
S14P1DP	Minimum POLY1 spacing to DRAIN PDIFF (in the direction of GATE length)	3.0	µm
S1FPNW	Fixed DFP spacing to NWELL (in CHANNEL region)	0.1	µm
S38DF	Fixed DRAIN-EDGE-STI length	5.0	µm
S9GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E1M2DP	Fixed MET2 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.5	µm
E2M2DP	Minimum MET2 enclosure of DRAIN PDIFF (in the direction of GATE width)	3.0	µm
E5M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.4	µm
E6M1DP	Minimum MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	µm
E13P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	2.0	µm
E16P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1FPGA	Fixed DFP overlap of GATE	0.75	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** phvre device must be labeled "phvre" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

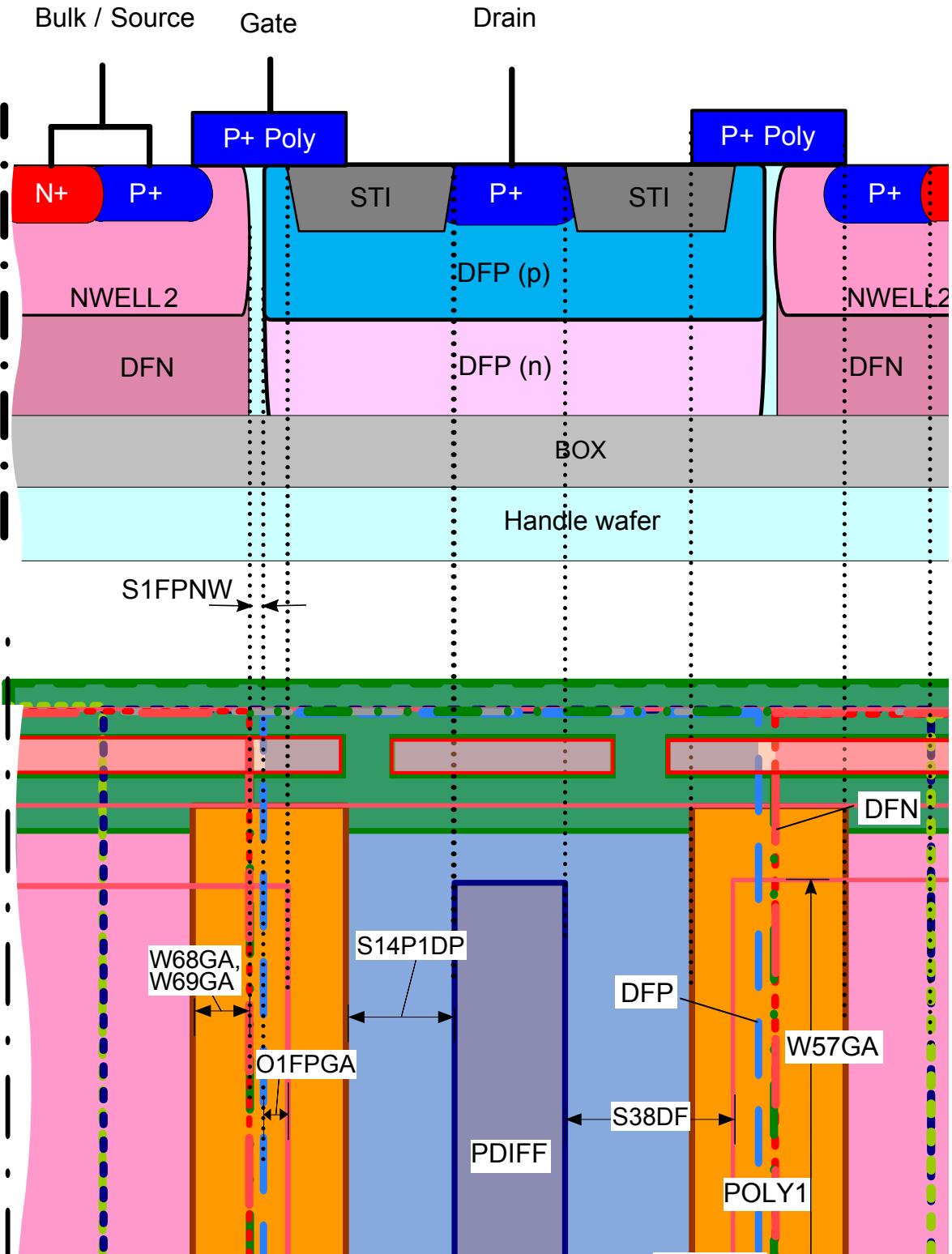
**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvre

### phvre



**Figure 3.241** phvre

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvrf

## phvrf

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W57GA	Minimum GATE width	3.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
W68GA	Minimum CHANNEL length	0.5	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
W69GA	Maximum CHANNEL length	25.0	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and NWELL.		
S15P1DP	Minimum POLY1 spacing to DRAIN PDIFF (in the direction of GATE length)	4.8	µm
S1FPNW	Fixed DFP spacing to NWELL (in CHANNEL region)	0.1	µm
S39DF	Fixed DRAIN-EDGE-STI length	8.0	µm
S9GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E1M2DP	Fixed MET2 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.5	µm
E2M2DP	Minimum MET2 enclosure of DRAIN PDIFF (in the direction of GATE width)	3.0	µm
E5M1DP	Fixed MET1 enclosure of DRAIN PDIFF (in the direction of GATE length)	0.4	µm
E6M1DP	Minimum MET1 enclosure of DRAIN PDIFF (in the direction of GATE width)	2.0	µm
E14P1DP	Minimum POLY1 extension beyond PDIFF (in the direction of GATE length)	3.2	µm
E16P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1FPGA	Fixed DFP overlap of GATE	0.75	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** phvrf device must be labeled "phvrf" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.33 PHVR module→ 3.33.2 Device rules→ phvrf

### phvrf

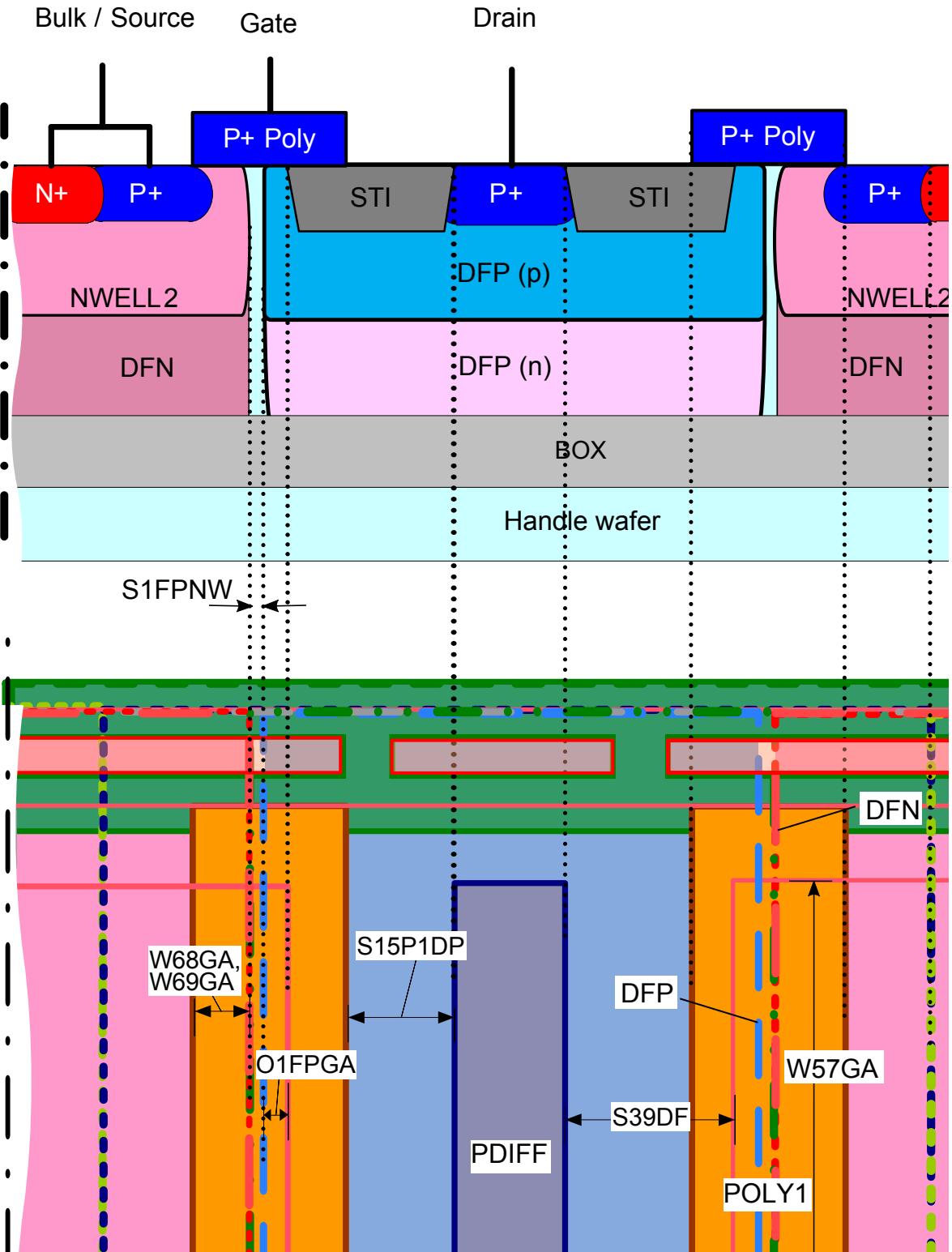


Figure 3.242 phvrf

3. Layer and Device rules → 3.34 PMV module

## 3.34 PMV module

### 3.34.1 Layer rules

#### PDFMV

Name	Description	Value	Unit
B1PD	PDFMV is only allowed for pmv#	-	-
B2PD	PDFMV overlap of NWELL, HVNWELL, HVPWELL or PWELL4 is not allowed	-	-
B3PD	PDFMV overlap of NDF, PDF, DEPL, NBASE, PBASE or PZENER is not allowed	-	-
B4PD	PDFMV without MV and SUBBLK is not allowed	-	-
W1PD	Minimum PDFMV width	1.6	μm
S1PD	Minimum PDFMV spacing / notch	1.5	μm
A1PD	Minimum PDFMV area	9.0	μm <sup>2</sup>

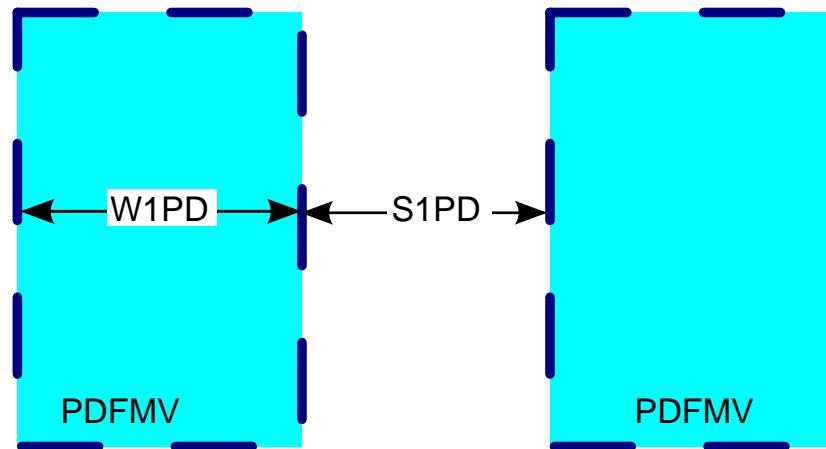


Figure 3.243 PDFMV

#### PDFMV\_E

Name	Description	Value	Unit
W2PD	Minimum PDFMV_E width	0.5	μm

### 3.34.2 Device rules

#### pmvb

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W42GA	Minimum CHANNEL length	0.4	μm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not PDFMV.		
W43GA	Minimum GATE width	3.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

⇒

## 3. Layer and Device rules → 3.34 PMV module→ 3.34.2 Device rules→ pmvb

Name	Description	Value	Unit
W44GA	Maximum CHANNEL length	25.0	µm
	<b>Note:</b> CHANNEL for this device is defined as GATE and not PDFMV.		
S23DF	Fixed DRAIN-EDGE-STI length	0.4	µm
S5P1DP	Minimum POLY1 spacing to DRAIN PDIFF	0.18	µm
S7GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
E14P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1PDGA	Fixed PDFMV overlap of GATE	0.32	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** pmvb device must be labeled "pmvb" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

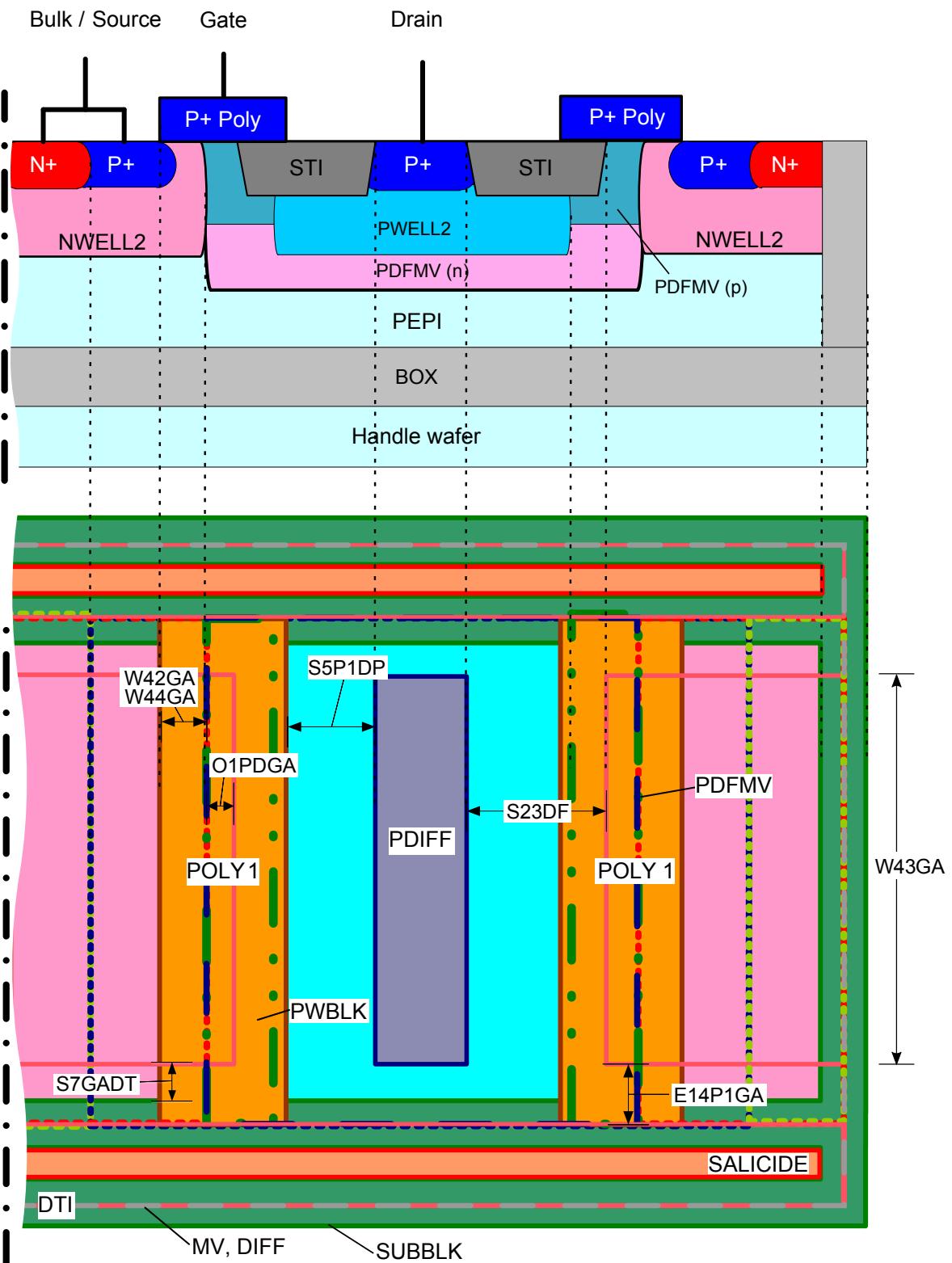
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.34 PMV module → 3.34.2 Device rules → pmvb

### pmvb



**Figure 3.244 pmvb**

3. Layer and Device rules → 3.34 PMV module→ 3.34.2 Device rules→ pmvd

## **pmvd**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W42GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not PDFMV.	0.4	µm
W43GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	µm
W44GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not PDFMV.	25.0	µm
S25DF	Fixed DRAIN-EDGE-STI length	0.47	µm
S7GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
S7P1DP	Minimum POLY1 spacing to DRAIN PDIFF	0.25	µm
E14P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1PDGA	Fixed PDFMV overlap of GATE	0.32	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** pmvd device must be labeled "pmvd" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

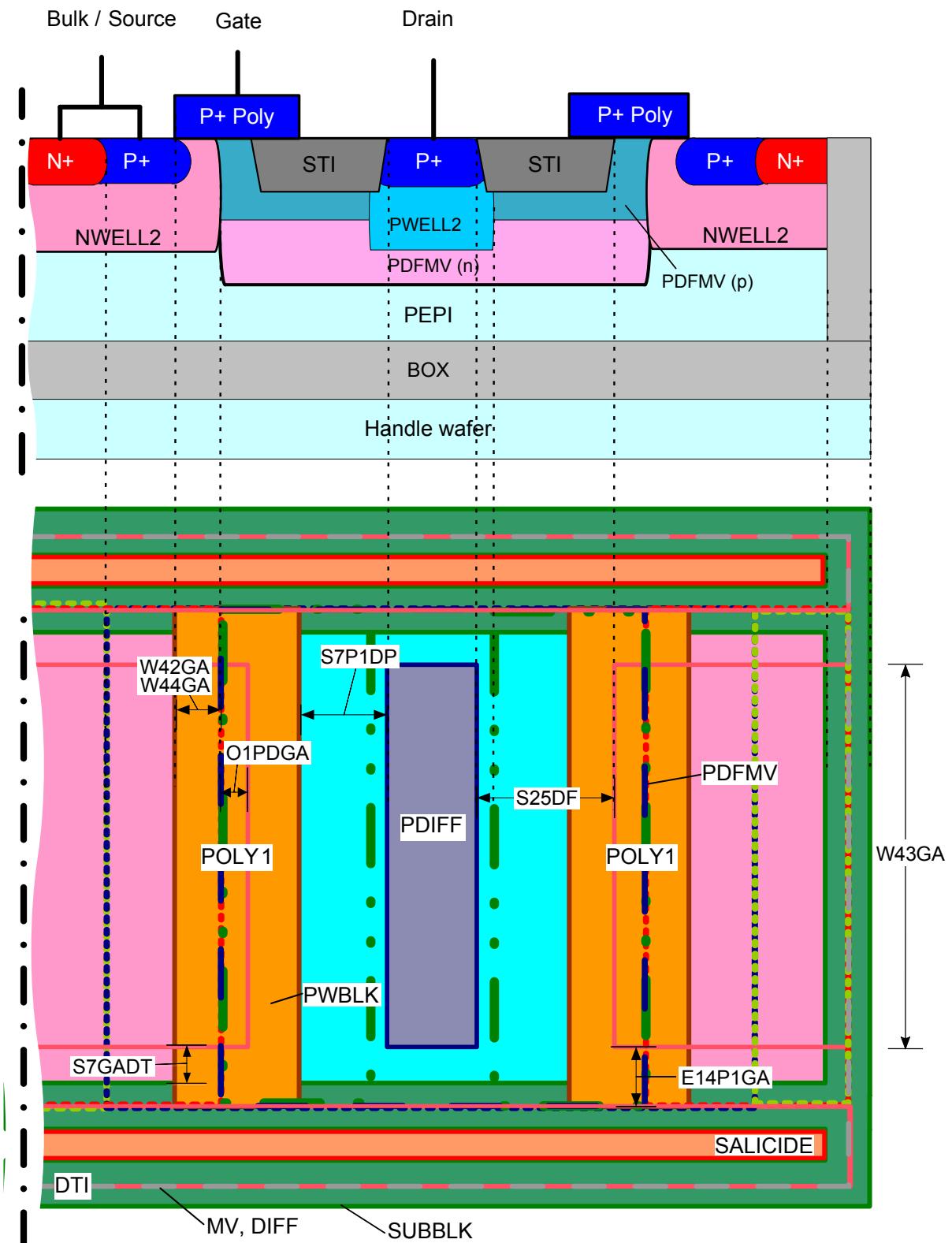
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.34 PMV module → 3.34.2 Device rules → pmvd

### pmvd



**Figure 3.245 pmvd**

3. Layer and Device rules → 3.34 PMV module→ 3.34.2 Device rules→ pmve

### **pmve**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W42GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not PDFMV.	0.4	µm
W43GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	µm
W44GA	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not PDFMV.	25.0	µm
S26DF	Fixed DRAIN-EDGE-STI length	0.77	µm
S7GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	µm
S8P1DP	Minimum POLY1 spacing to DRAIN PDIFF	0.55	µm
E14P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	µm
O1PDGA	Fixed PDFMV overlap of GATE	0.32	µm

**Note:** MV and SUBBLK are necessary for this device

**Note:** pmve device must be labeled "pmve" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

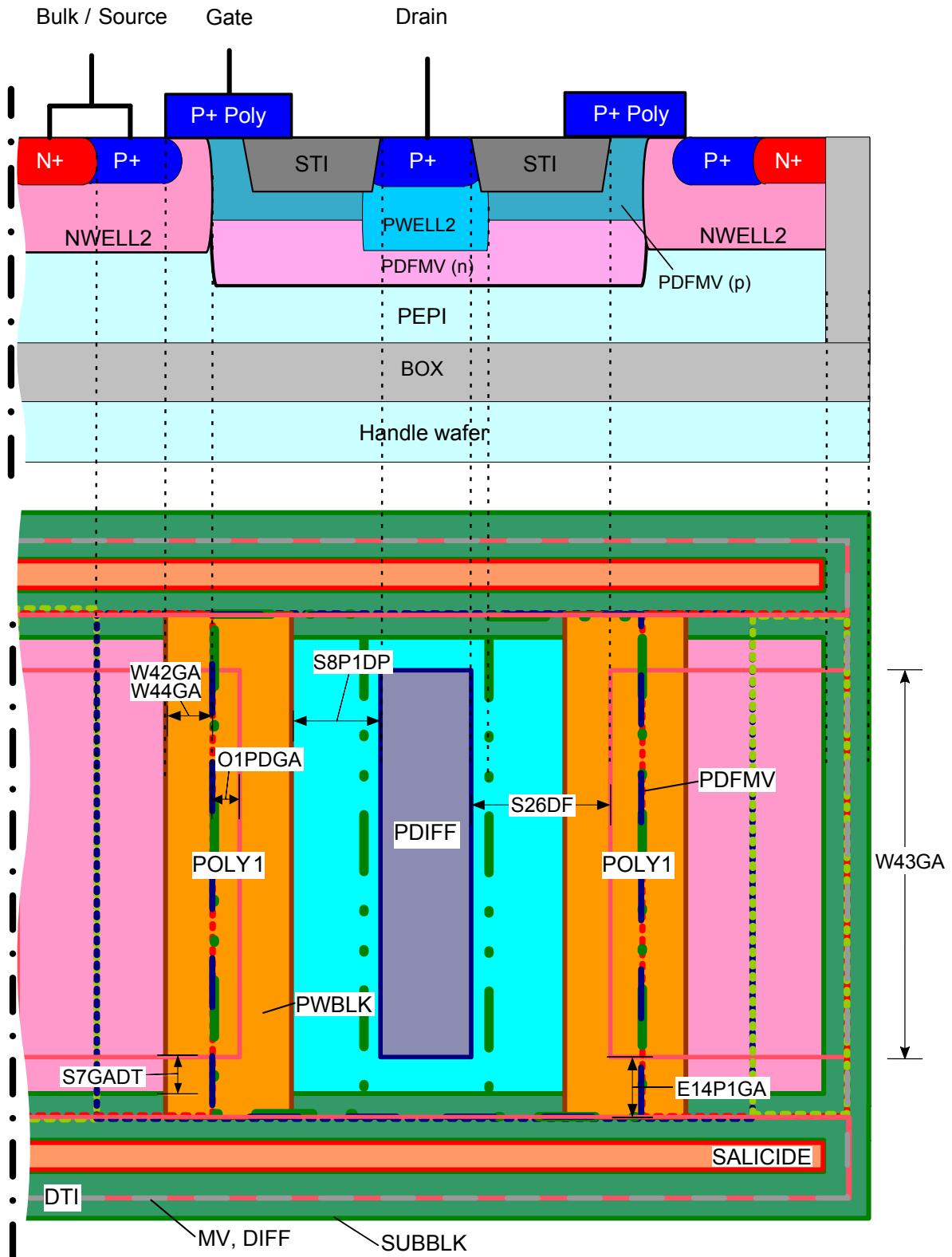
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.34 PMV module → 3.34.2 Device rules → pmve

### pmve



**Figure 3.246 pmve**

3. Layer and Device rules → 3.34 PMV module→ 3.34.2 Device rules→ pmvf

## **pmvf**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
W42GA	Minimum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not PDFMV.	0.4	μm
<b>W43GA</b>			
	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum number of GATE fingers is 2. The device's GATE fingers must be in even number.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	3.0	μm
<b>W44GA</b>			
	Maximum CHANNEL length  <b>Note:</b> CHANNEL for this device is defined as GATE and not PDFMV.	25.0	μm
S27DF	Fixed DRAIN-EDGE-STI length	1.47	μm
S7GADT	Fixed GATE spacing to DTI (in the direction of GATE width)	0.5	μm
S9P1DP	Minimum POLY1 spacing to DRAIN PDIFF	1.25	μm
E14P1GA	Fixed POLY1 extension beyond GATE (in the direction of GATE width)	1.0	μm
O1PDGA	Fixed PDFMV overlap of GATE	0.32	μm

**Note:** MV and SUBBLK are necessary for this device

**Note:** pmvf device must be labeled "pmvf" using POLY1 (VERIFICATION) layer over GATE

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The handle wafer must be biased by using the HWC module, by backside metalisation/packaging or by relying on large-area capacitive coupling through the BOX. In case of backside metalisation/packaging, the HWC (VERIFICATION) is used for auxiliary handle wafer contact and must be labeled by using HWC (TEXT) layer. Please refer to the Application Note "[XT018 Layout Techniques](#)" on "my X-FAB".

3. Layer and Device rules → 3.34 PMV module → 3.34.2 Device rules → pmvf

### pmvf

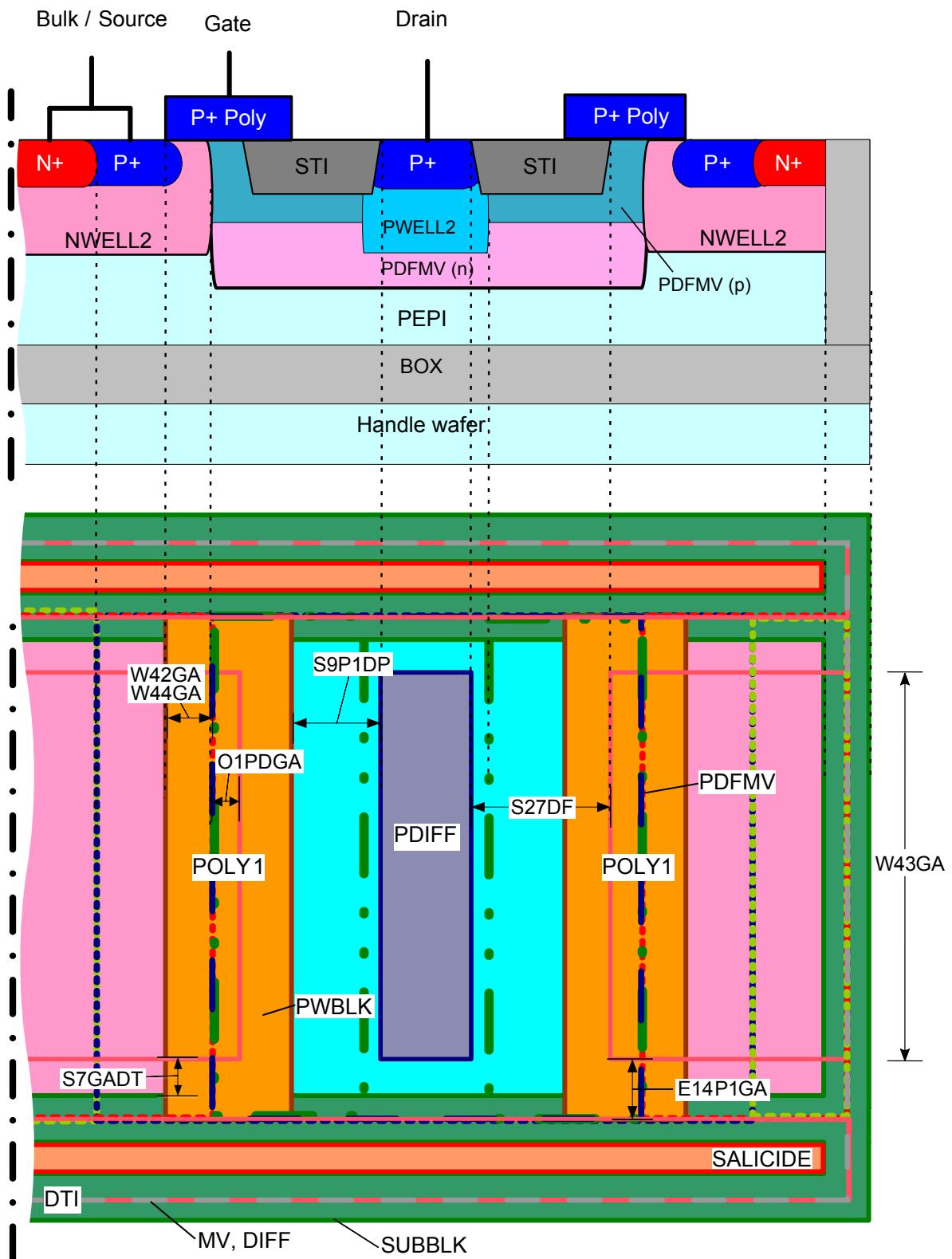


Figure 3.247 pmvf

3. Layer and Device rules → 3.35 SJHVL module

## 3.35 SJHVL module

### 3.35.1 Device rules

#### nhsj1b\_2

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	µm
W38GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	µm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_2 device must be labeled "nhsj1b\_2" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → nhsj1b\_2

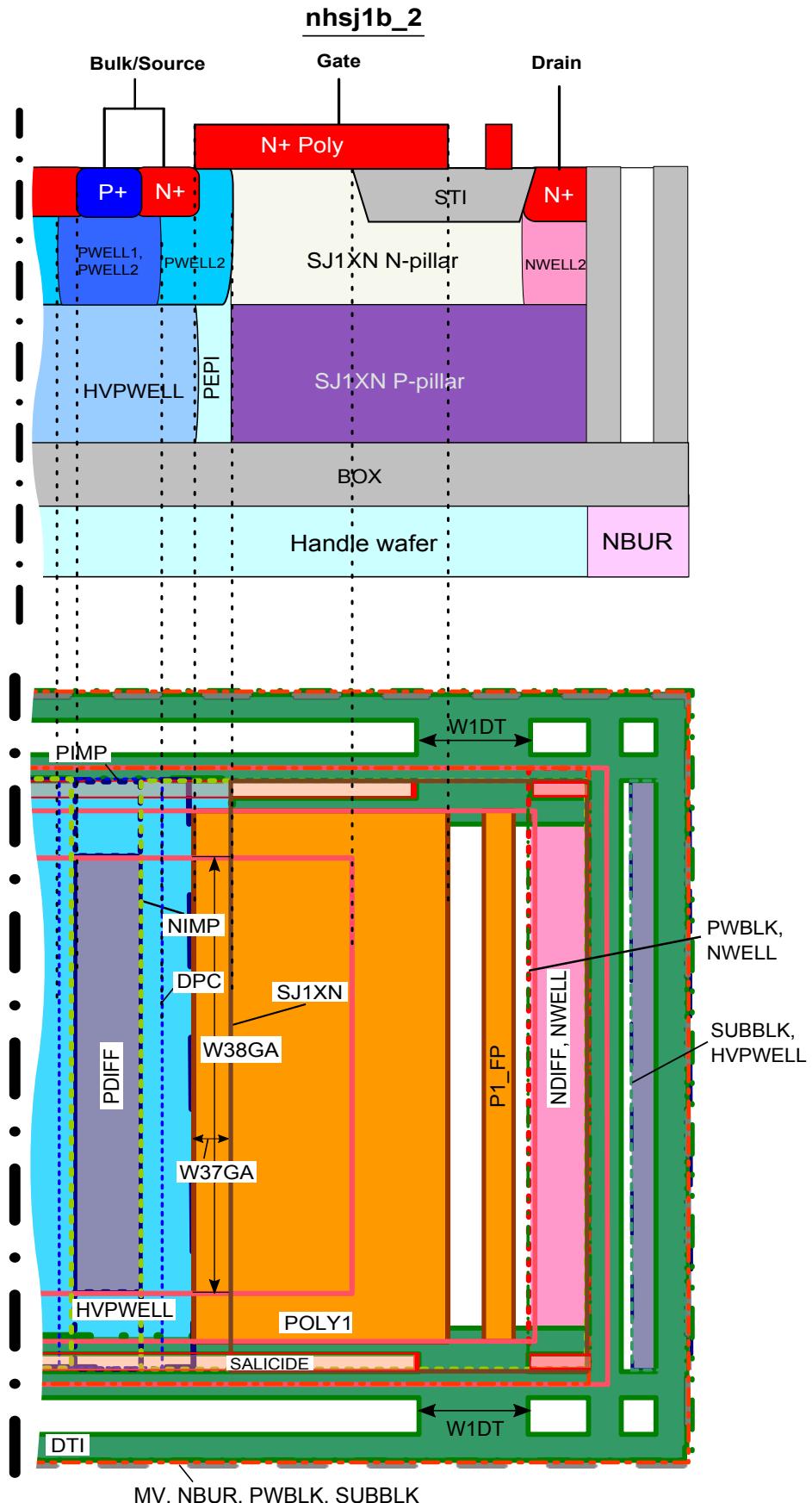


Figure 3.248 nhsj1b\_2

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ nhsj1b\_4

### **nhsj1b\_4**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
	Minimum GATE width	10.0	μm
W38GA	<b>Note:</b> Minimum GATE width is defined as single GATE finger width. <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		
W39GA	Minimum CHANNEL length	0.5	μm
W40GA	Maximum CHANNEL length	10.0	μm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_4 device must be labeled "nhsj1b\_4" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → nhsj1b\_4

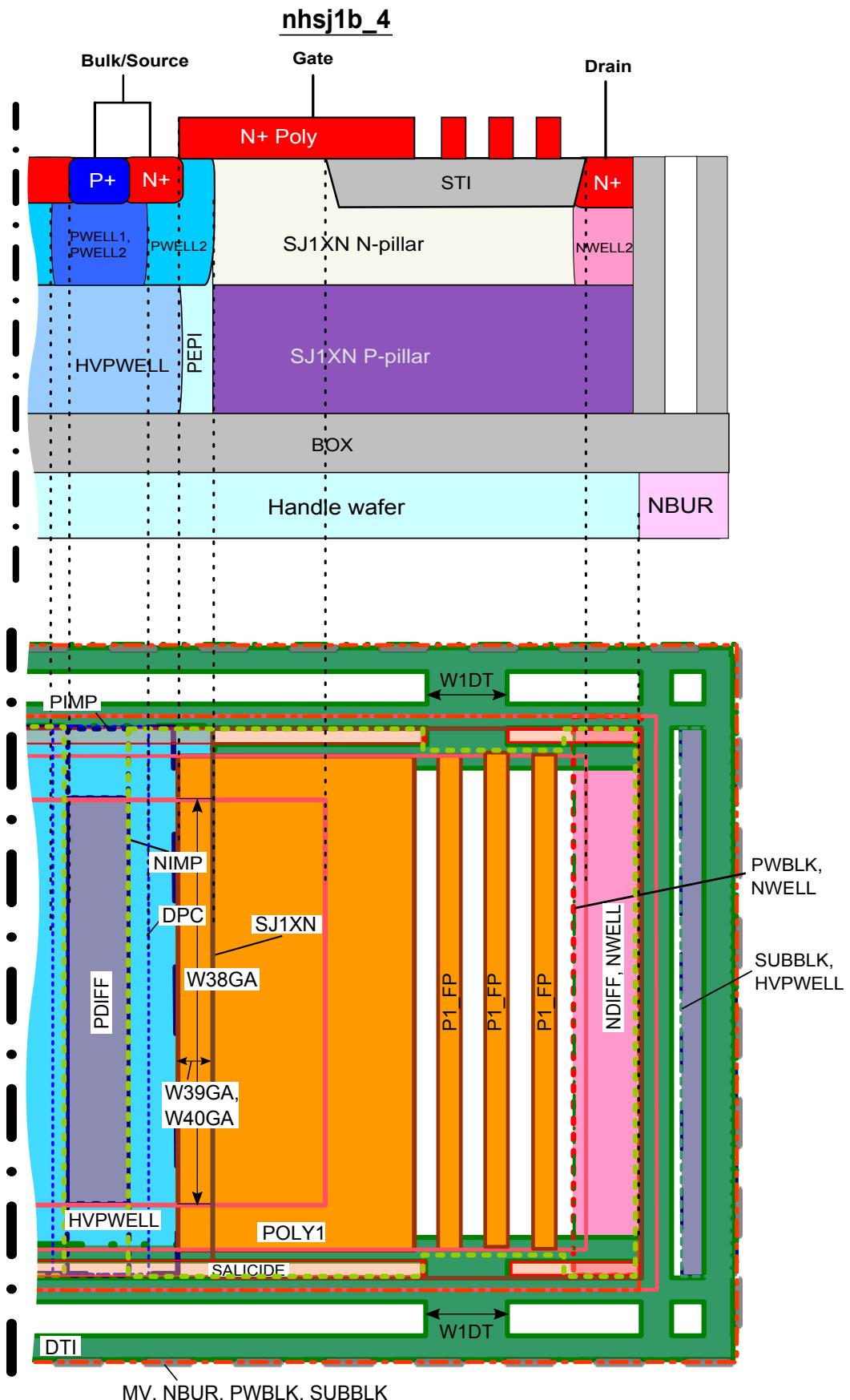


Figure 3.249 nhsj1b\_4

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ nhsj1b\_5

### **nhsj1b\_5**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W38GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_5 device must be labeled "nhsj1b\_5" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ nhsj1b\_5

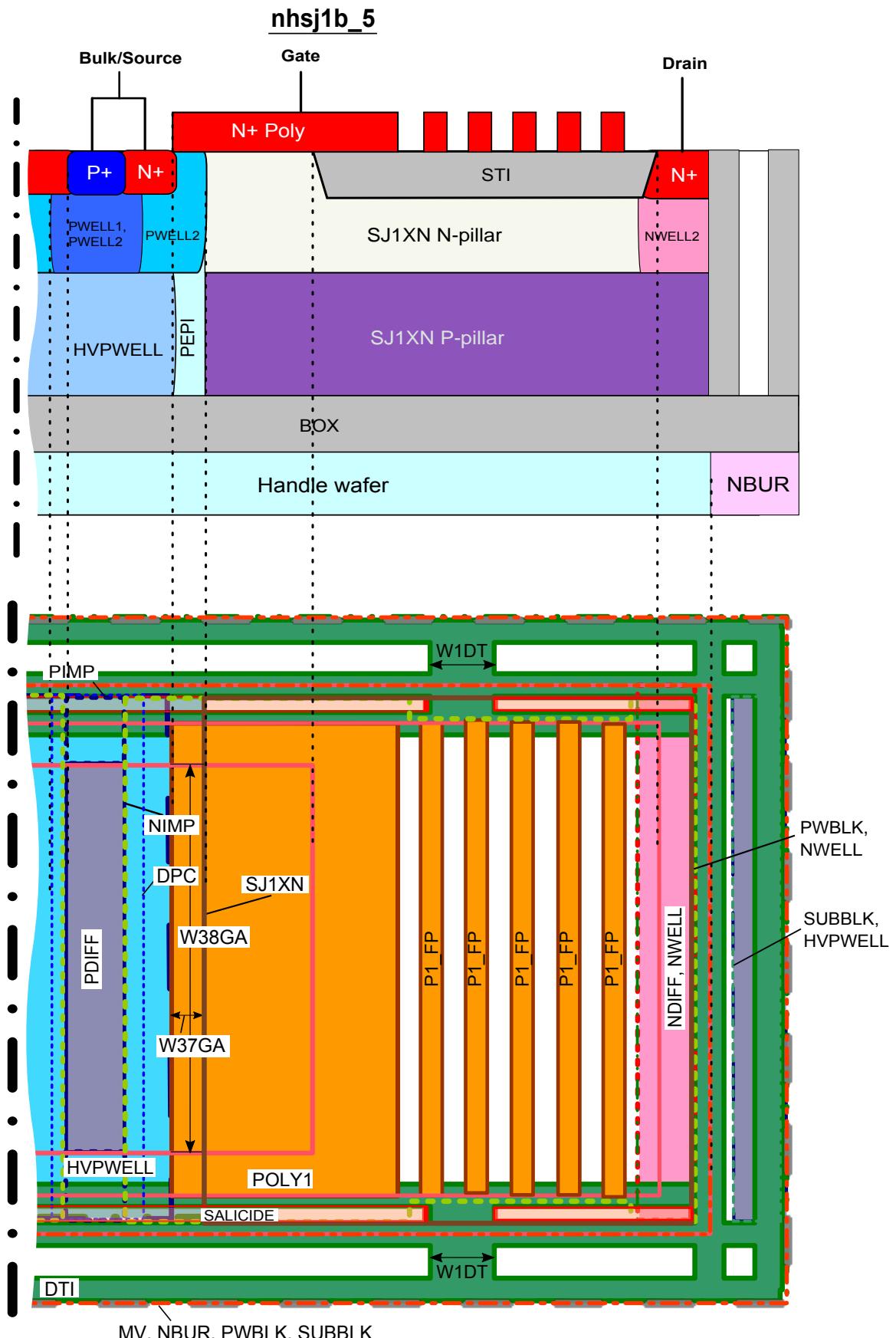


Figure 3.250 nhsj1b\_5

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ nhsj1b\_7

### **nhsj1b\_7**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W45GA	Minimum GATE width	15.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_7 device must be labeled "nhsj1b\_7" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

## 3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → nhsj1b\_7

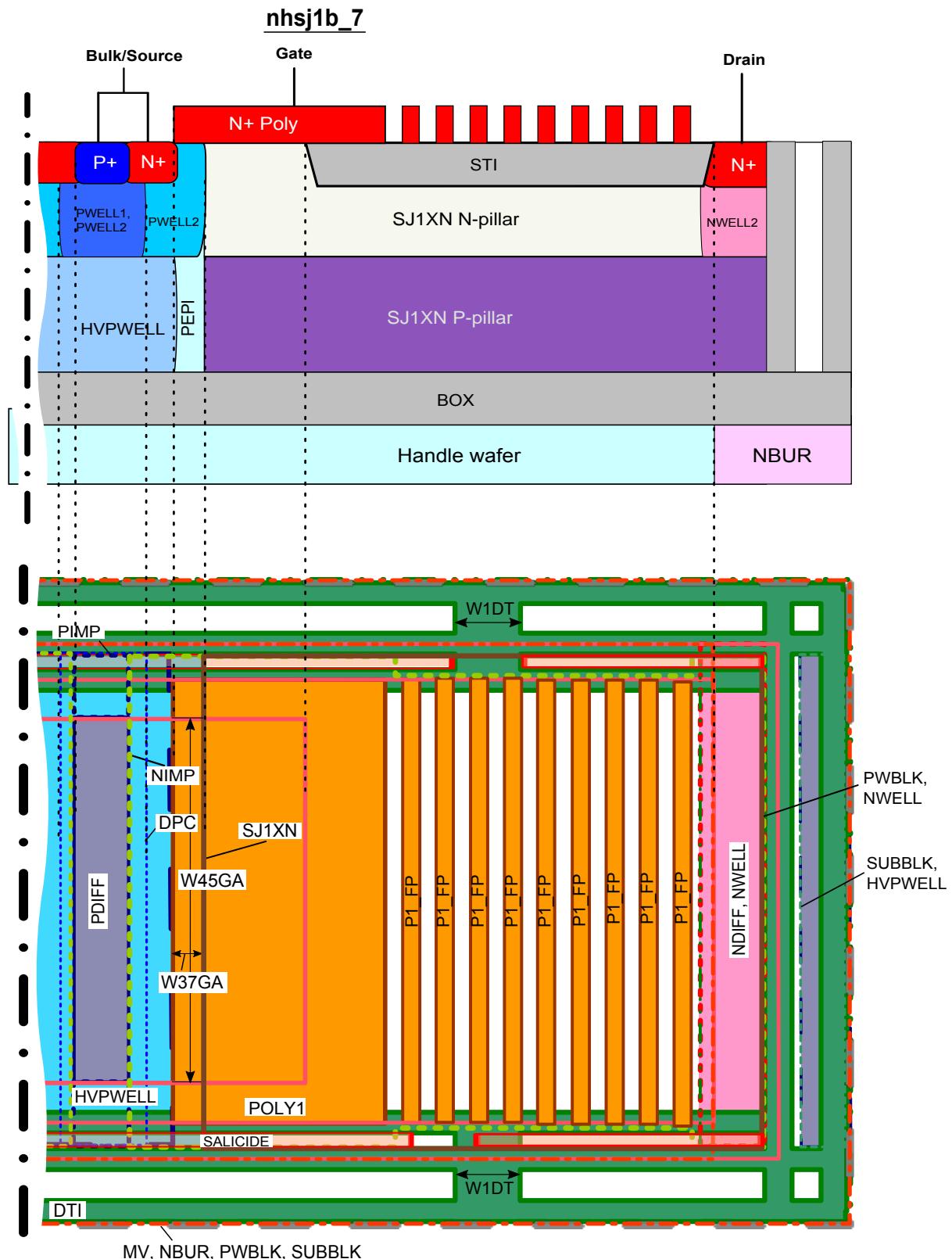


Figure 3.251 nhsj1b\_7

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ phsj2b\_7

### **phsj2b\_7**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
B8X4	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W61GA	Fixed CHANNEL length	0.5	μm
W63GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj2b\_7 device must be labeled "phsj2b\_7" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → phsj2b\_7

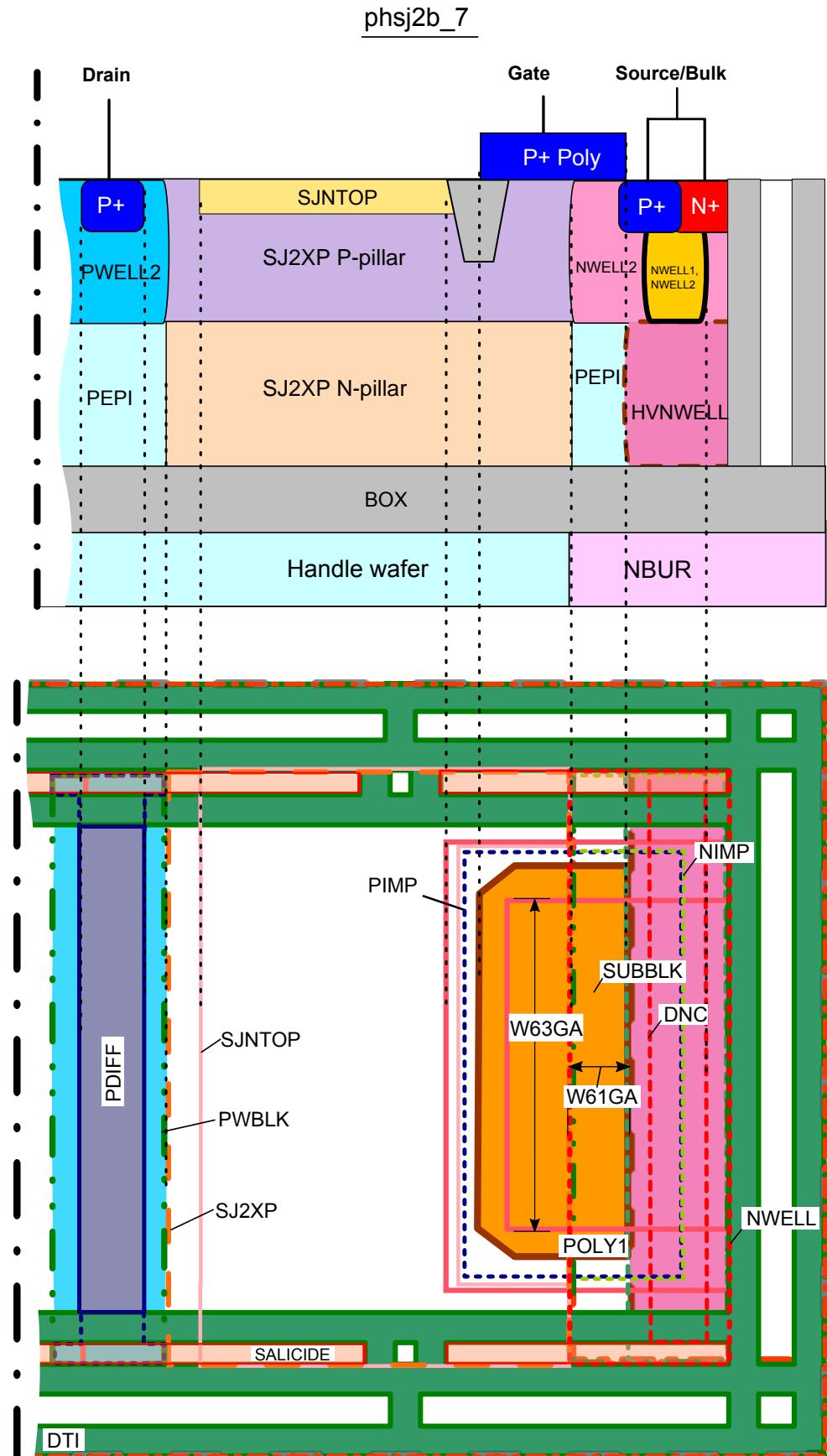


Figure 3.252 phsj2b\_7

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ phsj1a\_4

### **phsj1a\_4**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B6X2	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	μm

**Note:** phsj1a\_4 device must be labeled "phsj1a\_4" using POLY1 (VERIFICATION) layer over GATE

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → phsj1a\_4

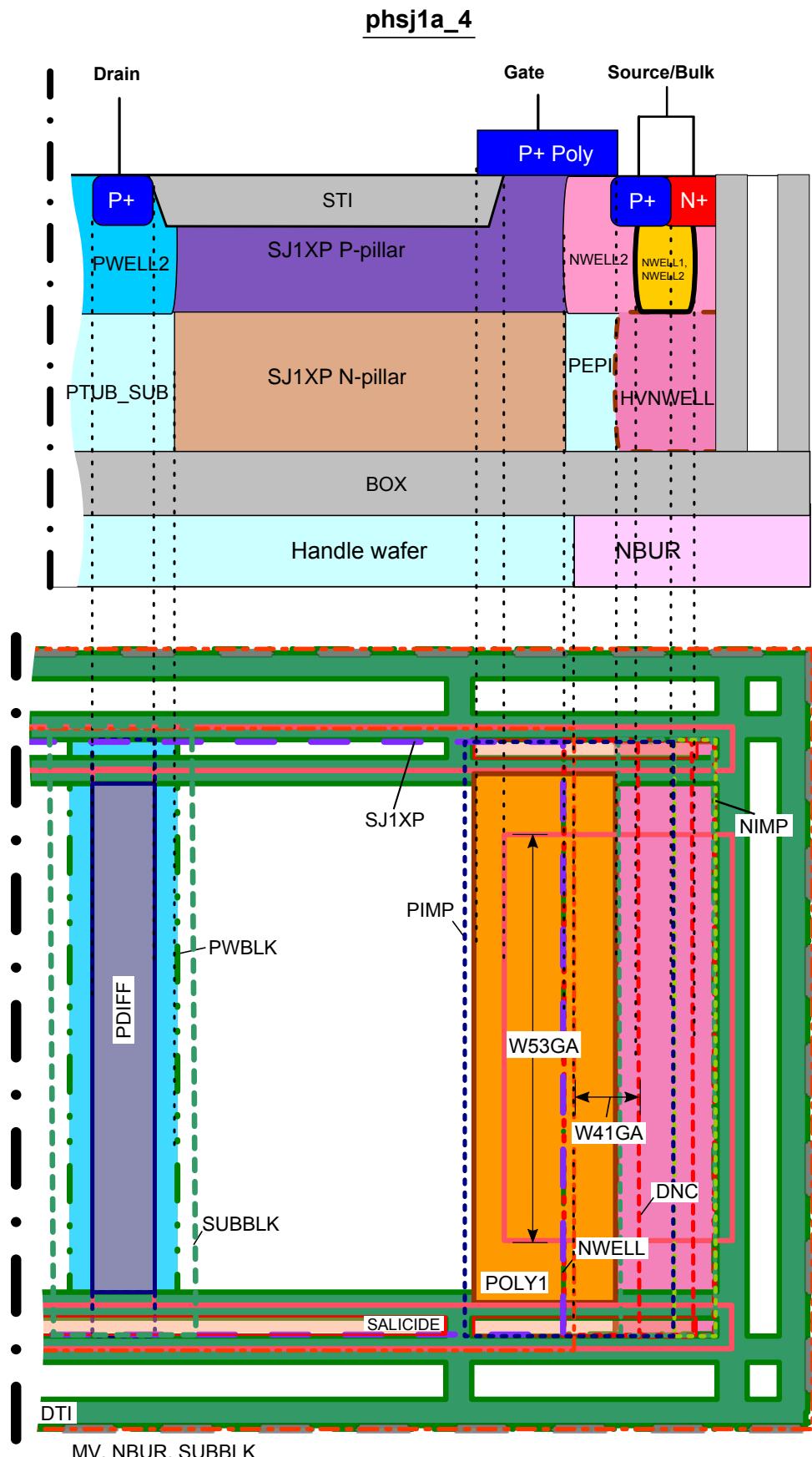


Figure 3.253 phsj1a\_4

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ phsj1a\_5

### **phsj1a\_5**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B6X2	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj1a\_5 device must be labeled "phsj1a\_5" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → phsj1a\_5

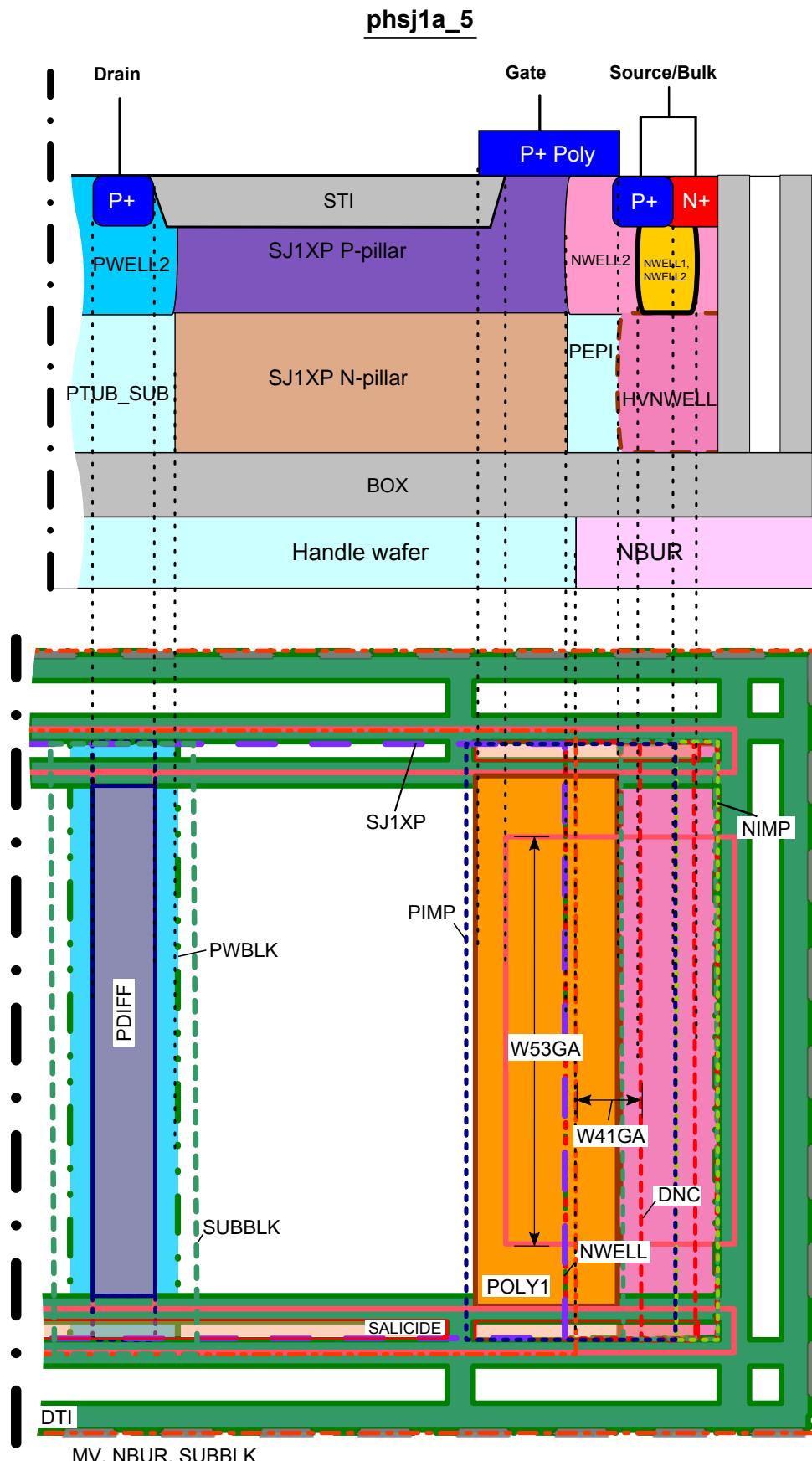


Figure 3.254 phsj1a\_5

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ phsj1a\_7

### **phsj1a\_7**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B6X2	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj1a\_7 device must be labeled "phsj1a\_7" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → phsj1a\_7

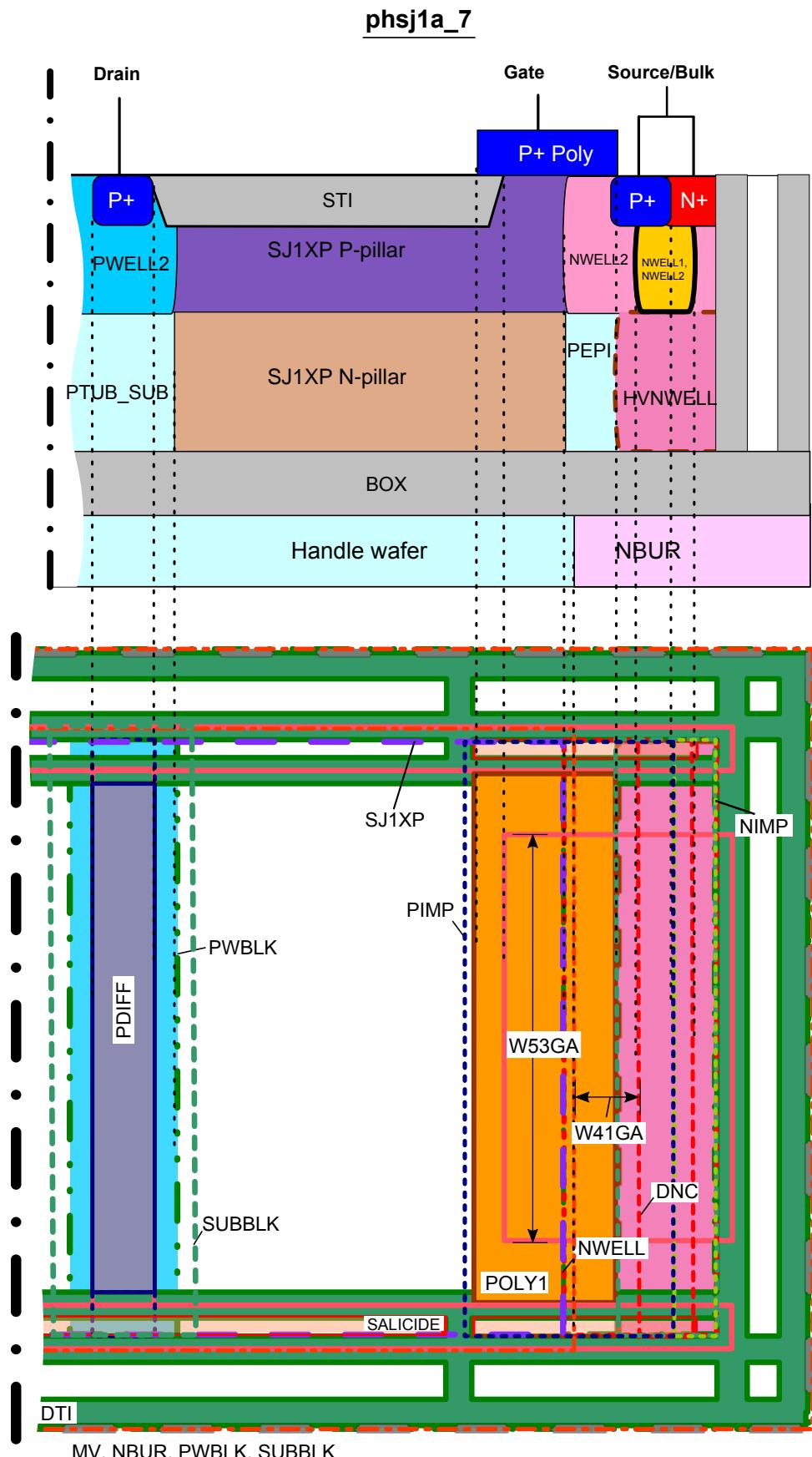


Figure 3.255 phsj1a\_7

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ dfwnsj1b\_2

### **dfwnsj1b\_2**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 11 µm

**Note:** MV is necessary for this device.

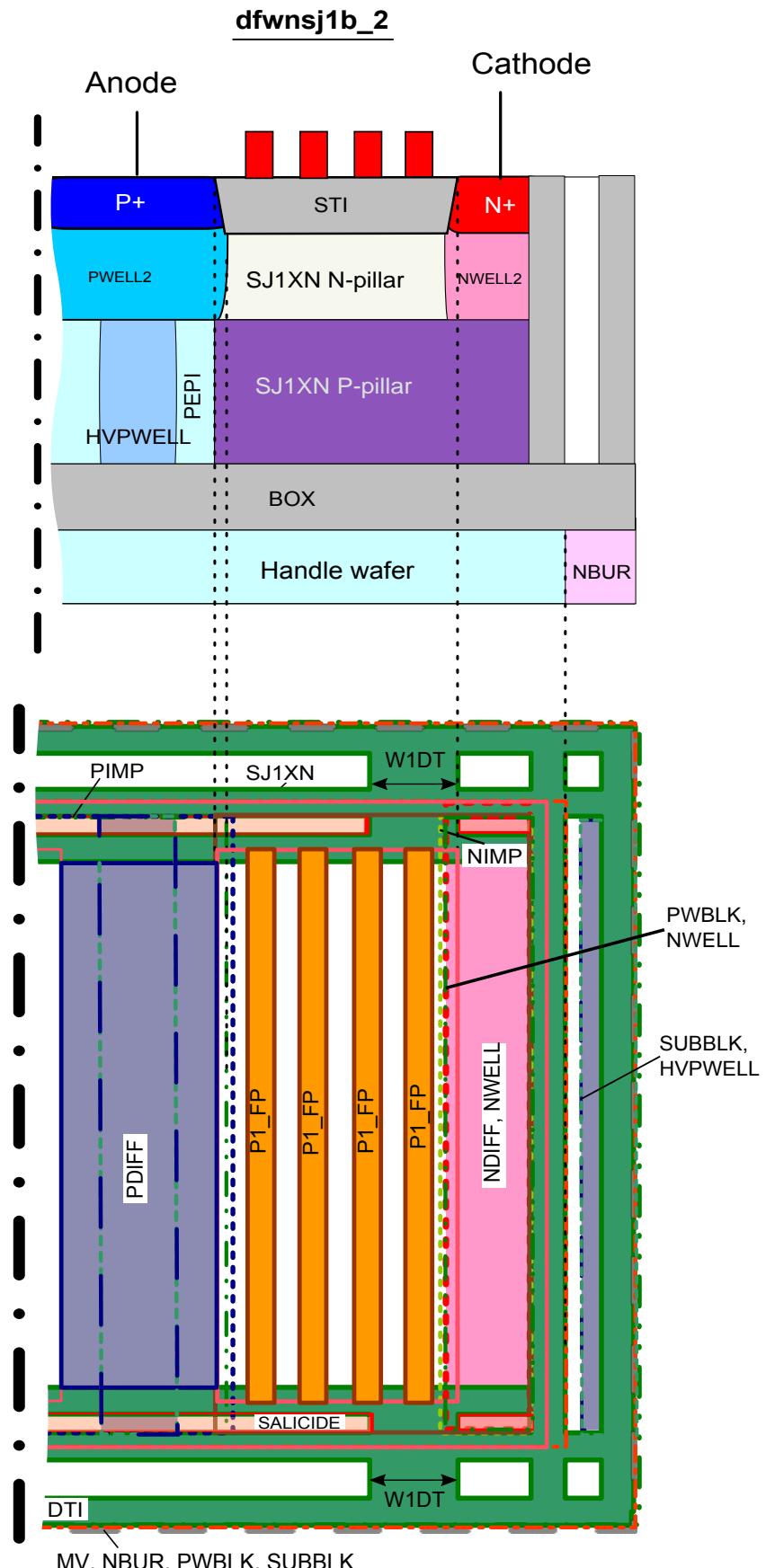
**Note:** dfwnsj1b\_2 device must be labeled "dfwnsj1b\_2" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → dfwnsj1b\_2



**Figure 3.256** dfwnsj1b\_2

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ dfwnsj1b\_4

### **dfwnsj1b\_4**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 11 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_4 device must be labeled "dfwnsj1b\_4" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

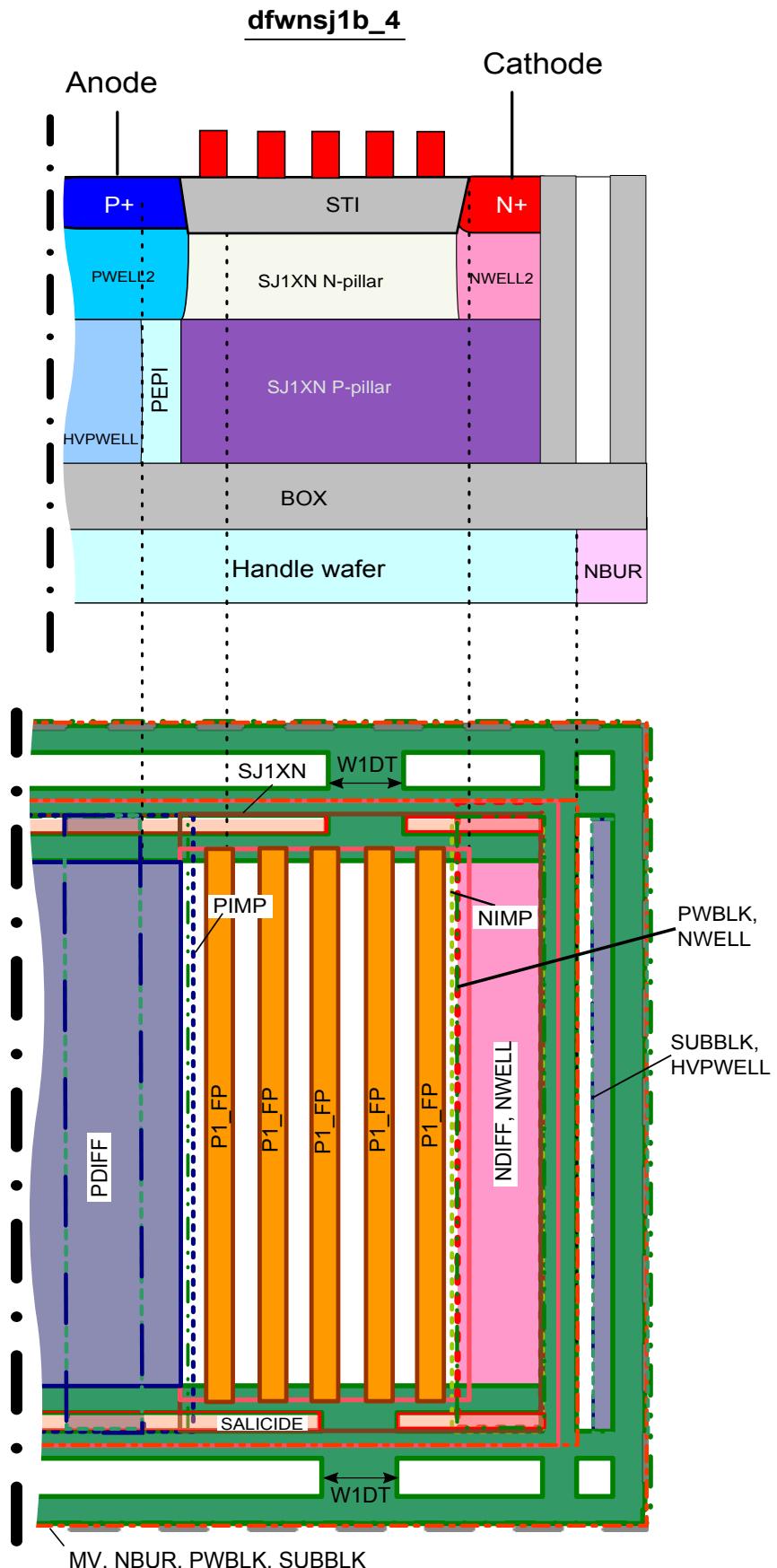
**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → dfwnsj1b\_4



**Figure 3.257** dfwnsj1b\_4

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ dfwnsj1b\_5

### **dfwnsj1b\_5**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 11 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_5 device must be labeled "dfwnsj1b\_5" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → dfwnsj1b\_5

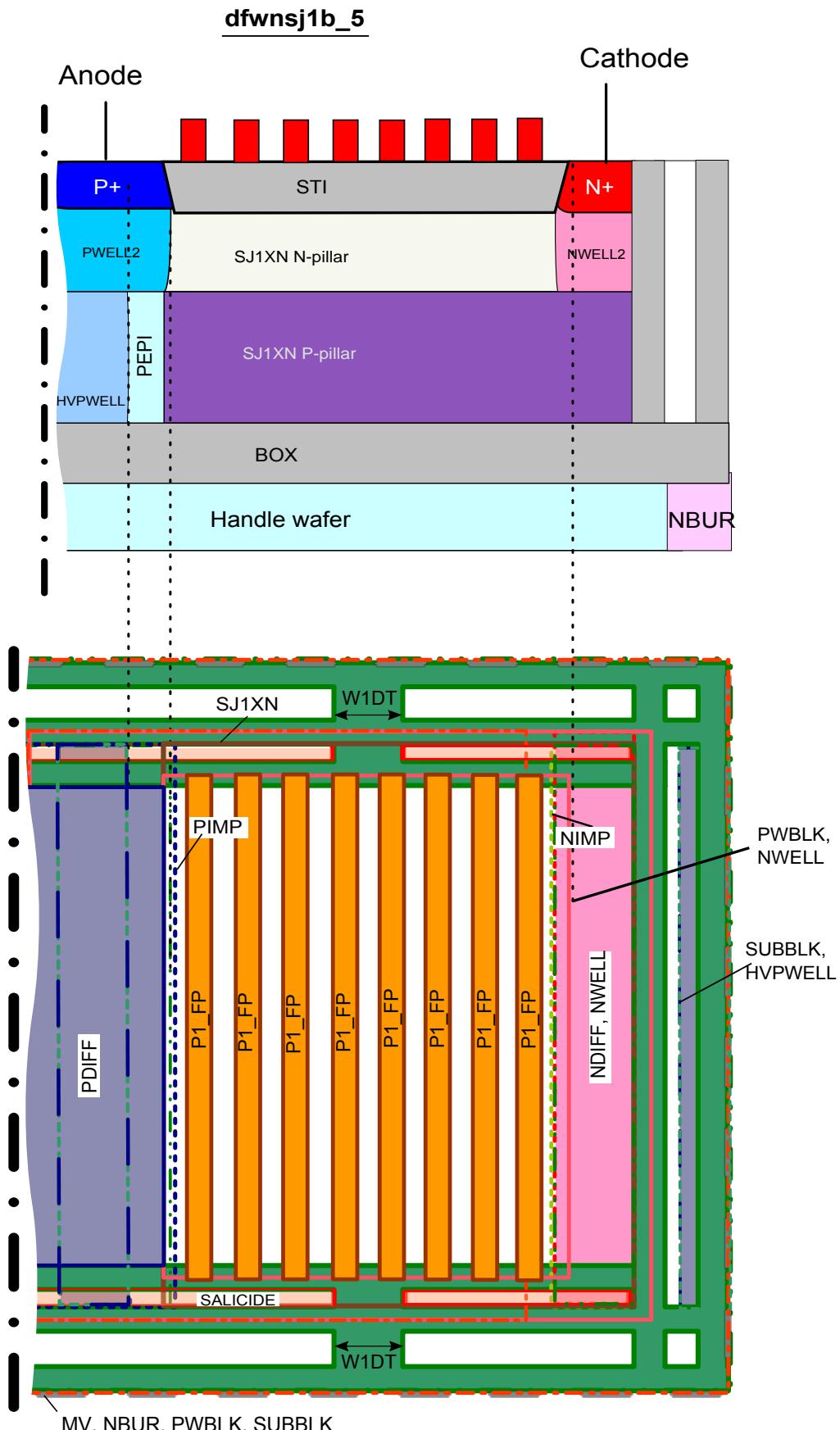


Figure 3.258 dfwnsj1b\_5

3. Layer and Device rules → 3.35 SJHVL module→ 3.35.1 Device rules→ dfwnsj1b\_7

### **dfwnsj1b\_7**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 16 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_7 device must be labeled "dfwnsj1b\_7" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

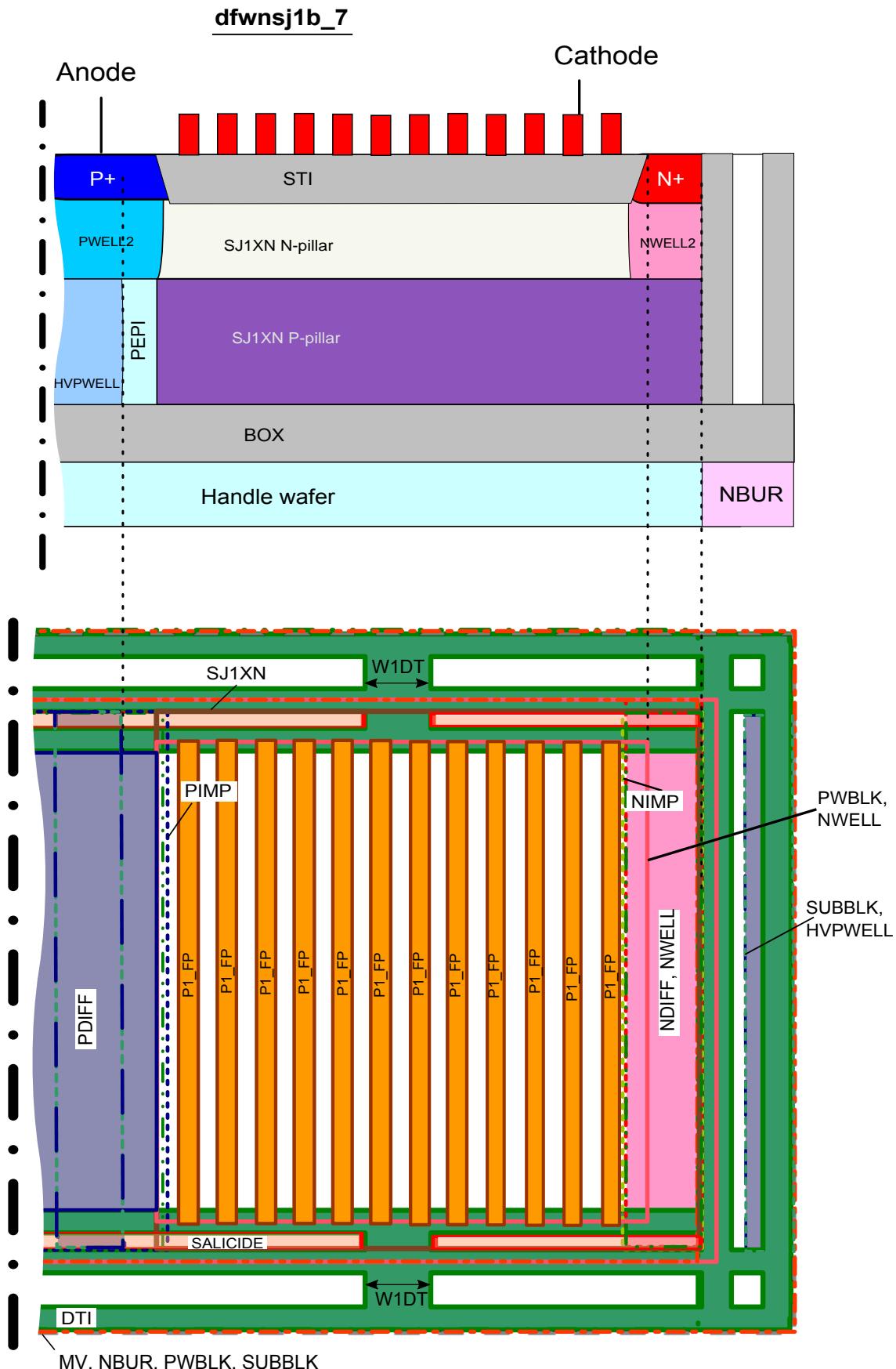
**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.35 SJHVL module → 3.35.1 Device rules → dfwnsj1b\_7



**Figure 3.259** dfwnsj1b\_7

3. Layer and Device rules → 3.36 SJHVM module

## 3.36 SJHVM module

### 3.36.1 Device rules

#### nhsj1b\_8

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)	-	-
<b>Note:</b> Valid only if module MET3 is not selected.			
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
<b>Note:</b> Valid only if module MET3 is selected.			
<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.			
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B7X1	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	µm
W46GA	Minimum GATE width	18.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.			

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_8 device must be labeled "nhsj1b\_8" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1b\_8m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → nhsj1b\_8

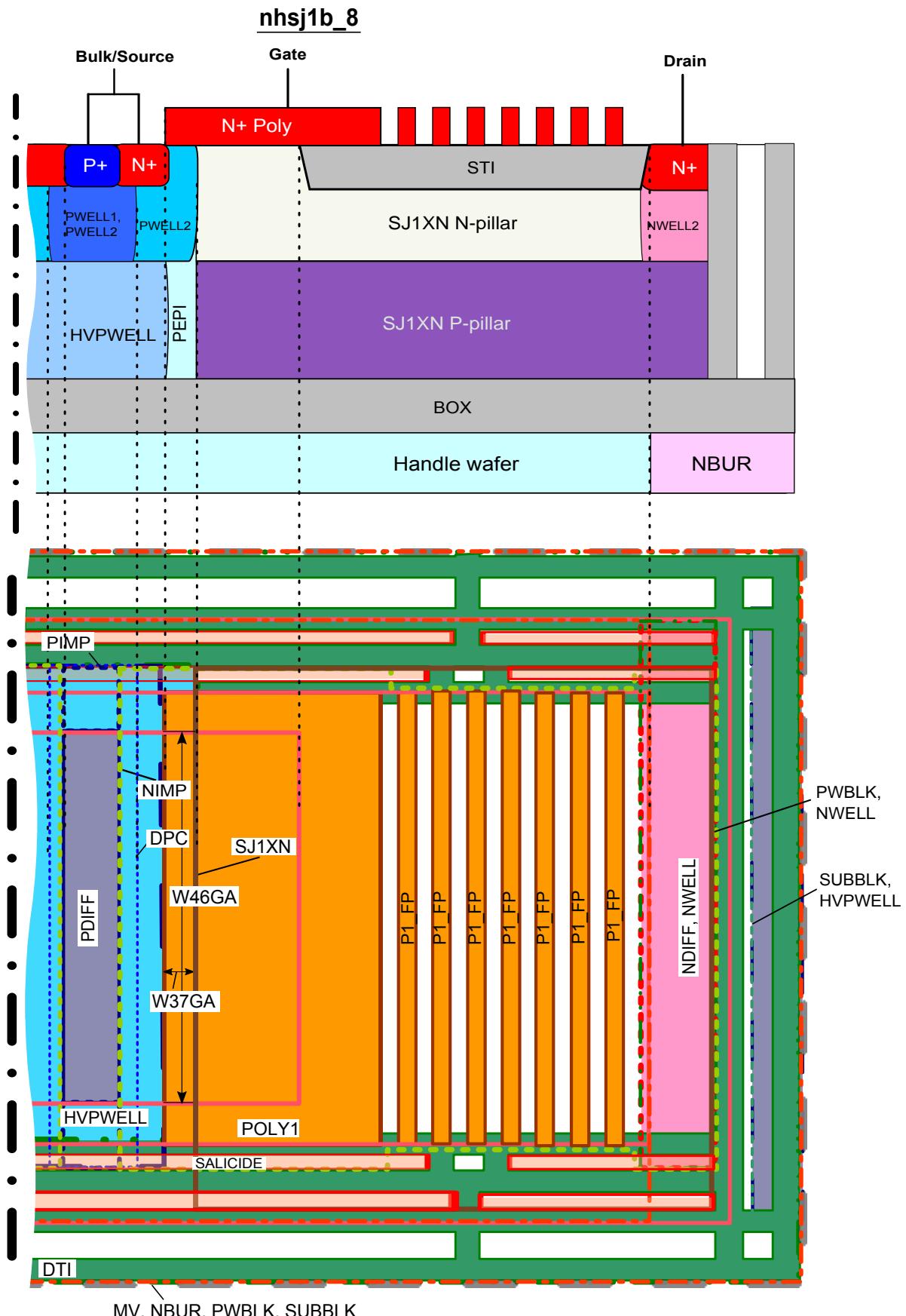


Figure 3.260 nhsj1b\_8

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → nhsj1b\_10

### **nhsj1b\_10**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B7X1	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W47GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	20.0	μm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_10 device must be labeled "nhsj1b\_10" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1b\_10m3" using DEVLBL (VERIFICATION) layer.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → nhsj1b\_10

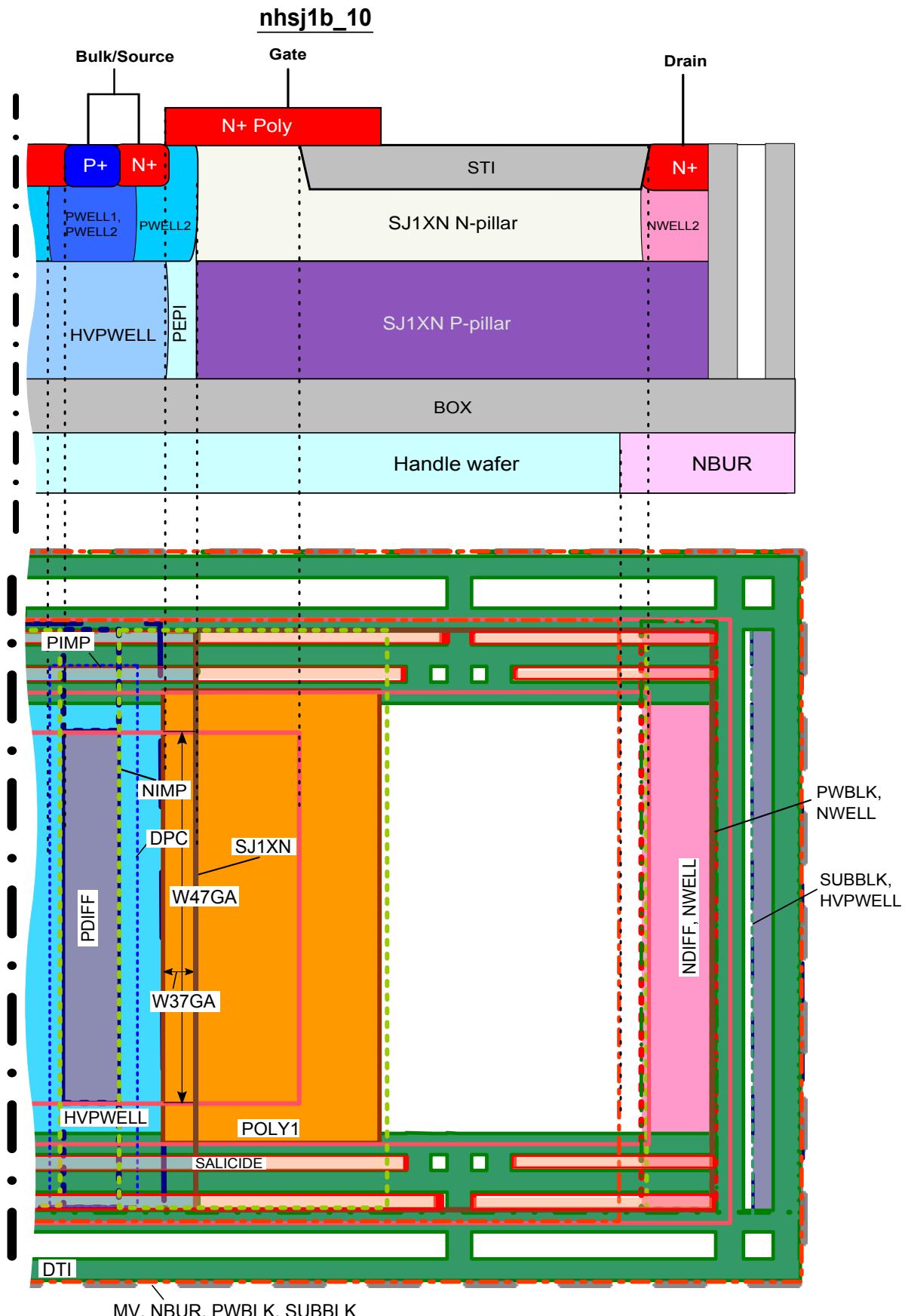


Figure 3.261 nhsj1b\_10

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → nhsj1a\_13

### **nhsj1a\_13**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B8X1	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W49GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	25.0	μm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1a\_13 device must be labeled "nhsj1a\_13" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

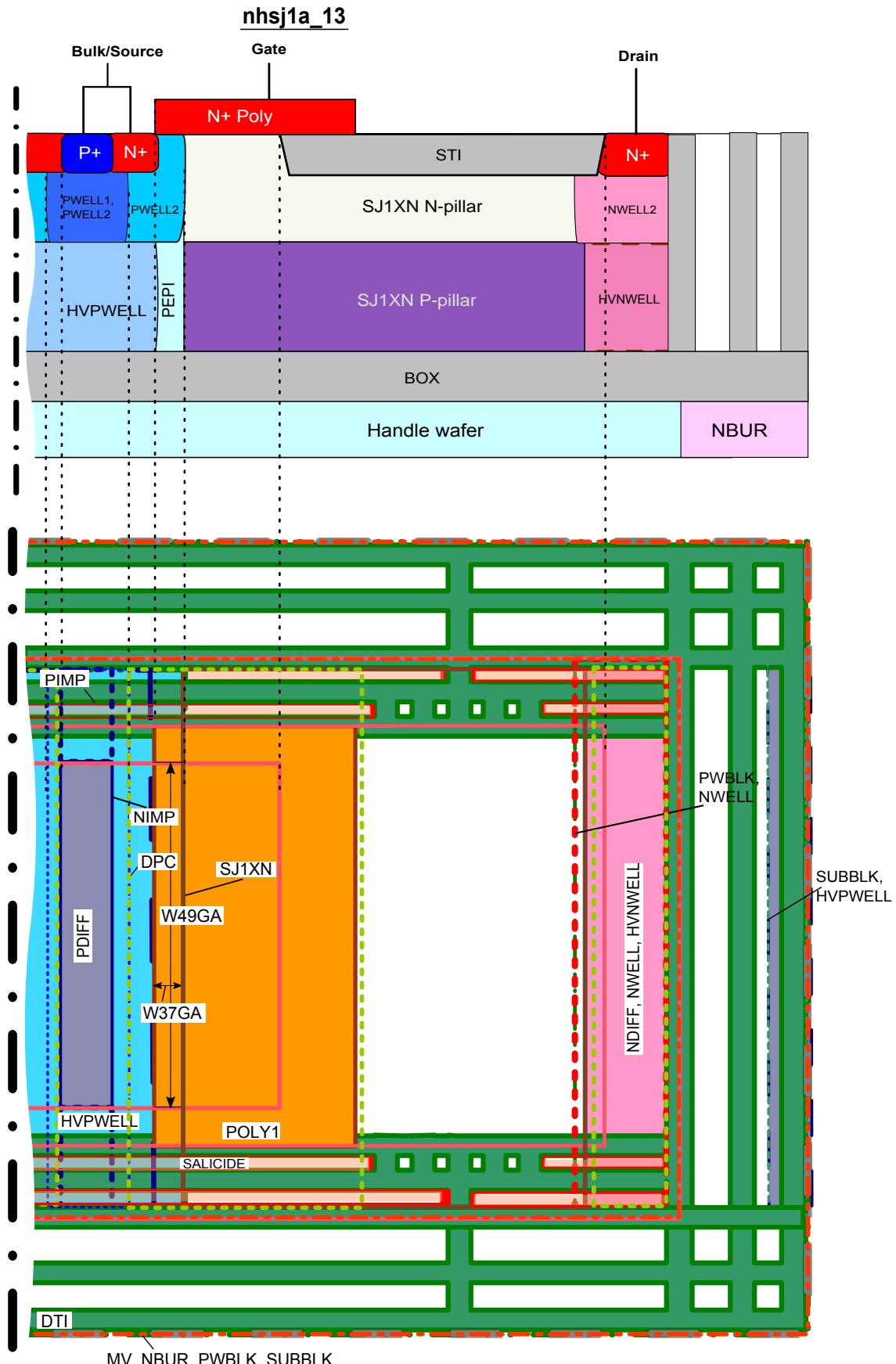
**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1a\_13m3" using DEVLBL (VERIFICATION) layer.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ nhsj1a\_13



**Figure 3.262 nhsj1a\_13**

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → nhsj1a\_16

### **nhsj1a\_16**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B9X1	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W50GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	30.0	μm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1a\_16 device must be labeled "nhsj1a\_16" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1a\_16m3" using DEVLBL (VERIFICATION) layer.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

## 3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ nhsj1a\_16

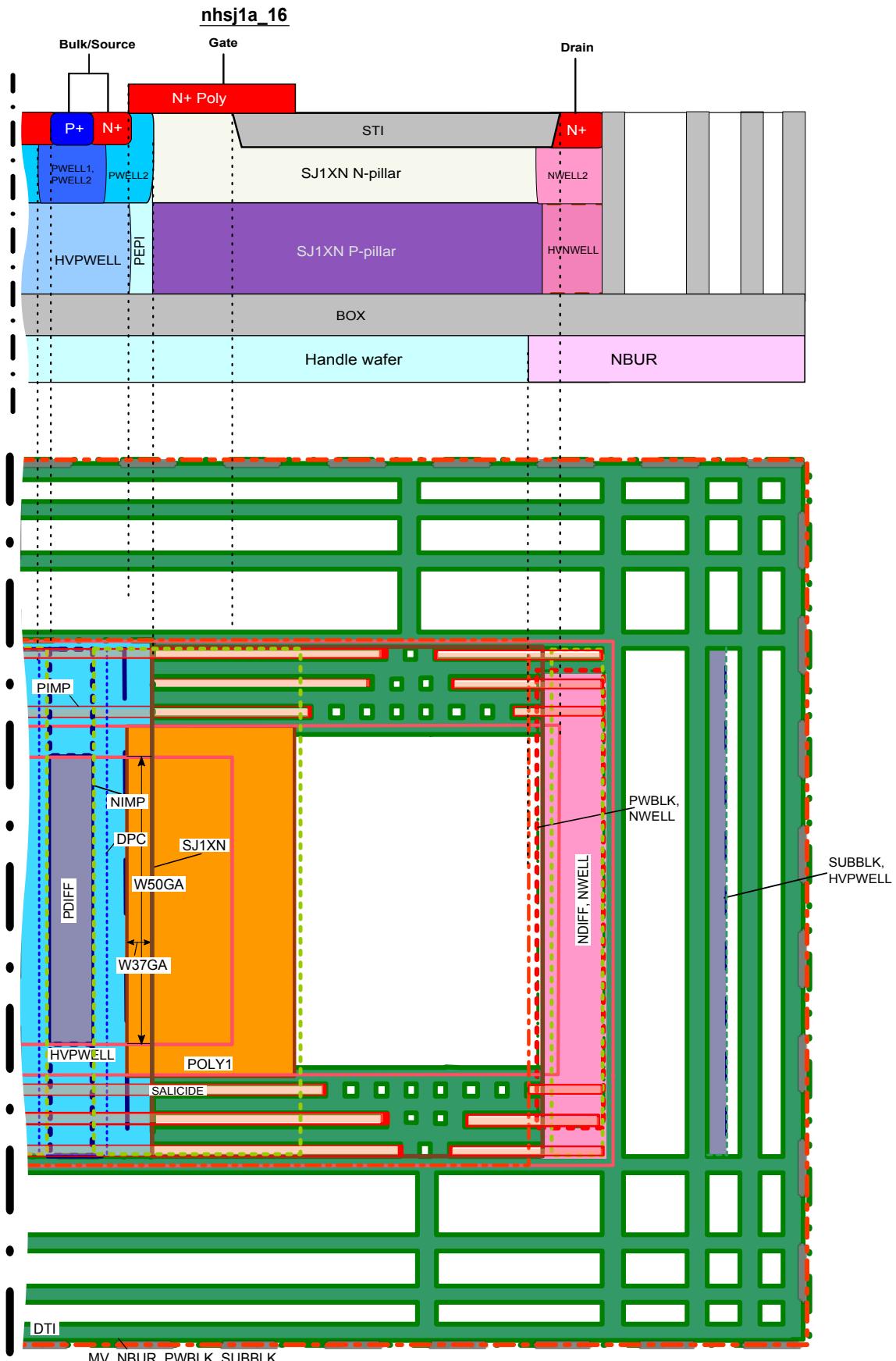


Figure 3.263 nhsj1a\_16

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj2b\_8

## **phsj2b\_8**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B15X4	METTP, METTPL are not allowed over SJ2XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X4	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ2XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
B9X4	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W61GA	Fixed CHANNEL length	0.5	μm
W63GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	μm

**Note:** phsj2b\_8 device must be labeled "phsj2b\_8" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

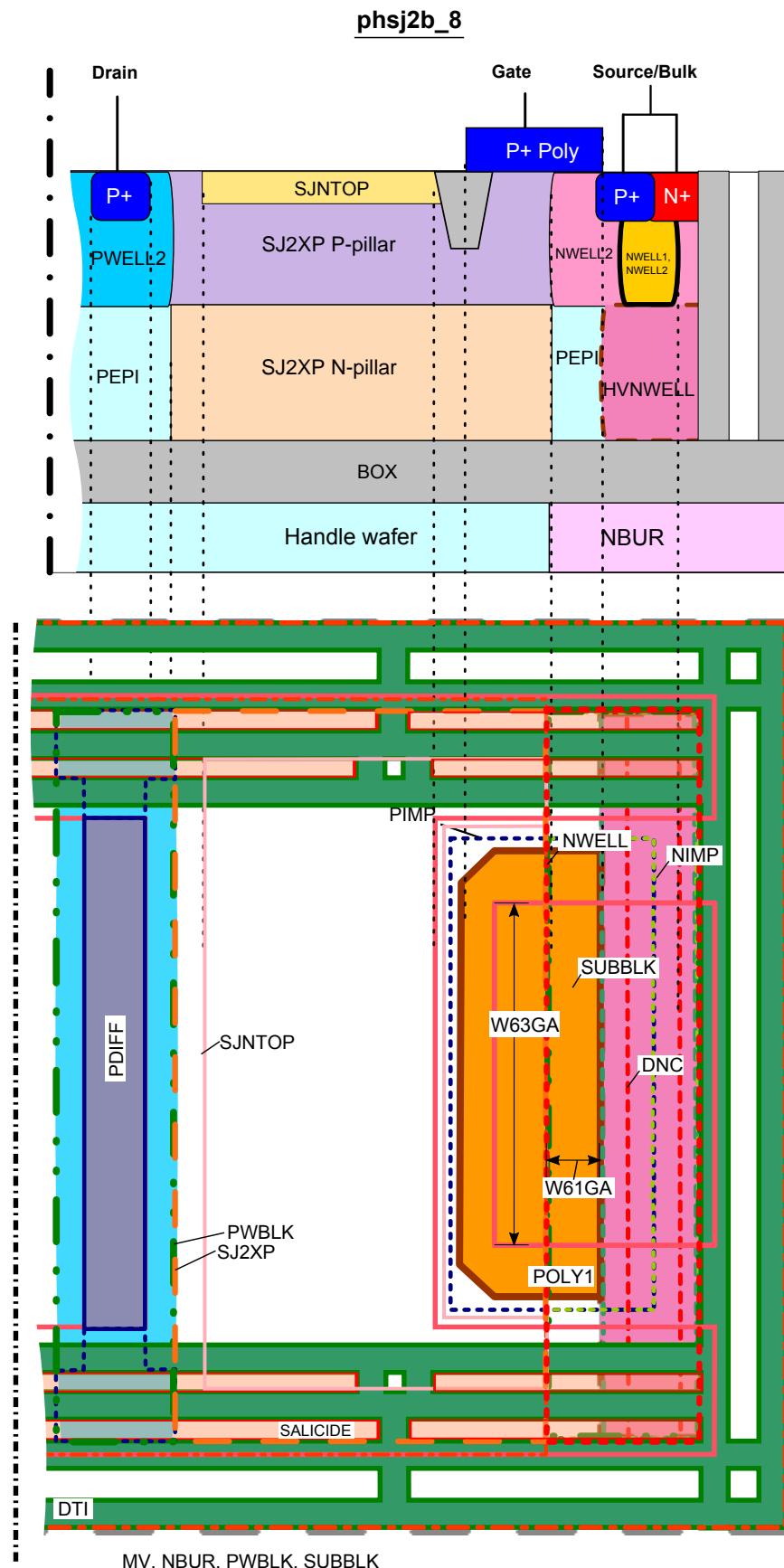
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj2b\_8m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj2b\_8



**Figure 3.264 phsj2b\_8**

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → phsj2b\_10

### **phsj2b\_10**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B15X4	METTP, METTPL are not allowed over SJ2XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X4	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ2XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
B9X4	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W61GA	Fixed CHANNEL length	0.5	μm
W63GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	μm

**Note:** phsj2b\_10 device must be labeled "phsj2b\_10" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

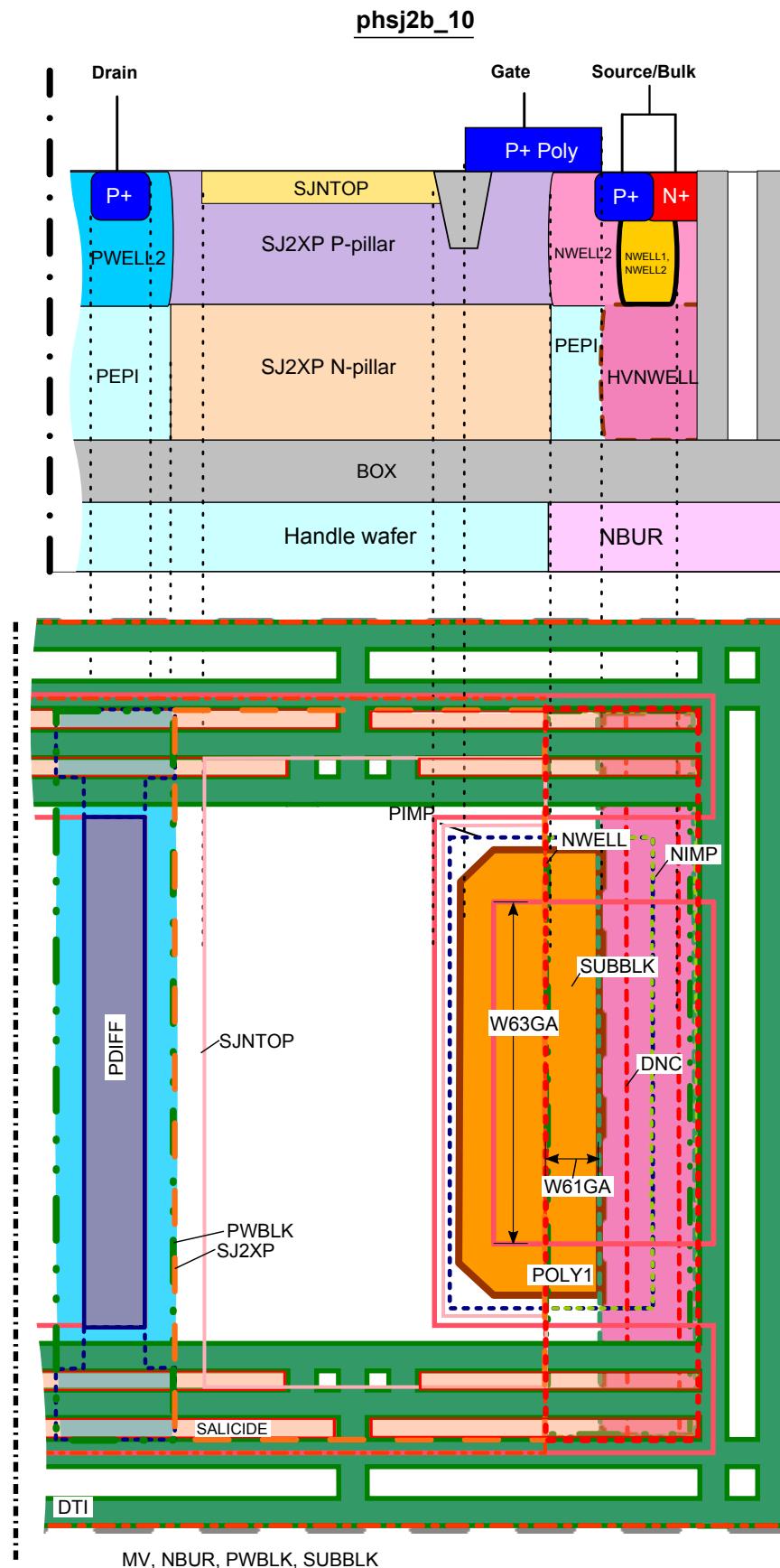
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj2b\_10m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj2b\_10



**Figure 3.265 phsj2b\_10**

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → phsj2b\_13

### **phsj2b\_13**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10X4	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B15X4	METTP, METTPL are not allowed over SJ2XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X4	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ2XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
W61GA	Fixed CHANNEL length	0.5	µm
W64GA	Minimum GATE width	25.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj2b\_13 device must be labeled "phsj2b\_13" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

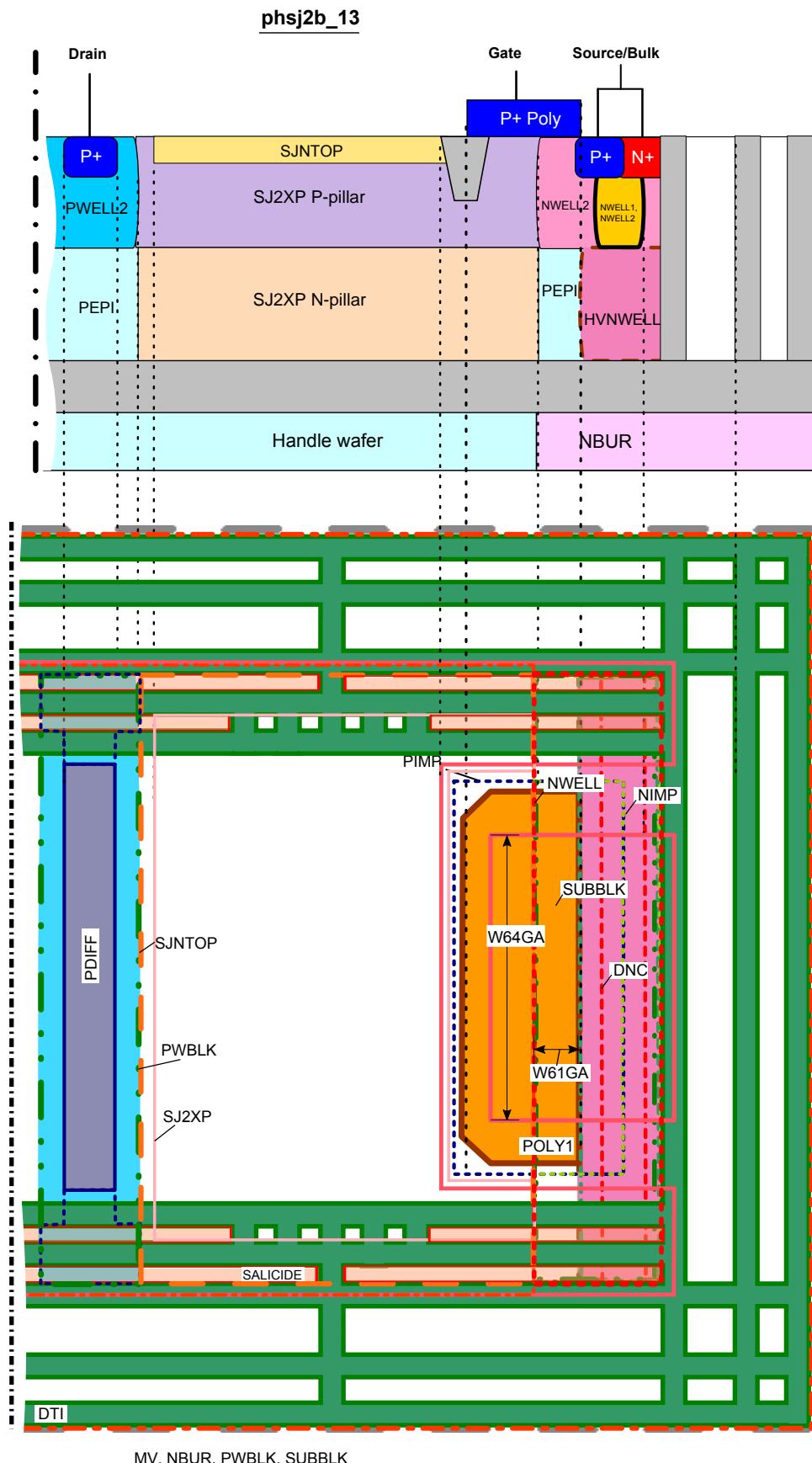
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj2b\_13m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj2b\_13



**Figure 3.266 phsj2b\_13**

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → phsj2b\_16

### **phsj2b\_16**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11X4	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
B13X4	MET2 is not allowed over SJ2XP (except predefined MET2 device terminal connections)	-	-
B15X4	METTP, METTPL are not allowed over SJ2XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X4	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ2XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B7X4	Fixed orientation is 0 degree or 180 degree	-	-
W61GA	Fixed CHANNEL length	0.5	µm
W65GA	Minimum GATE width	30.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj2b\_16 device must be labeled "phsj2b\_16" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

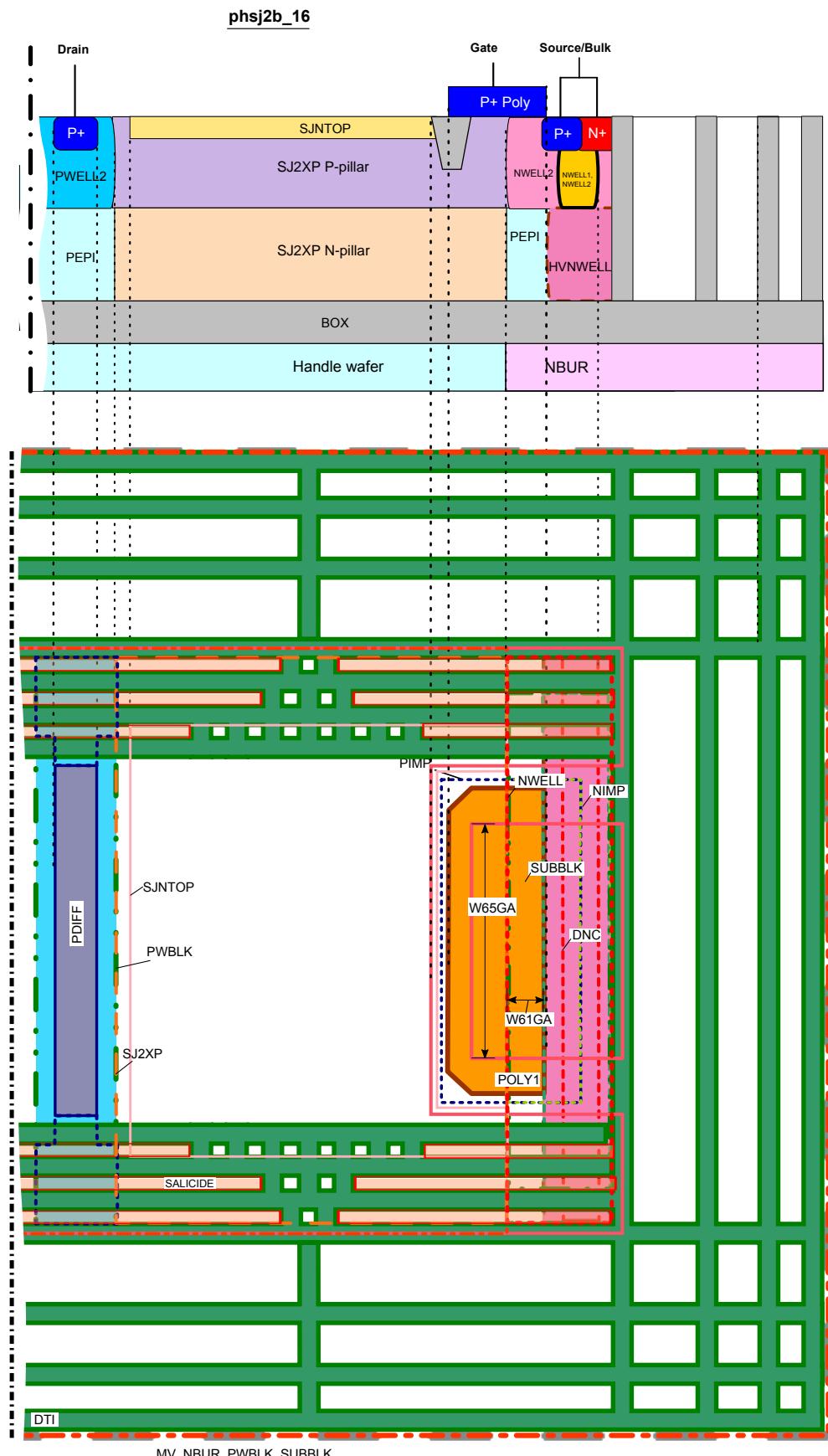
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj2b\_16m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj2b\_16

**Figure 3.267 phsj2b\_16**

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj1a\_8

### **phsj1a\_8**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B7X2	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj1a\_8 device must be labeled "phsj1a\_8" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_8m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj1a\_8

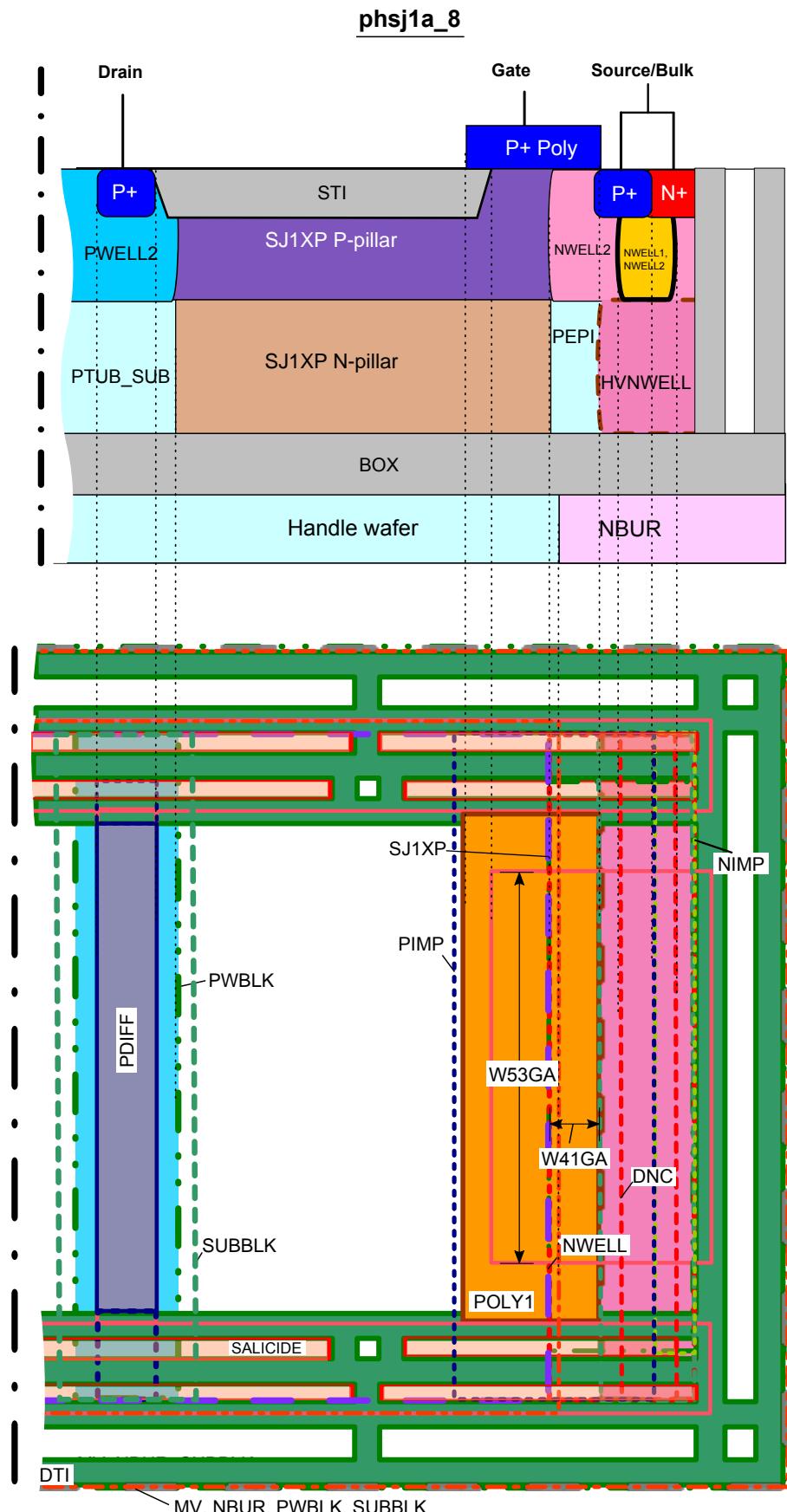


Figure 3.268 phsj1a\_8

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → phsj1a\_10

### **phsj1a\_10**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B7X2	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	μm

**Note:** phsj1a\_10 device must be labeled "phsj1a\_10" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_10m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj1a\_10

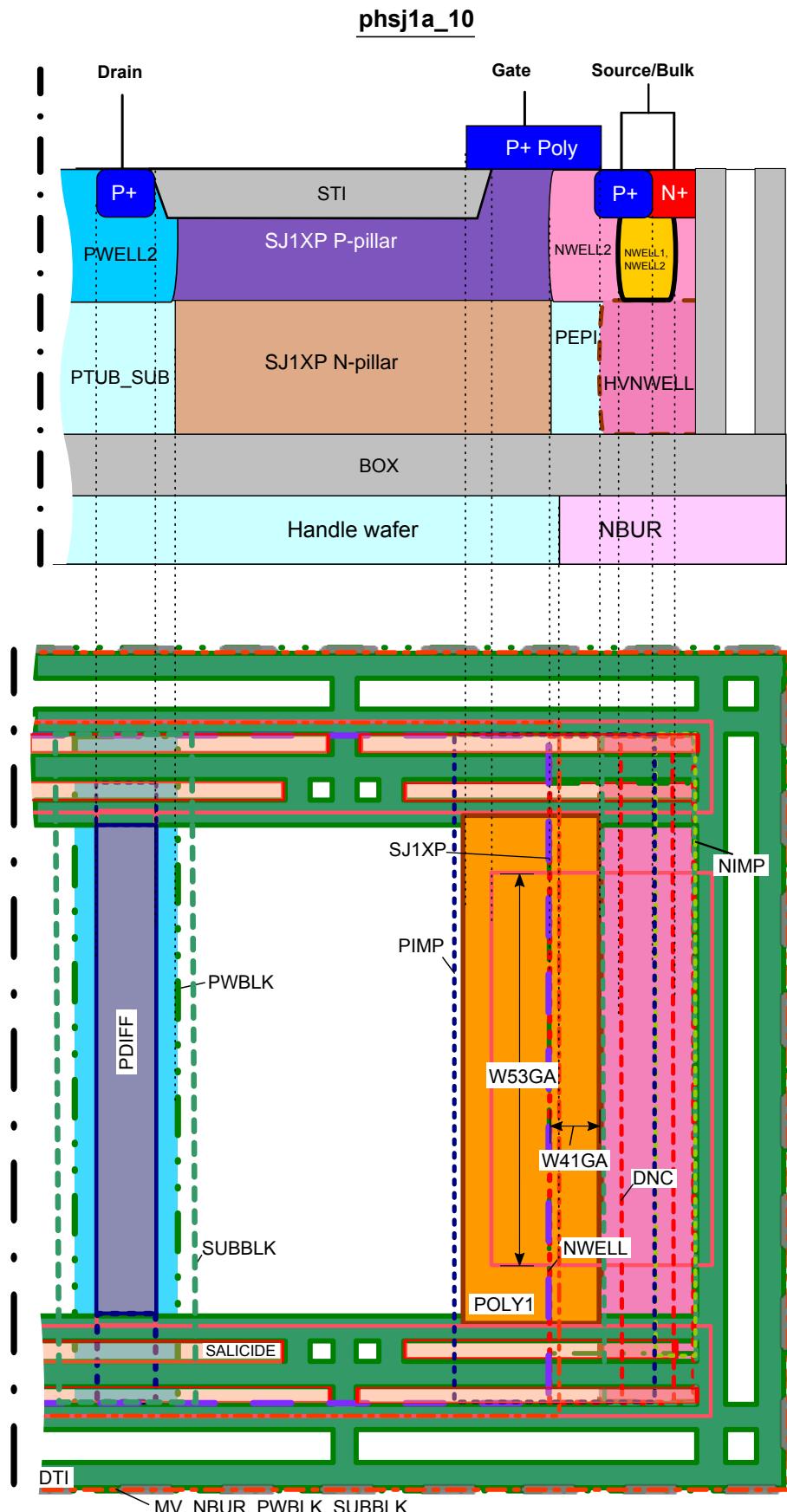


Figure 3.269 phsj1a\_10

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj1a\_13

### **phsj1a\_13**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B8X2	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W54GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	25.0	μm

**Note:** phsj1a\_13 device must be labeled "phsj1a\_13" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

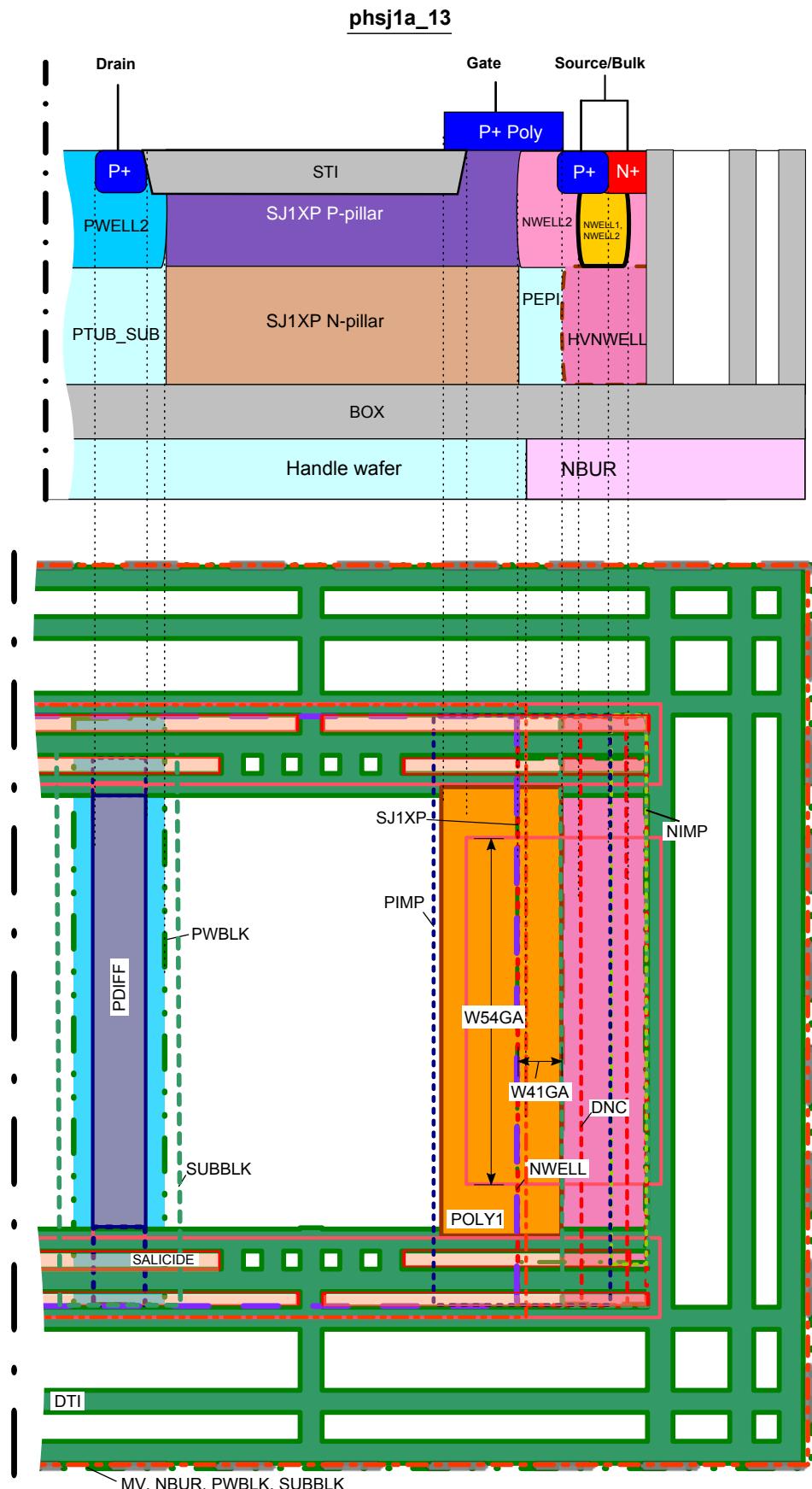
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_13m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj1a\_13

**Figure 3.270 phsj1a\_13**

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → phsj1a\_16

### **phsj1a\_16**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B9X2	This device must be used together with a dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W55GA	Minimum GATE width	30.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** phsj1a\_16 device must be labeled "phsj1a\_16" using POLY1 (VERIFICATION) layer over GATE

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_16m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ phsj1a\_16

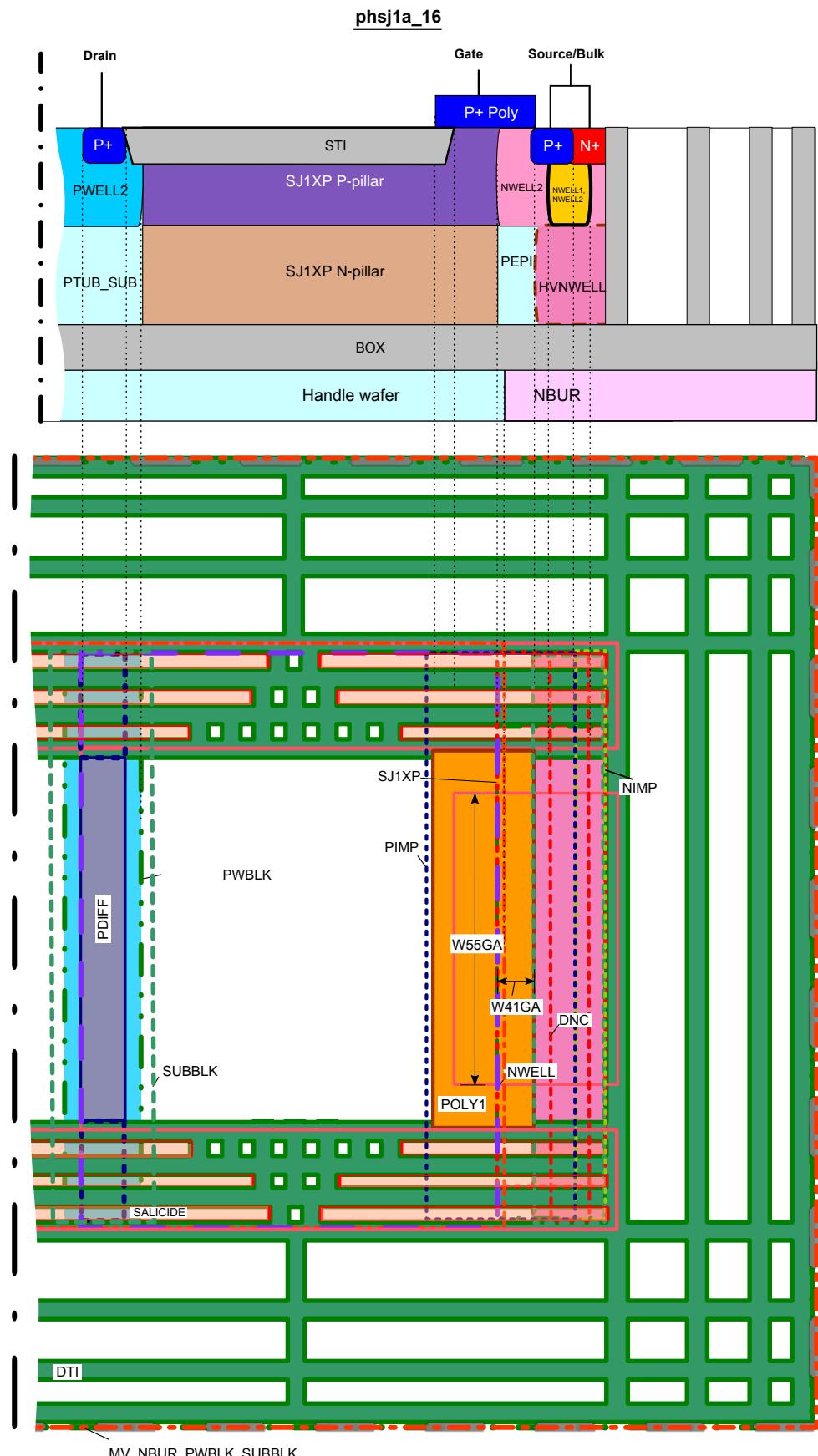


Figure 3.271 phsj1a\_16

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ dfwnsj1b\_8

### **dfwnsj1b\_8**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B7X1	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 19 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_8 device must be labeled "dfwnsj1b\_8" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1b\_8m3" using DEVLBL (VERIFICATION) layer.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → dfwnsj1b\_8

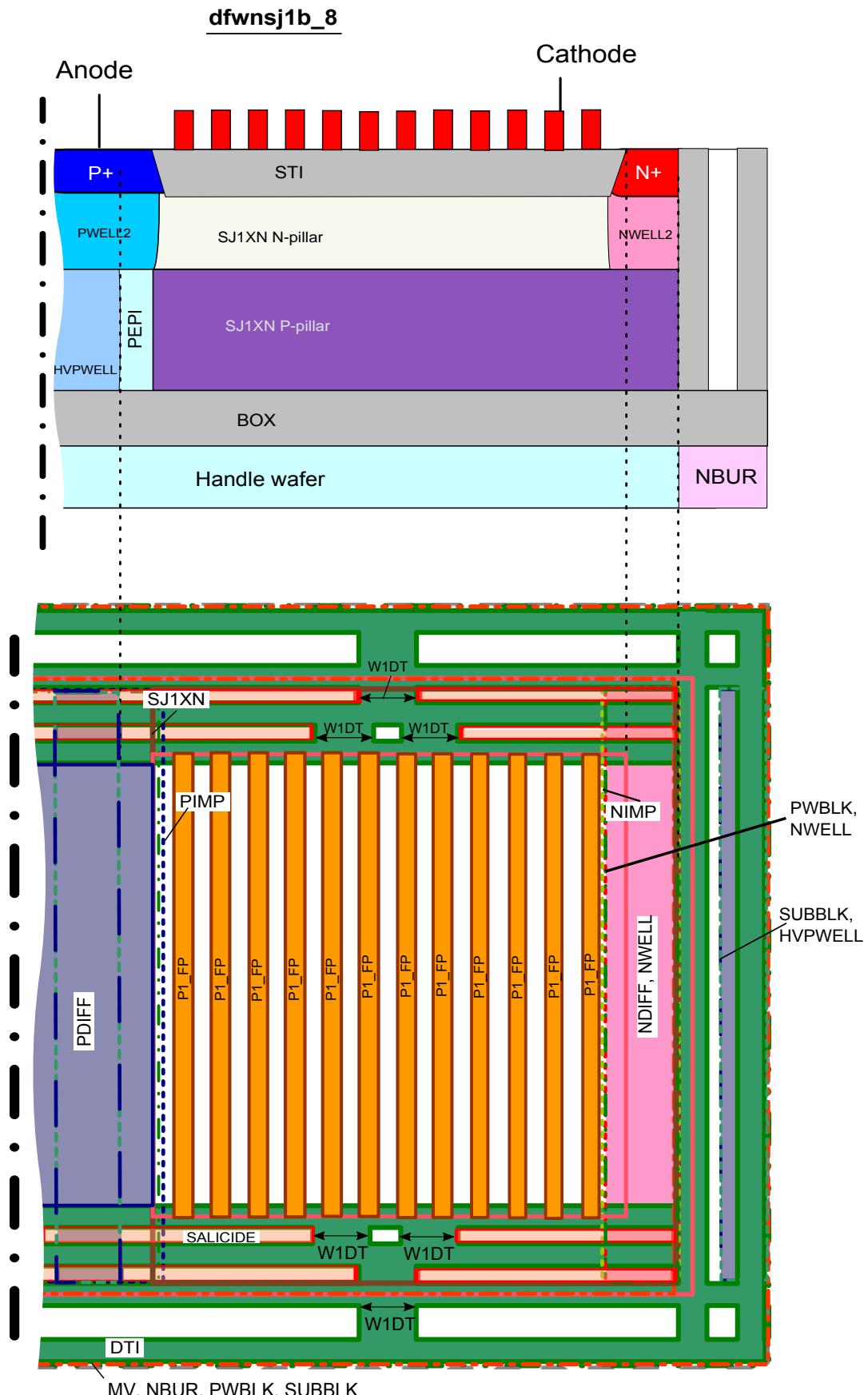


Figure 3.272 dfwnsj1b\_8

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → dfwnsj1b\_10

### **dfwnsj1b\_10**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B7X1	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 21 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_10 device must be labeled "dfwnsj1b\_10" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

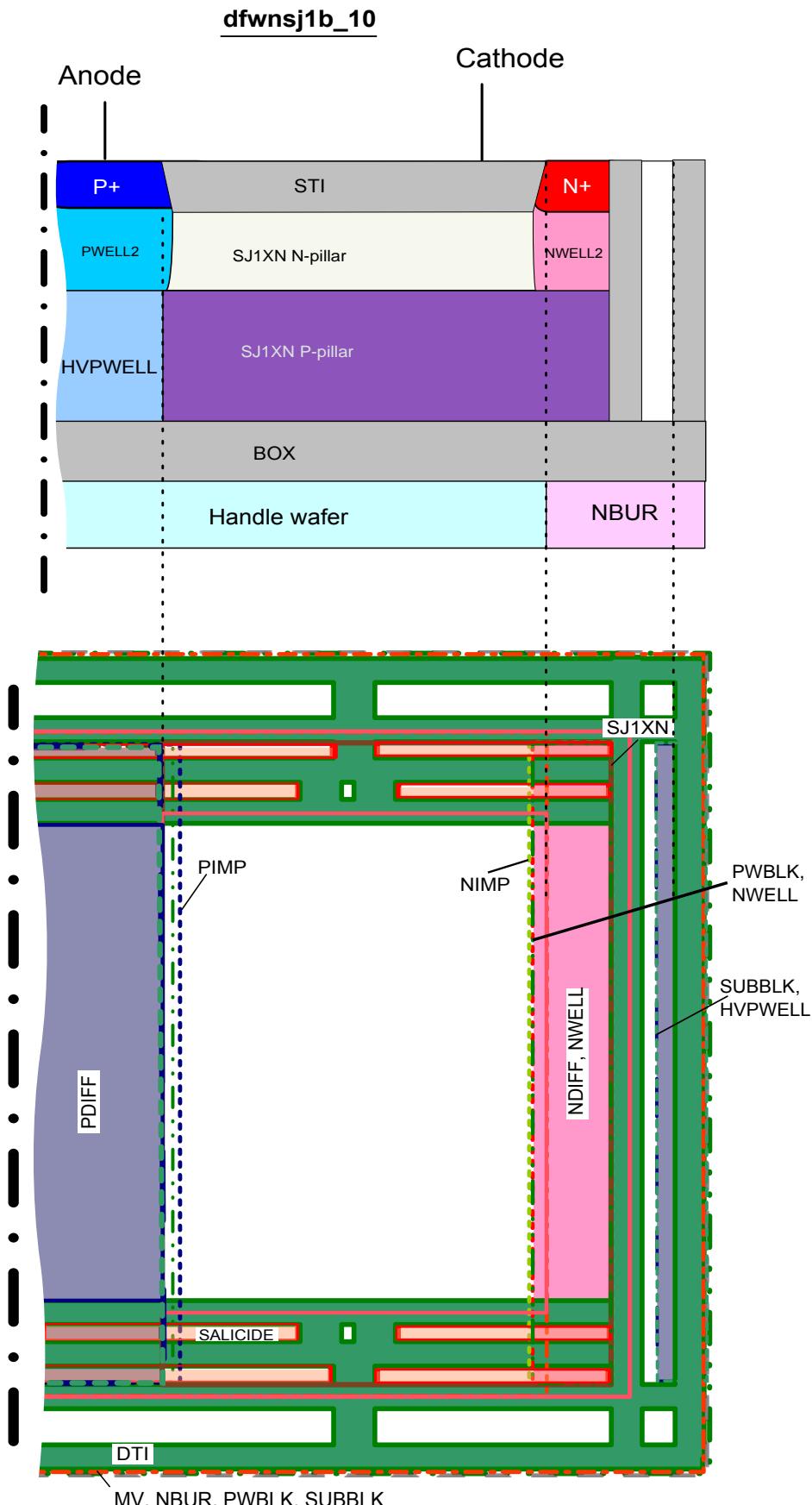
**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1b\_10m3" using DEVLBL (VERIFICATION) layer.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → dfwnsj1b\_10



**Figure 3.273 dfwnsj1b\_10**

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → dfwnsj1a\_13

### **dfwnsj1a\_13**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B8X1	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 26 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1a\_13 device must be labeled "dfwnsj1a\_13" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

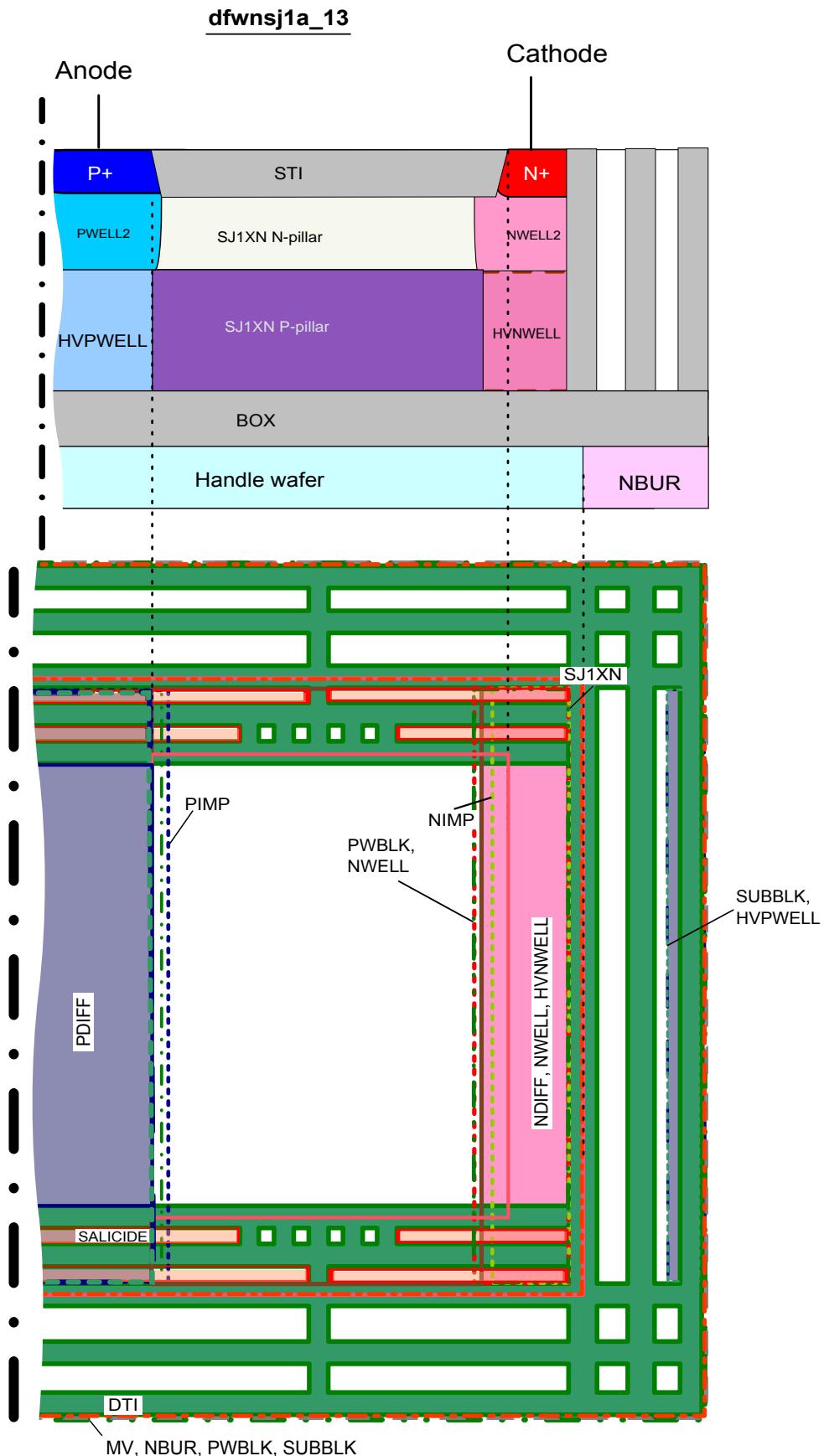
**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1a\_13m3" using DEVLBL (VERIFICATION) layer.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → dfwnsj1a\_13



**Figure 3.274 dfwnsj1a\_13**

3. Layer and Device rules → 3.36 SJHVM module → 3.36.1 Device rules → dfwnsj1a\_16

### **dfwnsj1a\_16**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B9X1	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 31 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1a\_16 device must be labeled "dfwnsj1a\_16" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

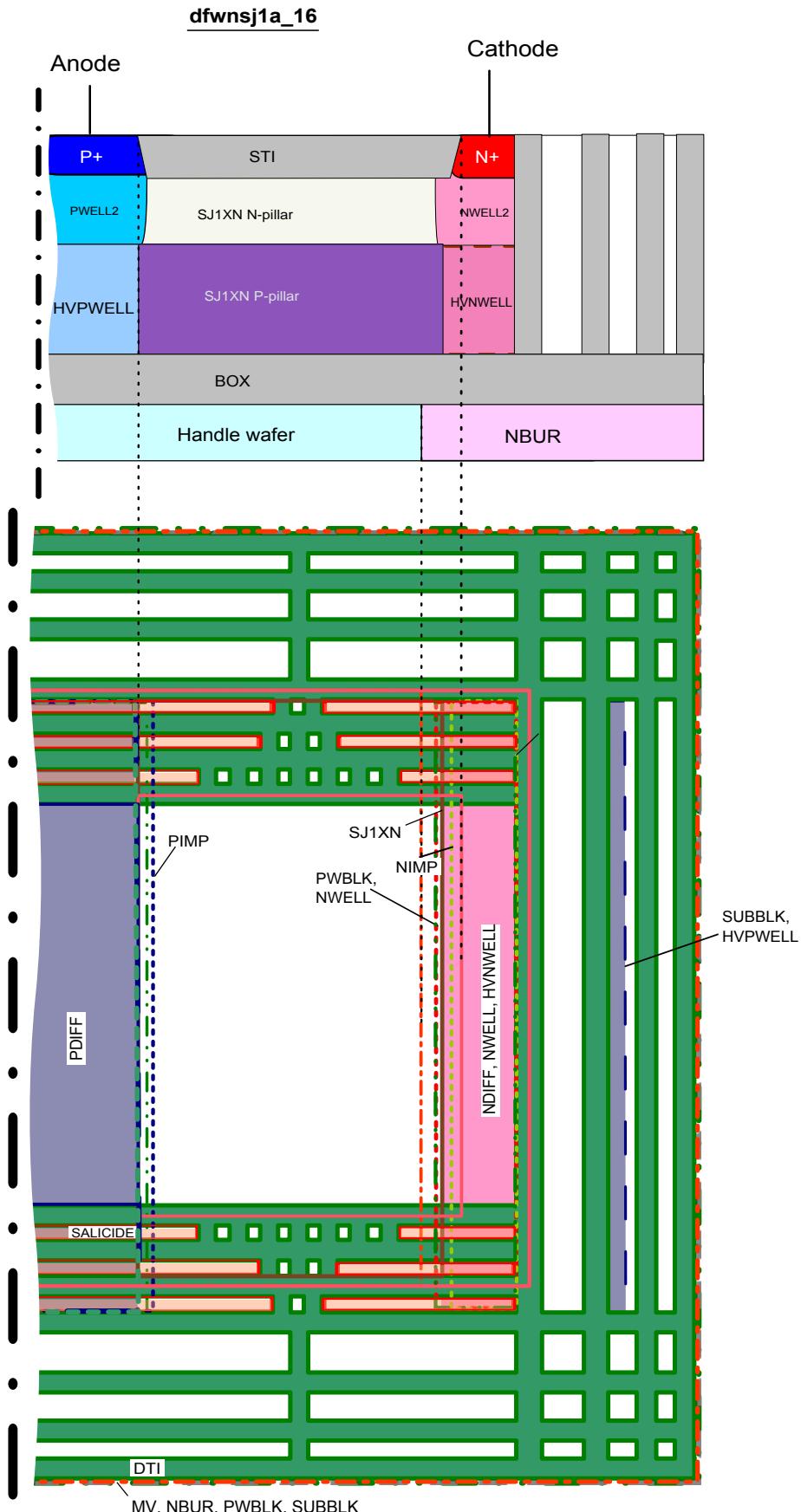
**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1a\_16m3" using DEVLBL (VERIFICATION) layer.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.36 SJHVM module→ 3.36.1 Device rules→ dfwnsj1a\_16



**Figure 3.275** dfwnsj1a\_16

3. Layer and Device rules → 3.37 SJHVU module

## 3.37 SJHVU module

### 3.37.1 Device rules

#### nhsj1a\_20

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10X1	This device must be used together with a dhw4d or dhw5d	-	-
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B14X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.		
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
W37GA	Fixed CHANNEL length	0.5	µm
W51GA	Minimum GATE width	40.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1a\_20 device must be labeled "nhsj1a\_20" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

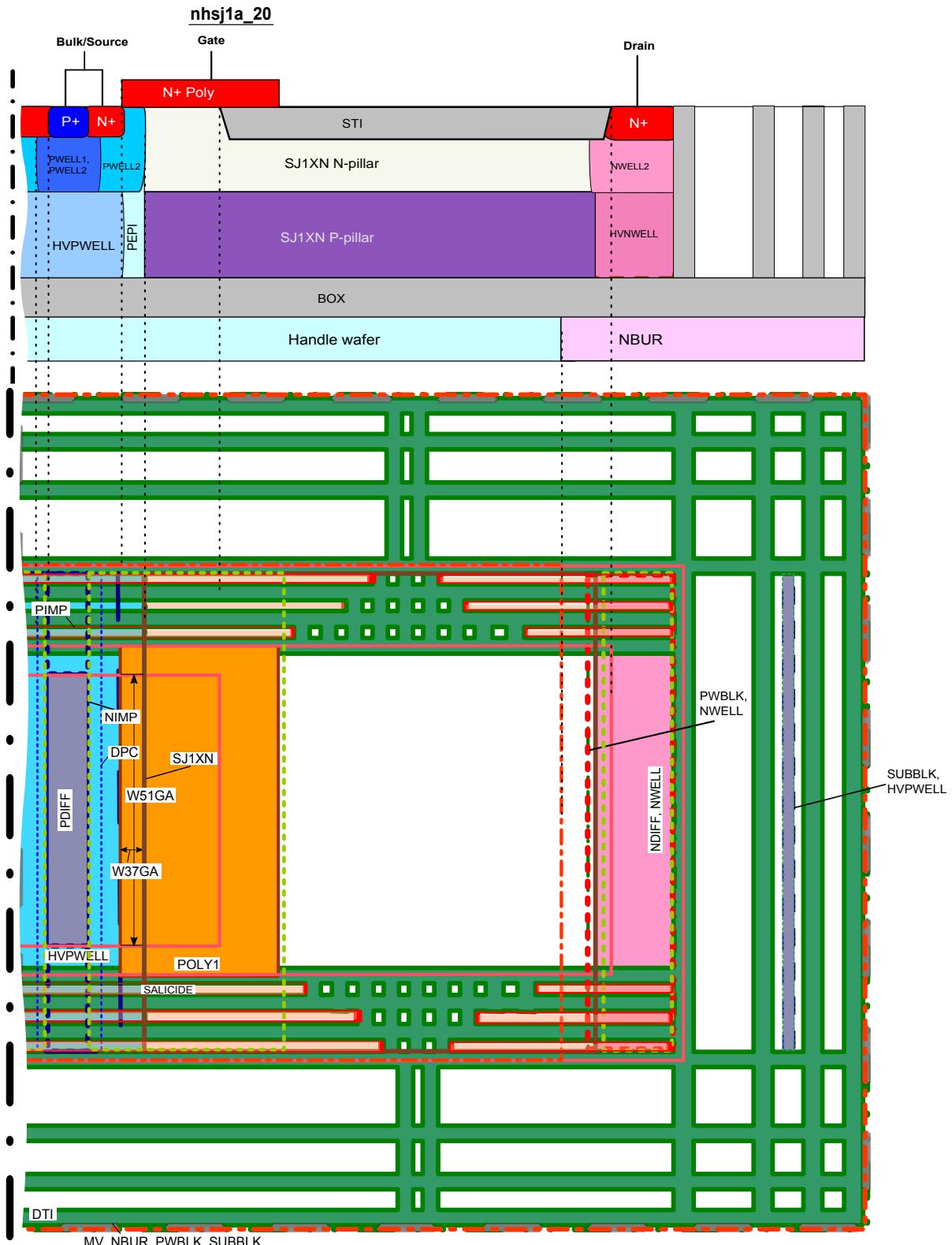
**Note:** NBUR connection to dhw4d or dhw5d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1a\_20m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.37 SJHVU module→ 3.37.1 Device rules→ nhsj1a\_20

**Figure 3.276 nhsj1a\_20**

3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → nhsj1a\_28

### **nhsj1a\_28**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11X1	This device must be used together with dhw5d	-	-
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B14X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
W37GA	Fixed CHANNEL length	0.5	µm
W52GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	60.0	µm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1a\_28 device must be labeled "nhsj1a\_28" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw5d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1a\_28m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → nhsj1a\_28

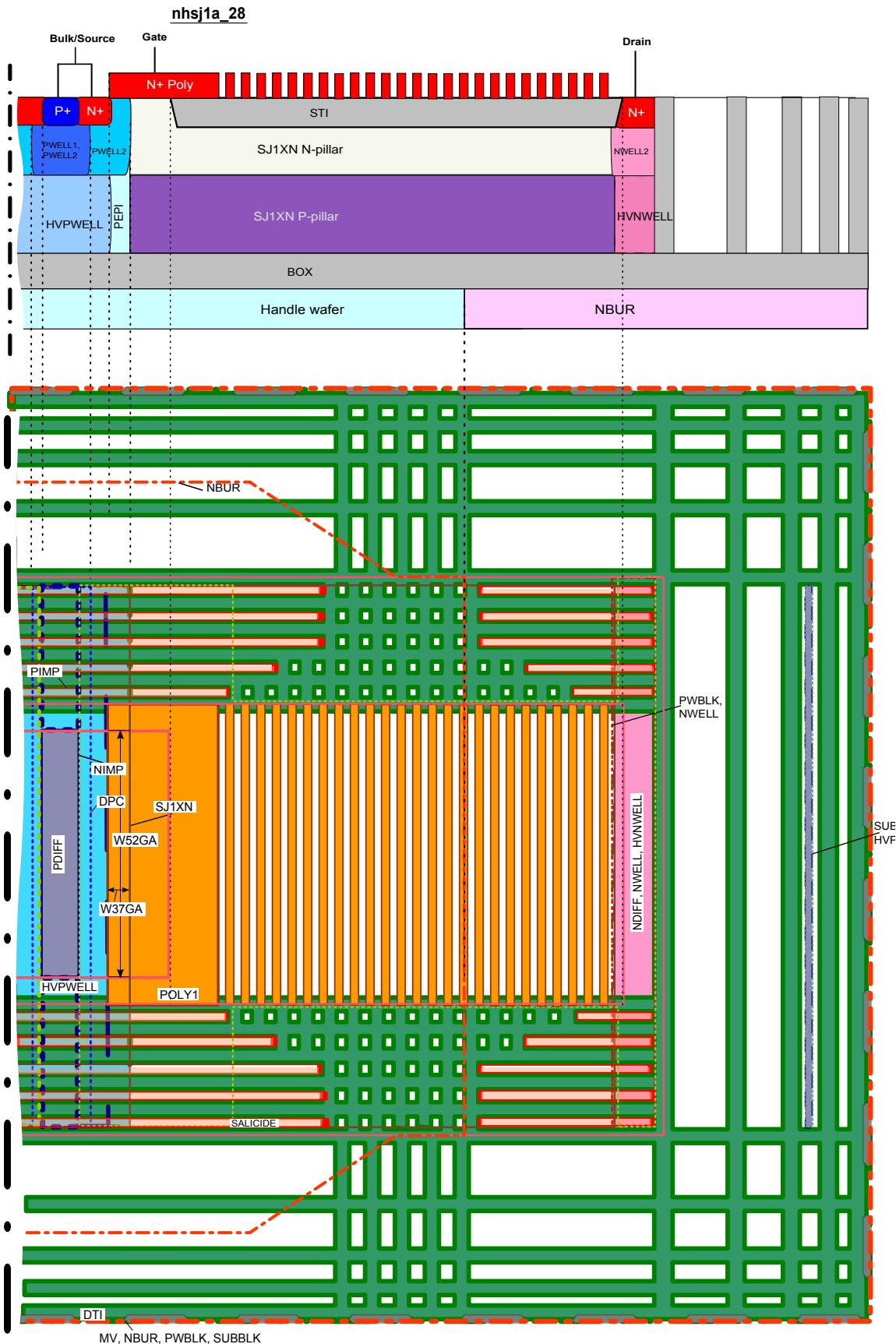


Figure 3.277 nhsj1a\_28

3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → phsj1a\_20

### **phsj1a\_20**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10X2	This device must be used together with a dhw4d or dhw5d	-	-
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B14X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.		
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
W41GA	Fixed CHANNEL length	0.5	µm
W60GA	Minimum GATE width	60.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** phsj1a\_20 device must be labeled "phsj1a\_20" using POLY1 (VERIFICATION) layer over GATE.

**Note:** NBUR connection to dhw4d or dhw5d is not shown in the diagram.

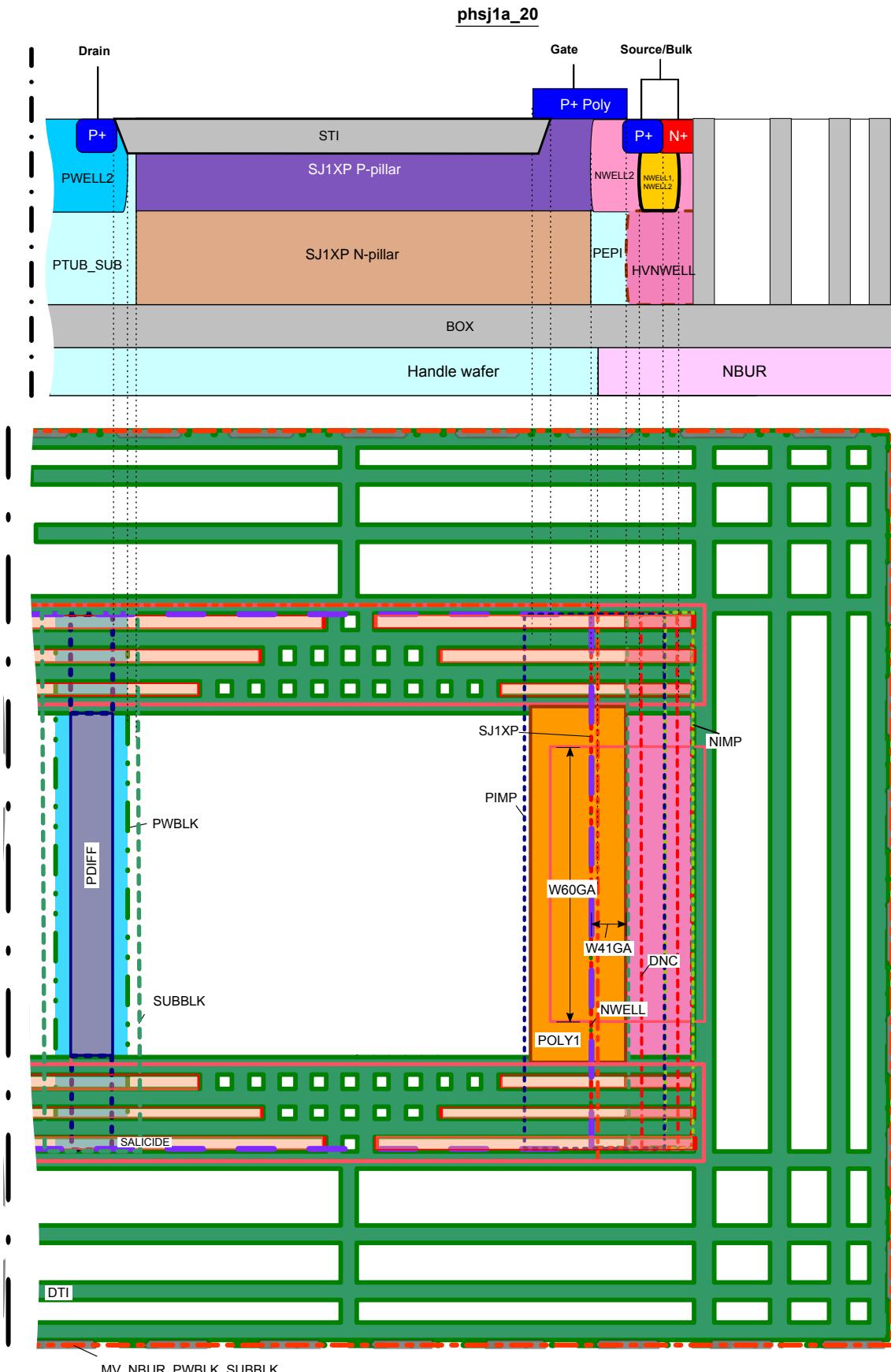
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_20m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.37 SJHVU module→ 3.37.1 Device rules→ phsj1a\_20

**Figure 3.278 phsj1a\_20**

3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → phsj1a\_31

### **phsj1a\_31**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11X2	This device must be used together with dhw5d	-	-
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B14X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
W41GA	Fixed CHANNEL length	0.5	µm
W80GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	80.0	µm

**Note:** MV is necessary for this device.

**Note:** phsj1a\_31 device must be labeled "phsj1a\_31" using POLY1 (VERIFICATION) layer over GATE.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw5d is not shown in the diagram.

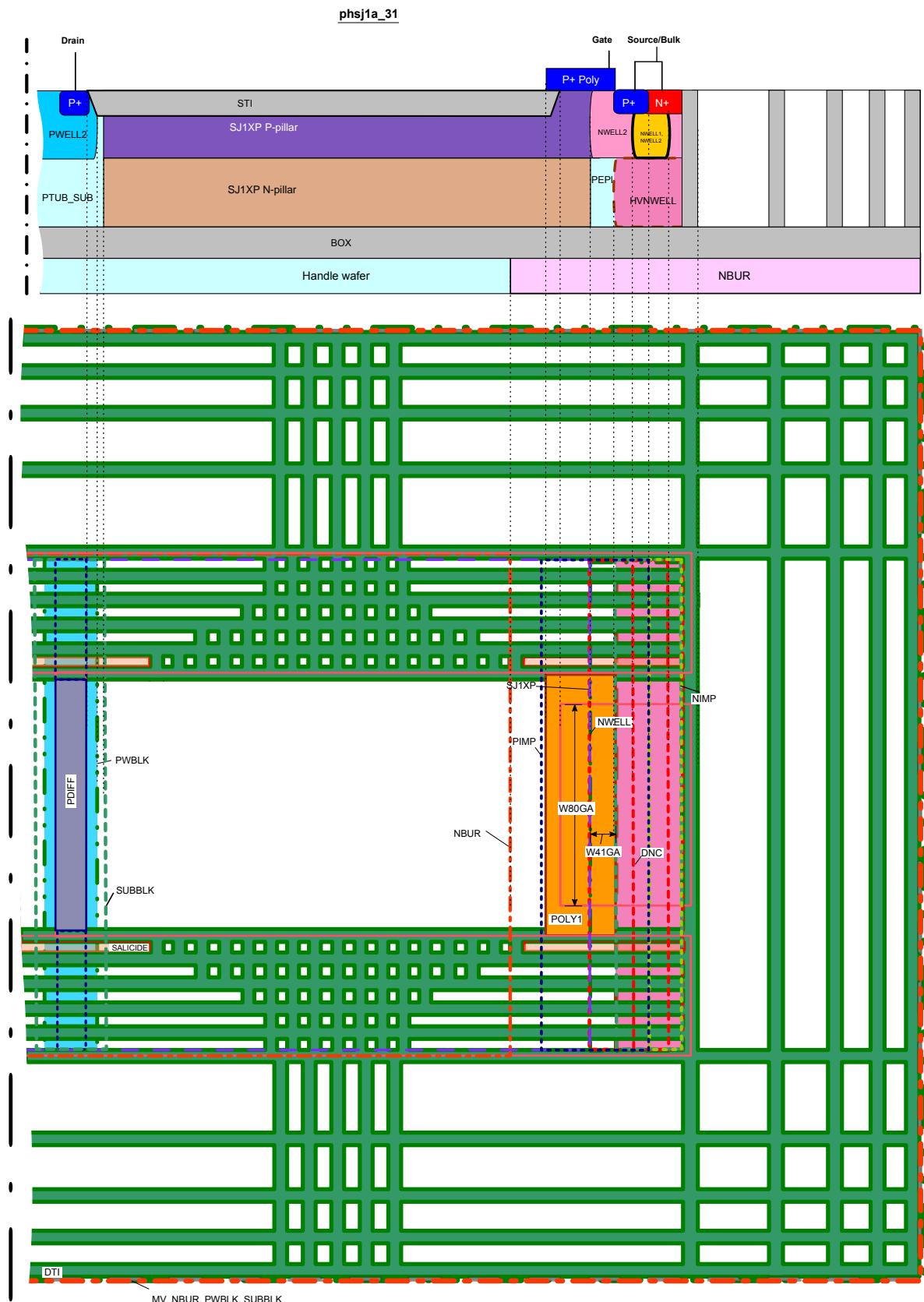
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_31m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.37 SJHVU module→ 3.37.1 Device rules→ phsj1a\_31

**Figure 3.279** phsj1a\_31

3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → dfwnsj1a\_20

## **dfwnsj1a\_20**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10X1	This device must be used together with a dhw4d or dhw5d	-	-
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B14X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-

**Note:** MV is necessary for this device.

**Note:** dfwnsj1a\_20 device must be labeled "dfwnsj1a\_20" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw4d or dhw5d is not shown in the diagram.

**Note:** Minimum drawn finger width is 61 µm

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1a\_20m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → dfwnsj1a\_20

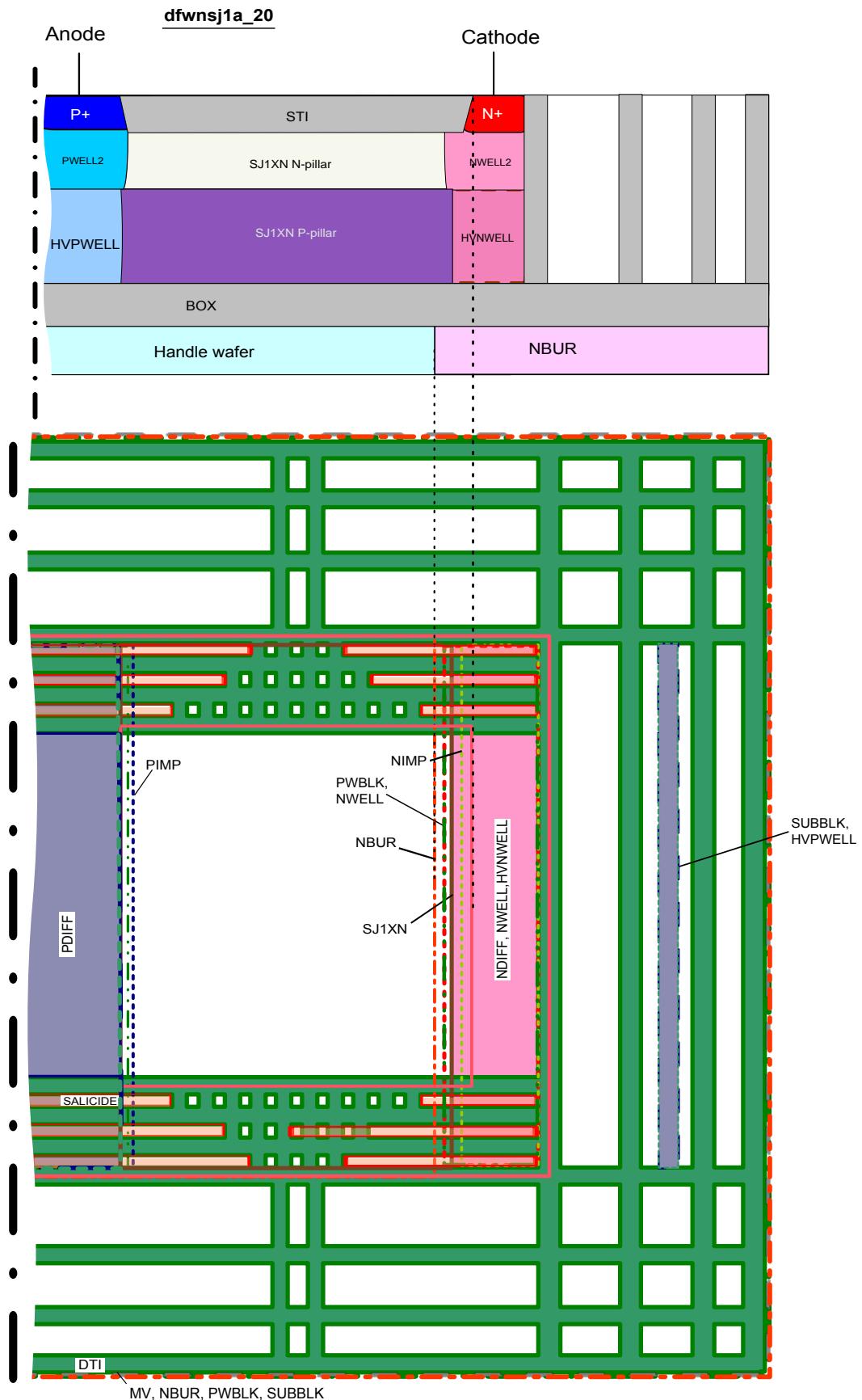


Figure 3.280 dfwnsj1a\_20

3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → dfwnsj1a\_28

### **dfwnsj1a\_28**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11X1	This device must be used together with dhw5d	-	-
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B14X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-

**Note:** MV is necessary for this device.

**Note:** dfwnsj1a\_28 device must be labeled "dfwnsj1a\_28" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw5d is not shown in the diagram.

**Note:** Minimum drawn finger width is 61 µm

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1a\_28m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → dfwnsj1a\_28

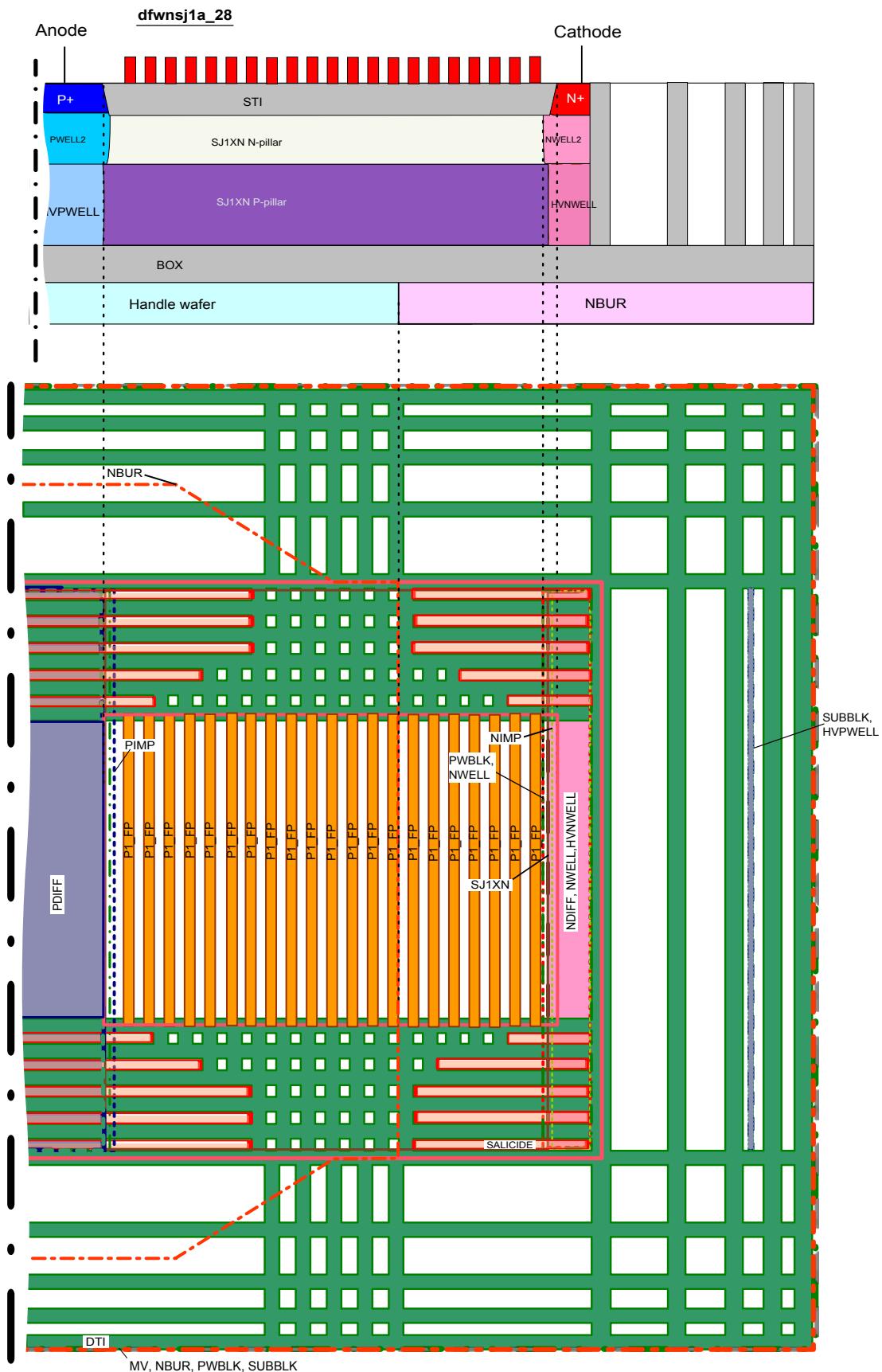


Figure 3.281 dfwnsj1a\_28

3. Layer and Device rules → 3.37 SJHVU module→ 3.37.1 Device rules→ dhw4d

### dhw4d

Name	Description	Value	Unit
B10NB	TUB inside dhw#c, dhw#d must be surrounded by HWNTUB (except ISOTUB or TIEDTUB)	-	-
<u>B11HW</u>	TUB inside dhw#c, dhw#d must have HWC on each side (except ISOTUB or TIEDTUB)	-	-
B3M1	MET1 overlap of ISOTUB is not allowed	-	-
B4NB	dhw#c, dhw#d terminal (Cathode/Anode) short is not allowed	-	-
B6HN	dhw#c, dhw#d must be surrounded by HWPTUB	-	-
W5TP	Minimum HWPTUB width	15.0	µm
W6M2	Maximum (MET2 inside ISOTUB) width	0.5	µm
W6TN	Minimum HWNTUB width	17.5	µm
S16NB	Minimum NBUR spacing (different net)	23.0	µm
S14NB	Minimum NBUR spacing to NBUR (dhw#, dhw#c)	23.0	µm
S5DTHW	Minimum DTI spacing to HWC	8.0	µm
<u>S6DTHW</u>	Maximum DTI spacing to HWC	16.0	µm
S7NBHB	Minimum NBUR spacing to SUBBLK	21.5	µm
S7NBHW	Minimum NBUR spacing to HWC	21.5	µm

**Note:** dhw4d device must be labeled "dhw4d" using DIODEF (VERIFICATION) layer.

3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → dhw4d

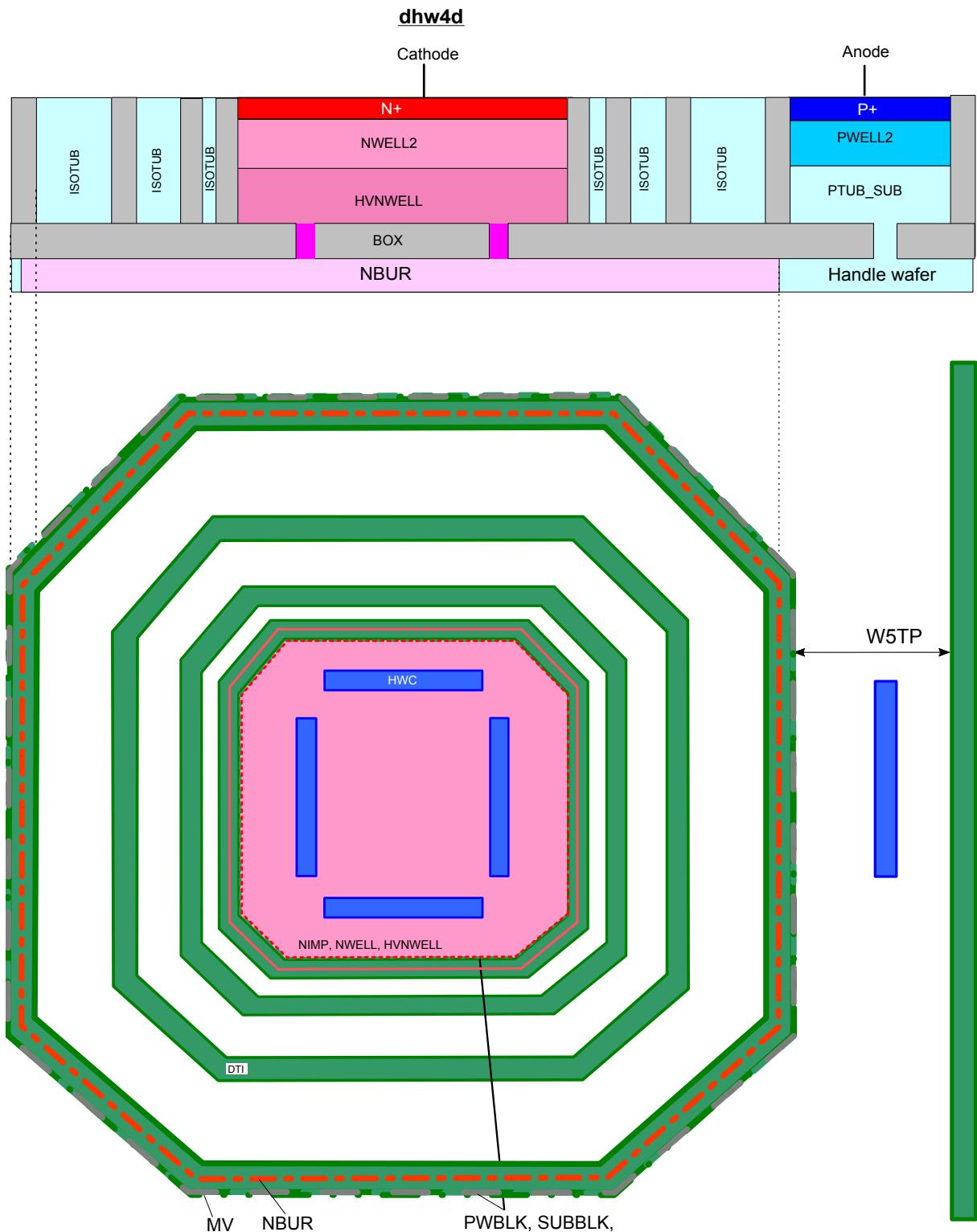


Figure 3.282 dhw4d

3. Layer and Device rules → 3.37 SJHVU module→ 3.37.1 Device rules→ dhw5d

### dhw5d

Name	Description	Value	Unit
B10NB	TUB inside dhw#c, dhw#d must be surrounded by HWNTUB (except ISOTUB or TIEDTUB)	-	-
<u>B11HW</u>	TUB inside dhw#c, dhw#d must have HWC on each side (except ISOTUB or TIEDTUB)	-	-
B3M1	MET1 overlap of ISOTUB is not allowed	-	-
B4NB	dhw#c, dhw#d terminal (Cathode/Anode) short is not allowed	-	-
B6HN	dhw#c, dhw#d must be surrounded by HWPTUB	-	-
W5TP	Minimum HWPTUB width	15.0	µm
W6M2	Maximum (MET2 inside ISOTUB) width	0.5	µm
W6TN	Minimum HWNTUB width	17.5	µm
S17NB	Minimum NBUR spacing (different net)	24.0	µm
S15NB	Minimum NBUR spacing to NBUR (dhw#, dhw#c, dhw4d)	24.0	µm
S5DTHW	Minimum DTI spacing to HWC	8.0	µm
<u>S6DTHW</u>	Maximum DTI spacing to HWC	16.0	µm
S8NBHB	Minimum NBUR spacing to SUBBLK	22.5	µm
S8NBHW	Minimum NBUR spacing to HWC	22.5	µm

**Note:** dhw5d device must be labeled "dhw5d" using DIODEF (VERIFICATION) layer.

## 3. Layer and Device rules → 3.37 SJHVU module → 3.37.1 Device rules → dhw5d

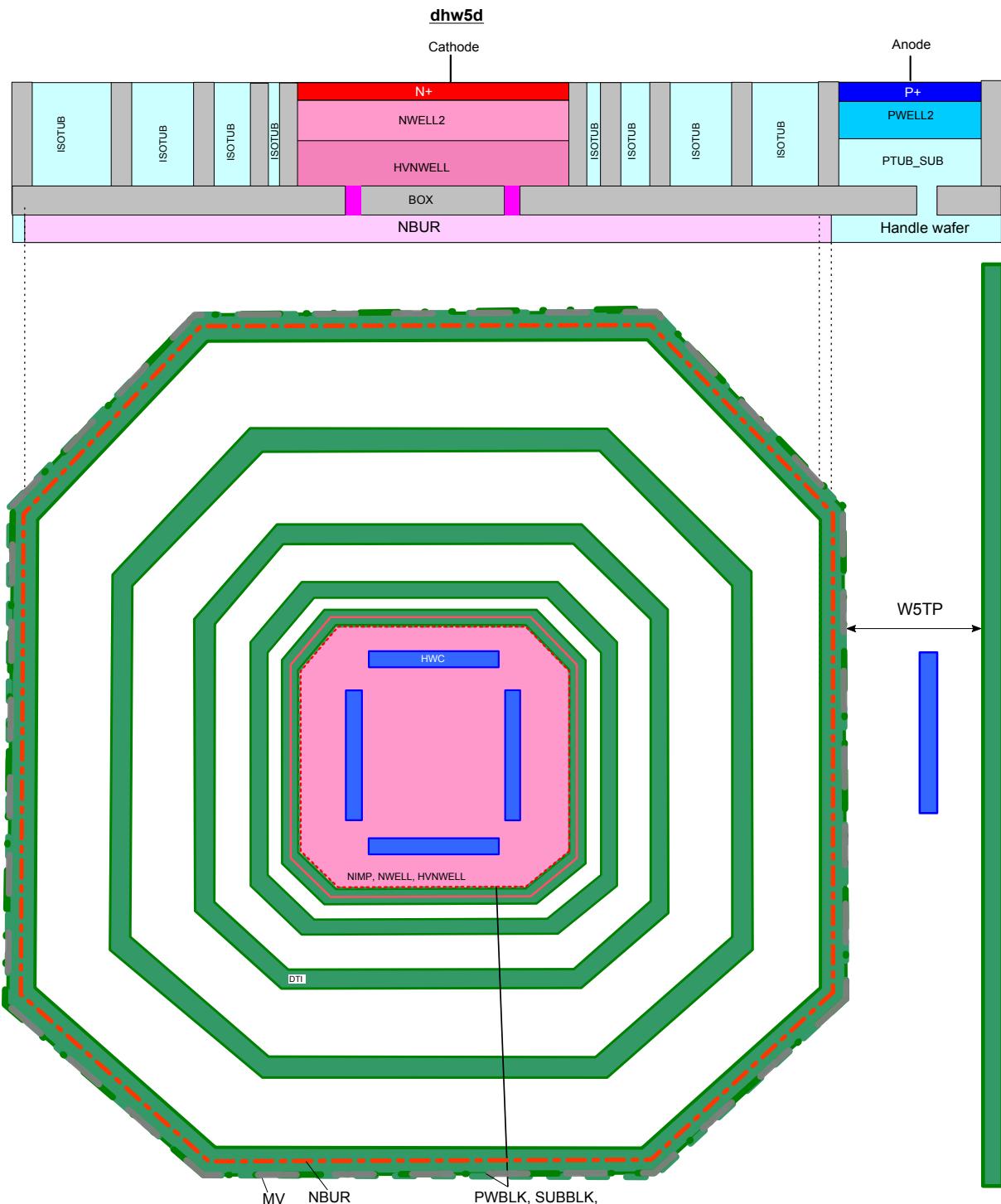


Figure 3.283 dhw5d

3. Layer and Device rules → 3.38 SJ1XN module

## 3.38 SJ1XN module

### 3.38.1 Layer rules

#### SJ1XN

Name	Description	Value	Unit
B12X1	MET1 is not allowed over SJ1XN (except predefined MET1 device terminal connections, M1_FP)	-	-
B1X1	SJ1XN without SUBBLK and MV is not allowed	-	-
B2X1	SJ1XN overlap of HWTUB, DNC, DPC, HVNWELL, HVPWELL, HRES, MRES, DEPL, PWELL4 is not allowed	-	-
B3X1	SJ1XN overlap of NDF, PDF, NDFMV, PDFMV, DFN, DFP, NBASE, PBASE is not allowed	-	-
B4X1	SJ1XN overlap of SJNP, SJPN, NBUF is not allowed	-	-
W1X1	Minimum SJ1XN width	2.0	μm
S1X1	Minimum SJ1XN spacing / notch	1.5	μm
S1X1NF	Minimum SJ1XN spacing to NBUF	2.0	μm
S1X1NT	Minimum SJ1XN spacing to SJNP	2.0	μm
S1X1PT	Minimum SJ1XN spacing to SJPN	2.0	μm
S1X1X2	Minimum SJ1XN spacing to SJ1XP	2.0	μm
S1X1X4	Minimum SJ1XN spacing to SJ2XP	2.0	μm
A1X1	Minimum SJ1XN area	9.5	μm <sup>2</sup>

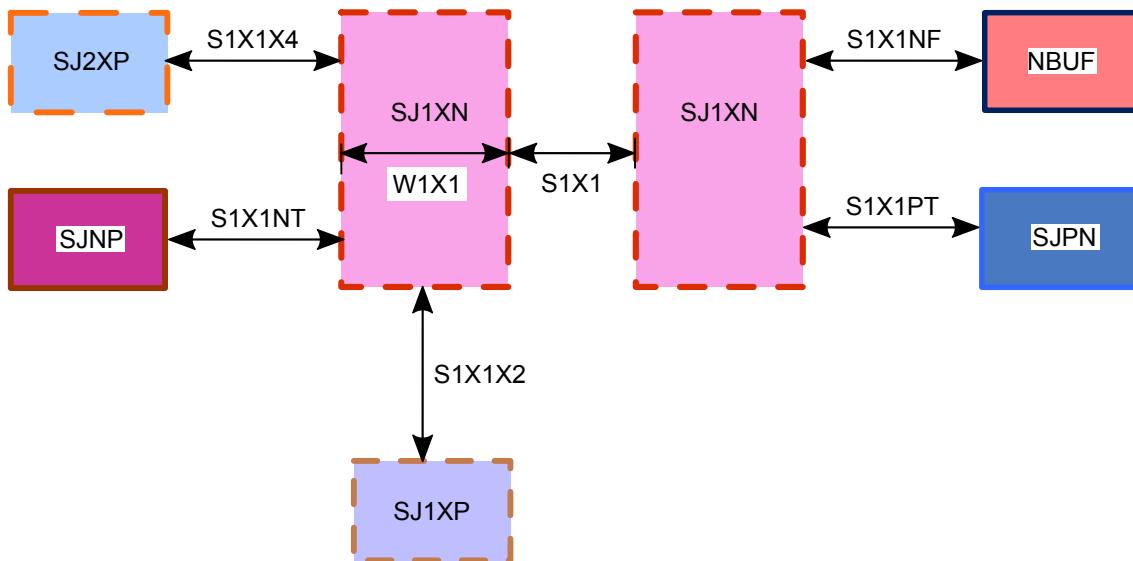


Figure 3.284 SJ1XN

#### SJ1XN\_E

Name	Description	Value	Unit
W2X1	Minimum SJ1XN_E width	0.5	μm

### 3.38.2 Device rules

#### nhsj1b\_2

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

⇒

## 3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1b\_2

Name	Description	Value	Unit
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	µm
W38GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	µm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_2 device must be labeled "nhsj1b\_2" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1b\_2

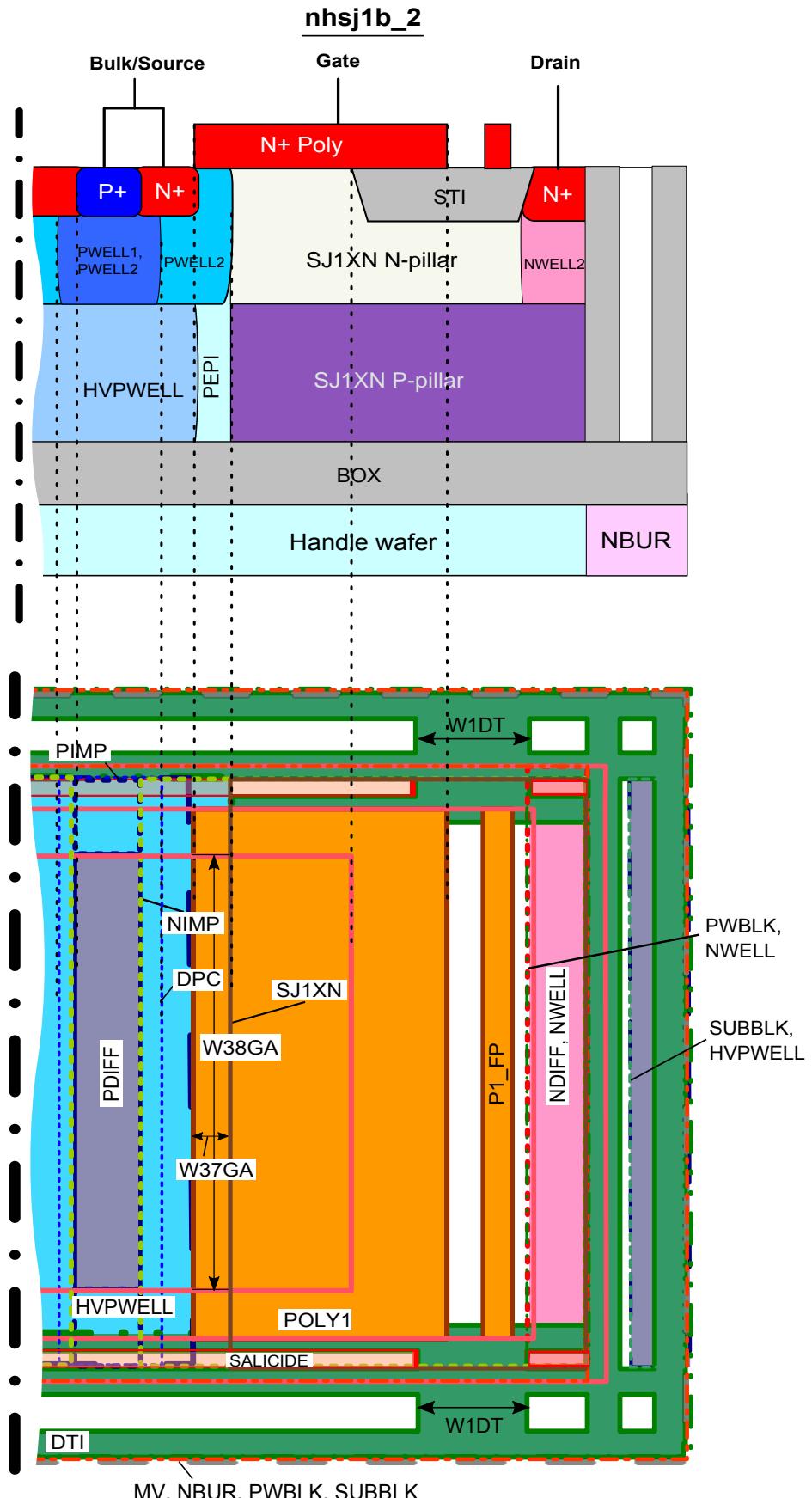


Figure 3.285 nhsj1b\_2

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1b\_4

### **nhsj1b\_4**

The layout is predefined and scalable concerning width and length. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W38GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	μm
W39GA	Minimum CHANNEL length	0.5	μm
W40GA	Maximum CHANNEL length	10.0	μm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_4 device must be labeled "nhsj1b\_4" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1b\_4

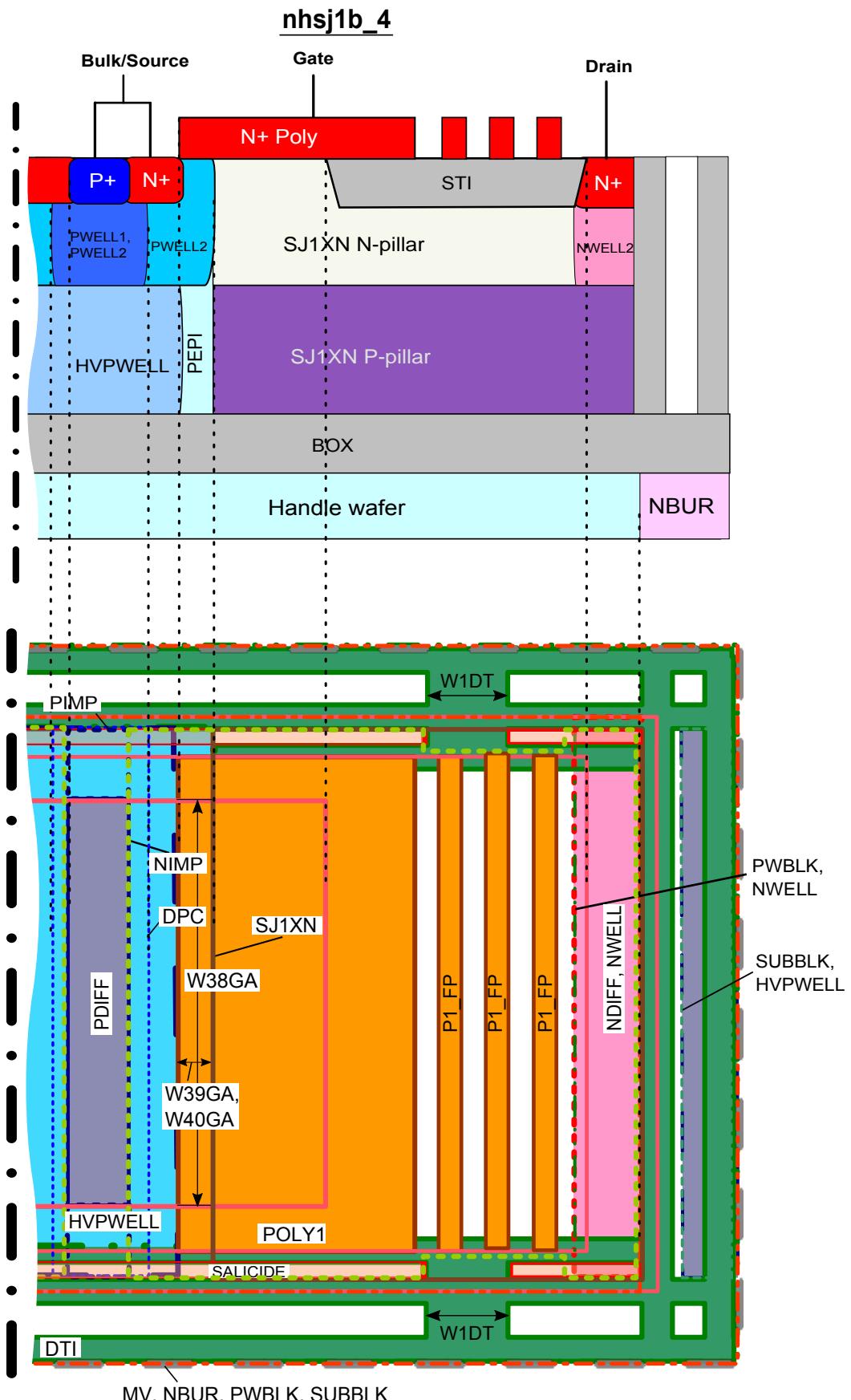


Figure 3.286 nhsj1b\_4

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1b\_5

### **nhsj1b\_5**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W38GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_5 device must be labeled "nhsj1b\_5" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1b\_5

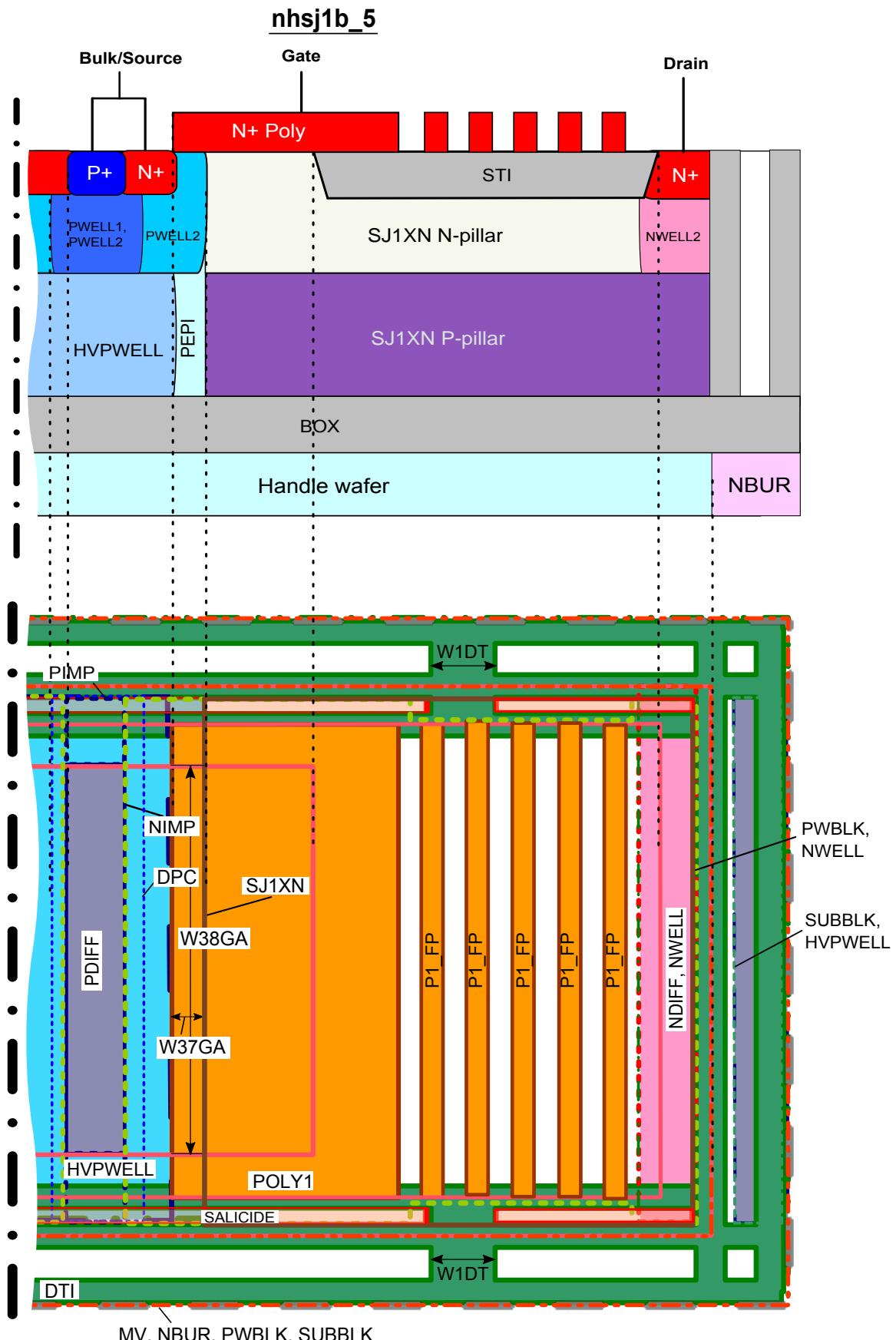


Figure 3.287 nhsj1b\_5

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1b\_7

### **nhsj1b\_7**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W45GA	Minimum GATE width	15.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_7 device must be labeled "nhsj1b\_7" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1b\_7

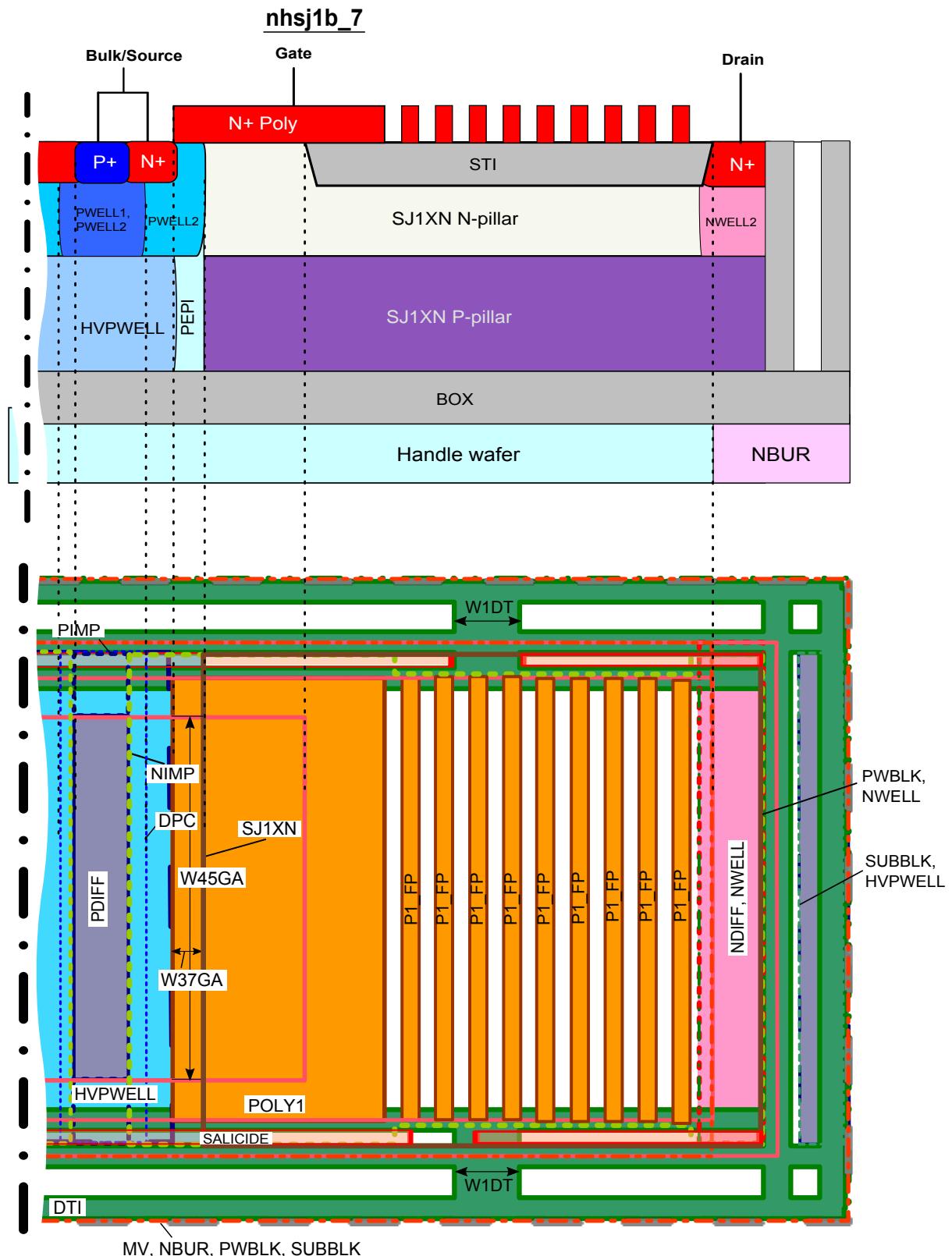


Figure 3.288 nhsj1b\_7

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1b\_8

### **nhsj1b\_8**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B7X1	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W46GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	18.0	μm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_8 device must be labeled "nhsj1b\_8" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1b\_8m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1b\_8

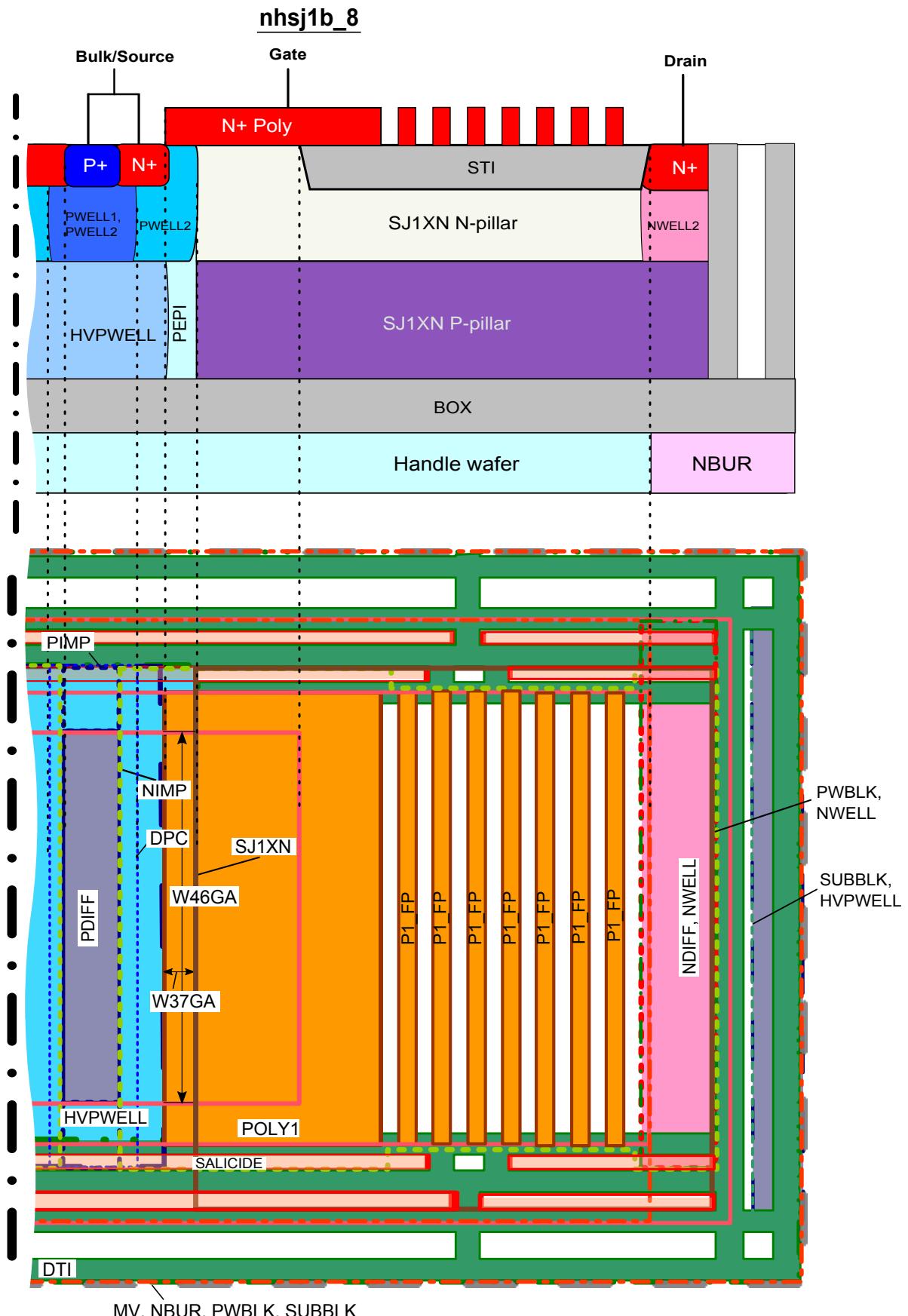


Figure 3.289 nhsj1b\_8

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1b\_10

### **nhsj1b\_10**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B7X1	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W47GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	20.0	μm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1b\_10 device must be labeled "nhsj1b\_10" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1b\_10m3" using DEVLBL (VERIFICATION) layer.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1b\_10

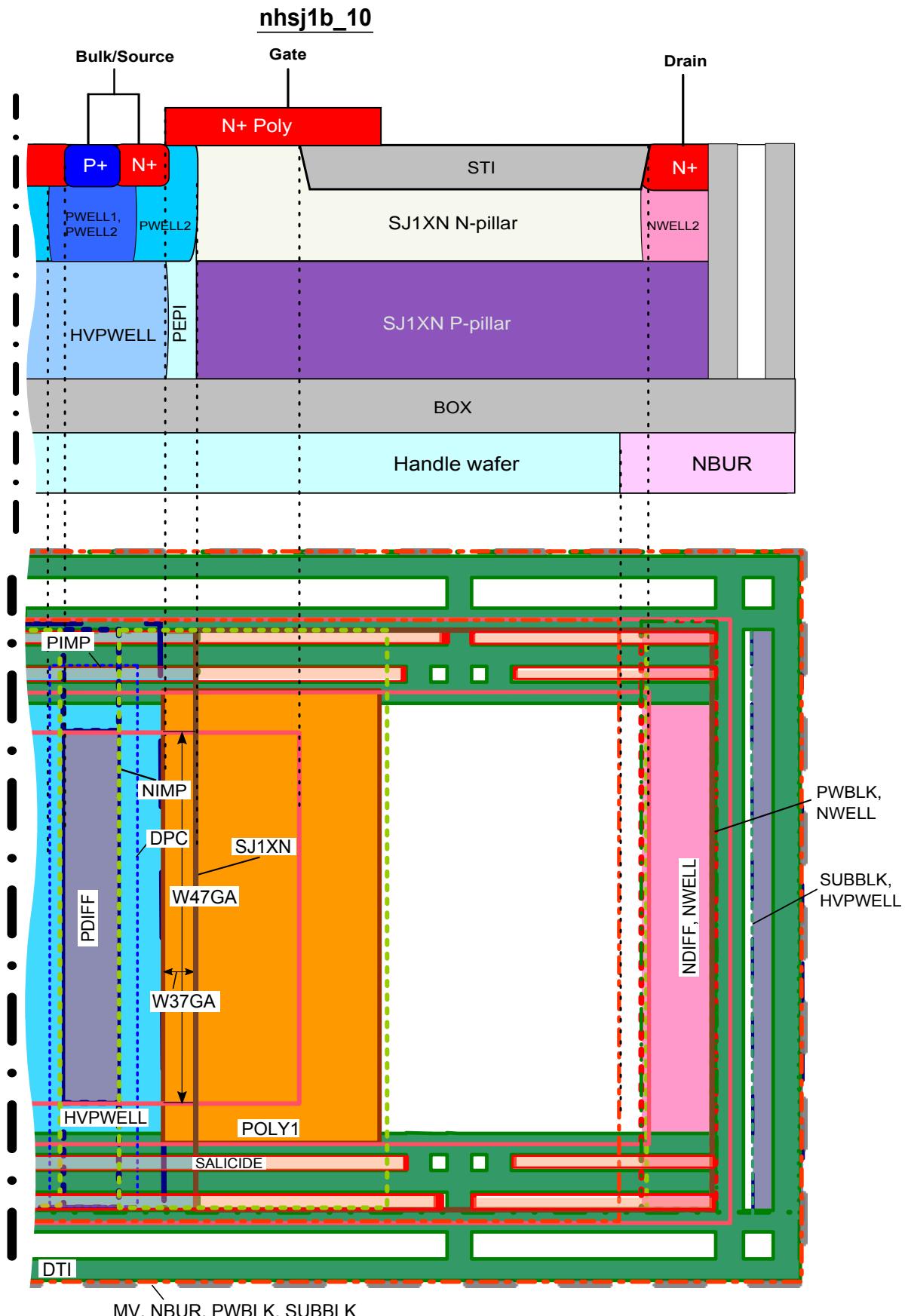


Figure 3.290 nhsj1b\_10

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1a\_13

### **nhsj1a\_13**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B8X1	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	µm
W49GA	Minimum GATE width	25.0	µm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1a\_13 device must be labeled "nhsj1a\_13" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1a\_13m3" using DEVLBL (VERIFICATION) layer.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1a\_13

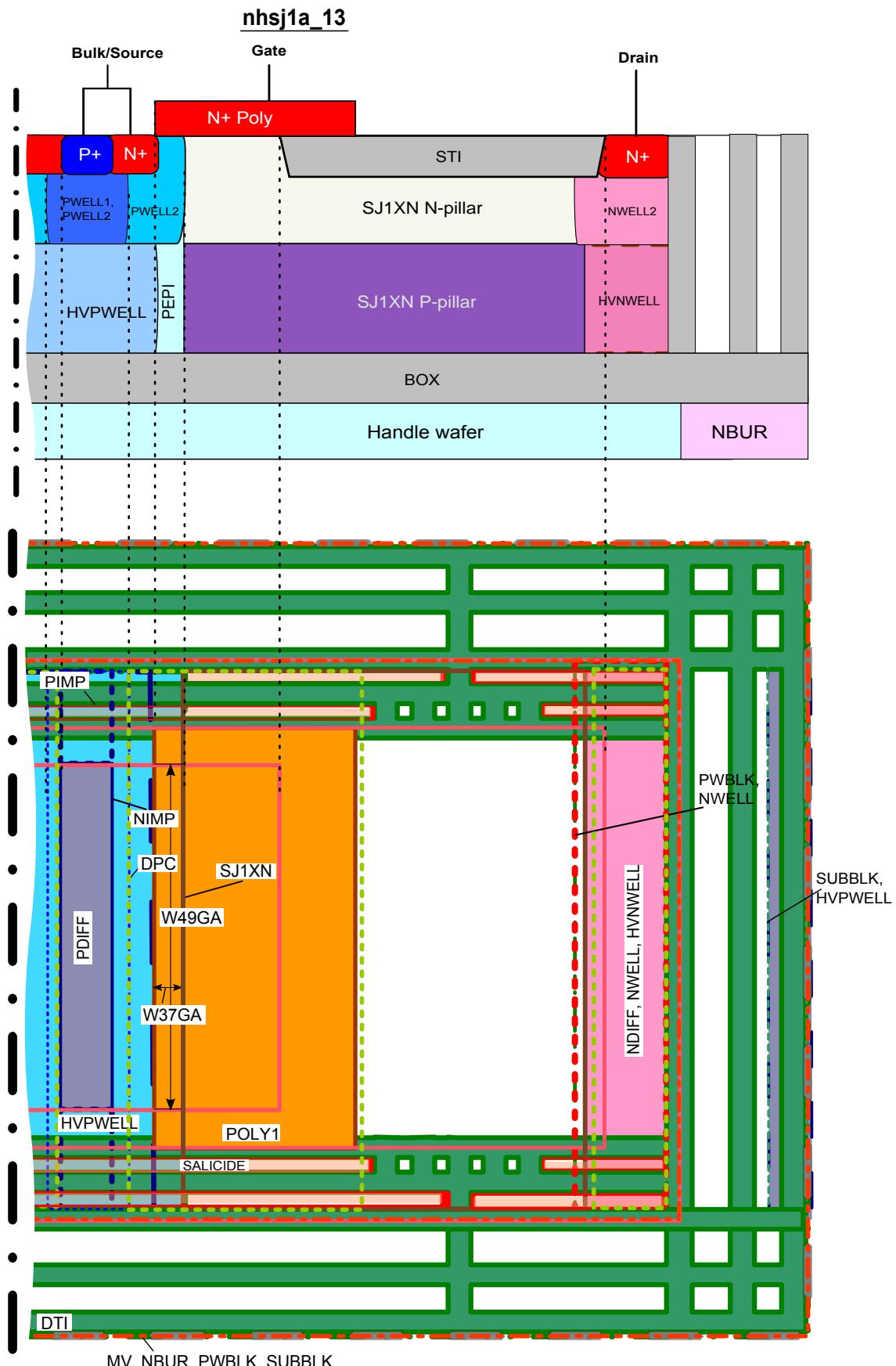


Figure 3.291 nhsj1a\_13

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1a\_16

### **nhsj1a\_16**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B9X1	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
W37GA	Fixed CHANNEL length	0.5	μm
W50GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	30.0	μm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1a\_16 device must be labeled "nhsj1a\_16" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1a\_16m3" using DEVLBL (VERIFICATION) layer.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1a\_16

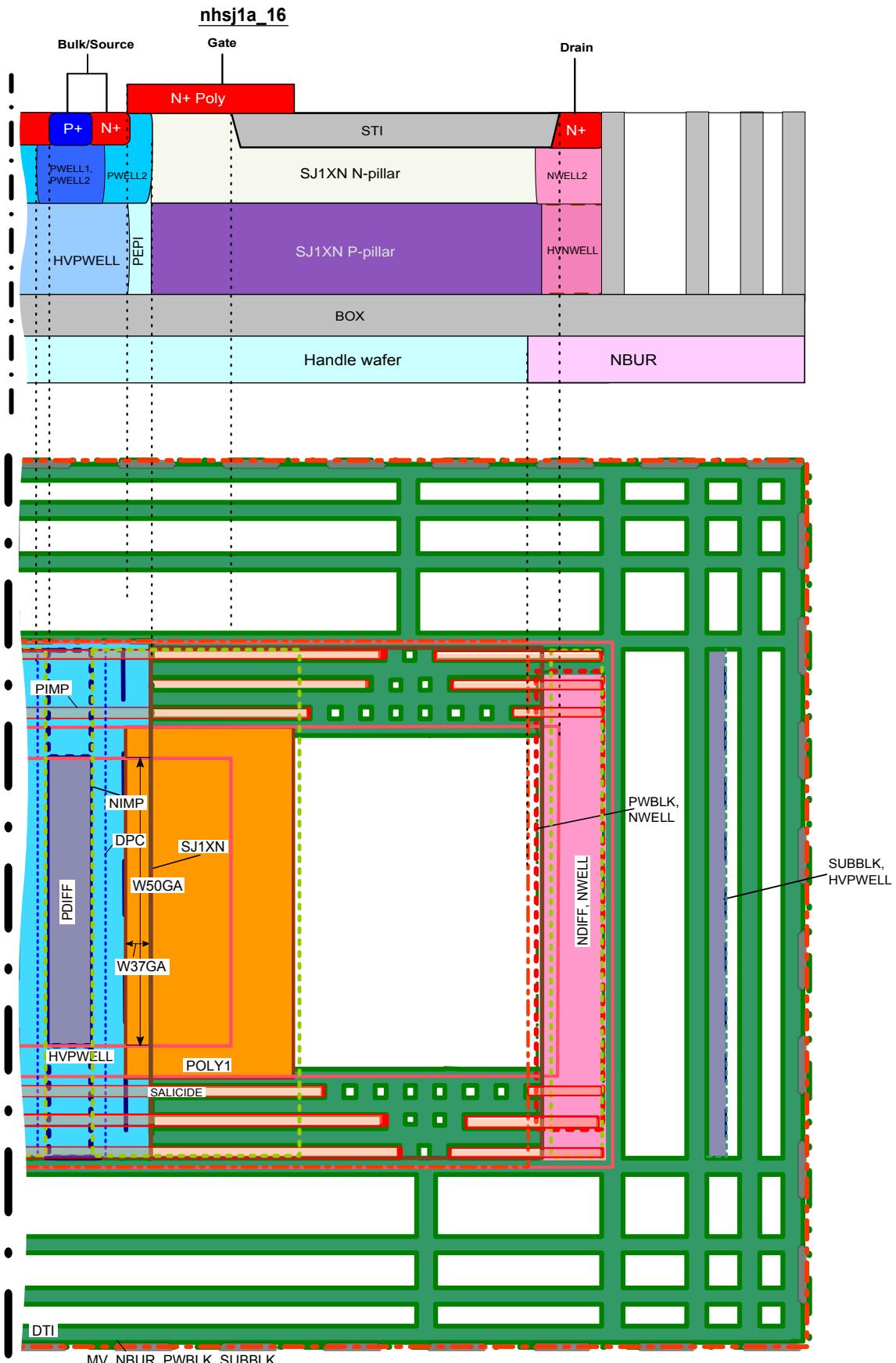


Figure 3.292 nhsj1a\_16

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1a\_20

### **nhsj1a\_20**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10X1	This device must be used together with a dhw4d or dhw5d	-	-
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B14X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
W37GA	Fixed CHANNEL length	0.5	µm
W51GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	40.0	µm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1a\_20 device must be labeled "nhsj1a\_20" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw4d or dhw5d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1a\_20m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1a\_20

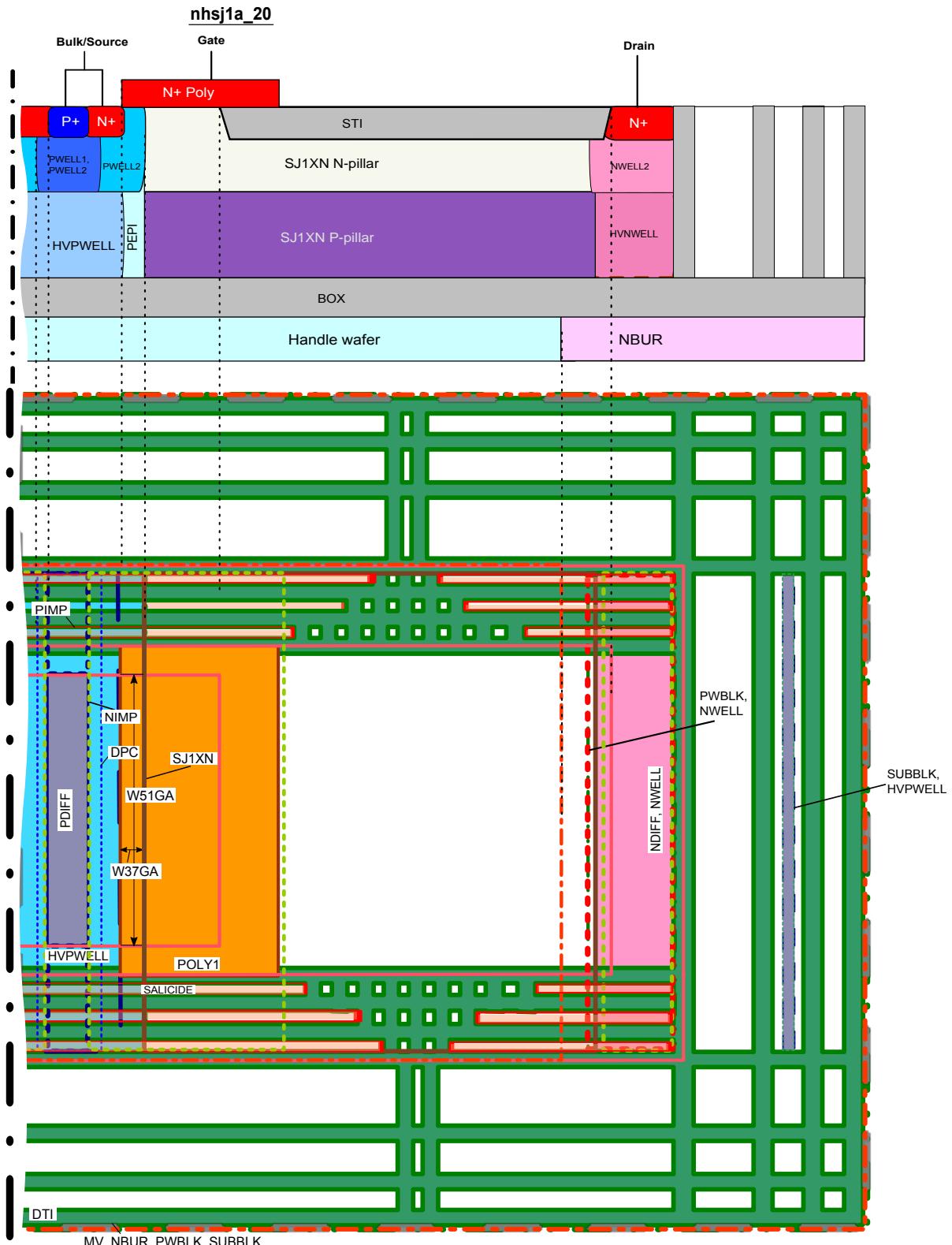


Figure 3.293 nhsj1a\_20

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ nhsj1a\_28

### **nhsj1a\_28**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11X1	This device must be used together with dhw5d	-	-
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B14X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
W37GA	Fixed CHANNEL length	0.5	µm
W52GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	60.0	µm

**Note:** This device is the type of Drain-Source-Drain design. Source-Drain-Source or Source-Drain design is forbidden.

**Note:** nhsj1a\_28 device must be labeled "nhsj1a\_28" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw5d is not shown in the diagram.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "nhsj1a\_28m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → nhsj1a\_28

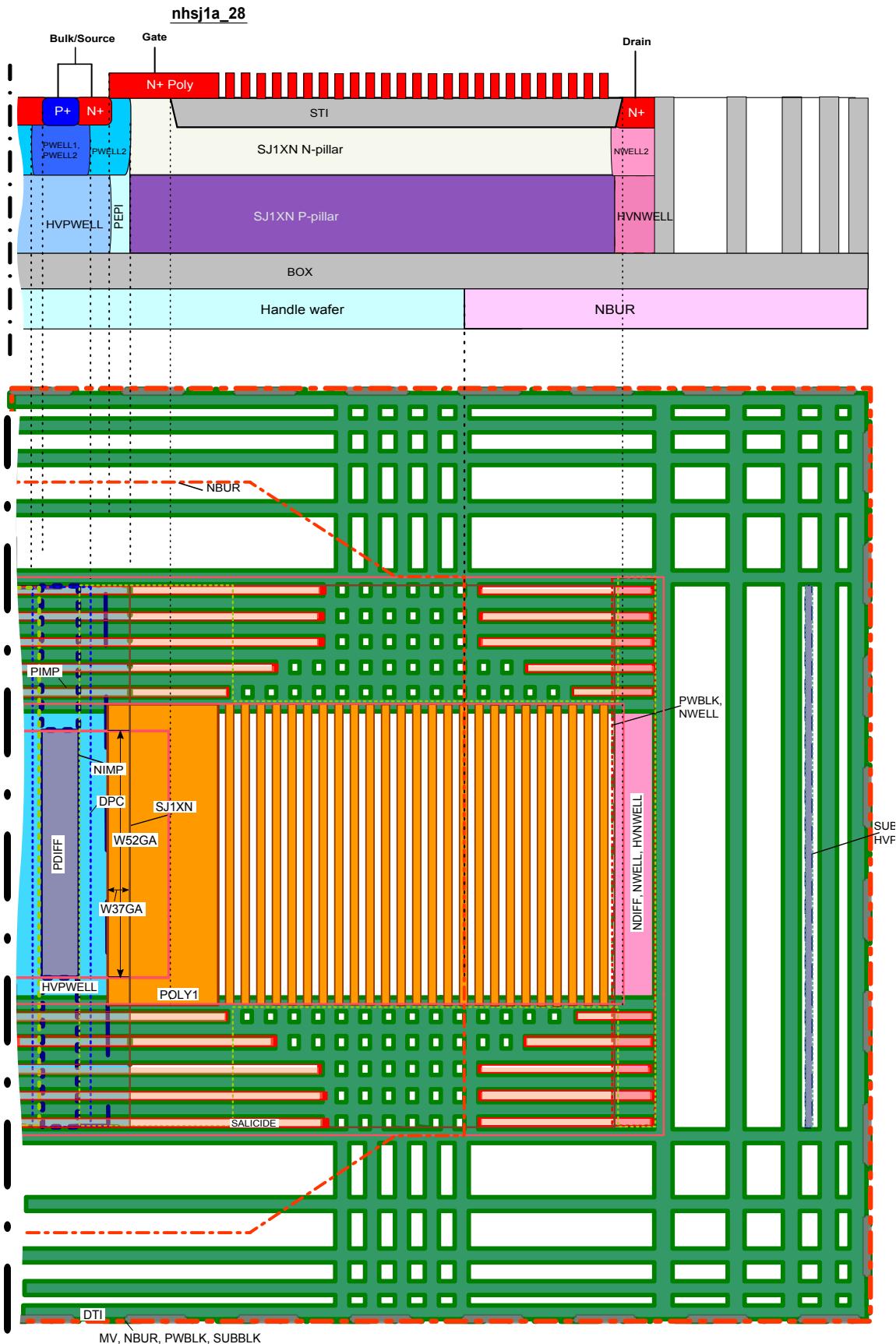


Figure 3.294 nhsj1a\_28

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1b\_2

### **dfwnsj1b\_2**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 11 µm

**Note:** MV is necessary for this device.

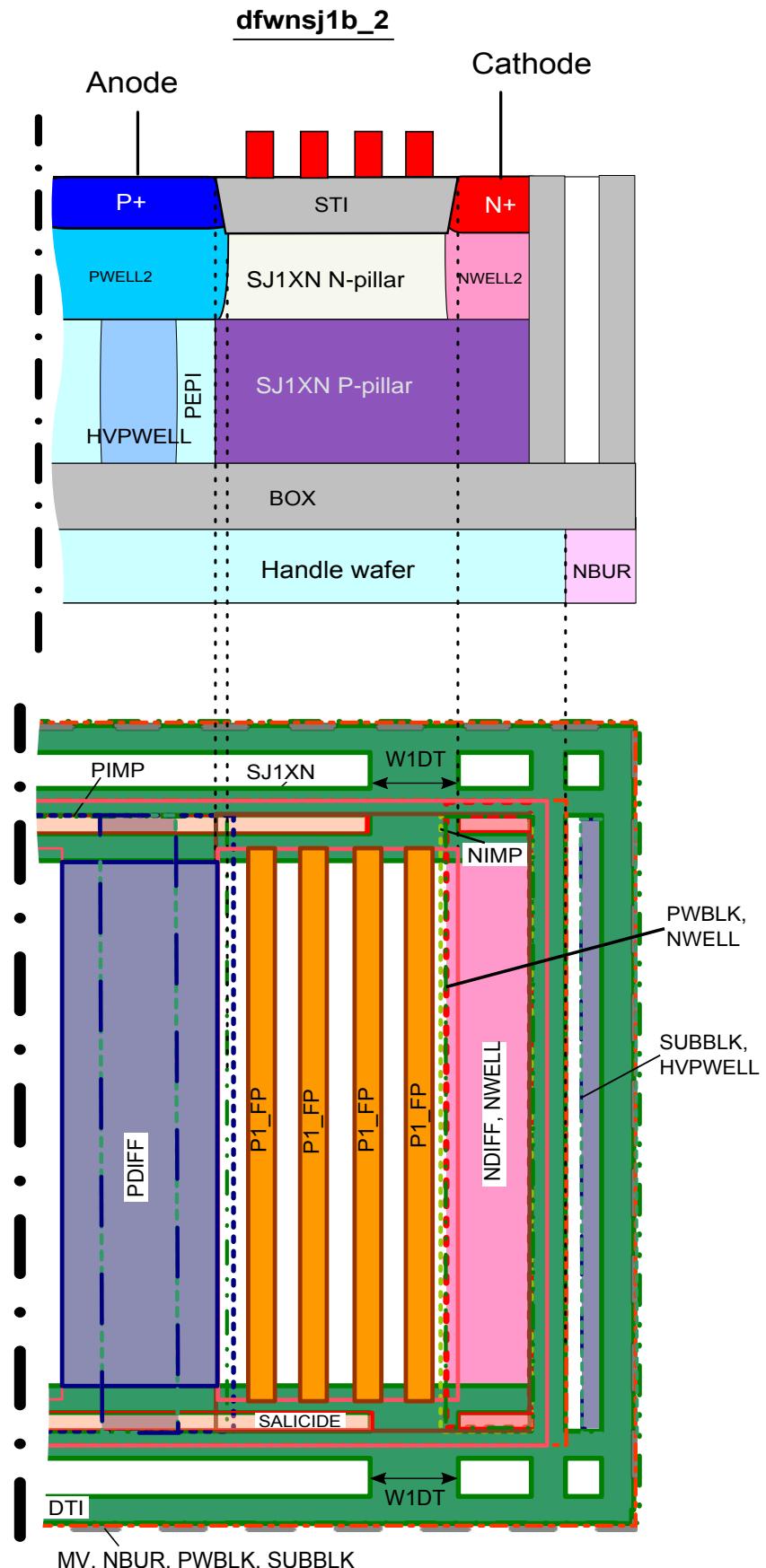
**Note:** dfwnsj1b\_2 device must be labeled "dfwnsj1b\_2" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1b\_2



**Figure 3.295** dfwnsj1b 2

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1b\_4

### **dfwnsj1b\_4**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 11 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_4 device must be labeled "dfwnsj1b\_4" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

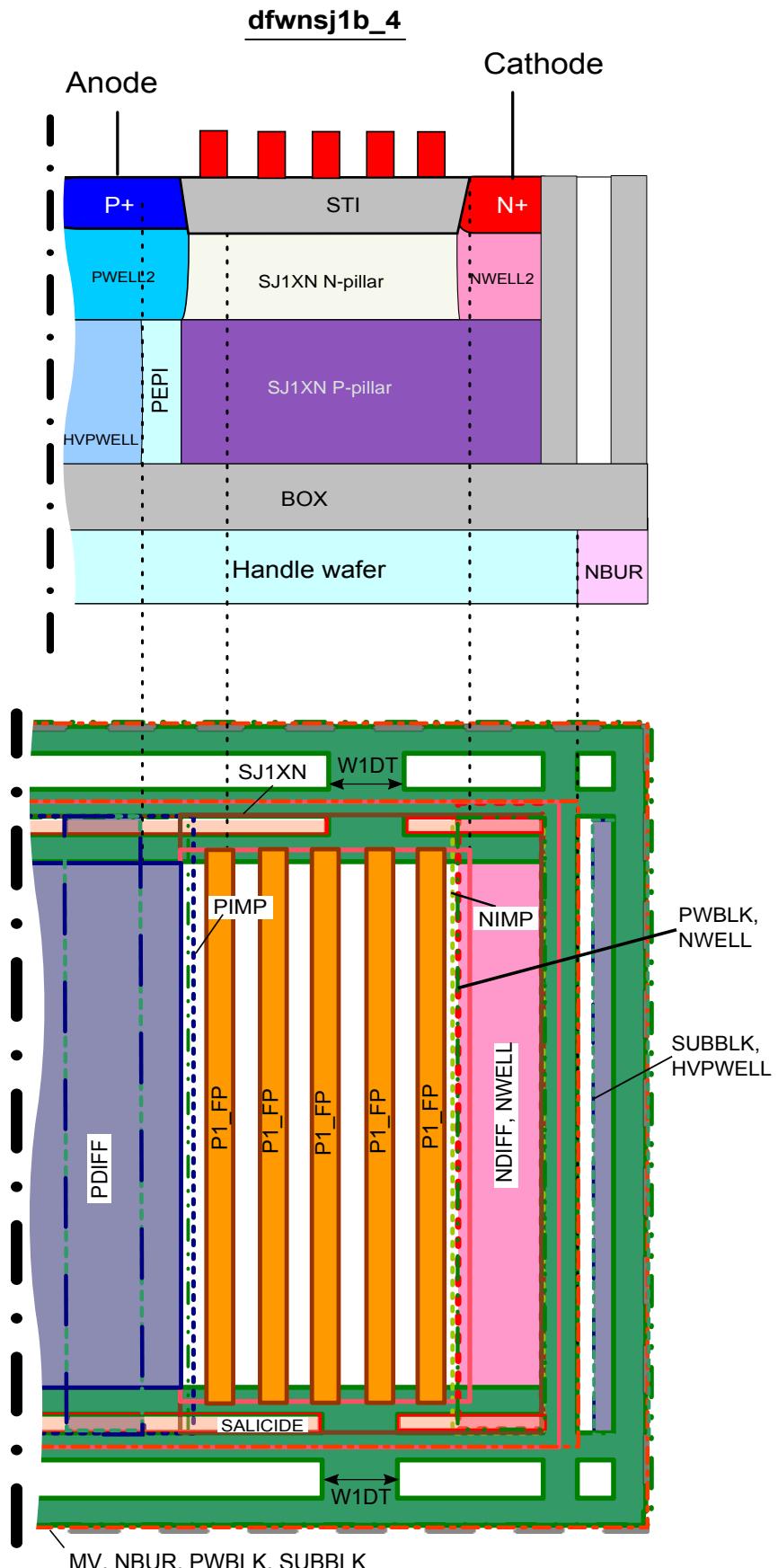
**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1b\_4



**Figure 3.296** dfwnsj1b\_4

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1b\_5

### **dfwnsj1b\_5**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 11 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_5 device must be labeled "dfwnsj1b\_5" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1b\_5

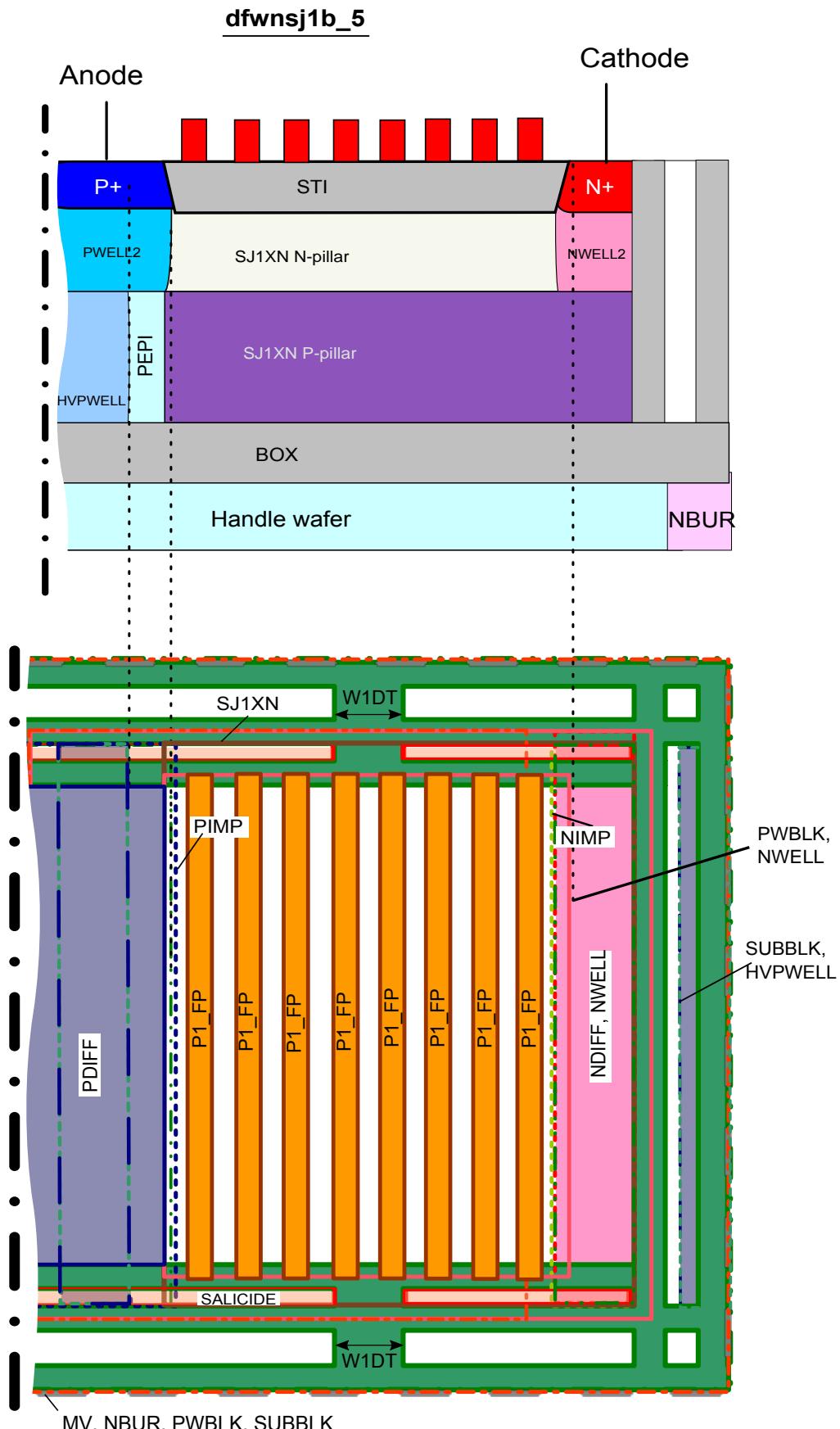


Figure 3.297 dfwnsj1b\_5

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1b\_7

### **dfwnsj1b\_7**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B6X1	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 16 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_7 device must be labeled "dfwnsj1b\_7" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

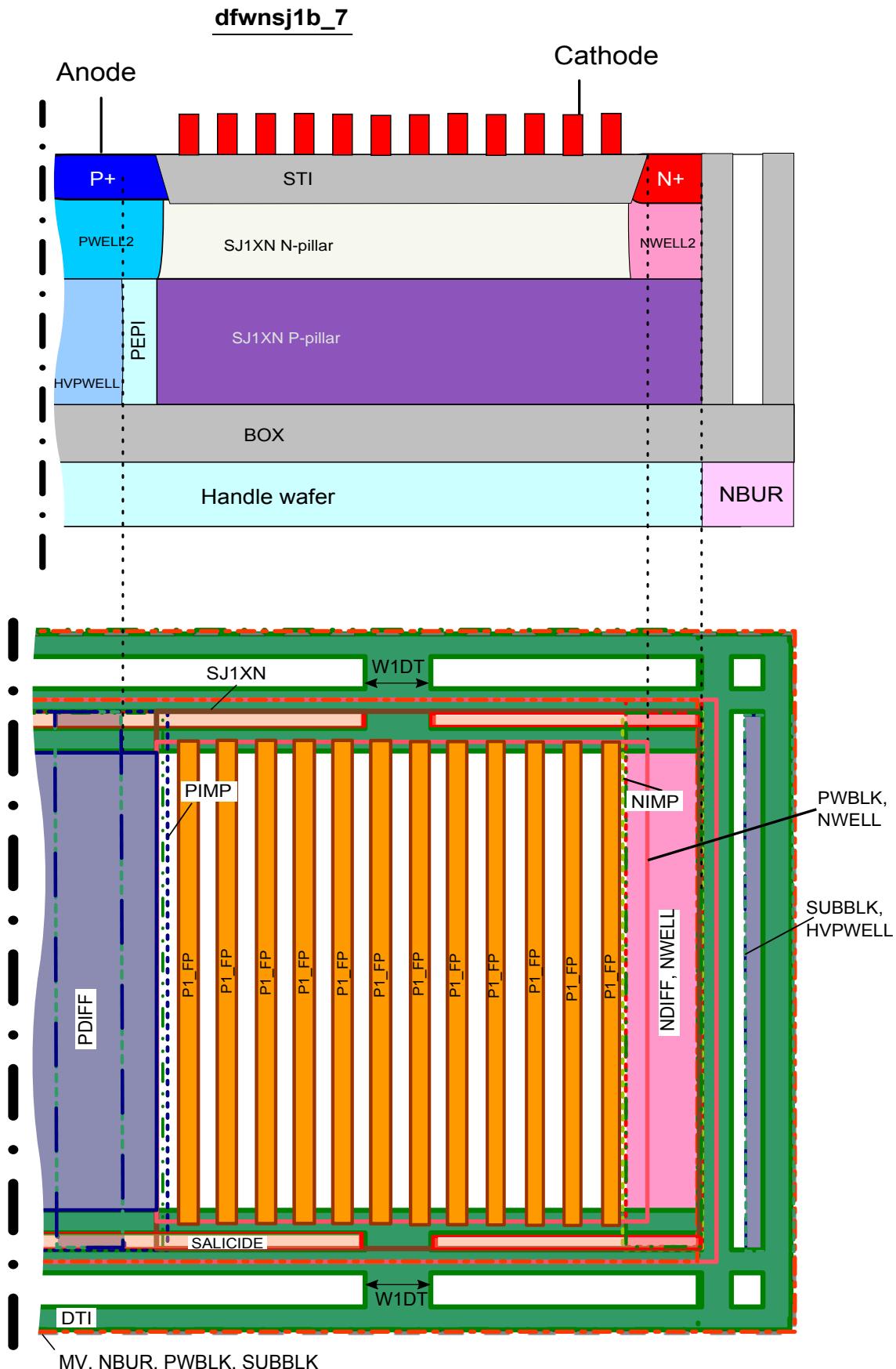
**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1b\_7



**Figure 3.298** dfwnsj1b\_7

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1b\_8

### **dfwnsj1b\_8**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B7X1	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 19 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_8 device must be labeled "dfwnsj1b\_8" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1b\_8m3" using DEVLBL (VERIFICATION) layer.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1b\_8

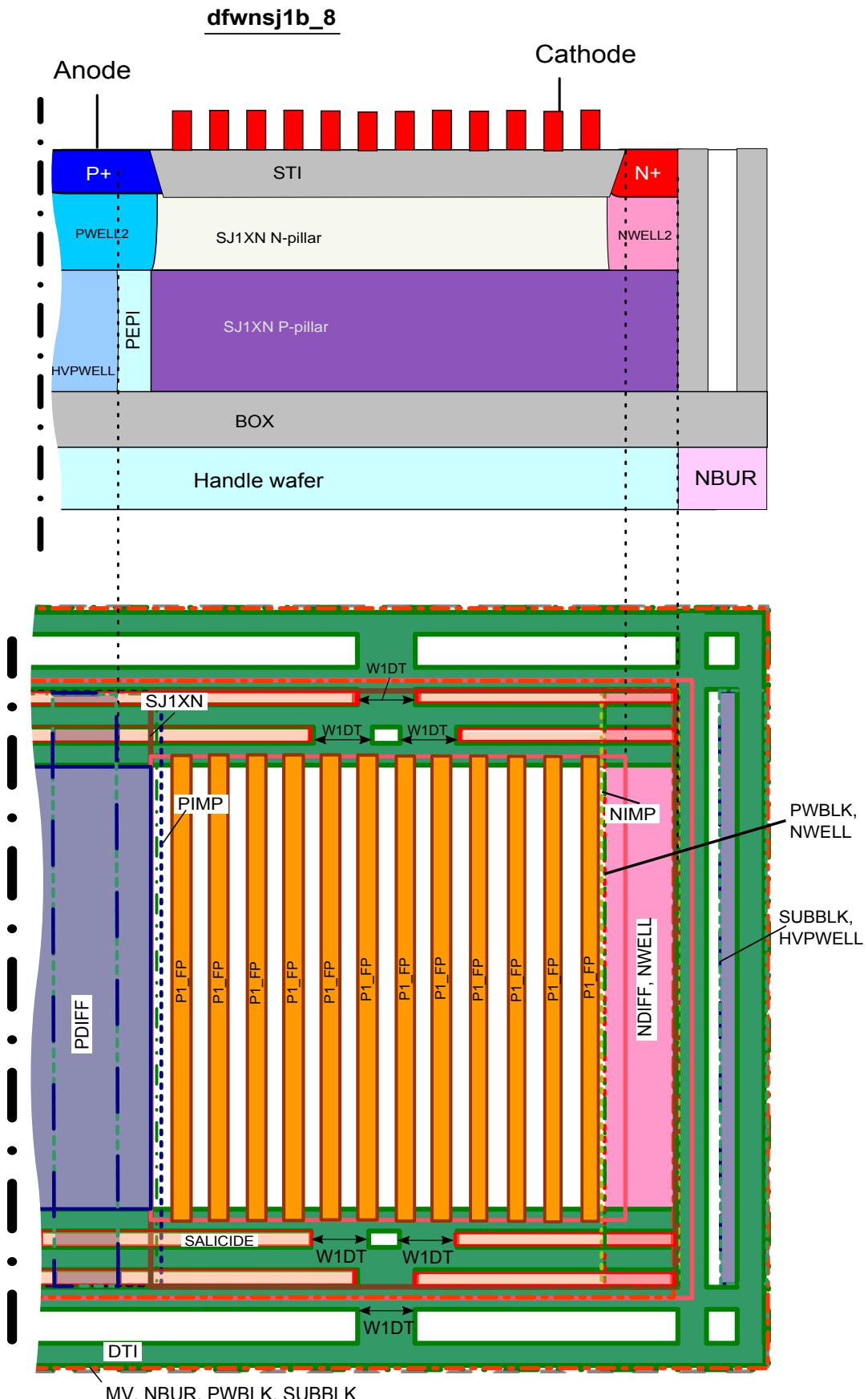


Figure 3.299 dfwnsj1b\_8

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1b\_10

### **dfwnsj1b\_10**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B7X1	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 21 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1b\_10 device must be labeled "dfwnsj1b\_10" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

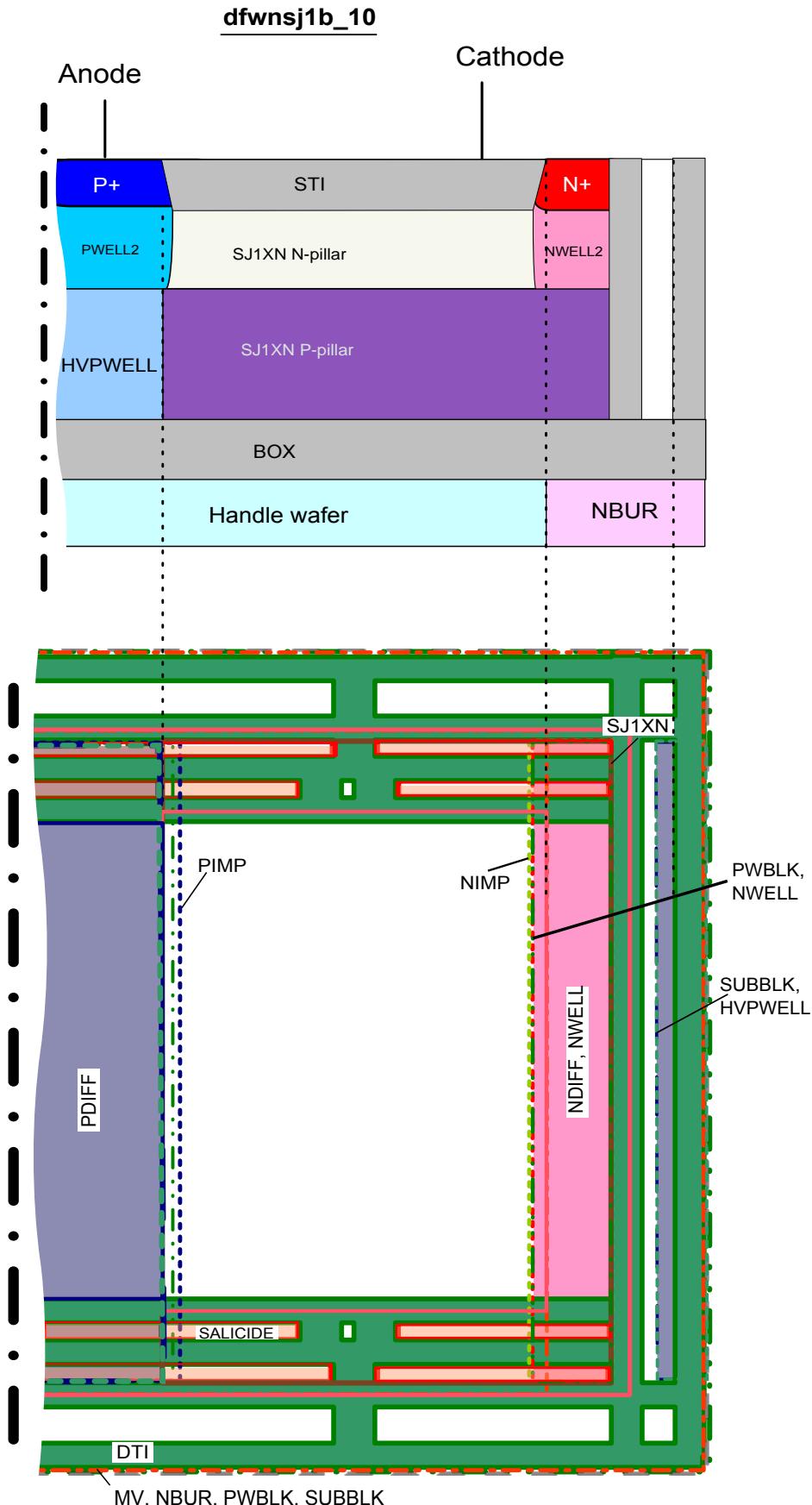
**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1b\_10m3" using DEVLBL (VERIFICATION) layer.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1b\_10



**Figure 3.300** dfwnsj1b\_10

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1a\_13

### **dfwnsj1a\_13**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B8X1	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 26 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1a\_13 device must be labeled "dfwnsj1a\_13" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

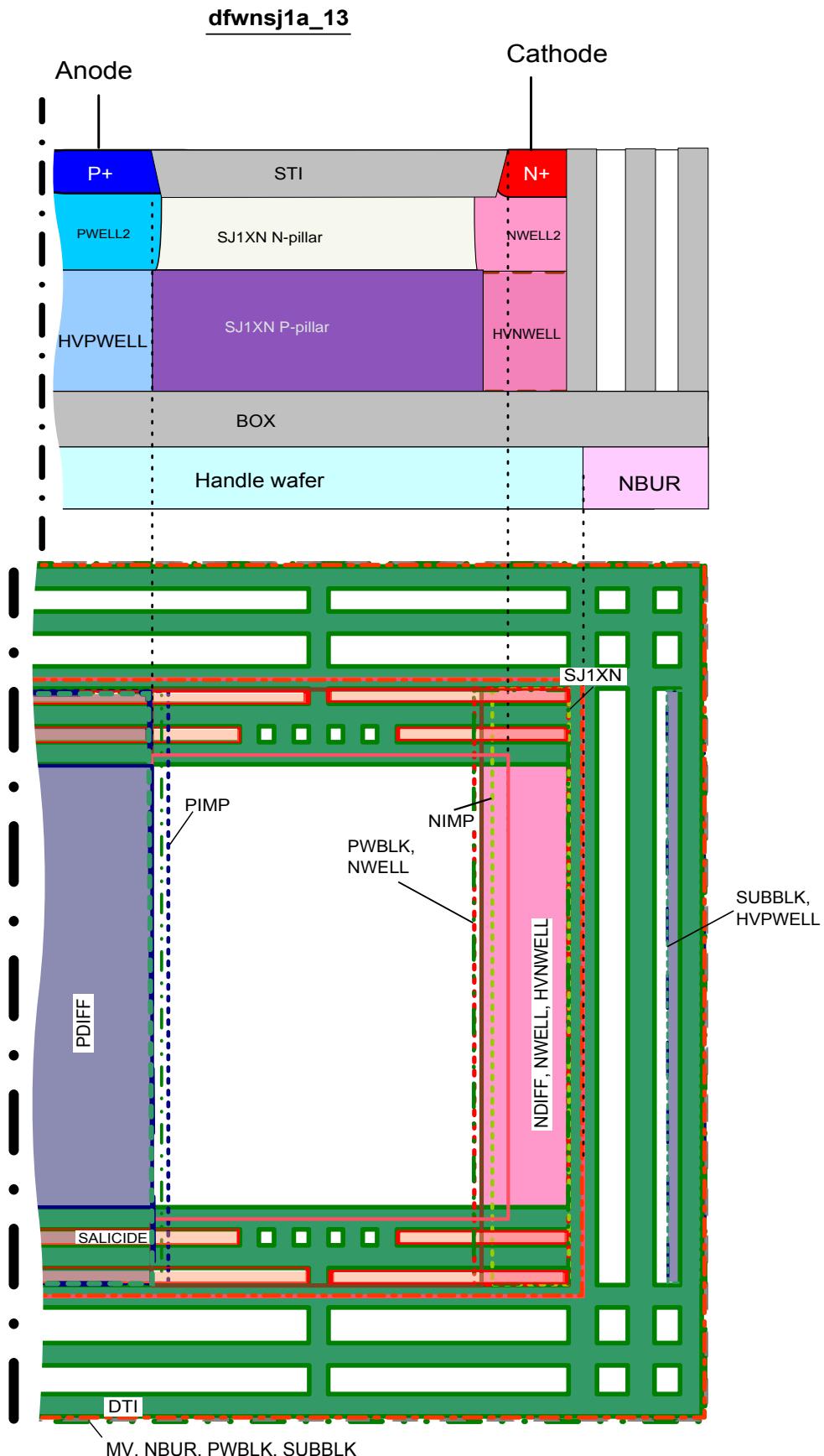
**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1a\_13m3" using DEVLBL (VERIFICATION) layer.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1a\_13



**Figure 3.301** dfwnsj1a\_13

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1a\_16

### **dfwnsj1a\_16**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-
B9X1	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-

**Note:** Minimum drawn finger width is 31 µm

**Note:** MV is necessary for this device.

**Note:** dfwnsj1a\_16 device must be labeled "dfwnsj1a\_16" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1a\_16m3" using DEVLBL (VERIFICATION) layer.

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1a\_16

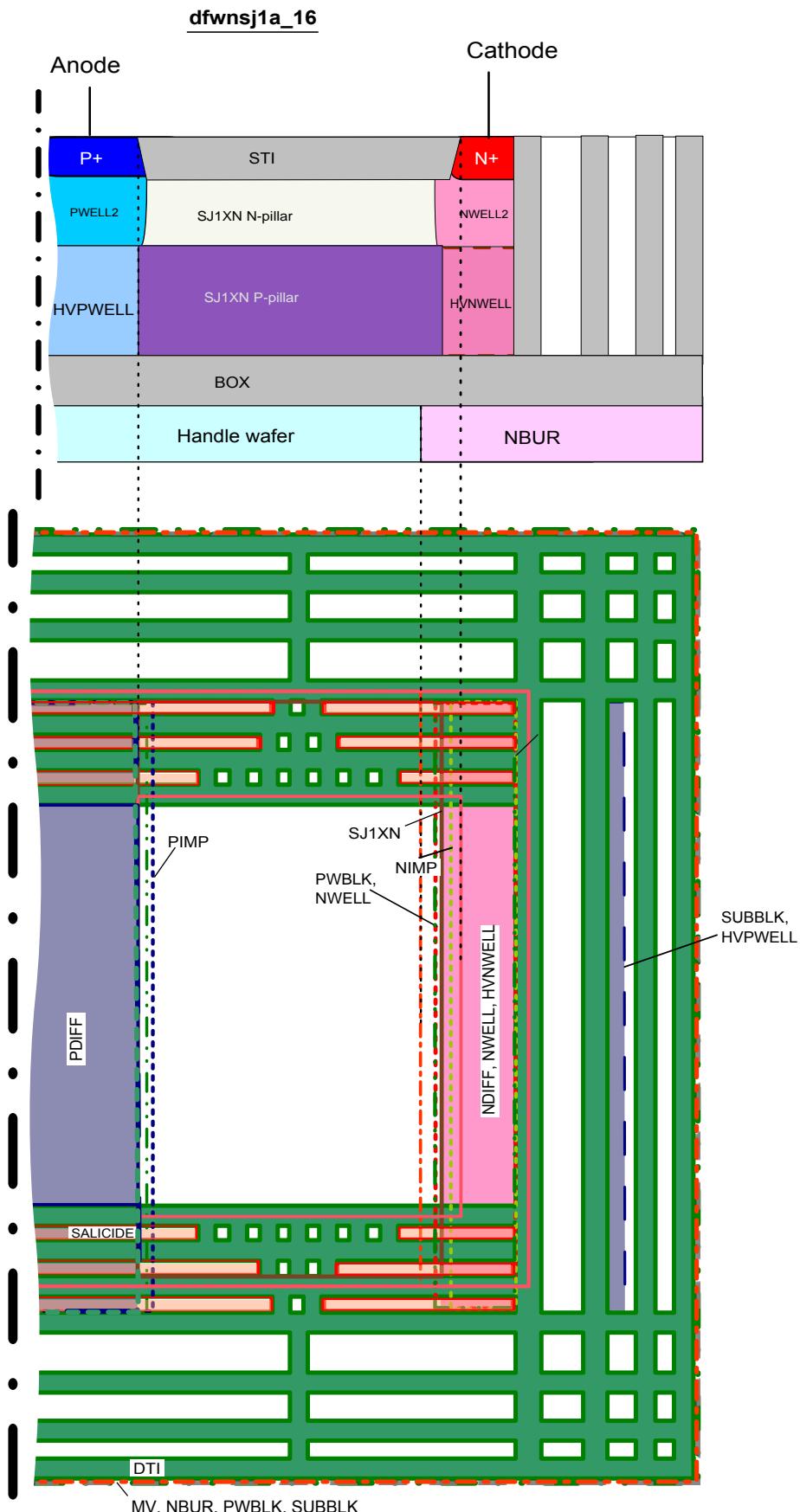


Figure 3.302 dfwnsj1a\_16

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1a\_20

### **dfwnsj1a\_20**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10X1	This device must be used together with a dhw4d or dhw5d	-	-
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B14X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-

**Note:** MV is necessary for this device.

**Note:** dfwnsj1a\_20 device must be labeled "dfwnsj1a\_20" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw4d or dhw5d is not shown in the diagram.

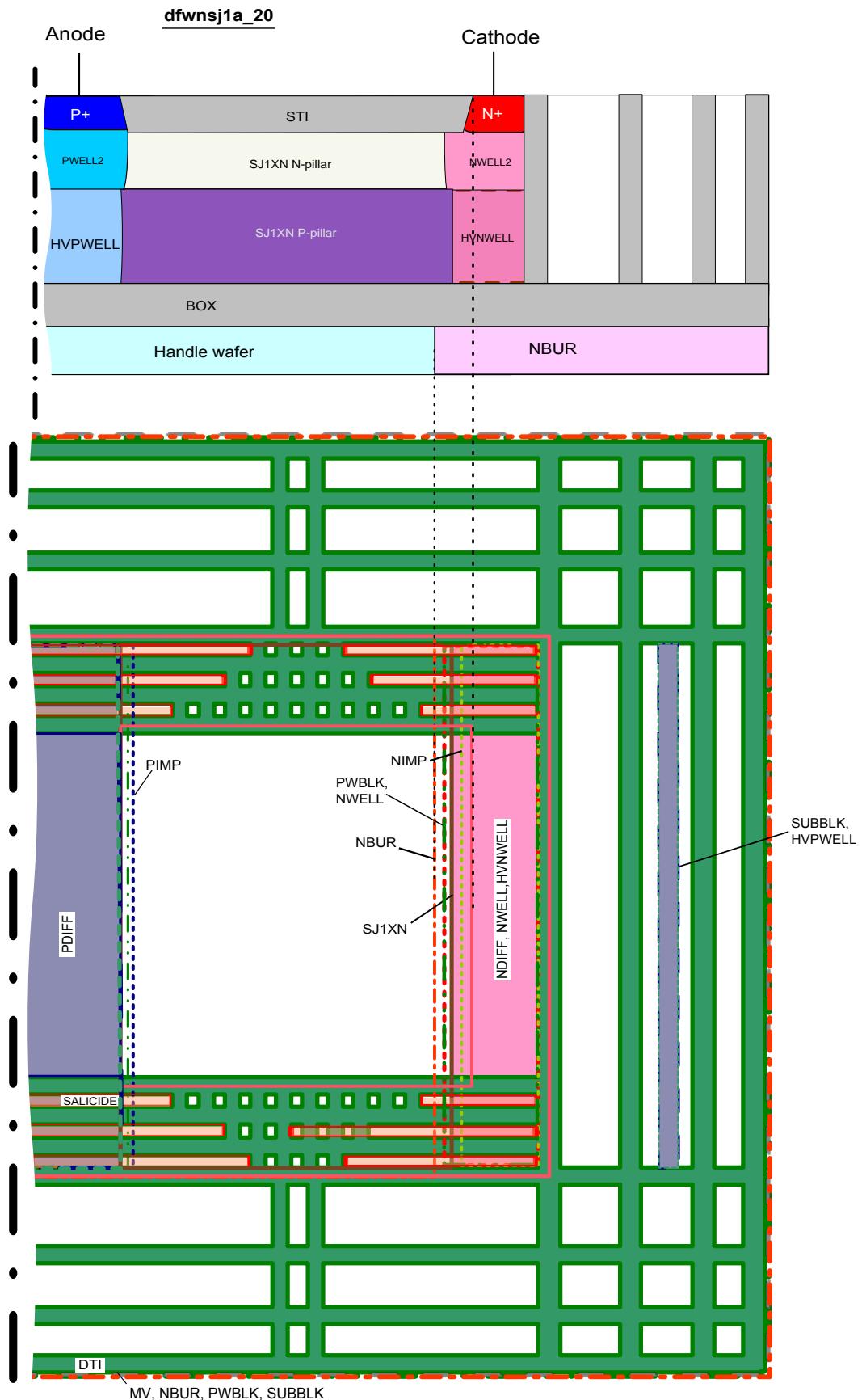
**Note:** Minimum drawn finger width is 61 µm

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1a\_20m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1a\_20



**Figure 3.303 dfwnsj1a\_20**

3. Layer and Device rules → 3.38 SJ1XN module→ 3.38.2 Device rules→ dfwnsj1a\_28

### **dfwnsj1a\_28**

The layout is predefined and scalable concerning device width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11X1	This device must be used together with dhw5d	-	-
B13X1	MET2 is not allowed over SJ1XN (except predefined MET2 device terminal connections)	-	-
B14X1	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XN (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X1	METTP, METTPL are not allowed over SJ1XN (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X1	Fixed orientation is 0 degree or 180 degree	-	-

**Note:** MV is necessary for this device.

**Note:** dfwnsj1a\_28 device must be labeled "dfwnsj1a\_28" using DIODEF (VERIFICATION) layer over (SJ1XN AND NOT NWELL) inside the innermost DTI hole.

**Note:** NBUR connection to dhw5d is not shown in the diagram.

**Note:** Minimum drawn finger width is 61 µm

**Note:** Each diode must be surrounded by DTI ring

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "dfwnsj1a\_28m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.38 SJ1XN module → 3.38.2 Device rules → dfwnsj1a\_28

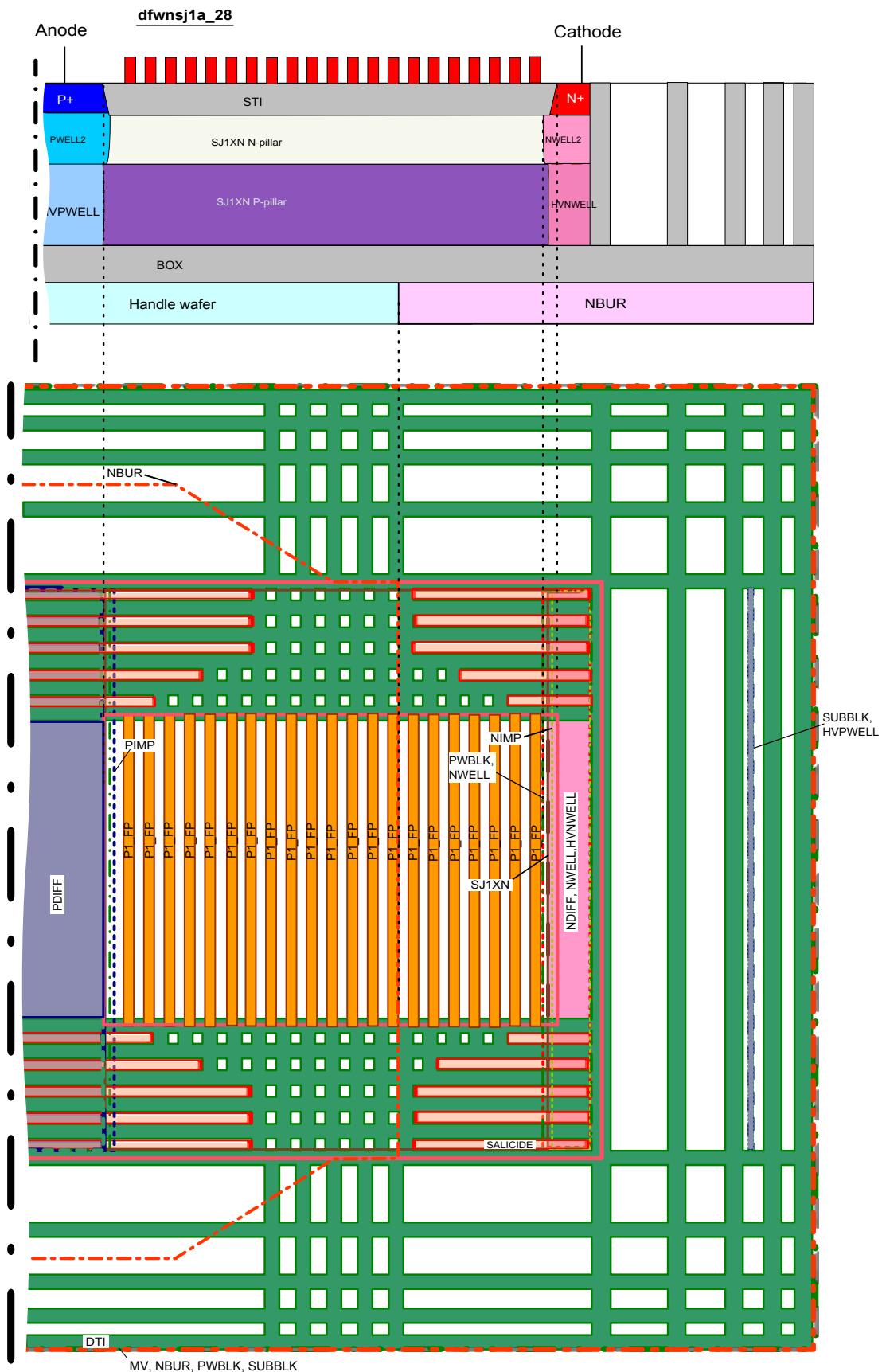


Figure 3.304 dfwnsj1a\_28

3. Layer and Device rules → 3.39 SJ1XP module

## 3.39 SJ1XP module

### 3.39.1 Layer rules

#### SJ1XP

Name	Description	Value	Unit
B12X2	MET1 is not allowed over SJ1XP (except predefined MET1 device terminal connections, M1_FP)	-	-
B1X2	SJ1XP without MV is not allowed	-	-
B2X2	SJ1XP overlap of HWTUB, DNC, DPC, HVNWELL, HVPWELL, HRES, MRES, DEPL, PWELL4 is not allowed	-	-
B3X2	SJ1XP overlap of NDF, PDF, NDFMV, PDFMV, DFN, DFP, NBASE, PBASE is not allowed	-	-
B4X2	SJ1XP overlap of SJNP, SJPN, NBUF, SJ1XN is not allowed	-	-
W1X2	Minimum SJ1XP width	2.0	μm
S1X2	Minimum SJ1XP spacing / notch	1.5	μm
S1X2NF	Minimum SJ1XP spacing to NBUF	2.0	μm
S1X2NT	Minimum SJ1XP spacing to SJNP	2.0	μm
S1X2PT	Minimum SJ1XP spacing to SJPN	2.0	μm
S1X2X4	Minimum SJ1XP spacing to SJ2XP	2.0	μm
A1X2	Minimum SJ1XP area	9.5	μm <sup>2</sup>

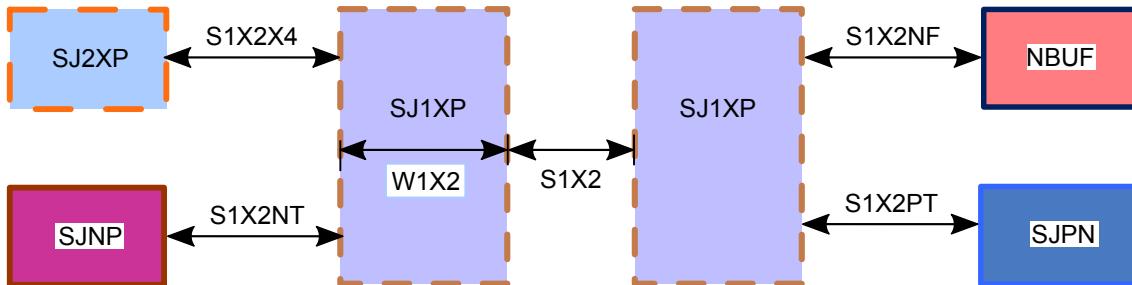


Figure 3.305 SJ1XP

#### SJ1XP\_E

Name	Description	Value	Unit
W2X2	Minimum SJ1XP_E width	0.5	μm

### 3.39.2 Device rules

#### phsj1a\_4

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B6X2	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm

⇒

## 3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_4

Name	Description	Value	Unit
W53GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	µm

**Note:** phsj1a\_4 device must be labeled "phsj1a\_4" using POLY1 (VERIFICATION) layer over GATE

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.39 SJ1XP module → 3.39.2 Device rules → phsj1a\_4

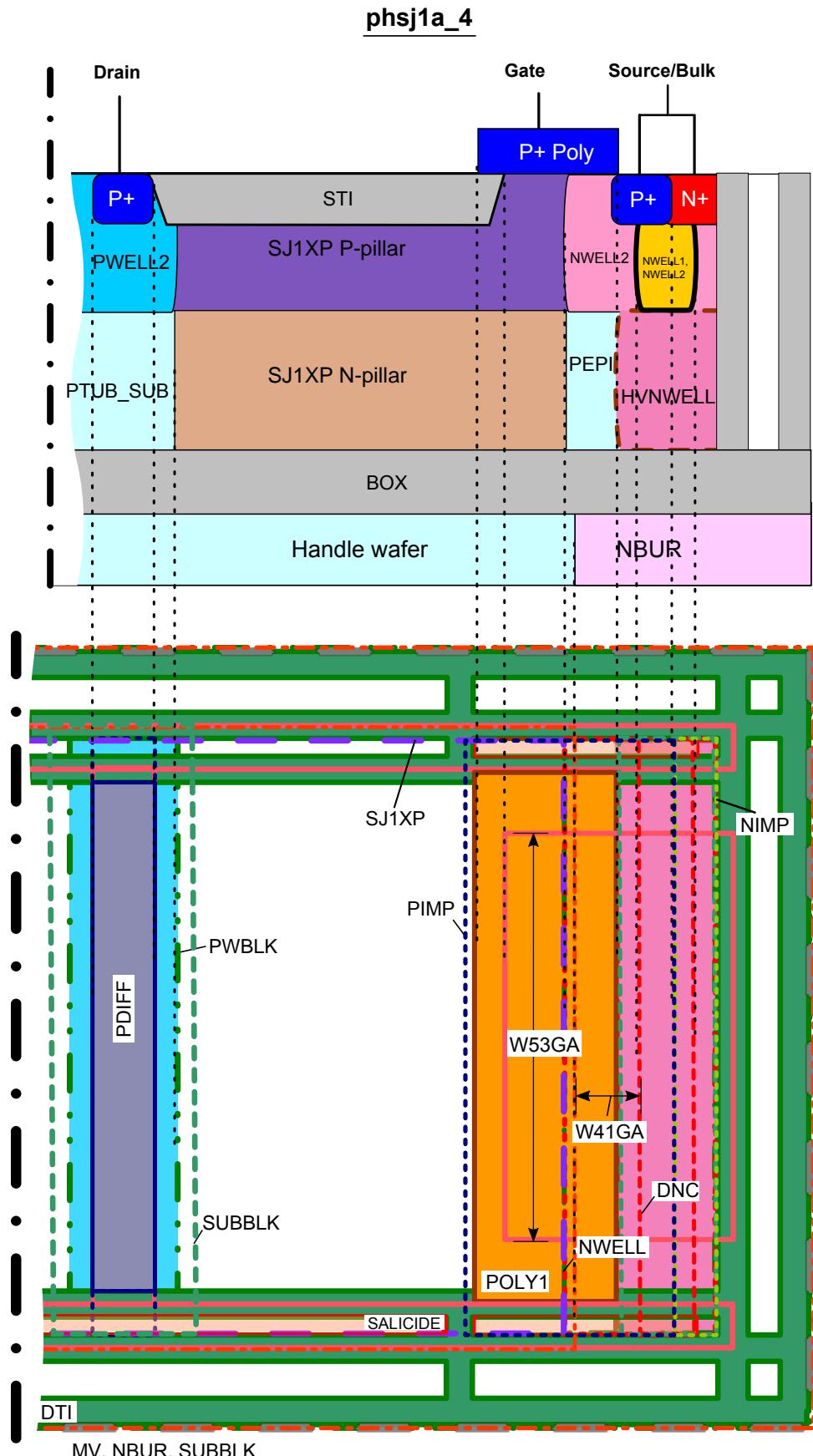


Figure 3.306 phsj1a\_4

3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_5

### **phsj1a\_5**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B6X2	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj1a\_5 device must be labeled "phsj1a\_5" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.39 SJ1XP module → 3.39.2 Device rules → phsj1a\_5

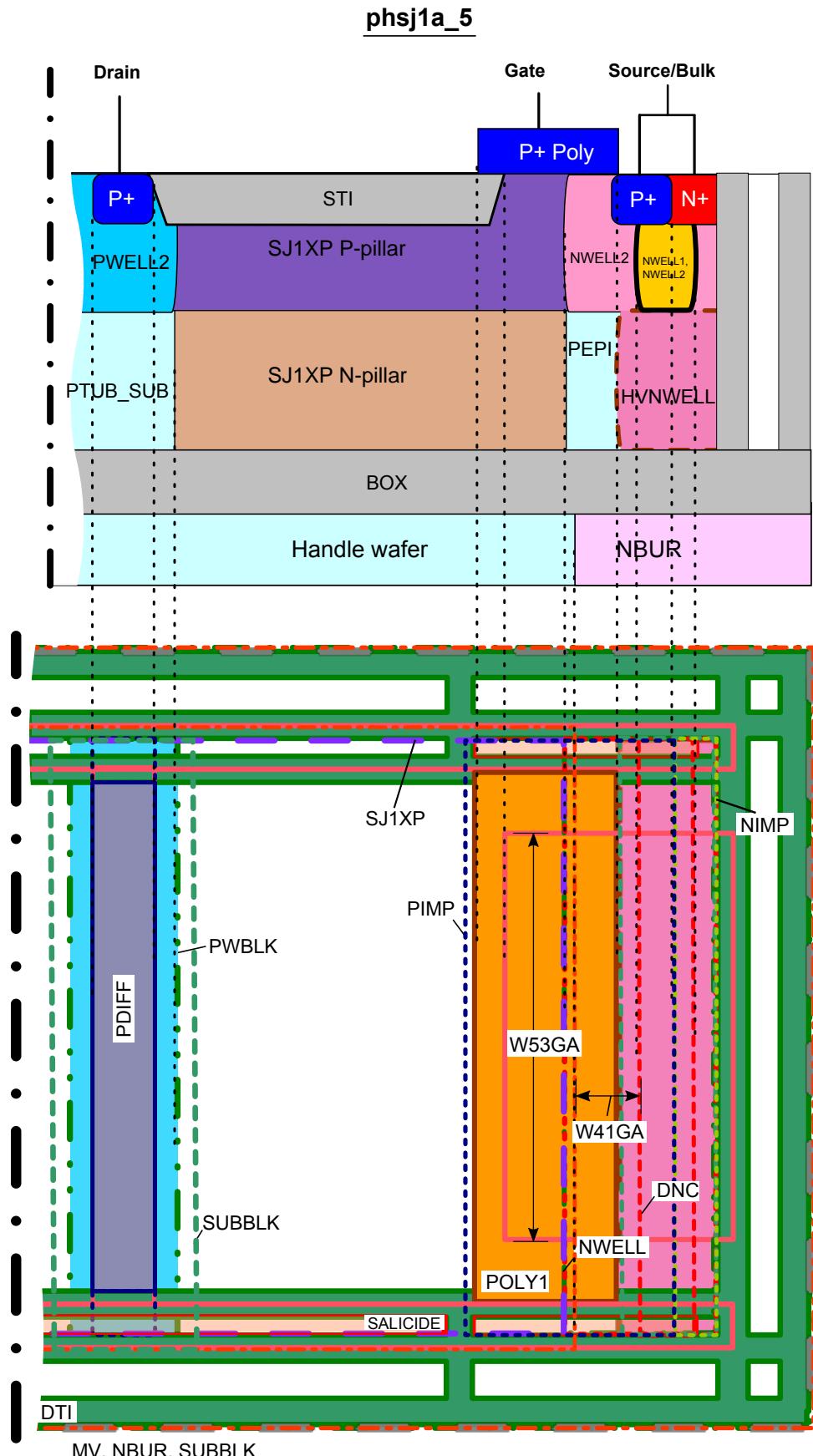


Figure 3.307 phsj1a\_5

3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_7

### **phsj1a\_7**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B6X2	This device must be used together with a dhw2b, dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj1a\_7 device must be labeled "phsj1a\_7" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Only metal wiring connected to the device terminals should be run over the drift region.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

3. Layer and Device rules → 3.39 SJ1XP module → 3.39.2 Device rules → phsj1a\_7

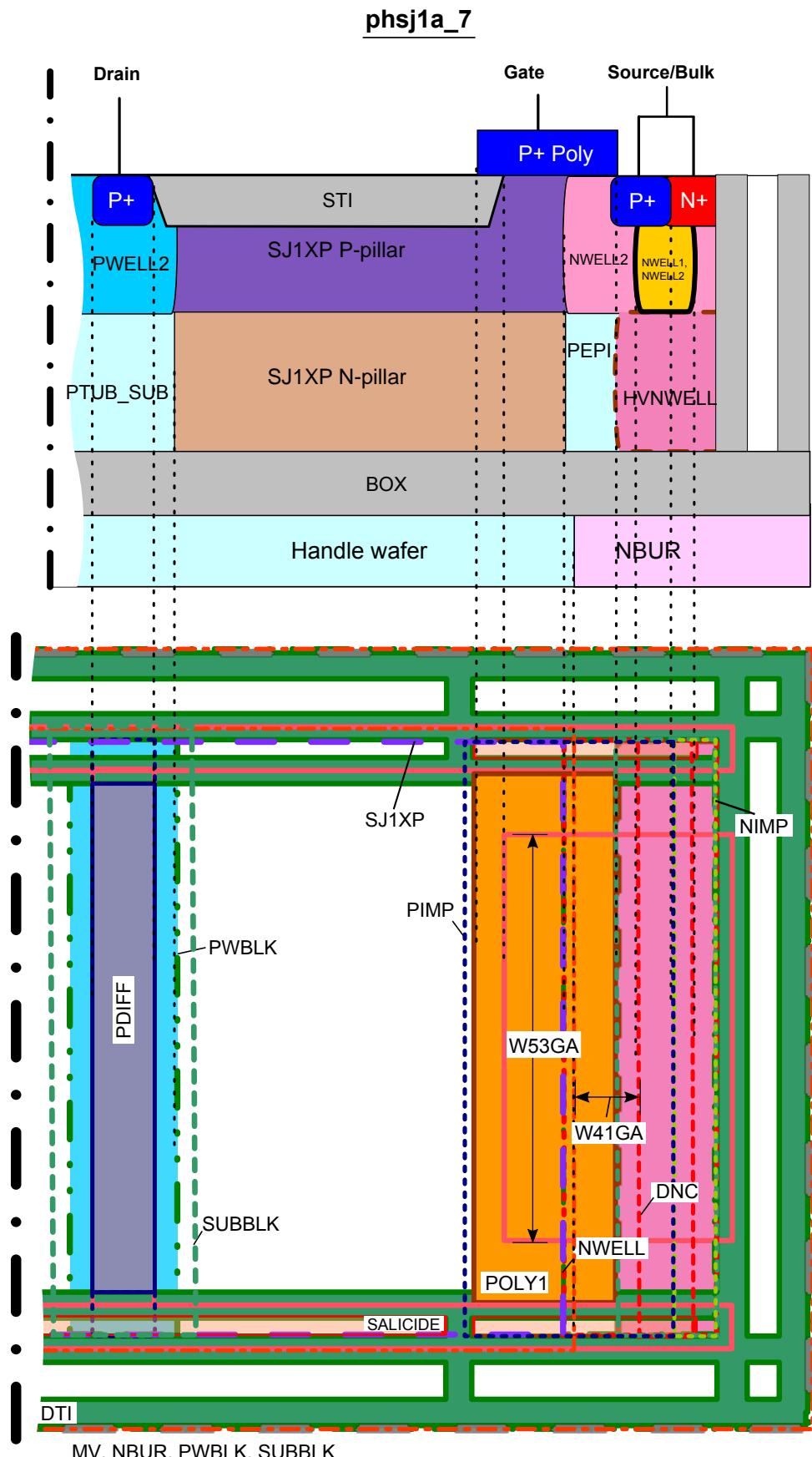


Figure 3.308 phsj1a\_7

3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_8

### **phsj1a\_8**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B7X2	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width	10.0	μm
	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** phsj1a\_8 device must be labeled "phsj1a\_8" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_8m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.39 SJ1XP module → 3.39.2 Device rules → phsj1a\_8

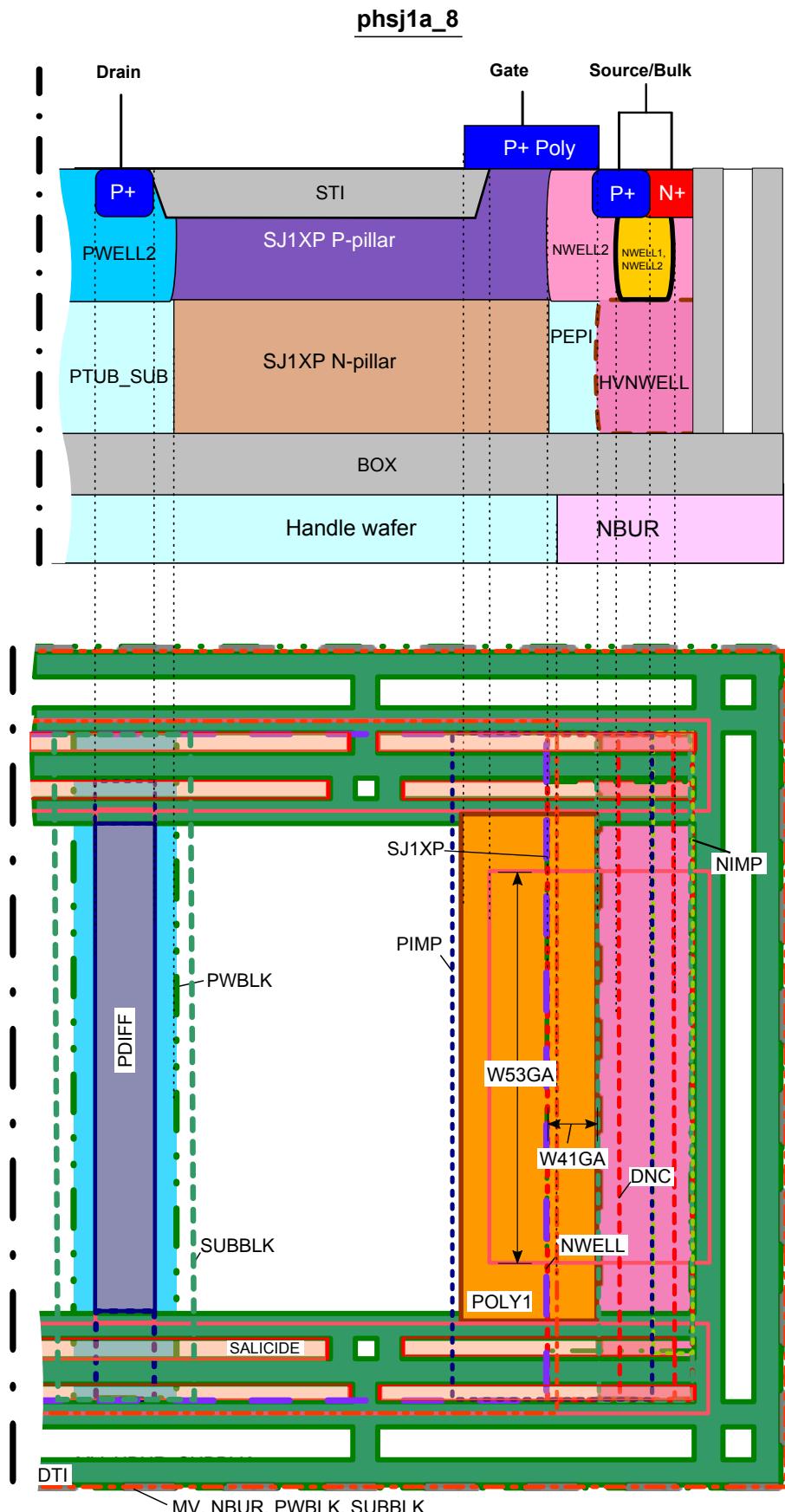


Figure 3.309 phsj1a\_8

3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_10

### **phsj1a\_10**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B7X2	This device must be used together with a dhw2c, dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W53GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	10.0	μm

**Note:** phsj1a\_10 device must be labeled "phsj1a\_10" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_10m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.39 SJ1XP module → 3.39.2 Device rules → phsj1a\_10

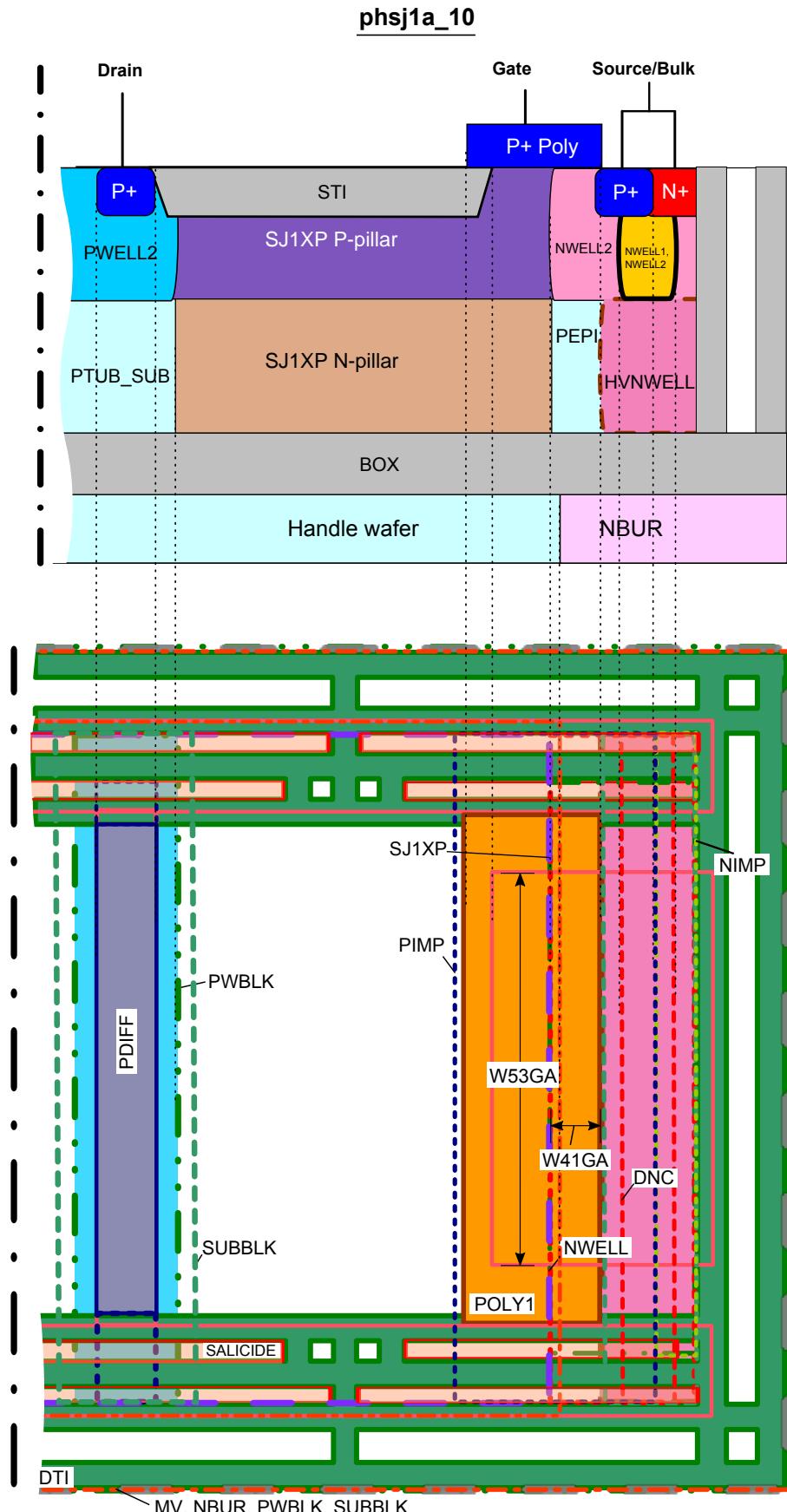


Figure 3.310 phsj1a\_10

3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_13

### **phsj1a\_13**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B16X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B8X2	This device must be used together with a dhw3c, dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
W54GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	25.0	μm

**Note:** phsj1a\_13 device must be labeled "phsj1a\_13" using POLY1 (VERIFICATION) layer over GATE

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_13m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.39 SJ1XP module → 3.39.2 Device rules → phsj1a\_13

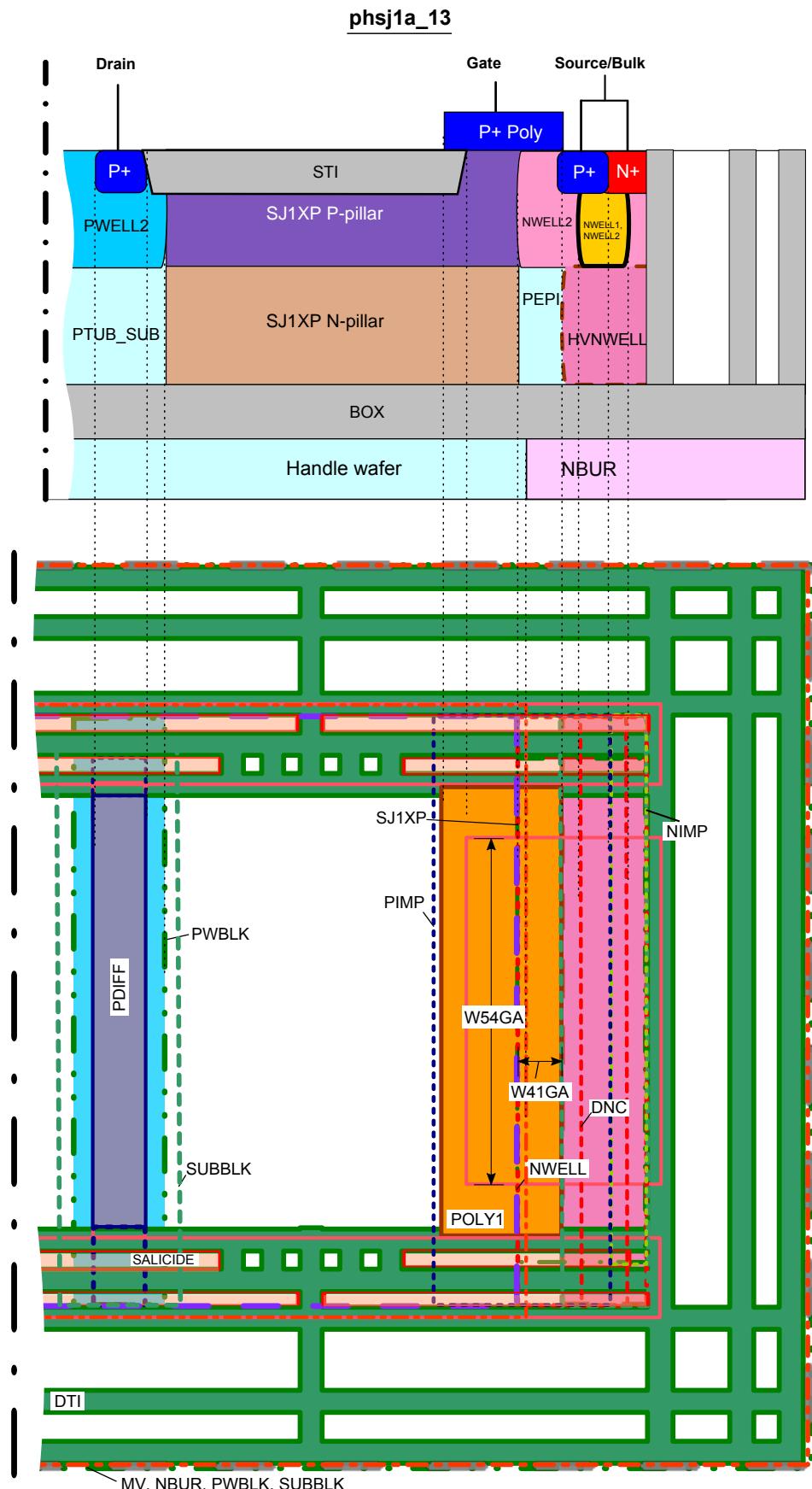


Figure 3.311 phsj1a\_13

3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_16

## **phsj1a\_16**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is not selected.		
B16X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)	-	-
	<b>Note:</b> Valid only if module MET3 is selected.		
	<b>Note:</b> Not valid if predefined MET3 Shield Plates are selected.		
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
B9X2	This device must be used together with a dhw4c, dhw4d or dhw5d	-	-
W41GA	Fixed CHANNEL length	0.5	μm
	Minimum GATE width	30.0	μm
W55GA	<b>Note:</b> Minimum GATE width is defined as single GATE finger width.		
	<b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.		

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw#c or dhw#d is not shown in the diagram.

**Note:** phsj1a\_16 device must be labeled "phsj1a\_16" using POLY1 (VERIFICATION) layer over GATE

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_16m3" using DEVLBL (VERIFICATION) layer.

3. Layer and Device rules → 3.39 SJ1XP module → 3.39.2 Device rules → phsj1a\_16

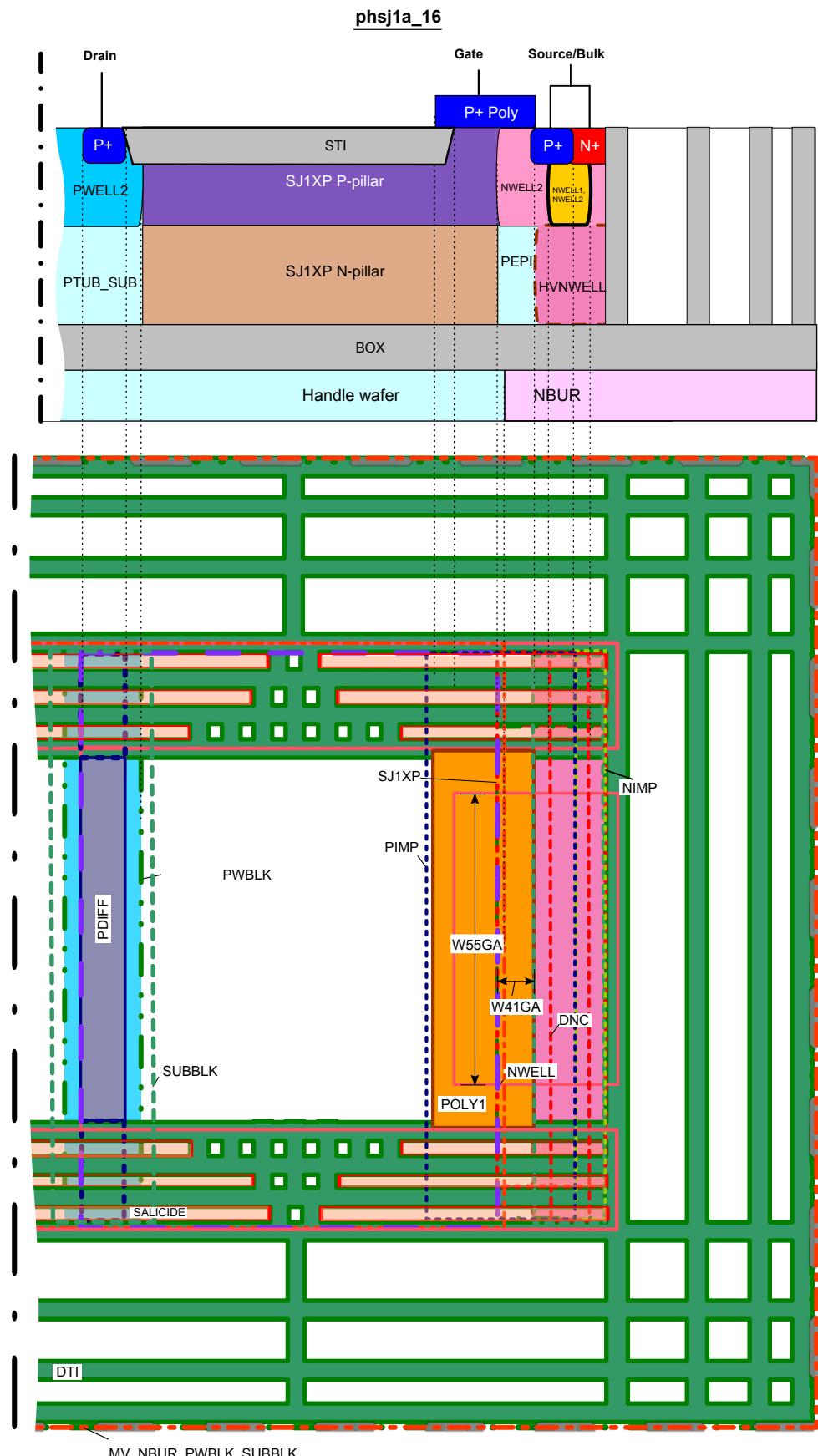


Figure 3.312 phsj1a\_16

3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_20

## **phsj1a\_20**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B10X2	This device must be used together with a dhw4d or dhw5d	-	-
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B14X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
W41GA	Fixed CHANNEL length	0.5	µm
W60GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	60.0	µm

**Note:** MV is necessary for this device.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** phsj1a\_20 device must be labeled "phsj1a\_20" using POLY1 (VERIFICATION) layer over GATE.

**Note:** NBUR connection to dhw4d or dhw5d is not shown in the diagram.

**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_20m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_20

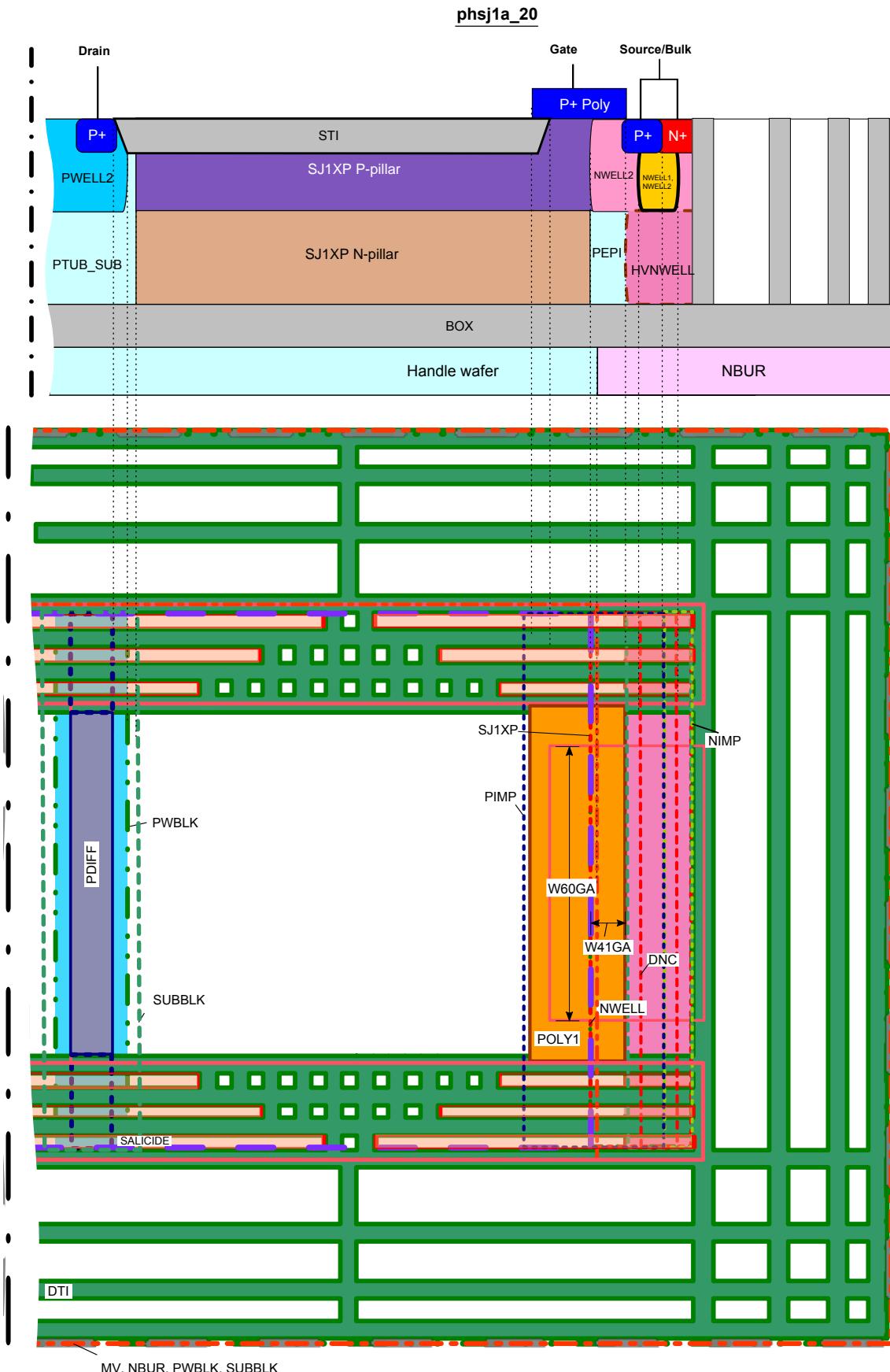


Figure 3.313 phsj1a\_20

3. Layer and Device rules → 3.39 SJ1XP module→ 3.39.2 Device rules→ phsj1a\_31

### **phsj1a\_31**

The layout is predefined and scalable concerning width only. All other dimensions must not be changed. The other rules support the fixed dimension of layout or describe the relation to adjacent structures.

Name	Description	Value	Unit
B11X2	This device must be used together with dhw5d	-	-
B13X2	MET2 is not allowed over SJ1XP (except predefined MET2 device terminal connections)	-	-
B14X2	MET3, MET4, MET5, METTP, METTPL are not allowed over SJ1XP (except predefined MET3, MET4, MET5, METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is selected.  <b>Note:</b> Except if predefined MET3 Shield Plates are selected AND finger width is greater than 200µm.	-	-
B15X2	METTP, METTPL are not allowed over SJ1XP (except predefined METTP, METTPL device terminal connections)  <b>Note:</b> Valid only if module MET3 is not selected.	-	-
B5X2	Fixed orientation is 0 degree or 180 degree	-	-
W41GA	Fixed CHANNEL length	0.5	µm
W80GA	Minimum GATE width  <b>Note:</b> Minimum GATE width is defined as single GATE finger width.  <b>Note:</b> Minimum GATE width is defined as minimum GATE finger width.	80.0	µm

**Note:** MV is necessary for this device.

**Note:** phsj1a\_31 device must be labeled "phsj1a\_31" using POLY1 (VERIFICATION) layer over GATE.

**Note:** Each transistor must be surrounded by DTI ring.

**Note:** NBUR connection to dhw5d is not shown in the diagram.

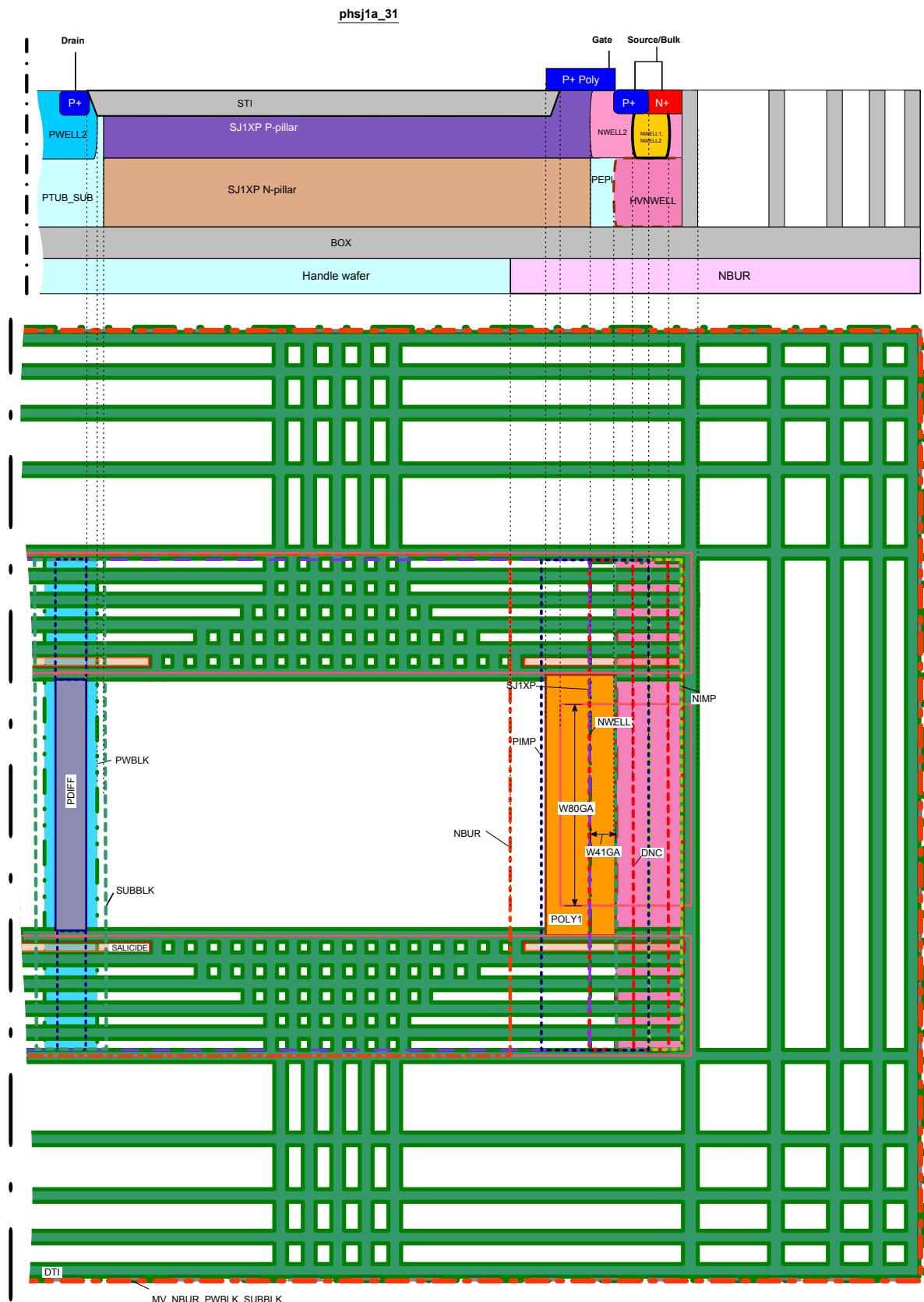
**Note:** This device is the type of Source-Drain-Source design. Drain-Source-Drain or Source-Drain design is forbidden.

**Note:** Source and Bulk must be butted.

**Note:** The DTI edge termination is predefined and must not be changed.

**Note:** In case MET3 Shield Plates are selected, device must be labeled "phsj1a\_31m3" using DEVLBL (VERIFICATION) layer.

## 3. Layer and Device rules → 3.39 SJ1XP module → 3.39.2 Device rules → phsj1a\_31

**Figure 3.314 phsj1a\_31**

3. Layer and Device rules → 3.40 DIODEA module

## 3.40 DIODEA module

### 3.40.1 Layer rules

#### PWELL4

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design.

Name	Description	Value	Unit
B1P4	PWELL4 is only allowed for nhv#, ndhv#, dfwdn#, dnpa, dnpati, nhvr#, ndhvr# or dfwdnh#	-	-
B2P4	PWELL4 overlap of NWELL, DPC, HVPWELL, SJNP or SJPN is not allowed	-	-
B4P4	PWELL4 without MV and SUBBLK is not allowed	-	-
W1P4	Minimum PWELL4 width	1.0	μm
S1P4	Minimum PWELL4 spacing/notch	1.0	μm
S1P4DN	Minimum PWELL4 spacing to NDIFF	0.25	μm
E1P4DN	Minimum PWELL4 enclosure of NDIFF	0.43	μm
E1P4DP	Minimum PWELL4 enclosure of PDIFF (except dfwdn#, dfwdnh#)	0.25	μm
A1P4	Minimum PWELL4 area	2.25	μm <sup>2</sup>

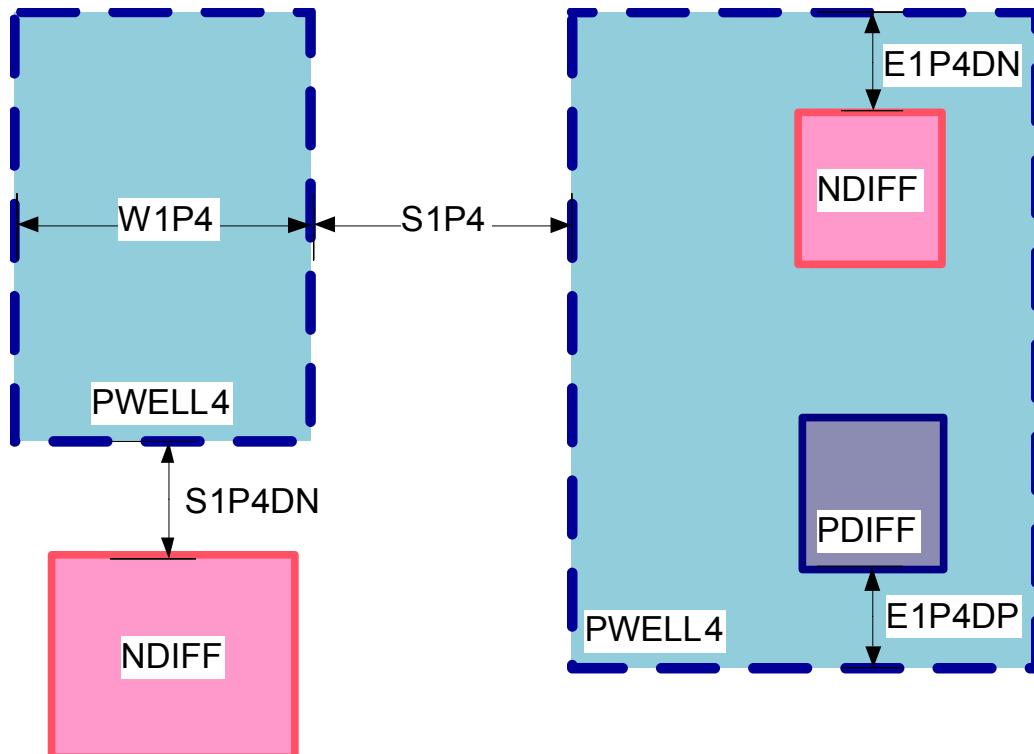


Figure 3.315 PWELL4

#### PWELL4\_E

Name	Description	Value	Unit
W2P4	Minimum PWELL4_E width	0.5	μm

3. Layer and Device rules → 3.40 DIODEA module→ 3.40.2 Device rules→ dnpa

### 3.40.2 Device rules

#### dnpa

The layout of the dnpa protection diode is predefined and only the cathode width can be changed in the range of 2.0  $\mu\text{m}$  to 200.0  $\mu\text{m}$ . Fixed cathode length is 1.0  $\mu\text{m}$ .

Name	Description	Value	Unit
E1HBDN	Minimum SUBBLK enclosure of NDIFF	1.68	$\mu\text{m}$
E1MVP4	Minimum MV enclosure of PWELL4	0.5	$\mu\text{m}$

**Note:** A DTI ring is necessary, valid if Vanode is higher than the handle wafer voltage.

**Note:** MV, PWELL4, SUBBLK are necessary for this device

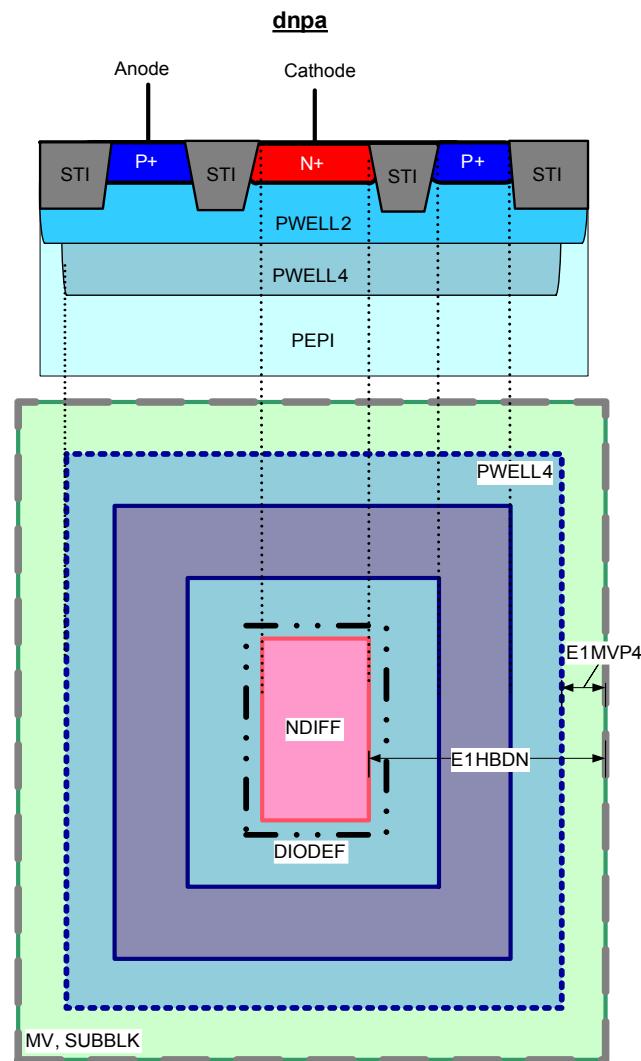


Figure 3.316 dnpa

3. Layer and Device rules → 3.40 DIODEA module→ 3.40.2 Device rules→ dnpati

### dnpati

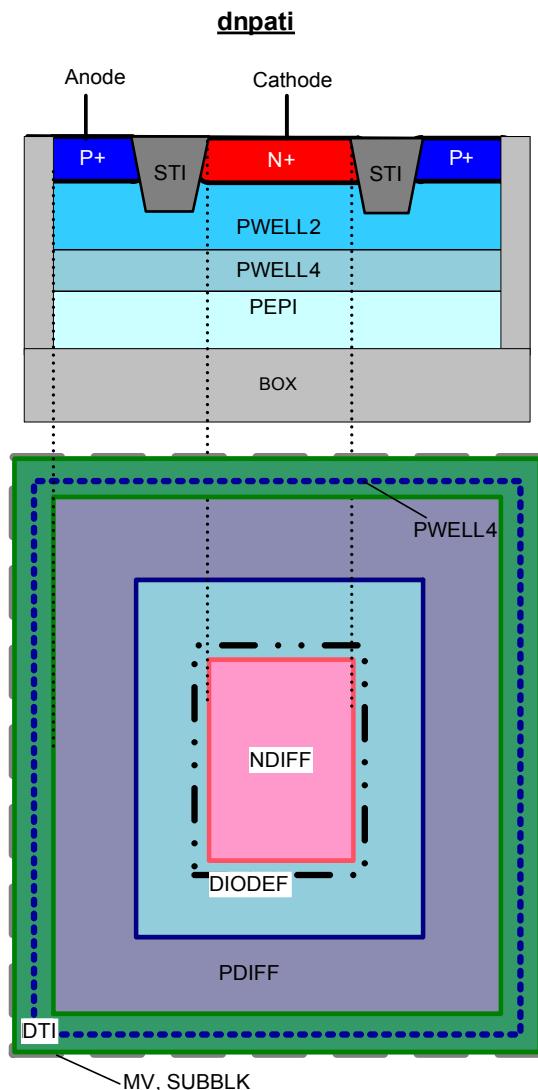
The layout of the dnpati protection diode is predefined and only the cathode width can be changed in the range of 2.0  $\mu\text{m}$  to 200.0  $\mu\text{m}$ . Fixed cathode length is 1.0  $\mu\text{m}$ .

**Note:** DTI ring is required for this device.

**Note:** dnpati device must be labeled "dnpati " using DIODEF (VERIFICATION).

**Note:** MV, PWELL4, SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.



**Figure 3.317** dnpati

3. Layer and Device rules → 3.41 DIODEB module

## 3.41 DIODEB module

### 3.41.1 Layer rules

#### PZENER

Name	Description	Value	Unit
B1PZ	PZENER overlap of DPC, NWELL, PWBLK or PWELL4 is not allowed	-	-
B2PZ	PZENER is only allowed for dza, dzati	-	-
B3PZ	PZENER without MV and SUBBLK is not allowed	-	-
W1PZ	Minimum PZENER width	0.6	μm
S1PZ	Minimum PZENER spacing/notch	0.6	μm
A1PZ	Minimum PZENER area	0.3844	μm <sup>2</sup>

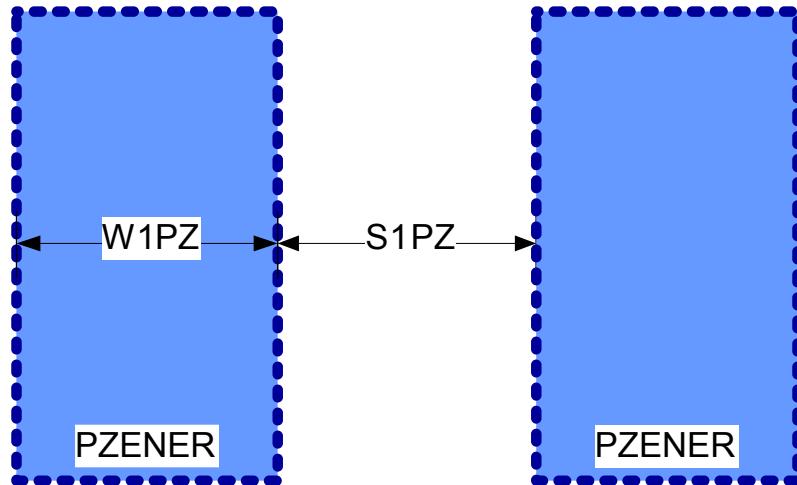


Figure 3.318 PZENER

#### PZENER\_E

Name	Description	Value	Unit
W2PZ	Minimum PZENER_E width	0.5	μm

### 3.41.2 Device rules

#### dza

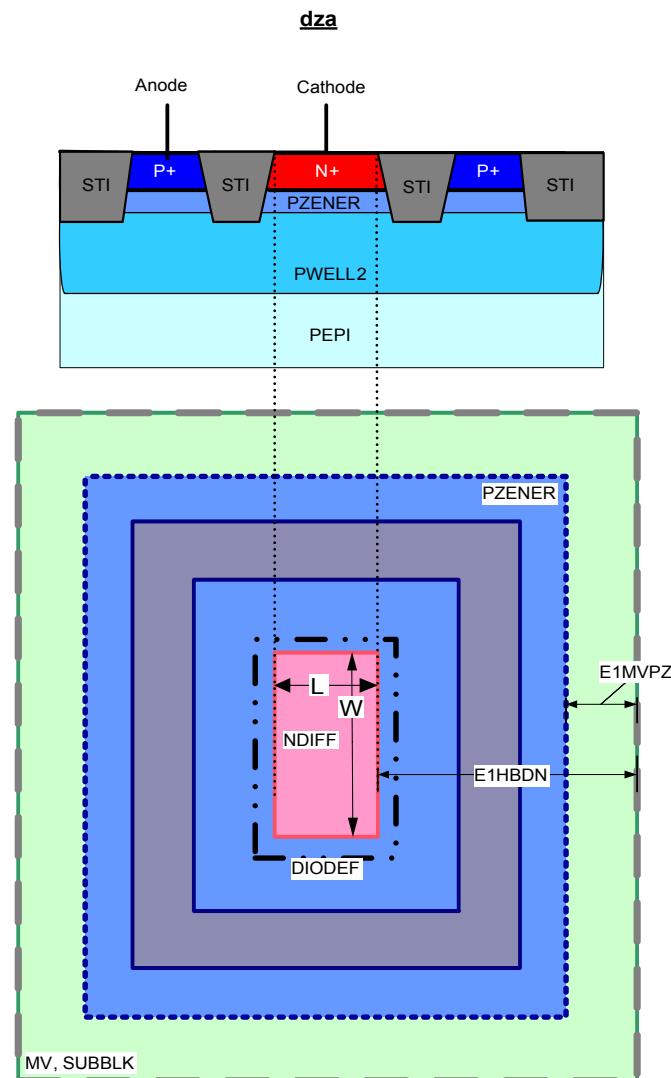
The layout of the dza protection diode is predefined and only the cathode width (defined by NDIFF AND PZENER) can be changed in the range of 2.0 μm to 200.0 μm. Fixed cathode length (defined by NDIFF AND PZENER) is 1.0 μm.

Name	Description	Value	Unit
E1HBDN	Minimum SUBBLK enclosure of NDIFF	1.68	μm
E1MVPZ	Minimum MV enclosure of PZENER	0.5	μm

**Note:** A DTI ring is necessary, valid if Vanode is higher than the handle wafer voltage.

**Note:** MV and SUBBLK are necessary for this device

3. Layer and Device rules → 3.41 DIODEB module→ 3.41.2 Device rules→ dza



**Figure 3.319 dza**

## 3. Layer and Device rules → 3.41 DIODEB module→ 3.41.2 Device rules→ dzati

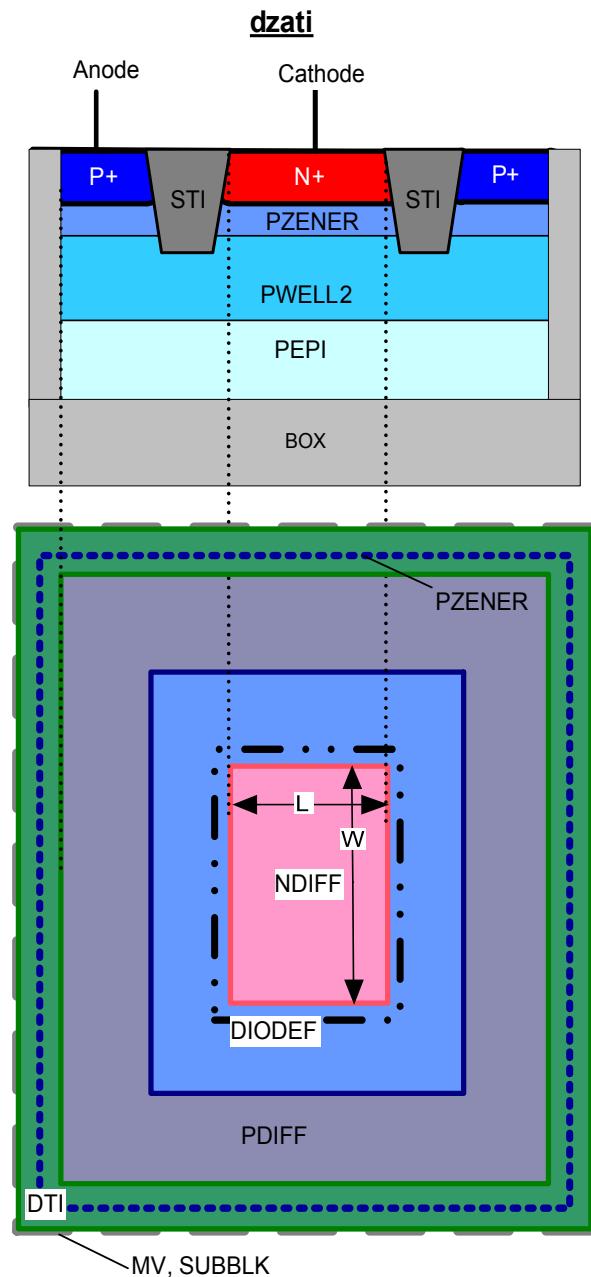
**dzati**

The layout of the dzati protection diode is predefined and only the cathode width (defined by NDIFF AND PZENER) can be changed in the range of 2.0  $\mu\text{m}$  to 200.0  $\mu\text{m}$ . Fixed cathode length (defined by NDIFF AND PZENER) is 1.0  $\mu\text{m}$ .

**Note:** DTI ring is required for this device.

**Note:** MV and SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.



**Figure 3.320** dzati

3. Layer and Device rules → 3.42 DIODEC module

## 3.42 DIODEC module

### 3.42.1 Layer rules

#### NZENER

Name	Description	Value	Unit
B1NZ	NZENER without NWELL and PDIFF is not allowed	-	-
B2NZ	NZENER is only allowed for dzbt, dzcti	-	-
B3NZ	NZENER overlap of DNC, PZENER, NBUR or HVNWELL is not allowed	-	-
B4NZ	NZENER without MV and SUBBLK is not allowed	-	-
W1NZ	Minimum NZENER width	0.6	μm
S1NZ	Minimum NZENER spacing/ notch	0.6	μm
A1NZ	Minimum NZENER area	0.3844	μm <sup>2</sup>

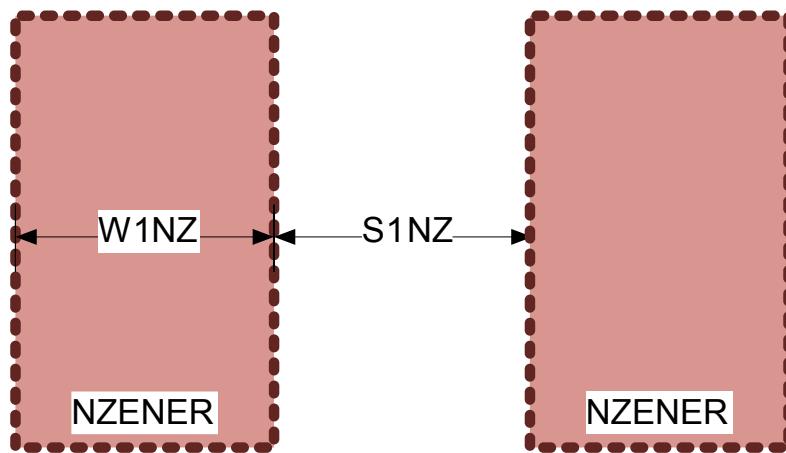


Figure 3.321 NZENER

#### NZENER\_E

Name	Description	Value	Unit
W2NZ	Minimum NZENER_E width	0.5	μm

### 3.42.2 Device rules

#### dzbt

The layout of the dzbt protection diode is predefined and only the anode width (defined by PDIFF AND NZENER) can be changed in the range of 5.0 μm to 25.0 μm. Fixed anode length (defined by PDIFF AND NZENER) is 1.16 μm.

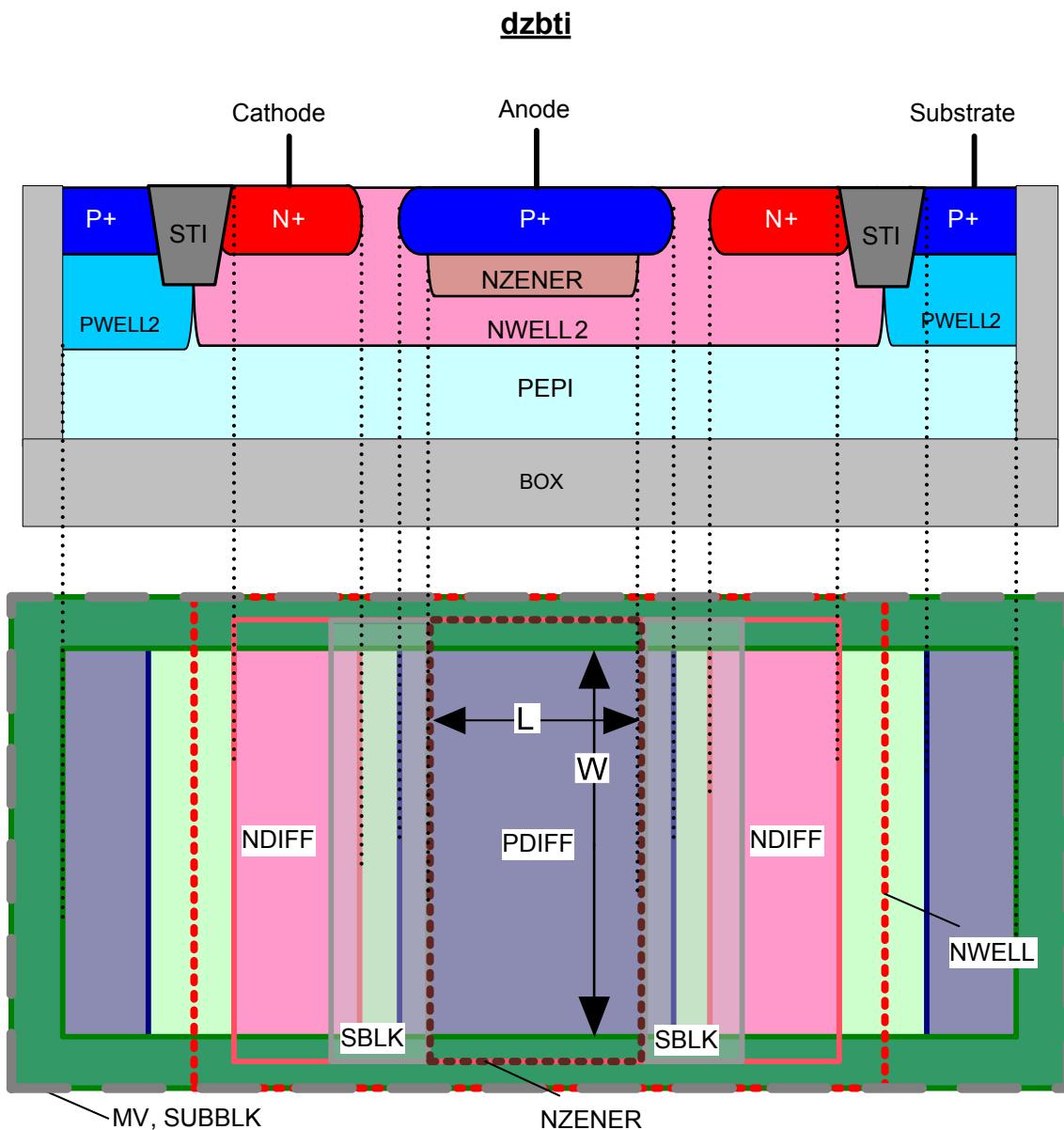
**Note:** DTI ring is required for this device.

**Note:** Maximum number of finger of dzbt is 8.

**Note:** MV and SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

3. Layer and Device rules → 3.42 DIODEC module→ 3.42.2 Device rules→ dzbt1



**Figure 3.322 dzbt1**

3. Layer and Device rules → 3.42 DIODEC module→ 3.42.2 Device rules→ dzcti

### **dzcti**

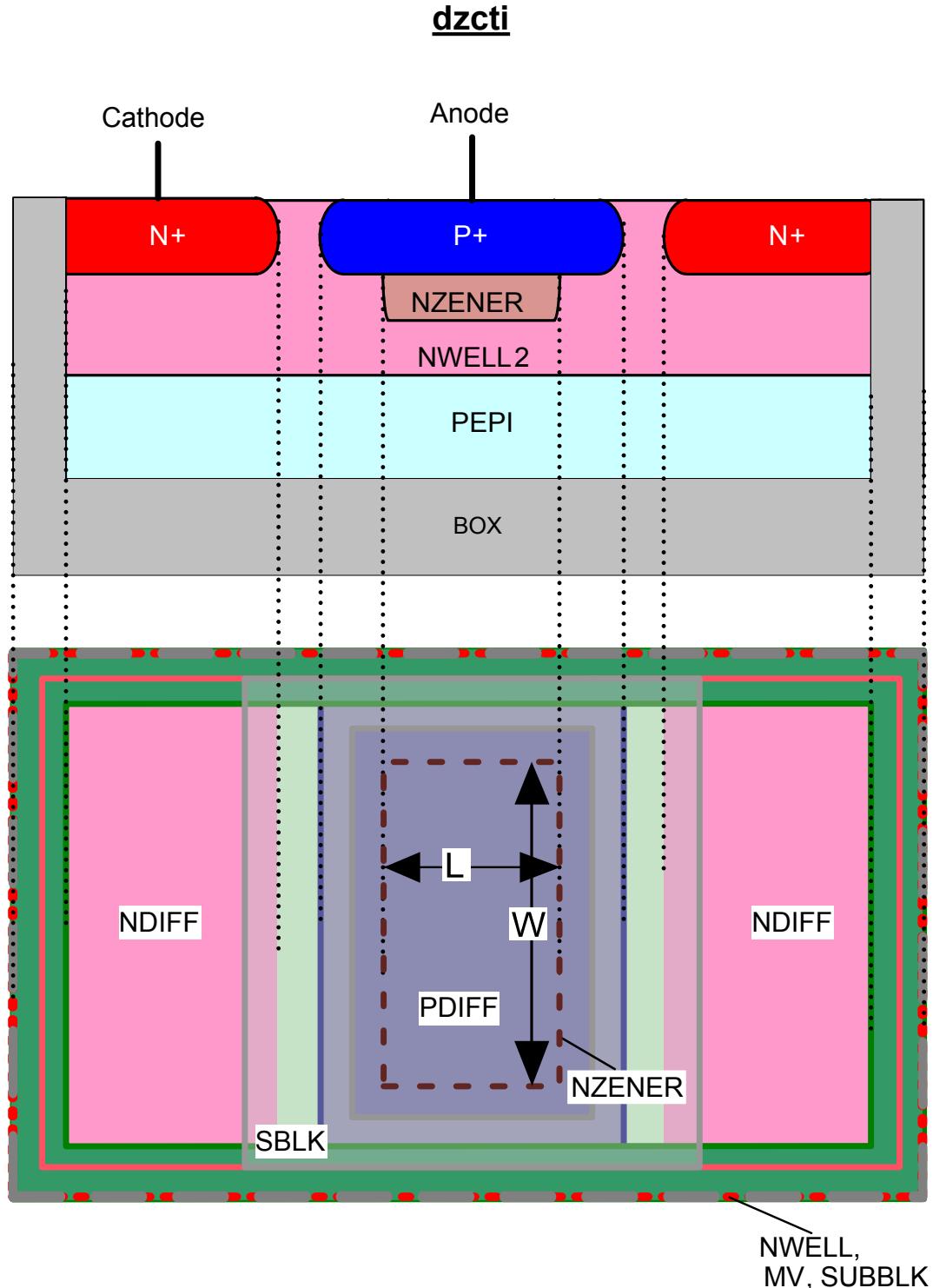
The layout of the dzcti protection diode is predefined and only the anode width (defined by PDIFF AND NZENER) can be changed in the range of 4.0  $\mu\text{m}$  to 24.0  $\mu\text{m}$ . Fixed anode length (defined by PDIFF AND NZENER) is 1.16  $\mu\text{m}$ .

**Note:** DTI ring is required for this device.

**Note:** MV and SUBBLK are necessary for this device

**Note:** Use >1DTI rings, if this device will be placed into HWPTUB.

**Note:** Maximum number of finger of dzcti is 8.



**Figure 3.323 dzcti**

3. Layer and Device rules → 3.43 MIM module

## 3.43 MIM module

### 3.43.1 Layer rules

#### CAPM

Name	Description	Value	Unit
B1CM	CAPM without BM is not allowed	-	-
B2CM	CAPM overlap of VIAn or PAD is not allowed	-	-
B3CM	CAPM is not allowed when CAPM23F, CAPM34F, CAPM45F, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B4CM	CAPM without module METMID is not allowed	-	-
W1CM	Minimum CAPM width	2.0	μm
W2CM	Maximum CAPM bounding box size  <b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	μm x μm
S1CM	Minimum CAPM spacing/notch	1.5	μm
S3VT	Minimum VIATP spacing on CAPM	2.0	μm
S1CMPA	Minimum CAPM spacing to PAD	10.0	μm
S1CMVN	Minimum CAPM spacing to VIAn	0.5	μm
S1CMVT	Minimum CAPM spacing to VIATP	0.5	μm
E1BMCM	Minimum BM enclosure of CAPM	0.5	μm
E1BMVN	Minimum BM enclosure of VIAn  <b>Note:</b> This rule is related to all VIAs inside CAPM regions extended by 2.5μm.	0.15	μm
E1BMVT	Minimum BM enclosure of VIATP  <b>Note:</b> This rule is related to all VIAs inside CAPM regions extended by 2.5μm.	0.15	μm
E1CMVT	Minimum CAPM enclosure of VIATP	0.3	μm
Q1VT	Recommended minimum ratio of VIATP to CAPM area	1.0	%

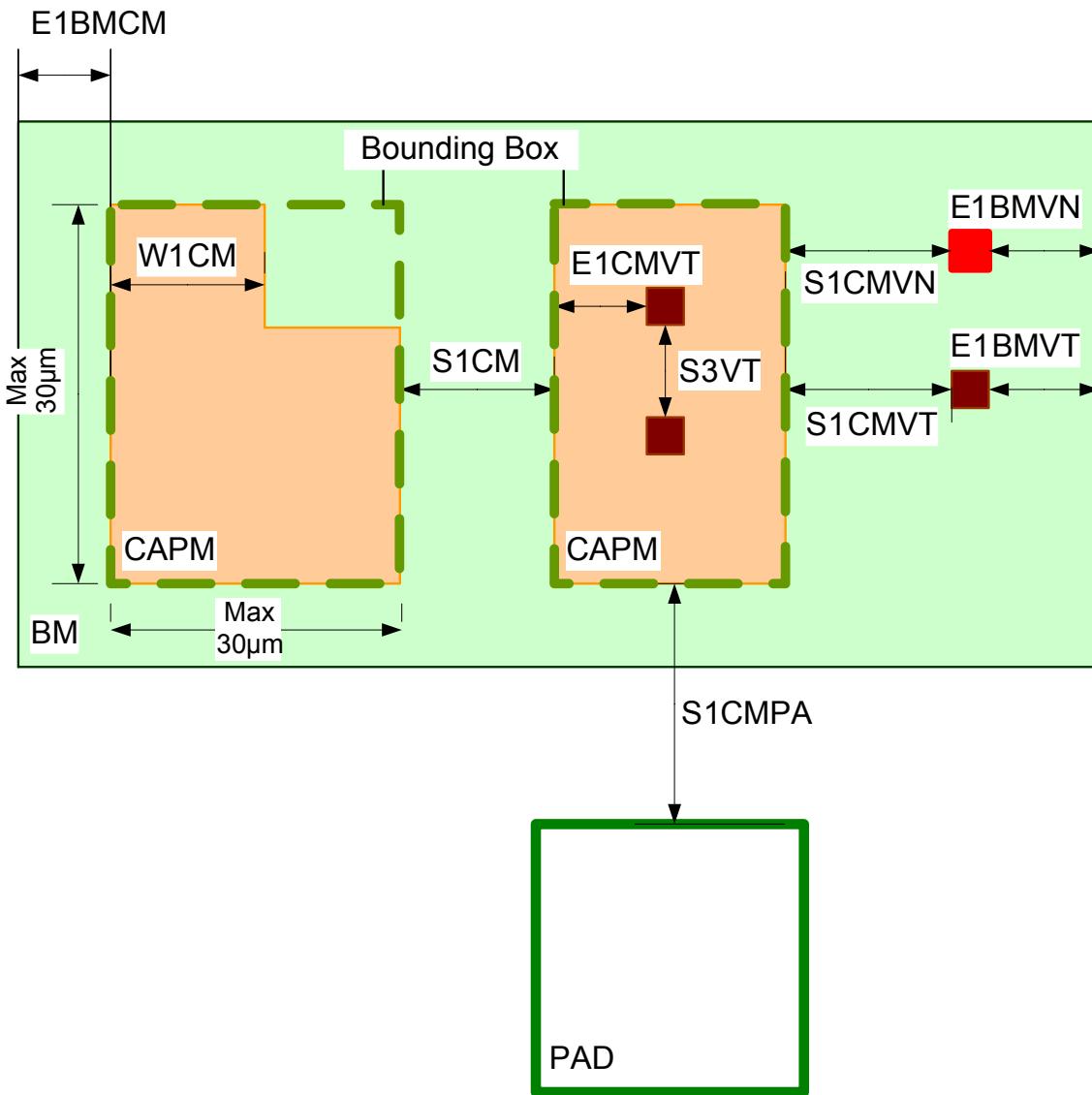
**Note:** The Single MIM Capacitor is located between the top metal and the metal layer underneath top metal. The table below shows the assignment of the MIM bottom layer BM and the via layer VIAn to the physical metal and via layers for the different metal module options.

Table for BM and VIAn assignment

module combination	bottom MIM metal (BM)	device	VIAn
LP5MOS/MOS5 and not MET3	MET2	cmm3t	VIA1
MET3 and not MET4	MET3	cmm4t	VIA2
MET4 and not MET5	MET4	cmm5t	VIA3
MET5	MET5	cmm6t	VIA4

3. Layer and Device rules → 3.43 MIM module→ 3.43.1 Layer rules→ CAPM

### CAPM

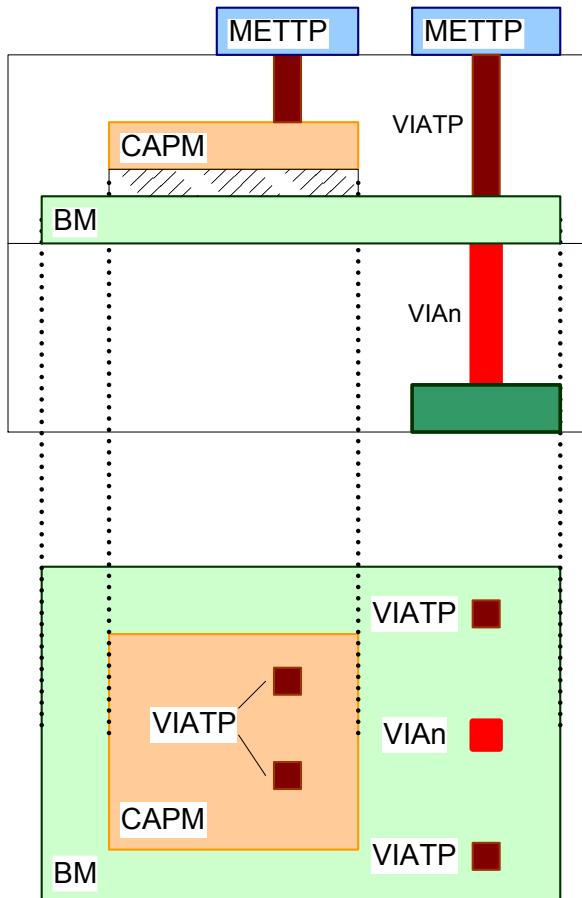


**Figure 3.324 CAPM**

3. Layer and Device rules → 3.43 MIM module→ 3.43.2 Device rules→ cmm3t, cmm4t, cmm5t,...

### 3.43.2 Device rules

cmm3t, cmm4t, cmm5t, cmm6t



**Figure 3.325** cmm3t, cmm4t, cmm5t, cmm6t

3. Layer and Device rules → 3.44 MIM23 module

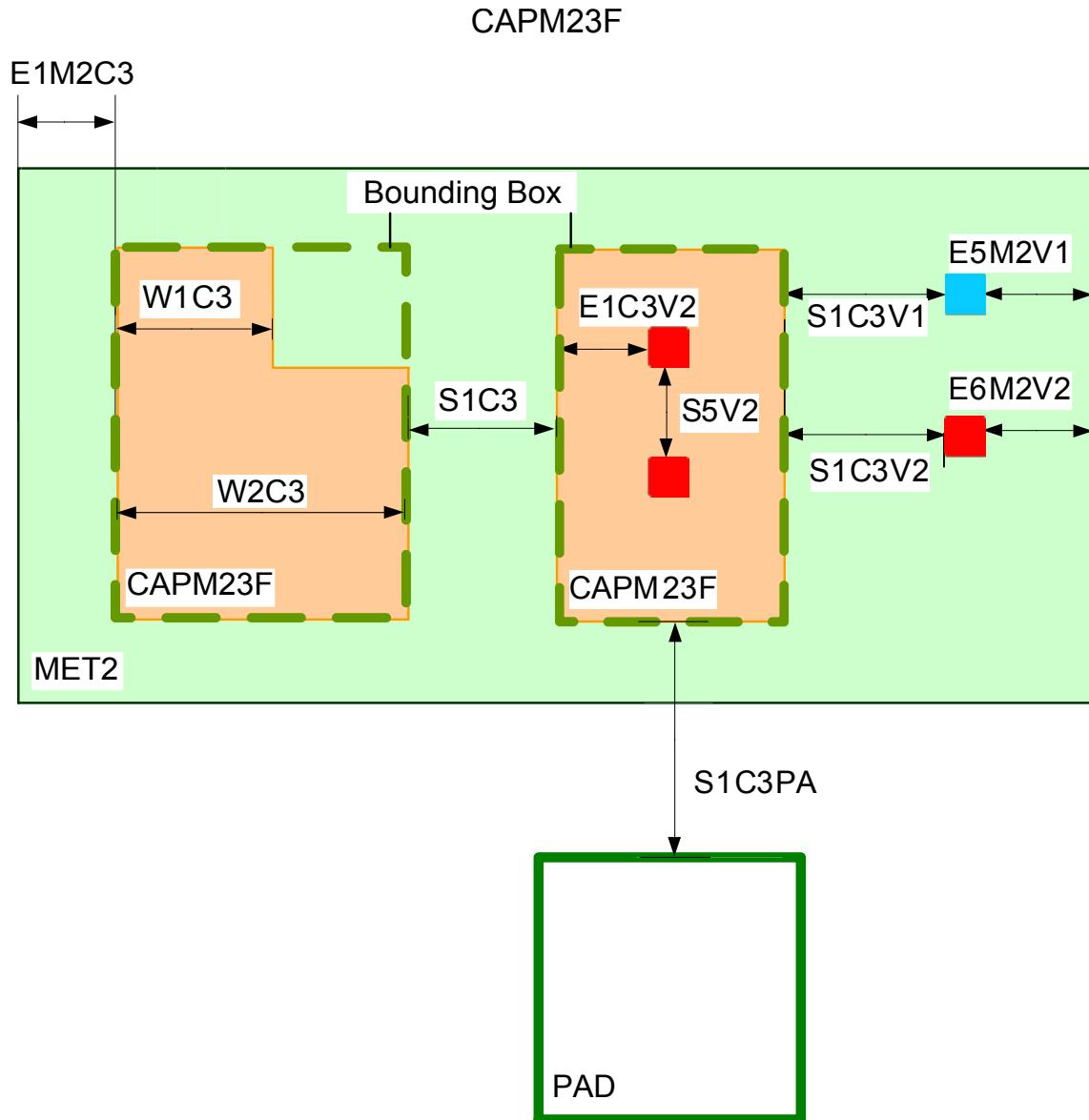
## 3.44 MIM23 module

### 3.44.1 Layer rules

#### CAPM23F

Name	Description	Value	Unit
B1C3	CAPM23F without MET2 is not allowed	-	-
B2C3	CAPM23F overlap of VIA1 or PAD is not allowed	-	-
B3C3	CAPM23F is not allowed when CAPM, CAPM34F, CAPM45F, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B4C3	CAPM23F without module MET3 is not allowed	-	-
W1C3	Minimum CAPM23F width	2.0	μm
W2C3	Maximum CAPM23F bounding box size	30.0 x 30.0	μm x μm
	<b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.		
S1C3	Minimum CAPM23F spacing/notch	1.5	μm
S5V2	Minimum VIA2 spacing on CAPM23F	2.0	μm
S1C3PA	Minimum CAPM23F spacing to PAD	10.0	μm
S1C3V1	Minimum CAPM23F spacing to VIA1	0.5	μm
S1C3V2	Minimum CAPM23F spacing to VIA2	0.5	μm
E1C3V2	Minimum CAPM23F enclosure of VIA2	0.3	μm
E1M2C3	Minimum MET2 enclosure of CAPM23F	0.5	μm
E5M2V1	Minimum MET2 enclosure of VIA1	0.15	μm
E6M2V2	Minimum MET2 enclosure of VIA2	0.15	μm
Q3V2	Recommended minimum ratio of VIA2 to CAPM23F area	1.0	%

3. Layer and Device rules → 3.44 MIM23 module → 3.44.1 Layer rules → CAPM23F

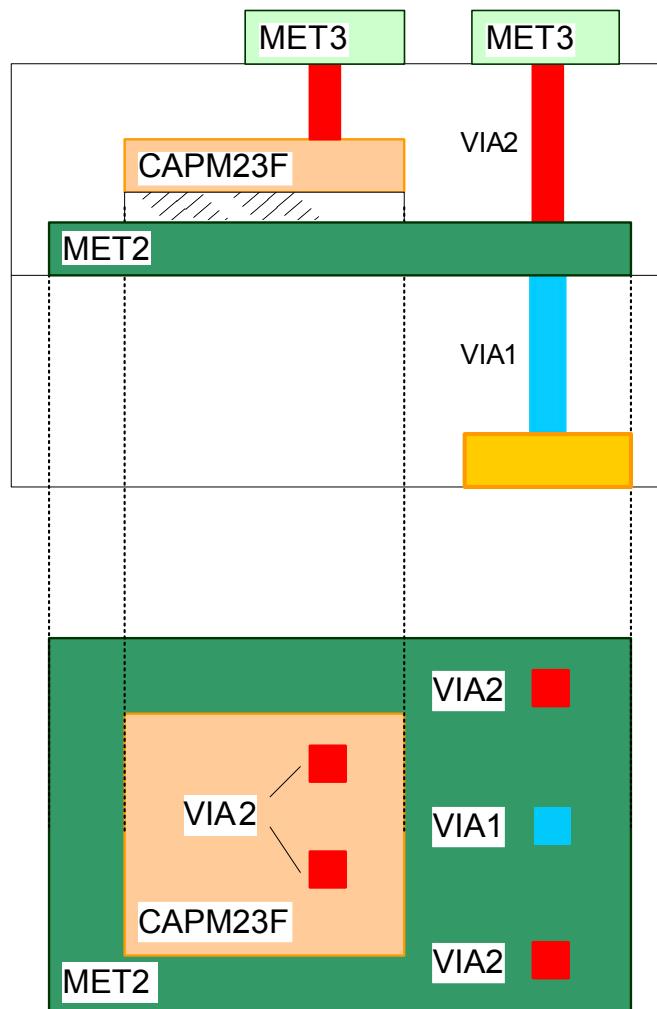


**Figure 3.326 CAPM23F**

3. Layer and Device rules → 3.44 MIM23 module → 3.44.2 Device rules → cmm3

### 3.44.2 Device rules

#### cmm3



**Figure 3.327** cmm3

3. Layer and Device rules → 3.45 MIM34 module

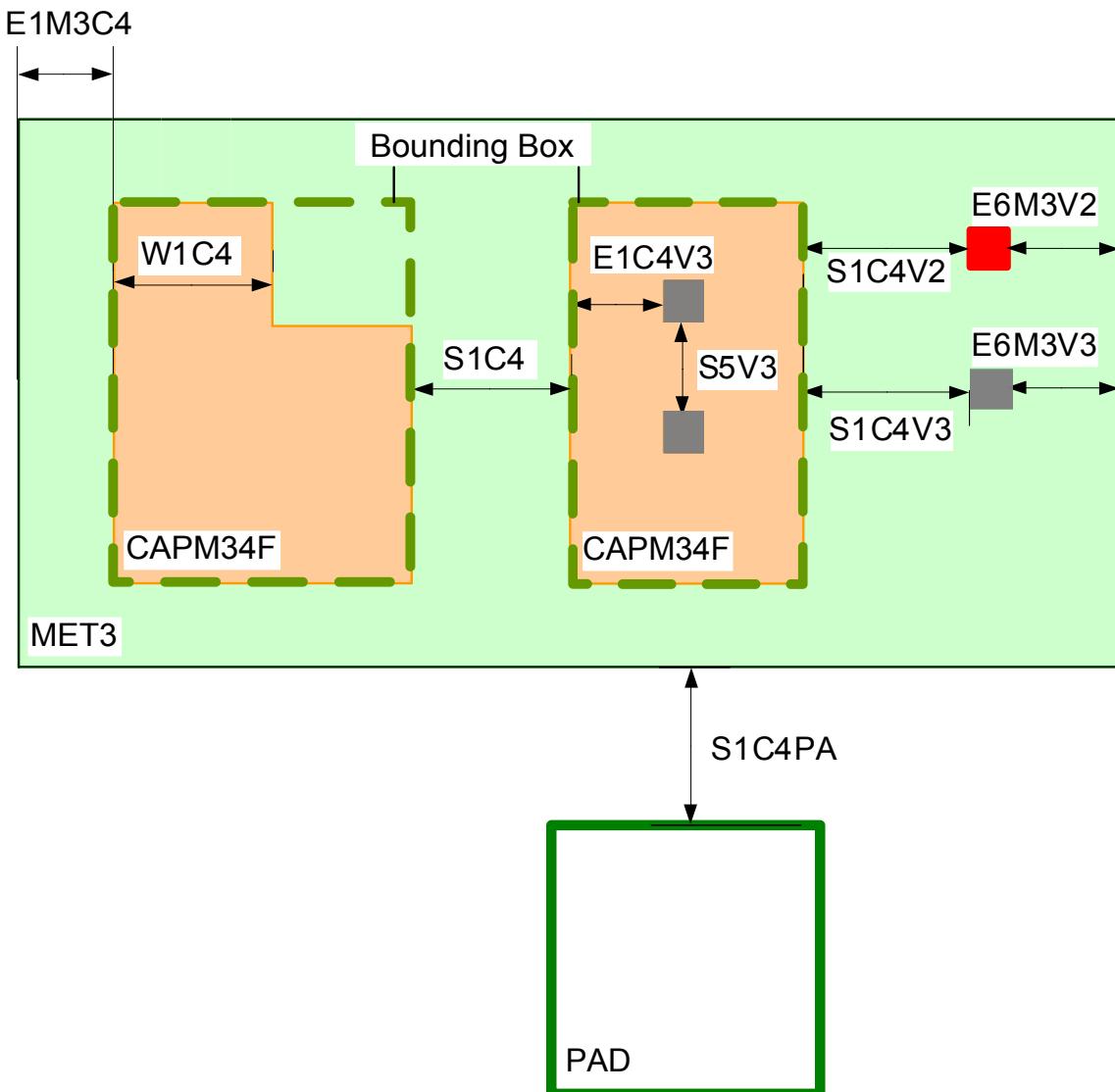
## 3.45 MIM34 module

### 3.45.1 Layer rules

#### CAPM34F

Name	Description	Value	Unit
B1C4	CAPM34F without MET3 is not allowed	-	-
B2C4	CAPM34F overlap of VIA2 or PAD is not allowed	-	-
B3C4	CAPM34F is not allowed when CAPM, CAPM23F, CAPM45F, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B4C4	CAPM34F without module MET4 is not allowed	-	-
W1C4	Minimum CAPM34F width	2.0	μm
W2C4	Maximum CAPM34F bounding box size	30.0 x 30.0	μm x μm
	<b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.		
S1C4	Minimum CAPM34F spacing/notch	1.5	μm
S5V3	Minimum VIA3 spacing on CAPM34F	2.0	μm
S1C4PA	Minimum CAPM34F spacing to PAD	10.0	μm
S1C4V2	Minimum CAPM34F spacing to VIA2	0.5	μm
S1C4V3	Minimum CAPM34F spacing to VIA3	0.5	μm
E1C4V3	Minimum CAPM34F enclosure of VIA3	0.3	μm
E1M3C4	Minimum MET3 enclosure of CAPM34F	0.5	μm
E6M3V2	Minimum MET3 enclosure of VIA2	0.15	μm
	<b>Note:</b> This rule is related to all VIAs inside CAPM34F regions extended by 2.5μm		
E6M3V3	Minimum MET3 enclosure of VIA3	0.15	μm
	<b>Note:</b> This rule is related to all VIAs inside CAPM34F regions extended by 2.5μm		
Q3V3	Recommended minimum ratio of VIA3 to CAPM34F area	1.0	%

3. Layer and Device rules → 3.45 MIM34 module → 3.45.1 Layer rules → CAPM34F

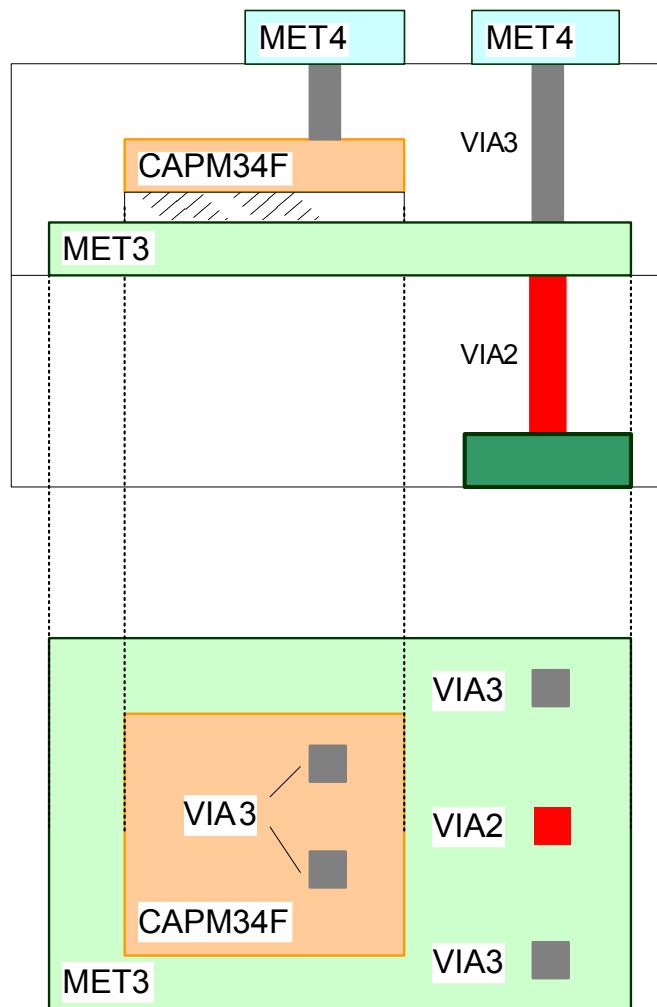


**Figure 3.328 CAPM34F**

3. Layer and Device rules → 3.45 MIM34 module → 3.45.2 Device rules → cmm4

### 3.45.2 Device rules

#### cmm4



**Figure 3.329** cmm4

3. Layer and Device rules → 3.46 MIM45 module

## 3.46 MIM45 module

### 3.46.1 Layer rules

#### CAPM45F

Name	Description	Value	Unit
B1C5	CAPM45F without MET4 is not allowed	-	-
B2C5	CAPM45F overlap of VIA3 or PAD is not allowed	-	-
B3C5	CAPM45F is not allowed when CAPM, CAPM23F, CAPM34F, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B4C5	CAPM45F without module MET5 is not allowed	-	-
W1C5	Minimum CAPM45F width	2.0	μm
W2C5	Maximum CAPM45F bounding box size	30.0 x 30.0	μm x μm
	<b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.		
S1C5	Minimum CAPM45F spacing/notch	1.5	μm
S6V4	Minimum VIA4 spacing on CAPM45F	2.0	μm
S1C5PA	Minimum CAPM45F spacing to PAD	10.0	μm
S1C5V3	Minimum CAPM45F spacing to VIA3	0.5	μm
S1C5V4	Minimum CAPM45F spacing to VIA4	0.5	μm
E1C5V4	Minimum CAPM45F enclosure of VIA4	0.3	μm
E1M4C5	Minimum MET4 enclosure of CAPM45F	0.5	μm
E6M4V3	Minimum MET4 enclosure of VIA3	0.15	μm
	<b>Note:</b> This rule is related to all VIAs inside CAPM45F regions extended by 2.5μm.		
E6M4V4	Minimum MET4 enclosure of VIA4	0.15	μm
	<b>Note:</b> This rule is related to all VIAs inside CAPM45F regions extended by 2.5μm.		
Q3V4	Recommended minimum ratio of VIA4 to CAPM45F area	1.0	%

3. Layer and Device rules → 3.46 MIM45 module → 3.46.1 Layer rules → CAPM45F

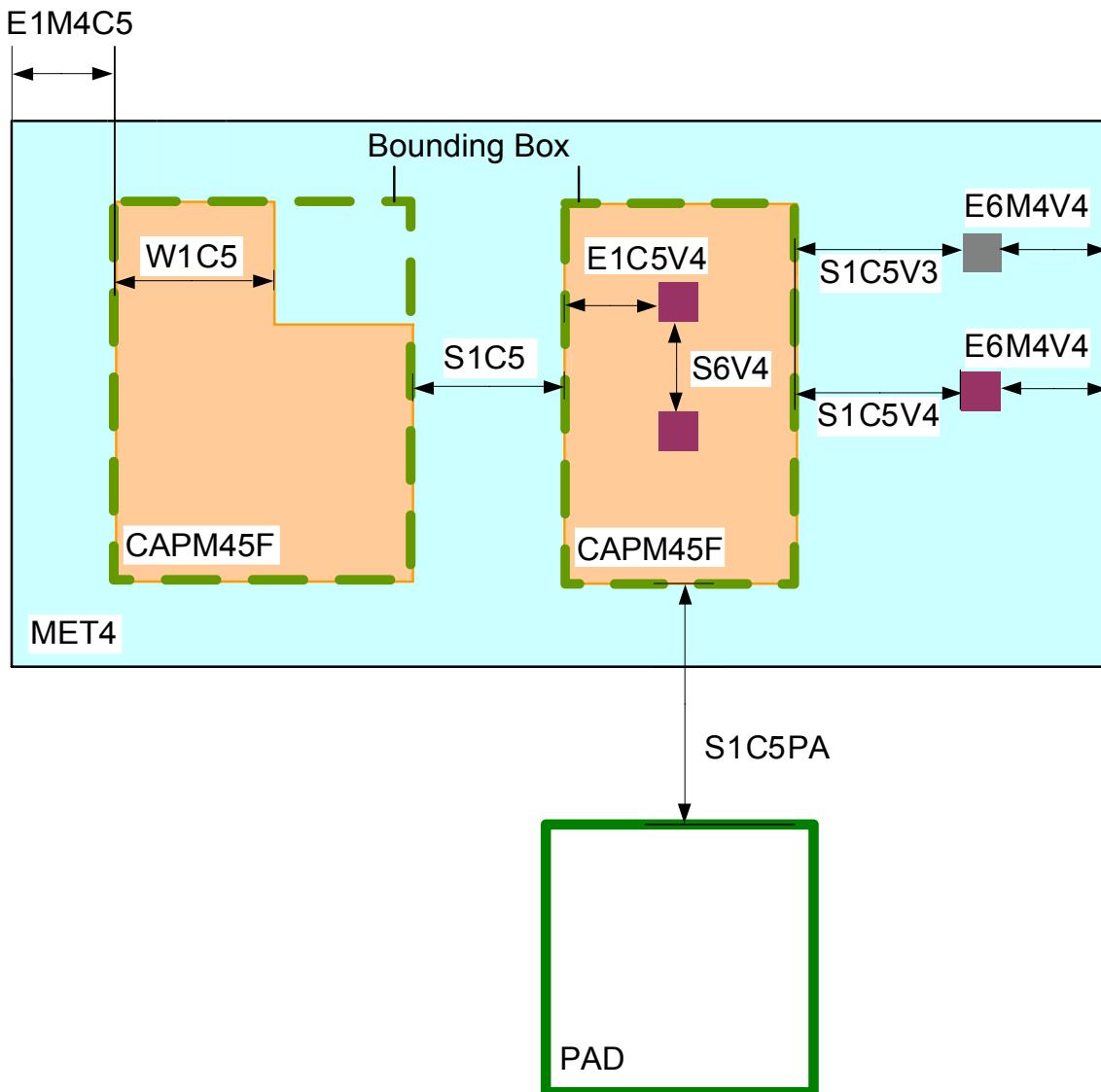
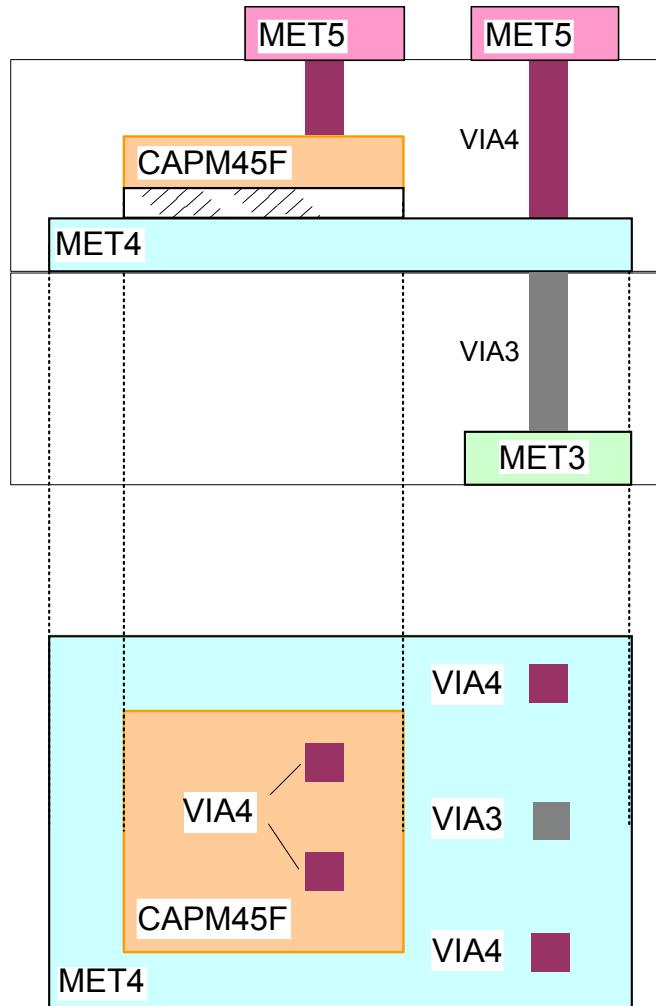


Figure 3.330 CAPM45F

3. Layer and Device rules → 3.46 MIM45 module → 3.46.2 Device rules → cmm5

### 3.46.2 Device rules

#### cmm5



**Figure 3.331** cmm5

3. Layer and Device rules → 3.47 DMIM module

## 3.47 DMIM module

### 3.47.1 Layer rules

#### CAPM2

Name	Description	Value	Unit
B10DM	CAPM2 without module MET4 or METMID is not allowed	-	-
B1DM	CAPM2 is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B2DM	CAPM2 must be enclosed by MET2 and MET3	-	-
B3DM	CAPM2 must not be over VIA1 or PAD	-	-
B4DM	CAPM2 without VIA2 is not allowed	-	-
B5DM	CAPM2 without VIATP is not allowed	-	-
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
B6DM	MET2 and METTP must be connected	-	-
	<b>Note:</b> CAPM2 must be enclosed by METTP.		
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
B7DM	CAPM2 without VIA3 is not allowed	-	-
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
B8DM	MET2 and MET4 must be connected	-	-
	<b>Note:</b> CAPM2 must be enclosed by MET4.		
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
B9DM	CAPM2 without module MET3 is not allowed	-	-
W1DM	Minimum CAPM2 width	2.0	µm
W2DM	Maximum CAPM2 bounding box size	30.0 x 30.0	µm x µm
	<b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.		
S1DM	Minimum CAPM2 spacing/notch	1.5	µm
S3V3	Minimum VIA3 spacing on CAPM2	2.0	µm
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
S5VT	Minimum VIATP spacing on CAPM2	2.0	µm
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
S1DMPA	Minimum CAPM2 spacing to PAD	10.0	µm
S1DMV1	Minimum CAPM2 spacing to VIA1	0.5	µm
S1DMV2	Minimum CAPM2 spacing to VIA2	0.5	µm
S1DMV3	Minimum CAPM2 spacing to VIA3	0.5	µm
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
S1DMVT	Minimum CAPM2 spacing to VIATP	0.5	µm
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
S3V2	Minimum VIA2 spacing on CAPM2	2.0	µm
E1DMV2	Minimum CAPM2 enclosure of VIA2	0.3	µm
E1DMV3	Minimum CAPM2 enclosure of VIA3	0.3	µm
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
E1DMVT	Minimum CAPM2 enclosure of VIATP	0.3	µm
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
E1M2DM	Minimum MET2 enclosure of CAPM2	0.5	µm

⇒

## 3. Layer and Device rules → 3.47 DMIM module→ 3.47.1 Layer rules→ CAPM2

Name	Description	Value	Unit
E1M3DM	Minimum MET3 enclosure of CAPM2	0.5	µm
E3M2V1	Minimum MET2 enclosure of VIA1  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M2V2	Minimum MET2 enclosure of VIA2  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3V2	Minimum MET3 enclosure of VIA2  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3V3	Minimum MET3 enclosure of VIA3  <b>Note:</b> Valid if MET4 or MET5 module is selected  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3VT	Minimum MET3 enclosure of VIATP  <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
Q1V2	Recommended minimum ratio of VIA2 to CAPM2 area	1.0	%
Q1V3	Recommended minimum ratio of VIA3 to CAPM2 area  <b>Note:</b> Valid if MET4 or MET5 module is selected	1.0	%
Q2VT	Recommended minimum ratio of VIATP to CAPM2 area  <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.	1.0	%

**Note:** The placement of DMIM must start from MET2 as described in the Table for DMIM Construction below.

Table for DMIM Construction

module combination	structure of metal stacking	device	Top MIM metal
LP5MOS/MOS5	MET2 / CAPM2 / MET3 / CAPM2 / METTP	cdmm4t	METTP
MET4, MET5	MET2 / CAPM2 / MET3 / CAPM2 / MET4	cdmm4	MET4

## 3. Layer and Device rules → 3.47 DMIM module → 3.47.1 Layer rules → CAPM2

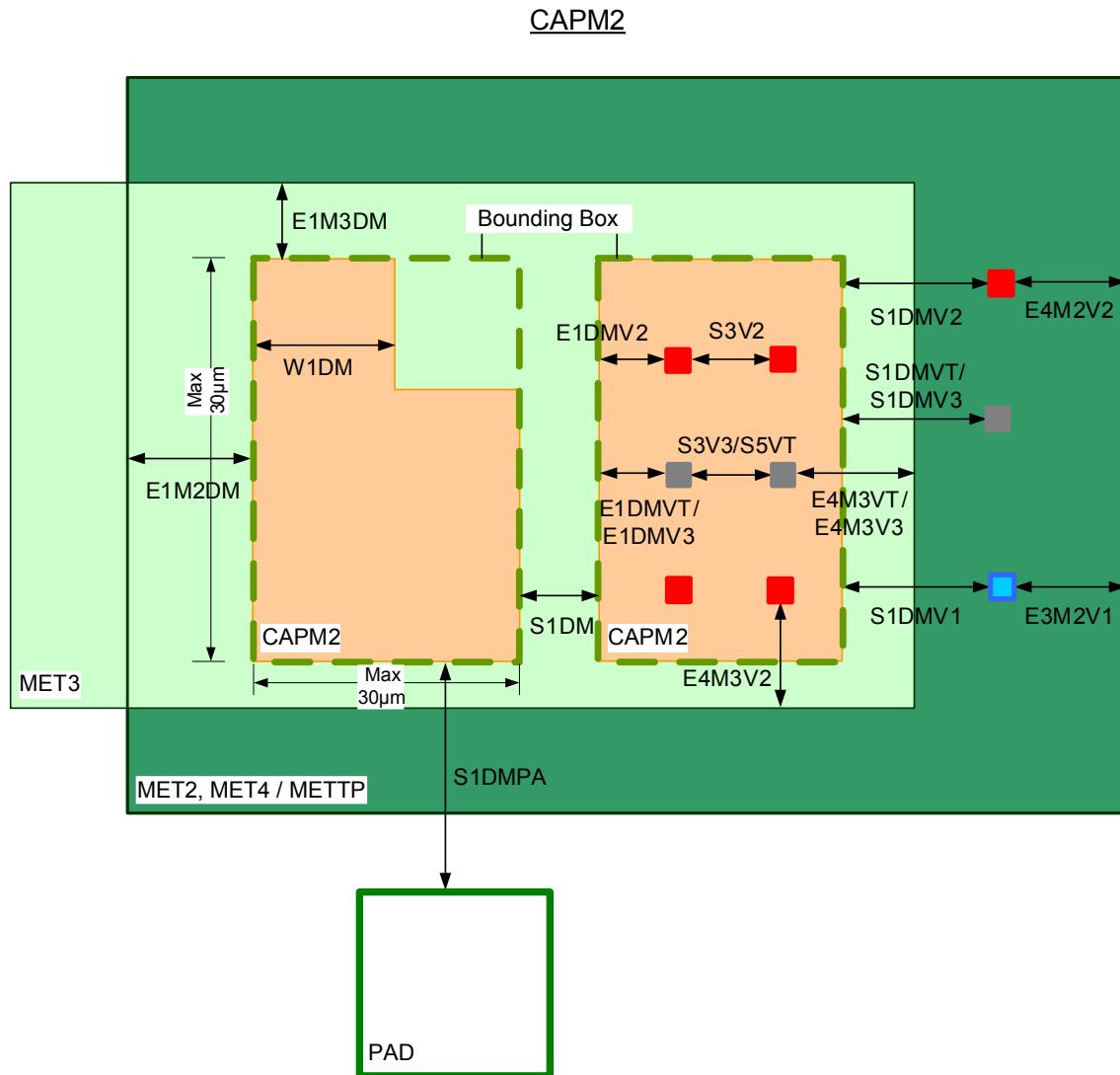
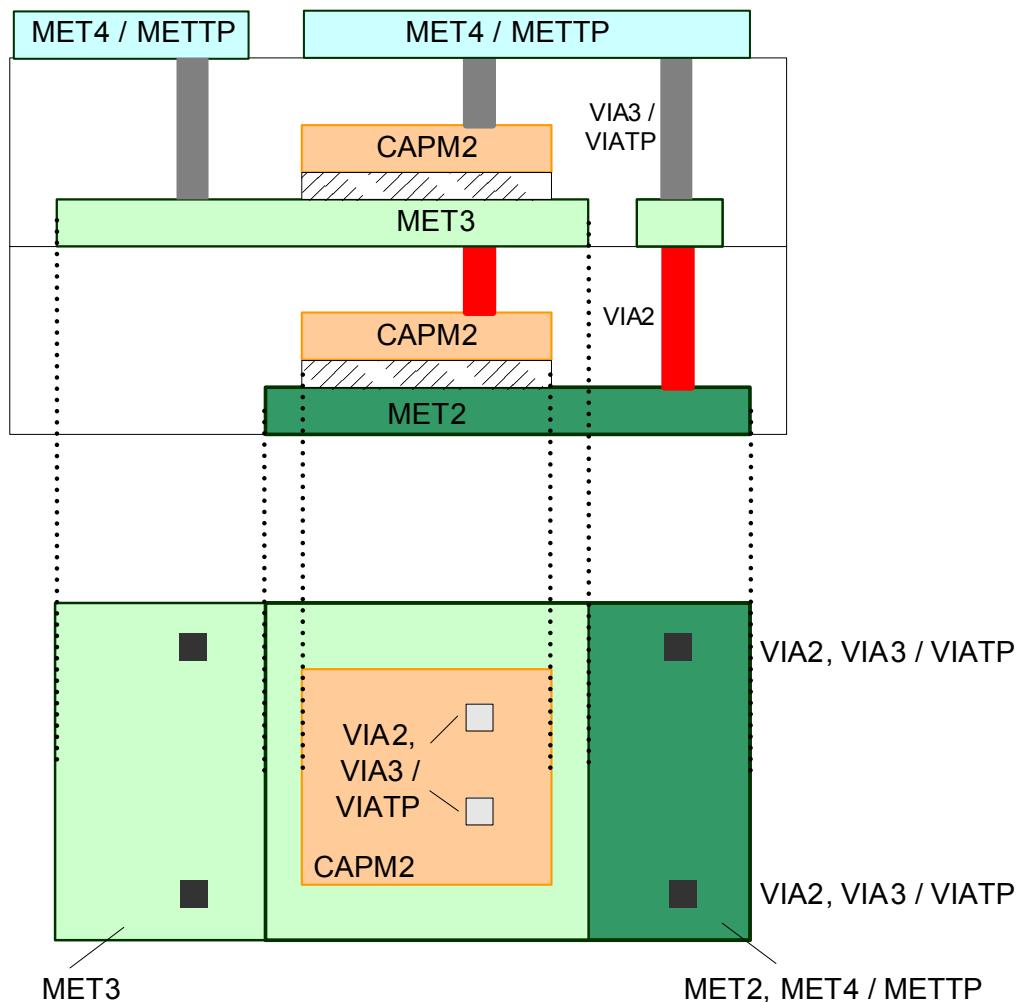


Figure 3.332 CAPM2

3. Layer and Device rules → 3.47 DMIM module→ 3.47.2 Device rules→ cdmm4, cdmm4t

### 3.47.2 Device rules

cdmm4, cdmm4t



**Figure 3.333** cdmm4t, cdmm4

3. Layer and Device rules → 3.48 DMIM3 module

## 3.48 DMIM3 module

### 3.48.1 Layer rules

#### CAPM2A

Name	Description	Value	Unit
B10D3	CAPM2A without module MET5 or METMID is not allowed	-	-
B1D3	CAPM2A is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPM2, CAPM3, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPMH2, CAPMH2A or CAPMH3 is present	-	-
B2D3	CAPM2A must be enclosed by MET3 and MET4	-	-
B3D3	CAPM2A must not be over VIA2 or PAD	-	-
B4D3	CAPM2A without VIA3 is not allowed	-	-
B5D3	CAPM2A without VIATP is not allowed  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	-	-
	MET3 and METTP must be connected	-	-
B6D3	<b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.  <b>Note:</b> CAPM2A must be enclosed by METTP		
B7D3	CAPM2A without VIA4 is not allowed  <b>Note:</b> Valid if MET5 module is selected.	-	-
B8D3	MET3 and MET5 must be connected  <b>Note:</b> Valid if MET5 module is selected.  <b>Note:</b> CAPM2A must be enclosed by MET5	-	-
B9D3	CAPM2A without module MET4 is not allowed	-	-
W1D3	Minimum CAPM2A width	2.0	µm
W2D3	Maximum CAPM2A bounding box size  <b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	µm x µm
S1D3	Minimum CAPM2A spacing/notch	1.5	µm
S5V4	Minimum VIA4 spacing on CAPM2A  <b>Note:</b> Valid if MET5 module is selected.	2.0	µm
S1D3PA	Minimum CAPM2A spacing to PAD	10.0	µm
S1D3V2	Minimum CAPM2A spacing to VIA2	0.5	µm
S1D3V3	Minimum CAPM2A spacing to VIA3	0.5	µm
S1D3V4	Minimum CAPM2A spacing to VIA4  <b>Note:</b> Valid if MET5 module is selected.	0.5	µm
S1D3VT	Minimum CAPM2A spacing to VIATP  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.5	µm
S2VT	Minimum VIATP spacing on CAPM2A  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	2.0	µm
S9V3	Minimum VIA3 spacing on CAPM2A	2.0	µm
E1D3V3	Minimum CAPM2A enclosure of VIA3	0.3	µm
E1D3V4	Minimum CAPM2A enclosure of VIA4  <b>Note:</b> Valid if MET5 module is selected.	0.3	µm
E1D3VT	Minimum CAPM2A enclosure of VIATP  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.3	µm
E1M3D3	Minimum MET3 enclosure of CAPM2A	0.5	µm

⇒

## 3. Layer and Device rules → 3.48 DMIM3 module→ 3.48.1 Layer rules→ CAPM2A

Name	Description	Value	Unit
E1M4D3	Minimum MET4 enclosure of CAPM2A	0.5	μm
E3M3V2	Minimum MET3 enclosure of VIA2  <b>Note:</b> This rule is related to all VIAs inside CAPM2A region extended by 2.5μm.	0.15	μm
E4M4V3	Minimum MET4 enclosure of VIA3  <b>Note:</b> This rule is related to all VIAs inside CAPM2A region extended by 2.5μm.	0.15	μm
E5M4V4	Minimum MET4 enclosure of VIA4  <b>Note:</b> Valid if MET5 module is selected.  <b>Note:</b> This rule is related to all VIAs inside CAPM2A region extended by 2.5μm.	0.15	μm
E5M4VT	Minimum MET4 enclosure of VIATP  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.  <b>Note:</b> This rule is related to all VIAs inside CAPM2A region extended by 2.5μm.	0.15	μm
E8M3V3	Minimum MET3 enclosure of VIA3  <b>Note:</b> This rule is related to all VIAs inside CAPM2A region extended by 2.5μm.	0.15	μm
Q5V4	Recommended minimum ratio of VIA4 to CAPM2A area  <b>Note:</b> Valid if MET5 module is selected.	1.0	%
Q7V3	Recommended minimum ratio of VIA3 to CAPM2A area	1.0	%
Q7VT	Recommended minimum ratio of VIATP to CAPM2A area  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	1.0	%

**Note:** The placement of DMIM3 must start from MET3 as described in the Table for DMIM3 Construction below.

Table for DMIM3 Construction

module combination	structure of metal stacking	device	Top MIM metal
LP5MOS/MOS5	MET3 / CAPM2A / MET4 / CAPM2A / METTP	cdmm5t	METTP
MET5	MET3 / CAPM2A / MET4 / CAPM2A / MET5	cdmm5	MET5

## 3. Layer and Device rules → 3.48 DMIM3 module → 3.48.1 Layer rules → CAPM2A

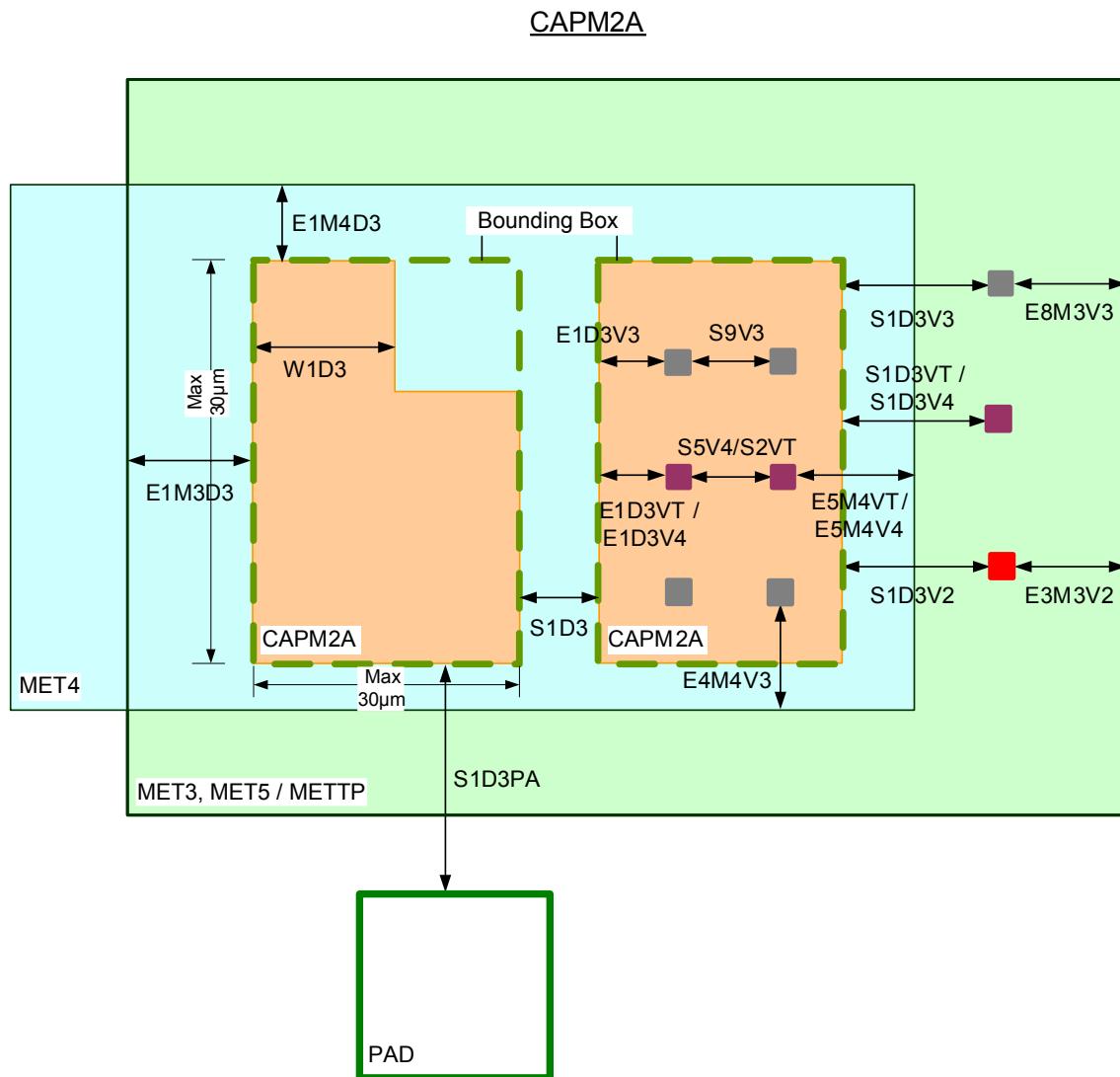
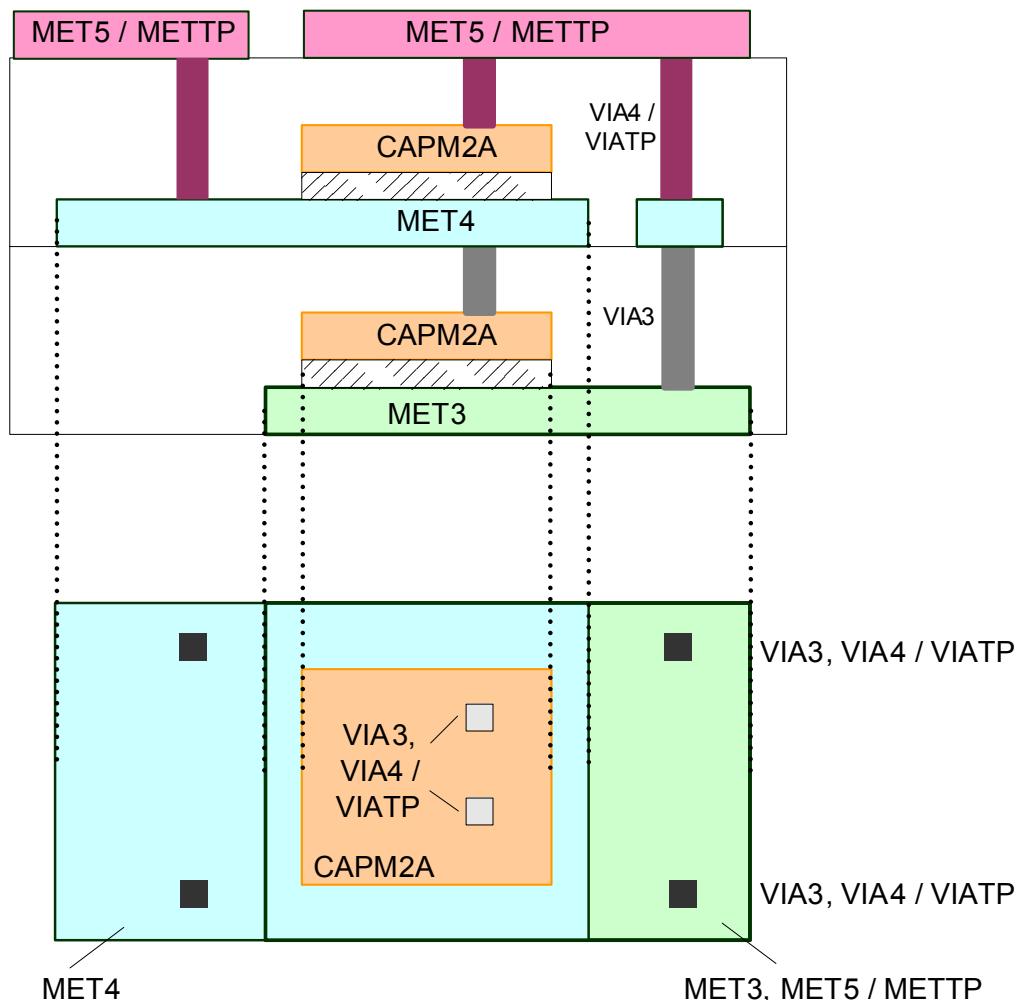


Figure 3.334 CAPM2A

3. Layer and Device rules → 3.48 DMIM3 module → 3.48.2 Device rules → cdmm5, cdmm5t

### 3.48.2 Device rules

#### cdmm5, cdmm5t



**Figure 3.335** cdmm5t, cdmm5

3. Layer and Device rules → 3.49 TMIM module

## 3.49 TMIM module

### 3.49.1 Layer rules

#### CAPM3

Name	Description	Value	Unit
B10TM	CAPM3 without module MET4 is not allowed	-	-
B11TM	CAPM3 without module MET5 or METMID is not allowed	-	-
B1TM	CAPM3 is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2A, CAPMH2, CAPM2, CAPMH2A or CAPMH3 is present	-	-
B2TM	CAPM3 must be enclosed by MET2, MET3 and MET4	-	-
B3TM	CAPM3 must not be over VIA1 or PAD	-	-
B4TM	CAPM3 without VIA2 or VIA3 is not allowed	-	-
B5TM	MET2 and MET4 must be connected	-	-
B6TM	CAPM3 without VIATP is not allowed <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	-	-
B7TM	MET3 and METTP must be connected <b>Note:</b> CAPM3 must be enclosed by METTP. <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	-	-
B8TM	CAPM3 without VIA4 is not allowed <b>Note:</b> Valid if MET5 module is selected.	-	-
B9TM	MET3 and MET5 must be connected <b>Note:</b> Valid if MET5 module is selected. <b>Note:</b> CAPM3 must be enclosed by MET5	-	-
W1TM	Minimum CAPM3 width	2.0	µm
W2TM	Maximum CAPM3 bounding box size <b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	µm x µm
S1TM	Minimum CAPM3 spacing/notch	1.5	µm
S3V4	Minimum VIA4 spacing on CAPM3 <b>Note:</b> Valid if MET5 module is selected.	2.0	µm
S4V2	Minimum VIA2 spacing on CAPM3	2.0	µm
S4V3	Minimum VIA3 spacing on CAPM3	2.0	µm
S6VT	Minimum VIATP spacing on CAPM3 <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	2.0	µm
S1TMPA	Minimum CAPM3 spacing to PAD	10.0	µm
S1TMV1	Minimum CAPM3 spacing to VIA1	0.5	µm
S1TMV2	Minimum CAPM3 spacing to VIA2	0.5	µm
S1TMV3	Minimum CAPM3 spacing to VIA3	0.5	µm
S1TMV4	Minimum CAPM3 spacing to VIA4 <b>Note:</b> Valid if MET5 module is selected.	0.5	µm
S1TMVT	Minimum CAPM3 spacing to VIATP <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.5	µm
E1M2TM	Minimum MET2 enclosure of CAPM3	0.5	µm
E1M3TM	Minimum MET3 enclosure of CAPM3	0.5	µm
E1M4TM	Minimum MET4 enclosure of CAPM3	0.5	µm

⇒

## 3. Layer and Device rules → 3.49 TMIM module→ 3.49.1 Layer rules→ CAPM3

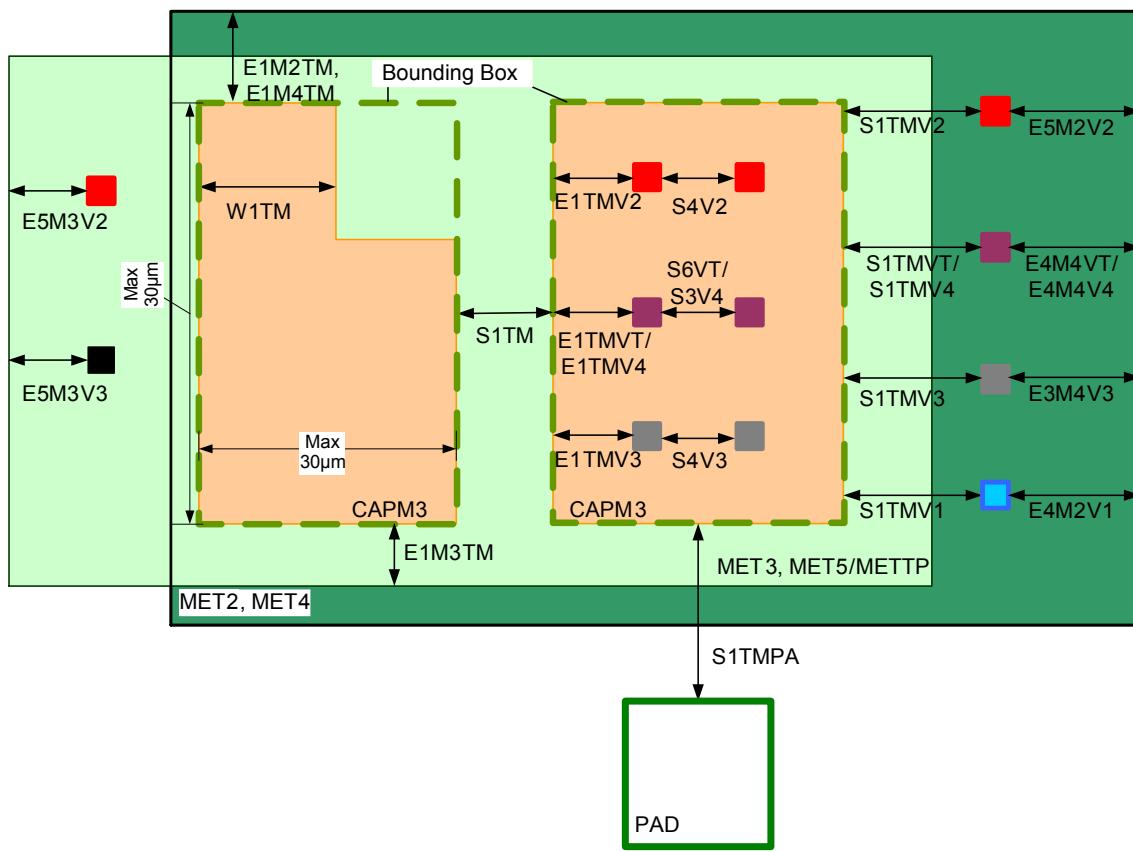
Name	Description	Value	Unit
E1TMV2	Minimum CAPM3 enclosure of VIA2	0.3	µm
E1TMV3	Minimum CAPM3 enclosure of VIA3	0.3	µm
E1TMV4	Minimum CAPM3 enclosure of VIA4 <b>Note:</b> Valid if MET5 module is selected.	0.3	µm
E1TMVT	Minimum CAPM3 enclosure of VIATP <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.3	µm
E3M4V3	Minimum MET4 enclosure of VIA3 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M2V1	Minimum MET2 enclosure of VIA1 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M4V4	Minimum MET4 enclosure of VIA4 <b>Note:</b> Valid if MET5 module is selected. <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M4VT	Minimum MET4 enclosure of VIATP <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm. <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.15	µm
E5M2V2	Minimum MET2 enclosure of VIA2 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E5M3V2	Minimum MET3 enclosure of VIA2 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E5M3V3	Minimum MET3 enclosure of VIA3 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
Q1V4	Recommended minimum ratio of VIA4 to CAPM3 area <b>Note:</b> Valid if MET5 module is selected.	1.0	%
Q2V2	Recommended minimum ratio of VIA2 to CAPM3 area	1.0	%
Q3VT	Recommended minimum ratio of VIATP to CAPM3 area <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	1.0	%

**Note:** The placement of TMIM must start from MET2 as described in the Table for TMIM Construction.

Table for TMIM Construction

module combination	structure of metal stacking	device	Top MIM metal
LP5MOS/MOS5	n/a	n/a	n/a
MET4	MET2 / CAPM3 / MET3 / CAPM3 / MET4 / CAPM3 / METTP	ctmm5t	METTP
MET5	METTP MET2 / CAPM3 / MET3 / CAPM3 / MET4 / CAPM3 / MET5	ctmm5	MET5

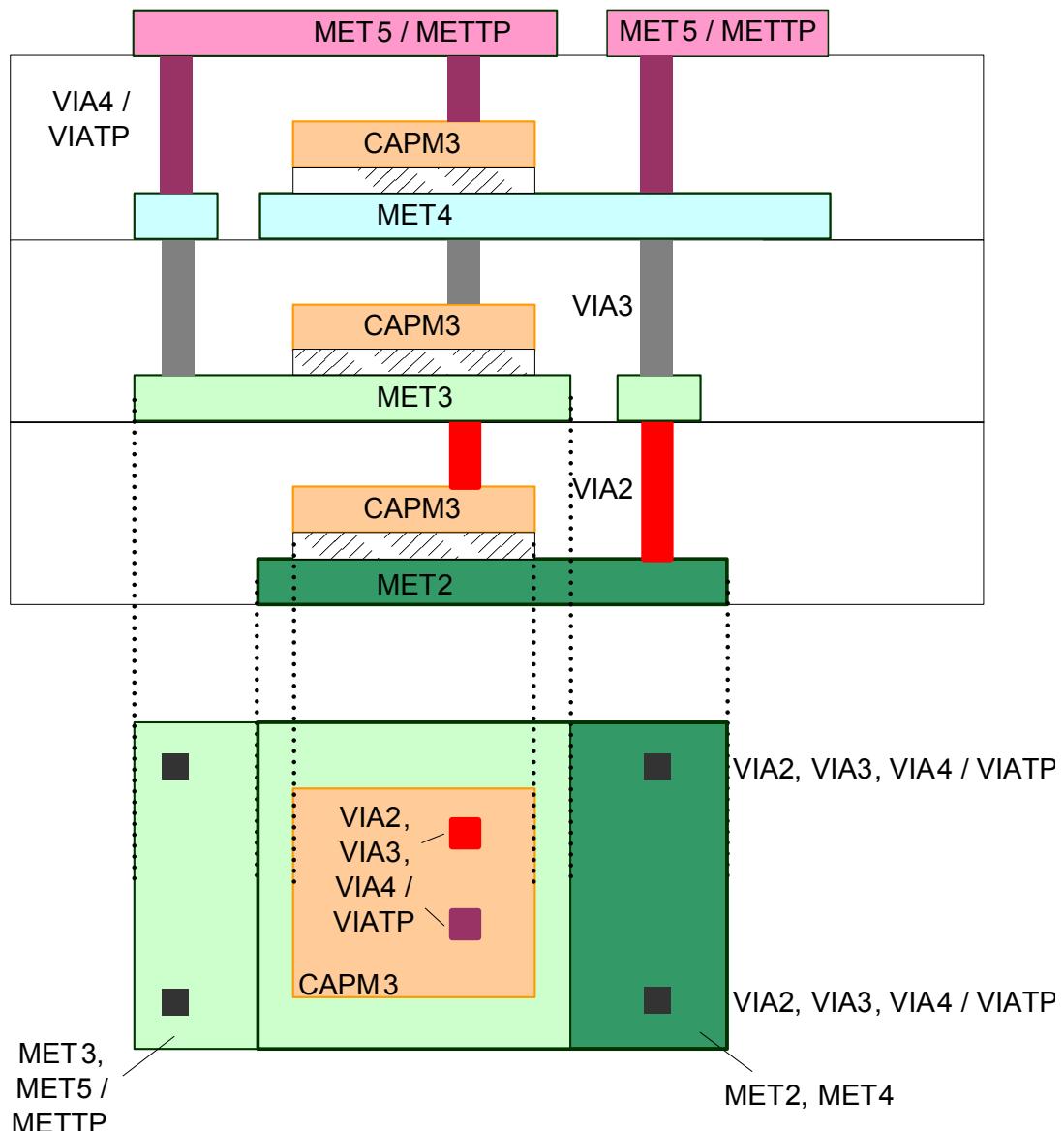
## 3. Layer and Device rules → 3.49 TMIM module→ 3.49.1 Layer rules→ CAPM3

CAPM3**Figure 3.336 CAPM3**

3. Layer and Device rules → 3.49 TMIM module→ 3.49.2 Device rules→ ctmm5, ctmm5t

### 3.49.2 Device rules

**ctmm5, ctmm5t**



**Figure 3.337** ctmm5t, ctmm5

3. Layer and Device rules → 3.50 MIMH module

## 3.50 MIMH module

### 3.50.1 Layer rules

#### CAPMH

Name	Description	Value	Unit
B1CH	CAPMH without BM is not allowed	-	-
B2CH	CAPMH overlap of VIAn or PAD is not allowed	-	-
B3CH	CAPMH is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
W1CH	Minimum CAPMH width	2.0	µm
W2CH	Maximum CAPMH bounding box size  <b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	µm x µm
S1CH	Minimum CAPMH spacing/notch	1.5	µm
S2VL	Minimum VIATPL spacing on CAPMH  <b>Note:</b> Valid if module METTHK is selected and not METMID	2.0	µm
S4VT	Minimum VIATP spacing on CAPMH  <b>Note:</b> Valid if module METMID is selected	2.0	µm
S1CHPA	Minimum CAPMH spacing to PAD	10.0	µm
S1CHVL	Minimum CAPMH spacing to VIATPL  <b>Note:</b> Valid if module METTHK is selected and not METMID	0.5	µm
S1CHVN	Minimum CAPMH spacing to VIAn	0.5	µm
S1CHVT	Minimum CAPMH spacing to VIATP  <b>Note:</b> Valid if module METMID is selected	0.5	µm
E1BMCH	Minimum BM enclosure of CAPMH	0.5	µm
E1BMVL	Minimum BM enclosure of VIATPL  <b>Note:</b> This rule is related to all VIAs inside CAPMH regions extended by 2.5µm.  <b>Note:</b> Valid if module METTHK is selected and not METMID	0.5	µm
E1CHVL	Minimum CAPMH enclosure of VIATPL  <b>Note:</b> Valid if module METTHK is selected and not METMID	0.5	µm
E1CHVT	Minimum CAPMH enclosure of VIATP  <b>Note:</b> Valid if module METMID is selected	0.3	µm
E2BMVN	Minimum BM enclosure of VIAn  <b>Note:</b> This rule is related to all VIAs inside CAPMH regions extended by 2.5µm.	0.15	µm
E2BMVT	Minimum BM enclosure of VIATP  <b>Note:</b> This rule is related to all VIAs inside CAPMH regions extended by 2.5µm.  <b>Note:</b> Valid if module METMID is selected	0.15	µm
Q1VL	Recommended minimum ratio of VIATPL to CAPMH area  <b>Note:</b> Valid if module METTHK is selected and not METMID	1.0	%
Q4VT	Recommended minimum ratio of VIATP to CAPMH area  <b>Note:</b> Valid if module METMID is selected	1.0	%

**Note:** The Single High Capacitance MIM Capacitor is located between the top metal and the metal layer underneath top metal. The table below shows the assignment of the MIMH bottom layer BM and the via layer VIAn to the physical metal and via layers for the different metal module options.

Table for BM and VIAn assignment



## 3. Layer and Device rules → 3.50 MIMH module → 3.50.1 Layer rules → CAPMH

module combination	bottom MIM metal (BM)	device	VIA <i>n</i>
LP5MOS/MOS5 and not MET3	MET2	cmmh3t	VIA1
MET3 and not MET4	MET3	cmmh4t	VIA2
MET3 and METTHK	MET3	cmmh4l	VIA2
MET4 and not MET5	MET4	cmmh5t	VIA3
MET4 and METTHK	MET4	cmmh5l	VIA3
MET5 and METMID	MET5	cmmh6t	VIA4
MET5 and METTHK	MET5	cmmh6l	VIA4

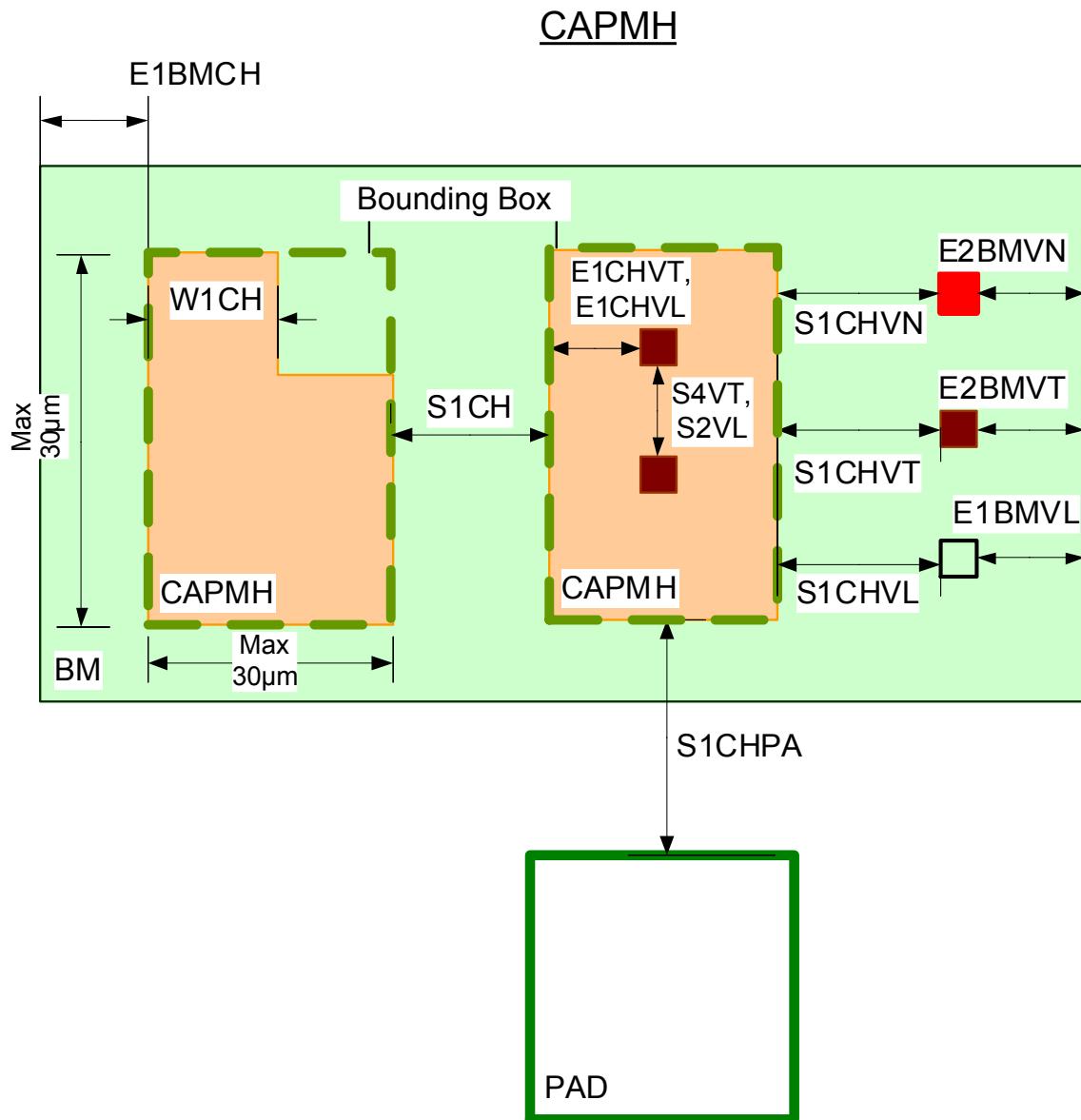
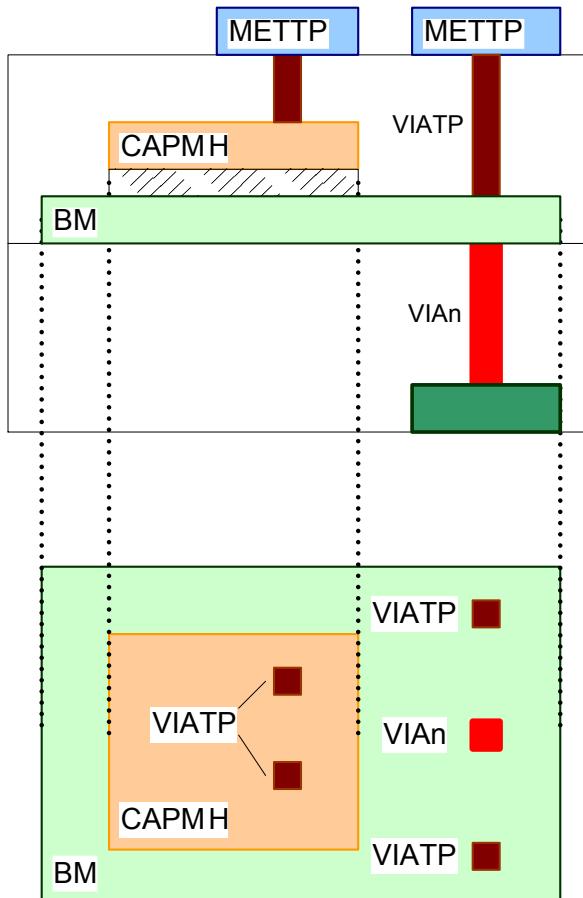


Figure 3.338 CAPMH

3. Layer and Device rules → 3.50 MIMH module → 3.50.2 Device rules → cmmh3t, cmmh4t, cmmh...

### 3.50.2 Device rules

cmmh3t, cmmh4t, cmmh5t, cmmh6t

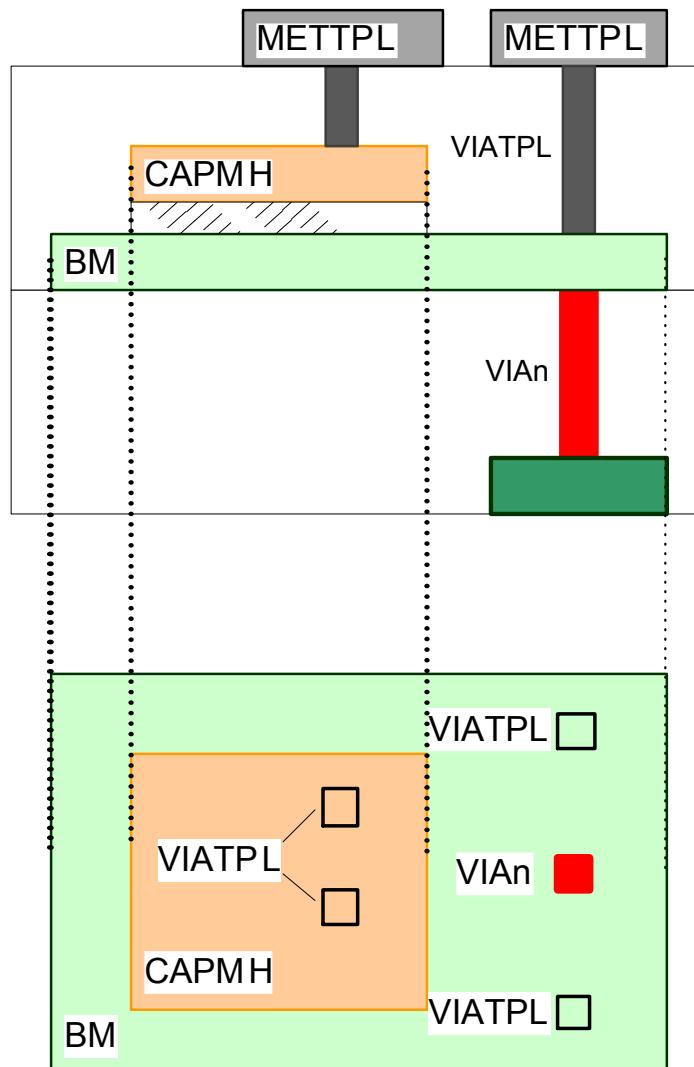


**Figure 3.339** cmmh3t, cmmh4t, cmmh5t, cmmh6t

3. Layer and Device rules → 3.50 MIMH module → 3.50.2 Device rules → cmmh4l, cmmh5l, cmmh...

### cmmh4l, cmmh5l, cmmh6l

#### cmmh4l, cmmh5l, cmmh6l



**Figure 3.340** cmmh4l, cmmh5l, cmmh6l

3. Layer and Device rules → 3.51 MIMH23 module

## 3.51 MIMH23 module

### 3.51.1 Layer rules

#### CAPMH23F

Name	Description	Value	Unit
B1H3	CAPMH23F without MET2 is not allowed	-	-
B2H3	CAPMH23F overlap of VIA1 or PAD is not allowed	-	-
B3H3	CAPMH23F is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPMH, CAPMH34F, CAPMH45F, CAPM2, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B4H3	CAPMH23F without module MET3 is not allowed	-	-
W1H3	Minimum CAPMH23F width	2.0	μm
W2H3	Maximum CAPMH23F bounding box size	30.0 x 30.0	μm x μm
	<b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.		
S1H3	Minimum CAPMH23F spacing/notch	1.5	μm
S6V2	Minimum VIA2 spacing on CAPMH23F	2.0	μm
S1H3PA	Minimum CAPMH23F spacing to PAD	10.0	μm
S1H3V1	Minimum CAPMH23F spacing to VIA1	0.5	μm
S1H3V2	Minimum CAPMH23F spacing to VIA2	0.5	μm
E1H3V2	Minimum CAPMH23F enclosure of VIA2	0.3	μm
E1M2H3	Minimum MET2 enclosure of CAPMH23F	0.5	μm
E6M2V1	Minimum MET2 enclosure of VIA1	0.15	μm
E7M2V2	Minimum MET2 enclosure of VIA2	0.15	μm
Q4V2	Recommended minimum ratio of VIA2 to CAPMH23F area	1.0	%

3. Layer and Device rules → 3.51 MIMH23 module → 3.51.1 Layer rules → CAPMH23F

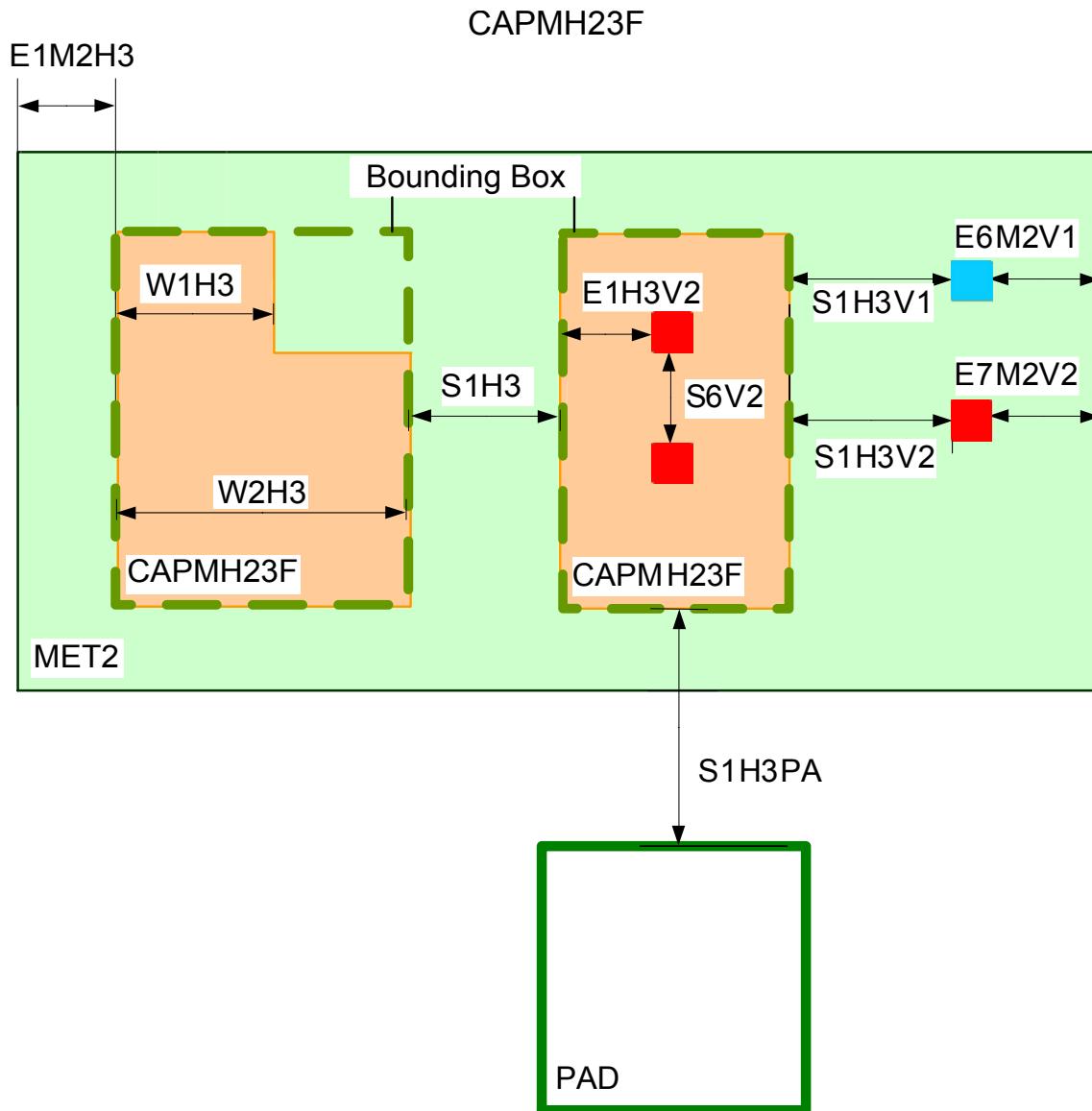


Figure 3.341 CAPMH23F

3. Layer and Device rules → 3.51 MIMH23 module → 3.51.2 Device rules → cmmh3

### 3.51.2 Device rules

#### cmmh3

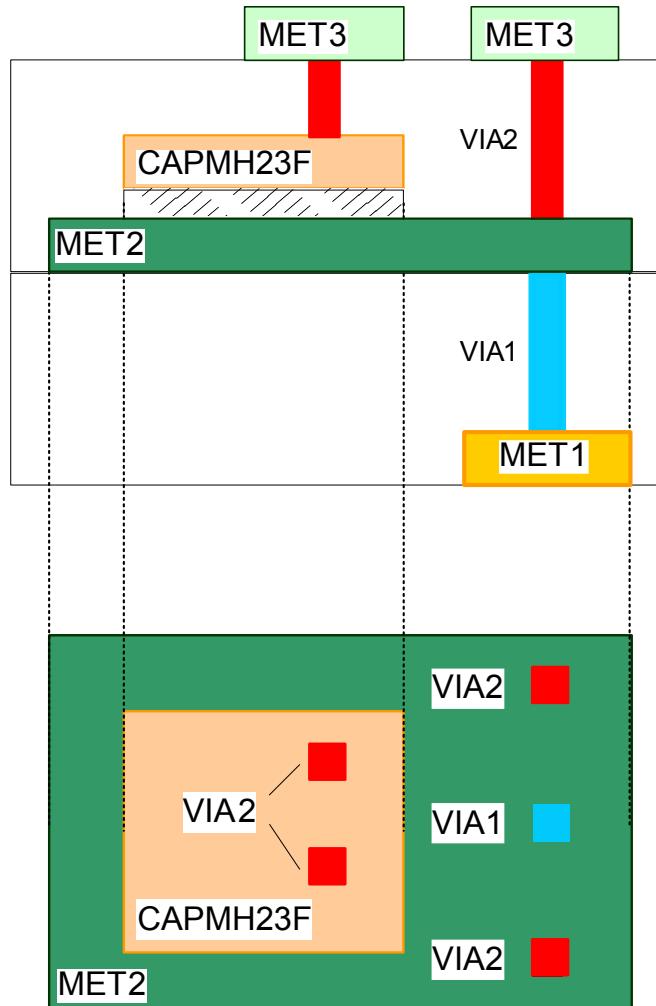


Figure 3.342 cmmh3

3. Layer and Device rules → 3.52 MIMH34 module

## 3.52 MIMH34 module

### 3.52.1 Layer rules

#### CAPMH34F

Name	Description	Value	Unit
B1H4	CAPMH34F without MET3 is not allowed	-	-
B2H4	CAPMH34F overlap of VIA2 or PAD is not allowed	-	-
B3H4	CAPMH34F is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPMH, CAPMH23F, CAPMH45F, CAPM2, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B4H4	CAPMH34F without module MET4 is not allowed	-	-
W1H4	Minimum CAPMH34F width	2.0	μm
W2H4	Maximum CAPMH34F bounding box size	30.0 x 30.0	μm x μm
	<b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.		
S1H4	Minimum CAPMH34F spacing/notch	1.5	μm
S6V3	Minimum VIA3 spacing on CAPMH34F	2.0	μm
S1H4PA	Minimum CAPMH34F spacing to PAD	10.0	μm
S1H4V2	Minimum CAPMH34F spacing to VIA2	0.5	μm
S1H4V3	Minimum CAPMH34F spacing to VIA3	0.5	μm
E1H4V3	Minimum CAPMH34F enclosure of VIA3	0.3	μm
E1M3H4	Minimum MET3 enclosure of CAPMH34F	0.5	μm
E7M3V2	Minimum MET3 enclosure of VIA2	0.15	μm
	<b>Note:</b> This rule is related to all VIAs inside CAPMH34F regions extended by 2.5μm.		
E7M3V3	Minimum MET3 enclosure of VIA3	0.15	μm
	<b>Note:</b> This rule is related to all VIAs inside CAPMH34F regions extended by 2.5μm.		
Q4V3	Recommended minimum ratio of VIA3 to CAPMH34F area	1.0	%

3. Layer and Device rules → 3.52 MIMH34 module → 3.52.1 Layer rules → CAPMH34F

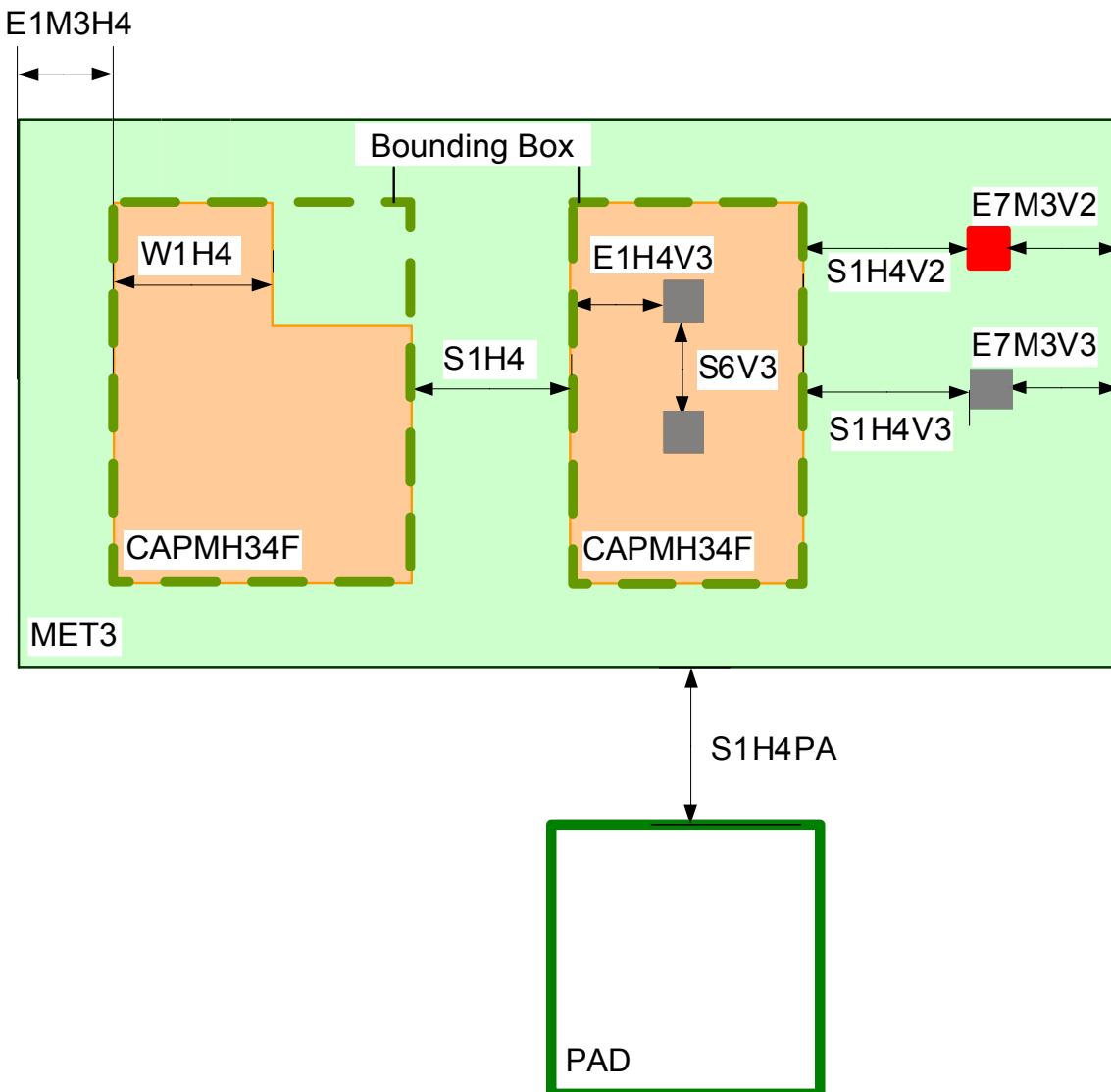


Figure 3.343 CAPMH34F

3. Layer and Device rules → 3.52 MIMH34 module → 3.52.2 Device rules → cmmh4

### 3.52.2 Device rules

#### cmmh4

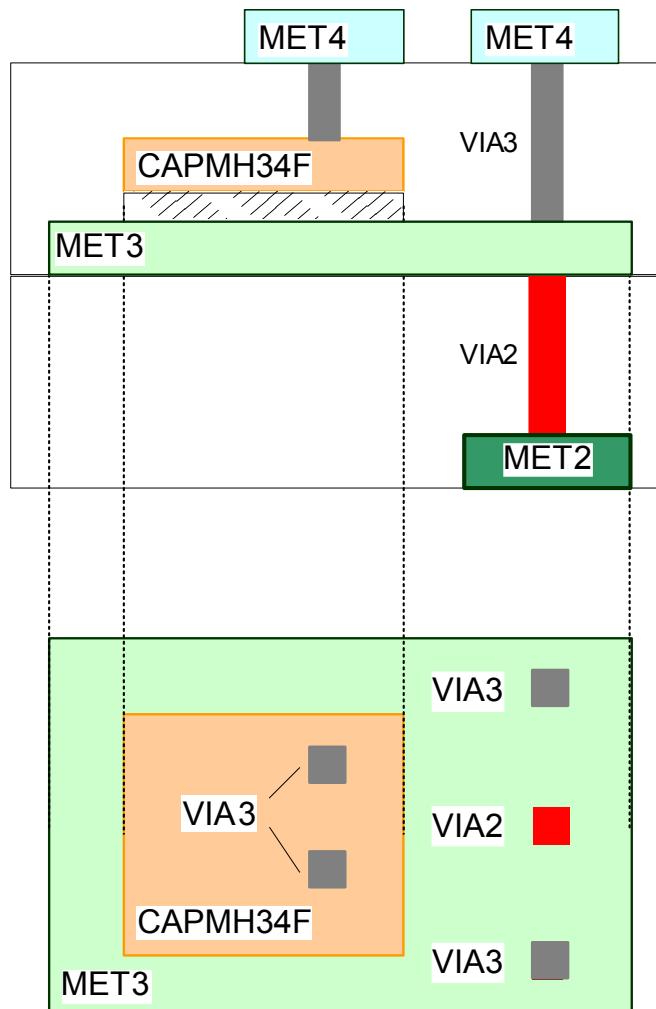


Figure 3.344 cmmh4

3. Layer and Device rules → 3.53 MIMH45 module

## 3.53 MIMH45 module

### 3.53.1 Layer rules

#### CAPMH45F

Name	Description	Value	Unit
B1H5	CAPMH45F without MET4 is not allowed	-	-
B2H5	CAPMH45F overlap of VIA3 or PAD is not allowed	-	-
B3H5	CAPMH45F is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPMH, CAPMH23F, CAPMH34F, CAPM2, CAPM2A, CAPMH2, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B4H5	CAPMH45F without module MET5 is not allowed	-	-
W1H5	Minimum CAPMH45F width	2.0	μm
W2H5	Maximum CAPMH45F bounding box size	30.0 x 30.0	μm x μm
	<b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.		
S1H5	Minimum CAPMH45F spacing/notch	1.5	μm
S7V4	Minimum VIA4 spacing on CAPMH45F	2.0	μm
S1H5PA	Minimum CAPMH45F spacing to PAD	10.0	μm
S1H5V3	Minimum CAPMH45F spacing to VIA3	0.5	μm
S1H5V4	Minimum CAPMH45F spacing to VIA4	0.5	μm
E1H5V4	Minimum CAPMH45F enclosure of VIA4	0.3	μm
E1M4H5	Minimum MET4 enclosure of CAPMH45F	0.5	μm
E7M4V3	Minimum MET4 enclosure of VIA3	0.15	μm
	<b>Note:</b> This rule is related to all VIAs inside CAPMH45F regions extended by 2.5μm.		
E7M4V4	Minimum MET4 enclosure of VIA4	0.15	μm
	<b>Note:</b> This rule is related to all VIAs inside CAPMH45F regions extended by 2.5μm.		
Q4V4	Recommended minimum ratio of VIA4 to CAPMH45F area	1.0	%

3. Layer and Device rules → 3.53 MIMH45 module → 3.53.1 Layer rules → CAPMH45F

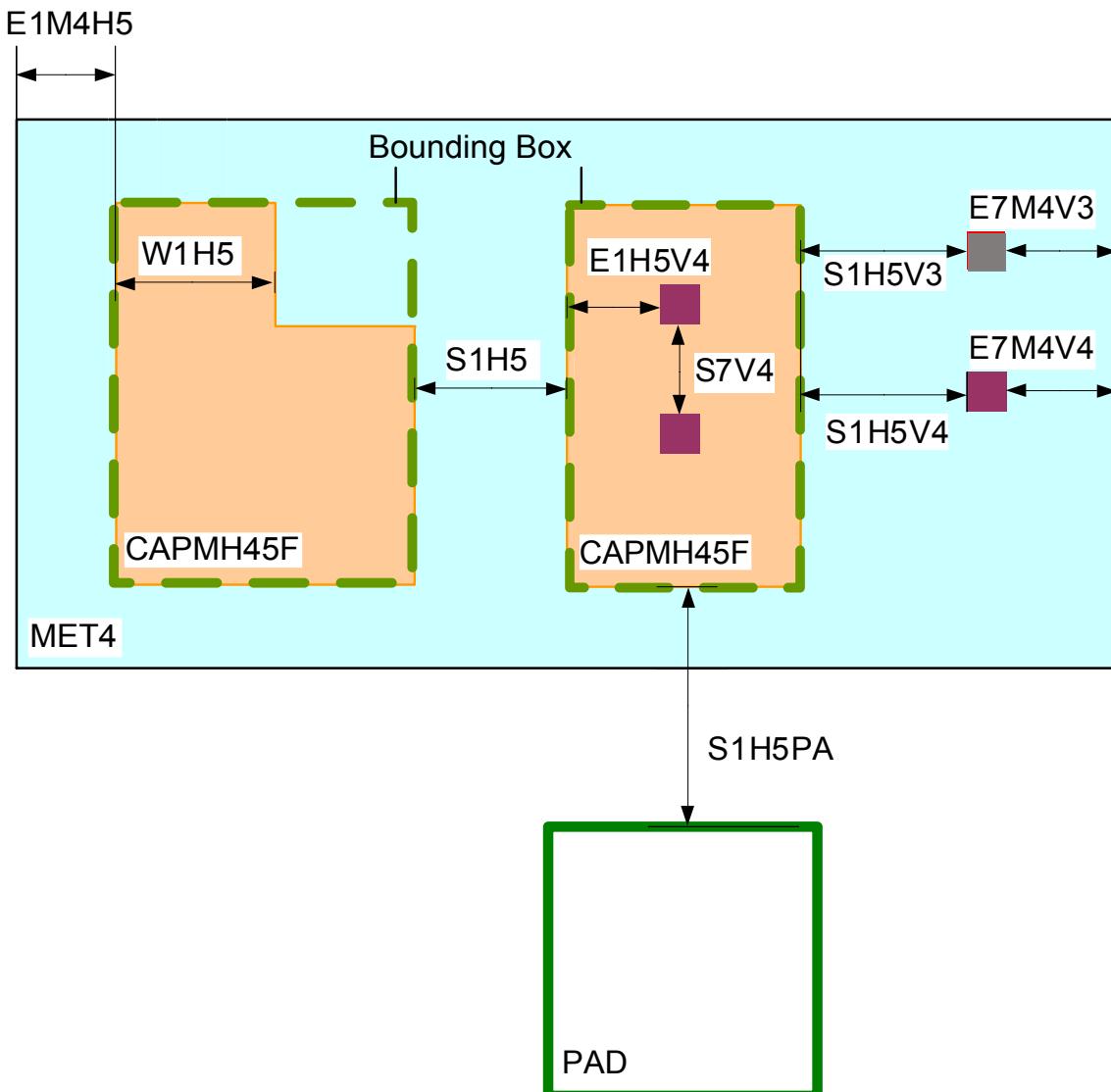


Figure 3.345 CAPMH45F

3. Layer and Device rules → 3.53 MIMH45 module → 3.53.2 Device rules → cmmh5

### 3.53.2 Device rules

#### cmmh5

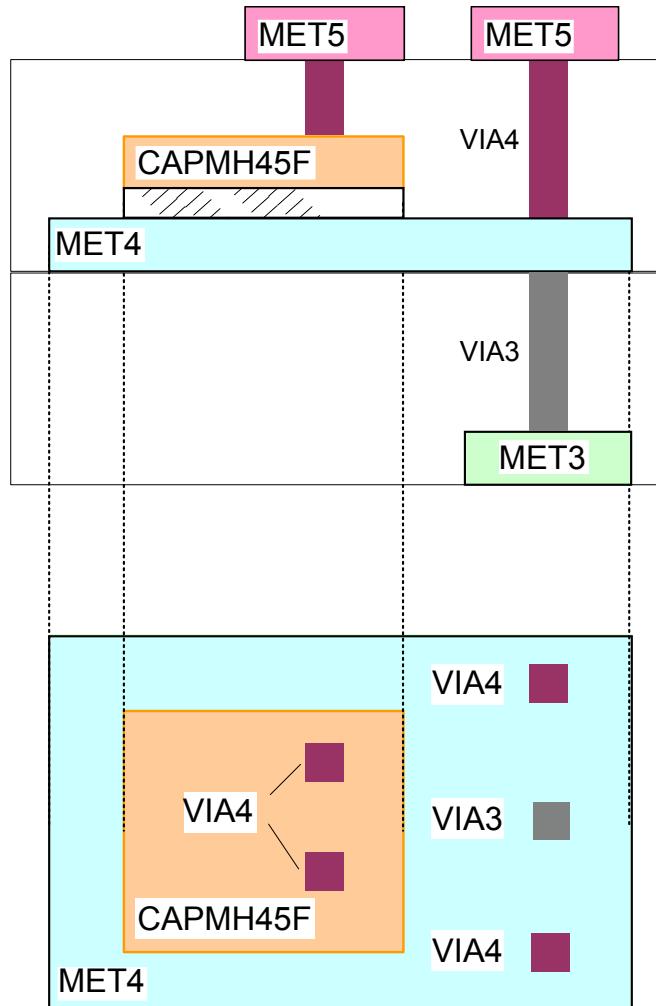


Figure 3.346 cmmh5

3. Layer and Device rules → 3.54 DMIMH module

## 3.54 DMIMH module

### 3.54.1 Layer rules

#### CAPMH2

Name	Description	Value	Unit
B10DH	CAPMH2 without module MET4 or METMID is not allowed	-	-
B1DH	CAPMH2 is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2, CAPM2A, CAPMH2A, CAPM3 or CAPMH3 is present	-	-
B2DH	CAPMH2 must be enclosed by MET2 and MET3	-	-
B3DH	CAPMH2 must not be over VIA1 or PAD	-	-
B4DH	CAPMH2 without VIA2 is not allowed	-	-
B5DH	CAPMH2 without VIATP is not allowed	-	-
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
B6DH	MET2 and METTP must be connected	-	-
	<b>Note:</b> CAPMH2 must be enclosed by METTP.		
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
B7DH	CAPMH2 without VIA3 is not allowed	-	-
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
B8DH	MET2 and MET4 must be connected	-	-
	<b>Note:</b> CAPMH2 must be enclosed by MET4.		
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
B9DH	CAPMH2 without module MET3 is not allowed	-	-
W1DH	Minimum CAPMH2 width	2.0	µm
W2DH	Maximum CAPMH2 bounding box size	30.0 x 30.0	µm x µm
	<b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.		
S1DH	Minimum CAPMH2 spacing/notch	1.5	µm
S7V2	Minimum VIA2 spacing on CAPMH2	2.0	µm
S7V3	Minimum VIA3 spacing on CAPMH2	2.0	µm
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
S7VT	Minimum VIATP spacing on CAPMH2	2.0	µm
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
S1DHPA	Minimum CAPMH2 spacing to PAD	10.0	µm
S1DHV1	Minimum CAPMH2 spacing to VIA1	0.5	µm
S1DHV2	Minimum CAPMH2 spacing to VIA2	0.5	µm
S1DHV3	Minimum CAPMH2 spacing to VIA3	0.5	µm
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
S1DHVT	Minimum CAPMH2 spacing to VIATP	0.5	µm
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
E1DHV2	Minimum CAPMH2 enclosure of VIA2	0.3	µm
E1DHV3	Minimum CAPMH2 enclosure of VIA3	0.3	µm
	<b>Note:</b> Valid if MET4 or MET5 module is selected		
E1DHVT	Minimum CAPMH2 enclosure of VIATP	0.3	µm
	<b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.		
E1M2DH	Minimum MET2 enclosure of CAPMH2	0.5	µm

⇒

## 3. Layer and Device rules → 3.54 DMIMH module→ 3.54.1 Layer rules→ CAPMH2

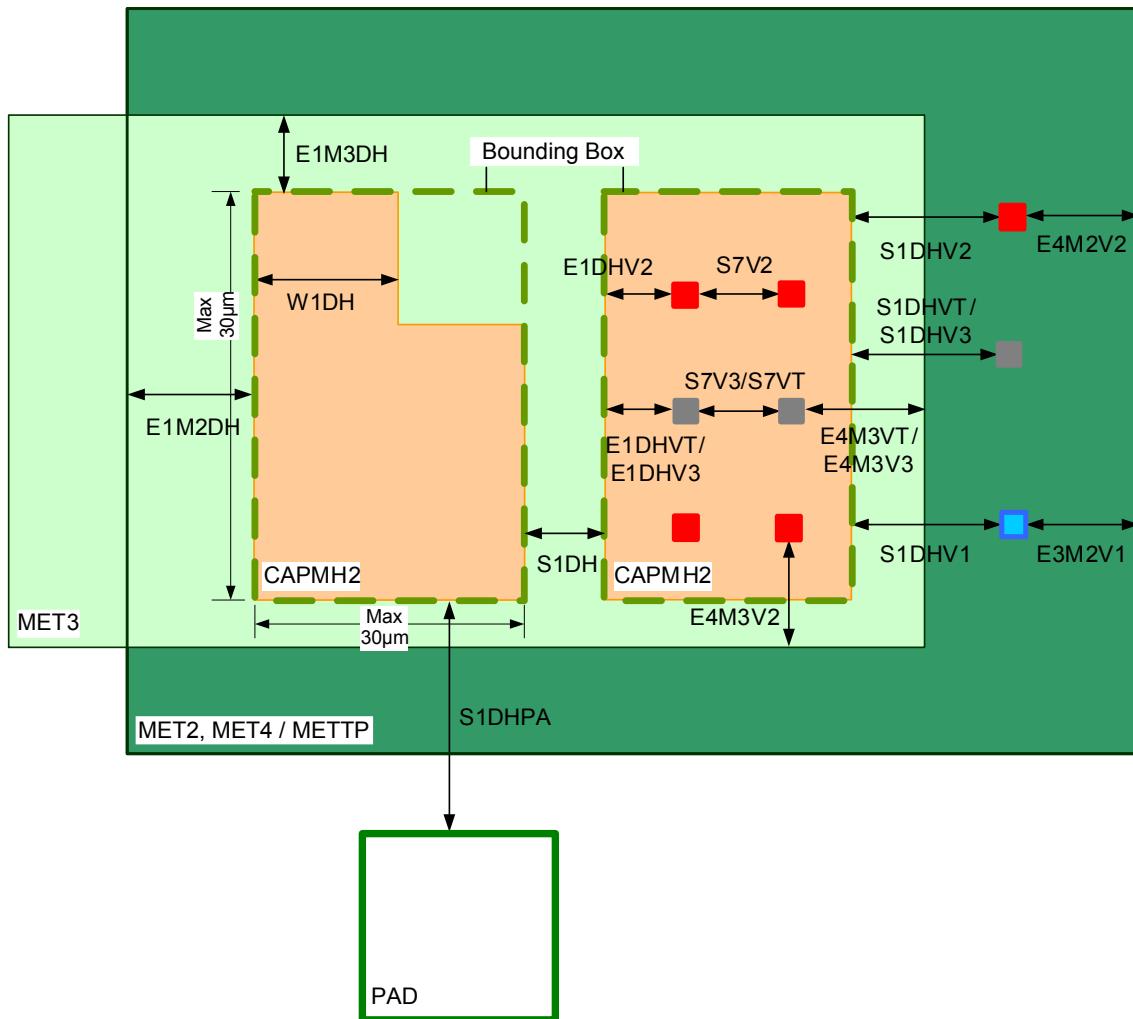
Name	Description	Value	Unit
E1M3DH	Minimum MET3 enclosure of CAPMH2	0.5	µm
E3M2V1	Minimum MET2 enclosure of VIA1  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M2V2	Minimum MET2 enclosure of VIA2  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3V2	Minimum MET3 enclosure of VIA2  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3V3	Minimum MET3 enclosure of VIA3  <b>Note:</b> Valid if MET4 or MET5 module is selected  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
E4M3VT	Minimum MET3 enclosure of VIATP  <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.  <b>Note:</b> This rule is related to all VIAs inside CAPM2 and CAPMH2 regions extended by 2.5µm.	0.15	µm
Q5V2	Recommended minimum ratio of VIA2 to CAPMH2 area	1.0	%
Q5V3	Recommended minimum ratio of VIA3 to CAPMH2 area  <b>Note:</b> Valid if MET4 or MET5 module is selected	1.0	%
Q5VT	Recommended minimum ratio of VIATP to CAPMH2 area  <b>Note:</b> Valid if MET3 module is selected and MET4 module is not selected.	1.0	%

**Note:** The placement of DMIMH must start from MET2 as described in the Table for DMIMH Construction below.

Table for DMIMH Construction

module combination	structure of metal stacking	device	Top MIM metal
LP5MOS/ MOS5	n/a	n/a	n/a
MET3	MET2 / CAPMH2 / MET3 / CAPMH2 / METTP	cdmmh4t	METTP
MET4, MET5	MET2 / CAPMH2 / MET3 / CAPMH2 / MET4	cdmmh4	MET4

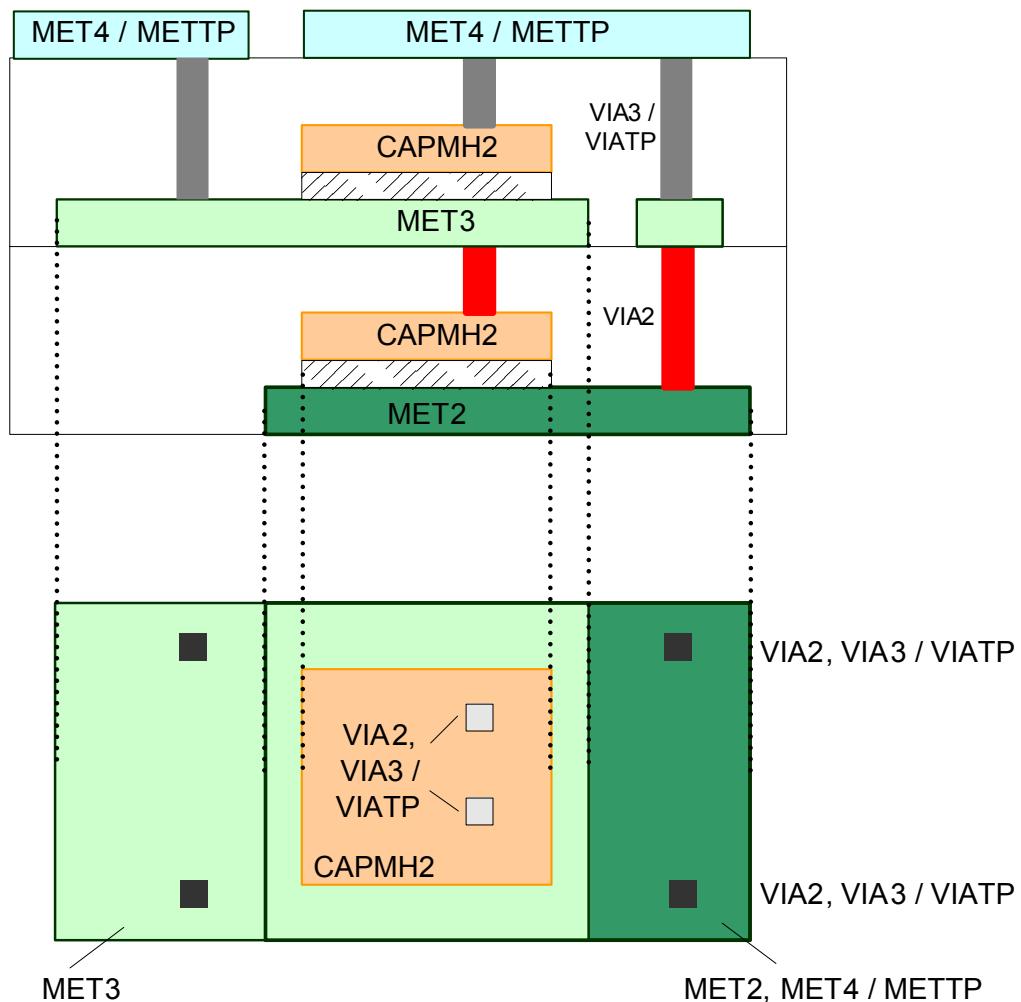
## 3. Layer and Device rules → 3.54 DMIMH module → 3.54.1 Layer rules → CAPMH2

CAPMH2**Figure 3.347 CAPMH2**

3. Layer and Device rules → 3.54 DMIMH module→ 3.54.2 Device rules→ cdmmh4, cdmmh4t

### 3.54.2 Device rules

**cdmmh4, cdmmh4t**



**Figure 3.348** cdmmh4t, cdmmh4

3. Layer and Device rules → 3.55 DMIMH3 module

## 3.55 DMIMH3 module

### 3.55.1 Layer rules

#### CAPMH2A

Name	Description	Value	Unit
B10K3	CAPMH2A without module MET5 or METMID is not allowed	-	-
B1K3	CAPMH2A is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPM2, CAPM3, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPMH2, CAPM2A or CAPMH3 is present	-	-
B2K3	CAPMH2A must be enclosed by MET3 and MET4	-	-
B3K3	CAPMH2A must not be over VIA2 or PAD	-	-
B4K3	CAPMH2A without VIA3 is not allowed	-	-
B5K3	CAPMH2A without VIATP is not allowed  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	-	-
	MET3 and METTP must be connected	-	-
B6K3	<b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.  <b>Note:</b> CAPMH2A must be enclosed by METTP		
B7K3	CAPMH2A without VIA4 is not allowed  <b>Note:</b> Valid if MET5 module is selected.	-	-
B8K3	MET3 and MET5 must be connected  <b>Note:</b> Valid if MET5 module is selected.  <b>Note:</b> CAPMH2A must be enclosed by MET5	-	-
B9K3	CAPMH2A without module MET4 is not allowed	-	-
W1K3	Minimum CAPMH2A width	2.0	µm
W2K3	Maximum CAPMH2A bounding box size  <b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	µm x µm
S10V3	Minimum VIA3 spacing on CAPMH2A	2.0	µm
S1K3	Minimum CAPMH2A spacing / notch	1.5	µm
S8V4	Minimum VIA4 spacing on CAPMH2A  <b>Note:</b> Valid if MET5 module is selected.	2.0	µm
S1K3PA	Minimum CAPMH2A spacing to PAD	10.0	µm
S1K3V2	Minimum CAPMH2A spacing to VIA2	0.5	µm
S1K3V3	Minimum CAPMH2A spacing to VIA3	0.5	µm
S1K3V4	Minimum CAPMH2A spacing to VIA4  <b>Note:</b> Valid if MET5 module is selected.	0.5	µm
S1K3VT	Minimum CAPMH2A spacing to VIATP  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.5	µm
S9VT	Minimum VIATP spacing on CAPMH2A  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	2.0	µm
E1K3V3	Minimum CAPMH2A enclosure of VIA3	0.3	µm
E1K3V4	Minimum CAPMH2A enclosure of VIA4  <b>Note:</b> Valid if MET5 module is selected.	0.3	µm
E1K3VT	Minimum CAPMH2A enclosure of VIATP  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.3	µm
E1M3K3	Minimum MET3 enclosure of CAPMH2A	0.5	µm

⇒

## 3. Layer and Device rules → 3.55 DMIMH3 module → 3.55.1 Layer rules → CAPMH2A

Name	Description	Value	Unit
E1M4K3	Minimum MET4 enclosure of CAPMH2A	0.5	µm
E5M4V3	Minimum MET4 enclosure of VIA3  <b>Note:</b> This rule is related to all VIAs inside CAPMH2A region extended by 2.5µm.	0.15	µm
E7M4VT	Minimum MET4 enclosure of VIATP  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.  <b>Note:</b> This rule is related to all VIAs inside CAPMH2A region extended by 2.5µm.	0.15	µm
E8M3V2	Minimum MET3 enclosure of VIA2  <b>Note:</b> This rule is related to all VIAs inside CAPMH2A region extended by 2.5µm.	0.15	µm
E8M4V4	Minimum MET4 enclosure of VIA4  <b>Note:</b> Valid if MET5 module is selected.  <b>Note:</b> This rule is related to all VIAs inside CAPMH2A region extended by 2.5µm.	0.15	µm
E9M3V3	Minimum MET3 enclosure of VIA3  <b>Note:</b> This rule is related to all VIAs inside CAPMH2A region extended by 2.5µm.	0.15	µm
Q6V4	Recommended minimum ratio of VIA4 to CAPMH2A area  <b>Note:</b> Valid if MET5 module is selected.	1.0	%
Q8V3	Recommended minimum ratio of VIA3 to CAPMH2A area	1.0	%
Q8VT	Recommended minimum ratio of VIATP to CAPMH2A area  <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	1.0	%

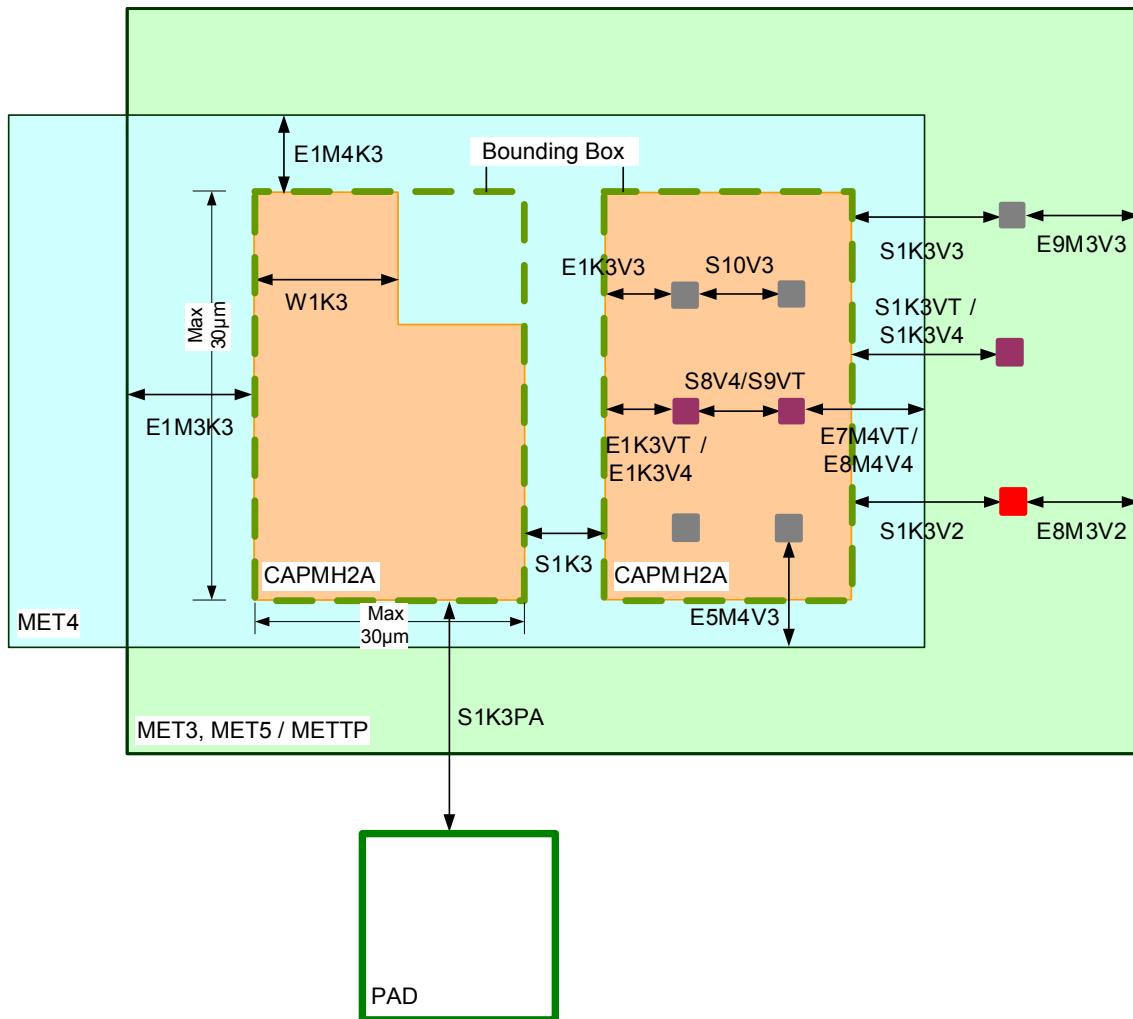
**Note:** The placement of DMIMH3 must start from MET3 as described in the Table for DMIMH3 Construction below.

Table for DMIMH3 Construction

module combination	structure of metal stacking	device	Top MIM metal
LP5MOS/MOS5	MET3 / CAPMH2A / MET4 / CAPMH2A / METTP	cdmmh5t	METTP
MET5	MET3 / CAPMH2A / MET4 / CAPMH2A / MET5	cdmmh5	MET5

3. Layer and Device rules → 3.55 DMIMH3 module → 3.55.1 Layer rules → CAPMH2A

CAPMH2A

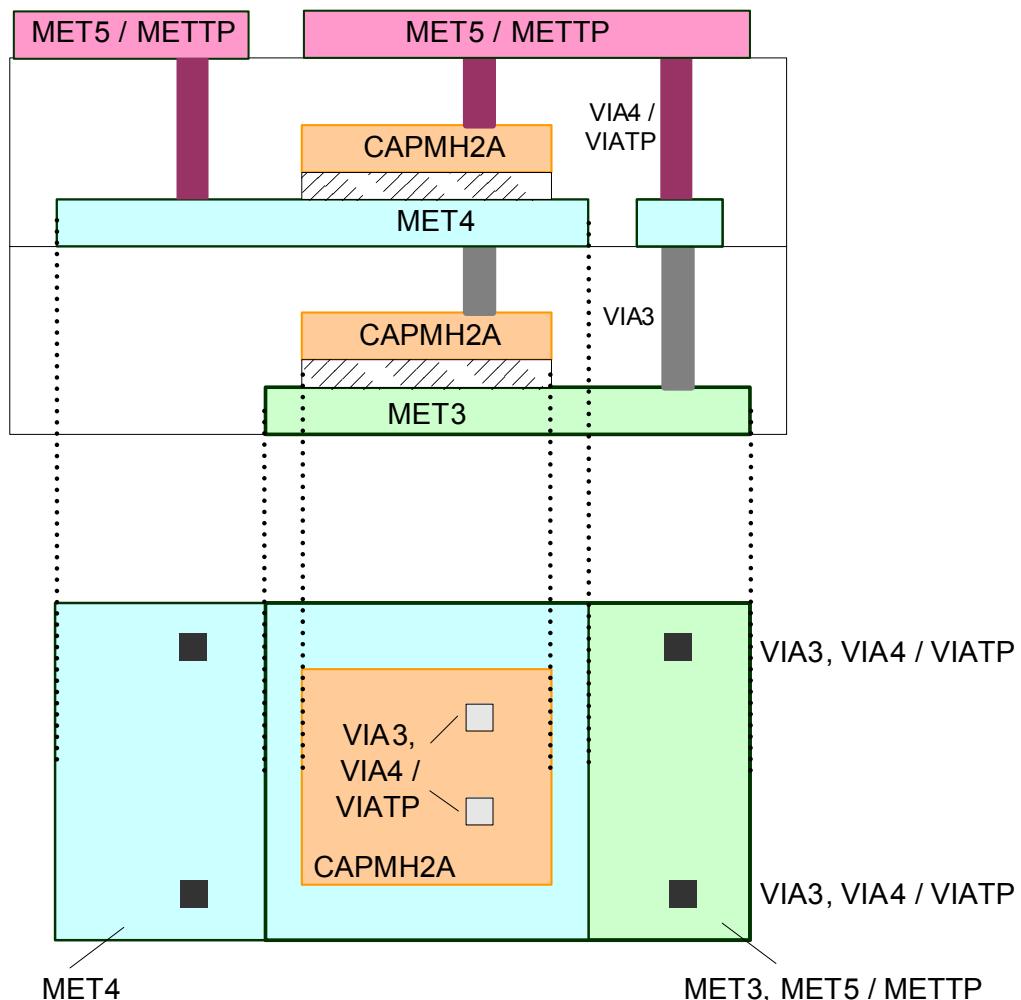


**Figure 3.349** CAPMH2A

3. Layer and Device rules → 3.55 DMIMH3 module → 3.55.2 Device rules → cdmmh5, cdmmh5t

### 3.55.2 Device rules

**cdmmh5, cdmmh5t**



**Figure 3.350** cdmmh5t, cdmmh5

3. Layer and Device rules → 3.56 TMIMH module

## 3.56 TMIMH module

### 3.56.1 Layer rules

#### CAPMH3

Name	Description	Value	Unit
B10TH	CAPMH3 without module MET4 is not allowed	-	-
B11TH	CAPMH3 without module MET5 or METMID is not allowed	-	-
B1TH	CAPMH3 is not allowed when CAPM, CAPM23F, CAPM34F, CAPM45F, CAPMH, CAPMH23F, CAPMH34F, CAPMH45F, CAPM2, CAPM2A, CAPMH2, CAPMH2A or CAPM3 is present	-	-
B2TH	CAPMH3 must be enclosed by MET2, MET3 and MET4	-	-
B3TH	CAPMH3 must not be over VIA1 or PAD	-	-
B4TH	CAPMH3 without VIA2 or VIA3 is not allowed	-	-
B5TH	MET2 and MET4 must be connected	-	-
B6TH	CAPMH3 without VIATP is not allowed <b>Note:</b> Valid if MET4 is selected and MET5 module is not selected	-	-
B7TH	MET3 and METTP must be connected <b>Note:</b> CAPMH3 must be enclosed by METTP. <b>Note:</b> Valid if MET4 is selected and MET5 module is not selected	-	-
B8TH	CAPMH3 without VIA4 is not allowed <b>Note:</b> Valid if MET5 module is selected.	-	-
B9TH	MET3 and MET5 must be connected <b>Note:</b> CAPMH3 must be enclosed by MET5. <b>Note:</b> Valid if MET5 module is selected.	-	-
W1TH	Minimum CAPMH3 width	2.0	µm
W2TH	Maximum CAPMH3 bounding box size <b>Note:</b> The bounding box is the generated minimum rectangle enclosing the polygon.	30.0 x 30.0	µm x µm
S1TH	Minimum CAPMH3 spacing/notch	1.5	µm
S4V4	Minimum VIA4 spacing on CAPMH3 <b>Note:</b> Valid if MET5 module is selected.	2.0	µm
S8V2	Minimum VIA2 spacing on CAPMH3	2.0	µm
S8V3	Minimum VIA3 spacing on CAPMH3	2.0	µm
S8VT	Minimum VIATP spacing on CAPMH3 <b>Note:</b> Valid if MET4 is selected and MET5 module is not selected	2.0	µm
S1THPA	Minimum CAPMH3 spacing to PAD	10.0	µm
S1THV1	Minimum CAPMH3 spacing to VIA1	0.5	µm
S1THV2	Minimum CAPMH3 spacing to VIA2	0.5	µm
S1THV3	Minimum CAPMH3 spacing to VIA3	0.5	µm
S1THV4	Minimum CAPMH3 spacing to VIA4 <b>Note:</b> Valid if MET5 module is selected.	0.5	µm
S1THVT	Minimum CAPMH3 spacing to VIATP <b>Note:</b> Valid if MET4 is selected and MET5 module is not selected	0.5	µm
E1M2TH	Minimum MET2 enclosure of CAPMH3	0.5	µm
E1M3TH	Minimum MET3 enclosure of CAPMH3	0.5	µm
E1M4TH	Minimum MET4 enclosure of CAPMH3	0.5	µm

⇒

## 3. Layer and Device rules → 3.56 TMIMH module → 3.56.1 Layer rules → CAPMH3

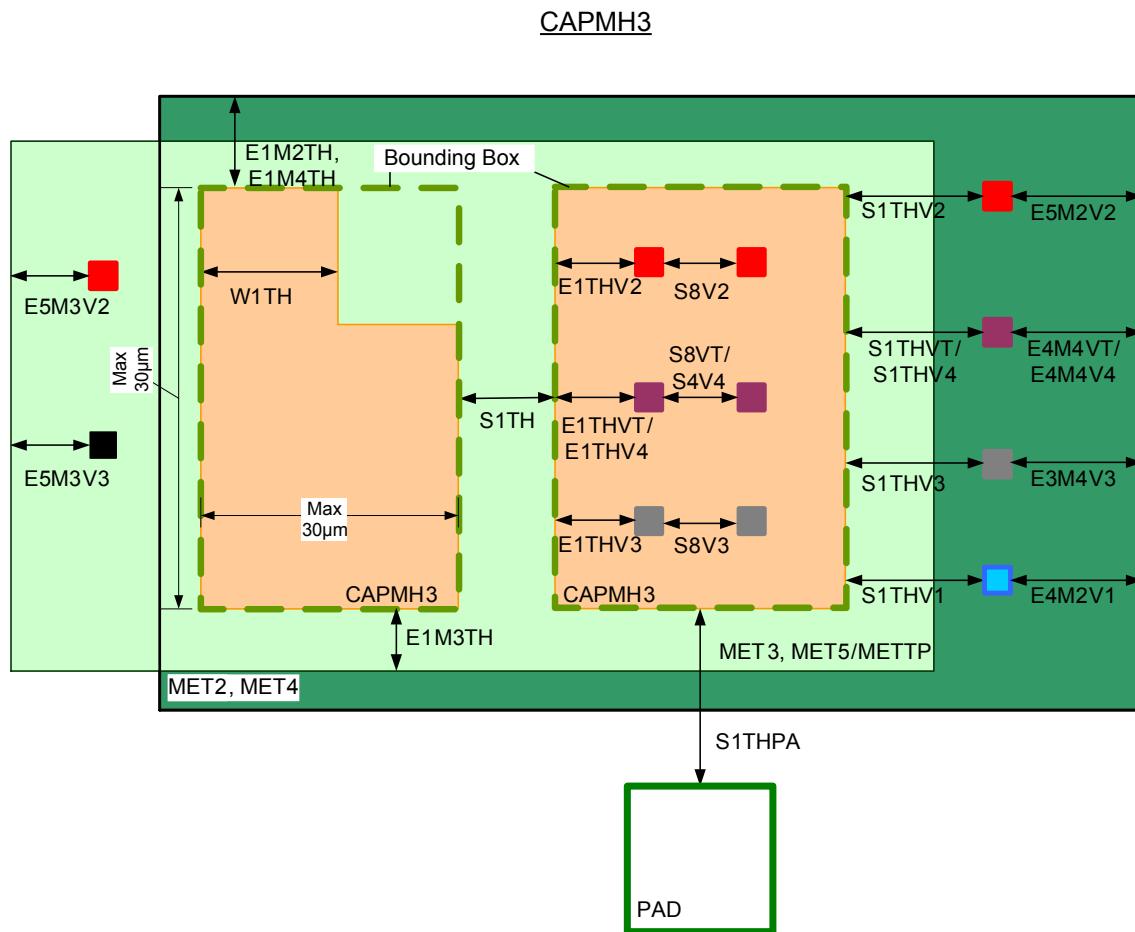
Name	Description	Value	Unit
E1THV2	Minimum CAPMH3 enclosure of VIA2	0.3	µm
E1THV3	Minimum CAPMH3 enclosure of VIA3	0.3	µm
E1THV4	Minimum CAPMH3 enclosure of VIA4 <b>Note:</b> Valid if MET5 module is selected.	0.3	µm
E1THVT	Minimum CAPMH3 enclosure of VIATP <b>Note:</b> Valid if MET4 is selected and MET5 module is not selected <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.3	µm
E3M4V3	Minimum MET4 enclosure of VIA3 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M2V1	Minimum MET2 enclosure of VIA1 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M4V4	Minimum MET4 enclosure of VIA4 <b>Note:</b> Valid if MET5 module is selected. <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E4M4VT	Minimum MET4 enclosure of VIATP <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm. <b>Note:</b> Valid if MET4 module is selected and MET5 module is not selected.	0.15	µm
E5M2V2	Minimum MET2 enclosure of VIA2 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E5M3V2	Minimum MET3 enclosure of VIA2 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
E5M3V3	Minimum MET3 enclosure of VIA3 <b>Note:</b> This rule is related to all VIAs inside CAPM3 and CAPMH3 regions extended by 2.5 µm.	0.15	µm
Q2V3	Recommended minimum ratio of VIA3 to CAPMH3 area	1.0	%
Q2V4	Recommended minimum ratio of VIA4 to CAPMH3 area <b>Note:</b> Valid if MET5 module is selected.	1.0	%
Q6V2	Recommended minimum ratio of VIA2 to CAPMH3 area	1.0	%
Q6V3	Recommended minimum ratio of VIA3 to CAPMH3 area	1.0	%
Q6VT	Recommended minimum ratio of VIATP to CAPMH3 area <b>Note:</b> Valid if MET4 is selected and MET5 module is not selected	1.0	%

**Note:** The placement of TMIMH must start from MET2 as described in the Table for TMIMH Construction.

Table for TMIMH Construction

module combination	structure of metal stacking	device	Top MIM metal
LP5MOS/MOS5	n/a	n/a	n/a
MET4	MET2 / CAPMH3 / MET3 / CAPMH3 / MET4 / CAPMH3 / METTP	ctmmh5t	METTP
MET5	MET2 / CAPMH3 / MET3 / CAPMH3 / MET4 / CAPMH3 / MET5	ctmmh5	MET5

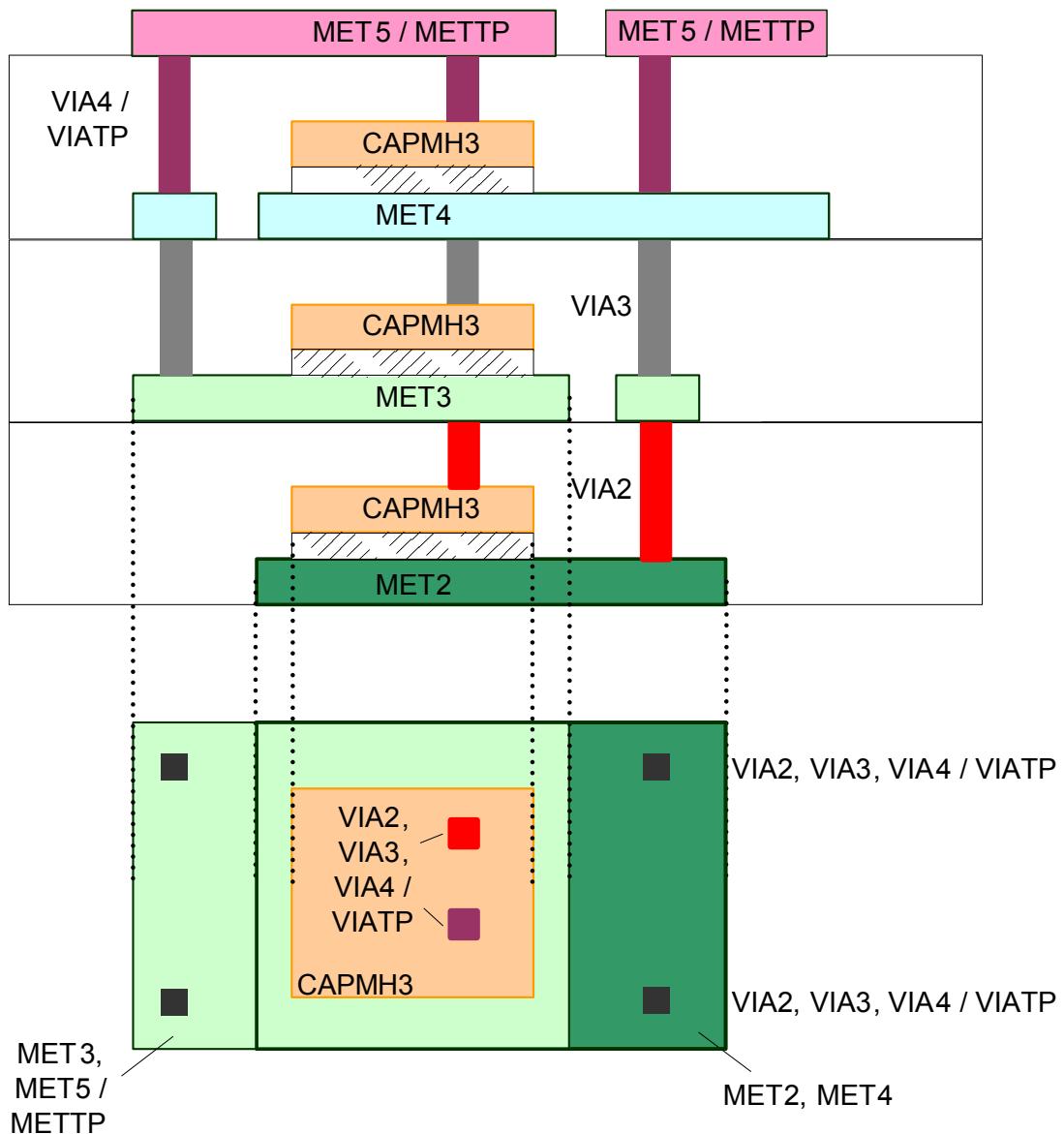
## 3. Layer and Device rules → 3.56 TMIMH module → 3.56.1 Layer rules → CAPMH3

**Figure 3.351** CAPMH3

3. Layer and Device rules → 3.56 TMIMH module → 3.56.2 Device rules → ctmmh5, ctmmh5t

### 3.56.2 Device rules

#### ctmmh5, ctmmh5t



**Figure 3.352** ctmmh5t, ctmmh5

3. Layer and Device rules → 3.57 CSP5L module

## 3.57 CSP5L module

### 3.57.1 Device rules

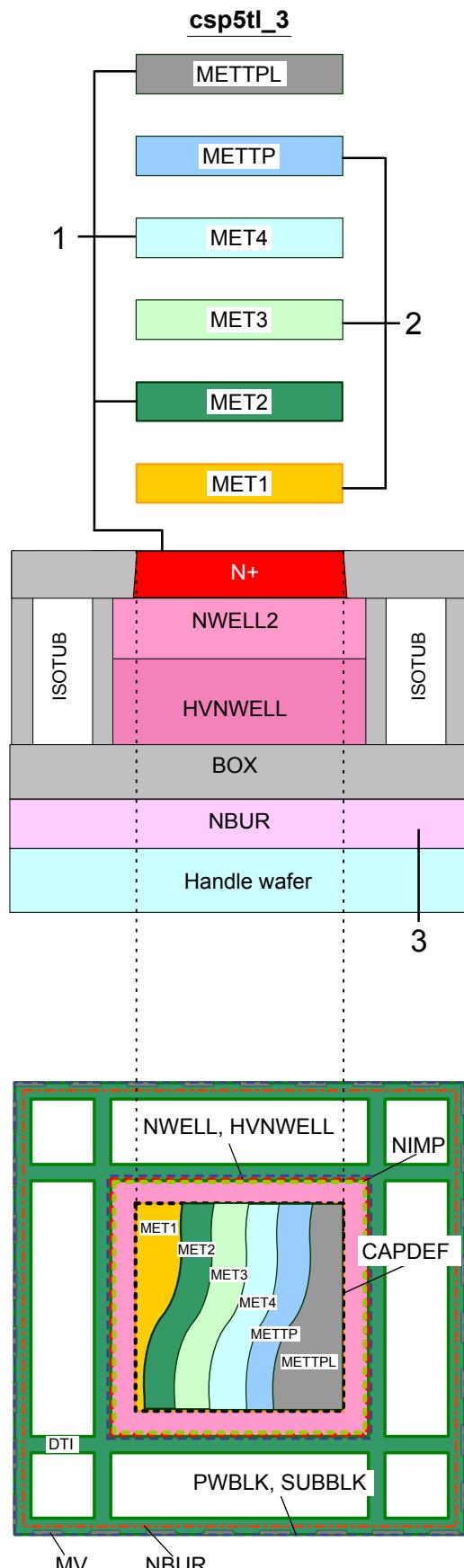
#### csp5tl\_3

The layout is predefined and scalable concerning width and length only. All other dimensions must not be changed.

**Note:** MV and HVNWELL are necessary for this device.

**Note:** CAPDEF is necessary for csp5tl\_3.

3. Layer and Device rules → 3.57 CSP5L module → 3.57.1 Device rules → csp5tl\_3



**Figure 3.353 csp5tl\_3**

3. Layer and Device rules → 3.57 CSP5L module→ 3.57.1 Device rules→ csp5tla\_3

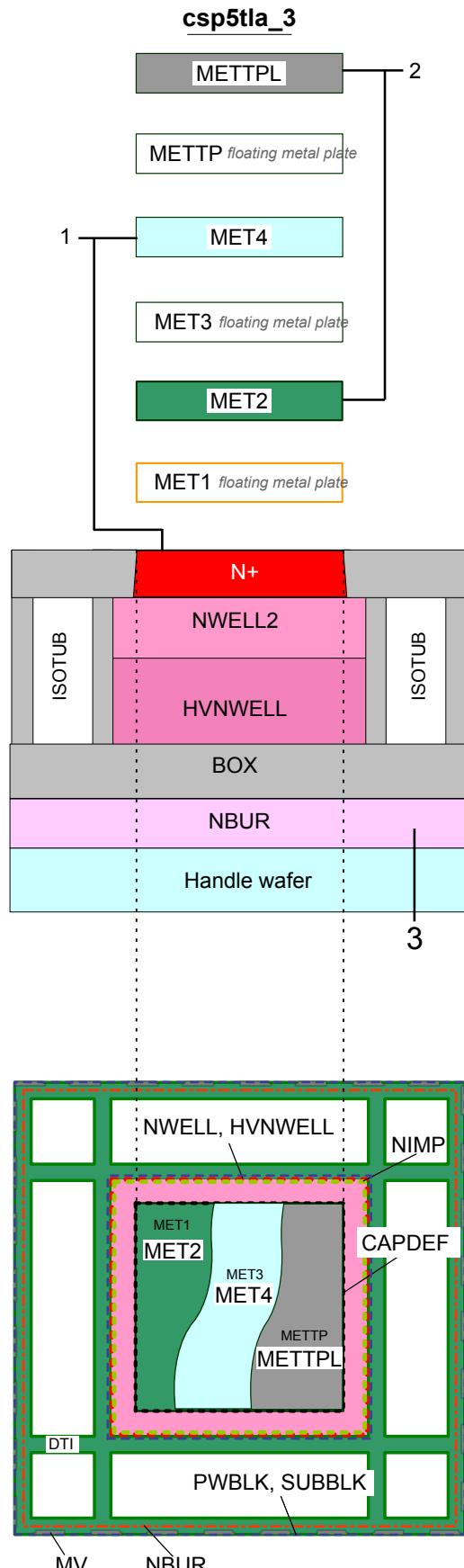
### **csp5tla\_3**

The layout is predefined and scalable concerning width and length only. All other dimensions must not be changed.

**Note:** MV and HVNWELL are necessary for this device.

**Note:** CAPDEF is necessary for csp5tla\_3.

3. Layer and Device rules → 3.57 CSP5L module → 3.57.1 Device rules → csp5tla\_3



**Figure 3.354 csp5tla\_§**

3. Layer and Device rules → 3.58 CEEPROM module

### **3.58 CEEPROM module**

No module specific layer or device rules are defined.

3. Layer and Device rules → 3.59 NVM module

## 3.59 NVM module

Ready-to-use SONOS based non-volatile memory blocks are available for NVM module (FLASH and EEPROM).

The rules of layers and devices only used for non-volatile memory blocks are not described in this specification. Because additional devices are not available for the NVM and FLASH modules this specification does not declare any additional rules.

### 3.59.1 Layer rules

#### PWS

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design

Name	Description	Value	Unit
BDPS	Not allowed to be used by customers	-	-
<b>Note:</b> Layer for predefined memory blocks only. Reserved layer.			

#### SCI

This layer is also relevant to the NLEAK/ PLEAK guidelines. It is required to follow the NLEAK/ PLEAK guidelines to ensure functionality of the circuit design

Name	Description	Value	Unit
BDSC	Not allowed to be used by customers	-	-
<b>Note:</b> Layer for predefined memory blocks only. Reserved layer.			

3. Layer and Device rules → 3.60 OTP5 module

## 3.60 OTP5 module

No module specific layer or device rules are defined.

3. Layer and Device rules → 3.61 BOTDIE module

## 3.61 BOTDIE module

### 3.61.1 Layer rules

#### BDO

Name	Description	Value	Unit
B1BD	BDO without METCOP is not allowed (except BDO_VERIFY)	-	-
B2BD	BDO overlap of METCOP is not allowed  <b>Note:</b> Only valid for BDO_VERIFY	-	-
B3BD	BDO overlap of VIACOP is not allowed  <b>Note:</b> Only valid for BDO_VERIFY	-	-
B4BD	BDO_VERIFY crossing BDO edge is not allowed	-	-
W1BD	Minimum BDO width	15.0	µm
S1BD	Minimum BDO spacing / notch	30.0	µm
S1BDML	Minimum BDO spacing to METTPL  <b>Note:</b> Valid if METTHK module is selected.	5.0	µm
S1BDMT	Minimum BDO spacing to METTP  <b>Note:</b> Valid if METMID module is selected and not METTHK	5.0	µm
E1BDVC	Minimum BDO enclosure of VIACOP	7.0	µm
<i>E1CEBD</i>	Minimum customer chip edge enclosure of BDO  <b>Note:</b> Customer chip is the polygon that represents the least enclosing rectangle of the database.	25.0	µm
E1BDML	Minimum BDO extension beyond METTPL  <b>Note:</b> Valid if METTHK module is selected.	5.0	µm
E1BDMT	Minimum BDO extension beyond METTP  <b>Note:</b> Valid if METMID module is selected and not METTHK	5.0	µm
E1MLBD	Minimum METTPL extension beyond BDO  <b>Note:</b> Valid if METTHK module is selected.	5.0	µm
E1MTBD	Minimum METTP extension beyond BDO  <b>Note:</b> Valid if METMID module is selected and not METTHK	5.0	µm
O1MLBD	Minimum METTPL overlap of BDO  <b>Note:</b> Valid if METTHK module is selected.	5.0	µm
O1MTBD	Minimum METTP overlap of BDO  <b>Note:</b> Valid if METMID module is selected and not METTHK	5.0	µm

## 3. Layer and Device rules → 3.61 BOTDIE module → 3.61.1 Layer rules → BDO

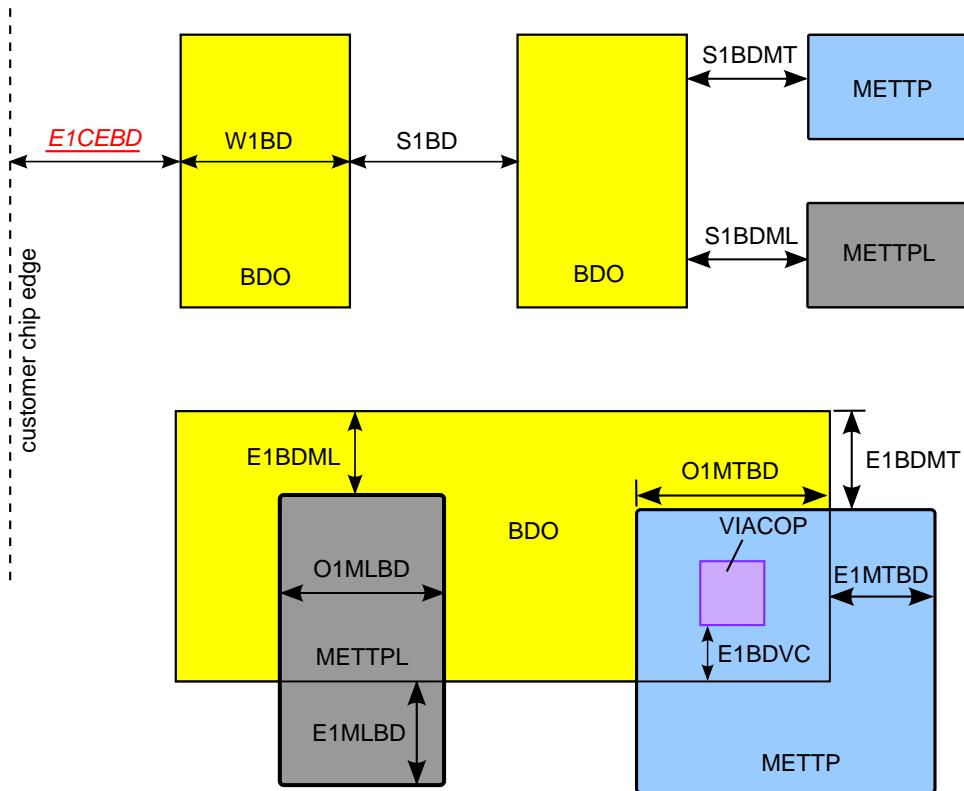


Figure 3.355 BDO

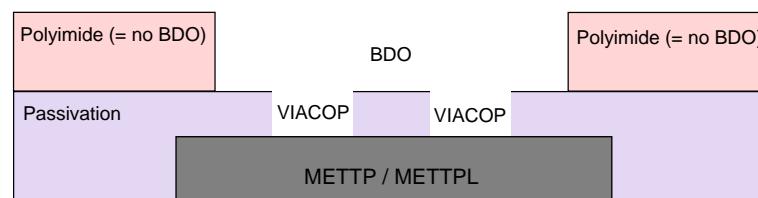
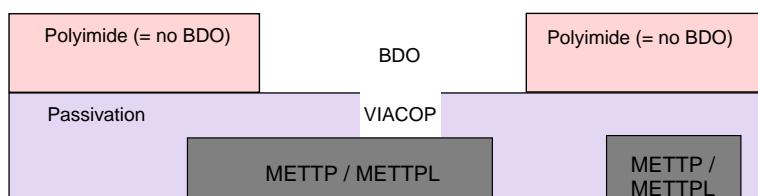
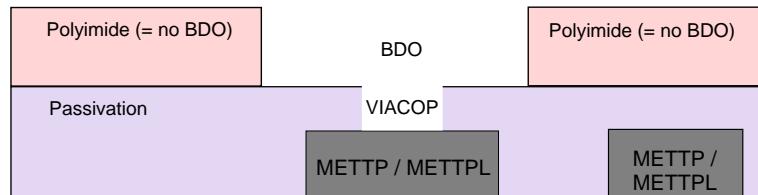


Figure 3.356 BDO related cross sectional diagram

3. Layer and Device rules → 3.62 FLATPV module

## 3.62 FLATPV module

For the FLATPV module, a planar passivation layer is offered as an alternative to the standard passivation, which is non-planar. The passivation thickness above the top metal layer is unchanged, refer to parameter THV. This alternative passivation scheme may be suitable for post-processing or packaging solutions requiring planar passivation. Primitive devices are not defined for the FLATPV module.

3. Layer and Device rules → 3.63 SMALLPAD module

### **3.63 SMALLPAD module**

Design rules for the SMALLPAD section are shown together with the Periphery Rules.

3. Layer and Device rules → 3.64 PIMIDE module

## 3.64 PIMIDE module

### 3.64.1 Layer rules

#### NOPIM

The layer NOPIM defines areas which are not covered by polyimide. PAD areas are realized by default as areas without polyimide according to the mask generation procedure (layer area including PAD + sizing).

Name	Description	Value	Unit
W1IB	Minimum NOPIM width	60.0	µm
S1IB	Minimum NOPIM spacing/notch	20.0	µm
S1IBPA	Minimum NOPIM spacing to PAD	40.0	µm

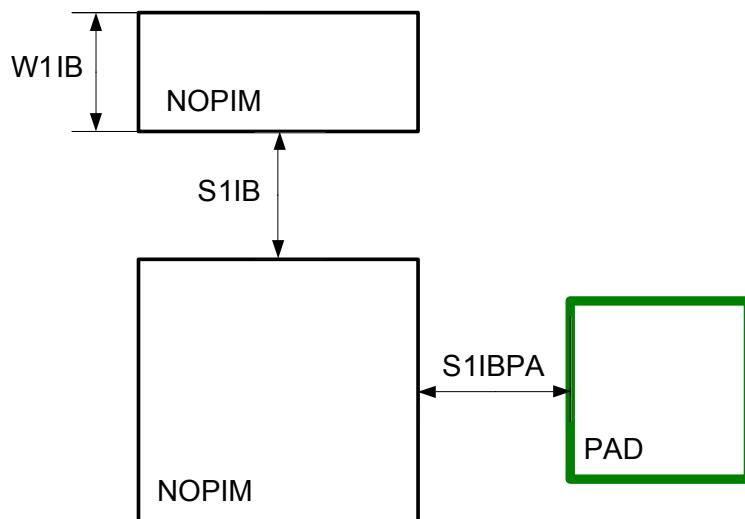


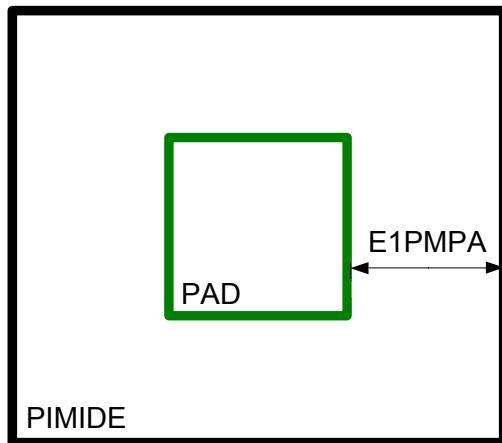
Figure 3.357 NOPIM

3. Layer and Device rules → 3.64 PIMIDE module → 3.64.1 Layer rules → PIMIDE

## PIMIDE

Name	Description	Value	Unit
<i>B1PAPM</i>	PAD without PIMIDE marker is not allowed	-	-
	<b>Note:</b> Checked with standard DRC if NOPIM or PIMIDE is present.		
	<b>Note:</b> Not checked with standard DRC, option for check is available.		
<i>E1PMPA</i>	Minimum PIMIDE marker enclosure of PAD	15.0	µm
	<b>Note:</b> Checked with standard DRC if NOPIM or PIMIDE is present.		
	<b>Note:</b> Not checked with standard DRC, option for check is available.		

**Note:** For these rules to be checked, the PIMIDE switch in DRC check must be turned on when PIMIDE module is selected.



**Figure 3.358** PIMIDE

## 4. Periphery rules

## 4. Periphery rules

### 4.1 Layer rules

#### PAD

The following rules are generally valid for PAD layer:

Name	Description	Value	Unit
B19PA	Small PAD overlap Circuit-Under-Pad Bond PAD, Probe PAD or User PAD is not allowed  <b>Note:</b> Valid if SMALLPAD module is selected.  <b>Note:</b> Valid if Small Pad is marked with text "SMALLPAD" on the layer PAD (SMALLPAD).	-	-
B1PA	PAD without METTP is not allowed  <b>Note:</b> Valid if METMID module is selected and METTHK module is not selected.	-	-
B1PAIB	Small PAD is not allowed when NOPIM is present  <b>Note:</b> Valid if SMALLPAD module is selected.  <b>Note:</b> Valid if Small Pad is marked with text "SMALLPAD" on the layer PAD (SMALLPAD).	-	-
B2PAPM	Small PAD is not allowed when PIMIDE is present  <b>Note:</b> Valid if SMALLPAD module is selected.  <b>Note:</b> Valid if Small Pad is marked with text "SMALLPAD" on the layer PAD (SMALLPAD).	-	-
B4PA	PAD without METTPL is not allowed  <b>Note:</b> Valid if METTHK module is selected.	-	-
B3VC	VIACOP crossing PAD edge is not allowed	-	-
B5PA	PAD crossing VIACOP edge is not allowed	-	-
W1PA	Minimum PAD width (except Small PAD)	15.0	µm
W2PA	Minimum Small PAD width  <b>Note:</b> Valid if SMALLPAD module is selected.  <b>Note:</b> Valid if Small Pad is marked with text "SMALLPAD" on the layer PAD (SMALLPAD).	2.0	µm
S1PA	Minimum PAD spacing/notch	7.0	µm
S1BDPA	Minimum BDO spacing to PAD	30.0	µm
S1MCPA	Minimum METCOP spacing to PAD	10.0	µm
S1VCPA	Minimum VIACOP spacing to PAD	7.0	µm
E1BDPA	Minimum BDO enclosure of PAD	7.0	µm
E1MLPA	Minimum METTPL enclosure of PAD  <b>Note:</b> Valid if METTHK module is selected.	2.0	µm
E2MTPA	Minimum METTP enclosure of PAD  <b>Note:</b> Valid if METMID module is selected and METTHK module is not selected.	2.0	µm

- Note:**
1. It is recommended to convert existing PAD structures into VIACOP when THKCOP module is used
  2. PAD without BDO will be covered with bottom dielectric (polyimide)
  3. In case of PAD without METCOP, the pad aluminum surface will be about 15µm to 20µm lower than the METCOP surface. Assembly process of aluminum pads together with METCOP landing area might lead to issues and it is not recommended
  4. No dedicated pad is necessary when using THKCOP module. Design of METCOP landing areas need to fulfill the assembly requirements
  5. PAD with BDO but without METCOP in PAD area (for example Probe Pad): additional usage of BDO\_VERIFY is required

**Note: Marking of PAD:**

The following PAD types must be marked with text on the layer PAD (VERIFICATION):  
 customer specific PAD with text "USERPAD"  
 Circuit-Under-Pad Bond PAD with text "CUPAD"



#### 4. Periphery rules → 4.1 Layer rules→ PAD

probe PAD with text "PROBEPAD"

The Small PAD must be marked with text on the layer PAD (SMALLPAD) with text "SMALLPAD".

If they have either no text or different text labels to those listed above, bond PAD rules will be used for checking the pad.

#### **Important Notes:**

The responsibility is wholly on the customer to agree with the assembly requirements of the assembly house used.

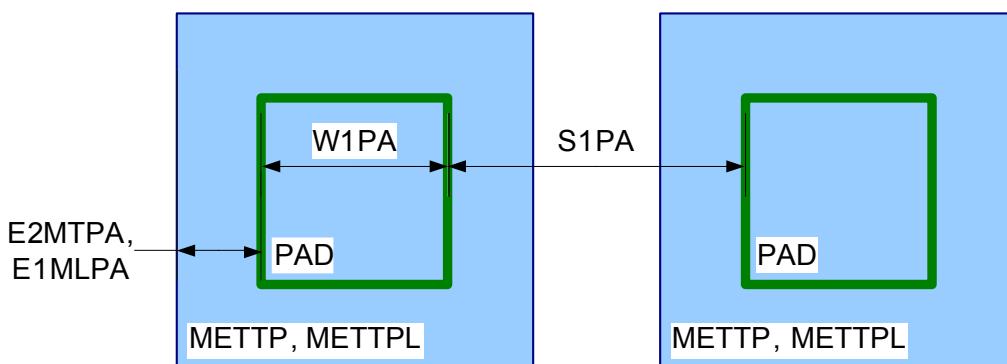
Customer specific pad layouts are only checked with the rules of this section "PAD Rules".

The rules of this section are to ensure the correct preparation of openings in layer PAD within the wafer process. They do not include any considerations related to other layers, devices or to the assembly process employed.

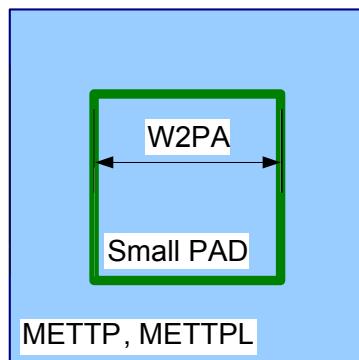
Customers must ensure that any extra requirements are satisfied, as X-FAB will take no responsibility for such items. For example:

- placing of further layers under PAD;
- placing of primitive devices under PAD;
- PAD spacing to any unrelated structures;
- assembly process influences;
- assembly design rules of the assembly house used;
- the needs of special assembly technologies (e.g. bumping, flip-chip, multi-die packaging).

Additional rules apply for bond pads and probe pads - see relevant sections.

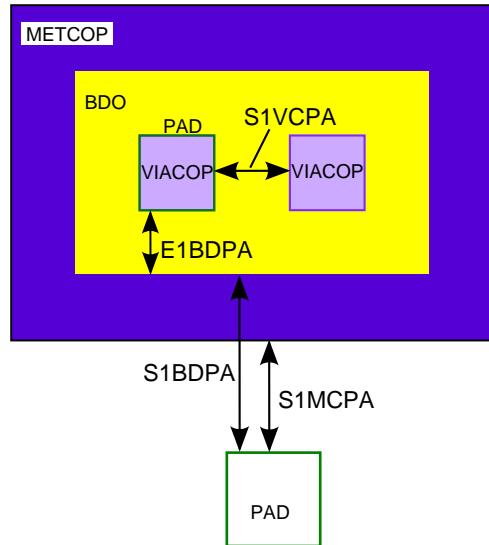


**Figure 4.1** PAD



**Figure 4.2** Small PAD

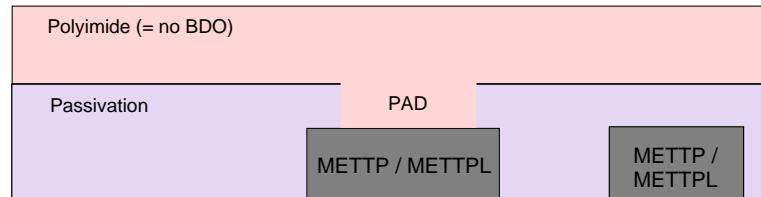
## 4. Periphery rules → 4.1 Layer rules→ PAD



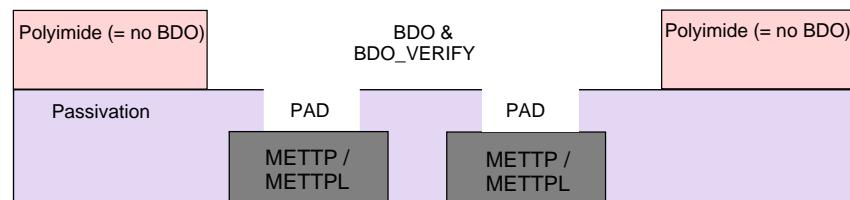
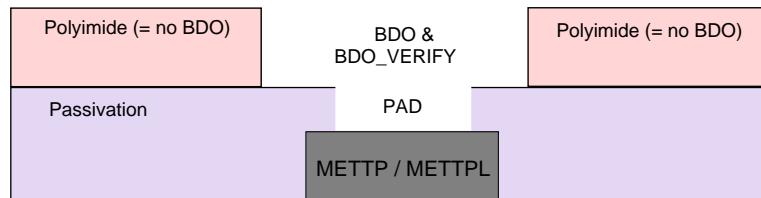
**Figure 4.3** PAD with THKCOP, BDO module

## 4. Periphery rules → 4.1 Layer rules→ PAD

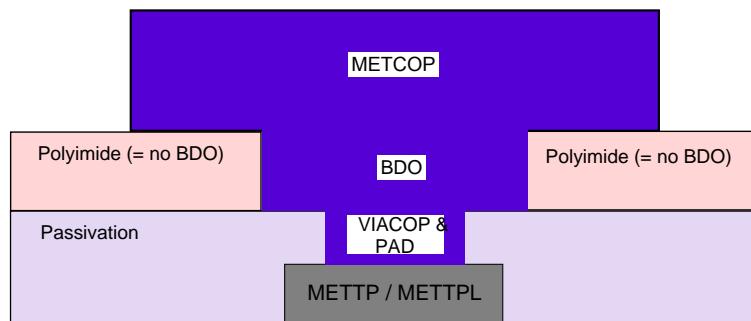
For existing layout, drawn PAD, no further changes.



For existing layout, drawn PAD, additionally drawn BDO & BDO\_VERIFY



For existing layout, drawn PAD, additionally drawn VIACOP, BDO & METCOP



**Figure 4.4** PAD with THKCOP, BDO module (cross sectional diagram)

4. Periphery rules → 4.2 Pad-type rules

## 4.2 Pad-type rules

**3 Metal METMID Bond Pad, 4 Metal METMID + METTHK Bond Pad, 4 Metal METMID Bond Pad, 5 Metal METMID + METTHK Bond Pad, 5 Metal METMID Bond Pad, 6 Metal METMID + METTHK Bond Pad, 6 Metal METMID Bond Pad, 4 Metal METTHK Bond Pad, 5 Metal METTHK Bond Pad, 6 Metal METTHK Bond Pad**

The bond pad stack is defined as follows:

Module	Bond Pad stack
LP5MOS/MOS5 and METMID	MET1 / VIA1 / MET2 / VIATP / METTP
LP5MOS/MOS5 and METMID and METTHK	MET1 / VIA1 / MET2 / VIATP / METTP / VIATPL / METTPL
MET3 and METMID	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIATP / METTP
MET3 and METTHK	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIATPL / METTPL
MET3 and METMID and METTHK	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIATP / METTP / VIATPL / METTPL
MET4 and METMID	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIA3 / MET4 / VIATP / METTP
MET4 and METTHK	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIA3 / MET4 / VIATPL / METTPL
MET4 and METMID and METTHK	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIA3 / MET4 / VIATP / METTP / VIATPL / METTPL
MET5 and METMID	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIA3 / MET4 / VIA4 / MET5 / VIATP / METTP
MET5 and METTHK	MET1 / VIA1 / MET2 / VIA2 / MET3 / VIA3 / MET4 / VIA4 / MET5 / VIATPL / METTPL

Name	Description	Value	Unit
B2PA	PAD overlap of DIFF, POLY1 or DTI is not allowed  <b>Note:</b> Not valid for DIFFDUMMY and P1DUMMY.	-	-
S2V1	Minimum VIA1 spacing  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	0.45	µm
S2V2	Minimum VIA2 spacing  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	0.45	µm
S2V3	Minimum VIA3 spacing  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	0.45	µm
S2V4	Minimum VIA4 spacing  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	0.45	µm
S1PADF	Minimum PAD spacing to DIFF  <b>Note:</b> Not valid for DIFFDUMMY.	5.0	µm
S1PADT	Minimum PAD spacing to DTI	2.0	µm
S1PAM1	Minimum PAD spacing to MET1 (different net)	5.0	µm
S1PAM2	Minimum PAD spacing to MET2 (different net)	5.0	µm
S1PAM3	Minimum PAD spacing to MET3 (different net)	5.0	µm
S1PAM4	Minimum PAD spacing to MET4 (different net)	5.0	µm
S1PAM5	Minimum PAD spacing to MET5 (different net)	5.0	µm
S1PAML	Minimum PAD spacing to METTPL (different net)	5.0	µm
S1PAMT	Minimum PAD spacing to METTP (different net)	5.0	µm
S1PAP1	Minimum PAD spacing to POLY1  <b>Note:</b> Not valid for P1DUMMY.	5.0	µm

⇒

## 4. Periphery rules → 4.2 Pad-type rules→ 3 Metal METMID Bond ...

Name	Description	Value	Unit
S1V2V1	Minimum VIA2 spacing to VIA1  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIA2 stacking over VIA1 is not allowed.	0.13	µm
S1V3V2	Minimum VIA3 spacing to VIA2  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIA3 stacking over VIA2 is not allowed.	0.13	µm
S1V4V3	Minimum VIA4 spacing to VIA3  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIA4 stacking over VIA3 is not allowed.	0.13	µm
S1VLV2	Minimum VIATPL spacing to VIA2  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIATPL stacking over VIA2 is not allowed  <b>Note:</b> Only valid if modules METTHK and MET3 are selected and not (MET4 and METMID)	0.06	µm
S1VLV3	Minimum VIATPL spacing to VIA3  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIATPL stacking over VIA3 is not allowed  <b>Note:</b> Only valid if modules METTHK and MET4 are selected and not (MET5 and METMID)	0.06	µm
S1VLV4	Minimum VIATPL spacing to VIA4  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIATPL stacking over VIA4 is not allowed  <b>Note:</b> Only valid if module METTHK and MET5 are selected	0.06	µm
S1VTV1	Minimum VIATP spacing to VIA1  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIATP stacking over VIA1 is not allowed  <b>Note:</b> Valid if MET3 module is not selected	0.06	µm
S1VTV2	Minimum VIATP spacing to VIA2  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIATP stacking over VIA2 is not allowed.  <b>Note:</b> Valid if MET3 is selected and MET4 module is not selected.	0.06	µm
S1VTV3	Minimum VIATP spacing to VIA3  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIATP stacking over VIA3 is not allowed.  <b>Note:</b> Valid if MET4 is selected and MET5 module is not selected.	0.06	µm
S1VTV4	Minimum VIATP spacing to VIA4  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> VIATP stacking over VIA4 is not allowed.  <b>Note:</b> Valid if MET5 module is selected.	0.06	µm
E1M1PA	Minimum MET1 enclosure of PAD	2.0	µm
E1M2PA	Minimum MET2 enclosure of PAD	2.0	µm
E1M3PA	Minimum MET3 enclosure of PAD	2.0	µm
E1M4PA	Minimum MET4 enclosure of PAD	2.0	µm
E1M5PA	Minimum MET5 enclosure of PAD	2.0	µm
E1MTPA	Minimum METTP enclosure of PAD	2.0	µm
E2MLVL	Minimum METTPL enclosure of VIATPL  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.  <b>Note:</b> Valid if module METTHK is selected	3.0	µm

## 4. Periphery rules → 4.2 Pad-type rules→ 3 Metal METMID Bond ...

Name	Description	Value	Unit
E2MTVL	Minimum METTP enclosure of VIATPL  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm. <b>Note:</b> Valid if module METMID is selected	3.0	µm
E2MTVT	Minimum METTP enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E3M1V1	Minimum MET1 and MET2 enclosure of VIA1  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E3M2V2	Minimum MET2 and MET3 enclosure of VIA2  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E3M2VT	Minimum MET2 enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm. <b>Note:</b> Valid if MET3 module is not selected	3.0	µm
E3M3V3	Minimum MET3 and MET4 enclosure of VIA3  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E3M3VL	Minimum MET3 enclosure of VIATPL  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm. <b>Note:</b> Only valid if modules METTHK and MET3 are selected and not (MET4 and METMID)	3.0	µm
E3M3VT	Minimum MET3 enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm. <b>Note:</b> Valid if MET3 is selected and MET4 module is not selected.	3.0	µm
E3M4V4	Minimum MET4 and MET5 enclosure of VIA4  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E3M4VL	Minimum MET4 enclosure of VIATPL  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm. <b>Note:</b> Only valid if modules METTHK and MET4 are selected and not (MET5 and METMID)	3.0	µm
E3M4VT	Minimum MET4 enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm. <b>Note:</b> Valid if MET4 is selected and MET5 module is not selected.	3.0	µm
E3M5VL	Minimum MET5 enclosure of VIATPL  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm. <b>Note:</b> Valid if modules METTHK and MET5 are selected	3.0	µm
E3M5VT	Minimum MET5 enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm. <b>Note:</b> Valid if MET5 module is selected.	3.0	µm
R1V1PA	Minimum ratio of VIA1 (in pad) area to PAD area	5.0	%
R1V2PA	Minimum ratio of VIA2 (in pad) area to PAD area	5.0	%
R1V3PA	Minimum ratio of VIA3 (in pad) area to PAD area	5.0	%
R1V4PA	Minimum ratio of VIA4 (in pad) area to PAD area	5.0	%
R1VLPA	Minimum ratio of VIATPL (in pad) area to PAD area	5.0	%
R1VTPA	Minimum ratio of VIATP (in pad) area to PAD area	5.0	%
Q1PA	Minimum recommended bond PAD width	53.0	µm

**Note:** The VIAs should form a diamond shape in the center of the PAD opening.

## 4. Periphery rules → 4.2 Pad-type rules→ 3 Metal METMID Bond ...

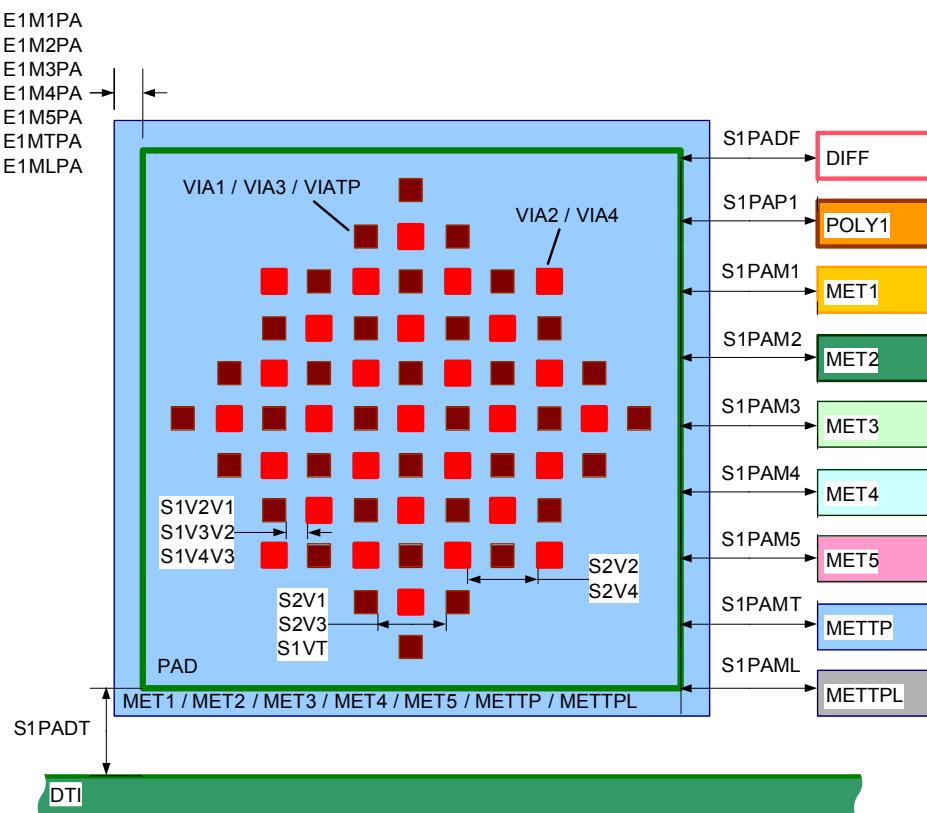


Figure 4.5 Bond Pad

4. Periphery rules → 4.2 Pad-type rules→ 4 Metal METMID + MET...

**4 Metal METMID + METTHK Circuit-Under-Pad Bond Pad, 4 Metal METMID Circuit-Under-Pad Bond Pad, 4 Metal METTHK Circuit-Under-Pad Bond Pad, 5 Metal METMID + METTHK Circuit-Under-Pad Bond Pad, 5 Metal METMID Circuit-Under-Pad Bond Pad, 5 Metal METTHK Circuit-Under-Pad Bond Pad, 6 Metal METMID + METTHK Circuit-Under-Pad Bond Pad, 6 Metal METMID Circuit-Under-Pad Bond Pad, 6 Metal METTHK Circuit-Under-Pad Bond Pad**

The following bond pad stacking for circuitry underneath bond pads applies when:

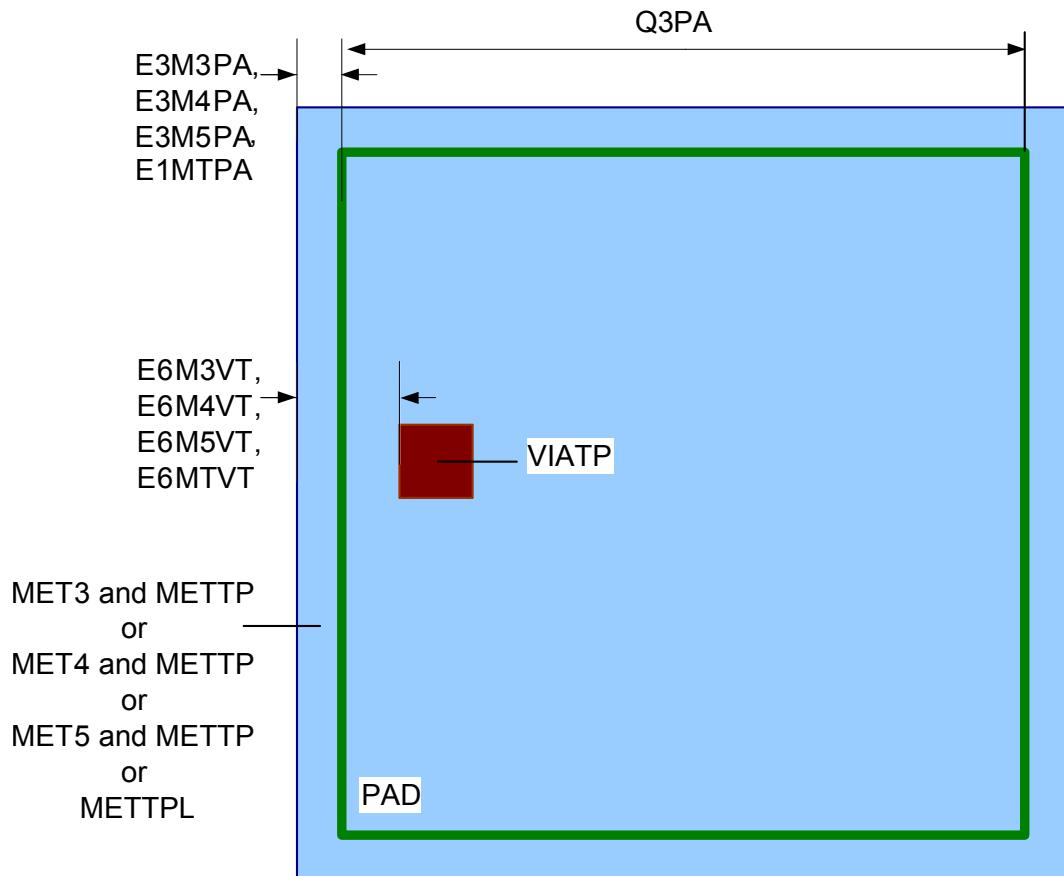
MET3 + METMID	MET3 / VIATP / METTP
MET4 + METMID	MET4 / VIATP / METTP
MET5 + METMID	MET5 / VIATP / METTP
METTHK	METTPL

**Note:** Rules are only appropriate to the modules which contain the relevant layers, as outlined above.

Name	Description	Value	Unit
B18PA	Circuit-Under-Pad Bond Pad is not available  <b>Note:</b> Only valid if module THKCOP is selected or if module METMID and module MET3 is not selected or module METTHK is not selected	-	-
E1MTPA	Minimum METTP enclosure of PAD	2.0	µm
E3M3PA	Minimum MET3 enclosure of PAD	2.0	µm
E3M4PA	Minimum MET4 enclosure of PAD	2.0	µm
E3M5PA	Minimum MET5 enclosure of PAD	2.0	µm
E6M3VT	Minimum MET3 enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E6M4VT	Minimum MET4 enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E6M5VT	Minimum MET5 enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
E6MTVT	Minimum METTP enclosure of VIATP  <b>Note:</b> VIA rules are related to all VIAs inside PAD regions extended by 2µm.	3.0	µm
R2VTPA	Minimum ratio of VIATP (in pad) area to PAD area	5.0	%
Q3PA	Minimum recommended PAD width	66.0	µm

**Note:** Circuit-Under-Pad bond pads allow non-critical circuitry underneath bond pads, as ESD structures or output drivers. For advice regarding the use of Circuit-Under-Pad bond pads within IC designs (regarding the handling of Circuit-Under-Pad bond pads during assembly etc) please refer to the [Application Note](#) available at "my X-FAB". Similarly, for reliability data for Circuit-Under-Pad bond pads please refer to the respective 'Bond Test Report'.

4. Periphery rules → 4.2 Pad-type rules→ 4 Metal METMID + MET...



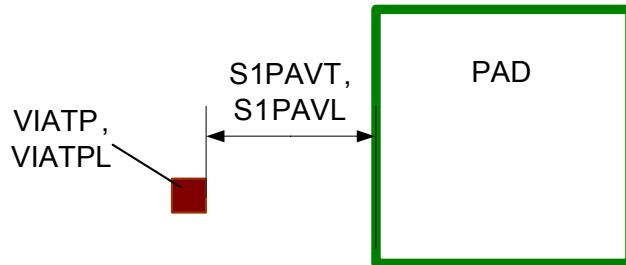
**Figure 4.6** Circuit Under Pad

4. Periphery rules → 4.2 Pad-type rules→ Probe Pad

### Probe Pad

Name	Description	Value	Unit
B15PA	Probe PAD with VIATPL is not allowed	-	-
	<b>Note:</b> Valid if METTHK module is selected.		
B3PA	Probe PAD with VIATP is not allowed	-	-
	<b>Note:</b> Valid if METTHK module is not selected.		
S1PAVL	Minimum PAD spacing to VIATPL	2.0	μm
	<b>Note:</b> Valid if METTHK module is selected.		
S1PAVT	Minimum PAD spacing to VIATP	2.0	μm
	<b>Note:</b> Valid if METTHK module is not selected.		

**Note:** The use of probe PAD is on responsibility of the customer.



**Figure 4.7** Probe Pad

4. Periphery rules → 4.3 Scribe rules

## 4.3 Scribe rules

Each single die is enclosed with a Peripheral Ring and a Scribe Lane.

**By default all the layout data within the peripheral ring is added by X-FAB at the mask tooling stage**, unless instruction is given in the SIFO document not to perform this task. In circumstances where the customer adds the peripheral ring by themselves, they should refer to the [Multi-Project Design Guide](#) available at "my X-FAB". This includes sample layout, a seal ring pcell and a dedicated technology file for use with the X-FAB Cadence design kit.

The final chip size is defined as follows:

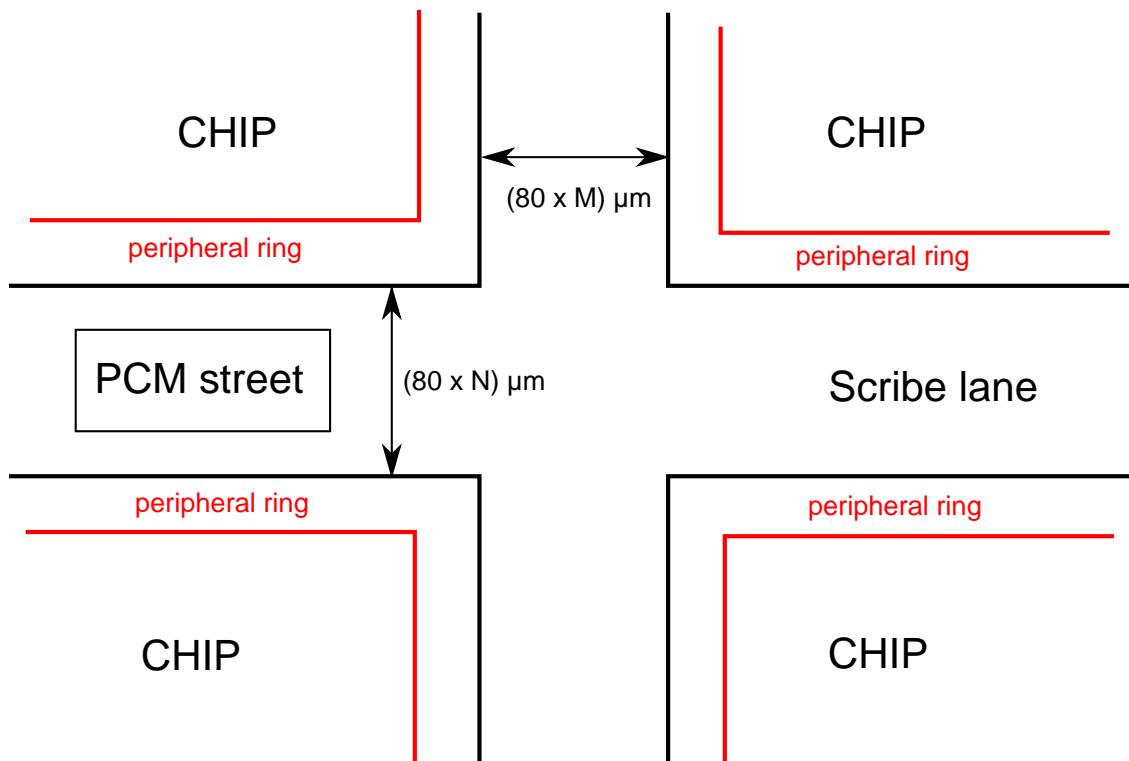
**final chip size = customer chip size + 2 x peripheral ring width + scribe lane width** , multiple of 1 $\mu$ m

### Peripheral Ring

This area contains the seal ring and a protective area without electrical structures. The peripheral ring width is defined as 15  $\mu$ m per side.

### Scribe Lane

This area contains all structures for controlling, alignment, measurement etc. The single scribe lane width is defined as default at 80  $\mu$ m, with minimum width at 60  $\mu$ m. Dependent on die size, used process family modules and reticle assembly, a multiple of scribe lane width can be necessary.



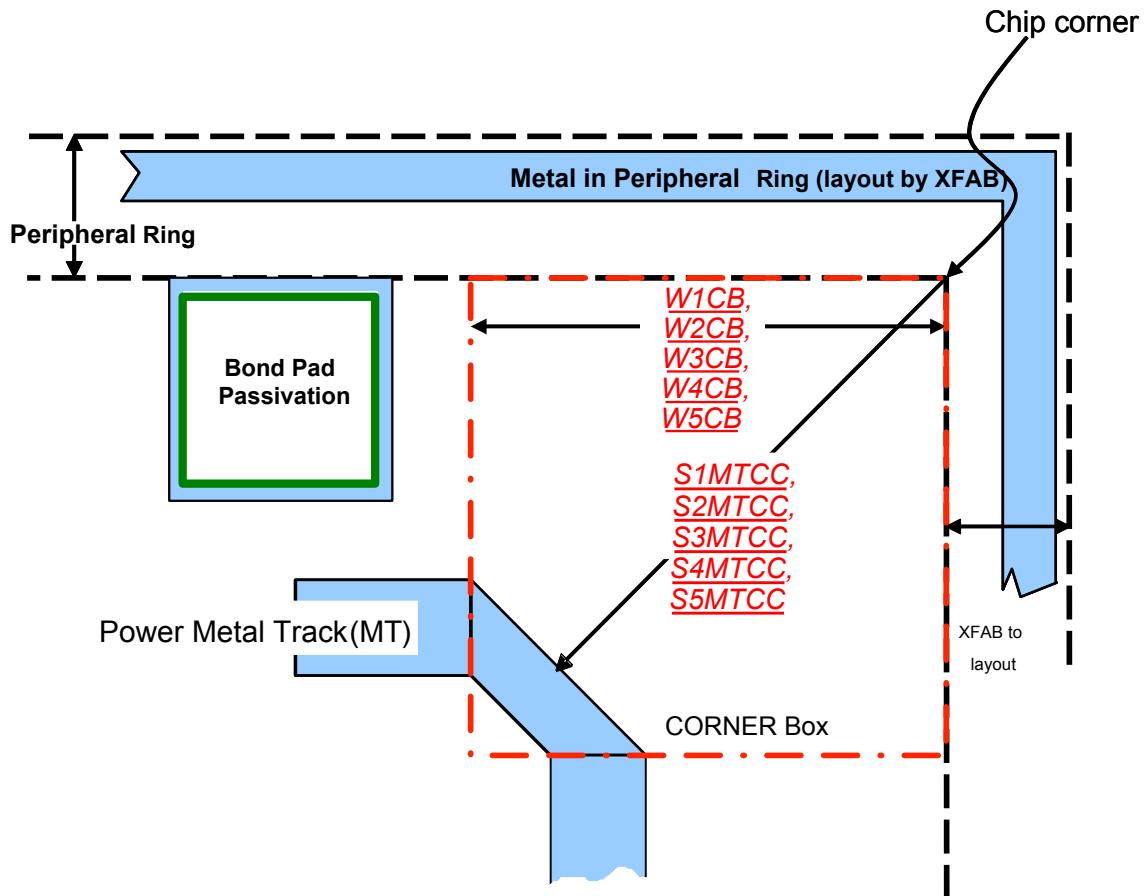
**Figure 4.8** final chip size

4. Periphery rules → 4.4 Corner rules

## 4.4 Corner rules

Name	Description	Value	Unit
<u>B1CB</u>	Active circuitry inside CORNER box is not allowed  <b>Note:</b> Only metal power rails and non-circuit structures, such as chip numbers, are allowed in this region.	-	-
<u>W1CB</u>	Minimum CORNER box edge length  <b>Note:</b> Valid for a very small chip (EXTENT area size < 1mm <sup>2</sup> ).	35.0	μm
<u>W2CB</u>	Minimum CORNER box edge length  <b>Note:</b> Valid for a small chip (1mm <sup>2</sup> <= EXTENT area size < 5mm <sup>2</sup> ).	40.0	μm
<u>W3CB</u>	Minimum CORNER box edge length  <b>Note:</b> Valid for a small chip (5mm <sup>2</sup> <= EXTENT area size < 10mm <sup>2</sup> ).	45.0	μm
<u>W4CB</u>	Minimum CORNER box edge length  <b>Note:</b> Valid for a small chip (10mm <sup>2</sup> <= EXTENT area size < 100mm <sup>2</sup> ).	75.0	μm
<u>W5CB</u>	Minimum CORNER box edge length  <b>Note:</b> Valid for a large chip (EXTENT area size >= 100mm <sup>2</sup> ).	150.0	μm
<u>S1MTCC</u>	Minimum metal track spacing to chip corner  <b>Note:</b> Valid for a very small chip (EXTENT area size < 1mm <sup>2</sup> ).	35.0	μm
<u>S2MTCC</u>	Minimum metal track spacing to chip corner  <b>Note:</b> Valid for a small chip (1mm <sup>2</sup> <= EXTENT area size < 5mm <sup>2</sup> ).	40.0	μm
<u>S3MTCC</u>	Minimum metal track spacing to chip corner  <b>Note:</b> Valid for a small chip (5mm <sup>2</sup> <= EXTENT area size < 10mm <sup>2</sup> ).	45.0	μm
<u>S4MTCC</u>	Minimum metal track spacing to chip corner  <b>Note:</b> Valid for a small chip (10mm <sup>2</sup> <= EXTENT area size < 100mm <sup>2</sup> ).	75.0	μm
<u>S5MTCC</u>	Minimum metal track spacing to chip corner  <b>Note:</b> Valid for a large chip (EXTENT area size >= 100mm <sup>2</sup> ).	150.0	μm

## 4. Periphery rules → 4.4 Corner rules



**Figure 4.9** Corner Rules

## 5. Design related guidelines

## 5. Design related guidelines

### 5.1 Miscellaneous

It is generally good practice to ensure that as many taps as possible exist on the design, in order to minimize resistive effects on the circuit. Unless used as an active node, all wells must be connected to a power rail using a TAP connection.

For precision analogue devices, it is recommended to use non-minimum geometries. Such devices should not be covered with metal. If this is not possible, metal coverage of matching devices should be identical.

For MIM devices stacked to subjacent primitive devices, it is recommended not to use the MIM device or the subjacent primitive devices as precision analogue devices.

The use of redundant contacts and redundant vias is recommended wherever it is possible in the design. Redundant via placement is supported by special functionality within the design kit.

It is strongly recommended to use MET2 or higher metal layers for high-voltage connection instead of MET1.

"my X-FAB" hosts further documentation on this process that may assist the reader in understanding and designing on it. Two documents identified as being of particular interest in helping to understand this capability are:

- [XT018 Application Note Layout Techniques](#)
- [XT018 1.8V & 5V MOS ESD Protection Device and Latch-up Guidelines](#)

5. Design related guidelines → 5.2 Antenna Rule definitions

## 5.2 Antenna Rule definitions

The definition of antenna ratio is given by the following equation:

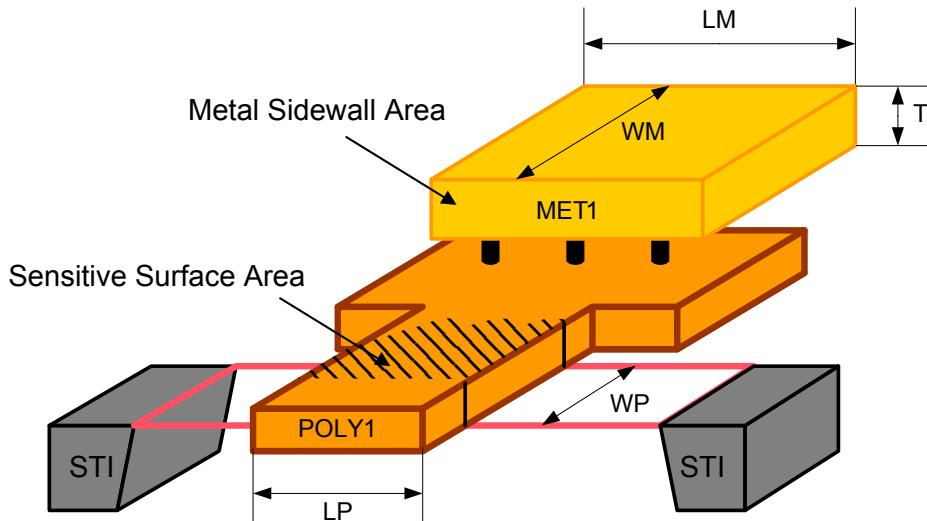
$$Rx = \frac{P \times T}{WP \times LP} = \frac{\text{Metal Sidewall Area}}{\text{Sensitive Surface Area}}$$

Metal Sidewall Area Terms:

- P = floating metal perimeter connected to gate ( $\mu\text{m}$ )
- WM = the width of metal ( $\mu\text{m}$ )
- LM = the length of metal ( $\mu\text{m}$ )
- T = the thickness of metal ( $\mu\text{m}$ )

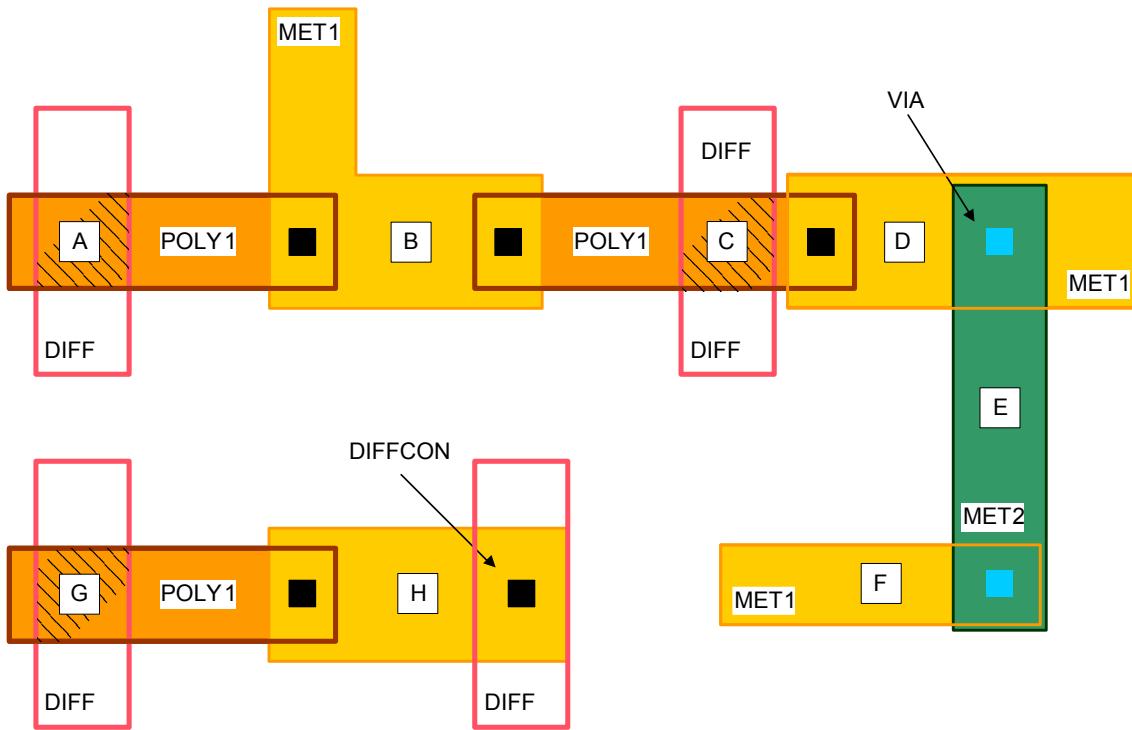
Sensitive Surface Area Terms:

- WP = connected transistor channel width ( $\mu\text{m}$ )
- LP = connected transistor channel length ( $\mu\text{m}$ )



**Figure 5.1** Antenna ratio definition (example for MET1)

## 5. Design related guidelines → 5.2 Antenna Rule definitions

**Figure 5.2** Contributing areas for antenna effects (example for MET1)Antenna ratios:

$$\frac{\text{area}(B + D)}{\text{area}(A + C)}$$

$$\frac{\text{area}(E)}{\text{area}(A + C)}$$

**Note:** Areas 'F' and 'H' do not contribute to antenna effects.

**Note:** Metal structures collect electric charge during ion-etching which can be a hazard for associated GATEs. Only metal areas without DIFFCONs must be considered.

MET1 areas connected to GATE via MET2 do not contribute. The similar approach applies to all the metal layers.

Please also refer to the "[Application Note MIM Capacitors](#)" available at "my X-FAB."

## 5. Design related guidelines → 5.3 NLEAK

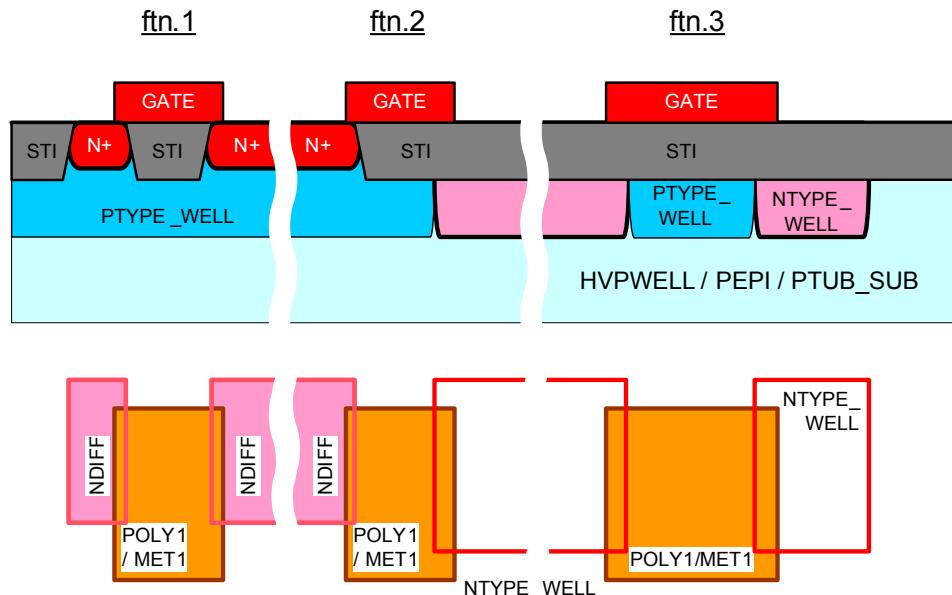
**5.3 NLEAK**

Inversion will occur and a parasitic NLEAK channel will be formed if laterally positioned N-P-N areas are crossed by POLY1 or MET1 over STI and the voltage difference between these crossing lines and the interposed P-area exceeds the corresponding field threshold voltage for that combination. P-area is defined as PTUB\_SUB, PEPI or PTYPE\_WELL.

**Notes:**

- For further information, please refer to the appropriate "Parasitic Field Parameters" within the Process & Device Specification, or search for 'VTF' parameters in the SpecXplorer.
- Both the case of complete and partial overlap of these P-doped regions by a POLY1 or MET1 line should be considered.
- NLEAK channels can connect NDIFF and NTYPE\_WELL in any combination.
- NLEAK channels cannot be found automatically with verification tools.

The associated NLEAK channels of such transistors can create unwanted electrical connections between two or more unrelated structures. Without loss of generality the following NLEAK constellations are possible with the XT018 layers. They are given as examples in cross sectional and plan view below. The gate may consist of POLY1 or MET1.



**Figure 5.3** NLEAK field transistor configurations

Implementing leakage suppression regions

Continuous NLEAK channels can be blocked by either inserting:

- P-areas with higher field threshold voltages;
- PDIFF
- POLY1 (connected to the P-area, unless said area is PSUB in which case this will not work)
- Note that these activities are not allowed for predefined device layouts

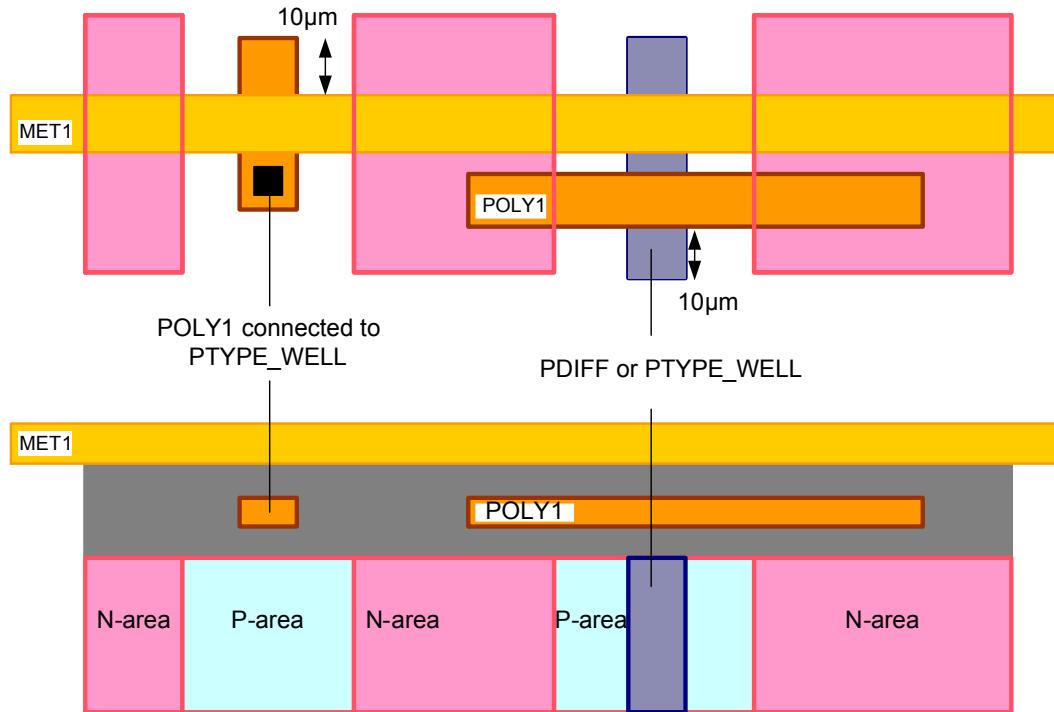
whenever possible.

When considering the size of the blocking regions the critical dimension is the extension beyond the offending polysilicon or metal lines. These dimensions are required in order to avoid the creation of continuous NLEAK channels (see diagram below):

Minimum PTYPE\_WELL, PDIFF or POLY1 extension beyond POLY1 or MET1 is 10.0 µm



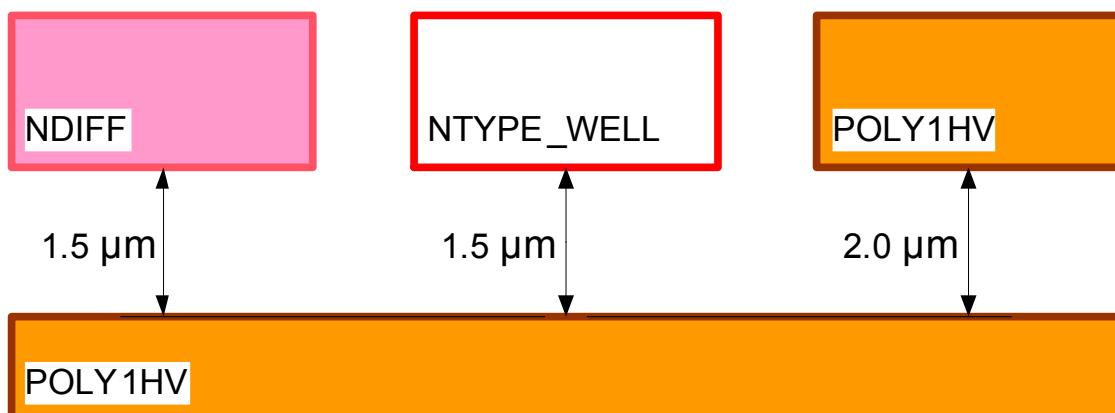
## 5. Design related guidelines → 5.3 NLEAK

**Figure 5.4** Suppression of NLEAK channels

**Note:** This diagram is only a conceptual illustration of method of suppressing field leakage. It might not reflect the actual device construction.

In addition to the cases described above, continuous NLEAK channels may already be formed if there is insufficient clearance between corresponding N-type regions and a polysilicon or metal line exceeding the respective field threshold voltage for the given well or well combination.

In the case of transistors, NLEAK channels can extend beyond these lines and appear larger than the parasitic gate, such that P-area leakage can occur even if the parasitic gate only approaches it.

**Figure 5.5** NLEAK related layer spacings

Minimum POLY1HV spacing to NDIFF over PTYPE\_WELL is 1.50  $\mu\text{m}$

Minimum POLY1HV spacing to NTYPE\_WELL is 1.50  $\mu\text{m}$

Minimum spacing between POLY1HV is 2.00  $\mu\text{m}$

**Note:** It is strongly recommended to use MET1 or MET2 for >5V routing purpose, instead of POLY1.

**Note:** Routing over PWBLK should be limited due to the low field VT.

## 5. Design related guidelines → 5.4 PLEAK

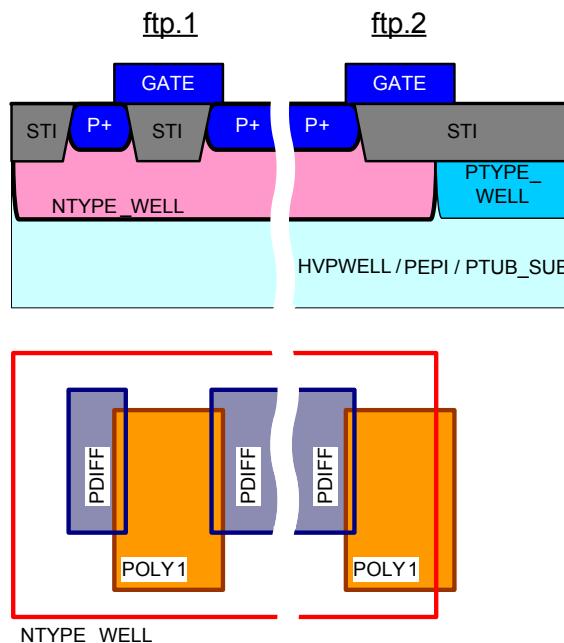
**5.4 PLEAK**

Inversion will occur and a parasitic PLEAK channel will be formed if laterally positioned P-N-P areas are crossed by POLY1 or MET1 over STI and the voltage difference between these crossing lines and the interposed N-area exceeds the corresponding field threshold voltage for that combination. N-area is defined as NTYPE\_WELL.

**Notes:**

- For further information, please refer to the appropriate "Parasitic Field Parameters" within the Process & Device Specification, or search for 'VTF' parameters in the SpecXplorer.
- Both the case of complete and partial overlap of these NTYPE\_WELL regions by a POLY1 or MET1 line should be considered.
- PLEAK channels can connect PDIFF and PTYPE\_WELL in any combination.
- PLEAK channels cannot be found automatically with verification tools.

The associated PLEAK channels of such transistors can create unwanted electrical connections between two or more unrelated structures. Without loss of generality the following PLEAK constellations are possible with the XT018 layers. They are given as examples in cross sectional and plan view below. The gate may consist of POLY1 or MET1.



**Figure 5.6** PLEAK field transistor configurations

Implementing leakage suppression regions

Continuous PLEAK channels can be blocked by either inserting:

- N-areas with higher field threshold voltages;
- NDIFF
- POLY1 (connected to the N-area)
- Note that these activities are not allowed for predefined device layouts

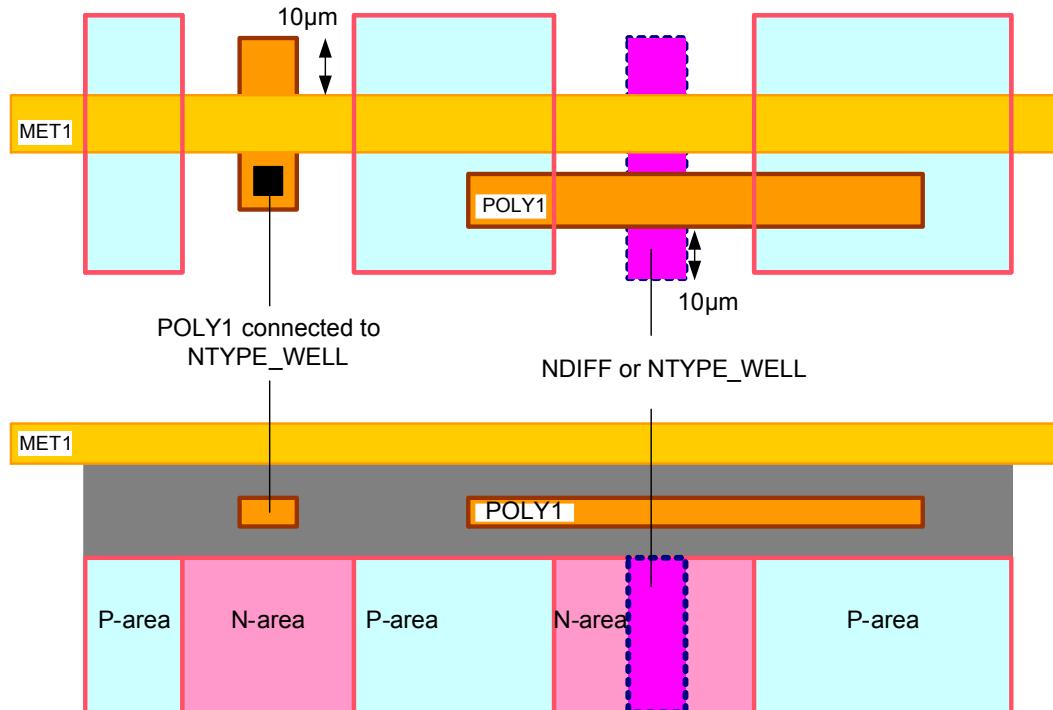
whenever possible.

When considering the size of the blocking regions the critical dimension is the extension beyond the offending polysilicon or metal lines. These dimensions are required in order to avoid the creation of continuous PLEAK channels (see diagram below):

Minimum NTYPE\_WELL, NDIFF or POLY1 extension beyond POLY1 or MET1 is 10.0 µm



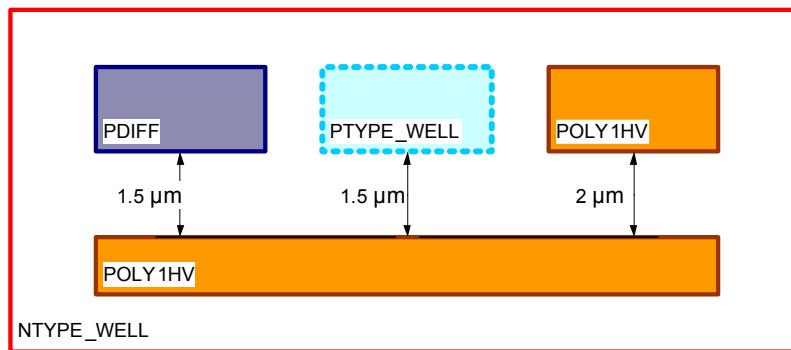
## 5. Design related guidelines → 5.4 PLEAK

**Figure 5.7** Suppression of PLEAK channels

Note: This diagram is only a conceptual illustration of method of suppressing field leakage. It might not reflect the actual device construction.

In addition to the cases described above, continuous PLEAK channels may already be formed if there is insufficient clearance between corresponding P-type regions and a polysilicon or metal line exceeding the respective field threshold voltage for the given well or well combination.

In the case of transistors, PLEAK channels can extend beyond these lines and appear larger than the parasitic gate, such that N-area leakage can occur even if the parasitic gate only approaches it.

**Figure 5.8** PLEAK related layer spacings

Minimum POLY1HV spacing to PDIFF over NTYPE\_WELL is 1.50 µm

Minimum POLY1HV spacing to PTYPE\_WELL over NTYPE\_WELL is 1.50 µm

Minimum spacing between POLY1HV is 2.00 µm

**Note:** It is strongly recommended to use MET1 or MET2 for >5V routing purpose, instead of POLY1.

**Note:** Routing over PWBLK should be limited due to the low field VT.

5. Design related guidelines → 5.5 Dummy Pattern Generation

## 5.5 Dummy Pattern Generation

Dummy pattern generation is necessary to ensure robust manufacturing and achieve better yields in lower geometry node such as 0.18µm technology.

Some advantages of dummy pattern insertion are listed below.

### 1. Better control of electrical parameters such as well resistance and breakdown voltage.

The 0.18µm technology node uses a Shallow Trench Isolation (STI) scheme to isolate primitive devices. STI uses Chemical Mechanical Polishing (CMP) to planarise the oxide which fills the trenches. If the active area pattern is non-uniform, over-polishing occurs ('dishing'), reducing the thickness of oxide in the trenches. Since well implants are performed through the trenches, electrical parameters like resistance and breakdown voltage can vary with the local pattern density. This is especially significant for high voltage devices. The addition of dummy pattern eliminates this problem.

### 2. Better CD and sidewall profile control.

Etch processes typically exhibit 'loading effects', where the etch rate depends on the pattern density. To achieve good critical dimension (CD) control and correct control of sidewall profiles, a uniform pattern density is necessary. This is achieved through the addition of dummy pattern. It is especially critical for poly and metal layers.

### 3. Better control of contact/via resistance and interlayer capacitance.

For metal layers, the dummy pattern generation reduces the thickness variation in the next dielectric layer (less dishing) which improves CD control for subsequent photolithography stages. A more uniform dielectric stack helps to reduce the variation in contact and via depth and results in smaller contact and via resistance variation and less variation in interlayer capacitance values.

Dummy fill insertion is applied in vacant layout spaces after the layout density scan using a design rule based script. The script identifies the vacant spaces and fills them with auto generated active/poly/metal dummies (purpose DUMMY) to equalise the pattern density as much as possible. Script based analysis is done to determine the regions of the layout violating density rules and the amount of dummy fill required in each region.

These auto generated dummy fill patterns/features are electrically isolated from the original layout.

The dummy layer generation is done for the following layers:

DIFF, POLY1, MET1, MET2, MET3, MET4, MET5, METTP, METTPL

The auto-generated dummy pattern sizes are summarised below:

Dummy Layer Name	Size (µm x µm)
DIFFDUMMY	0.4 x 3 (Donut shape)
P1DUMMY	1.4 x 1.4
M1DUMMY	5 x 2
M2DUMMY	5 x 2
M3DUMMY	5 x 2
M4DUMMY	5 x 2
M5DUMMY	5 x 2
MTPDUMMY	2 x 4
MTPLDUMMY	7 x 5

The dummy pattern is generated by a software routine. It uses dummy blocking layers to define regions that must not have pattern fill added. In the Design Layers section of this document, the purpose of the dummy blocking layers is defined as "DMYBLK" as summarised below:

Layer	Design Layer	Remarks
DIFF, POLY	POLY1: DMYBLK	blocks DIFF and POLY1 dummy generation
MET1	MET1: DMYBLK	
MET2	MET2: DMYBLK	



## 5. Design related guidelines → 5.5 Dummy Pattern Generation

METTP	METTP: DMYBLK	
MET3	MET3: DMYBLK	
MET4	MET4: DMYBLK	
MET5	MET5: DMYBLK	
METTPL	METTPL:DMYBLK	
BLKALL	BLKALL: DMYBLK	blocks all dummy generation

### Important notes:

**Dummy blocking layers should be used only on critical elements and not to block the entire layout.**

Excessive use of dummy blocking layers might result in unsuitable design for manufacturing which could lead to poor performance with respect to inline defects and yield.

Note that the layer BLKALL removes ALL dummy fills; this is an unwanted by-product for the designer in many cases.

Dummy blocking areas can be used to prevent dummy pattern generation nearby or underneath sensitive circuit elements (e.g. to avoid additional parasitic capacitance).

**It is strongly recommended that the dummy blocking areas should only be used for the critical circuit elements.**

The dummy pattern generation script does not guarantee that the minimum and maximum structure densities of the related layer are met. Please refer to rules R1DF, R1P1, R1M1, R2M1, R1M2, R2M2, R1M3, R2M3, R1M4, R2M4, R1M5, R2M5, R1MT, R2MT, R1ML, R2ML. These rules will be checked by X-FAB after IP replacement and dummy pattern generation.

It is recommended to use X-FAB's dummy pattern generation option (DUMMY\_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules (DIFFDUMMY, P1DUMMY, M1DUMMY, M2DUMMY, M3DUMMY, M4DUMMY, M5DUMMY, MTPDUMMY and MTPLDUMMY).

5. Design related guidelines → 5.6 Voltage class definitions

## 5.6 Voltage class definitions

With voltage class definitions, X-FAB offers a methodology for the voltage level information transfer between design and layout. The definition of tag devices (virtual devices which do not exist in silicon) allows an LVS check for coincidence and a DRC of the spacing rules for different voltage classes.

By using tag devices which assign a net to a specified voltage class, the correct and complete implementation from schematics to layout can be checked. For that purpose, the tag device symbol is placed to the net at schematics. At the layout, the voltage classification of the net is done by adding the tag device layout (label) to the shape.

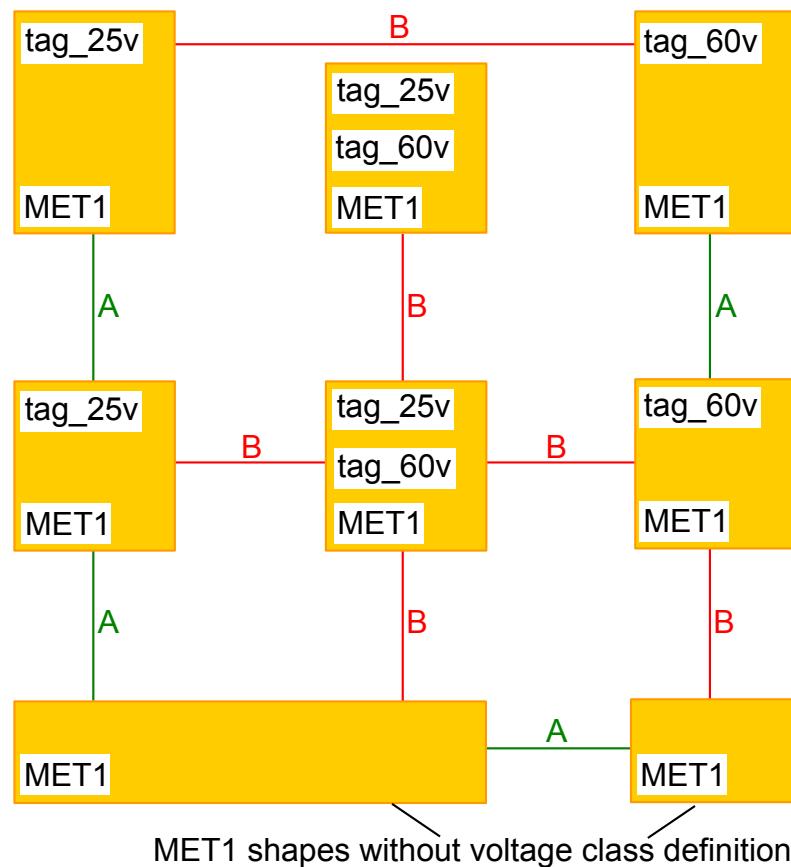
The primitive device list shows which voltage classes and therefore which tag devices are defined for the process family.

The voltage of the net can vary within a wider range than defined by one voltage class. In such cases, one net can be part of several voltage classes and therefore several tag devices can coexist on the same net.

Between shapes without any tag labels, the basic spacing rules are valid.

Between shapes assigned to different voltage classes, different spacing might be required.

The following drawing illustrates the system used for voltage dependent spacing rules. Here the example with the voltage classes tag\_25v and tag\_60v is shown for layer MET1 (not wide metal):



A: S1M1 is valid

B: S1M1 and S4M1 are valid

**Figure 5.9** Voltage class

The resistor rules (for example Q1M1 in case of metal1 resistor) are warnings for thinking about the correct voltage class definition at both resistor terminals.

A resistor splits the net. If the resistor is assigned to a net having a voltage class then this voltage class is only assigned to one resistor terminal and the net ends. The other resistor terminal net requires an additional voltage class definition. The resistor body is always part of both resistor terminal nets.

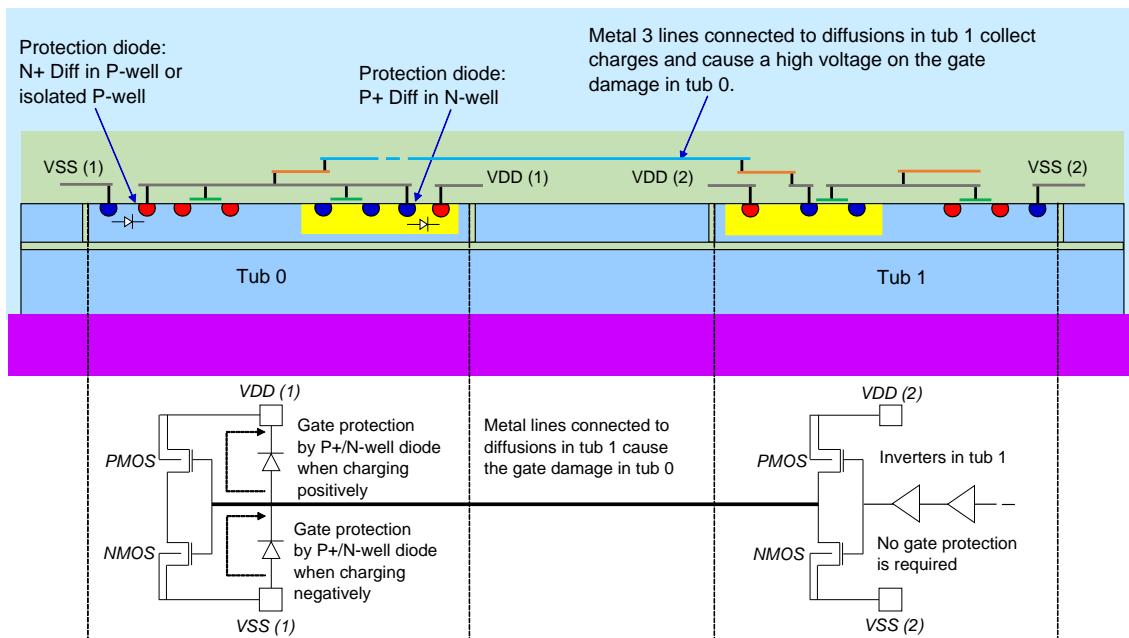
## 5. Design related guidelines → 5.7 Strategies for Avoiding Plasma Induced Damage (PID) Risks

## 5.7 Strategies for Avoiding Plasma Induced Damage (PID) Risks

### 1. PID Protection Diodes

Protection diodes are used in an SOI process just as they are used in a bulk silicon process. There is one additional restriction to their use in SOI processes; the diode has to be placed such that it connects the gate antenna network to the tub antenna network for the tub containing the transistor. In most cases, a simple N+/P-well or P+/N-well diode can be used for this protection diode. It is also possible to place the protection diode in the tub that is connected to the drain of a high voltage transistor. However, if the transistor being protected is a high voltage transistor, a high voltage diode is usually required, due to the voltage range difference between the gate and drain of a high voltage transistor.

Figure 5.10 shows a practical example of the proper use of protection diodes to protect the gate of a transistor connected to the diffusion in another tub. This example is a case of using a Metal 3 line when the output of the inverter circuit of tub 1 is connected to the input of the inverter circuit of tub 0. As the Metal 3 line connects the diffusion of tub 1 and the poly gate of tub 0, the charge accumulated in tub 1 can affect the gate damage of the tub 0 inverter circuit. To protect the poly gate of tub 0, it is recommended to use appropriate protection diodes at the top and bottom of the poly gate as shown in figure 5.10. These protection diodes are effective in preventing the gate damage of tub 0 caused by the discharging of plasma-induced current proportional to the amount of charge collected positively or negatively in tub 1.

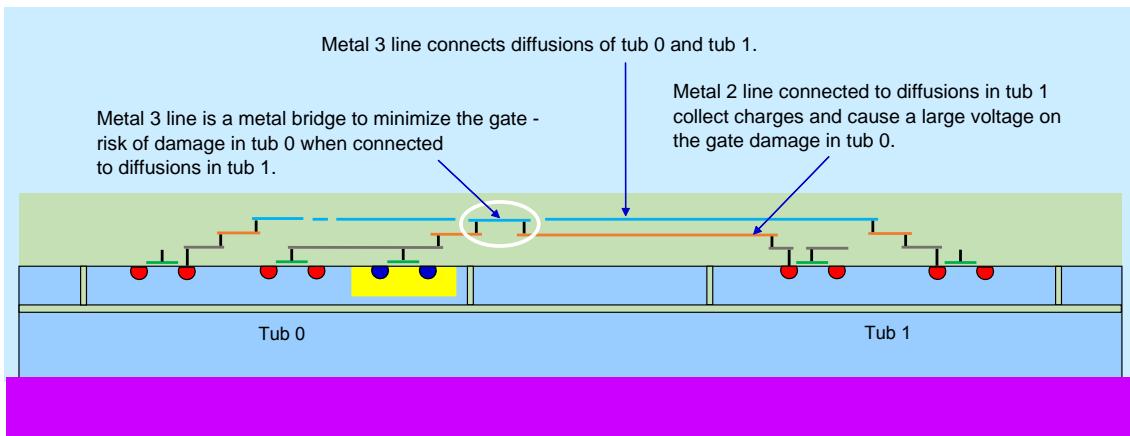


**Figure 5.10** PID protection diodes for a poly gate connected to diffusions in another tub

### 2. Late Gate Connection

The other main method of protecting devices from PID is to try to connect the gate of the device as late as possible in the process flow. Figure 5.11 shows a practical example of the proper use of metal bridges to protect the poly gate of a transistor connected to the diffusion in another tub. In this example, when the diffusion of tub 1 and the poly gate of tub 0 are connected to the Metal 2 line, the charge accumulated in tub 1 can cause gate damage of tub 0. As shown in figure 5.11, if tub 0 and tub 1 are connected by a Metal 3 line somewhere, it is recommended to use the same metal layer for metal bridge (also known as "jumper") as the most effective way to prevent the poly gate in tub 0 from PID.

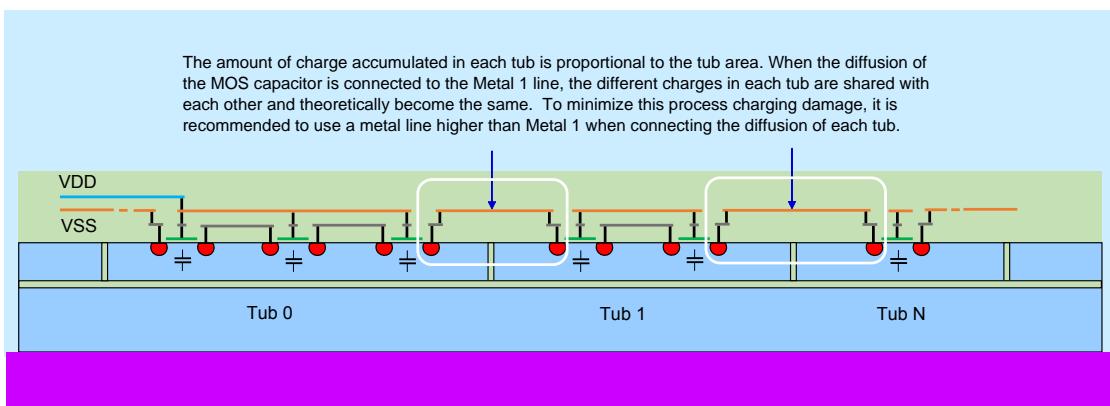
## 5. Design related guidelines → 5.7 Strategies for Avoiding Plasma Induced Damage (PID) Risks

**Figure 5.11** Use of a metal bridge to prevent PID**3. Capacitors**

Capacitors, like MOS and varactor devices consist of two conductive layers separated by a usually thin dielectric layer.

The situation for capacitors in an SOI process is not much different than the situation in a bulk silicon process. As a result, they are also subject to PID.

Figure 5.12 shows a practical example of the proper use of MOS capacitors in SOI processes. This example is a case where the diffusions of each tub are bound by a metal 1 line in order to use the MOS capacitors of each tub as decoupling or bypass capacitors. The amount of charge accumulated in each tub is proportional to the tub area and when the diffusions of each tub are connected to the metal 1 line, the different charge of each tub is shared and theoretically equal. This charge sharing can cause a high voltage difference between the poly gate and the diffusion, leading to gate damage in the connected MOS capacitor. To minimize the process-induced charging damage, it is recommended to use a metal line higher than the metal 1 layer for connecting the diffusion in each tub. Figure 5.12 shows the connection of each diffusion using the metal 2 line to minimize the risk. **In order to minimize the amount of charge accumulated in each tub, it is also recommended to make the area of each tub containing decoupling or bypass capacitor array as small as possible and limit the size of a single tub to a maximum of  $30,000\mu\text{m}^2$  for the capacitor array design.**

**Figure 5.12** Use of MOS capacitors in SOI process

Please also refer to the "Differential Antenna PID in SOI Processes" available at "my X-FAB."

The information furnished herein by X-FAB Global Services GmbH (X-FAB) is substantially correct and accurate. However, X-FAB shall not be liable to licensee or any third party for any damages, including but not limited to property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data. No obligation or liability to licensee or any third party shall arise or flow out of X-FAB rendering technical or other services.

X-FAB makes no warranty, express, implied, statutory, or descriptive of the information contained herein or of warranties of merchantability, fitness for a particular purpose, or non-infringement. X-FAB reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with X-FAB for current information. The products listed herein are intended for use in standard commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by X-FAB for each application.