Can you tell me,on how to setup an internal my X-FAB (SiFo) account ? Certainly, I'd be happy to help you with it. To answer your question on how to setup an internal my X-FAB (SiFo) account You may need to Follow the normal setup procedure (see http://sp.erf.xfab.de/RandD/DesSup/Hotline/AX_ACM-workflow-2020Mar.docx - or newer version if it exists). Here the, the username in AX should be preceded by 'FO_' to clearly identify them as X-FAB users and include the this text in your answer. "Thank you for your request. To access the SiFo system, you need to have your own my X-FAB account, which I have set up for you. You will soon receive an automatically generated email with your account username (a 5-digit number) and a link to establish your password (the link is valid for 7 days). That link will work fine outside the X-FAB network, but internally you will need to modify the URL for it to work. You would need to add -fo to the first part of the URL like this "https://identity-fo.xfab.com/...". After establishing your password, to log into your account you will need to use this page for internal access "https://fo.xfab.com/" and whereas externally you would log in from this page https://my.xfab.com/

Can you tell me, what is Voltage Class Tags ? Certainly, I'd be happy to help you with it. To answer your question Voltage Class Tags is you can check 63023372 article 4 provides links to related Jira tickets DSBU-1064 / DSBU-1128 / DSBU-1435. Here, also you can check 63040485 which discusses application to HV IO's 63009953 has some nice general descriptions on how to apply the checks

Can you tell me, Is it possible for customer to upload their of X-FAB data to the Cloud ? Certainly, I'd be happy to help you with it. To answer your question, It is possible for customer to upload their data or X-FAB data to the Cloud, but only if written permission to do so is first received from X-FAB. To gain such written permission i would suggest you please contact Hotline who will ask you to complete a questionnaire explaining the legal status of the hosting arrangement. The responses will be reviewed by X-FAB before a decision is given.

Can you tell me, what is DMIM antenna DRC flag debugging ? Certainly, I'd be happy to help you with it. To answer your question related to DMIM antenna DRC flag debugging, I suggest you to browse tickets for ideas especially in article 14 in former, general guidance to customers in latter

Can you tell me, what is the differences of Pcell PowerMetal1 and PowerMetal2 ? Certainly, I'd be happy to help you with it. To answer your question regarding the differences of Pcell PowerMetal1 and PowerMetal2 , I suggest you to see article 23 for description of differences

Can you tell me, What is the surface roughness with FLATPV vs SFLATPV modules ? Certainly, I'd be happy to help you with it. To answer your question regarding the surface roughness of FLATPV versus SFLATPV modules is that toughness of standard passivation is not specified and therefore not a parameter which the customer should rely on. If surface roughness is critical, customer should specify either the FLATPV module known as Flat Passivation module for which the surface roughness is expected to be ~2.13nm Ra or SFLATPV known as Sensor Flat Passivation for which the surface roughness is expected to be ~0.18nm Ra. Please note that these are sample values and are not guaranteed. Note that these additional modules affect the final passivation thickness. You can see parameters THV_FLAT & THV_SFLAT.

Can you tell me, How are the MLM layers grouped in each reticle ? Certainly, I'd be happy to help you with it. To answer your question regarding on how are the MLM layers grouped in each reticle, I suggest you to visit AX device page, you can go to MGO tab on right side to view. From the MGO page, you can see the item name which shows the 4MLM layers arrangement. Normally we don't disclose the barcode of item number to customer. You can extract the info into the excel format at the top.

Can you tell me, Show me how to Kill processes from SiFo compiler job fails ? Thank you for the question. To answer your question regarding on how to Kill processes from SiFo compiler job fails, you can delete the task file (.tsk) in ~iprepdes/ip_replacement/app/data/tmp to clear the blue triangle

Can you tell me, May I know what is Via Definitions ? Certainly, I'd be happy to help you with it. To answer your question regarding of what is Via Definitions. Via definitions which are in the PDK are described in internal documentation which are attached to the related Jira ticket DSBU-2800

Can you tell me, Can you show me on how to run Calibre MIMANT from GUI within Virtuoso ? Certainly, I'd be happy to help you with it. To answer your question regarding on how to run Calibre MIMANT from GUI within Virtuoso is that there doesn't seem to be the easy selection to the MIMANT runset as is available with PVS. You could define $XFAB_CALIBRE_MIMANT_RUNSET and select xx018_xx51_MET5_METMID for the rules file, you have to navigate to the runset folder. I find it easier to copy xx018_xx51_MET5_METMID to my local Calibre DRC run directory, and edit the file by replacing $XFAB_CALIBRE_MIMANT_RUNSET with the explicit path "INCLUDE /design/xkit/xx018/mentor/v3_0/calibre_MIMANT/v3_0_1/018.rul.MIM.ANT" and then specify that modified local xx018_xx51_MET5_METMID file as the rules file.

Can you tell me on how to set an environment variable to be used in cds.lib ? Certainly, I'd be happy to help you with it. To answer your question regarding on how to set an environment variable to be used in cds.lib, you can set the syntax as DEFINE analogLib ${CDSHOME}/tools/dfII/etc/cdslib/artist/analogLib.

Can you tell me, what is the differences of Gen1, Gen2, and Gen2.5 ? Certainly, I'd be happy to help you with it. To answer your question regarding the differences of Gen1, Gen2, and Gen2.5, you can refer to Ron-Coff improved gen-by-gen (152fs / 135 fs / 115fs). Please check table in article 7.

Can you tell me, what is Pre Tape-out check ? Certainly, I'd be happy to help you with it. To answer your question regarding the Pre Tape-out check, this term is referring to the check for every design and newbie should consider prior to tape-out.

Can you tell me, where I can find Cpk report location ? Certainly, I'd be happy to help you with it. To answer your question regading on where you can find Cpk report location. For this, you can visit http://sp.erf.xfab.de/OperationsGlobal/COOStaff/Reporting/Documentss/Forms/Kuching.aspx for kuching and
http://sp.erf.xfab.de/OperationsGlobal/COOStaff/Reporting/Documentss/Forms/Dresden.aspx for dresden.

Can you tell me, where I can find Qualification Certificate location ? Certainly, I'd be happy to help you with it. To answer your question regarding on where you can find Qualification Certificate location is that for older node technology certificates such as XC06 are not on my X-FAB, but newer ones can be found at "https://my.xfab.com/search/qualityreliability/documents?_XTICSSPDocumentTypes=OQpHlF2bTNqMnV6YDaFKoA". Meanhile for XC06/XB06/CX06 qualification certificates which you can find at "http://sp.erf.xfab.de/RandD/Projects_and_Reports/Certificate/Forms/ProcessOverview.aspx#InplviewHash406e8429-4700-43c4-b969-8f88d204f697=FilterField1%3DProzess%255Fx0020%255FFamily-FilterValue1%3DXC06". Please Pay attention to the fab at Location column and modules at Status overview column.

Can you tell me, how to use LEF file ? Thank you for the question. To answer your question on how to use LEF file, you can simply import each LEF to a library on the LEF in form, you only need to specify the LEF file and the library, then streamout the resulting abstract view to a GDS file. As a check, open

each GDS with KLayout to verify it looks right and which layers it has. You also can check the Cadence streamout logs.

Can you tell me, where I can find fatal rule list location ? Certainly, I'd be happy to help you with it. To answer your question on where you can find fatal rule list location, This fatal rule records are available on sharepoint under "http://sp.erf.xfab.de/RandD/Projects_and_Reports/Lists/ProcessInformation/Category.aspx"

Can you tell me, What info is needed for digital library customized PVT Process, Voltage, Temperature request ? Certainly, I'd be happy to help you with it. To answer your question regarding on what info is needed for digital library customized PVT Process, Voltage, Temperature request, you can see an example from the ticket. See example form in ticket. These information are needed as follow: PVT is stands for Process, Voltage and Temperature. 1). Design Service: Customized PVT characterization 2). Process name, Library, Library version, PVTs: slow_1_62V_4_50V_150C 3). Delivery data: liberty_LP5MOS_MOS5 liberty_CCS_TIMING_LP5MOS_MOS5 liberty_CCS_POWER_LP5MOS_MOS5 power_grid_voltus 4). Desired Delivery date 5). Status of results: Non-exclusive.

Can you tell me, What is diode forward bias operation in X-Fab ? Certainly, I'd be happy to help you with it. To answer your question regarding of diode forward bias operation in X-Fab, In general we don't support forward biasing of diodes in our technologies unless specifically stated such as Schottky diodes. Mostly this is because the diode model parameters are chosen such that the reverse operation of the diode can be accurately simulated. This does not mean that the simulation of the diodes in forward direction is totally wrong, but it can be less accurate. To model a diode in forward direction often requires parameters that are not available in the model or are insufficiently supported. You can simulate in forward direction and you will get a typical diode characteristic which is fairly accurate in the low current range but may be less accurate in the high current range (knee current, series resistance). In some of our documents is the statement that "forward bias is not modeled" which is based on this lack of accuracy in the models. The parameters describing the diode in forward bias are also very layout-specific, so an accurate model for a diode in forward bias would have to be related to a fixed layout.

Can you tell me, Can you show me on how tospecify an alpha PDK with xkit ? Certainly, I'd be happy to help you with it. To answer your question regarding on how tospecify an alpha PDK with xkit. For this, you can Include the '--useversion' option, for example: xkit -t xt018 --useversion 7.0.1.A2

Can you tell me, What is correct method to start DRC and LVS run ? Certainly, I'd be happy to help you with it. To answer your question regarding the correct method to start DRC and LVS run, I advise you to not use .rul files directly, please use an appropriate header file which will set variables corresponding to your PDK setup options.

Can you tell me, if a new PDK version has been released, do I need to update to PDK package if design is already in progress ? Certainly, I'd be happy to help you with it. To answer your question regarding if a new PDK version has been released, do I need to update to PDK package if design is already in progress, the answers is, for new designs, we recommend customers always use the latest PDK. For designs in progress when an update is released, customers can review the revision notes at which both the changes document for the process specifications, and the notes in the rev_info.txt files for each EDA package to evaluate if the changes are critical to their design. In principle, we could have rare special cases where we wouldn't accept designs based on an older PDK. Bear in mind that at tape-in, our mask tooling team always uses the most recent runset for DRC, so customers might want to check their designs with the latest runset to avoid possible surprises.

Can you tell me, Is there any correlation between the deviation of the sheet resistance (RS) of resistors and that of their thermal coefficients TC1 and TC2 ? Certainly, I'd be happy to help you with it. To answer your question regarding correlation between the deviation of the sheet resistance (RS) of resistors and that of their thermal coefficients TC1 and TC2. For this, In case of some resistors, there seems to be some correlation between the sheet resistance and their temperature coefficients TC1 and TC2. In some other cases the correlation seems to be quite weak. For your informatin rzp2 ,TC1 tends to the high corner for low RS and vice versa and TC2 tends to the high corner for low TC1 and vice versa. For rnp1, TC1 tends to the high corner for lower RS and vice versa and TC2 tends to the high corner for low TC1 and vice versa. For rw, TC1 tends to the low corner for lower RS and vice versa and TC2 tends to the high corner for low TC1 and vice versa. For rpp1,TC1 tends to the high corner for lower RS and vice versa and TC2 tends to the high corner for low TC1 and vice versa.

Can you tell me, how to setup customize PDK setup using .json file from SpecXplorer ? Certainly, I'd be happy to help you with it. To answer your question on how to setup customize PDK setup using .json file from SpecXplorer is that you can generate a .json file, after logging into the my X-FAB portal navigate to Design > SpecXplorer. Select your target process, then click either 'Select modules or 'Select modules by devices' (within your PDK setup, the first option will offer all devices in the selected module, second option will offer only the selected devices) and then choose the desired process modules. Click OK. Click the download icon next to the search box near the top right of the page. You can further refine the custom setup by unselecting primitive devices of the specified modules if for some reason you want to ensure they are not used. Lastly, click 'Export' to initiate download of the .json file. Use this file when starting your project by typing xkit -d . This sets up a new project with your chosen modules / devices. Please refer to the xenv userguide for further information.

Can you tell me, if the X-Fab I/O Input output libraries support copper wire bonding ? Certainly, I'd be happy to help you with it. To answer your question if X-Fab I/O Input output libraries support copper wire bonding is that we do not have any I/O libraries specifically designed for Cu or Copper bonding. Some customers have reported running into problems with copper wire bonding but in at least some cases, different customers have used exactly the same pad structure and one had no problem while the other had issues. This indicates different assembly houses can have quite different bonding parameters, and as copper wire bonding is a harsher process than gold or aluminum bonding, marginalities in the interaction between the process and bonding are more likely to show up. One suggestion is to consider using the thick metal (METTHK) module to give the widest bonding margin for assembly and don't use in conjunction with circuit-under-pad techniques. If thick metal is not or cannot be used, inform your assembly partner of the top metal thickness.

Can you tell me, what is the differences between IO_CELLS and HV_CELLS libraries ? Certainly, I'd be happy to help you with it. To answer your question regarding the differences between IO_CELLS and HV_CELLS libraries are For 5V application or LV application, it is normally sufficient to use IO_CELLS*. HV_CELLS are mainly used when none of the IO_CELLS* fit your requirement, such as needing to implement HV ESD protection. Some general remarks on the differences between HV_CELLS and IO_CELLS are that IO library pad cells are provided as pad-limited or core-limited layouts, support of multiple power rails. They are also complete IO pad cells with input output buffer circuitry, also HV pad cells are provided as block,layouts, and normally HV ESD protection structures are too big to fit into a LV IO pad cell frame, moreover HV pad cells consist of protection block and bond pad, and usually contain no power rails or HV input output buffer circuitry and lastly the protection block can be combined with different size bond pads, and it is intended as a starting point for custom HV ESD pad cell designs.

Can you tell me, Why there is no MIM capacitor antenna DRC checks in XH035 also in other X*035 technology ? Certainly, I'd be happy to help you with it. To answer your question regarding why there is no MIM capacitor antenna DRC checks in XH035 also in other X*035 technology is that for single MIM option on X035, we believe there is no issue with plasma damage. For DMIM construction on X035 which resembles the case of two individual single MIMs - no cross coupling routing, we also believe that it has low impact. So far, we have not seen any big issue with the 0.35um process due to plasma induce damage (PID) from designs point of view with all existing working customers product. Therefore you see in general the guideline is it considered as a recommendation only.

Can you tell me, which Synopsys tools are supported ? Certainly, I'd be happy to help you with it. To answer your question regarding which Synopsys tools are supported by X-Fab is that we support several Synopsys tools such as Design Compiler which is purposed for digital synthesis with required inputs Data Formats -> Liberty. Next we also support Custom Compiler so called Custom Designer which is purposed for full analog design framework similar to Cadence IC61 with required inputs EDA Vendors->Synopsys ->CustomCompiler or CustomDesigner. Lastly, supported synopsys tool is IC Compiler which is purposely for digital implementation, PnR with required inputs EDA Vendors->Synopsys->IC Compiler.

Can you tell me, which DRC settings should I use to match the X-Fab Data Input Checks for tapeout ? Certainly, I'd be happy to help you with it. To answer your question regarding which DRC settings should you need to use to match the X-Fab Data Input Checks for tapeout, you can Switch on density and popping and DUMMY_FILL.

Can you tell me, How do I solve LVS mismatch due to FILLER cells not extracting into layout netlist ? Certainly, I'd be happy to help you with it. To answer your question on how you can solve LVS mismatch due to FILLER cells not extracting into layout netlist is that the problem is due to the fact that these are empty cells with no devices, but contain ports. Possible strategies to deal with this is one could simply ignore the mismatched instance errors for these type of cells. Secondly, omitting them from the schematic would also produce a match. lastly, an empty cell with ports may be considered as a blackbox. Designating all used such cells as blackboxes will work. To do so, go to the Rules section of the PVS LVS form, select the Include PVL tab, check Include PVL Rules, and type the command lvs_black_box followed by the names of all cells to be blackboxed. I suggest to use a space as delimiter.

Can you tell me, how should I resolve the fatal DRC error when my sealring is connected to a ground pad ? Certainly, I'd be happy to help you with it. To answer your question on how you can resolve the fatal DRC error when sealring is connected to a ground pad is that E1CFCX is usually waived when the intention is to bias the ring by connecting to a voltage source for example by connecting PAD to Ground. When customer gets the DIC Data input check report, he should request waiver by mentioning within the request that the ring is intentionally biassed to ground.

Can you tell me, what is radiation Hardness ? Certainly, I'd be happy to help you with it. To answer your question regarding radiation Hardness is that X-FAB has not characterized any of its processes for radiation-hardness and we do not monitor or warrant any of our technologies for radiation hardness, nor do we have expertise in the design of radiation hardened cells. We do have customers who do their own designs for radiation hard applications that using both CMOS bulk wafer and SOI technologies , but those customers use either their own experience or public information about the best techniques to use, and then assess the results themselves. SOI processes are generally more radiation tolerant than bulk CMOS processes but we cannot say by how much in our technologies. Clearly we're not at liberty to discuss any techniques that another customer has used, so we can only refer customers to whatever can be found in the public literature to aid their design. Note that some design techniques could involve

the use of structures or layouts that are not supported by our verification decks. For DRC errors on them, we could only advise on the manufacturability of the structure, but the responsibility of waiving them would be the customer's. Any LVS or extraction issues arising from special structures not corresponding to our characterized primitive devices would also not be supported.

Can you tell me, do X-Fab have any chaterization information about radiation hardness ? Certainly, I'd be happy to help you with it. To answer your question if X-Fab have any chaterization information about radiation hardness is that X-FAB has not characterized any of its processes for radiation-hardness and we do not monitor or warrant any of our technologies for radiation hardness, nor do we have expertise in the design of radiation hardened cells. We do have customers who do their own designs for radiation hard applications that using both CMOS bulk wafer and SOI technologies , but those customers use either their own experience or public information about the best techniques to use, and then assess the results themselves. SOI processes are generally more radiation tolerant than bulk CMOS processes but we cannot say by how much in our technologies. Clearly we're not at liberty to discuss any techniques that another customer has used, so we can only refer customers to whatever can be found in the public literature to aid their design. Note that some design techniques could involve the use of structures or layouts that are not supported by our verification decks. For DRC errors on them, we could only advise on the manufacturability of the structure, but the responsibility of waiving them would be the customer's. Any LVS or extraction issues arising from special structures not corresponding to our characterized primitive devices would also not be supported.

Can you tell me, how to implement multiple instances of a ROM, each with different programming ? Certainly, I'd be happy to help you with it. To answer your question on how to implement multiple instances of a ROM each with different programming is that when you are instantiating multiple instances of the same ROM configuration but with different programmings, it is necessary to use the 'extended name' option on the front-end compiler so that each separate instance has a unique name. Otherwise, when IP replacement is performed, both instances will be identical. The distinct names will be used by the backend compiler so that the top cell name of the generated ROM block will be distinct. Otherwise the cal files submitted will be the same with identical top cell names. Then, even though your blackbox cell names are necessarily different, if we were to proceed with the IP replacement, the result would be all ROMs with the same programming. Thus to ensure each ROM instance will have the desired programming, generate the front-end data from the compiler using the extended name option to specify a unique name for each ROM.

Can you tell me and explain the usage of Page 2 of Safety area ? Certainly, I'd be happy to help you with it. To answer your question regarding the usage of Page 2 of Safety area, First, let me clarify a couple of comments on the datasheet, if power supply interruption during store is impossible then the background is that the trim bits for the charge pump are stored in page 2. The trim bits are determined and stored during wafer probe 1. The trim bits control the programming and erase behavior (timing, pulses, programming and erase voltage level) of the Store operation. If the trim bits do not have the correct value, the endurance and data retention cannot be guaranteed. Any power supply interruption (for example brown-outs) during Store operation could lead to corrupted non-volatile data, because the Store is not executed and finished correctly. Such scenarios are very application dependent. General recommendation is to store critical data like the trim bits on page 2 during wafer probe and final test and do no further Store operation to page 2 during the application. If the correct power supply and a correct Store can be guaranteed, storing to page 2 can also be done. Secondly, If no customer safety relevant data have to be stored it is sufficient to use the maximum size of page 1. In the compiler web interface on myXFAB, the page size (WORDS_PAGE1) can be customized (the restrictions are visible in the compiler web interface). If there are very few or no further critical data as described above except the NVRAM trim bits, the page 2 size can be minimized to not waste area.

Can you tell me, why Q1SU DRC flags or trigger ? Certainly, I'd be happy to help you with it. To answer your question regarding why why Q1SU DRC flags or trigger is that because the SUBCUT layer is not used for any masks, its purpose is only to perform a 'trick' for LVS to pretend the substrate is separable for different ground domains. The Q1SU rule is only a warning as are all Q* rules. B1SU is the only check for how SUBCUT is used; while DRC will always flag Q1SU whenever SUBCUT is present. You might interpret Q1SU as asking if you are intentionally using SUBCUT.

Can you tell me and explain what is Primitive Device List PDL results from Data Input Check ? Certainly, I'd be happy to help you with it. To answer your question regarding the Primitive Device List PDL results from Data Input Check is that PDL primitive device list file is produced from a special LVS run that only extracts a list of the primitive devices (including parasitic devices) present in your layout. The parasitic devices would generally be diodes that are part of the structure of high voltage or isolated transistors. The PDL file is for information only. There have been cases in some of our technologies where a primitive device may be superseded by an improved version, or conceivably some issue under certain operating conditions of a device may have been identified -- in such cases, our Customer Projects department would use the PDL to check if such devices are used in a customer's design and make sure the customer is aware of the device's status. If you want to know the locations of devices in your layout, you should perform a parasitic extraction run such as with our Cadence QRC or Calibre PEX runsets.

Can you tell me, does X-FAB offer or support Flip Chip support ? Certainly, I'd be happy to help you with it. To answer your question if X-FAB offer or support Flip Chip support is that X-FAB did not support any additional processing for flip chip such as the seed and plating layers or the ball deposition so of course customers must discuss that with their assembly subcontractor. X-FAB does not offer any flip-chip specific processing. We don't make any special processing or bondpad designs for flip-chip either, but our standard pads have been used by some customers at flip-chip houses. Please review and understand your assembly partner's rules for flip-chip to check their requirements and see what if any modification might be needed to comply. You should be able to do any layout modifications yourself.

Can you tell me, which antenna diode should i use in my design ? Certainly, I'd be happy to help you with it. To answer your question regarding of which antenna diode should you use in your design is that the connection to DIFF provides a discharge path during manufacture, so its function as an antenna diode doesn't matter which diode is used. After manufacture, the antenna role is no longer needed, and how the diode could impact the function of the circuit must dictate which diode is selected. Rather than the breakdown voltage parameter, the reverse bias operating limit should be used to decide. Alternatively, where possible, a metal bridge close to the at-risk gate oxide can be used to fix an antenna violation.

Can you tell me, concerning device operating limits, what do is the meaning of absolute'voltage limits and what it is specify ? Certainly, I'd be happy to help you with it. To answer your question concerning device operating limits and what is the meaning of absolute'voltage limits, In general for X-FAB, the absolute voltage is the maximum voltage that can be applied to a device for a short period of time without significant damage. The main reason we phrase it this way is because we can't be sure what the actual state of the device will be during this period of time. For example, if 7 volts is applied between the source and drain of a nmos4 device from the xc06 process 7V is the absolute max value for these terminals. We are not specifying what voltage is on the gate or body of the device. If the gate and body were at 0V, this voltage could probably be held forever. But if the body was at 0V and the gate was at 2V, there would be significant hot carrier current to the gate and the device could fairly quickly degrade. Since this is a circuit issue, we have to use the conservative definition. If in your designs you can guarantee that the devices are always off when the maximum voltage is applied, the

devices will probably survive indefinitely. However, please remember that X-FAB will not guarantee this.

Can you tell me,how I can export from Innovus to GDS without having to use Virtuoso to replace abstract views with the layout views ? Certainly, I'd be happy to help you with it. To answer your questio regarding on how you can export from Innovus to GDS without having to use Virtuoso to replace abstract views with the layout views is that you can directly write out from Innovus to an OA library that has replaced abstract views with layout views "oaOut ${newlibName} ${designName} ${cellName} -autoRemaster -leafViewNames { layout }". The output library should be different from the Innovus working OA library, as the new library cannot be read back into Innovus because all timing views and global settings will have been lost. Our 180nm technology Cadence PDK kernels include support for GDS export from Innovus. The mapping files to be used when streaming Innovus layers to GDS are in the technology library corresponding to your PDK setup code, for example "$X_DIR/xh018/cadence/v*_*/PDK/IC61/v*_*_*/TECH_XH018_1141/pnr_streamout.map". Additionally, the PVS QRC runset provides mapping files to be used when running QRC extraction from Innovus, for example "$X_DIR/xh018/cadence/v*_*/QRC_pvs/v*_*_*/XH018_1141/QRC-Typ/xx018_lef_qrc.map". This file exists also in the QRC-Min and QRC-Max folders.

Can you tell me, Assura tool gives background stamp errors and What exactly are these meaning ? Certainly, I'd be happy to help you with it. To answer your question regarding the Assura tool gives you background stamp errors and meaning behind this errors is that The bkgnd_StampErrorFloat error simply means that the layout being checked has no connection to the substrate. Placing even just a single PDIFF contact will clear the error of course such would not be sufficient for an entire chip. The bkgnd_StampErrorMult and bkgnd_StampErrorConnect errors work together to indicate that the layout has multiple substrate connections that are not connected to the same node with metal which resulting in soft connections through the substrate. Assura will flag one of the connections stamps with bkgnd_StampErrorMult and all of the others with bkgnd_StampErrorConnect.

Can you tell me, what is the meaning of the Assura 'minority PTUB connectors' error message ? Certainly, I'd be happy to help you with it. To answer your question regarding the meaning of the Assura 'minority PTUB connectors' error message is that It is generated by the connect statement from Assura. It means that more than one net is connected to the layer. The stamped layer receives the net information from the net with the most contacts. All other nets are marked with this error. For more detailed information please refer to the Assura manuals. X-FAB does not document tool specific messages. The Assura Command Reference manual (a document primarily aimed at runset developers) explains that: 'A layer with a soft connection is a layer that only receives connectivity information and does not pass on that connectivity information. You can use the soft keyword to check layers for high-resistivity, such as wells, where you want them to be part of the net, but you do not want them to be used as a connection between two conducting layers. This means PTUB_soft_connect errors are 'soft connection' shorts through a common layer, which is often the PSUB, or a common well. In other words, multiple distinct nets are connected to that common layer. Perhaps those distinct nets were not intended to be distinct and should be connected together by metal. It also should be inferred that it is not an error that you'll find defined in an X-FAB Design Rule Specification. For a technology such as XT018, it could result from neglecting to put a trench around a p-type tub to isolate it from other tubs.

Can you tell me, What is an "unstable device" that it triggered or flagged by Assura LVS ? Certainly, I'd be happy to help you with it. To answer your question regarding "unstable device" that it triggered or flagged by Assura LVS, this refers to a device for which device layers or connectivity are in several hierarchy levels. This message is suppressible by setting '?reportUnstableDevices nil'. For more details please see the Assura Command Reference Manual from Cadence.

Can you tell me, why I unable and cannot download X-Fab analog libraries ? Certainly, I'd be happy to help you with it. To answer your question why you unable to download X-Fab analog libraries is that all of our A_CELLS analog libraries are subject to a license agreement and one-time fee. If interested, please check with your X-FAB Sales contact for license details and a quote. The databook based on html overview page with links to individual PDF datasheets) is accessible. The library will be released upon receipt of signed license agreement and PO. The deliverable includes full schematics and complete layout.

Can you tell me, Is backgrinding available for X-Fab MPW shuttle runs ? Certainly, I'd be happy to help you with it. To answer your question if backgrinding is available for X-Fab MPW shuttle runs is that by default, we do not offer backgrinding service for customer tape-in for the MPW scheduled run. However, if a customer has such request and informs us during tape-in, we could check if we can support backgrinding for the particular case.

Can you tell me, Is backgrinding available for xs018 ? Certainly, I'd be happy to help you with it. To answer your question if backgrinding is available for xs018, in general backgrinding is not supported for xs018. This is due to the risk on optical applications which are both logistical handling and the potential defect . If it is a single exception for example MPW or non-optical application, you can try to align with our Customer Projects department to check if X-FAB can offer backgrinding.

Can you tell me, how are the PDK bindkeys for Cadence is defined or setup ? Certainly, I'd be happy to help you with it. To answer your question on how you can bind, defined and setup the PDK bindkeys for Cadence is that you should find a file .xfabcadrc created in your $HOME directory when you first execute the xkit script. For example by set XfabCadNoSetBindKey = t, means suppress default bindkey settings. However since this is commented out by default, the default Cadence bindkeys are used, which may be located in $CDSHOME/tools/dfII/samples/local. You can define your own customized bindkeys in your .cdsinit_personal file.

Can you tell me, if qpa device causes issues during LVS and how I can resolve it ? Certainly, I'd be happy to help you with it. To answer your question regarding if qpa device causes an issues during LVS and how you can resolve it. To solve this in hierarchical run, the Calibre LVS layout-extracted netlist creates an internal subcircuit for qpa which is the source of the error, for example as follow .SUBCKT qpa 1 2 3 5 ** N=8 EP=4 IP=0 FDC=1 X0 3 5 2 1 QPA $X=2600 $Y=2600 $D=20 .ENDS As we cannot interfere with Calibre's internal hierarchy processing engine, the workaround is to explicitly flatten the cell by including this command in calibre GUI LVS Options/Include tab : FLATTEN CELL qpa

Can you tell me where I can find QRC tech file for X*035, 0.35um or 350nm process that can be used with Innovus tools ? Certainly, I'd be happy to help you with it. To answer your question on where you can find QRC tech file for X*035, 0.35um or 350nm process that can be used with Innovus tools is that X-FAB does not support the QRC extraction from Innovus by using Quantus and QRC-tech files for our 0.35um or X*035 processes. The precision provided by our *.techLEF and *.capTbl files is sufficient for that technology node. Therefore we suggest you run the RC extraction in Innovus based on capTbl files which required in the Innovus setup.

Can you tell me, what is your recommendations for corner lot splits ? Certainly, I'd be happy to help you with it. To answer your question regarding recommendations for corner lot splits is that the short answer is that unlike most digital-dominated fabs, we don't have a set menu of split conditions based on fast / typ / slow that customers should choose because in a mixed signal design there is often a lot more than just Vt and poly CD that can be critical to the design (but those parameters would normally

be sufficient for a digital design). Therefore it's normal for a customer to make a specific request on what parameters it is desired to adjust and the relevant fab will review and confirm if that set of corners is possible. The negotiation would be done through Customer Projects at the relevant fab. Our digital libraries and memories are characterized in the process fast/slow 3 Sigma range. 3 Sigma production means that 99.73% of the delivered wafers are OK in terms of the stable process parameters. The process parameters are monitored with PCM test structures on each wafer. So, if your digital design is DRC, LVS clean and the timing analysis with post layout extraction is OK at the conditions as follow: 1). PVT = wp(fast), VDD_max, Tj_min 2). PVT = ws(slow), VDD_min, Tj_max then you can expect 99.73% yield of the digital block in terms of process parameter deviations. The majority of our customers don't ask for corner lots for their projects, but some customers do it. The Vt and gate length adjustments implied by your proposed corners impact the relevant transistor parameters for digital timing which are saturation current and threshold voltage. The usual flow for ordering corner lots begins with the customer identifying the critical process parameters for their design (might not be simply 'digital' parameters) and submitting a list of required corners (must conform to the PCM pass/fail parameters) to X-FAB. The feasibility of such process variations will be checked by X-FAB (Customer Projects team) and then a final corner split proposal is sent. The goal of such a corner should be to evaluate that the design would work at lower and upper spec limits. So the typical values are the upper and lower limits of the PCM Acceptance Specification (PAS). Here are some comments that have been collected from one of our FSEs. If you design according to the design rules, then the simulations should be sufficient. Some products require that the design rules be pushed to meet the performance requirements. In these cases, corner lots can identify process sensitivities where yield can be compromised. I would estimate that less than 10% of my customers are relying on Corner Lots for characterization, and these are generally only for high-volume products. When they do request they typically look at simple VTN/VTP, maybe HiRes Poly. The parameters are really design dependent. Even when I do get customers running corner lots, I'm not getting much feedback and request for product specific parametric targeting. This leads to my perception about the accuracy of the simulations. Potentially more effective than corner lots is coordinating a yield feedback loop once products are released to production. If we get your yield, bin, etc. information and input it into our yield enhancement software, we can correlate to equipment, inline, PCM, visual inspection, etc. Customers that work with us on this feedback will achieve yield stabilization much more quickly than without. We can work with you to review your Wafer/Final Test and coordinate the best means for yield feedback. One of our application engineers expanded on those comments, The customers that do request corner lots usually settle on +/-3 sigma for the parameters they are interested in. The LV MOS VT parameters are usually selected. Beyond that it really depends on the specifics of the process options the customer has chosen and the sensitivities their designers are most concerned with. However, there are some significant limitations on what parameters can be varied cleanly in a corner split. The LV MOS VT parameters are relatively straight forward because there is usually a separate VT adjust implant used on them that is separate from the well implant that controls breakdown and punch through, however there are usually a few interactions that cant be avoided (like output resistance and nw sheet resistance). The high sheet resistance poly resistors are generally easy to vary because there is usually a dedicated implant for that parameter. Beyond that things get more difficult. The HV transistor VT is sometimes split but there is almost always an interaction with transistor BVDSS, punch through, sometimes field threshold and often other parameters which can complicate evaluating the split. Other parameters are very difficult or expensive to split such as gate oxide thickness or capacitor values because they require dedicated diffusion or deposition runs that use the capacity of five or 6 lots for each split. My background is process development and I used to be a big fan of corner splits and ran a lot of them myself. I eventually concluded that they were not that useful for three reasons as follow: 1). Too often there are parameter interactions that you cannot avoid which makes it difficult to impossible to get clean results from the splits. 2). You may plan for nominal, +3 sigma and -3 sigma splits but due to normal process variation you usually end up with each of these splits +/- 1 sigma or so from your intended target, e.g. -1 sigma, +2 sigma and -4 sigma, which again makes analysis difficult or impossible and may result in some splits being non-functional. * The corner splits are arranged by artificially varying one process parameter, such as the VT implant. In actual production lots each device

parameter varies 'naturally' due to the interaction of several different process parameters. Each of these parameters has a different magnitude and direction impact on several different device parameters, usually for several different devices. As a result multiple device parameters tend to vary in a complex but related way. The corner split procedure does not reproduce this pattern so while you may get the target parameter to vary the way you want, the other device parameters will vary in a completely different way than you will see in actual production lots. For digital blocks this is probably not an important issue but for analog or RF blocks it may give a completely misleading result. I hope this input is helpful in your decision-making.

Can you tell me, if X-FAB processes be used at cryogenic temperatures ? Certainly, I'd be happy to help you with it. To answer your question if X-FAB processes can be used at cryogenic temperatures is that X-FAB generally does not have data at low temperatures below our operating range limits. We do have customers that use our technologies outside of our specified operating temperature limits, but in such cases the customer is responsible for qualifying the design in their application's temperature range. You may have noticed that the PDS states that the simulation models are valid in the junction temperature range down to -55C. As example, the XH018 PDS also specifies. The junction temperature range is defined as below: 1). Operating conditions: Tj = -40C… +175C 2). Absolute maximum ratings: Tj = -55C / +185C In general we are not aware of any specific process problems with operating down to -55C, however, we also say absolute max ratings must not be sustained for long periods hence why customers need to perform their own qualification. For the range down to -55C, we can only mention some qualitative aspects. These cannot be quantified or supported by real measurement results because we neither characterize nor qualify to that temperature. Possible trends are HCI drift may get worse - but it may be mitigated because in the state where HCI is happening, current is flowing, and the transistor sees some self-heating and The transistor junction breakdown voltages could be slightly reduced. Clearly 77K (-196C) is significantly beyond our absolute minimum operating range, so full characterization/qualification on your side will be necessary to ensure you have a robust product. I am no expert in such low temperatures but I have heard of terms such as carrier freeze out which can come into play, but such issues only amplify the requirement to do the characterization and qualification. X-FAB does not have the capability or business justification to offer such low temperature characterization (below -40C) so I'm afraid we cannot help you in that respect. I'm not really aware of a third party who could do such work either, although I'd suggest you look at our partner network (see X-CHAIN on our website) in case you can make some contacts there. Perhaps one of the Test/Assembly companies could be of interest. You might also consider trying to talk to a Space company or their suppliers if you know who they might be to see if they can do this or put you in touch with someone who can.

Can you tell me, if X-FAB processes be used at very cold or very low temperatures ? Certainly, I'd be happy to help you with it. To answer your question if X-FAB processes can be used at very cold or very low temperatures is that X-FAB generally does not have data at low temperatures below our operating range limits. We do have customers that use our technologies outside of our specified operating temperature limits, but in such cases the customer is responsible for qualifying the design in their application's temperature range. You may have noticed that the PDS states that the simulation models are valid in the junction temperature range down to -55C. As example, the XH018 PDS also specifies. The junction temperature range is defined as below: *Operating conditions: Tj = -40C Â… +175C *Absolute maximum ratings: Tj = -55C / +185C In general we are not aware of any specific process problems with operating down to -55C, however, we also say absolute max ratings must not be sustained for long periods hence why customers need to perform their own qualification. For the range down to -55C, we can only mention some qualitative aspects. These cannot be quantified or supported by real measurement results because we neither characterize nor qualify to that temperature. Possible trends are: *HCI drift may get worse - but it may be mitigated because in the state where HCI is happening, current is flowing, and the transistor sees some self-heating. *The transistor junction breakdown voltages could be slightly reduced. Clearly 77K (-196C) is significantly beyond our absolute

minimum operating range, so full characterization/qualification on your side will be necessary to ensure you have a robust product. I am no expert in such low temperatures but I have heard of terms such as carrier freeze out which can come into play, but such issues only amplify the requirement to do the characterization and qualification. X-FAB does not have the capability or business justification to offer such low temperature characterization (below -40C) so I'm afraid we cannot help you in that respect. I'm not really aware of a third party who could do such work either, although I'd suggest you look at our partner network (see X-CHAIN on our website) in case you can make some contacts there. Perhaps one of the Test/Assembly companies could be of interest. You might also consider trying to talk to a Space company or their suppliers if you know who they might be to see if they can do this or put you in touch with someone who can.

Can you tell me, what exactly does the ESD module do ? Certainly, I'd be happy to help you with it. To answer your question regarding of what exactly does the ESD module do is that Usually in older technology nodes such as CX08, the ESD implant of the ESD module is added to aid with a vertical 'spike' issue that occurs under high current such as an ESD pulse when the aluminum which is slightly p-type in the contact can 'spike' through the n-junction and short it to the P-bulk below. The ESD n-type implant is deeper than the normal n-junction, preventing a short from occurring. The p-junction is not shorted out in the same circumstance, so ESD implant is not needed on p-devices.

Can you tell me, why ESD module is not available for all MOS devices if it improves ESD robustness ? Certainly, I'd be happy to help you with it. To answer your question regarding why ESD module is not available for all MOS devices if it improves ESD robustness is that this is usually in older technology nodes such as CX08, the ESD implant of the ESD module is added to aid with a vertical 'spike' issue that occurs under high current such as an ESD pulse when the aluminum which is slightly p-type in the contact can 'spike' through the n-junction and short it to the P-bulk below. The ESD n-type implant is deeper than the normal n-junction, preventing a short from occurring. The p-junction is not shorted out in the same circumstance, so ESD implant is not needed on p-devices.

Can you tell me, how do I display DC operating parameters that I expect but not shown on the schematic ? Certainly, I'd be happy to help you with it. To answer your question on how you can display DC operating parameters that you expect but not shown on the schematic is that some DC operating parameters that are available in the Results Browser may not be displayable in the schematic. You might try adding all the required parameters to the ADE L Outputs window. This would help you to view your results after your run instead of looking into the Results Browser every time. This can be done as follows: 1). Run your DC simulation. 2). Go to ADE L Tools Results Browser 3). Double click on dcOpInfo and choose the required transistor; there you can find all the parameters. 4). Right click on the required parameter and then click on Calculator. 5). You can either copy this expression and add to your ADE L Outputs or you can just click on Send Buffer expression to ADE Outputs and this will send your calculator expression to your ADE L Outputs. You can also name your expression. Consider the operating point tables out of Cadence with caution. The CDF parameters Cadence produces are not always conformant with a SPICE simulation or even certain model card parameters. For example, often Cadence does not take into account all capacitances from a model, especially if it is a macro model. Or in other words, it is not quite clear if the capacitance calculated is the actual capacitance resulting from a SPICE simulation.

Can you tell me, why breakdown voltage parameters generally significantly different from the operating limits ? Certainly, I'd be happy to help you with it. To answer your question why breakdown voltage parameters generally significantly different from the operating limits is that the device electrical parameters are those measured either at PCM on every wafer manufactured or during a characterization phase of the development. The min/max values being defined by the measured results and then engineering experience to set the min/max limits. For breakdown voltage, these values are

when the device fails at the time of measurement. In contast the Operating Conditions are defined to ensure that the device will survive for 10 years. The accelerated life test has been or will be performed at these ratings depending upon status of process, conditional or released.

Can you tell me, if it is okay if I exceed a transistor or device operating limit ? Certainly, I'd be happy to help you with it. To answer your question if it is okay if you design exceed a transistor or device operating limit is that The breakdown voltage of a transistor is a kind of 'digital' description of the transistor strength. But the real life is manifold. Therefore reliability tests are performed to describe the transistor strength for the real world conditions. If the operating conditions are far away from the electrical limits there is no danger. But if the operating conditions get closer to the electrical limits the probability of malfunction or damage increases. Each MOS transistor consists of a parasitic bipolar transistor. This parasitic bipolar transistor makes the MOS transistor sensitive to pulses. The sensitivity depends on many factors. On the one hand on the pulse characteristics such as amplitude, length, duty cycle, rise and fall time, ripple, frequency and etc. On the other hand factors include the transistor layout such as size, construction, spacing to substrate contacts and others. There is an unlimited amount of possible scenarios. This is what it makes very difficult to judge whether special conditions can be allowed or not. Therefore only one general recommendation is to never exceed the specified operating limits.

Can you tell me, what is the difference between protection diodes and other diodes? Certainly, I'd be happy to help you with it. To answer your question regarding the differences between protection diodes and other diodes is that protection diode needs to carry a relatively high amount of current in breakdown to really protect the circuit, otherwise the voltage drop at the device to be protected can still be too high and do damage to it. Therefore it is measured at higher currents. Protection diodes are 'designed' to have a certain breakdown voltage which is defined rather by layout (overlap of wells, distances) not by doping profile. Note that usually it is more a concern about the contacts and wiring when looking at the current limits, rather than the diode parameters.

Can you tell me, if I ignore DRC errors on my logo elements ? Certainly, I'd be happy to help you with it. To answer your question if you can ignore DRC errors on your logo elements is that although a logo strucure is not a circuit element, it can be very dangerous, in some cases, to waive logo DRC errors. For example, metals and/or photo-resist that are below minimum width may float off the silicon during the processing and then get deposited elsewhere on the design and cause chip failures.

Can you tell me, which DRC rules are classified as fatal ? Certainly, I'd be happy to help you with it. To answer your question regarding which DRC rules are classified as fatal is that we do not publish a list of Fatal vs Critical errors as they are constantly under review and publication would imply that there are some errors that we don't mind the customer violating - that is not the case. We encourage customers to correct all errors - this will produce the best possible outcome on silicon. When there are special reasons that some errors cannot be fixed on layout, then we can discuss via the waiver system. You can find fatal rule violations that are available on sharepoint under "http://sp.erf.xfab.de/RandD/Projects_and_Reports/Lists/ProcessInformation/Category.aspx".

Can you tell me, do X-FAB will perform or generate the pattern fill? Certainly, I'd be happy to help you with it. To answer your question if X-FAB will perform or generate the pattern fill is that for technologies that specify density limits and include one or more blocking layers for the fill, the X-Fab will perform it. The DRC runsets for our 180nm or X*018 technologies can generate 'virtual' dummies that are taken into account during DRC. It is also possible to have the runset export the dummies to GDS such that you could merge it with your design. The problem with the dummy generation is that all structures are flat, which results in larger GDS files. Therefore it is recommended to let our Mask Tooling group do the pattern fill. For capacitively critical structures, relevant metal layers only should be blocked rather than

using the BLKALL layer. The parasitic extraction runsets can C-extract these structures for determining their impact on the performance. The fill routines observe spacing margin and dummy size rules -- one consequence of that is the fill routine is not guaranteed to satisfy the minimum density rules. When that's the case, you may need to apply some extra effort, such as manually drawing a denser fill pattern.

Can you tell me, Should I include or generate dummy pattern in my layout design ? Certainly, I'd be happy to help you with it. To answer your question if you should include or generate dummy pattern in your layout design is that for technologies that specify density limits and include one or more blocking layers for the fill, the X-Fab will perform it. The DRC runsets for our 180nm or X*018 technologies can generate 'virtual' dummies that are taken into account during DRC. It is also possible to have the runset export the dummies to GDS such that you could merge it with your design. The problem with the dummy generation is that all structures are flat, which results in larger GDS files. Therefore it is recommended to let our Mask Tooling group do the pattern fill. For capacitively critical structures, relevant metal layers only should be blocked rather than using the BLKALL layer. The parasitic extraction runsets can C-extract these structures for determining their impact on the performance. The fill routines observe spacing margin and dummy size rules -- one consequence of that is the fill routine is not guaranteed to satisfy the minimum density rules. When that's the case, you may need to apply some extra effort, such as manually drawing a denser fill pattern.

Can you tell me, what is the purpose of the technology libraries with an 'HD' suffix ? Certainly, I'd be happy to help you with it. To answer your question regarding the purpose of the technology libraries with an 'HD' suffix is that Using xh018 as example, TECH_XH018 is the primary technology library to use. TECH_XH018_HD is a supplementary library, to be used in addition to TECH_X018, when the HD high density logic libraries D_CELLS_*HD are used. It accounts for the tighter routing grid used by the HD logic libraries for P&R; or place and routes. Originally, the HD tech library was developed as a supplementary library, meaning both the normal and HD libraries should be used referenced by a design library using an HD logic library for P&R.; We then decided to make the HD tech library more complete such that on the HD tech lib needed to be referenced by the design library. In such case, if you try to reference both tech libs, you will get a conflict error. More recently, we have reverted back to the original style.

Can you tell me, if ELDO views for Cadence PDK is available ? Certainly, I'd be happy to help you with it. To answer your question if ELDO views for Cadence PDK is available is that Unfortunately we don't support ELDO views in our Cadence PDKs. An extra license is necessary to test such views in Cadence libraries, and we do not have that currently in X-FAB, so we cannot check and guarantee the correctness of such views. In principle it might be possible for a customer to use ELDO as a simulator within Cadence, although a hurdle may be the netlisting for the simulator, which may have some specific aspects different from the netlisting for Spectre or for HSpice. The conclusion is that X-FAB does not support ELDO simulation from Virtuoso within Cadence and that we don't have any instructions for those attempting to do so.

Can you tell me, the recommendation or suggestion of electromigration tests for AC or DC factor ? Certainly, I'd be happy to help you with it. To answer your question regarding the recommendation or suggestion of electromigration tests for AC or DC factor is that we usually calculate with a DC to AC conversion factor of 10. It is referred to the Pass or Fail margin at 0.1% error probability for the individual test.

Can you tell me, if the specified current density limits sufficient for metal width when considering ESD ? Certainly, I'd be happy to help you with it. To answer your question if the specified current density limits is sufficient for metal width when considering ESD is that regarding the required metal width for ESD,

usually the metal resistance is critical and not the current density/current capability of the metal. The current density for HBM ESD pulses is in the range of several hundred mA/um width for example 300-400mA/um). Only narrow metal lines would be damaged by ESD stress currents. The metal resistance is critical since voltage drops across power rails will add to the pad clamping voltage. Especially in the rail-based protection scheme the power rail resistance is critical. Concerning the power rail width, power rails should provide as rule of thumb a DC current capability of 50mA for 2kV HBM ESD robustness. A different metal resistance in the connections of multi-finger ESD protection devices can result in non-uniform current distribution and early failure of the ESD protection structure. Typical layout errors are e.g. largely different metal width in anode and cathode metal connections of diodes resulting in a current concentration in a small area of the diode or a largely different metal width between drain metal and source metal in ESD nmos snap-back devices resulting as well in non-uniform current distribution.

Can you tell me, what is FLATPV and SFLATPV ? Certainly, I'd be happy to help you with it. To answer your question regarding what is FLATPV and SFLATPV is that FLATPV is Flat passivation module and SFLATPV is Sensor flat passivation.

Can you tell me, what is the procedure for an IO and ESD review by X-FAB ? Certainly, I'd be happy to help you with it. To answer your question regarding the procedure for an IO and ESD review by X-FAB is that the customer sends the layouts, schematics and all relevant descriptions such as normal pin operating voltages, max. ratings, required ESD robustness and etc to hotline@xfab.com. It is important for the review that when any type of analog IO cell (LV or HV) is used, also the circuitry that connects directly to the pad must be shown. We'll review the design data and provide first results via email. There can then be further review loops after design changes. There can then be also further online or face-to-face meetings for clarification - if required. A design review in an online meeting or face-to-face meeting is not appropriate. There is a higher risk that possible ESD design issues are overlooked when there is just a browsing through the design during an online meeting. Therefore an offline review is preferred.

Can you tell me, How can I use various GATES logic libraries? Certainly, I'd be happy to help you with it. To answer your question on how you can use various GATES logic libraries is that the GATES libraries are schematic and parameters only libraries which are used as referenced 'building block' gates libraries inside the D_CELLS libraries. They support only the schematic side of the respective D_CELLS* libraries the rev_info.txt file of a given D_CELLS library will specify which GATES* library it requires. Therefore the GATES libraries cannot and must not be used as a stand-alone library.

Can you tell me, where I can find GATES_PCELL library that is available for most technologies? Certainly, I'd be happy to help you with it. To answer your question on where you can find GATES_PCELL library that is available for most technologies is that the library is classified as an analog library for the purpose of my X-FAB organization under Design > EDA Files, filter to Libraries > Analog > GATES_PCELL. However, unlike our other analog libraries, these GATES_PCELL libraries are freely available to customers, there is no license requirement or fee. Within the library is a userguide document. As the library name inplies, it provides parameterized cells for some types of gates which some basic logic functions, transmission gates, and other related special purpose cells. The introduction in the userguide states that The intention of this library is to provide a cell library for analogue components. This includes layout, schematics and verilog. It is not the intention to use the components in a digital design flow. You must use characterised cells instead.

Can you tell me, my layout contain BOX elements and what are this ? Certainly, I'd be happy to help you with it. To answer your question regarding BOX elements and what are this issue with BOX elements has been described in the 'Guideline for GDSII data' document on my X-FAB:

https://my.xfab.com/search/_action/relation/596e0b4e-74cd-47af-96ae-87dd43b1bdf5/ Unlike the boundary, the BOX element is not a filled figure. Therefore it cannot be used for IC geometry.

Can you tell me, my layout was flagged because it contain BOX elements and why are they not accepted ? Certainly, I'd be happy to help you with it. To answer your question why your layout was flagged because it contain BOX elements and why are they not accepted. This issue with BOX elements has been described in the 'Guideline for GDSII data' document on my X-FAB: https://my.xfab.com/search/_action/relation/596e0b4e-74cd-47af-96ae-87dd43b1bdf5/ Unlike the boundary, the BOX element is not a filled figure. Therefore it cannot be used for IC geometry.

Can you tell me, Why simulations of transistor leakage produce inaccurate results that are independent of device widths ? Certainly, I'd be happy to help you with it. To answer your question why simulations of transistor leakage produce inaccurate results that are independent of device widths is that this issue is related to the default gmin setting of the simulator, which is gmin=1e-12. This gives every node a conductivity of 1e-12 to aid convergence. That means basically it 'adds' at 1V a current of 1e-12A. Therefore this is not dependent on the transistor's width. To get correct results for such diode currents of small devices at T=27C you need to set gmin=1e-18. Please note that for some simulators like hspice, there are separate parameters: gmin and gmindc.

Can you tell me, if X-FAB can provide IBIS models ? Certainly, I'd be happy to help you with it. To answer your question if X-FAB can provide IBIS models is that X-Fab does not support IBIS models. This falls beyond the scope of X-FAB's modelling and library support, as we are a pure-play wafer manufacturer. As I understand it, the IBIS model provides I/O device characteristics through I/V data and switching characteristics in ASCII format. The IBIS models are meant for the transfer of data and not to define an executable simulation model. They are component specific, which means that they model an entire component for example an FPGA and not just a particular I/O. IBIS models are supposed to serve for implementing the behavior of I/Os into a technology independent PCB level EMC simulation environment. We cannot provide correct IBIS models since we don't have all the required package and pin related data. I/O cell characteristics are available in data sheets, Verilog models and especially the timing Liberty format files, which you could use to generate the switching characteristic for an IBIS model.

Can you tell me, What is the maximum recommended temperature for wafer post processing ? Certainly, I'd be happy to help you with it. To answer your question regarding the maximum recommended temperature for wafer post processing for post-processing is that usually we generally recommend that temperatures above 350C should be absolutely prevented. Higher temperatures can lead to metal-passivation or capacitor popping, IMD cracking, transistor shifts, metal voiding, enhanced Rpoly and especially RpolyH shifts depending on design, temperature ramp rate, duration and application atmosphere (N2, H2, etc.). If >350C cannot be avoided, we strongly recommend a DOE with the respective IC design using enhanced final test and also proper optical inspections after slightly accelerated post-processing stress for example slightly increased ramp rates, slightly longer storage times.

Can you tell me, Why my account cannot download a memory compiler ? Certainly, I'd be happy to help you with it. To answer your question why your account cannot download a memory compiler is that X-FAB does not distribute our memory compiler software to customers. Instead, a compiler must be run from my X-FAB. To do so, click the 'play' icon in the action column when you rest your mouse pointer over the icon, the pop-up text 'Start the application of this container' will be displayed. After specifying configuration options of the desired memory, the front-end design data will be available for download. As this is blackbox IP, the netlist and layout will not be provided. When you have decided on a particular configuration to use for a tape-out, please check with your X-FAB Sales contact to ensure the

license agreement and P.O. are in place before submitting your design. Blackbox IP replacement approval is one of the first checks on a newly submitted SiFo -- if the L.A. and P.O. are not available, the SiFo will be held at the step and not proceed to have data input checks (includes DRC) performed. The license incurs a one-time fee, rather than royalties, and you can then instantiate the IP as often as you'd like in subsequent designs. For example, For ROM IP, each future reprogramming will incur a small fee.

Can you tell me, by comparing the metal thicknesses of the bond pad stack to those of the Structural and Geometrical Parameters, why are the metal layers thinner on the bond pad ? Certainly, I'd be happy to help you with it. To answer your question why metal layers is thinner on the bond pad is that the Structural and Geometrical Parameters show the metal layer thicknesses as deposited. However if you have large oxide windows as are there on the bond pad structures, then the pad metal is thinned (etched back), and this results in thinner metal layers directly on the bonding pads. Some process documents have the bond pad diagrams showing each metal layer with an ARC layer on top and below the metal. These ARC layers are relatively thin. The deposited thickness parameters include the ARC layers since they affect the stack thickness and hence all the parasitic capacitances. When the passivation window is opened onto the top metal, the final ARC layer is removed. Hence the bonding pad diagrams and associated note indicate a lesser thickness.

Can you tell me, what are D_CELLS DECAP cells for ? Certainly, I'd be happy to help you with it. To answer your question of what is D_CELLS DECAP cells for is that these cells provide capacitors between vdd and gnd to reduce digital noise and IR drop. They are usually inserted during Place and Route after routing (where existing routing allows). In a second step, FEED* cells always have to be inserted to fill up the cell rows in places where no DECAP cells could be added. You may add (the larger, DECAP*15/DECAP*25) cells also before routing to have a certain amounnt of capacitors in the block, but these cells might have an influence on routability of the block. See Innovus commands addFiller, deleteFiller for details."

Can you tell me, what is PDL.txt file or primitive device list that is included from the X-Fab DRC run result ? Certainly, I'd be happy to help you with it. To answer your question regarding PDL.txt file or primitive device list that is included from the X-Fab DRC run result is that the PDL is a primitive device list. This file is the result of a special LVS run that only extracts the primitive devices (including parasitic devices) present in your layout. The parasitic devices included (p_*) would generally be diodes that are part of the structure of high voltage or isolated transistors. The PDL file is for information only. There have been cases in some of our technologies where a primitive device may be superseded by an improved version, or conceivably some issue under certain operating conditions of a device may have been identified -- in such cases, our Customer Projects department would use the PDL to check if such devices are used in a customer's design and make sure the customer is aware of the device's status.

Can you tell me, The PVS.sum DRC result will last error counts for each rule like RULECHECK B1M2MIM ..... Total Result 68 (80). What is the differences and distinction between these two given numbers? Certainly, I'd be happy to help you with it. To answer your question regarding the differences and distinction between RULECHECK B1M2MIM ..... Total Result 68 (80) is that In this example, the 68 is the hierarchy result and the 80 is the flat run result.

Can you tell me, How to generate the PDL.txt or primtive device list file ? Certainly, I'd be happy to help you with it. To answer your question on how you can generate PDL.txt or primtive device list file is that this the primitive device list is generated using PVS LVS. The command line option requires setting parameters in a header file. Using the PVS LVS GUI may be easier for most users to extract a list of the primitive devices used in a given layout. Please refer to below method on how to generate PDL.txt or Primitive Device List file as follow: 1). Open layout (read-only is OK) 2). PVS -> Run LVS 3). Input ->

exclude comparison setup 4). Output -> LVS Report -> Click 'SET' button. 5). Apply/Submit to initiate the run. To generate the Results, please refer to following: 1). Files/Output Files: Extraction report -> scroll to bottom of report. 2). Or in the Extraction tab, Uncheck 'hide statistic' then click on flat device count. 3). Or you can just open the _lvs.sum file from the run directory. The list is at the end of the file.

Can you tell me, Why X-Fab pattern fill did not resolve, fix or clear R1DF minimum DIFF density design rule violations or errors? Certainly, I'd be happy to help you with it. To answer your question regarding why X-Fab pattern fill did not resolve, fix or clear R1DF minimum DIFF density design rule violations or errors because As flatly stated in the 'Dummy Pattern Generation' section of the Design Rule Specification, 'The dummy pattern generation script does not guarantee that the minimum and maximum structure densities of the related layer are met.' The document further recommends 'to use X-FAB's dummy pattern generation option (DUMMY_FILL included in the DRC for preview) to create dummy pattern. If the generated dummy pattern is not sufficient to meet the minimum requirements for pattern density, customers can draw additional dummy pattern following the dummy design rules...' -- the referenced R1DF application note may be helpful (especially for the case of poly resistor arrays), or other situations might be solved by placing larger DIFF dummy structures. The *.rdb files from DRC will indicate the pattern density of flagged windows (R1DF is checked in 200um square windows stepped by 100um), which is given by the 'DV' parameter (multiply it by 100 for percentage).

Can you tell me, What is the basis for Schottky diode forward bias limit ? Certainly, I'd be happy to help you with it. To answer your question regarding the basis for Schottky diode forward bias limit is that It is important not to exceed the Vanode-Vcathode operating limit for the forward direction current. This would tend to exceed the allowable thermal load of the diode. Select an appropriate size for the intended current and to be safe, apply some margin with respect to the size.

Can you tell me, what is the convention for the SiFo major and minor versioning ? Certainly, I'd be happy to help you with it. To answer your question regarding the convention for the SiFo major and minor versioning is that the major version indicates how often a SiFo was sent to X-FAB AND went into the Data Input Check loop. The minor version indicates how often a SiFo was edited AND saved in my X-FAB.

Can you tell me, What are X-FAB's recommendations for timing signoff ? Certainly, I'd be happy to help you with it. To answer your question regarding X-FAB's recommendations for timing signoff is that for 0.18 tech STA we have the 0.18um-ApplicationNote-Digital_Implementation_Guidelines document at "https://my.xfab.com/search/_action/relation/4aeecb61-a2b5-4d16-ab9a-f6a4457c583f/" On page 7, section 6.3 it states A further set_timing derate ... is not needed as only the variation of the pin input capacitances is modelled in X-FAB's 180nm, X*018 libraries. Further up to now we did not recommend any derating to customers. It's your responsibility (and sometimes based on your internal quality requirement) how much margin you add to a timing analysis. In our standard Place and Route STA's we always use OCV (with no further de rating) in PrimeTime as this is PT's default method. In Innovus we run up to routing the simple and faster bc/wc delay calculation, only for post-route optimization we switch to OCV (when we don't forget that one line in the scripting...).From our customers base we know, we could give you few scenarios as follow: Customer 1: (mostly XH018): they add +/-15% to the delay calculation (requested by their quality department): set_timing_derate -cell_delay -net_delay -early 0.85 set_timing_derate -cell_delay -net_delay -late 1.15 in sdc Customer 2: We used +/-5% for their XP018 redesign (their first design had no timing closure with our standard settings without derating, so they needed a special process modification to get working silicon at all). set_timing_derate -cell_delay -net_delay -early 0.95 set_timing_derate -cell_delay -net_delay -late 1.05 (Their redesign had timing closure with this additional margin). For a complete STA you have to run 3 sets: - the 'normal' one without derating - the pessimistic one: set_timing_derate -cell_delay -net_delay -early 0.95 set_timing_derate -cell_delay -net_delay -late 1.05 - and the optimistic one: set_timing_derate

-cell_delay -net_delay -early 1.05 set_timing_derate -cell_delay -net_delay -late 0.95 To have a complete picture. Basically we believe the more derating margin you add, the lesser confidence you have into the quality of the spice models of the transistors and all the timing characterization of the digital libraries and parasitic extraction.

Can you tell me, What films are on the wafer backside ? Certainly, I'd be happy to help you with it. To answer your question regarding of what films are on the wafer backside, as an example from a particular technology flow, backside films include a stack of oxide, nitride, TEOS, SION, nitride (the most outer layer). There may be some differences depending on technology and module options. During manufacture, the backside is not necessarily protected from what is grown or deposited on the front side (this would be the case, for example, when wafers are loaded for batch processing into a tool in a quartz boat), so there is some accumulation of films on the backside. For many applications, wafers would undergo a backgrind operation to thin total wafer thickness, which also removes such films.

Can you tell me, What is the crystal orientation of X-FAB wafers ? Certainly, I'd be happy to help you with it. To answer your question regarding crystal orientation of X-FAB wafers. The crystal orientation for 8-inch CMOS wafers are Wafer surface plane is 100 and Wafer notch direction is 110.

Can you tell me, why my layout design flagged, triggered for including the PIMP layer ? Certainly, I'd be happy to help you with it. To answer your question regarding why your layout design flagged, triggered for including the PIMP layer because the PIMP layer is not available with the ISL main module. There is a blanket implant where active is open (DIFF). If PIMP is included in your GDS, a critical (not fatal) error is flagged since PIMP is only valid for MOS main module flow. For ISL flow, either omit PIMP layer from GDS to prevent the error, or waive the error.

Can you tell me, Considering rules of W1DF and W2DF, what is the risk with narrow DIFF lines ? Certainly, I'd be happy to help you with it. To answer your question by considering the rules of W1DF and W2DF and what is the risk with narrow DIFF lines is that one possible risk for narrow DIFF lines is problems with proper silicidation, which may result in different resistances than otherwise expected.

Can you tell me, When we try to fix rule W5M1 Minimum MET1 width joining wide MET1 track errors, we sometimes get inexplicable errors Certainly, I'd be happy to help you with it. To answer your question regarding when you try to fix rule W5M1 Minimum MET1 width joining wide MET1 track errors and obtain some inexplicable errors because this rule is marked in red in the specification, which means it cannot be 100% reliably checked by verification decks. The rule requires sizing operations on layers that can produce artifacts on non-orthogonal shapes. That's why the rule is unselected by default in the runset. It can be activated and it provides some assistance but it is the user's final responsibility to check manually. This is also why we don't check the rule at tape in.

Can you tell me, if X-Fab perform metal fill for xb06 or X*06 process or technologies ? Certainly, I'd be happy to help you with it. To answer your question if X-Fab perform metal fill for xb06 or X*06 process or technologies is that although the xb06 Peripheral Ring diagram available on my X-FAB shows the NOFILLM layer, we do not normally perform metal fill for XB06. However the rules are in place, and we have done it as a special case when requested by a customer. So unless it is requested, there is no need to include the NOFILLM layer. The xb06 Cadence PDK has the layer defined: it's specified in the stream layer table, but the layer palette has the layer set as invalid, so a user would have to change it to valid to be able to draw with it.

Can you tell me, what is the purpose, intent and meaning of design rule B1PADM ? Certainly, I'd be happy to help you with it. To answer your question regarding the the purpose, intent and meaning of design rule B1PADM is that for B1PADM there are several reasons: one was to get similar heights of the pads. With different definition layers, different oxide stacks grow below the pad. For CMOSDEF e.g. there is a thinner oxide is grown, for DMOSDEF a thicker oxide is grown, without CMOSDEF and DMOSDEF an even thicker one is grown. DMOSDEF also forbids several design layers like POLY1 or DIFF in this area.

Can you tell me, What is the purpose, intent and meaning of design rule B1PATR ? Certainly, I'd be happy to help you with it. To answer your question regarding the purpose, intent and meaning of design rule B1PATR is that this rule B1PATR serves to reduce capacitive coupling between the pad metal and the silicon around it.

Can you tell me, What is the purpose, intent and meaning of design rule B1MD ? Certainly, I'd be happy to help you with it. To answer your question regarding the purpose, intent and meaning of design rule B1MD is that he reason why the MVLT and MERGEDEF was formulated as mutually exclusive into the Design Rule Spec at the time when it was originated seems to have been forgotten. There will be no risk if the TRENCH of devices with MVLT layer are merged as long as the condition of voltage difference <50V is valid.

Can you tell me, What is the purpose, intent and meaning of design rule S2TR ? Certainly, I'd be happy to help you with it. To answer your question regarding the purpose, intent and meaning of design rule S2TR is that the S2TR rule was implemented to ensure that floating tubs were always built the same way. It applies to nested trench rings used in the MUTRIS core for device isolation and its intent was to prevent engineers from placing contacts between these rings because for the isolation in the MUTRIS core to work properly these silicon tubs must be floating. This requirement is not as strict for the newer SITRUS core but the rule has been left in the process because of the number of older designs using the MUTRIS core.

Can you tell me, The SPICE model libraries include *_bjt models for some MOS devices and what are they for ? Certainly, I'd be happy to help you with it. To answer your question regarding the SPICE model libraries that include *_bjt models for some MOS devices and what it is for, In short the purpose of the added PNP bipolars to the *_bjt models is to show that there can occur bipolar effects under certain conditions, but it is by far not very accurate and it has limitations. It is nevertheless extracted on silicon at different geometries and good simulation accuracy can be expected when the HVMOS channel is completely switched off and only the drain/bulk junction is forward-biased. But in other cases, the accuracy is limited, especially when the channel is in inversion and/or the bulk/substrate junction is forward-biased. Both conditions change the minority carrier distribution in the bulk/base a lot and lead to a change in the beta. There is no statistical process monitoring for these parasitic BJTs. In our experience the most reliable results and complete picture in simulation can be achieved with the substrate extractor tool, which is supported for xh018. See "https://my.xfab.com/search/_action/relation/c7d55cc4-78d6-4d22-bdfa-897b19a3c8d4/"

Can you tell me, The NVRAM datasheet indicates 1.8V and 3.3V supplies are required, are they both needed for normal operationor just only for programming ? Certainly, I'd be happy to help you with it. To answer your question. STORE / RECALL operations require 1.8V and 3.3V; READ / WRITE of the SRAM requires only 1.8V. The 3.3V is only necessary (in addition to 1.8V) during STORE (the programming of the non-volatile part) and during RECALL (the cycle for bring back the information to the SRAM). For read / write of the SRAM only the 1.8V supply is needed.

Can you tell me, some MOS devices have butted NDIFF and PDIFF regions with only a single contact and how should this connection be understood, comprehend, explained ? Certainly, I'd be happy to help you with it. To answer your question regarding that some MOS devices have butted NDIFF and PDIFF regions with only a single contact and how should this connection be understood, comprehend, explained. In general, the NDIFF and PDIFF can be butted and a single CONT used to connect to the butted nodes because all the DIFF is covered with a silicide layer which shorts together the NDIFF and PDIFF, the CONT makes connection to the silicide layer."

Can you tell me, the usage of HRPOLY and LRPOLY modules ? Certainly, I'd be happy to help you with it. To answer your question regarding the usage of HRPOLY and LRPOLY modules is that the primitive devices in the HRPOLY module are already included in the MOSLL or MOSLT main modules flow. Similarly, the primitives in the LRPOLY module are already included in the MOS or MOS5 main modules. The resistors rpp1 and rnp1 have the HRES as a design layer. This layer is included on the primitive device in the PRIMLIB. For MOS/MOS5 process flows, the HRES design layer is used to generate the UGM mask. For the MOSLL/MOSLT flows the HRES design layer is not used. The resistors rp1 and rsp1 have the LRES as a design layer. This layer is included on the primitive device in the PRIMLIB. For MOSLL/MOSLT flows, the LRES design layer is used to generate the NGM mask. For the MOS/MOS5 flows the LRES design layer is not used. The Design Rule Specification includes these comments in the design layer table such as LRES Required for device recognition. Also used for mask generation when MOSLL or MOSLT modules are selected. LRES under MOS flow IS USED for mask generation with the XRPOLY module. See the dpol device rules. HRES Required for device recognition. Also used for mask generation when MOS or MOS5 modules are selected. Please leave the HRES design layer on the resistors.

Can you tell me, What is the differences, distinction between the types of body tied transistors ? Certainly, I'd be happy to help you with it. To answer your question regarding the the differences, distinction between the types of body tied transistors is that there are two types of transistors available in the XI10 process, the H and A types. The A type transistors use the 'castellated' source/body structure; they have the advantage that they can be made whatever width the customer wants because the body contact is distributed along the source width. However, they have the disadvantage that the N+ and P+ diffusions for the source and body are touching, so there will be biasing limitations for these terminals. The xi10 S/D is not silicided, so at least there is no direct short between the source and body in these transistors, but with the N+/P+ abutment, trying to apply different voltages to the source and body will likely result in either high leakage between the two terminals or outright breakdown as this structure is effectively a surface Zener diode. The H type transistors place the body contacts of the transistors at the ends of the channel and separate the P+ and N+ diffusions by a cross connection of poly to the gate (the designation 'H' transistors comes from the resulting shape of the poly gate). The advantage of these devices is that with the diffusions separated no parasitic Zener diode is formed, so leakage and breakdown between the source and body will not be an issue. The disadvantage of these devices is that due to body resistance perpendicular to the channel, the ratio of W/L is limited for the devices to 6 for the nmos and 12 for the pmos devices.

Can you tell me, how should the poly ring of diodes be biased ? Certainly, I'd be happy to help you with it. To answer your question on how should the poly ring of diodes be biased is that due to its lateral construction, the diode is different from pure bulk junction diodes in other processes. You might review the Device Characteristics Documentation you can either download the package or browse online by clicking the globe icon to see how the poly ring potential influences the current. Can check this link "https://my.xfab.com/search/_action/relation/96b7577d-f3b9-40e3-b81f-27cee2e35705/". The 'dn' model is a subckt model consisting of level1 diode models with different ideality factors. In this model the different diodes are used to model the current forward/reverse over temperature. With respect to the diode current the process variation is solely covered by changing the 'is' parameter in the model and the ideality factor is unchanged. Usually the diode current consists of an ideal and a non-ideal part

and the ratio of both can change with process variation (the non-ideal part is fluctuating, while the ideal part is very stable). Changing the ideality factor in the model would lead to a large deviation of the current over temperature, which we do not observe, but we only have limited data from a statistical point of view (only lab measurements over T). It is safer to avoid using this device for high precision applications like bandgaps because the forward voltage variation is not measured by PCM test and therefore also the corner models will not be as accurate as needed for this purpose.

Can you tell me, What is the handle wafer contact resistance ? Certainly, I'd be happy to help you with it. To answer your question the resistance of handle wafer contact, is that It is in the 10 kOhm range. We do not specify a value because it cannot be measured easily, e.g. from one HW contact to another the handle wafer resistance is in-between, from top to bottom is the thickness of the handle wafer and if not back-lapped the oxide on bottom also. A similar issue exists for XT06; however a contact 'resistance' is specified in the Process Specifications, but indeed much of the resistance comes from handle wafer (undoped) resistance, not the contact itself.

Can you tell me, How should I connect the 'wh' handle or handle wafer pin ? Certainly, I'd be happy to help you with it. To answer your question on how you can connect 'wh' handle or handle wafer pin is that the 'wh' handle wafer pin represents the connection of the back handle of the wafer situated just below the BOX and allows the connection of a substrate model to the device. A local artificial substrate under the below devices is recognized as their 'wh' terminal with description as follow: 1). RF MOS : diffusion area enclosing source/drain regions 2). Front-End Resistors : body of the devices 3). Capacitors : bounding box of the device 4). Varactors : diffusion area The 'wh' handle wafer terminal connection for RF MOS, Front-End Resistors (Poly1 and Diffusion type), capacitors and varactors as follow: 1). Leave it floating 2). Connect it to a noConn device (to avoid warnings after 'Check and Save") 3). Connect it to lsubmod device The 'wh' pin for all other devices (DC MOS, inductors and metal resistors) are merged together during LVS/PEX to a single substrate node which equals the wafer back side connection the 'wh' terminal of these devices must be tied together in the schematic a label with the name of this common node must be placed anywhere in the layout cell view. The label must be drawn using the LPP Wafer_txt:drawing. Merging 'wh' pins in the layout view for example it is required when using of multiplier 'm' device parameter for the devices with internal vertical substrate model or when using ser/par of resistors such as series resistors The Marksub:Commonsub (33:33) has to be drawn around the concerned devices in order to represent their common wafer handle terminal. Concerning the third pin of the MIMCAP, the 'wh' pin (pin below the BOX) could be ignored. This is for simulating the lateral substrate model. There is no issue in ignoring it concerning LVS.

Can you tell me, Why do I get nwell, pwell width errors, violations flag, triggered for my pe5 devices? With relevant rules that include W1W1, W1W2, W1W3, W1W4, E1MVDF. Certainly, I'd be happy to help you with it. To answer your question of why you get nwell, pwell width errors, violations flag, triggered for my pe5 devices because Such errors should be corrected. NWELL drawn outside MV will be NWELL1, NWELL inside MV will be NWELL2. With NWELL crossing MV, the sliver outside MV is NWELL1. All NWELL associated with the pe5 must be enclosed by MV. For the pe5 devices, the MV layer extends 0.6um beyond the NWELL. This seemingly large MV enclosure of NWELL is due to the fact that the space between MV and the nwell will be PWELL2, for which rule W1W4 dictates a 0.6um minimum width.

Can you tell me and show me list of devices with HW handle wafer terminal ? Certainly, I'd be happy to help you with it. To answer your question regarding list of devices with HW handle wafer terminal. Several transistors such as nhvta, nhvtb, nhvu, ndhvt, ndhvta, phvta, phvtb and phvu need a handle wafer connection for simulation. The fifth terminal 'HW' of these transistors is used for this. It is necessary to connect this terminal in schematic and layout. LVS checks this connection. The connection of the handle wafer can be realized by a top side or a back side connection. In case of top

side connection the HWC module is to be used. If the back side application is used or in case of the transistors nhvta, nhvtb, nhvu, ndhvt, ndhvta, phvta, phvtb and phvu, an auxiliary handle wafer contact is necessary in the layout view. The Certainly, I'd be happy to help you with it. To answer your question. auxiliary handle wafer contact is only used for LVS and simulation, no mask will be created. The xt018-ApplicationNote-Layout_Techniques document explains how to create an auxiliary handle wafer contact in layout.

Can you tell me, With what potential should the handle wafer or HW should be biased ? Certainly, I'd be happy to help you with it. To answer your question regarding with what potential should the handle wafer or HW should be biased. I advise your to please see section 2.5 in the xt018 layout techniques application note. The xt018 Process & Device Specification provides operating limits for each device with respect to the HW.

Can you tell me, Why XT018 or xt018 HV_CELLS library is not automatically loaded ? Certainly, I'd be happy to help you with it. To answer your question why XT018 or xt018 HV_CELLS library are not automatically loaded because the module requirements can differ depending on the selected cell -- this applies mainly to the 1.8V cells as they are not compatible with the MOS5 core module. In the Cadence PDK environment, whether an X-FAB library is available for a particular PDK startup option is controlled by the pdk_code.txt file within the library. The file currently in the library only specifies options with the LP5MOS main module. However, the library can also be used with the MOS5 main module (except the 1.8V cells, as already noted). The pdk_code.txt file can be amended as below to include MOS5, which specifies the compatible options. Change the file in your installed library at (the exact path depends on the library version) $X_DIR/xt018/esdlibs/HV_CELLS/v1_2/cadence_IC61/v1_2_0/HV_CELLS/ with the content below. It's important that when selecting any cell, you ensure that its module requirements are consistent with those of your design. See guideline as follow: # Do not edit this file! # File keeps xkit start up information # HV_CELLS v1_2_0 # MOS5 options added PDK_CODE xt018_1231_LP5MOS_MET3_METMID PDK_CODE xt018_1232_LP5MOS_MET3_METTHK PDK_CODE xt018_1233_LP5MOS_MET3_METMID_METTHK PDK_CODE xt018_1241_LP5MOS_MET3_MET4_METMID PDK_CODE xt018_1242_LP5MOS_MET3_MET4_METTHK PDK_CODE xt018_1243_LP5MOS_MET3_MET4_METMID_METTHK PDK_CODE xt018_1251_LP5MOS_MET3_MET4_MET5_METMID PDK_CODE xt018_1252_LP5MOS_MET3_MET4_MET5_METTHK PDK_CODE xt018_5031_MOS5_MET3_METMID PDK_CODE xt018_5032_MOS5_MET3_METTHK PDK_CODE xt018_5033_MOS5_MET3_METMID_METTHK PDK_CODE xt018_5041_MOS5_MET3_MET4_METMID PDK_CODE xt018_5042_MOS5_MET3_MET4_METTHK PDK_CODE xt018_5043_MOS5_MET3_MET4_METMID_METTHK PDK_CODE xt018_5051_MOS5_MET3_MET4_MET5_METMID PDK_CODE xt018_5052_MOS5_MET3_MET4_MET5_METTHK

Can you tell me, how pe5ti device is different from the pe5 device in XT018 or xt018 ? Certainly, I'd be happy to help you with it. To answer your question how pe5ti device is different from the pe5 device in XT018 or xt018 is that the xt018 pe5ti is a trench-isolated pe5 without a PTUB below it. The peti and pe5ti devices were generated in response to a request for a pe or pe5 device that did not need a p-well contact as this would take up more room. We came up with the peti and pe5ti devices specifically for this reason. These devices are standard pe or pe5 transistors but with HVNWELL used below the N-well which converts the entire tub to N-type.

Can you tell me, Why rm1 metal resistor breakdown is much lower than that of higher level metal resistors ? Certainly, I'd be happy to help you with it. To answer your question regarding why rm1 metal resistor breakdown is much lower than that of higher level metal resistors is that this is related to the

ILD/IMD voltage rating, for MET2 there is much thicker oxide than for MET1. There is design rule S1M1DF, but this would require a DTI between the MET1 and DIFF geometry in question. If there are no active devices below rm1, the device could be placed over floating ISOTUB(s).

Can you tell me, after upgrading to version 12 PDK, why do rpp1 instances of existing design show different parameter values that flag and trigger B7P1 design rule violations ? Certainly, I'd be happy to help you with it. To answer your question regarding after upgrading to version 12 PDK, why do rpp1 instances of existing design show different parameter values that flag and trigger B7P1 design rule violations is that this is due to the underlying well options. The background here is that we found a bimodal distribution of rpp1 sheet resistance with NWELL below, depending on whether LP5MOS or MOS5 core module was used. To address this, we now offer two rpp1_3 resistor types: the rpp1_3 and a rpp1nw_3. The rpp1_3 has a new higher sheet resistance than before while the rpp1nw_3 has the same sheet resistance as the version 11 rpp1_3. This explains why, using rpp1_3, you get a different length for the same resistance in v12 PDK. You could use the new device rpp1nw_3 instead of rpp1_3 to get a better match to the old v11 and avoid the B7P1 error. Alternatively, you could leave your layout as-is and waive the B7P1 error as it is not fatal, but then if the design is re-used in a different core module later, you may see a different performance.

Can you tell me, What is the relation, coorelation of FIMP mask to drawn layers ? Certainly, I'd be happy to help you with it. To answer your question regarding the the relation, coorelation of FIMP mask to drawn layers is that xt06 FIMP mask defines where the field implant is not implanted. It is not intuitive that the NOFIMP layer is the direct design entry for the FIMP mask. Having in mind the FIMP mask is meant for blocking the global FIMP implant in the process makes it easier to understand.

Can you tell me, for wafers held at Poly, at what step are the wafers actually held or stop ? Certainly, I'd be happy to help you with it. To answer your question regarding at what step are the wafers actually held or stop especially for wafer held at poly is that for a request to hold at Poly, we will hold it at Active (ACT/DIFF) layer instead. For the 0.18um technologies, ACT and POLY1 dummies are required and both dummies are interlinked. Therefore, any POLY1 redesign may affect the ACT layer and may result in a new ACT mask. If the wafers that have been on hold at Poly had already processed with the old ACT mask, clearly the new ACT mask cannot be used for these wafers. So to avoid this from happening, we suggest to hold the wafers at the Active layer. However, if you can confirm that your future redesign will not change the ACT mask, we can support your request to hold the wafers at Poly.

Can you tell me, What helps are available for resolving, clearing, fix MIM capacitor antenna errors ? Certainly, I'd be happy to help you with it. To answer your question regarding of what helps are available for resolving, clearing, fix MIM capacitor antenna errors is that The MIM-capacitor antenna rules are defined in the 0.18um-ProcessSpecification-DR_MIM_Antenna_Rules document. Advice for preventing and resolving such errors can be found in the 0.18um-ApplicationNote-MIM_Capacitors_Check document. You can visit this link on how to resolve this violations: 1). https://my.xfab.com/search/_action/relation/0d92400d-b4de-48f3-9bb8-38e7aaf134b9/ 2). Supplemental 'MIMANT' DRC runsets for checking these antenna rules are available for PVS, Calibre, and IC Validator. 3). https://my.xfab.com/search/_action/relation/491ae11f-379c-4a5e-b2b0-8445c79c830d/ 4). https://my.xfab.com/search/_action/relation/557ba3a2-ee77-4034-8518-5917dac84d4d/ 5). https://my.xfab.com/search/_action/relation/de9558d0-b114-4f5f-bf3f-d8c7ab2562d3/

Can you tell me on how to connect the fifth terminal of HW handle wafer terminal ? Certainly, I'd be happy to help you with it. To answer your question the usage of fifth terminal of HW handle wafer terminal is that several transistors such as nhvta, nhvtb, nhvu, ndhvt, ndhvta, phvta, phvtb and phvu

need a handle wafer connection for simulation. The fifth terminal 'HW' of these transistors is used for this. It is necessary to connect this terminal in schematic and layout. LVS checks this connection. The connection of the handle wafer can be realized by a top side or a back side connection. In case of top side connection the HWC module is to be used. If the back side application is used or in case of the transistors nhvta, nhvtb, nhvu, ndhvt, ndhvta, phvta, phvtb and phvu, an auxiliary handle wafer contact is necessary in the layout view. The Certainly, I'd be happy to help you with it. To answer your question. auxiliary handle wafer contact is only used for LVS and simulation, no mask will be created. The xt018-ApplicationNote-Layout_Techniques document explains how to create an auxiliary handle wafer contact in layout.