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Code: 15EC32T

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III Semester Diploma Examination, April/May-2018

DIGITAL ELECTRONICS

Time: 3 Hours		[Max. Marks : 100
No	ote: (i) Answer any six full questions from Part – A (ii) Answer any seven full questions from Part – B	
	PART – A	BETA CONSOLE!
1.	Define decoder. List applications of Decoder.	Diploma - [All Branches Beta Console Education 3
2.	State race around problem. Illustrate elimination of same using	g logic diagram. 5
3.	Define registor. List application of shift registors.	Diploma Question Papers [2015] 19] Beta Console Education 5
4.	Write short note on Counter.	5
5.	Define following w.r.t. ADC: (a) Conversion time (b) Quantization error (c) Accuracy	5
6.	Explain Dynamic Random Access Memory Cell.	5
7.	Write a note on Flash memory.	5
8.	Compare fixed logic device and programmable logic device.	5
9.	Define: (a) fan out (b) power dissipation (c) propagation delay of logic gates	5
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	PART – B	
10.	Explain decimal to BCD encoder and also write logic diagram, truth table and logic symbol.	10
11.	Construct BCD to seven segment decoder and explain logic diagram, truth table and logic symbol.	10
12.	Explain JK flip-flop with the help of logic diagram, truth table and timing diagram.	10
13.	(a) Explain with the help of circuit diagram of a stable multivibrator using IC 555 timer.	7
•	(b) List features of IC 555 timer. BETA CONSO	DLEI
14.	(a) Explain serial in serial out shift register with logic diagram and truth table? Ma-	[A § Branche
	(b) Explain ring counter with diagram and truth table.	5 .
15.	State modulus of a counter. Explain configuration of decade counter using IC 749 and write logic diagram and truth table.	0 io n (japers [20
16.	(a) List application of DAC.	5
	(b) List specifications of DAC.	5 .
17.	Construct circuit diagram of dual slope ADC and explain.	10
18.	(a) Implement and explain full adder using PAL write logic diagram and trut table.	h 5
,	(b) Explain memory word size and capacity of memory with examples.	5
19.	(a) Compare TTL and CMOS logic families.	5
1.71	(b) Explain circuit diagram & working of TTL NAND gate.	5