## Code: 15EC52T

Register						
Number				er		

## V Semester Diploma Examination, April/May-2019

## ARM CONTROLLER

	ARM CONTROLLER					
Tim	ne: 3 Hours] [Max. Marks: 1	[ Max. Marks : 100				
Instructions: (i) Answer any six questions from Part – A. (6 × 5 = 30 marks)  (ii) Answer any seven full questions from Part – B. (7 × 10 = 70 m						
1.	PART - A  Describe the functions of flags of CPSR register.  FOXY ORO  BY BETA CONSOLE  Explain MAC unit with an example.	5				
3.	BETA CONSOLE  Explain ARM THUMB networking using BX instructions.	5				
4.	Explain the functions of following directives:  (i) DCD  (ii) DCB  (iii) DCW	5				
5.	Explain exception handling in ARM processor.	5				
6.	Write code for enabling IRQ & FIQ interrupts.	5				
7.	List any five features of LPC 2148.	5				
8.	Define timer & PWM of LPC 2148.	5				
9.	Explain the bit structure of PLLCFG register.	5				

## PART - B

10.	Expl	ain typical ARMCORE embedded device.	10
11.	(a)	Explain different ARM processor modes.	6
	<b>(b)</b>	Explain the AMBA bus protocol.	4
12.	Expl	ain banked registers with a neat diagram.	10
13.	(a)	Explain SWAP & SWI instructions with example.	5
	(b)	Explain TST & TEQ instructions with example.	5
14.	(a)	Compare ARM & THUMB instructions.	5
	(b)	Write an ALP to find factorial of a no.  FOXY ORO BY BETA CONSOLE W.	5
15.	(a)	Explain non-nested interrupt handler with a neat sketch.	6
	(b)	List the interrupt handling schemes.	4
16.	(a)	List any five features of UART.	5
	(b)	Explain the importance of brown out detector.	5
17.	(a)	Sketch a neat block diagram of PLL.	6
	(b)	List any four features of timer in LPC 2148.	4
18.	(a)	Explain the features of GPIO.	5
	(b)	Explain the applications of GPIO.	5
19.	(a)	Explain legacy GPIO registers.	, , , , , , , , , , , , , , , , , , ,
	(b)	Describe bit structure of DACR registers.	5