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V Semester Diploma Examination, Nov./Dec. 2017

ARM CONTROLLER

Tim	ne : 3 Hours	Max. Marks : 100
Note	2: (1) Answer any six questions from Part – A. $(6 \times 5 = 3)$ (2) Answer any seven full questions from Part – B. (7)	•
	PART – A	
1.	List the applications of ARM processor.	SETA CONSOLE!
2.	Explain Barrel shifter with a neat sketch.	5 Diploma - [All Branches]
3.	Describe the following directives :	Beta Console Education 3*
	EQU, SPACE, ALIGN, DCD, DCW	
4.	Explain ARM-THUMB networking using BLX instruction.	Diploma Qu S stion Papers [2015-19]
5.	Write code for disabling IRQ and FIQ interrupts.	Beta Console Education
6.	Explain interrupt stack design with a neat sketch.	5
7.	List any five features of RTC.	5
8.	Name any five features of I ² C.	5
9.	Explain the bit structure of PLL STAT register.	5
	1 of 2	[Turn over
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10.	(a) (b)	PART – B Explain ARM CORE data flow model. Justify the features that improves code density.	8 2
11.	(a) (b)	Explain bit structure of CPSR. Justify how ARM is suitable for mobile applications.	8 2
12.	(a) (b)	Explain MVN, MRS and MSR instruction with example. Distinguish between post and pre indexed addressing mode with an example.	6 4
13.	(a) (b)	Test whether the following instructions are pre or post index addressing mode (i) STR R6, [R4, #4] (ii) LDR R3, [R12], #6 (iii) LDRB R4, [R3, R2] (iv) LDR R6, [R0, R1, ROR #6] (v) STR R3, [R0, R5, LSL # 3] Calculate the effective address of the following instructions if Register R3 = 0×4000 & register R4 = 0×20 . (i) STRH R9, [R3, R4] (ii) LDRB R8, [R3, R4, LSL #3] (iii) LDR R7, [R3], R4 (iv) STRB R6, [R3], R4, ASR #2 (v) LDR R0, [R3, -R4, LSL #3]	• [All Branches]
14.	(a) (b)	Compare ARM and THUMB instructions. Write an ALP to find largest number in an array.	5 5
15.	(a) (b)	Explain non-nested interrupt handler with a neat sketch List the interrupt handling schemes. 19 Beta Console Education	stion Papers [2015- 6 4
16.	Sket	ch a memory map of LPC 2148.	10
17.	(a) (b)	Calculate the values of PLL configuration register (PLLCFG) for the following frequency specification CCLK = 60 MHz, PCLK = 15 MHz, FCCO 156 MHz to 320 MHz, FOSC = 10 MHz. List any four features of Timer in LPC2148.	ng is 6 4
18.	(a) (b)	Write C program to interface LEDs to all pins in port 0 (P0.0 to Po.15) make repeatedly blink all LEDs high then low, then high and so on (introduce some delay). List any four applications of GPIO.	ке
19.	(a) (b)	Sketch a neat block diagram of TIMER. List the Legacy GPIO registers.	8 2