386

Code : 15EC52T

V Semester Diploma Examination, Oct./Nov.-2019

ARM CONTROLLER

Time : 3 Hours]   [Max. Marks : 100

Note :   (i)   Answer any **six** questions from PART – **A**.

       (ii)   Answer any **seven** full questions from PART – **B**.

PART – A   6 × 5 = 30

1.   List the special features of ARM processor design.   5

2.   Explain conditional execution with an example.   5

3.   Explain register usage in thumb.   5

4.   List any five difference between ARM and thumb state.   5

5.   Define the following terms with respect to ARM7 :   1 × 5 = 5
    (i)   Exception
    (ii)   Vector table
    (iii)   Interrupt latency
    (iv)   Exception handler
    (v)   Pre-fetch abort

6.   Discuss link register offsets.   5

7.   List any five features of LPC – 2148.   5

8.   Explain power modes in LPC 2148.   5

9.   List any five features of GPIO.   5

PART – B   7 × 10 = 70

10.   Sketch and explain ARM core data flow model.   10

11. (a) Explain the role of software components in an embedded system.   5
    (b) Explain 3-stage pipeline with example.   5

12. Explain the following instructors : $2 \times 5 = 10$
    (i) RSC R_0, R_1, R_2
    (ii) BIC R_0, R_1, #256
    (iii) SWAP R_0, R_1, [R_2]
    (iv) CMP, R_0, R_1
    (v) ADD R_0, R_1, R_2

13. (a) Write the instruction to perform the following operations : $1 \times 5 = 5$
    (i) Copy a CPSR into R_1 register.
    (ii) Add the two register R_1 & R_2 content along with carry flog, placing the result in the R_3 register.
    (iii) Instruction which causes a software interrupt exception.
    (iv) To returning from subroutine
    (v) Copy a complement of 4 into R_1
    (b) Write a note on MAC unit.   5

14. (a) Explain the structure of ARM assembly language format.   5
    (b) Write an ALP to find factorial of a number.   5

15. (a) Explain Non-nested interrupt handler with a neat sketch.   7
    (b) Distinguish between nested and non-nested interrupt handler.   3

16. Sketch memory map of LPC 2148 and explain briefly the features of on chip program memory and on chip static RAM.   10

17. Explain the architecture of Timer module.   10

18. Sketch a neat block diagram of PLL and explain.   10

19. (a) Write C program to interface LEDs to all pins in Port 0 (P0.0 to P0.15) make repeatedly blink all LEDs high then low then high and soon (introduce some delay)   5
    (b) Choosing, FOSC = 10 MHz and CCLK = 60 MHz configure PLL.   5