1431

Code : 15MC21T

Register Number | | | | | | | |

II Semester Diploma Examination, April/May - 2018

FUNDAMENTALS OF DIGITAL ELECTRONICS

Time : 3 Hours] **[Max. Marks : 100**

Note : (i) Part-**A** : Answer any **six** questions.
(ii) Part-**B** : Answer any **seven** questions.

PART - A

Answer any **six** of the following.

1. Explain constituents of mechatronics system. **5**

2. Discuss the properties of BCD Code. **5**

3. Subtract 47 from 61using 1's complement method. **5**

4. Define the following with respect to logic gates : **5**
   (i) Fan-in
   (ii) Propagation delay

5. State and prove De-Morgan's theorem. **5**

6. Distinguish between combinational circuits and sequential circuits. **5**

7. Explain the operation of 4 : 1 multiplexer with a logic diagram and truth table. **5**

8. Explain race around condition. How it is eliminated in master slave flip-flop ? **5**

9. Explain the features of PLA. **5**

[Turn over

PART – B

Answer any **seven** full questions of the following.

10. Explain building blocks of mechatronics system with the help of block diagram. 10

11. Perform the following operations : 10
    (i) $121.25_{(10)}$ to Binary number
    (ii) $825_{(10)}$ to BCD
    (iii) $57.06_{(8)}$ to Decimal number
    (iv) $5C7_{(16)}$ to Binary number
    (v) $1110011_{(2)}$ to gray code

12. What are universal gates ? Realize all Basic gates using NAND gate. 10

13. Solve the following expression using k-map to obtain minimal expression and implement the same using logic gates. 10
    $Y = \Sigma m\ (0, 2, 3, 4, 6, 8, 10, 11)$

14. Explain the operation of full subtractor circuit using Truth table, output expression and logic diagram. 10

15. Explain the operation of 3 to 8 line decoder using Truth table and logic diagram. 10

16. (a) Compare asynchronous and synchronous counters. 5
    (b) Explain the significance of PRESET and CLEAR inputs in flip-flops. 5

17. (a) Draw the schematic diagram of an edge triggered JK flip-flop using NAND gates and write its truth table. 5
    (b) Draw the logic diagram of 4-bit SISO shift register and its truth table (using D flip-flop). 5

18. Explain the operation of Mod-10 ripple up counter with the help of logic diagram, truth table and timing diagram. 10

19. Implement full adder using PAL with Boolean expressions for output. 10
