726 Register No.:

April 2019

Time – Three hours
(Maximum Marks: 75)

[N.B: (1) Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory. Answer any FOUR questions from the remaining in each PART – A and PART – B

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 marks in PART – A, 3 marks in Part – B and 10 marks in PART – C.]

PART – A

1. What are the various fields in an instruction format?
2. What is the advantage of interrupt initiated data transfer?
3. Define paging.
4. List down the Flynn's classification of computer.
5. What is pipelining?
6. Expand NUMA.
7. List any two characteristics of SMP.
8. What is the function of a decoder in a memory connection?

PART – B

9. Give the RTL for memory read operations.
10. Draw the block diagram of I/O interface.
11. Write a short note about MODEM.
12. How to initialize a cache memory?
13. Explain four stage pipeline with block diagram.
14. Differentiate NUMA from SMP.
15. What are the advantages of using dedicated caches over shared caches?
16. Draw the flag register. Explain about the various setting of the flags.

[Turn over.....

PART – C

17. (a) Explain about register transfer in detail.

(Or)

(b) Explain in detail the functioning of the control unit with block diagram.

18. (a) (i) Explain destination initiated hand shaking method of data transfer.
(ii) Draw the flow chart of CPU-IOP communication.

(Or)

(b) Explain interrupt controller operation.

19. (a) (i) Explain the operation of a magnetic disk.
(ii) How to map a virtual address using pages?

(Or)

(b) Explain about direct mapping technique of cache memory.

20. (a) (i) Explain the different blocks in BIU of 8086.
(ii) Write the various types of parallel computer organisations.

(Or)

(b) Explain the instruction pipeline in detail.

21. (a) (i) Write about different approaches to vector computation.
(ii) Explain about SMP organization.

(Or)

(b) Draw and explain the core i7 processor operation.
