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October 2018

Time – Three hours
(Maximum Marks: 75)

[N.B: (1) Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory. Answer any FOUR questions from the remaining in each PART – A and PART – B

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 marks in PART – A, 3 marks in Part – B and 10 marks in PART – C.]

PART – A

1. Give an example for inter-register transfer.
2. Mention the drawback in strobe control of data transfer.
3. What is I/O bus?
4. Define address space.
5. Name the machine control flags in 8086 processor.
6. What is vector computation?
7. Define thread.
8. Write the purpose of RAM and ROM.

PART – B

9. Write about interrupt cycle.
10. Mention the main components of CPU and write their functions.
11. What is vectored interrupt? Explain with an example.
12. Mention the different methods of serial communication.
13. Give a short note about pipelining.
14. Give the detail of pointer registers available in 8086 processor.
15. What is the need for page replacement technique in memory operation?
16. Write some features of SMP.

[Turn over.....

PART – C

17. (a) Explain the function of stack and its limits.

(Or)

(b) Brief about the applications logic micro operations.

18. (a) (i) Explain asynchronous mode of serial transfer.
(ii) Mention the I/O commands available in I/O transfer.

(Or)

(b) How a DMA transfer operation is performed? Explain in detail.

19. (a) (i) Explain about memory table for mapping a virtual address.
(ii) Write about secondary memory.

(Or)

(b) Explain the following cache memory mapping techniques:
(i)Direct (ii)Associative.

20. (a) (i) Draw the block diagram of 8086.
(ii) Mention the Flynn's classification of parallel organizations.

(Or)

(b) Explain instruction pipelining in detail.

21. (a) Explain the various approaches of vector computation with diagram.

(Or)

(b) Explain in detail the organization of a z990 mainframe.
