857 Register No.: ____

October 2018

Time – Three hours
(Maximum Marks: 75)

[N.B: (1) Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory. Answer any FOUR questions from the remaining in each PART – A and PART – B

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 marks in PART – A, 3 marks in Part – B and 10 marks in PART – C.]

PART – A

1. Define need of test.
2. What the benefit of automation?
3. List out the types of waveform used in VI characteristics.
4. What is BSDL?
5. List the functionalities of JTAG.
6. Define the term load-board.
7. What is a simulator?
8. What is digital guarding?

PART – B

9. Discuss about the basic principle of memory testing.
10. Write the functional faults in memory.
11. Whether board integrity can be tested using ICFT? Justify.
12. List the few elements of BSDL.
13. Draw the logic diagram of half subtractor and its truth table.
14. What is the difference between boundary scan, JTAG and IEEE 1149.1?
15. What do you mean by test fixture?
16. Draw the VI signature of good versus bad signature of inductor and capacitor.

[Turn over.....

PART – C

17. (a) Explain about the fundamental testing methods.

(Or)

(b) Explain in detail the process involved in PCB troubleshooting.

18. (a) What is clock termination? Explain in brief about different clock termination techniques.

(Or)

(b) Construct a two input NAND gate using TTL logic. Explain its operation.

19. (a) Describe in brief about the characteristics of passive components.

(Or)

(b) With an example, explain how the ageing effects are analyzed using VI curve trace.

20. (a) Explain boundary scan TAP controller with state diagram.

(Or)

(b) Explain boundary scan test application with block diagram.

21. (a) Explain the concepts of fault simulation and fault dictionary in reference to test program set.

(Or)

(b) What are the prerequisites for developing an effective test program to test a PCB module?
