Notes on Compiler Optimizations

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November 2, 2004

Basic Blocks in the Quad Table:

p := 1 for i:= 1 to 10 do $p := i * p$

Table 1: default

$L \rightarrow 11$	:=	1		p
12	:=	1		i
$L \rightarrow 13$	$\leq$	i	1	t1
14	jfalse	t1		block
$L \rightarrow 15$	$*$	i	p	p
16	$+$	i	1	i
17	jmp			t3
$L \rightarrow 18$				

There are concepts of leaders for basic blocks.

In the basic blocks, we are to try to use local block for usage optimization. This is useful for going from basic block to basic block. This produces a large amount of information to deal with unreachable code.

Basic Block

1.

Given expression:

$$X := ((Y * 4) + (X + 3))/(4 * 2) + 3$$

Check out the quads for this expression.

Op code R A R, mem AR R1, R2

Table 2: default

10	*	y	4	t1
11	+	X	3	t2
12	+	t1	t2	t3
13	*	4	Z	t4
14	/	t3	t4	t5
15	+	t5	3	t6
16	:=	t6		X

L 1, Y M 1, =F'4' // full word '4' ST 1, t1 L 1, X A 1, =F'3' ST 1, t2 L 1, t1 A 1, t2 ST 1, t3 L 1, =F'4' M 1, Z ST 1, t4 L 1, t3 D 1, t3 ST 1, t5 L 1, t5 A 1, =F'3' ST 1, t6 L 1, t6 ST 1, X

Assumption, register is empty on leaving the quad. ? . There is apparently 20 quads for 6 quads. This amounts to about 3 instructions per quad. The idea optimization is use a large number of registers to reduce loads and stores.

Table 3: default

$L \rightarrow 11$	:=	1		p
12	:=	1		i
$L \rightarrow 13$	$\leq$	i	1	t1
14	jfalse	t1		block
$L \rightarrow 15$	*	i	p	p
16	+	i	1	i
17	jmp			t3
$L \rightarrow 18$				

Memory allocation table

Temporary memory may exist only exist in registers. However, memory address can exist in memory or registers. There is also a need for a register table, which is specific for the processor. There are also Live Next Uses to apply to operand fields and result fields.

Table 4: default

ID	L/NU	Loc - R/M
X		
Y		
Z		
t1 X		
t2		
t3		
t4		
t5		
t6		