PCI Bus Pin Out, [Parallel Bus]

PCI Bus pinout for both 32 bit and 64 bit cards is shown below;
Signal Pins 63-94 are only used on 64 bit PCI bus cards. The PCI pinout for the 32 bit bus stops at the key-way [Spacer], while the 64 bit pin out occupies the entire table. The PCI local bus was used in personal computers to provide expansion slots for add-on cards to the motherboard.
The PCI bus replaced the ISA PC-AT expansion slot in PCs.
The PCI local bus is not the same as the new PCI Express bus which has a completely different pinout.

Peripheral Component Interface Pinout

The number sign in the pinout table below refers to: "A # symbol at the end of a signal name indicates that the signal's asserted state occurs when it is at a low voltage. The absence of a # symbol indicates that the signal is asserted at a high voltage.

PCI Bus PinOut

Pin #	name	PCI Pin Description	Pin #	name	PCI Pin Description
A1	TRST	Test Logic Reset [JTAG Bus]	B1	-12V	-12 VDC
A2	+12V	+12 VDC	B2	TCK	Test Clock [JTAG Bus]
A3	TMS	Test Mode Select [JTAG Bus]	B3	GND	Ground
A4	TDI	Test Data Input [JTAG Bus]	B4	TDO	Test Data Output [JTAG Bus]
A5	+5V	+5 VDC	B5	+5V	+5 VDC
A6	INTA	Interrupt A	B6	+5V	+5 VDC
A7	INTC	Interrupt C	B7	INTB	Interrupt B
A8	+5V	+5 VDC	B8	INTD	Interrupt D
A9	---	Reserved	B9	PRSNT1	Present
A10	+5V	Power (+5 V or +3.3 V)	B10	---	Reserved
A11	---	Reserved	B11	PRSNT2	Present
A12	GND03	Ground or Keyway for 3.3/Universal PWB	B12	GND	Ground or Keyway for 3.3/Universal PWB
A13	GND05	Ground or Key-way for 3.3/Universal PWB	B13	GND	Ground or Open (Key) for 3.3/Universal PWB
A14	3.3Vaux	--	B14	RES	Reserved
A15	RESET	Reset	B15	GND	Ground
A16	+5V	Power (+5 V or +3.3 V)	B16	CLK	Clock
A17	GNT	Grant PCI use	B17	GND	Ground
A18	GND08	Ground	B18	REQ	Request
A19	PME#	Power Management Event	B19	+5V	Power (+5 V or +3.3 V)
A20	AD30	Address/Data 30	B20	AD31	Address/Data 31
A21	+3.3V01	+3.3 VDC	B21	AD29	Address/Data 29

A22	AD28	Address/Data 28	B22	GND	Ground
A23	AD26	Address/Data 26	B23	AD27	Address/Data 27
A24	GND10	Ground	B24	AD25	Address/Data 25
A25	AD24	Address/Data 24	B25	+3.3V	+3.3VDC
A26	IDSEL	Initialization Device Select	B26	C/BE3	Command, Byte Enable 3
A27	+3.3V03	+3.3 VDC	B27	AD23	Address/Data 23
A28	AD22	Address/Data 22	B28	GND	Ground
A29	AD20	Address/Data 20	B29	AD21	Address/Data 21
A30	GND12	Ground	B30	AD19	Address/Data 19
A31	AD18	Address/Data 18	B31	+3.3V	+3.3 VDC
A32	AD16	Address/Data 16	B32	AD17	Address/Data 17
A33	+3.3V05	+3.3 VDC	B33	C/BE2	Command, Byte Enable 2
A34	FRAME	Address or Data phase	B34	GND13	Ground
A35	GND14	Ground	B35	IRDY#	Initiator Ready
A36	TRDY#	Target Ready	B36	+3.3V06	+3.3 VDC
A37	GND15	Ground	B37	DEVSEL	Device Select
A38	STOP	Stop Transfer Cycle	B38	GND16	Ground
A39	+3.3V07	+3.3 VDC	B39	LOCK#	Lock bus
A40	SMBCLK	SMB CLK [SMbus Description]	B40	PERR#	Parity Error
A41	SMBDAT	SMB DATA [SMbus Description]	B41	+3.3V08	+3.3 VDC
A42	GND17	Ground	B42	SERR#	System Error
A43	PAR	Parity	B43	+3.3V09	+3.3 VDC
A44	AD15	Address/Data 15	B44	C/BE1	Command, Byte Enable 1
A45	+3.3V10	+3.3 VDC	B45	AD14	Address/Data 14
A46	AD13	Address/Data 13	B46	GND18	Ground
A47	AD11	Address/Data 11	B47	AD12	Address/Data 12
A48	GND19	Ground	B48	AD10	Address/Data 10
A49	AD9	Address/Data 9	B49	GND20	Ground
A50	Keyway	Open or Ground for 3.3V PWB	B50	Keyway	Open or Ground for 3.3V PWB
A51	Keyway	Open or Ground for 3.3V PWB	B51	Keyway	Open or Ground for 3.3V PWB
A52	C/BE0	Command, Byte Enable 0	B52	AD8	Address/Data 8
A53	+3.3V11	+3.3 VDC	B53	AD7	Address/Data 7
A54	AD6	Address/Data 6	B54	+3.3V12	+3.3 VDC
A55	AD4	Address/Data 4	B55	AD5	Address/Data 5
A56	GND21	Ground	B56	AD3	Address/Data 3
A57	AD2	Address/Data 2	B57	GND22	Ground
A58	AD0	Address/Data 0	B58	AD1	Address/Data 1
A59	+5V	Power (+5 V or +3.3 V)	B59	VCC08	Power (+5 V or +3.3 V)
A60	REQ64	Request 64 bit	B60	ACK64	Acknowledge 64 bit
A61	VCC11	+5 VDC	B61	VCC10	+5 VDC
A62	VCC13	+5 VDC	B62	VCC12	+5 VDC
64 bit spacer KEYWAY					
64 bit spacer KEYWAY					

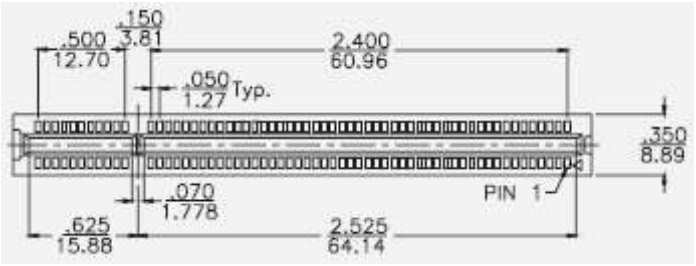
A63	GND	Ground	B63	RES	Reserved
A64	C/BE[7]#	Command, Byte Enable 7	B64	GND	Ground
A65	C/BE[5]#	Command, Byte Enable 5	B65	C/BE[6]#	Command, Byte Enable 6
A66	+5V	Power (+5 V or +3.3 V)	B66	C/BE[4]#	Command, Byte Enable 4
A67	PAR64	Parity 64	B67	GND	Ground
A68	AD62	Address/Data 62	B68	AD63	Address/Data 63
A69	GND	Ground	B69	AD61	Address/Data 61
A70	AD60	Address/Data 60	B70	+5V	Power (+5 V or +3.3 V)
A71	AD58	Address/Data 58	B71	AD59	Address/Data 59
A72	GND	Ground	B72	AD57	Address/Data 57
A73	AD56	Address/Data 56	B73	GND	Ground
A74	AD54	Address/Data 54	B74	AD55	Address/Data 55
A75	+5V	Power (+5 V or +3.3 V)	B75	AD53	Address/Data 53
A76	AD52	Address/Data 52	B76	GND	Ground
A77	AD50	Address/Data 50	B77	AD51	Address/Data 51
A78	GND	Ground	B78	AD49	Address/Data 49
A79	AD48	Address/Data 48	B79	+5V	Power (+5 V or +3.3 V)
A80	AD46	Address/Data 46	B80	AD47	Address/Data 47
A81	GND	Ground	B81	AD45	Address/Data 45
A82	AD44	Address/Data 44	B82	GND	Ground
A83	AD42	Address/Data 42	B83	AD43	Address/Data 43
A84	+5V	Power (+5 V or +3.3 V)	B84	AD41	Address/Data 41
A85	AD40	Address/Data 40	B85	GND	Ground
A86	AD38	Address/Data 38	B86	AD39	Address/Data 39
A87	GND	Ground	B87	AD37	Address/Data 37
A88	AD36	Address/Data 36	B88	+5V	Power (+5 V or +3.3 V)
A89	AD34	Address/Data 34	B89	AD35	Address/Data 35
A90	GND	Ground	B90	AD33	Address/Data 33
A91	AD32	Address/Data 32	B91	GND	Ground
A92	RES	Reserved	B92	RES	Reserved
A93	GND	Ground	B93	RES	Reserved
A94	RES	Reserved	B94	GND	Ground

Designer note; the pinout provided on this page relates to the PCI main board connector on the mother board. Add-in cards [daughter boards may have a slightly different connector pin out.

Internal Buses on the PCI Bus

Address/Data Bus:	64bit Address; 64bit Data, Time Multiplexed
System Bus:	2bits; Clock/Reset
Interface Control Bus:	7bits; Ready, Acknowledge, Stop
Parity Bus:	2 bits, 1 for the 32 LSBs and 1 for the 32 MSB bits

Errors Bus:	2 bits, 1 for Parity and 1 for System
Command/Byte Enable:	8 bits (0-3 @ 32bit, and 4-7@ 64bit Bus)
64MHz Control:	6 bits; (2) Enable/Running, (2) Present, (2) Ack/Req
Cache Size:	2 Bits
Interrupt bus:	4 bits [INTA#, INTB#, INTC#, INTD#]
JTAG Serial Bus:	5 Bits [JTAG Signal Description]
Power Supply:	+5, +3.3, +12, -12v, GND



PCI Connector Dimensions

RST# [input] Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state.

CLKRUN# [input] [Open Drain, Tri-state] Clock running is an optional signal used as an input for a device to determine the status of CLK.

M66EN [input] The 66MHZ_ENABLE pin indicates to a device whether the bus segment is operating at 66MHz or 33 MHz.

AD[31::00] [Tri-state] Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The Time Multiplexed Address and Data bus may exist as either 0 to 31 bits (32bits) or 0 to 63 bits (64bits) using the 64 bit expansion bus. Both the Address and Data line use the same bus, Address first then Data. 32 bit PCI may also use 64 bit addressing by using two address cycles; termed Dual Address Cycles (DAC), the low order address is sent first. Additional control bits are utilized once the bus is increased to 64 bits.

PME# The Power Management Event signal is an optional signal that can be used by a device to request a change in the device or system power state.

FRAME# [Sustained Tri-State] Cycle Frame is driven by the current master to indicate the beginning and duration of an access.

IRDY# [Sustained Tri-State] Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#.

TRDY# [Sustained Tri-State] Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.

STOP# [Sustained Tri-State] Stop indicates the current target is requesting the master to stop the current transaction.

LOCK# [Sustained Tri-State] Lock indicates an atomic operation to a bridge that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to a bridge that is not currently locked.

INT# [Open Drain] Interrupts on PCI are optional and are "level sensitive," asserted low (negative true).
--- INTA#, INTB#, INTC#, INTD#

PAR [Tri-state] Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after each address phase.

PERR# [Sustained Tri-State] Parity Error is only for the reporting of data parity errors. Two Parity lines are made available, one for the 32 bit bus width (bits 0 to 31) and an additional one for the 64 bit expansion (bits 32 to 63). Two

error bits; I assume, 1 for the LSB 32 bits and one for the upper 32 bits.

REQ# [Tri-state] Request indicates to the arbiter that this agent desires use of the bus. This is a point-to-point signal. Every master has its own REQ# line.

GNT# [Tri-state] Grant indicates to the agent that access to the bus has been granted. The GNT line is a point-to-point signal, each master has its own GNT# signal.

IDSEL [input] Initialization Device Select is used as a chip select during configuration read and write transactions.

DEVSEL# [Sustained Tri-State] Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access.

SERR# [Open Drain] System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error.

C/BE[3::0]# [Tri-state] Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command.

The specification defines both a Reset line and a Clock line. The Clock may be either 33MHz or 66MHz. I believe the 66MHz clock rate is only defined for the 64bit bus width.
A number of 'Handshake' lines exist to allow communication, i.e. Ready, and Acknowledge, see pin out above.

JTAG The JTAG interface is optional on the PCI bus. Add-in cards [expansion boards] that do not implement the JTAG Boundary Scan are required to connect [short] TDI and TDO (pins 4A and 4B) so the scan chain is not broken.

The pinout listings showing (+5 V or +3.3 V) mean: In a +5 volt system the pins are +5 volts, in a +3.3 volt system the pins are +3.3 volts.

64-Bit Bus Extension
PCI supports a high 32-bit bus, referred to as the 64-bit extension to the standard low 32-bit bus.
The high 32-bit extension for 64-bit devices needs an additional 39 signal pins: REQ64#, ACK64#, AD[63::32], C/BE[7::4]#, and PAR64.

PAR64 Parity bit, even parity. Parity generation is required by all PCI agents. PAR is stable and valid one clock after each address phase. PAR64 covers AD[63::32] and C/BE[7::4]# and has the same timing and function as the PAR bit. PAR64 requires a pull-up resistor when 32-bit transactions are used. When PAR64 is not used the line will float to the threshold level causing oscillation or high power drain through the input buffer.

REQ64# [Request-64] is bused to all devices on the system board (including PCI connector slots) that support a 64-bit data path and indicate that the Bus Master wants to make a 64-bit transfer. This signal has a single pull-up resistor on the system board.

ACK64# [Acknowledge 64-bit Transfer] is bused to all 64-bit devices and slots on the system board and pulled up with a single resistor located on the system board. ACK64# is actively driven by the device that has positively decoded its address as the target of the current access, indicating that the target is willing to transfer data using 64 bits.

AD[63::32], Note these are Tri-state lines and require a pull-up resistor during 32-bit transactions to keep the nets from floating. The upper Address and Data bits are multiplexed on the same pins and provide 32 additional bits. During an address phase (when using the DAC command and when REQ64# is asserted), the upper 32-bits of a 64-bit address are transferred; otherwise, these bits are reserved.

C/BE[7::4]#, [Bus Command and Byte Enable] Note these lines Tri-state and require a pull-up resistor during 32-bit transactions to keep the nets from floating. The Bus Command and Byte Enable lines are multiplexed on the same pins. During an address phase (when using the DAC command and when REQ64# is asserted), the actual bus command is transferred on C/BE[7::4]#; otherwise, these bits are reserved and indeterminate. During a data phase, C/BE[7::4]# are Byte Enables indicating which byte lanes carry meaningful data when a 64-bit transaction has been negotiated by the assertion of REQ64# and ACK64#.

Back to the main **PCI Bus** page, or the PCI Board Dimension page **PCI Card Size** or **Personal Computer bus** page.

PRSNT[1::2]# Add-in card Present
Note; PRSNT1 [B9] and PRSNT2 [B11] are present detect pins used just to detect the presence or absence of a PCI card. The PRSNT# pins relate only to the PCI connector.

Mother boards must decouple both of these pins individually to ground with 0.01 uF capacitors, because one or both of the pins also provide an AC return path. These pins may not be bused or connected to each other on the system board. Further the PRSNT# pins on the system board is optional. If the system board design accesses these pins to obtain add-in card information, each pin must have an appropriate pull-up resistor (of approximately 5 k ohm) on the system board.

PRSNT1#	PRSNT2#	Function
Open	Open	No add in card present
Ground	Open	Add in card present, 25 watts max
Open	Ground	Add in card present, 15 watts max
Ground	Ground	Add in card present, 7.5 watts max

Description of PCI pins and signal names'

The **Peripheral Component Interface** 'PCI' Bus was originally developed as a local bus expansion for the PC (ISA) bus. The PCI spec defines the Electrical requirements for the interface. No bus terminations are specified, the bus relies on signal reflection to achieve level threshold. The first version of the PCI bus ran at 33MHz with a 32 bit bus (133MBps), the current version runs at 66MHz with a 64 bit bus. The PCI bus operates either synchronously or asynchronously with the mother board bus rate. While operating asynchronously the bus will operate at any frequency from 66MHz down to (and including) 0Hz. Flow control is added to allow the bus to operate with slower devices on the bus, allowing the bus to operate at their speed. PCI is an unterminated bus, the signal relay on signal reflections to attain there final value.

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