5.1 GENISYS SERIAL COMMUNICATION PROTOCOL

5.1.1 General Message Format

The GENISYS protocol is a binary, byte oriented, serial, polling protocol in which all messages are framed by unique header/control and terminator bytes. It is normally transmitted and received by asynchronous serial communication controllers configured to process 8 bit characters with one start bit and one stop bit.

A typical GENISYS message is composed of a header/control character, a station address, data bytes (optional), two checksum bytes, and a terminator byte as shown in figure 5-1. Note that in the following paragraphs character (byte) values preceded by "$" are hexadecimal values.

CONTROL CHARACTER (HEADER)	STATION ADDRESS	DATA BYTE(S)	SECURITY CHECKSUM (CRC)	TERMINATOR CHARACTER

Figure 5-1. Typical GENISYS Protocol Message

5.1.1.1 Control Character

There are 13 possible header/control characters (bytes) in the GENISYS protocol ($F1 - $FE). Character $F0 is reserved for use as an "escape" character, $F6 is reserved for use as a message terminator, and $FF is not used. The basic GENISYS protocol defines 9 of the 23 available headers. Headers $F1 - $F3 are assigned to slave to master message while headers $F9 - $FE are assigned to master to slave messages.

It is possible for characters to appear in the data field which have bit patterns identical to the header/control and terminator characters. In order to preserve the uniqueness of the control and terminator characters, data bytes having values between $F0 $FF are sent as 2 byte sequences. The first byte in the sequence is always $F0 and the second byte in the sequence is (<byte value> - $F0). Whenever the character $F0 is received, it is always arithmetically added to the character which immediately follows to form the original data byte.

5.1.1.2 Station Address

In master to slave messages the station address is the address of the slave to which the message is sent. In slave to master messages the station address is the address of the slave sending the message. As there is only one master on any GENISYS protocol communication channel, and all messages are sent either to or from the master, the master requires no address. Valid station addresses are $01 to $$FF (1 to 255). The common mode message, transmitted from master to slave, may use $00 as a broadcast address.

5.1.1.3 Data Bytes

All data bytes are sent as a two byte pair. The first byte of the pair is a byte address while the second byte is the actual data. Theoretically, the range of valid data byte addresses is $00 to $DF (0 to 223 decimal). GENISYS 2000, however, normally only accepts byte addresses between $00 and $1F (and 31 decimal). Serial data bits 1 - 8 are packaged in the first byte, 9 - 16 in the second, etc. The lowest numbered bit in a data byte is the least significant bit.

5.1.1.4 Security Checksum

All GENISYS messages except the slave to master acknowledge message and the master to slave non-secure poll message include a two-byte CRC-16 checksum. The standard CRC-16 generator polynomial X(16) + X(15) + X(2) + 1 is used. This checksum is calculated before any escape characters are inserted and includes all characters in the message except the message terminator.

5.1.2 BASIC GENISYS PROTOCOL MASTER TO SLAVE MESSAGES

5.1.2.1 Common Control Message ($F9)

The common control message is used to deliver the same data to all GENISYS units on the communication channel at the same time. Common control mode must have previously been enabled for all slaves to receive the common control message by setting the common control mode flag in the slave configuration ($E0) control byte. This message is normally sent only by GENISYS master protocol handlers used in US&S computer-based CTC control machines. It is not implemented in the GENISYS 2000 master port handler. The slave units receiving the common control message are not permitted to respond.

5.1.2.2 Acknowledge and Poll Message ($FA)

The acknowledge and poll message is generated to acknowledge data successfully received from a slave. All data received from a slave must be acknowledged by the master. Unacknowledged data is repeated by the slave when subsequently addressed by the master until the data is successfully acknowledged. Valid responses include:

1. Acknowledge ($F1)
2. Data ($F2)

5.1.2.3 Poll Message ($FB)

The poll message is generated to allow the addressed slave to return any new or changed data from its database. This message has both secure and non-secure formats. The secure format, which includes a CRC-16 checksum, improves data security while the shorter non-secure form is slightly more efficient. The secure form is normally recommended. Valid response include:

1. Acknowledge ($F1)
2. Data ($F2)

5.1.2.4 Control Data Message ($FC)

The control data message is generated to pass changed or new data from the master to the slave. If the checkback control sequence is enabled the only valid response is slave checkback ($F3). If checkback is disabled valid responses included:

1. Acknowledge ($F1)
2. Data ($F2)

5.1.2.5 Indication Recall (Master Recall) Message ($FD)

The indication recall message is generated to cause the slave to respond with its entire indication database. This message is normally sent on protocol startup and any time communication is restored after an outage. It may also be sent periodically to verify the integrity of the master's database. The only valid response is a full indication data message ($F2).

5.1.2.6 Control Execute Message ($FE)

This message is generated to cause execution of previously delivered control data. It is valid only if the checkback control sequence has been previously enabled for the addressed slave and it immediately follows a valid control data message. The checkback control sequence is enabled by setting the checkback controls flag in the slave configuration control byte ($E0). Employing the checkback control sequence improves the security of data passed from master to slave. Valid responses include:

1. Acknowledge ($F1)
2. Data ($F2)

5.1.3 Basic GENISYS Protocol Slave to Master Messages

5.1.3.1 Acknowledge Message ($F1)

The acknowledge message is the default responds for a slave which receives a message from the master unit. It is sent when the slave has no data to return to the master. It is a non-secure message and includes no CRC-16 checksum. Loss or misinterpretation of a slave acknowledge message does not comprise data security.

5.1.3.2 Indication Data Message ($F2)

The indication data message is generated by a slave to deliver new or changed data to the master is in response to acknowledge, poll, control (non-checkback mode), recall or control execute (checkback mode) messages from the master.

5.1.3.3 Control Checkback Message ($F3)

A control checkback message is generated in response to a control data message received from the master when checkback control mode is enabled. The control checkback message contains all control data bytes in the control data message exactly as received from the master. This control data image is saved and executed if a control executed message is the next message form the master received by the slave. If the control checkback sequence fails, the control data is discarded and the entire sequence must be repeated.

5.1.4 GENISYS Master Protocol Drivers Operation

When the GENISYS master protocol driver is started, shortly after the GENISYS 2000 unit initialization is completed, a recall message is sent to each of the slave addresses defined in the MASTER section of the GENISYS 2000 application program. Each time the master protocol driver addresses a slave, it waits a predetermined time (the no-response time out) for a response. When the first no-response timer is aborted and a message timer is started. If a valid terminator character is received before the message timer expires, the response is immediately processed and the next communication cycle is started. A good response has a valid header/control character, is from the addressed slave, has a valid CRC-16 checksum (if applicable), has a valid terminator and a valid length.

The GENISYS master protocol driver will continue to address recall messages to each defined slave in turn until a valid response is received from each slave. As a complete indication data response is received from each slave, the slave will be marked active (SLAVE.ON.nn set), a control data message will be sent to the responding slave, and normal polling will begin.

Whenever a slave does not respond when addressed by the master or when an error is detected in the response, the station will be addressed again (usually with the same message). After at least 3 consecutive failed attempts to communicate with a slave, the slave will be marked failed (SLAVE.ON.nn cleared). Whenever retries are exhausted for a control data message, the message is discarded. When reliable communication is again established with the slave, the CURRENT control database for that slave is delivered. Failed slaves are always addressed with recall messages until they again respond correctly unless there are new control data changes to be sent. New control data changes are sent to failed slaves once. Messages sent to failed slaves are not retried.

5.1.5 GENISYS Slave Protocol Driver Operation

The GENISYS slave protocol driver constantly "listens" for commands addressed to it by the GENISYS master. A GENISYS protocol slave may never transmit a message unless it receives a properly addressed, valid message from the master. When the GENISYS slave protocol driver receives a valid message from the master it sets SERIAL.MASTER.ON indicating that communication has been established with the master. It then generates a response which is appropriate for the received message. GENISYS slaves respond to all messages addressed to them except common control messages. SERIAL.MASTER.ON remains set unless successful communication with the master has not occurred for 5 minutes (this time is user adjustable).

NOTE:

If dualport operation is initiated, SERIAL.SLAVE communication is indicated using SER1.MASTER.ON and SERIAL.SLAVE2 communication is indicated using SER2.MASTER.ON.

5.1.6 GENISYS Configuration Control Bytes

The GENISYS protocol reserves control byte addresses $E0 - $FF for configuration control purposes. At the present time, only one byte ($E0) is used. GENISYS configuration control bytes are transferred as ordinary control and indication bytes within control data ($FC) and indication data ($F2) messages.

Using the $E0 byte, the GENISYS master configures its connected slaves and they report their internal status. The bits are defined as follows:

0 - Database complete
1 - Use checkback control delivery
2 - Respond to secure poll only
3 - Enable common control message processing
4 - Reserved
5 - Reserved
6 - Reserved
7 - Reserved

5.1.7 Detailed Message Formats for Master to Slave Messages

This section describes the format for each GENISYS protocol message which is sent from master to slave. All byte values and value ranges are specified in hexadecimal. Message fields which may be repeated within a message are identified by placing square brackets [ ] around the description of the repeated field.

5.1.7.1 Common Control Message

Byte	Range	Description
1	$F9	Message header
2	$00-$FF	Slave address
	$00-$01	[Control byte address]
	$00-$FF	[Control byte data]
n-2	$00-$FF	CRC-16 low byte
n-1	$00-$FF	CRC-16 high byte
n	$F6	End of message

5.1.7.2 Acknowledge and Poll Message

Byte	Range	Description
1	$FA	Message header
2	$01-$FF	Slave address
3	$00-$FF	CRC-16 low byte
4	$00-$FF	CRC-16 high byte
5	$F6	End of message

5.1.7.3 Poll Message

Secure format:

Byte	Range	Description
1	$FB	Message header
2	$01-$FF	Slave address
3	$00-$FF	CRC-16 low byte
4	$00-$FF	CRC-16 high byte
5	$F6	End of message

Non-secure format:

Byte	Range	Description
1	$FB	Message header
2	$01-$FF	Slave address
3	$F6	End of message

5.1.7.4 Control Message

Byte	Range	Description
1	$FC	Message header
2	$01-$FF	Slave address
	$00-$1F	[Control byte address]
	$00-$FF	[Control byte data]
n-2	$00-$FF	CRC-16 low byte
n-1	$00-$FF	CRC-16 high byte
n	$F6	End of message

5.1.7.5 Recall Message

Byte	Range	Description
1	$FD	Message header
2	$01-$FF	Slave address
3	$00-$FF	CRC-16 low byte
4	$00-$FF	CRC-16 high byte
5	$F6	End of message

5.1.7.6 Control Execute Message

Byte	Range	Description
1	$FE	Message header
2	$01-$FF	Slave address
3	$00-$FF	CRC-16 low byte
4	$00-$FF	CRC-16 high byte
5	$F6	End of message

5.1.8 Detailed Message Formats for Slave to Master Messages

This section describes the format for each GENISYS protocol message which is sent from slave to master. All byte values and value ranges are specified in hexadecimal. Message fields which may be repeated within a message are identified by placing square brackets [ ] around the description of the repeated field.

5.1.8.1 Acknowledge Message

Byte	Range	Description
1	$F1	Message header
2	$01-$FF	Slave address
3	$F6	End of message

5.1.8.2 Indication Data Message

Byte	Range	Description
1	$F2	Message header
2	$01-$FF	Slave address
	$00-$1F	[Indication byte address]
	$00-$FF	[Indication byte data]
n-2	$00-$FF	CRC-16 low byte
n-1	$00-$FF	CRC-16 high byte
n	$F6	End of message

5.1.8.3 Control Data Checkback Message

Byte	Range	Description
1	$F3	Message header
2	$01-$FF	Slave address
	$00-$1F	[Control byte address]
	$00-$FF	[Control byte data]
n-2	$00-$FF	CRC-16 low byte
n-1	$00-$FF	CRC-16 high byte
n	$F6	End of message

5.1.9 Control Character Summary

Control Character	Function
$F0	Escape
$F1	Acknowledge master header
$F2	Indication data header
$F3	Control data checkback header
$F4	Reserved
$F5	Reserved
$F6	Message terminator
$F7	Reserved
$F8	Reserved
$F9	Common control data header
$FA	Acknowledge indication and poll header
$FB	Poll header
$FC	Control data header
$FD	Recall header
$FE	Execute controls header
$FF	Reserved