#### KICAD STYLE GUIDE

A brief style guide for KiCad and general electronics design.

# **Project**

## Creating KiCad Project

- 1) KiCad projects should be created in their own folder (usually within the Hardware folder of a project). Note that KiCad will create the project folder for you.
- 2) Once KiCad creates the project, Add two more folders: One labeled "PDFs" and one labeled "Gerbers".

#### **Schematic**

# Starting Schematic Capture

- 1) When starting your schematic, start with the *default\_layout.kicad\_wks* worksheet at size A4. Increase size of paper incrementally as need be up to maximum size A2. Anything larger than A2 should be done as a hierarchical, multi-sheet schematic.
- 2) Set dimensions to use imperial units.
- 3) Use only Grid Select sizes of 100 mil, 50 mil, or 25 mil.

### Schematic Capture

- 1) Use "Up Arrow" symbol for all voltage rails as shown in Figure 1.
- 2) When dealing with voltages such as 3.3 Vdc, show them on the schematic as 3V3. Voltages of 5.0 Vdc should be shown as just 5V. **Figure 1**.
- 3) The same voltage level coming from multiple sources (provided isolation between those levels is required) should be named like the following: Ex) Two 5 Vdc sources, isolation required between sources. One source is the system 5 Vdc, the other is the UART 5 Vdc. The system 5 Vdc should be labeled +5V. The UART 5 Vdc should be labeled +5V\_UART. **Figure 1**.
- 4) Connections to/from a pin on a part should extend at least 50 mil from that part before terminating into the connecting part. **Figure 1**. Note: Shown as the green wire in **Figure 1**.
- 5) The standard GND symbol should be used for all system grounding unless a multiple grounding scheme is needed. **Figure 1**.

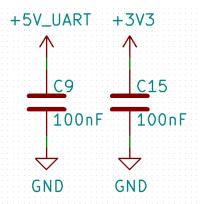


Figure 1 - Basic KiCad Source Labeling and Minimum Connection Distance

- 6) Connections to sources should have positive power on the top and ground/negative connections on the bottom. **Figure 2**.
- 7) No-connects should be labeled with the no-connect symbol (x) directly on their pin. Figure 2.
- 8) All individual signal labels (global labels, hierarchal labels, and net names) should be in size 1.194mm text. **Figure 2**.
- 9) All global labels and hierarchal labels should be I/O shapes associated with the block they are going to/coming from. Ex) **Figure 2** shows a JTAGICE3-SWD connector. The signals SWDCLK and SWDIO are outputs from the connector into the microcontroller (not pictured), they are therefore labeled as outputs. SWO is an input to the connector from the microcontroller and is also labeled as an input. Likewise, nRST is a bidirectional signal and is labeled as such.
- 10) All active low signals should be labeled with a bar across the signal name. See RST in Figure 2. Note: In KiCad you can make the bar by putting a tilde (~) in front of the signal name like so: ~RST.

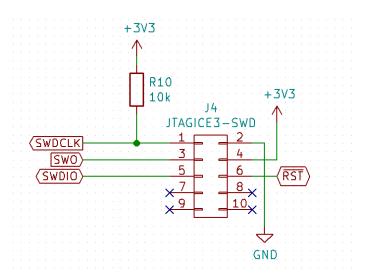


Figure 2 - Source Locations and Connector Labels

- 11) All major nets should have net names or labels. Nets that terminate with a continuous wire connection should have a net name. **Figure** 3 is an example of using net names as each net pictured terminates using a continuous wire, no jumps are necessary. Nets that do not terminate (i.e. jump around the board) should have a global or hierarchal labels. Single sheet schematics should use global labels rather than hierarchal labels. **Figure 2** is an example of global labels being used to label nets as these nets are not continuous with a single green wire.
- 12) Local net names should all line up on a part. There should be some space between the part's pin number and the net name. **Figure 3** shows aligned net names with sufficient space before the part's pin number.
- 13) Nets with terminating resistors should be labeled with an extra \_R on the terminating side of the resistor. Another net name or label should follow the other side of the resistor **Figure 3** shows proper labeling for a terminating resistor on the MCCK net.

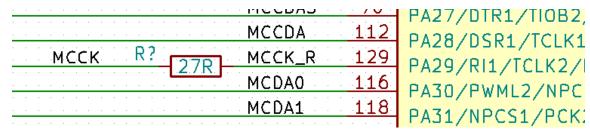


Figure 3 – Local Net Naming and Terminating Resistor

- 14) Resistors, capacitors, and inductors should all be the "normal" sized symbol, not the small sized symbol. Diodes should be "foreground filled" so they appear opaque. Integrated circuits should be "background filled". **Figure 4**.
- 15) Components should have their reference designators above their values. Horizontal resistors should have their values inside the resistor. All capacitors and inductors must specify Farads or Heneries for their value: Ex) 4.7uF or 2.2uH. Resistors under 1 kOhm should specify their value ending in "R": Ex) 150R. Resistors over 1 kOhm should specify their value ending in "k": Ex) 10k. Figure 4.
- 16) Junctions should connect no more than three signals. Ex) **Figure 4** junction between +3V3, R22, and C41 is connected using two separate junctions to connect all three nets rather than one.

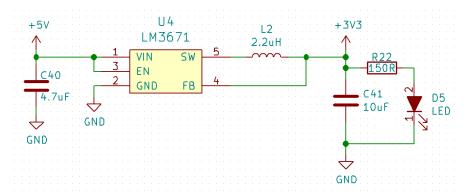


Figure 4 - Buck Regulator Schematic

17) Bypass/Decoupling capacitors should be shown as directly connected to their parts positive or negative voltage rails. Bypass/Decoupling capacitors should not be shown as connected directly to ground pins on an IC. **Figure 5** 

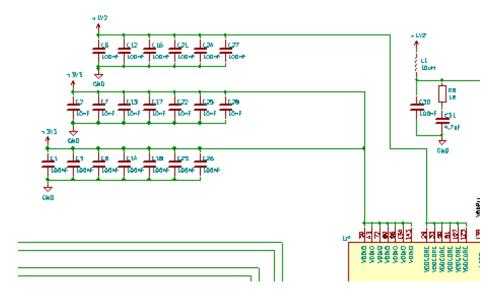


Figure 5 - Bypass/Decoupling Capacitor Placement

18) Busses should be labeled with a Global Label. All bus net names should be labeled at both entrance and exit to/from a bus. All bus entrances/exits should "step" down 50 mil. Figure 6.

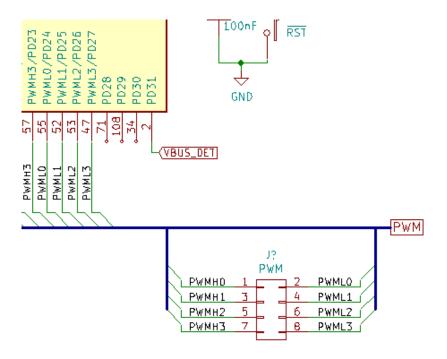


Figure 6 - Bus Labeling, Entry, and Exit

19) Differential pairs should be labeled with a "+" or a "-" at the end of the net name or label. **Figure 7** shows a two differential Ethernet pairs properly labeled. Note: the "+" or "-" character must always be the last character in the name or label of a differential pair. Differential pairs with terminating resistors should be labeled as "\_R+" or "\_R-".

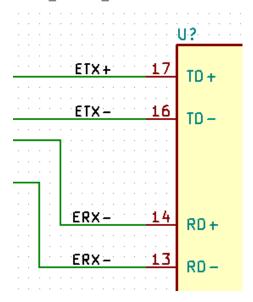


Figure 7 - Labeling Differential Pairs

20) Non-populated parts should be enclosed in a graphic rectangle and labeled "DNP" per Figure 8.

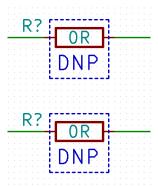


Figure 8 - Non-populated Part Labeling

- 21) Spacing between nets on the same function block should be 100 mil as shown in the right side of **Figure 9**.
- 22) Notes and TODOs should be added in 1.524 size text as shown in Figure 9.

TODO: CHECK THESE CAPACITOR VALUES. THEY SEEM A BIT HIGH. +5V\_UART +3V3 100nF 100nF GND GND +373 +5V\_UART U1 R5 TXS0102 10k VCCB VCCA UART\_TXD В1 A1 UART\_RXD B2 A2 GND UO\_TXD UO\_RXD

Figure 9 - Net Spacing and Text

Library Management

1) TODO

**Creating Schematic Symbols** 

1) TODO

# **Bill of Materials**

**BOM Generation** 

1) TODO

**BOM Format** 

1) TODO

# **Board Layout**

Starting Board Layout