Avaliando o uso de memórias HMC em Sistemas Embarcados

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Roteiro

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- ❏ Objetivos
- ❏ Metodologia
- ❏ Andamento e Resultados Preliminares
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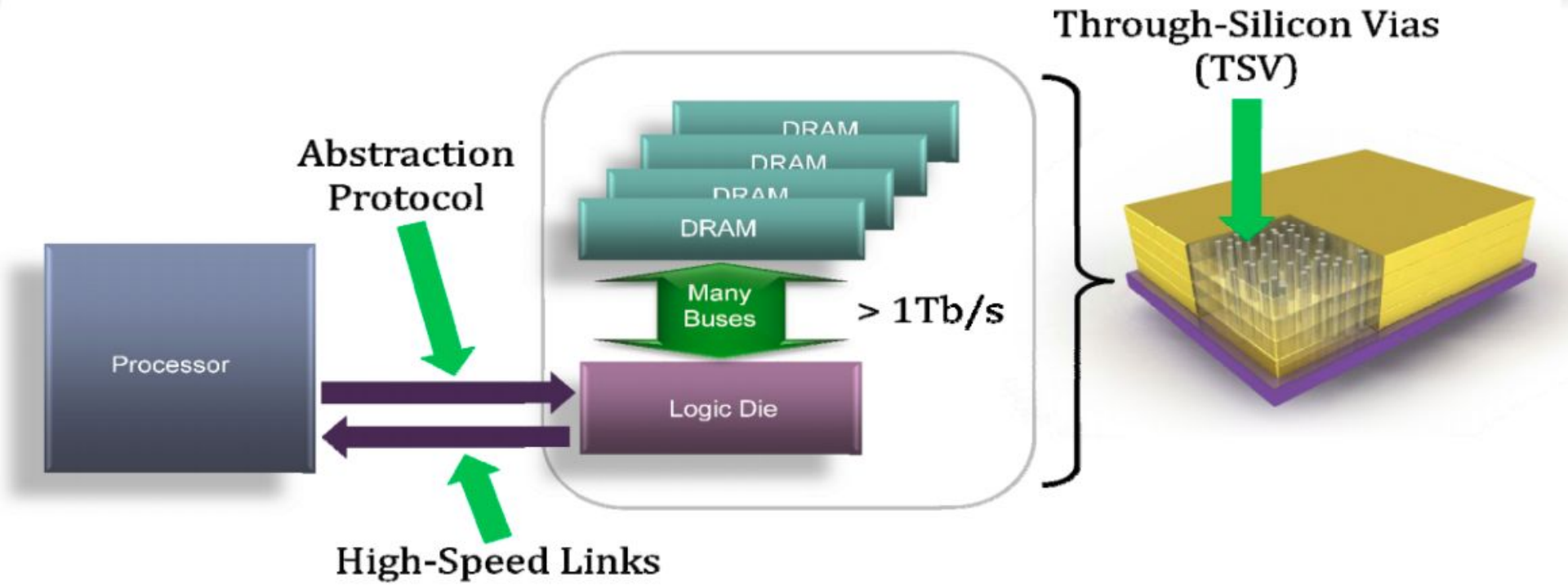
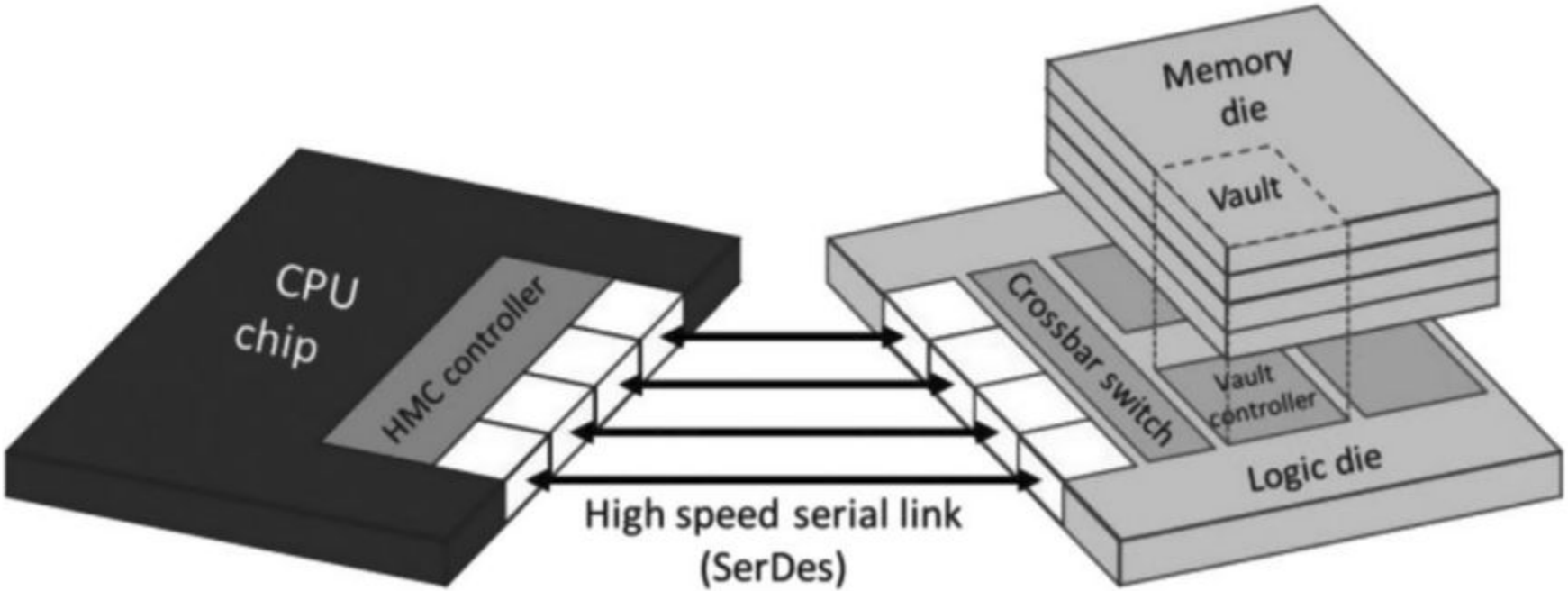
Introdução



Jeddeloh and Keeth, 2012

Introdução

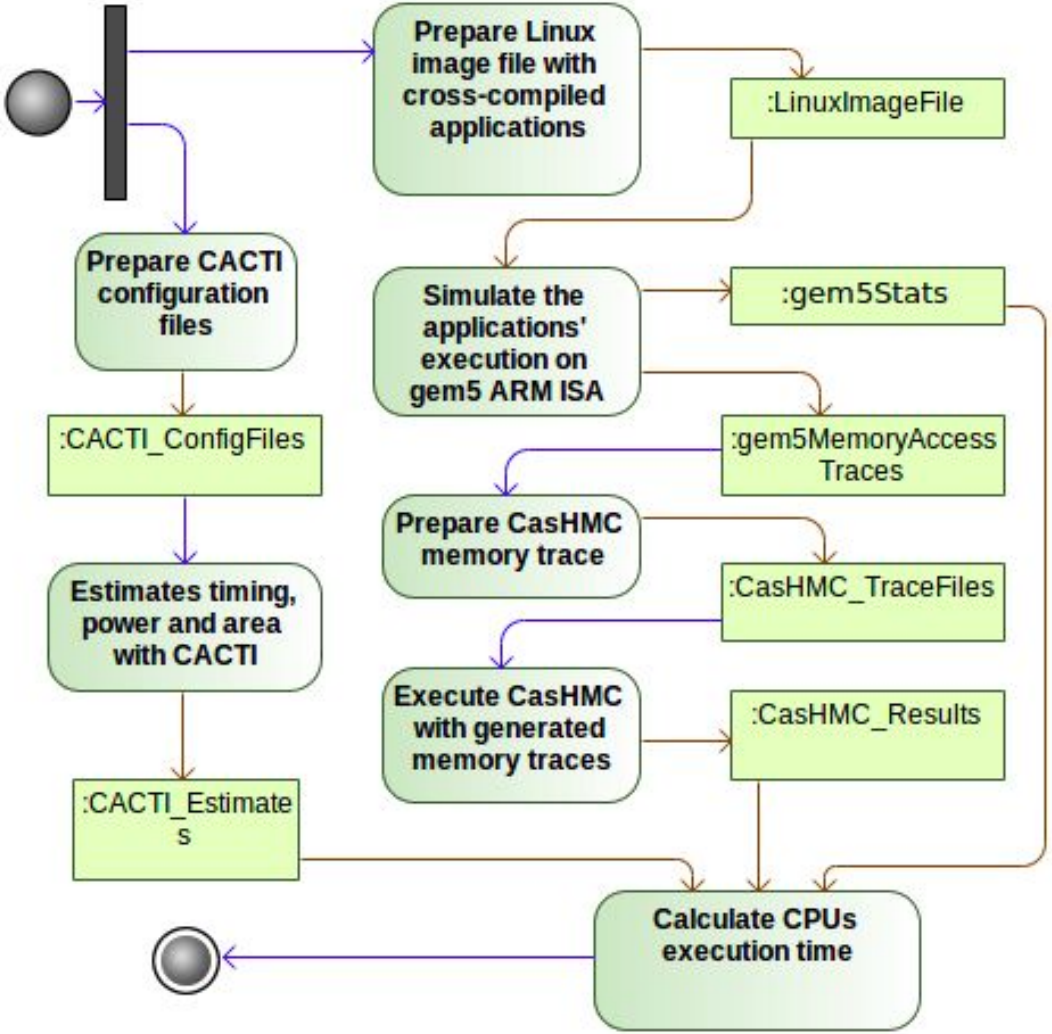


Jeon and Chung 2017

Objetivos

- ❏ Avaliar o uso de HMC como Memória Principal
- ❏ Verificar a possibilidade de retirar o nível L2 de cache

Metodologia



gem5 Stats

stats.txt

```
---------- Begin Simulation Statistics ----------
sim_seconds                                     0.163511
sim_ticks                                  163510806000
final_tick                                 13064937930500
simulation (restored from checkpoints and never reset)
sim_freq                                   1000000000000
host_inst_rate                                   429969
host_op_rate                                     488749
op/s)
host_tick_rate                                 120902076
host_mem_usage                                   2675016
host_seconds                                     1352.42
sim_insts                                      581500589
sim_ops                                        660995104
simulated
system.voltage_domain.voltage                          1
system.clk_domain.clock                             1000
system.mem_ctrls.pwrStateResidencyTicks::UNDEFINED 13064937930500
various power states
system.mem_ctrls.bytes_read::cpu0.dtb.walker        17452
system.mem_ctrls.bytes_read::cpu0.itb.walker         5472
system.mem_ctrls.bytes_read::cpu0.inst      209090368
system.mem_ctrls.bytes_read::cpu0.data       16885184
system.mem_ctrls.bytes_read::cpu1.dtb.walker        63016
system.mem_ctrls.bytes_read::cpu1.itb.walker         3280
system.mem_ctrls.bytes_read::cpu1.inst      275864448
system.mem_ctrls.bytes_read::cpu1.data       26516288
system.mem_ctrls.bytes_read::cpu2.dtb.walker      1351900
system.mem_ctrls.bytes_read::cpu2.itb.walker        32396
system.mem_ctrls.bytes_read::cpu2.inst       60122880
system.mem_ctrls.bytes_read::cpu2.data       80921344
system.mem_ctrls.bytes_read::cpu3.dtb.walker         6024
system.mem_ctrls.bytes_read::cpu3.itb.walker         3004
system.mem_ctrls.bytes_read::cpu3.inst       12210368
system.mem_ctrls.bytes_read::cpu3.data        6004800
system.mem_ctrls.bytes_read::realview.ide        24000
```

Memory Access Trace (gem5)

```
12900997345500: system.terminal: attach terminal 0
12900997346000: system.mem_ctrls: IFetch from cpu2.inst of size 64 on address 0xfff9cec0 C
12900997346000: system.mem_ctrls: 00000000  10 01 21 ee 0e f0 a0 e1  10 01 30 ee 0e f0 a0 e1     !n p a  0n p a
12900997346000: system.mem_ctrls: 00000010  10 01 31 ee 0e f0 a0 e1  10 01 40 ee 0e f0 a0 e1     1n p a  @n p a
12900997346000: system.mem_ctrls: 00000020  10 01 41 ee 0e f0 a0 e1  10 01 42 ee 0e f0 a0 e1     An p a  Bn p a
12900997346000: system.mem_ctrls: 00000030  10 01 43 ee 0e f0 a0 e1  10 01 50 ee 0e f0 a0 e1     Cn p a  Pn p a
12900997346500: system.mem_ctrls: IFetch from cpu2.inst of size 64 on address 0xfff9ccc0 C
12900997346500: system.mem_ctrls: 00000000  d0 00 cd e1 d8 20 cd e1  88 00 00 eb 14 d0 8d e2   P MaX Ma   k P b
12900997346500: system.mem_ctrls: 00000010  04 f0 9d e4 04 e0 2d e5  14 d0 4d e2 0d 20 a0 e1    p d `-e PMb   a
12900997346500: system.mem_ctrls: 00000020  02 30 a0 e3 95 ff ff eb  d0 00 cd e1 d8 20 cd e1    0 c   kP MaX Ma
12900997346500: system.mem_ctrls: 00000030  7c 00 00 eb 14 d0 8d e2  04 f0 9d e4 04 e0 2d e5   |  k P b p d `-e
12900997347000: system.mem_ctrls: Read from cpu2.data of size 64 on address 0x81946d00 C
12900997347000: system.mem_ctrls: 00000000  b4 fe ff 7e 00 00 00 00  0c 00 00 00 c0 8c 00 00   4~ ~        @
12900997347000: system.mem_ctrls: 00000010  00 00 00 00 00 00 00 00  00 00 00 00 00 00 00 00
12900997347000: system.mem_ctrls: 00000020  00 00 00 00 78 8e 00 00  00 00 00 00 b4 fe ff 7e       x       4~ ~
12900997347000: system.mem_ctrls: 00000030  02 00 00 00 00 00 00 00  5c 87 00 00 78 fd ff 7e           \   x} ~
12900997348500: system.mem_ctrls: IFetch from cpu2.inst of size 64 on address 0xfff9ce40 C
12900997348500: system.mem_ctrls: 00000000  01 00 a0 e3 6b fe ff eb  14 d0 8d e2 f0 8f bd e8      ck~ k P bp =h
12900997348500: system.mem_ctrls: 00000010  01 00 a0 e3 67 fe ff eb  c4 ff ff ea 0c a0 a0 e3      cg~ kD  j    c
12900997348500: system.mem_ctrls: 00000020  9a 94 24 e0 80 02 9d e9  08 60 94 e5 02 00 49 e2     $`    i ` e  Ib
12900997348500: system.mem_ctrls: 00000030  08 10 87 e2 36 ff 2f e1  08 00 a0 e1 14 fe ff eb      b6 /a   a ~ k
12900997349500: system.mem_ctrls: IFetch from cpu2.inst of size 64 on address 0xfff9c6c0 C
12900997349500: system.mem_ctrls: 00000000  08 ca 8c e2 24 fd bc e5  00 c6 8f e2 08 ca 8c e2    J b$}<e F b J b
12900997349500: system.mem_ctrls: 00000010  1c fd bc e5 00 c6 8f e2  08 ca 8c e2 14 fd bc e5    }<e F b J b }<e
12900997349500: system.mem_ctrls: 00000020  00 b0 a0 e3 00 e0 a0 e3  04 10 9d e4 0d 20 a0 e1    0 c ` c   d   a
12900997349500: system.mem_ctrls: 00000030  04 20 2d e5 04 00 2d e5  10 c0 9f e5 04 c0 2d e5     -e  -e @ e @-e
12900997350500: system.mem_ctrls: Read from cpu2.data of size 64 on address 0xef7293c0 C
12900997350500: system.mem_ctrls: 00000000  dc 85 00 00 dc 85 00 00  dc 85 00 00 dc 85 00 00   \   \   \   \
12900997350500: system.mem_ctrls: 00000010  dc 85 00 00 dc 85 00 00  dc 85 00 00 dc 85 00 00   \   \   \   \
12900997350500: system.mem_ctrls: 00000020  dc 85 00 00 dc 85 00 00  dc 85 00 00 a1 c6 f2 76   \   \   \   !Frv
```

Trace para CasHMC

```
5216   288787 0x817a5600 READ
5217   288827 0xef075500 READ
5218   288863 0xef0754c0 READ
5219   288959 0x817a5900 READ
5220   288959 0x817ad900 WRITE
5221   289106 0x817a5940 READ
5222   289127 0x80074800 READ
5223   289130 0x800cdec0 READ
5224   289130 0x8072dec0 WRITE
5225   289156 0x8004fb00 READ
5226   289169 0x8004fb40 READ
5227   289174 0x81790c00 READ
5228   289176 0x8004f880 READ
5229   289185 0x8004f8c0 READ
5230   289187 0x80074a00 READ
5231   289199 0x800cdbc0 READ
5232   289205 0x80043480 READ
5233   289217 0x817a58c0 READ
5234   289220 0x817a5240 READ
5235   289231 0x817a5200 READ
5236   289249 0x800cdc00 READ
5237   289261 0x80730780 READ
5238   289276 0x80043140 READ
5239   289291 0x817a5280 READ
5240   289296 0x8022f440 READ
5241   289301 0x8022f480 READ
```

Resultados CasHMC

```
************************************************************
*                    CasHMC version 1.3                    *
*                     result log file                      *
*           Date : 2017/08/16      Time : 21:06:08         *
************************************************************

- Trace type : file
- Trace file : /home/betemps/GEM5_Dados/HMC_Work/NO-L2-L1_8KB_memory-trace.trc

  ============= CasHMC statistic result =============

  Elapsed epoch : 328
  Elapsed clock : 328598098

        HMC bandwidth : 1.61563 GB/s  (Considered only data size)
       Link bandwidth : 7.58772 GB/s  (Included flow packet)
 Effec Link bandwidth : 1.61563 GB/s  (Data bandwidth regardless of packet header and tail)
    Link utilization : 1.58077 %     (Max link bandwidth : 480 GB/S)

    Tran latency mean : 40.6991 ns
                 std  : 6.87714 ns
                 max  : 245 ns
                 min  : 16 ns
    Link latency mean : 33.3515 ns
                 std  : 6.81579 ns
                 max  : 237 ns
                 min  : 9 ns
   Vault latency mean : 22.7676 ns
                 std  : 2.41262 ns
                 max  : 103.2 ns
                 min  : 4 ns
   Retry latency mean : 4 ns
                 std  : 0 ns
                 max  : 4 ns
                 min  : 4 ns
```

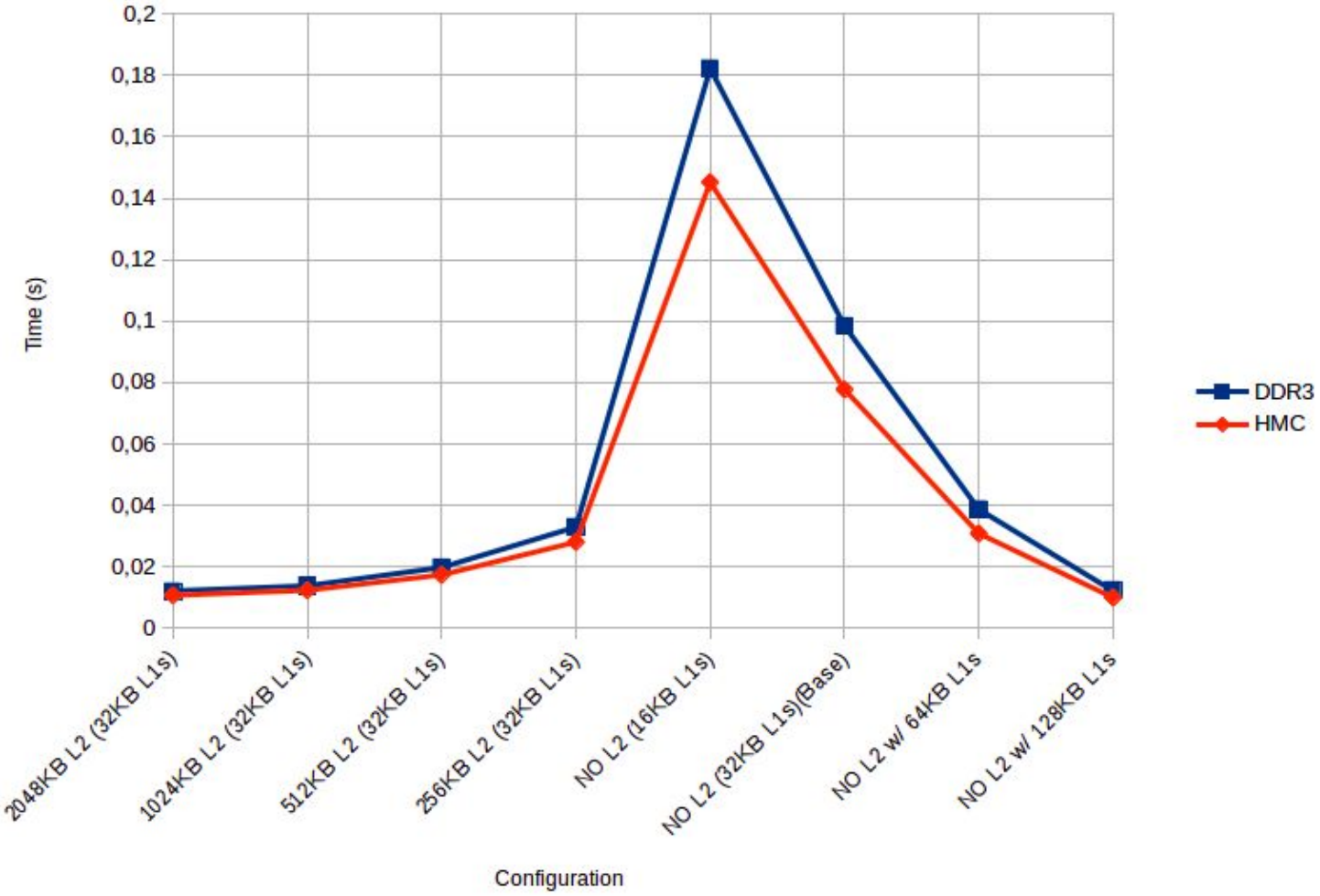
Andamento e Resultados Preliminares

- Problemas para geração de estimativas de energia e de área para HMC
- Equações para cálculo de Miss Penalty, MSC, e Tempo de Execução (por CPU)

A	B	C	D	E	K	L	M	N
	2048KB L2 (32KB L1s)	1024KB L2 (32KB L1s)	512KB L2 (32KB L1s)	256KB L2 (32KB L1s)	*NO L2 (16KB L1s)*	*NO L2 (32KB L1s)*	NO L2 w/ 64KB L1s	NO L2 w/ 128KB L1s
CPU0 Exec Time (DDR3)	0,0119732	0,0138618	0,0198433	0,0329998	0,1822261	0,0984123	0,0387309	0,012469
CPU1 Exec Time (DDR3)	0,0138811	0,0154747	0,0213655	0,0344403	0,2433502	0,1229693	0,0269515	0,0106473
CPU2 Exec Time (DDR3)	0,0115065	0,0134672	0,0194709	0,0326474	0,1136869	0,0636246	0,0370876	0,0231893
CPU3 Exec Time (DDR3)	0,0094127	0,0116971	0,0178004	0,0310663	0,0148242	0,0094445	0,0048746	0,00318
CPU0 Exec Time (HMC)	0,0107622	0,0124038	0,0174185	0,0281099	0,1451912	0,0777682	0,0308792	0,0100052
CPU1 Exec Time (HMC)	0,01267	0,0140167	0,0189407	0,0295505	0,1938927	0,0971739	0,0214877	0,0085434
CPU2 Exec Time (HMC)	0,0102955	0,0120092	0,0170462	0,0277575	0,0905817	0,050278	0,029569	0,0186073
CPU3 Exec Time (HMC)	0,0082017	0,0102391	0,0153756	0,0261765	0,0118114	0,0074633	0,0038864	0,0025517

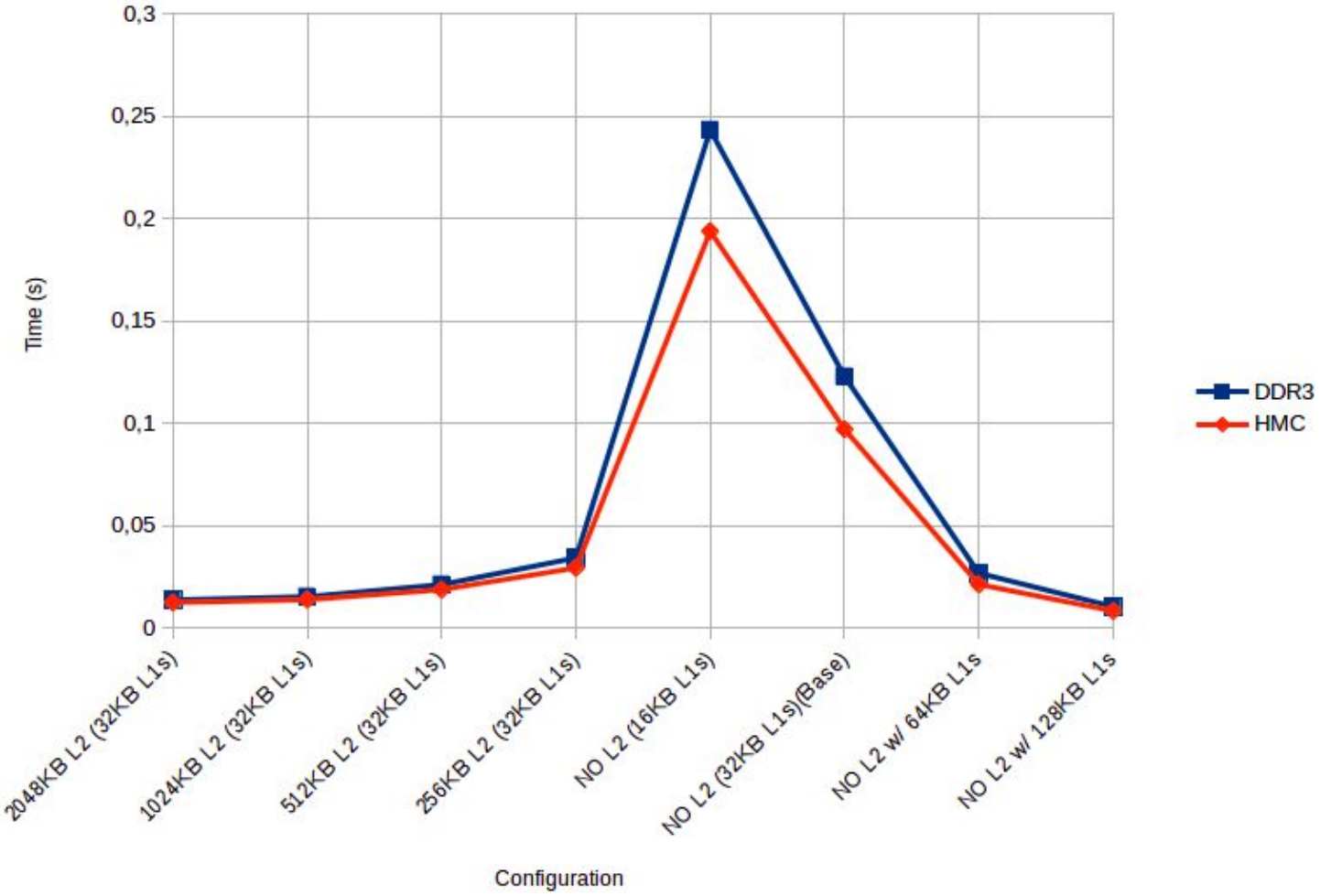
basicmath

(CPU0)



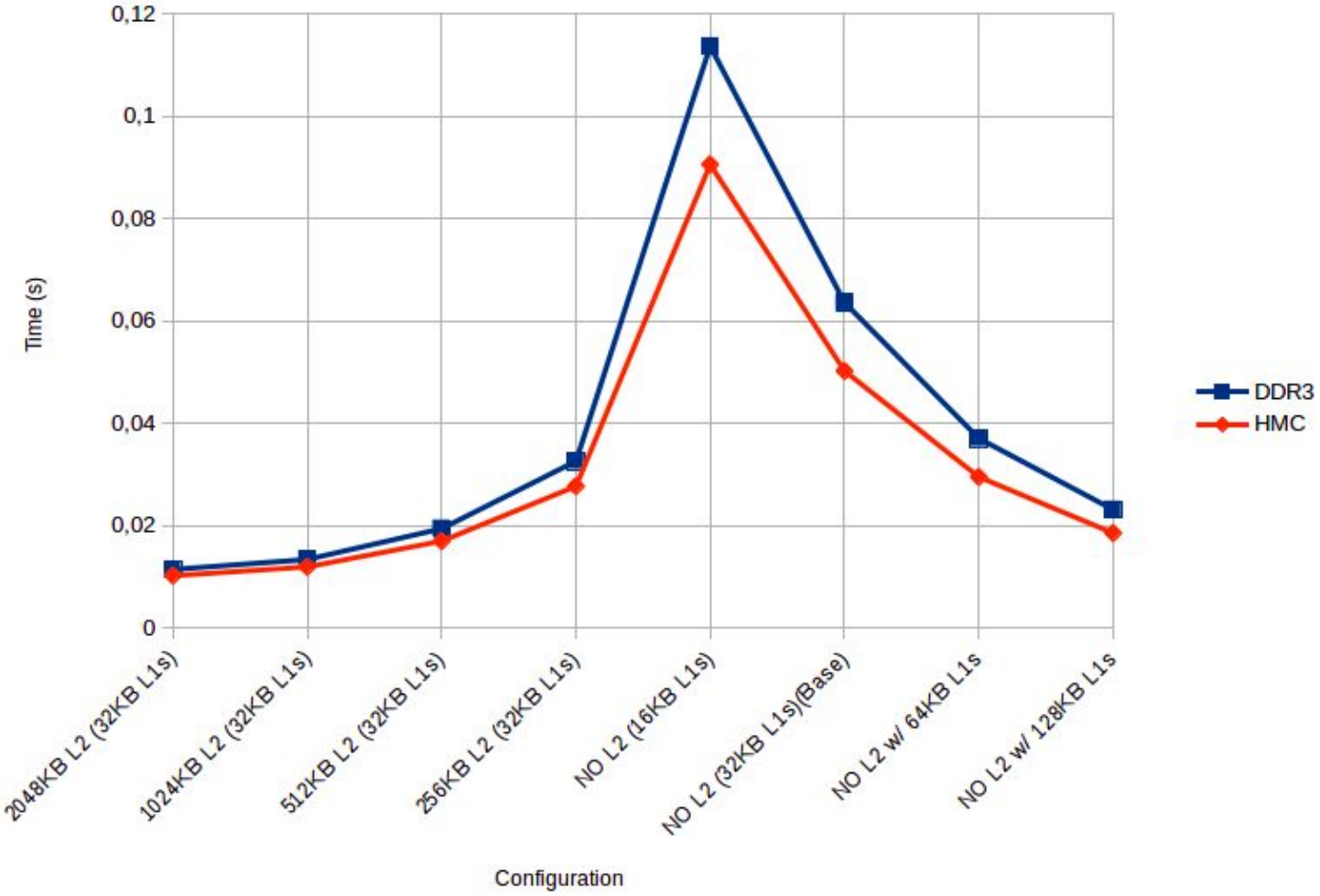
patricia

(CPU1)



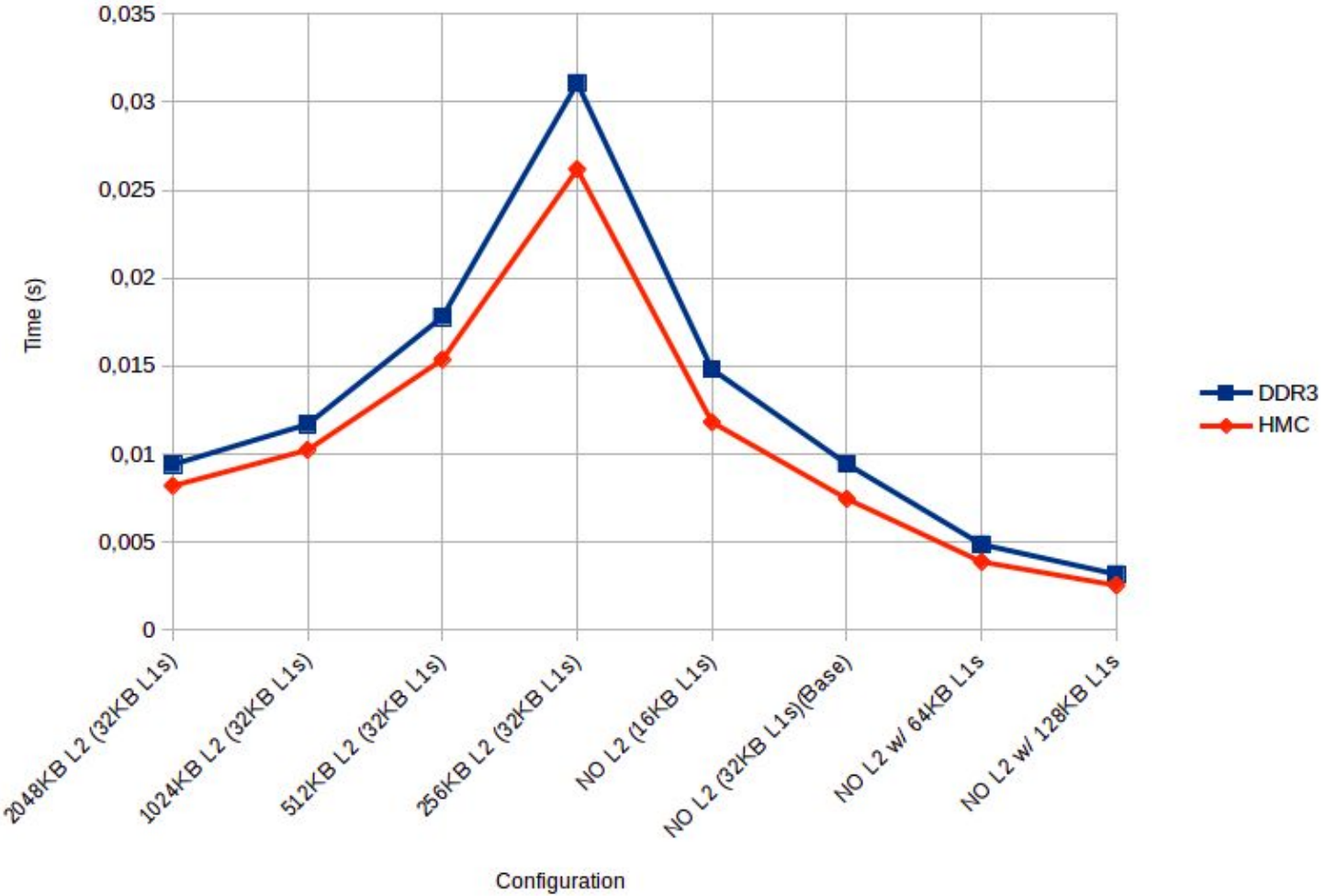
typeset

(CPU2)



blowfish (enc.)

(CPU3)



Andamento e Resultados Preliminares

- Aplicações pequenas → demandam pouca cache
- Ajuste nos tamanhos de cache L1i&d e L2

Ajuste das Configurações dos Experimentos

#	L1i&d Size (KB)	L2 Size (KB)	MM Type	#	L1i&d Size (KB)	L2 Size (KB)	MM Type
1	8	2048 512	DDR	9	8	512	HMC
2	8	1024 256	DDR	10	8	256	HMC
3	32 8	512 128	DDR	11	8	128	HMC
4	8	256 64	DDR	12	8	64	HMC
5	8	-	DDR	13	8	-	HMC
6	64 16	-	DDR	14	16	-	HMC
7	128 32	-	DDR	15	32	-	HMC
8	64	-	DDR	16	64	-	HMC

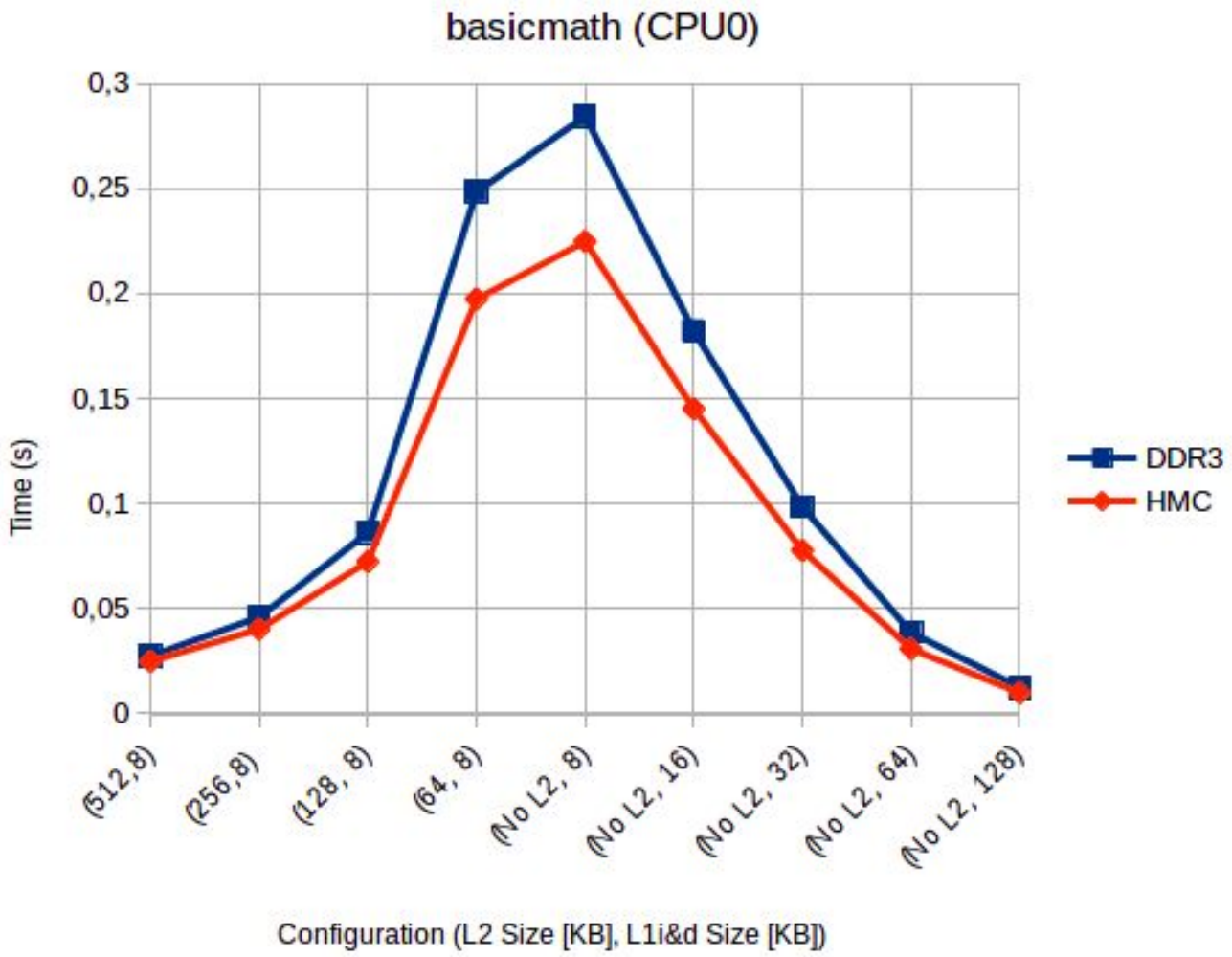
Novas simulações

	W/ 512KB L2 8KB L1s	W/ 256KB L2 8KB L1s	W/ 128KB L2 8KB L1s	W/ 64KB L2 8KB L1s	NO L2 8KB L1s	*NO L2 16KB L1s*	*NO L2 32KB L1s*	NO L2 64KB L1s	NO L2 128KB L1s
CPU0 Exec Time (DDR3)	0,027516	0,045991	0,086318	0,24853	0,284404	0,182226	0,098412	0,038731	0,012469
CPU1 Exec Time (DDR3)	0,028592	0,047009	0,086604	0,248739	0,31862	0,24335	0,122969	0,026951	0,010647
CPU2 Exec Time (DDR3)	0,025253	0,043849	0,085715	0,248088	0,212474	0,113687	0,063625	0,037088	0,023189
CPU3 Exec Time (DDR3)	0,019265	0,038182	0,084119	0,246916	0,022007	0,014824	0,009445	0,004875	0,00318
CPU0 Exec Time (HMC)	0,024968	0,040288	0,072391	0,197466	0,224855	0,145191	0,077768	0,030879	0,010005
CPU1 Exec Time (HMC)	0,026043	0,041306	0,072677	0,197675	0,251907	0,193893	0,097174	0,021488	0,008543
CPU2 Exec Time (HMC)	0,022704	0,038146	0,071787	0,197024	0,167986	0,090582	0,050278	0,029569	0,018607
CPU3 Exec Time (HMC)	0,016717	0,032479	0,070192	0,195852	0,017399	0,011811	0,007463	0,003886	0,002552

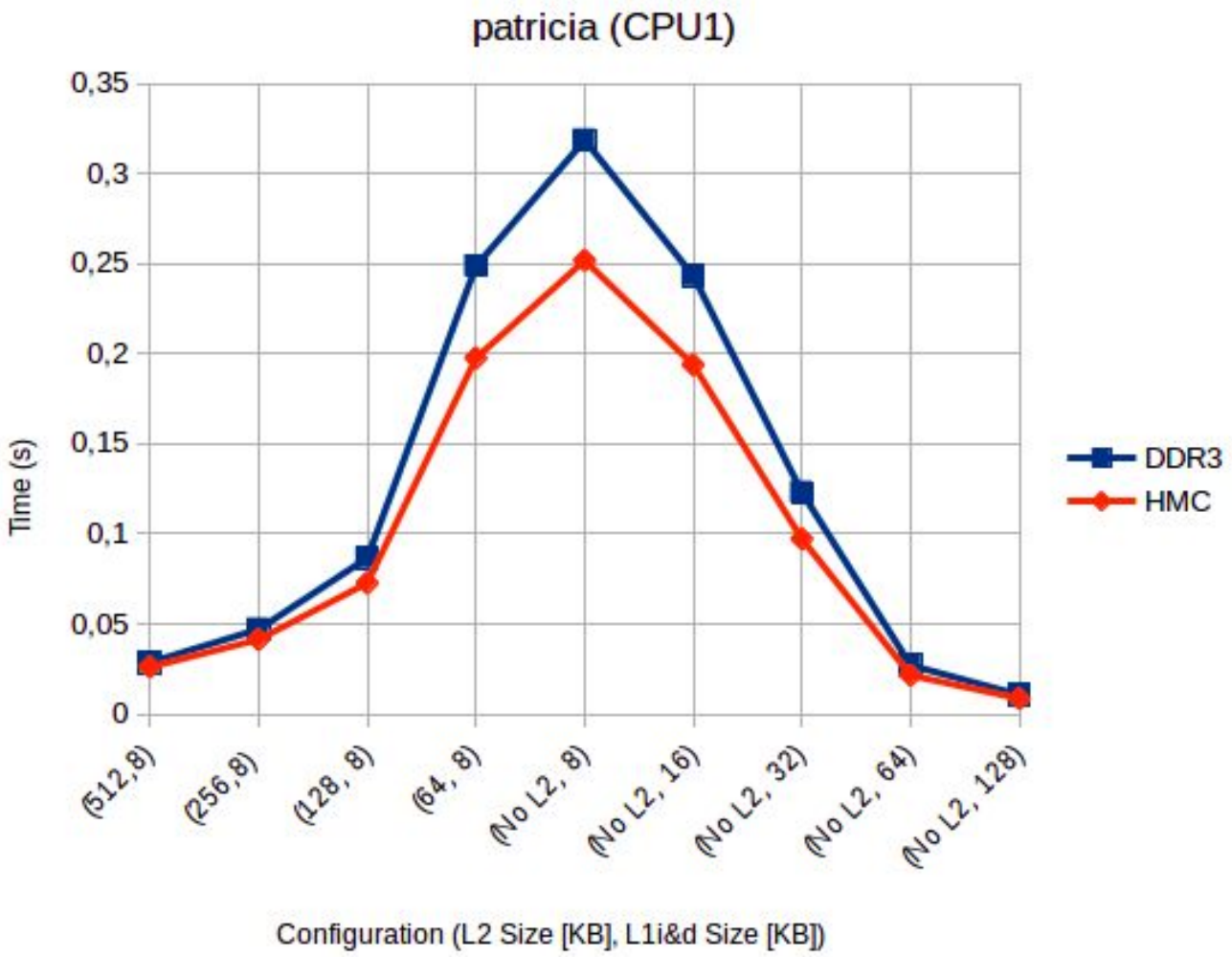
Tempo Total


Total Execution Time
0,35
0,3
0,25
0,2
0,15
0,1
0,05
0
Time (s)
(512,8)
(256,8)
(128, 8)
(64, 8)
(No L2, 8)
(No L2, 16)
(No L2, 32)
(No L2, 64)
(No L2, 128)
Configuration (L2 Size [KB], L1i&d Size [KB])
DDR3
HMC

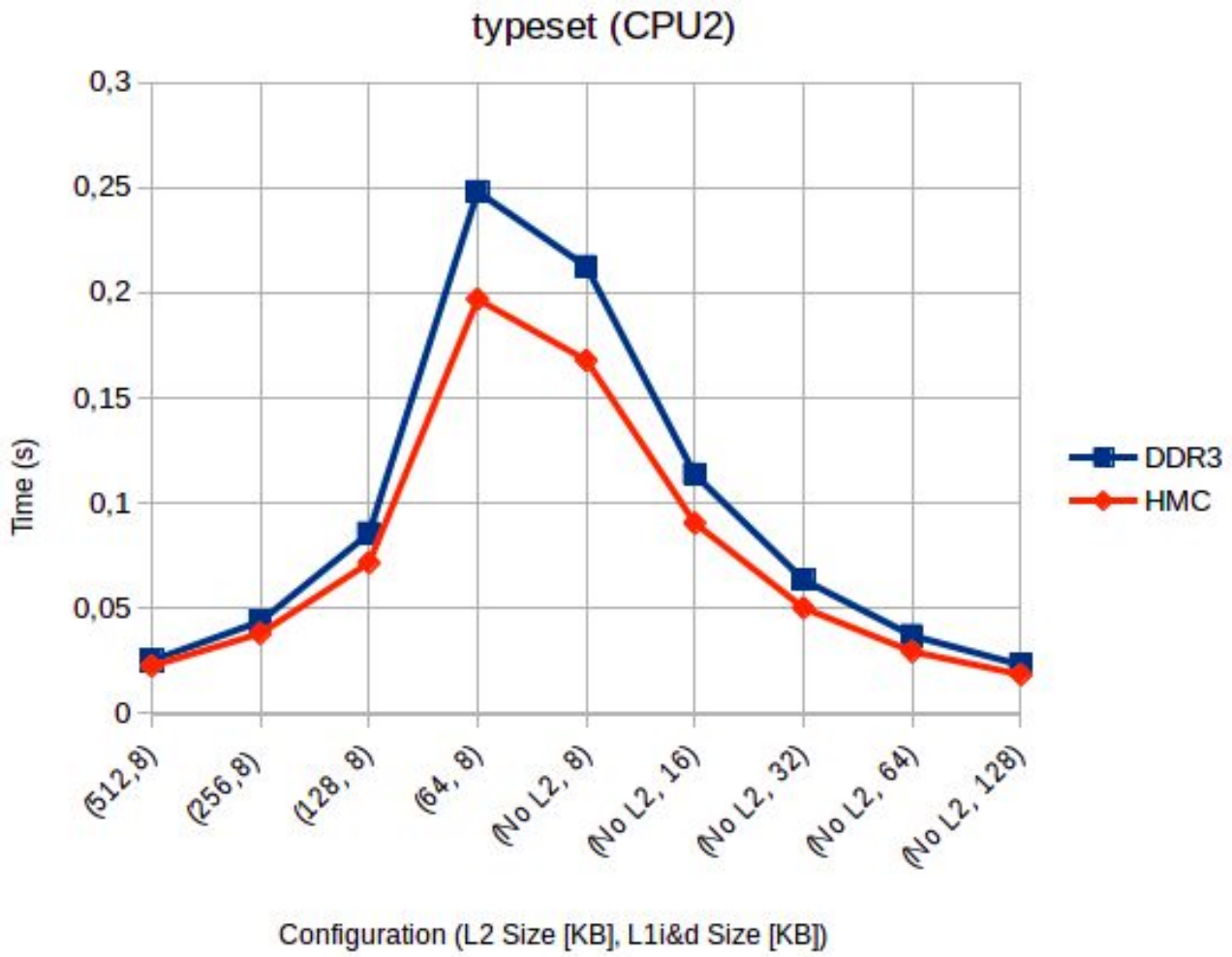
basicmath


basicmath (CPU0)
0,3
0,25
0,2
0,15
0,1
0,05
0
Time (s)
(512,8)
(256,8)
(128, 8)
(64, 8)
(No L2, 8)
(No L2, 16)
(No L2, 32)
(No L2, 64)
(No L2, 128)
Configuration (L2 Size [KB], L1i&d Size [KB])
DDR3
HMC

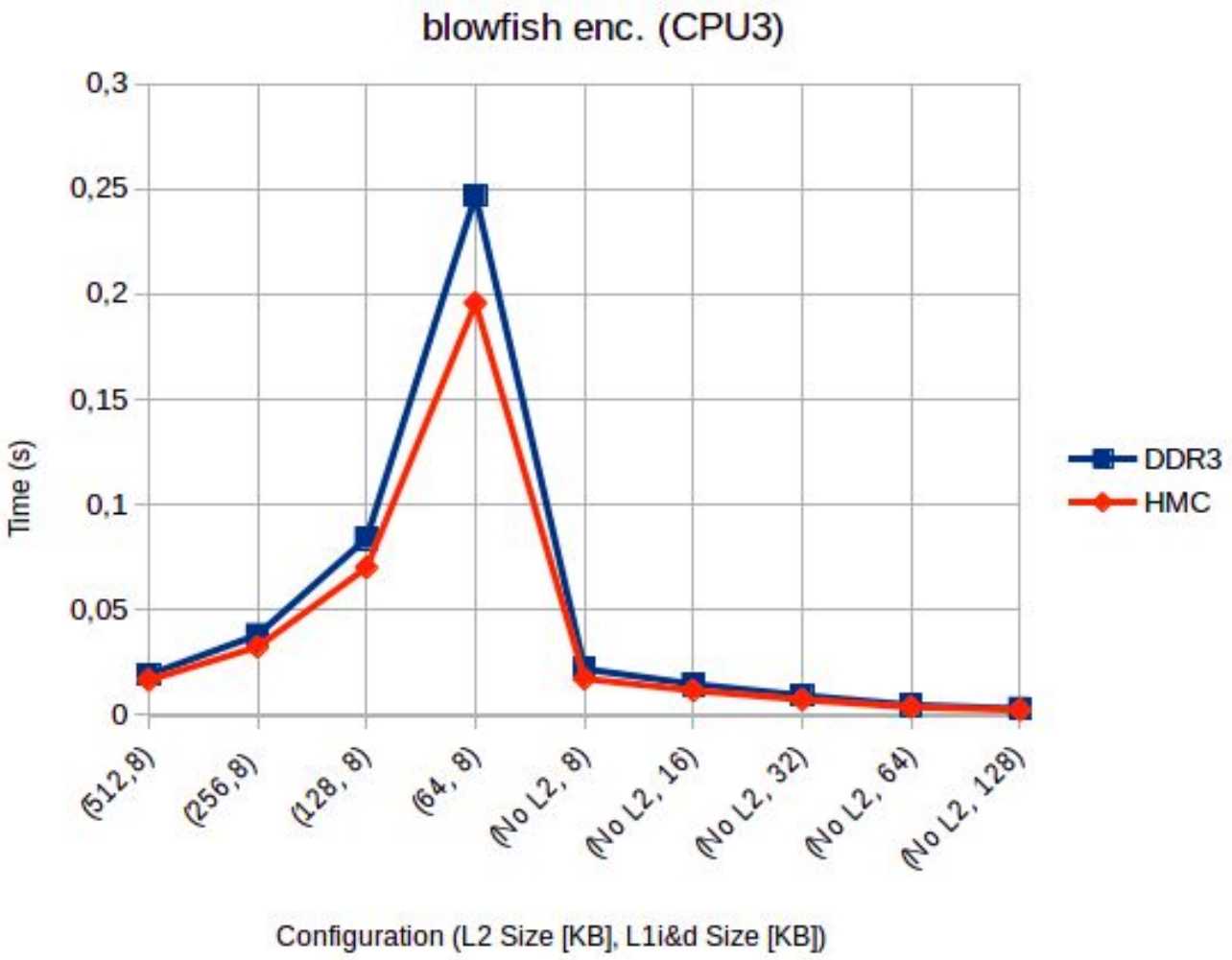
patricia


patricia (CPU1)
0,35
0,3
0,25
0,2
0,15
0,1
0,05
0
Time (s)
(512,8)
(256,8)
(128, 8)
(64, 8)
(No L2, 8)
(No L2, 16)
(No L2, 32)
(No L2, 64)
(No L2, 128)
Configuration (L2 Size [KB], L1i&d Size [KB])
DDR3
HMC

typeset


typeset (CPU2)
0,3
0,25
0,2
0,15
0,1
0,05
0
Time (s)
(512,8)
(256,8)
(128, 8)
(64, 8)
(No L2, 8)
(No L2, 16)
(No L2, 32)
(No L2, 64)
(No L2, 128)
Configuration (L2 Size [KB], L1i&d Size [KB])
DDR3
HMC

blowfish


blowfish enc. (CPU3)
0,3
0,25
0,2
0,15
0,1
0,05
0
Time (s)
(512,8)
(256,8)
(128, 8)
(64, 8)
(No L2, 8)
(No L2, 16)
(No L2, 32)
(No L2, 64)
(No L2, 128)
Configuration (L2 Size [KB], L1i&d Size [KB])
DDR3
HMC

Conclusões (parciais)

- Menor Latência de Acesso pode compensar ao ponto de dispensar L2 caso usando HMC
- DSE com dados de energia e área podem apontar as configurações mais interessantes considerando também estes aspectos
  - EDP
  - EDPA
- Realizar simulações com menos configurações, porém utilizando versões “large” das aplicações do MiBench, visando maior demanda nas caches.