A Multi-Mode Software-Defined CMOS BPSK Receiver SoC for the Newly Enhanced WWVB Atomic Clock Broadcast

O. Eliezer, T. Jung, R. Lobo, M. Appel, Y. Liang, D. Robbins, P. Nelsen, and Z. Islam

Xtendwave, Dallas, Texas, USA

Abstract — **The first receiver system-on-chip (SoC) for the newly enhanced phase-modulation based WWVB broadcast is presented. Having an extensively digital architecture, and relying on the new features of the broadcast, it demonstrates 2-3 orders of receiver sensitivity superiority when compared to receiver ICs designed for the legacy WWVB broadcast. To allow for robust reception at very low signal levels, as well as in proximity to the station, it accommodates a dynamic range of over 130dB, representing the widest dynamic range found in any consumer-market receiver IC. The SoC is implemented in a 180nm CMOS process and has a die size of about 7mm^2.**

Index Terms — **radio controlled clock (RCC), atomic clock, WWVB, synchronization, software defined radio (SDR).**

I. Introduction

Radio controlled clocks (RCCs), colloquially referred to as 'atomic clocks', offer the benefits of initial self-setting when first powered, timing drift compensation for accurate time-keeping, and automatic one-hour adjustments at the beginning and end of daylight saving time periods. They can be designed with relatively small antennas and at low implementation cost, targeting the consumer market, by relying on powerful low frequency (LF) broadcasts of digitally represented time information. Such broadcasts are available in Europe, Asia, and North America, and are based on accurate atomic clock sources. The WWVB station, located in Colorado and operated by the National Institute of Standards and Technology (NIST), has begun with its first digital broadcast of a time-code in 1965. This broadcast was based on an amplitude/pulse-width modulation (AM/PWM) scheme and a binary-coded-decimal (BCD) representation of the digital information [1]. While this allowed for a relatively simple implementation of a receiver, it resulted in inefficient use of the broadcast energy and a need for a relatively high SNR for reliable reception. Consequently, in locations distant from the station, such as on the East Coast, as well as inside buildings, where high penetration losses are experienced, reception of this broadcast often fails. Furthermore, the prevalence of electronic equipment and electrical appliances results in a high level of electromagnetic interference (EMI) in both residential and industrial/office environments, potentially further degrading the reception SNR.

In order to ensure reliable coverage throughout the USA, the broadcast format has been enhanced to include a binary-phase-shift-keying (BPSK) modulation scheme and a more efficient representation of the time information [2], for which the presented SoC is the first receiver IC.

II. The Prior-Art AM Receivers

Receiver ICs for the AM based broadcast, having the structure shown in Fig. 1, have been available for over a decade and have typically been based on a BiCMOS process, in which a low-noise and high-gain front-end could operate at very low current [3].
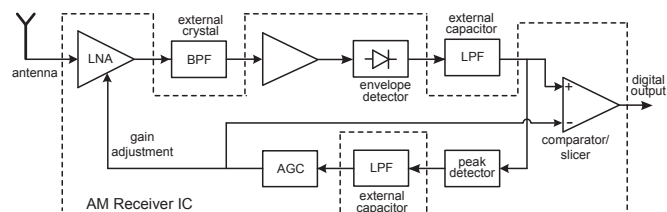

Fig. 1. Block diagram of typical prior art AM receiver for RCC

Since the bit rate in this system is only 1 bps, these analog ICs require several external passive components that provide filtering functions that are related with this low rate. The first of these is a crystal filter centered at 60kHz, the carrier frequency of the broadcast. Its bandwidth is typically narrower than 10 Hz and establishes the receiver's selectivity and noise bandwidth, since the demodulator operates at the carrier frequency. The next external filtering component is a capacitor on the order of several nF, which determines the time-constant for the envelope-detector circuit that recovers the envelope from the AM signal. Finally, a large capacitor, on the order of several μF, is used to create a time-constant of several seconds for the analog AGC function. This is necessary for the identification of the two amplitude levels in the digital AM signal and for correct adjustment of the threshold of the slicer producing the output signal. The information recovery function, which is based on measuring the duration of the pulses representing each received bit at the output of the slicer, is usually performed in a separate CMOS IC, which serves for time-keeping and control functions in the RCC.

III. DIGITAL SIGNAL PROCESSING BASED RECEPTION

A. Other work on DSP based RCC reception

A receiver based on digital signal processing for the German broadcast DCF77 has been proposed in [4], where a significant performance improvement is demonstrated when compared to the conventional envelope detection based receiver, particularly for reception durations as long as one hour. However, while timing information on the DCF77 signal is phase-modulated, all time information (time and date) is represented only in the AM/PWM, which greatly limits the performance that can be obtained within reasonable reception durations of a few minutes.

B. The EverSet® System-on-Chip

After successful demonstration of a software-based solution that was based on a discrete implementation and an existing processor [5], the presented SoC, being introduced to the market at this time, was designed in a 180 nm standard CMOS process from TowerJazz. It incorporates a dual-input front-end, a sigma-delta ADC, digital logic for initial signal processing, and a processor core licensed from EnSilica, where the majority of the information recovery and control functions take place, as shown in Fig. 2. With the BPSK demodulation operation implemented entirely digitally, the external filtering components, mentioned in the previous section in the context of the AM receivers, have been eliminated, thus offering the first commercially available fully integrated digital solution for RCCs.
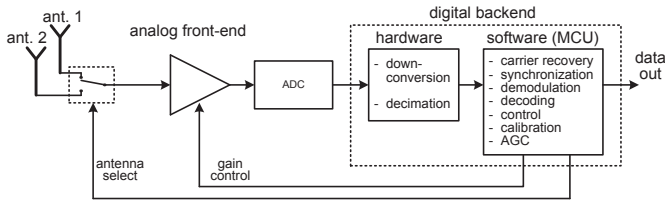

Fig. 2. Block diagram of presented receiver's signal path

The design of a dual-input front-end was motivated by the need to overcome antenna orientation problems, which are common in stationary RCCs and can result in significant losses. By using two separate antennas, which are positioned perpendicularly, the receiver is provided not only with the opportunity to receive at the different orientations, but also to avoid interference that may be stronger in one antenna than in the other. The receiver's antenna switching system can accommodate shorting of the inactive antenna, thus minimizing its passive effects on the active one.

Fig. 3 provides a detailed block diagram of the presented SoC, where several functions beyond those of the receiver signal path are shown. These include a power-on-reset (POR) function, high-rate RC oscillator for the processor, a serial interface function to allow the SoC to communicate with a host MCU and be controlled by it, voltage regulators for the analog and digital circuitry, a timer, ROM for program data, and RAM, which is used primarily for storage of the digitized received signal.
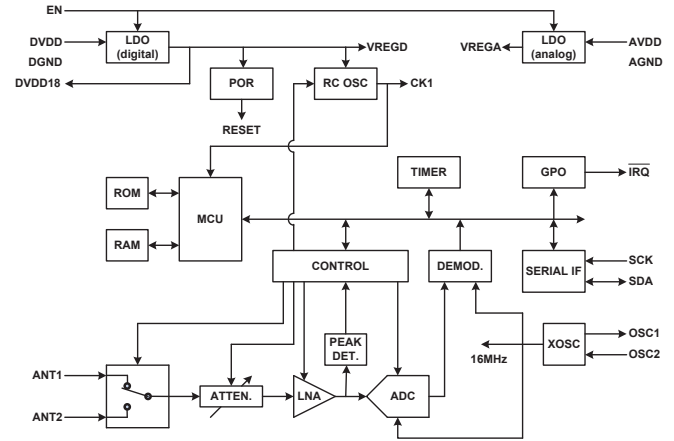

Fig. 3. Block diagram of the receiver SoC

The antennas used in RCCs are typically based on a ferrite-rod inductor on the order of 1 mH, which resonates with a parallel capacitor on the order of several nF. The typical dimensions for such rod in wall-clocks is 6 - 10 cm, with a diameter of 1 cm, and about 2 cm (and a smaller diameter) in wrist-watches. The parallel resonant circuit has a high impedance at resonance, on the order of $0.1\,\text{M}\Omega$, depending on the quality factor Q of the inductor. Therefore, the LNA in the receiver's front-end is designed to have a high-impedance, rather than the conventional $50\,\Omega$ impedance used in higher frequency receivers. This high impedance is in excess of $1\,\text{M}\Omega$ in the presented CMOS receiver, to ensure minimal loading and attenuation when fed by the high-impedance antenna. While the noise-figure and sensitivity specifications and measurements for such receivers should consider this parameter, sensitivity for prior-art receivers is often misleadingly specified for a $50\,\Omega$ source, which would effectively shunt the receiver's input noise, thereby not reflecting the actual performance that is experienced with the antenna at that input.

It is common to specify the receiver's sensitivity and input signal range in units of voltage rather than power [3]. Typical values for these may be on the order of $0.5\,\mu\text{V}$ for the receiver's sensitivity and 50 mV for the highest input voltage, representing a dynamic range of 100 dB. This range appears to be accommodated primarily by a front-end with an adjustable attenuation/gain in the range of -40 dB to 47 dB, in the example of [3], since the AM demodulation function is very limited in its dynamic range.

In addition to the advantages of the new modulation scheme, as discussed in [1], [5] and [6], the BPSK demodulation is not sensitive to saturation and does not require the linearity that is critical for AM demodulation. Hence, the highest signal level accommodated by the

presented receiver is limited only by what may cause instability in the sigma-delta ADC. Therefore, adequate adjustable attenuation, shown in Fig. 3, was placed in the signal path, to allow for the receiver's input signal to exceed 0.1 V. Such high signal level was measured by the authors on a 6 cm ferrite-rod antenna in Fort Collins, Colorado, where the WWVB station is located and many common RCC products fail to operate, as a result of saturation. Naturally, there is no lower bound on the received signal level, when considering propagation and penetration losses, as well as other reception challenges [1].

C. The Receiver's Principles of Operation

A typical 6 cm ferrite-rod antenna of 1.5 mH inductance and $Q \cong 120$ may be represented, at resonance, as a signal source having the output resistance of 67 kΩ, for which the corresponding thermal noise floor is 32 nV/√Hz. Although 60 kHz is a relatively low frequency, for which 1/f noise could be a dominating factor in certain designs, the noise floor achieved in the LNA is as low as 17 nV/√Hz. The noise increase introduced by the LNA is, therefore,

$$10 \cdot \log \left[(32^2 + 17^2) / 32^2 \right] = 1.1 \text{ dB}.$$

When considering the slight attenuation caused by the LNA's finite impedance of over 1 MΩ, introducing a loss below 0.5 dB, the overall noise figure is about **1.5 dB**.

Whenever overly high signal levels are received, an appropriate amount of attenuation is automatically introduced by the controller in response to an ADC overload indication. The attenuation is realized by a switchable array of capacitor based voltage dividers, providing attenuation in the range 0 - 24 dB in steps of 3 dB. Since the adjustable attenuator is placed before the LNA, as shown in Fig. 3, the selected attenuation results in a corresponding degradation in NF, which is affordable at strong signal levels. Additional gain adjustment is available through the control of the degeneration resistance in the LNA, but the majority of the dynamic range is realized by the ADC and the signal processing that follows.

The effective resolution of the digitization operation reaches 16 bits, when considering the decimated samples that are produced from the raw 16 Mbps bit-stream of the ADC. However, more importantly, the significant ratio between the bandwidth of the digitized signal, which is over 100 kHz, with respect to the bandwidth of the information, which is 1 Hz or lower, provides a processing gain that greatly contributes to the dynamic range. To illustrate this, the minimal carrier-to-noise ratio (CNR) for reliable reception in the normal rate mode of 1 bps is about 10 dB in a bandwidth of 1 Hz (corresponding to an effective SNR of about 8 dB, due to the presence of the AM on the carrier). However, this corresponds to CNR = - 40 dB in a bandwidth of 100 kHz, which means that the digitized samples are dominated by noise. This remains the situation even when

the signal level increases by several orders of magnitude beyond this threshold value, allowing the outcome of the ADC to appear unchanged, while only the signal processing that follows may reveal the differences. For this reason, the enhanced receiver sensitivity of about -3 dB (in a 1 Hz bandwidth), which is reached in the extended mode based on 6-minute symbols, as described in [6], does not represent an additional challenge for the front-end, and is achieved merely through signal processing.

Fig. 4 shows a die micrograph of the 180 nm CMOS SoC, highlighting some of the major functions in it. As can be seen in this figure, the die area, totaling about 7 mm^2, is dominated by the memory and digital logic, for which favorable scaling can be expected when migrating to processes of smaller geometries. While the IC is equipped with a sufficient amount of ROM for storing program memory, it can also run from external flash memory, providing for a convenient software-defined radio (SDR) platform for the development of extensions and improvements. The internal RAM, capable of being loaded with program data, as well as with many minutes of recorded digitized samples of the input signal, was designed with significant margin, allowing for reduction in its size in future revisions. Furthermore, it may be completely eliminated, alongside with the processor core, when the receiver functionality is incorporated into a larger CMOS SoC that already has such resources.
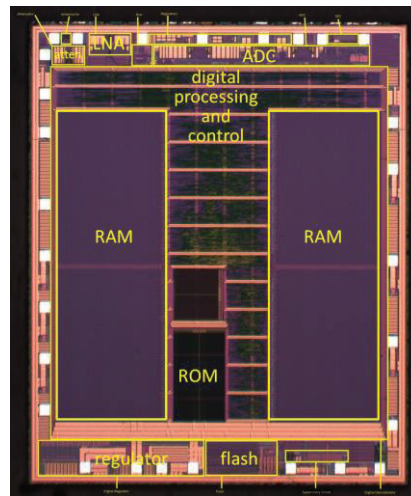

Fig. 4. Die micrograph highlighting some of the SoC functions

IV. MEASURED RESULTS

The sensitivity of the presented receiver depends on the mode of operation selected for it amongst the modes made available in the new broadcast format, for which different signal-processing based reception algorithms are used [6]. In the normal mode of reception, based on a 2-minute operation and an information bit-rate of 1bps, the receiver

exhibits sensitivity of about -78 dBmV, corresponding to $CNR_{min}=10\,dB\ @\,BW=1\,Hz$, when fed with a source calibrated to have the same high impedance as the antenna (i.e. not a $50\,\Omega$ source). During this 2-minute operation the receiver consumes about 5 mA from a 3 V supply, followed by a few seconds of current in excess of 20 mA, dominated by the signal processing algorithms. However, this operation is performed only once, for time acquisition, while the periodic operation that is typically performed once a day, intended only for timing-drift compensation, is a simpler tracking operation of shorter duration. These different operations are described in [5]-[6]. Overall, when averaged over a day, the receiver's operation consumes well below 10 μA, representing less than 10% of the current consumption of a typical analog wall-clock and having a correspondingly low impact on its battery lifetime.

Table 1 below lists the measured sensitivity results for several AM based radio-controlled clocks available on the market, normalized to the $CNR_{min}=10\,dB\ @\,BW=1\,Hz$ sensitivity level of the presented receiver (when acquiring the time information in normal mode). These results were measured with a high-impedance source emulating the antenna (i.e. without actual antennas). As can be seen in the table, the sensitivity performance advantage ranges from 18 dB to 24 dB, without even engaging the extended mode that offers an additional order of magnitude of sensitivity, and without considering the more robust tracking operation.

TABLE I

RECEPTION SENSITIVITY COMPARISON IN NORMAL MODE

AM RCC product		minimum CNR at BW=1Hz [dB]	EverSet® advantage [dB]
maker	model		
Ken-Tech	T-4660	28	18
Westclox	70026	30	20
La Crosse	S98642	34	24
AcuRite	13131	34	24

Although the advantage of the BPSK modulation was shown to be only about 10 dB in [5]-[6], this assumed an optimal digital receiver for both schemes, whereas in practice, the AM receivers are based on an envelope detector and cannot perform optimal filtering. Furthermore, additional factors, such as the more efficient information encoding, the error-correction coding, and practical implementation considerations, altogether provide the presented receiver with a second order of magnitude of a performance advantage. The reception superiority was also demonstrated extensively in field trials with the actual broadcast, as reported in [5]-[6]. It is to be noted that it is not only manifested in scenarios of weak reception, but also in the presence of strong interference, which is commonly found at such frequency, particularly in office and industrial environments.

V. CONCLUSION

The first receiver IC for the enhanced BPSK-based WWVB broadcast was presented, having multiple modes of operation and exhibiting a dynamic range of over 130dB, the widest available in any consumer market wireless receiver IC. Its reception sensitivity outperforms previous generation ICs by several orders of magnitude, depending on the selected mode of operation. Contrary to existing radio-controlled-clock (RCC) receiver ICs in the market, which are based on a BiCMOS process and rely on external components for filtering, the presented receiver SoC, implemented in standard 180 nm CMOS, is extensively digital. At this time, several radio-controlled clock products are being designed based on it, providing them reliable reception and time-keeping throughout North America. Beyond the important benefit offered by the integrability of the presented EverSet® receiver into a CMOS SoC environment, the performance advantage offered by it allows for reduction in the antenna size. This results not only in an associated reduction in cost, but also allows smaller devices, such as small/thin wristwatches, to benefit from this technology.

REFERENCES

[1] M. A. Lombardi, "The Evolution of Time Measurement, Part 5: Radio Controlled Clocks," *IEEE Instrumentation & Measurement Magazine*, April 2012.

[2] J. Lowe, M. Deutch, G. Nelson, D. Sutton, W. Yates, P. Hansen, O. Eliezer, T. Jung, S. Morrison, Y. Liang, D. Rajan, S. Balasubramanian, A. Ramasami, W. Khalil, "New Improved System for WWVB Broadcast," in *43rd Annual PTTI Meeting Proceedings*, November 2011.

[3] C-MAX Time Solutions, CME6005 Receiver IC Datasheet, *available at* http://www.c-max-time.com

[4] D. Engeler, "Performance Analysis and Receiver Architectures of DCF77 Radio-Controlled Clocks," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 59, no. 5, May 2012.

[5] Y. Liang, D. Rajan, O. Eliezer, S. Balasubramanian, and W. Khalil, "A New Broadcast Format and Receiver Architecture for Radio Controlled Clocks," in *IEEE MWSCAS Proceedings*, August 2013.

[6] Y. Liang, O. Eliezer, D. Rajan, and J. Lowe, "WWVB Time Signal Broadcast: An Enhanced Broadcast Format and Multi-Mode Receiver," *IEEE Comm. Magazine, April 2014.*