PREFIX ADDER AND SUBTRACTOR

Prefix adder is a parallel adder. Below diagram is a 8-bit Prefix adder. In the diagram, there are two modules. Here, c0 is the input carry and c8 is the output carry. For n-bit binary number we use n XOR gates to output the sum. C1 to c7 are the intermediate carries.

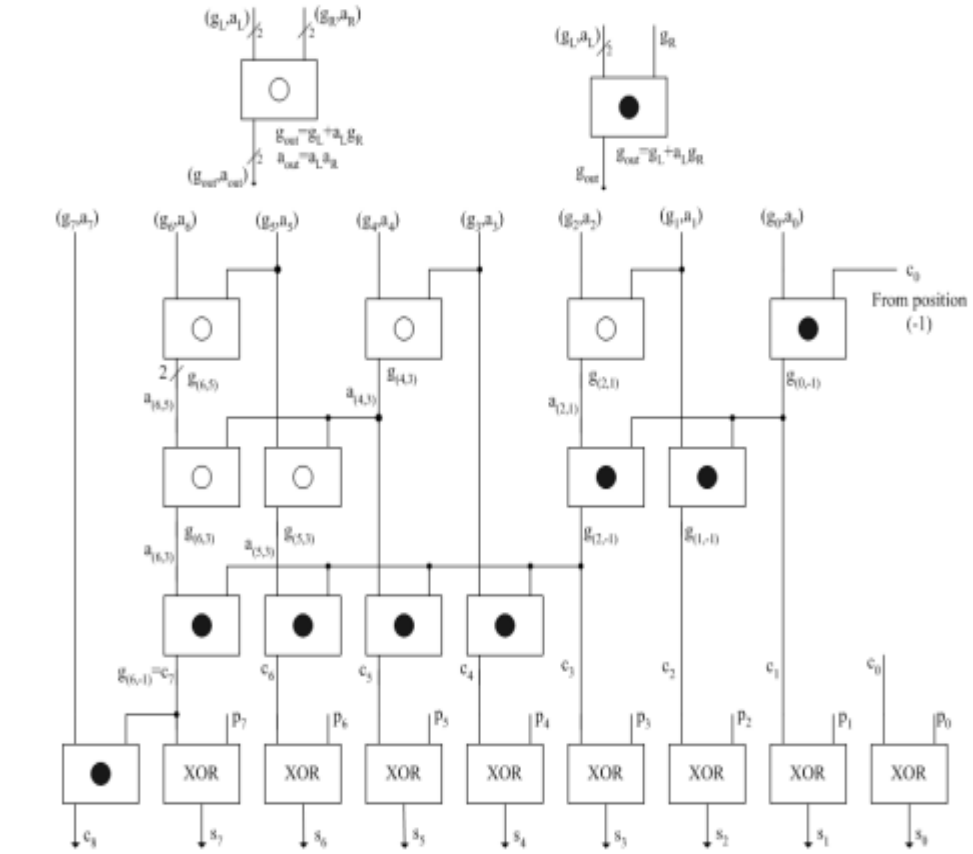

Figure 4 8-bit prefix adder (Modules to obtain p_i,g_i and a_i signals not shown.)

For the first module, output is gout.

For the second module, output is (gout, aout).

Where gout=gL+(aL*gR), aout=aL*aR

The above 8-bit prefix adder is converted into 16-bit prefix adder by increasing number of cells and levels.

The delay in addition or subtraction can be eliminated by increasing the number of levels or by increasing the number of cells.

Subtraction of 16-bit binary numbers is performed by finding 2’s complement and adding it using prefix adder.

Example:

a-b=a+bbar+1