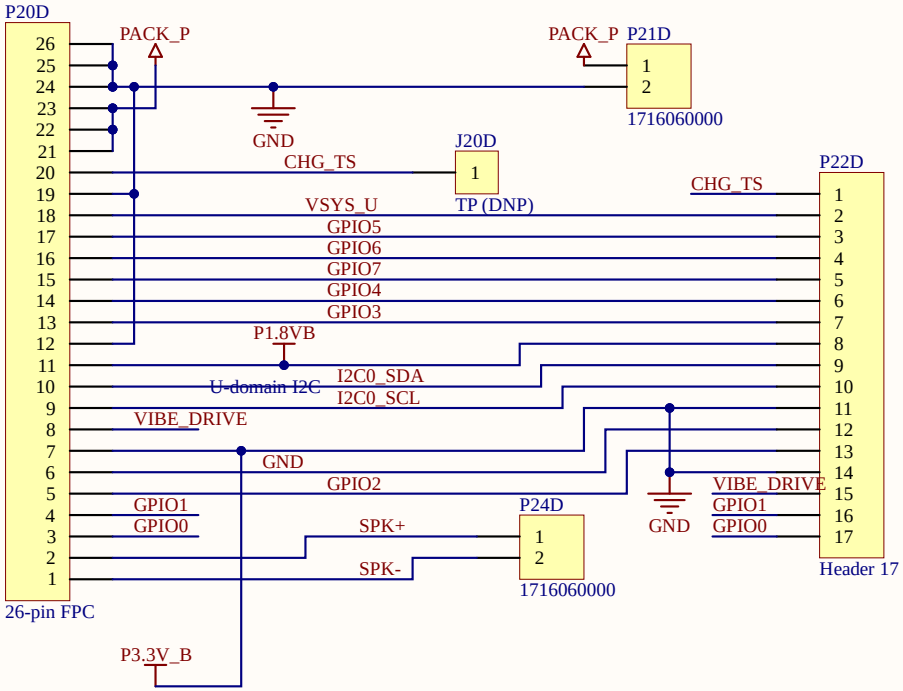
Top-side FPC (pack + speaker + backlight + GPIO)



https://github.com/betrusted-io

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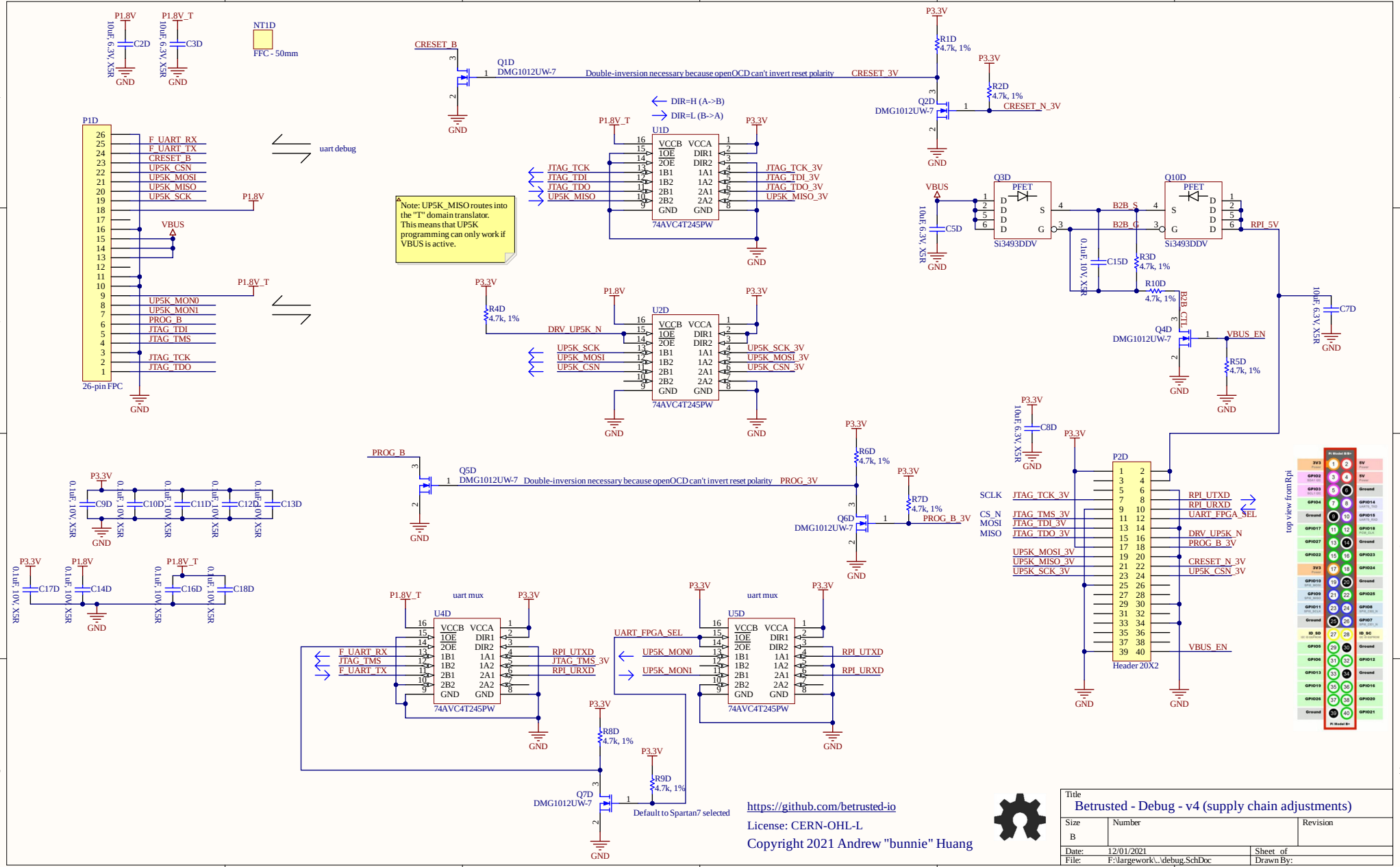
Title	Betrusted - Debug	
Size A	Number	Revision
Date: 12/01/2021		Sheet of
File: F:\largework\..\breakout.SchDoc		Drawn By:


P1.8V
P1.8V_T
C2D
C3D
10uF, 6.3V, X5R
GND
NT1D
FFC - 50mm
CRESET_B
Q1D
DMG1012UW-7
Double-inversion necessary because openOCD can't invert reset polarity
CRESET_3V
P3.3V
R1D
4.7k, 1%
R2D
Q2D
CRESET_N_3V
P1D
F_UART_RX
F_UART_TX
CRESET_B
UP5K_CSN
UP5K_MOSI
UP5K_MISO
UP5K_SCK
uart debug
VBUS
UP5K_MON0
UP5K_MON1
PROG_B
JTAG_TDI
JTAG_TMS
JTAG_TCK
JTAG_TDO
26-pin FPC
DIR=H (A->B)
DIR=L (B->A)
U1D
74AVC4T245PW
JTAG_TCK_3V
JTAG_TDI_3V
JTAG_TDO_3V
UP5K_MISO_3V
Note: UP5K_MISO routes into the "T" domain translator. This means that UP5K programming can only work if VBUS is active.
Q3D
Si3493DDV
Q10D
B2B_S
B2B_G
RPI_5V
C5D
C15D
R3D
R10D
B2B_CTL
Q4D
VBUS_EN
R5D
C7D
R4D
DRV_UP5K_N
U2D
UP5K_SCK_3V
UP5K_MOSI_3V
UP5K_CSN_3V
C8D
P2D
Header 20X2
SCLK
CS_N
MOSI
MISO
RPI_UTXD
RPI_URXD
UART_FPGA_SEL
DRV_UP5K_N
PROG_B_3V
CRESET_N_3V
UP5K_CSN_3V
top view from Rpi
Q5D
R6D
R7D
Q6D
C9D
C10D
C11D
C12D
C13D
C17D
C14D
C16D
C18D
uart mux
U4D
U5D
F_UART_RX
JTAG_TMS
F_UART_TX
RPI_UTXD
JTAG_TMS_3V
RPI_URXD
UART_FPGA_SEL
UP5K_MON0
UP5K_MON1
R8D
R9D
Q7D
Default to Spartan7 selected
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Title
Betrusted - Debug - v4 (supply chain adjustments)
Size
B
Number
Revision
Date: 12/01/2021
File: F:\largework\..\debug.SchDoc
Sheet of
Drawn By: