Artix-7 FPGAs Data Sheet: DC and Switching Characteristics

DS181 (v1.6) April 17, 2013 **Product Specification**

Introduction

Artix™-7 FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices can operate at either of two V_{CCINT} voltages, 0.9V and 1.0V and are screened for lower maximum static power. When operated at V_{CCINT} = 1.0V, the speed specification of a -2L device is the same as the -2 speed grade. When operated at V_{CCINT} = 0.9V, the -2L static and dynamic power is reduced.

Artix-7 FPGA DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Artix-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

All specifications are subject to change without notice.

DC Characteristics

Table 1: **Absolute Maximum Ratings(1)**

Symbol	Description	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage	–0.5	1.1	V
V_{CCAUX}	Auxiliary supply voltage	–0.5	2.0	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.5	1.1	V
V_{CCO}	Output drivers supply voltage for 3.3V HR I/O banks	–0.5	3.6	V
V_{REF}	Input reference voltage	–0.5	2.0	V
V_{IN}(2)(3)(4)	I/O input voltage	–0.4	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(5)	–0.4	2.625	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V
GTP Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTP transmitter and receiver circuits	–0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTP transmitter and receiver termination circuits	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
I_{DCIN}	DC input current for receiver input pins DC coupled $V_{MGTAVTT}$ = 1.2V	–	10	mA
I_{DCOUT}	DC output current for transmitter pins DC coupled $V_{MGTAVTT}$ = 1.2V	–	10	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies(6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies(6)	–	+260	°C
T_j	Maximum junction temperature(6)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
5. See Table 9 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage	0.95	1.00	1.05	V
	For -2L (0.9V) devices: internal supply voltage	0.87	0.90	0.93	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCBRAM}	Block RAM supply voltage	0.95	1.00	1.05	V
V_{CCO}(3)(4)	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
V_{IN}(5)	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(6)	–0.20	–	2.625	V
I_{IN}(7)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT}(8)	Battery voltage	1.0	–	1.89	V
GTP Transceiver					
$V_{MGTAVCC}$(9)	Analog supply voltage for the GTP transmitter and receiver circuits	0.97	1.0	1.03	V
$V_{MGTAVTT}$(9)	Analog supply voltage for the GTP transmitter and receiver termination circuits	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V

Table 2: **Recommended Operating Conditions[1][2] *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground.
2. For the design of the power distribution system consult UG483, *7 Series FPGAs PCB Design and Pin Planning Guide*.
3. Configuration data is retained even if V_{CCO} drops to 0V.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. See Table 9 for TMDS_33 specifications.
7. A total of 200 mA per bank should not be exceeded.
8. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
9. Each voltage listed requires the filter circuit described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}[2]	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}[3]	Battery supply current	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40) for commercial (C), and industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50) for commercial (C), and industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60) for commercial (C), and industrial (I), and extended (E) temperature devices	44	60	83	Ω

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[1]	Max	Units
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7A100T	155	155	155	108	mA
		XC7A200T	328	328	328	232	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	5	5	5	5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7A100T	36	36	36	36	mA
		XC7A200T	73	73	73	73	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7A100T	4	4	4	4	mA
		XC7A200T	11	11	11	11	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 6 shows the minimum current, in addition to I_{CCQ}, that is required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 6: **Power-On Current for Artix-7 Devices(1)**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
	Typ(2)	Typ(2)	Typ(2)	Typ(2)	
XC7A100T	I_{CCINTQ} + 170	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7A200T	I_{CCINTQ} + 340	I_{CCAUXQ} + 50	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 80	mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.
2. Typical values are specified at nominal voltage, 25°C.

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100°C$(1)	–	500	ms
		$T_J = 85°C$(1)	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS33	–0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVTTL	–0.300	0.8	2.000	3.450	0.400	2.400	Note 5	Note 5
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.00	–13.00
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.90	–8.90
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.00	–13.00
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.90	–8.90
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.00	–8.00
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.40	–13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

Table 9: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–		Note 5	
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

Table 11: **LVDS_25 DC Specifications**(1)

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in v1.08 from the ISE® Design Suite 14.5 and Vivado® Design Suite 2013.1 for the -3, -2, -2L (1.0V), and -1 speed grades and v1.05 from the ISE® Design Suite 14.5 and Vivado® Design Suite 2013.1 for the -2L (0.9V) speed grade.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix-7 FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 12 correlates the current status of each Artix-7 device on a per speed grade basis.

Table 12: **Artix-7 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7A100T			-3, -2, -2L (1.0V), -1, and -2L (0.9V)
XC7A200T			-3, -2, -2L (1.0V), -1, and -2L (0.9V)

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 13 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 13: **Artix-7 Device Production Software and Speed Specification Release**

Device	Speed Grade			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7A100T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07			ISE 14.5 or Vivado 2013.1 v1.05
XC7A200T	ISE 14.4 and Vivado 2012.4 with the 14.4/2012.4 device pack v1.07			

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 9.

Table 14: **Networking Applications Interface Performances**

Description	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	1250	950	950	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	680	680	600	600	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1250	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 15: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

Memory Standard	Speed Grade				Units
	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	
4:1 Memory Controllers					
DDR3	1066	800	800	800	Mb/s
DDR3L	800	800	667	667	Mb/s
DDR2	800	800	667	667	Mb/s
LPDDR2	667	667	533	533	Mb/s
2:1 Memory Controllers					
DDR3	800	700	620	620	Mb/s
DDR3L	800	700	620	620	Mb/s
DDR2	800	700	620	620	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).

IOB Pad Input/Output/3-State

Table 16 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 16: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.26	1.34	1.41	1.58	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVTTL_S8	1.26	1.34	1.41	1.58	3.54	3.66	3.92	4.15	4.11	4.32	4.75	4.80	ns
LVTTL_S12	1.26	1.34	1.41	1.58	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVTTL_S16	1.26	1.34	1.41	1.58	3.07	3.19	3.45	3.68	3.64	3.85	4.28	4.33	ns
LVTTL_S24	1.26	1.34	1.41	1.58	3.29	3.41	3.67	3.90	3.86	4.07	4.50	4.55	ns
LVTTL_F4	1.26	1.34	1.41	1.58	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVTTL_F8	1.26	1.34	1.41	1.58	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVTTL_F12	1.26	1.34	1.41	1.58	2.73	2.85	3.10	3.33	3.29	3.51	3.93	3.98	ns
LVTTL_F16	1.26	1.34	1.41	1.58	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVTTL_F24	1.26	1.34	1.41	1.58	2.52	2.65	2.90	3.22	3.09	3.31	3.73	3.87	ns
LVDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
MINI_LVDS_25	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
BLVDS_25	0.73	0.81	0.88	0.90	1.84	1.96	2.21	2.44	2.40	2.62	3.04	3.09	ns
RSDS_25 (point to point)	0.73	0.81	0.88	0.90	1.27	1.40	1.65	1.88	1.84	2.06	2.48	2.53	ns
PPDS_25	0.73	0.81	0.88	0.90	1.29	1.41	1.67	1.88	1.86	2.07	2.49	2.53	ns
TMDS_33	0.73	0.81	0.88	0.90	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
PCI33_3	1.24	1.32	1.39	1.57	3.10	3.22	3.48	3.71	3.67	3.88	4.31	4.36	ns
HSUL_12	0.67	0.75	0.82	0.87	1.80	1.93	2.18	2.41	2.37	2.59	3.01	3.06	ns
DIFF_HSUL_12	0.68	0.76	0.83	0.88	1.80	1.93	2.18	2.21	2.37	2.59	3.01	2.86	ns
HSTL_I_S	0.67	0.75	0.82	0.87	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
HSTL_II_S	0.65	0.73	0.80	0.85	1.41	1.54	1.79	1.99	1.98	2.20	2.62	2.64	ns
HSTL_I_18_S	0.67	0.75	0.82	0.87	1.29	1.41	1.67	1.86	1.86	2.07	2.49	2.51	ns
HSTL_II_18_S	0.66	0.75	0.81	0.87	1.41	1.54	1.79	1.97	1.98	2.20	2.62	2.62	ns
DIFF_HSTL_I_S	0.68	0.76	0.83	0.85	1.59	1.71	1.96	2.13	2.15	2.37	2.79	2.78	ns
DIFF_HSTL_II_S	0.68	0.76	0.83	0.85	1.51	1.63	1.88	2.07	2.08	2.29	2.71	2.72	ns
DIFF_HSTL_I_18_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.96	1.95	2.17	2.59	2.61	ns
DIFF_HSTL_II_18_S	0.70	0.78	0.85	0.87	1.46	1.58	1.84	2.00	2.03	2.24	2.67	2.65	ns
HSTL_I_F	0.67	0.75	0.82	0.87	1.10	1.22	1.48	1.69	1.67	1.88	2.31	2.34	ns

Table 16: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
HSTL_II_F	0.65	0.73	0.80	0.85	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
HSTL_I_18_F	0.67	0.75	0.82	0.87	1.13	1.26	1.51	1.72	1.70	1.92	2.34	2.37	ns
HSTL_II_18_F	0.66	0.75	0.81	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_HSTL_I_F	0.68	0.76	0.83	0.85	1.18	1.30	1.56	1.77	1.75	1.96	2.39	2.42	ns
DIFF_HSTL_II_F	0.68	0.76	0.83	0.85	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
DIFF_HSTL_I_18_F	0.71	0.79	0.86	0.87	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
DIFF_HSTL_II_18_F	0.70	0.78	0.85	0.87	1.21	1.33	1.59	1.77	1.78	1.99	2.42	2.42	ns
LVCMOS33_S4	1.26	1.34	1.41	1.62	3.80	3.93	4.18	4.41	4.37	4.59	5.01	5.06	ns
LVCMOS33_S8	1.26	1.34	1.41	1.62	3.52	3.65	3.90	4.13	4.09	4.31	4.73	4.78	ns
LVCMOS33_S12	1.26	1.34	1.41	1.62	3.09	3.21	3.46	3.69	3.65	3.87	4.29	4.34	ns
LVCMOS33_S16	1.26	1.34	1.41	1.62	3.40	3.52	3.77	4.00	3.97	4.18	4.60	4.65	ns
LVCMOS33_F4	1.26	1.34	1.41	1.62	3.26	3.38	3.64	3.86	3.83	4.04	4.46	4.51	ns
LVCMOS33_F8	1.26	1.34	1.41	1.62	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVCMOS33_F12	1.26	1.34	1.41	1.62	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVCMOS33_F16	1.26	1.34	1.41	1.62	2.55	2.68	2.93	3.16	3.12	3.34	3.76	3.81	ns
LVCMOS25_S4	1.12	1.20	1.27	1.43	3.13	3.26	3.51	3.72	3.70	3.91	4.34	4.37	ns
LVCMOS25_S8	1.12	1.20	1.27	1.43	2.88	3.01	3.26	3.49	3.45	3.67	4.09	4.14	ns
LVCMOS25_S12	1.12	1.20	1.27	1.43	2.48	2.60	2.85	3.08	3.05	3.26	3.68	3.73	ns
LVCMOS25_S16	1.12	1.20	1.27	1.43	2.82	2.94	3.20	3.43	3.39	3.60	4.03	4.08	ns
LVCMOS25_F4	1.12	1.20	1.27	1.43	2.74	2.87	3.12	3.35	3.31	3.52	3.95	4.00	ns
LVCMOS25_F8	1.12	1.20	1.27	1.43	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVCMOS25_F12	1.12	1.20	1.27	1.43	2.16	2.29	2.54	2.77	2.73	2.95	3.37	3.42	ns
LVCMOS25_F16	1.12	1.20	1.27	1.43	2.01	2.13	2.39	2.61	2.58	2.79	3.21	3.26	ns
LVCMOS18_S4	0.74	0.83	0.89	0.94	1.62	1.74	1.99	2.19	2.19	2.40	2.82	2.84	ns
LVCMOS18_S8	0.74	0.83	0.89	0.94	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVCMOS18_S12	0.74	0.83	0.89	0.94	2.18	2.30	2.56	2.79	2.75	2.96	3.39	3.44	ns
LVCMOS18_S16	0.74	0.83	0.89	0.94	1.52	1.65	1.90	2.13	2.09	2.31	2.73	2.78	ns
LVCMOS18_S24	0.74	0.83	0.89	0.94	1.60	1.72	1.98	2.21	2.17	2.38	2.81	2.86	ns
LVCMOS18_F4	0.74	0.83	0.89	0.94	1.45	1.57	1.82	2.05	2.01	2.23	2.65	2.70	ns
LVCMOS18_F8	0.74	0.83	0.89	0.94	1.68	1.80	2.06	2.29	2.25	2.46	2.89	2.94	ns
LVCMOS18_F12	0.74	0.83	0.89	0.94	1.68	1.80	2.06	2.29	2.25	2.46	2.89	2.94	ns
LVCMOS18_F16	0.74	0.83	0.89	0.94	1.40	1.52	1.77	2.00	1.97	2.18	2.60	2.65	ns
LVCMOS18_F24	0.74	0.83	0.89	0.94	1.34	1.46	1.71	1.94	1.90	2.12	2.54	2.59	ns
LVCMOS15_S4	0.77	0.86	0.93	0.98	2.05	2.18	2.43	2.50	2.62	2.84	3.26	3.15	ns
LVCMOS15_S8	0.77	0.86	0.93	0.98	2.09	2.21	2.46	2.69	2.65	2.87	3.29	3.34	ns
LVCMOS15_S12	0.77	0.86	0.93	0.98	1.59	1.71	1.96	2.19	2.15	2.37	2.79	2.84	ns
LVCMOS15_S16	0.77	0.86	0.93	0.98	1.59	1.71	1.96	2.19	2.15	2.37	2.79	2.84	ns

Table 16: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVCMOS15_F4	0.77	0.86	0.93	0.98	1.85	1.97	2.23	2.27	2.42	2.63	3.06	2.92	ns
LVCMOS15_F8	0.77	0.86	0.93	0.98	1.60	1.72	1.98	2.21	2.17	2.38	2.81	2.86	ns
LVCMOS15_F12	0.77	0.86	0.93	0.98	1.35	1.47	1.73	1.96	1.92	2.13	2.56	2.61	ns
LVCMOS15_F16	0.77	0.86	0.93	0.98	1.34	1.46	1.71	1.94	1.90	2.12	2.54	2.59	ns
LVCMOS12_S4	0.87	0.95	1.02	1.08	2.57	2.69	2.95	3.18	3.14	3.35	3.78	3.83	ns
LVCMOS12_S8	0.87	0.95	1.02	1.08	2.09	2.21	2.46	2.69	2.65	2.87	3.29	3.34	ns
LVCMOS12_S12	0.87	0.95	1.02	1.08	1.79	1.91	2.17	2.40	2.36	2.57	2.99	3.05	ns
LVCMOS12_F4	0.87	0.95	1.02	1.08	1.98	2.10	2.35	2.58	2.54	2.76	3.18	3.23	ns
LVCMOS12_F8	0.87	0.95	1.02	1.08	1.54	1.66	1.92	2.15	2.11	2.32	2.75	2.80	ns
LVCMOS12_F12	0.87	0.95	1.02	1.08	1.38	1.51	1.76	1.97	1.95	2.16	2.59	2.62	ns
SSTL135_S	0.67	0.75	0.82	0.87	1.35	1.47	1.73	1.93	1.92	2.13	2.56	2.58	ns
SSTL15_S	0.60	0.68	0.75	0.80	1.30	1.43	1.68	1.88	1.87	2.09	2.51	2.53	ns
SSTL18_I_S	0.67	0.75	0.82	0.87	1.67	1.79	2.04	2.24	2.23	2.45	2.87	2.89	ns
SSTL18_II_S	0.67	0.75	0.82	0.85	1.31	1.43	1.68	1.91	1.87	2.09	2.51	2.56	ns
DIFF_SSTL135_S	0.68	0.76	0.83	0.87	1.35	1.47	1.73	1.93	1.92	2.13	2.56	2.58	ns
DIFF_SSTL15_S	0.68	0.76	0.83	0.87	1.30	1.43	1.68	1.88	1.87	2.09	2.51	2.53	ns
DIFF_SSTL18_I_S	0.71	0.79	0.86	0.87	1.68	1.80	2.06	2.24	2.25	2.46	2.89	2.89	ns
DIFF_SSTL18_II_S	0.71	0.79	0.86	0.87	1.38	1.51	1.76	1.94	1.95	2.17	2.59	2.59	ns
SSTL135_F	0.67	0.75	0.82	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
SSTL15_F	0.60	0.68	0.75	0.80	1.07	1.19	1.45	1.68	1.64	1.85	2.28	2.33	ns
SSTL18_I_F	0.67	0.75	0.82	0.87	1.12	1.24	1.49	1.72	1.69	1.90	2.32	2.37	ns
SSTL18_II_F	0.67	0.75	0.82	0.85	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_SSTL135_F	0.68	0.76	0.83	0.87	1.12	1.24	1.49	1.71	1.69	1.90	2.32	2.36	ns
DIFF_SSTL15_F	0.68	0.76	0.83	0.87	1.07	1.19	1.45	1.68	1.64	1.85	2.28	2.33	ns
DIFF_SSTL18_I_F	0.71	0.79	0.86	0.87	1.23	1.35	1.60	1.80	1.79	2.01	2.43	2.45	ns
DIFF_SSTL18_II_F	0.71	0.79	0.86	0.87	1.21	1.33	1.59	1.79	1.78	1.99	2.42	2.44	ns

Table 17 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 17: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{IOTPHZ}	T input to pad high-impedance	2.06	2.19	2.37	2.19	ns
$T_{IOIBUFDISABLE}$	IBUF turn-on time from IBUFDISABLE to O output	2.11	2.30	2.60	2.30	ns

Input/Output Logic Switching Characteristics

Table 18: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK	0.48/0.02	0.54/0.02	0.76/0.02	0.50/–0.07	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK	0.60/0.01	0.70/0.01	1.13/0.01	0.88/–0.35	ns
T_{IDOCK}/T_{IOCKD}	D pin setup/hold with respect to CLK without Delay	0.01/0.27	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY)	0.02/0.27	0.02/0.29	0.02/0.33	0.01/0.33	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.11	0.11	0.13	0.14	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY)	0.11	0.12	0.14	0.15	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.41	0.44	0.51	0.54	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY)	0.41	0.44	0.51	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.53	0.57	0.66	0.71	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.96	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs	0.61	0.72	0.72	0.72	ns, Min

Table 19: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK	0.67/–0.11	0.71/–0.11	0.84/–0.11	0.64/0.03	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.28/0.01	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK	0.37/0.21	0.44/0.21	0.80/0.21	0.62/–0.25	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK	0.69/–0.14	0.73/–0.14	0.89/–0.14	0.66/0.02	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.24/0.05	ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.83	0.96	1.16	1.36	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.47	0.49	0.56	0.63	ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out	0.72	0.80	0.95	1.12	ns
T_{GSRQ_OLOGIC}	Global set/reset to Q outputs	7.60	7.60	10.51	11.39	ns
Set/Reset						
T_{RPW_OLOGIC}	Minimum pulse width, SR inputs	0.64	0.74	0.74	0.74	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 20: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV	0.01/0.14	0.02/0.15	0.02/0.17	0.02/0.21	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin setup/hold with respect to CLK (for CE1)	0.45/–0.01	0.50/–0.01	0.72/–0.01	0.45/–0.11	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin setup/hold with respect to CLKDIV (for CE2)	–0.10/0.33	–0.10/0.36	–0.10/0.40	–0.17/0.40	ns
Setup/Hold for Data Lines						
T_{ISDCK_D} /T_{ISCKD_D}	D pin setup/hold with respect to CLK	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.04/0.19	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY)(1)	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.03/0.19	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode	–0.02/0.12	–0.02/0.14	–0.02/0.17	–0.04/0.19	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1)	0.12/0.12	0.14/0.14	0.17/0.17	0.19/0.19	ns
Sequential Delays						
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.53	0.54	0.66	0.67	ns
Propagation Delays						
T_{ISDO_DO}	D input to DO output pin	0.11	0.11	0.13	0.14	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in the timing report.

Output Serializer/Deserializer Switching Characteristics

Table 21: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input setup/hold with respect to CLKDIV	0.42/0.03	0.45/0.03	0.63/0.03	0.44/–0.02	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input setup/hold with respect to CLK	0.69/–0.13	0.73/–0.13	0.88/–0.13	0.66/–0.25	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input setup/hold with respect to CLKDIV	0.31/–0.13	0.34/–0.13	0.39/–0.13	0.46/–0.25	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input setup/hold with respect to CLK	0.32/0.58	0.34/0.58	0.51/0.58	0.28/–0.04	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV	0.47	0.52	0.85	0.70	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input setup/hold with respect to CLK	0.32/0.01	0.34/0.01	0.51/0.01	0.24/0.00	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.40	0.42	0.48	0.54	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.47	0.49	0.56	0.63	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.83	0.92	1.11	1.18	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 22: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL	3.67	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00(1)	200.00	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00(1)	300.00	300.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	59.28	59.28	59.28	59.28	ns
IDELAY						
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY	680.00	680.00	600.00	520.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY	0.12/0.11	0.16/0.13	0.21/0.16	0.14/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY	0.12/0.16	0.14/0.18	0.16/0.22	0.10/0.23	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY	0.15/0.09	0.16/0.11	0.18/0.14	0.22/0.19	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 23: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T_{OFFCKO_DO}	RDCLK to Q outputs	0.55	0.60	0.68	0.81	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags	0.55	0.61	0.77	0.79	ns
Setup/Hold						
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.47/0.02	0.51/0.02	0.58/0.02	0.76/0.09	ns
$T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$	WREN to WRCLK	0.42/–0.01	0.47/–0.01	0.53/–0.01	0.70/–0.05	ns
$T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$	RDEN to RDCLK	0.53/0.02	0.58/0.02	0.66/0.02	0.79/–0.02	ns
Minimum Pulse Width						
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	1.62	2.15	2.15	2.15	ns
Maximum Frequency						
F_{MAX}	RDCLK and WRCLK	266.67	200.00	200.00	200.00	MHz

CLB Switching Characteristics

Table 24: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.10	0.11	0.13	0.15	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.27	0.30	0.36	0.41	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.42	0.46	0.55	0.65	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.94	1.05	1.27	1.51	ns, Max
T_{AXA}	AX inputs to AMUX output	0.62	0.69	0.84	1.01	ns, Max
T_{AXB}	AX inputs to BMUX output	0.58	0.66	0.83	0.98	ns, Max
T_{AXC}	AX inputs to CMUX output	0.60	0.68	0.82	0.98	ns, Max
T_{AXD}	AX inputs to DMUX output	0.68	0.75	0.90	1.08	ns, Max
T_{BXB}	BX inputs to BMUX output	0.51	0.57	0.69	0.82	ns, Max
T_{BXD}	BX inputs to DMUX output	0.62	0.69	0.82	0.99	ns, Max
T_{CXC}	CX inputs to CMUX output	0.42	0.48	0.58	0.69	ns, Max
T_{CXD}	CX inputs to DMUX output	0.53	0.59	0.71	0.86	ns, Max
T_{DXD}	DX inputs to DMUX output	0.52	0.58	0.70	0.84	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.44	0.53	0.62	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.47	0.53	0.66	0.73	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.07/0.12	0.09/0.14	0.11/0.18	0.11/0.22	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.06/0.19	0.07/0.21	0.09/0.26	0.09/0.33	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.59/0.08	0.66/0.09	0.81/0.11	0.97/0.15	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.15/0.00	0.17/0.00	0.21/0.01	0.34/–0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.38/0.03	0.43/0.04	0.53/0.05	0.62/0.19	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.53	0.59	0.71	0.83	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.58	0.70	0.83	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 25: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.98	1.09	1.32	1.54	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.37	1.53	1.86	2.18	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.54/0.28	0.60/0.30	0.72/0.35	0.96/0.40	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.27/0.55	0.30/0.60	0.37/0.70	0.43/0.71	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.69/0.18	0.77/0.21	0.94/0.26	1.11/0.31	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.38/0.10	0.43/0.12	0.53/0.17	0.62/0.13	ns, Min
T_{CECK_LRAM}/ T_{CKCE_LRAM}	CE input to CLK	0.39/0.10	0.44/0.11	0.53/0.17	0.63/0.12	ns, Min
Clock CLK						
T_{MPW_LRAM}	Minimum pulse width	1.05	1.13	1.25	1.61	ns, Min
T_{MCP}	Minimum clock period	2.10	2.26	2.50	3.21	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 26: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	1.19	1.33	1.61	1.89	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.58	1.77	2.15	2.53	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.12	1.23	1.46	1.68	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS_SHFREG}/ T_{WH_SHFREG}	WE input	0.37/0.10	0.41/0.12	0.51/0.17	0.59/0.13	ns, Min
T_{CECK_SHFREG}/ T_{CKCE_SHFREG}	CE input to CLK	0.37/0.10	0.42/0.11	0.52/0.17	0.60/0.12	ns, Min
T_{DS_SHFREG}/ T_{DH_SHFREG}	A – D inputs to CLK	0.33/0.34	0.37/0.37	0.44/0.43	0.54/0.55	ns, Min
Clock CLK						
T_{MPW_SHFREG}	Minimum pulse width	0.77	0.86	0.98	1.22	ns, Min

Block RAM and FIFO Switching Characteristics

Table 27: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.85	2.13	2.46	2.87	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.64	0.74	0.89	1.02	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.77	3.04	3.84	5.30	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.73	0.81	0.94	1.11	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with cascade (without output register)[2]	2.61	2.88	3.30	3.76	ns, Max
	Clock CLK to DOUT output with cascade (with output register)[4]	1.16	1.28	1.46	1.56	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.76	0.87	1.05	1.14	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.94	1.02	1.15	1.30	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.78	0.85	0.94	1.10	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.56	2.81	3.55	4.90	ns, Max
	Clock CLK to BITERR (with output register)	0.68	0.76	0.89	1.05	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.75	0.88	1.07	1.15	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.84	0.93	1.08	1.29	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDRA}/T_{RCKC\_ADDRA}$	ADDR inputs[8]	0.45/0.31	0.49/0.33	0.57/0.36	0.77/0.45	ns, Min
$T_{RDCK\_DI\_WF\_NC}/T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9]	0.58/0.60	0.65/0.63	0.74/0.67	0.92/0.76	ns, Min
$T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode[9]	0.20/0.29	0.22/0.34	0.25/0.41	0.29/0.38	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.50/0.43	0.55/0.46	0.63/0.50	0.78/0.54	ns, Min
$T_{RDCK\_DI\_ECCW}/T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only[9]	0.93/0.43	1.02/0.46	1.17/0.50	1.38/0.48	ns, Min
$T_{RDCK\_DI\_ECC\_FIFO}/T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode[9]	1.04/0.56	1.15/0.59	1.32/0.64	1.55/0.77	ns, Min
$T_{RCCK\_INJECTBITERR}/T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.58/0.35	0.64/0.37	0.74/0.40	0.92/0.48	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM enable (EN) input	0.35/0.20	0.39/0.21	0.45/0.23	0.57/0.26	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.24/0.15	0.29/0.15	0.36/0.16	0.40/0.19	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.29/0.07	0.32/0.07	0.35/0.07	0.41/0.07	ns, Min

Table 27: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/0.42	0.34/0.43	0.36/0.46	0.40/0.47	ns, Min
$T_{RCCK\_WEA}/T_{RCKC\_WEA}$	Write enable (WE) input (block RAM only)	0.44/0.18	0.48/0.19	0.54/0.20	0.64/0.23	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN FIFO inputs	0.46/0.30	0.46/0.35	0.47/0.43	0.77/0.44	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	RDEN FIFO inputs	0.42/0.30	0.43/0.35	0.43/0.43	0.71/0.50	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers(10)	0.90	0.98	1.10	1.25	ns, Max
$T_{RREC\_RST}/T_{RREM\_RST}$	FIFO reset recovery and removal timing(11)	1.87/–0.81	2.07/–0.81	2.37/–0.81	2.44/–0.71	ns, Max
Maximum Frequency						
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (write first and no change modes) when not in SDP RF mode	509.68	460.83	388.20	315.66	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B	509.68	460.83	388.20	315.66	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses	447.63	404.53	339.67	268.96	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM cascade (write first, no change mode) when cascade but not in RF mode	467.07	418.59	345.78	273.30	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled	467.07	418.59	345.78	273.30	MHz
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	405.35	362.19	297.35	226.60	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	509.68	460.83	388.20	315.66	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	410.34	365.10	297.53	215.38	MHz

Notes:

1. The timing report shows all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 28: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.26/ 0.12	0.30/ 0.13	0.37/ 0.14	0.45/ 0.14	ns
$T_{DSPDCK\_B\_BREG}$/$T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.33/ 0.15	0.38/ 0.16	0.45/ 0.18	0.60/ 0.19	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.17/ 0.17	0.20/ 0.19	0.24/ 0.21	0.34/ 0.29	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.25/ 0.25	0.32/ 0.27	0.42/ 0.27	0.54/ 0.23	ns
$T_{DSPDCK\_ACIN\_AREG}$/$T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.23/ 0.12	0.27/ 0.13	0.32/ 0.14	0.36/ 0.14	ns
$T_{DSPDCK\_BCIN\_BREG}$/$T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.25/ 0.15	0.29/ 0.16	0.36/ 0.18	0.41/ 0.19	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_B\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.40/ –0.01	2.76/ –0.01	3.29/ –0.01	4.31/ –0.07	ns
$T_{DSPDCK\_\{A, B\}\_ADREG}$/ $T_{DSPCKD\_ D\_ADREG}$	{A, D} input to AD register CLK	1.29/ –0.02	1.48/ –0.02	1.76/ –0.02	2.29/ –0.27	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\} \_PREG\_MULT}$	{A, B} input to P register CLK using multiplier	4.02/ –0.28	4.60/ –0.28	5.48/ –0.28	6.95/ –0.48	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.93/ –0.73	4.50/ –0.73	5.35/ –0.73	6.73/ –1.68	ns
$T_{DSPDCK\_\{A, B\} \_PREG}$/ $T_{DSPCKD\_\{A, B\} \_PREG}$	A or B input to P register CLK not using multiplier	1.73/ –0.28	1.98/ –0.28	2.35/ –0.28	2.80/ –0.48	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.54/ –0.26	1.76/ –0.26	2.10/ –0.26	2.54/ –0.45	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.32/ –0.15	1.51/ –0.15	1.80/ –0.15	2.13/ –0.25	ns
Setup and Hold Times of the CE Pins						
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.35/ 0.06	0.42/ 0.08	0.52/ 0.11	0.64/ 0.11	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.28/ 0.10	0.34/ 0.11	0.42/ 0.13	0.49/ 0.16	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.36/ –0.03	0.43/ –0.03	0.52/ –0.03	0.68/ 0.14	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.17/ 0.18	0.21/ 0.20	0.27/ 0.23	0.45/ 0.29	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.36/ 0.01	0.43/ 0.01	0.53/ 0.01	0.63/ 0.00	ns

Table 28: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.41/ 0.11	0.46/ 0.13	0.55/ 0.15	0.63/ 0.40	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.07/ 0.10	0.08/ 0.11	0.09/ 0.12	0.13/ 0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.44/ 0.07	0.50/ 0.08	0.59/ 0.09	0.67/ 0.08	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.21/ 0.22	0.23/ 0.24	0.27/ 0.28	0.28/ 0.35	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.27/ 0.01	0.30/ 0.01	0.35/ 0.01	0.43/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.79	4.35	5.18	6.61	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.72	4.26	5.07	6.41	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier	1.53	1.75	2.08	2.48	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.33	1.53	1.82	2.22	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.55	0.63	0.74	0.87	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	4.06	4.65	5.54	7.03	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.97	4.54	5.40	6.81	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.77	2.03	2.41	2.88	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.58	1.81	2.15	2.62	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.65	4.19	5.00	6.40	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.37	1.57	1.88	2.44	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.38	0.44	0.53	0.63	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.90	4.47	5.33	6.79	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.61	1.85	2.21	2.84	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	1.11	1.28	1.52	1.82	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.36	1.56	1.85	2.21	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.37	0.44	0.54	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.52	0.59	0.69	0.84	ns

Table 28: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.68	1.93	2.31	2.73	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.92	2.21	2.64	3.12	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.72	3.10	3.69	4.60	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.96	3.38	4.02	4.99	ns
Clock to Outs from Input Register Clock to Output Pins						
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.94	4.51	5.37	6.84	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.64	1.87	2.22	2.65	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.69	1.93	2.30	2.81	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.91	4.48	5.32	6.77	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.64	0.73	0.87	1.02	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	4.19	4.79	5.70	7.24	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.88	2.15	2.55	3.04	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	4.16	4.76	5.65	7.17	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK CREG to CARRYCASCOUT output	1.94	2.21	2.63	3.20	ns
Maximum Frequency						
F_{MAX}	With all registers used	628.93	550.66	464.25	363.77	MHz
F_{MAX_PATDET}	With pattern detector	531.63	465.77	392.93	310.08	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	349.28	305.62	257.47	210.44	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	317.26	277.62	233.92	191.28	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	397.30	346.26	290.44	223.26	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	397.30	346.26	290.44	223.26	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	260.01	227.01	190.69	150.13	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	241.72	211.15	177.43	140.10	MHz

Clock Buffers and Networks

Table 29: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold	0.12/0.39	0.13/0.40	0.16/0.41	0.31/0.67	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold	0.12/0.39	0.13/0.40	0.16/0.41	0.31/0.67	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.09	0.10	0.14	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	628.00	628.00	464.00	394.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 30: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.11	1.26	1.54	1.56	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	680.00	680.00	600.00	600.00	MHz

Table 31: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.64	0.76	0.99	1.24	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.34	0.39	0.52	0.72	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.81	0.85	1.09	0.96	ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	420.00	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 32: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.16	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin setup and hold	0.19/0.13	0.22/0.15	0.28/0.21	0.35/0.25	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	628.00	628.00	464.00	394.00	MHz

Table 33: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global clock tree duty-cycle distortion(1)	All	0.20	0.20	0.20	0.25	ns
T_{CKSKEW}	Global clock tree skew(2)	XC7A100T	0.27	0.33	0.36	0.48	ns
		XC7A200T	0.40	0.48	0.54	0.69	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.14	0.14	0.14	0.14	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.18	0.18	0.18	0.18	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 34: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F_{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10.00	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency	550.00	500.00	450.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	600.00	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600.00	1440.00	1200.00	1200.00	MHz

Table 34: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$MMCM\_F_{BANDWIDTH}$	Low MMCM bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
$MMCM\_T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs(2)	0.12	0.12	0.12	0.12	ns
$MMCM\_T_{OUTJITTER}$	MMCM output jitter	Note 3				
$MMCM\_T_{OUTDUTY}$	MMCM output clock duty-cycle precision(4)	0.20	0.20	0.20	0.25	ns
$MMCM\_T_{LOCKMAX}$	MMCM maximum lock time	100.00	100.00	100.00	100.00	µs
$MMCM\_F_{OUTMAX}$	MMCM maximum output frequency	800.00	800.00	800.00	800.00	MHz
$MMCM\_F_{OUTMIN}$	MMCM minimum output frequency(5)(6)	4.69	4.69	4.69	4.69	MHz
$MMCM\_T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
$MMCM\_RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
$MMCM\_F_{PFDMAX}$	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
$MMCM\_F_{PFDMIN}$	Minimum frequency at the phase frequency detector	10.00	10.00	10.00	10.00	MHz
$MMCM\_T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE	0.59	0.68	0.81	0.78	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, $MMCM\_F_{OUTMIN}$ is 0.036 MHz.

PLL Switching Characteristics

Table 35: **PLL Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F_{INMAX}	Maximum input clock frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency	19.00	19.00	19.00	19.00	MHz
$PLL\_F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency	2133.00	1866.00	1600.00	1600.00	MHz
$PLL\_F_{BANDWIDTH}$	Low PLL bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
$PLL\_T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs(2)	0.12	0.12	0.12	0.12	ns
$PLL\_T_{OUTJITTER}$	PLL output jitter	Note 3				
$PLL\_T_{OUTDUTY}$	PLL output clock duty-cycle precision(4)	0.20	0.20	0.20	0.25	ns
$PLL\_T_{LOCKMAX}$	PLL maximum lock time	100.00	100.00	100.00	100.00	µs
PLL_F_{OUTMAX}	PLL maximum output frequency	800.00	800.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency(5)	6.25	6.25	6.25	6.25	MHz
$PLL\_T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
$PLL\_RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector	550.00	500.00	450.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	19.00	19.00	19.00	19.00	MHz
$PLL\_T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T_{PLLDCK_DADDR}/ T_{PLLCKD_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
$T_{PLLDCK\_DI}/T_{PLLCKD\_DI}$	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T_{PLLDCK_DEN}/ T_{PLLCKD_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T_{PLLDCK_DWE}/ T_{PLLCKD_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 36: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF *without* MMCM/PLL (near clock region)	XC7A100T	5.14	5.74	6.72	7.62	ns
		XC7A200T	5.47	6.11	7.16	8.08	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 37: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF *without* MMCM/PLL (far clock region)	XC7A100T	5.38	6.01	7.02	7.94	ns
		XC7A200T	6.17	6.89	8.05	9.03	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 38: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7A100T	1.00	1.00	1.00	1.79	ns
		XC7A200T	1.01	1.02	1.04	1.84	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 39: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7A100T	0.82	0.82	0.82	1.40	ns
		XC7A200T	0.81	0.81	0.81	1.45	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 40: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.						
$T_{ICKOFCS}$	Clock to out of I/O clock	5.01	5.61	6.64	7.32	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 41: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks	XC7A100T	2.69/–0.34	2.89/–0.34	3.34/–0.34	5.66/–0.51	ns
		XC7A200T	3.03/–0.36	3.27/–0.36	3.79/–0.36	6.66/–0.55	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 42: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(2) with MMCM	XC7A100T	2.47/–0.62	2.81/–0.62	3.36/–0.62	2.15/–0.48	ns
		XC7A200T	2.59/–0.63	2.95/–0.63	3.52/–0.63	2.32/–0.51	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 43: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(2) with PLL	XC7A100T	2.78/–0.20	3.15/–0.20	3.78/–0.20	2.47/–0.59	ns
		XC7A200T	2.91/–0.21	3.29/–0.21	3.94/–0.21	2.64/–0.62	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 44: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.						
T_{PSCS}/T_{PHCS}	Setup and hold of I/O clock	–0.38/1.31	–0.38/1.46	–0.38/1.76	–0.16/1.89	ns

Table 45: **Sample Window**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{SAMP}	Sampling error at receiver pins(1)	0.59	0.64	0.70	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO(2)	0.35	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

Table 46: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew(1)	XC7A100T	CSG324	113	ps
			FTG256	120	ps
			FGG484	144	ps
			FGG676	153	ps
		XC7A200T	SBG484	111	ps
			FBG484	109	ps
			FBG676	121	ps
			FFG1156	151	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTP Transceiver Specifications

GTP Transceiver DC Input and Output Levels

Table 47 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further details.

Table 47: **GTP Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
$V_{CMOUTAC}$	Common mode output voltage: AC coupled		1/2 $V_{MGTAVTT}$			mV
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew (FFG, FBG, SBG packages)		–	–	10	ps
	Transmitter output pair (TXP and TXN) intra-pair skew (FGG, FTG, CSG packages)		–	–	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG482: *7 Series FPGAs GTP Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

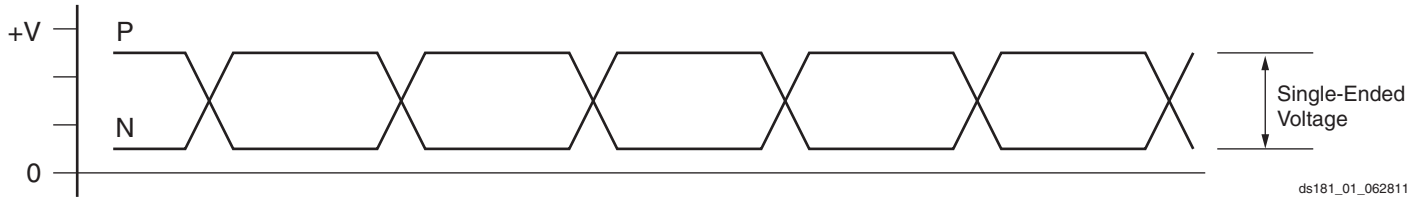

Figure 1: **Single-Ended Peak-to-Peak Voltage**

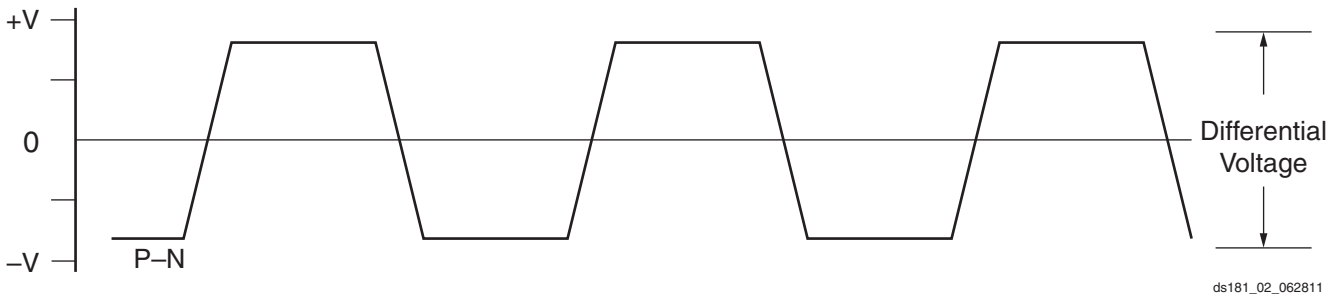

Figure 2: **Differential Peak-to-Peak Voltage**

Table 48 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further details.

Table 48: **GTP Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	350	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTP Transceiver Switching Characteristics

Consult UG482: *7 Series FPGAs GTP Transceiver User Guide* for further information.

Table 49: **GTP Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1		-2L		
			Package Type								
			FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	FFG FBG SBG	FGG FTG CSG	
F_{GTPMAX}	Maximum GTP transceiver data rate		6.6	5.4	6.6	5.4	3.75	3.75	3.75	3.75	Gb/s
F_{GTPMIN}	Minimum GTP transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
$F_{GTPRANGE}$	PLL line rate range	1	3.2–6.6		3.2–6.6		3.2–3.75		3.2–3.75		Gb/s
		2	1.6–3.3		1.6–3.3		1.6–3.2		1.6–3.2		Gb/s
		4	0.8–1.65		0.8–1.65		0.8–1.6		0.8–1.6		Gb/s
		8	0.5–0.825		0.5–0.825		0.5–0.8		0.5–0.8		Gb/s
$F_{GTPPLLRANGE}$	GTP transceiver PLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz

Table 50: **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{GTPDRPCLK}$	GTPDRPCLK maximum frequency	175	175	156	125	MHz

Table 51: **GTP Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	660	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	–	60	%

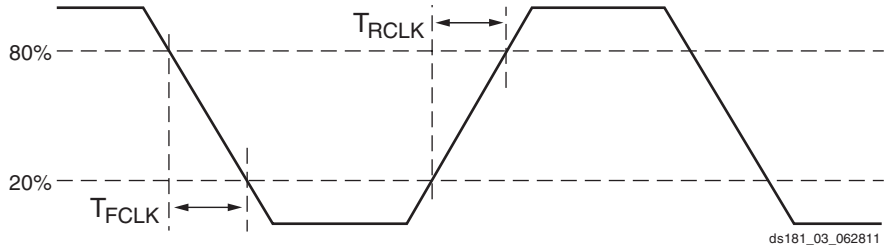

Figure 3: **Reference Clock Timing Parameters**

Table 52: **GTP Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time.	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	2.3 x10^6	UI

Table 53: **GTP Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
F_{TXOUT}	TXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		412.500	412.500	234.375	234.375	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	234.375	234.375	MHz

Notes:

1. Clocking must be implemented as described in UG482: *7 Series FPGAs GTP Transceiver User Guide*.

Table 54: **GTP Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.500	–	F_{GTPMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	50	–	ps
T_{FTX}	TX fall time	80%–20%	–	50	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	20	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{6.6}$	Total Jitter(2)(3)	6.6 Gb/s	–	–	0.30	UI
$DJ_{6.6}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(2)(3)	3.20 Gb/s(4)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(2)(3)	3.20 Gb/s(5)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(6)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(7)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{500}	Total Jitter(2)(3)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 55: **GTP Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTPRX}	Serial data rate	RX oversampler not enabled	0.500	–	F_{GTPMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	5000	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance		–1250	–	1250	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{6.6}$	Sinusoidal Jitter(3)	6.6 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal Jitter(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal Jitter(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total Jitter with Stressed Eye(8)	3.2 Gb/s	0.70	–	–	UI
$JT\_TJSE_{6.6}$		6.6 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal Jitter with Stressed Eye(8)	3.2 Gb/s	0.1	–	–	UI
$JT\_SJSE_{6.6}$		6.6 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter.

GTP Transceiver Protocol Jitter Characteristics

For Table 56 through Table 60, the UG482: *7 Series FPGAs GTP Transceiver User Guide* contains recommended settings for optimal usage of protocol specific characteristics.

Table 56: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 57: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 58: **PCI Express Protocol Characteristics(1)**

Standard	Description	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation					
PCI Express Gen 1	Total transmitter jitter	2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter	5000	–	0.25	UI
PCI Express Receiver High Frequency Jitter Tolerance					
PCI Express Gen 1	Total receiver jitter tolerance	2500	0.65	–	UI
PCI Express Gen 2(2)	Receiver inherent timing error	5000	0.40	–	UI
	Receiver inherent deterministic timing error		0.30	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

Table 59: **CEI-6G Protocol Characteristics**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

Table 60: **CPRI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2(1)	0.60	–	UI
	6144.0(1)	0.60	–	UI

Notes:

1. Tested to CEI-6G-SR.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

Table 61: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{USERCLK}$	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

XADC Specifications

Table 62: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±2	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Unipolar operation	–	–	±8	LSBs
		Bipolar operation	–	–	±4	LSBs
Gain Error			–	–	±0.5	%
Offset Matching			–	–	4	LSBs
Gain Matching			–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio(2)	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion(2)	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	70	–	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs(3)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate(4)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz

Table 62: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for BitGen option XADCEnhancedLinearity = ON.
3. For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
4. For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480).
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 63: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T_{PL}(1)	Program latency	5.00	5.00	5.00	5.00	ms, Max
T_{POR}(1)	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250.00	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay	150.00	150.00	150.00	150.00	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max

Table 63: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency	100.00	100.00	100.00	70.00	MHz, Max
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	DIN setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T_{CCO}	DOUT clock to out	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B setup/hold	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	7.00	7.00	7.00	8.00	ns, Max
T_{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	10.00	ns, Max
F_{RBCCK}	Readback frequency	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI setup/hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	8.50	ns, Max
F_{TCK}	TCK frequency	66.00	66.00	66.00	50.00	MHz, Max
BPI Flash Master Mode Programming Switching						
T_{BPICCO} (2)	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	10.00	ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] setup/hold	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Flash Master Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] setup/hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T_{SPICCM}	MOSI clock to out	8.00	8.00	8.00	9.00	ns, Max
$T_{SPICCFC}$	FCS_B clock to out	8.00	8.00	8.00	9.00	ns, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in UG470: *7 Series FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 64 lists the programming conditions specifically for eFUSE. For more information, see UG470: *7 Series FPGA Configuration User Guide*.

Table 64: **eFUSE Programming Conditions** (1)

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document:

Date	Version	Description
09/26/2011	1.0	Initial Xilinx release.
11/07/2011	1.1	Revised the V_{OCM} specification in Table 11. Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 12 and Table 13. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 34 and PLL to the symbol names in Table 35. In Table 36 through Table 43, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46.
02/13/2012	1.2	Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade. Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Updated the notes in Table 5. Added MGTAVCC and MGTAVTT power supply ramp times to Table 7. Rearranged Table 8, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 9 and Table 10. Revised the specifications in Table 11. Revised V_{IN} in Table 47. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the table. Revised F_{TXIN} and F_{RXIN} in Table 53. Revised I_{CCADC} and updated Note 1 in Table 62. Revised DDR LVDS transmitter data width in Table 14. Removed notes from Table 24 as they are no longer applicable. Updated specifications in Table 63. Updated Note 1 in Table 33.
06/01/2012	1.3	Reorganized entire data sheet including adding Table 40 and Table 44. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 8, updated many parameters including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 10. Updated V_{OL} in Table 11. Updated Table 14 and removed notes 2 and 3. Updated Table 15. Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document. In Table 27, updated Reset Delays section including Note 10 and Note 11. In Table 53, replaced F_{TXOUT} with F_{GLK}. Updated many of the XADC specifications in Table 62 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 63 to Table 34 and Table 35.
09/20/2012	1.4	In Table 1, updated the descriptions, changed V_{IN} and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet. Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 17 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 24.Changed F_{PFDMAX} conditions in Table 34 and Table 35. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 62, updated Note 1. In Table 63, updated T_{POR}.

Date	Version	Description
02/01/2013	1.5	Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 12 and Table 13 for -3, -2, -2L (1.0V), -1 speed specifications. Revised I_{DCIN} and I_{DCOUT} and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 12. Added a 2:1 memory controller section to Table 15. Updated Note 1 in Table 31. Revised Table 33. Updated Note 1 and Note 2 in Table 46. Updated D_{VPPIN} in Table 47. Updated V_{IDIFF} in Table 48. Removed T_{LOCK} and T_{PHASE} and revised F_{GCLK} in Table 51. Updated T_{DLOCK} in Table 52. Updated Table 53. In Table 54, updated T_{RTX}, T_{FTX}, $V_{TXOOBVDPP}$, and revised Note 1 through Note 7. In Table 55, updated RX_{SST} and RX_{PPMTOL} and revised Note 4 through Note 7. In Table 60, revised and added Note 1. Revised the maximum external channel input ranges in Table 62. In Table 63, revised F_{MCCK} and added the Internal Configuration Access Port section.
04/17/2013	1.6	Updated the AC Switching Characteristics based upon v1.07 of the ISE 14.5 and Vivado 2013.1 for the -3, -2, -2L (1.0V), and -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications. Production changes to Table 12 and Table 13 for -2L (0.9V) speed specifications. In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4 and combined Note 4 with old Note 5 and then added new Note 5. Revised V_{IN} description, removed Note 10, and added Note 6 in Table 2. Updated first 3 rows in Table 4. Also revised PCI33_3 voltage minimum in Table 8 to match values in Table 1 and Table 4. Added Note 1 to Table 11. Removed Note 1 from Table 13. Updated Table 15 title. Throughout the data sheet (Table 25, Table 26, and Table 41) removed the obvious note “A Zero “0” Hold Time listing indicates no hold time or a negative hold time.”

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