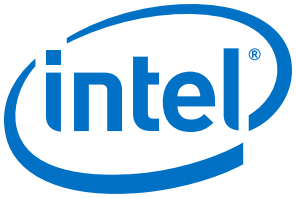

Intel® Stratix 10 Device Datasheet

S10-DATASHEET
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Contents

Stratix® 10 Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Stratix® 10 devices.

Table 1. Stratix 10 Device Grades and Speed Grades Supported

Device Grade	Speed Grade Supported
Extended	• –E1V (fastest) • –E2V • –E2L • –E3V • –E3X
Industrial	• –I1V • –I2V • –I2L • –I3V • –I3X

The suffix after the speed grade denotes the power options offered in Stratix 10 devices.

- V—SmartVID with standard static power
- L—0.85 V fixed voltage with low static power
- X—0.80 V fixed voltage with lowest static power

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Stratix 10 devices.

Operating Conditions

Stratix 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Stratix 10 devices, you must consider the operating requirements described in this section.

The Maximum Allowed Overshoot During Transitions specifications will be available in a future release of the *Stratix 10 Device Datasheet*.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Stratix 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2. Absolute Maximum Ratings for Stratix 10 Devices—Preliminary

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.26	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.26	V
V_{CCERAM}	Embedded memory and digital transceiver power supply	—	–0.50	1.24	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCIO_SDM}	Configuration pins power supply	—	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O (1)	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter analog power supply	—	–0.50	1.47	V

continued...

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCR_GXB}	Receiver analog power supply	—	–0.50	1.47	V
V_{CCH_GXB}	Transmitter output buffer power supply	—	–0.50	2.46	V
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	—	–0.50	1.30	V
V_{CCIO_HPS}	HPS I/O buffers power supply	LVDS I/O (1)	–0.50	2.46	V
V_{CCPLL_HPS}	HPS PLL power supply	—	–0.50	2.46	V
I_{OUT}	DC output current per pin	—	–25	40	mA
T_J	Operating junction temperature	—	–55	125	°C
T_{STG}	Storage temperature (no bias)	—	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

Table 3. Maximum Allowed Overshoot During Transitions for Stratix 10 Devices—Preliminary

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The LVDS I/O values are applicable to the VREFP_ADC and VREFN_ADC I/O pins.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O (2)	3 V I/O		
Vi (AC)	AC input voltage	2.50	3.80	100	%
		2.55	3.85	42	%
		2.60	3.90	18	%

continued...

(2) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition (V)		Overshoot Duration as % at T_J = 100°C	Unit
		LVDS I/O (2)	3 V I/O		
		2.65	3.95	9	%
		2.70	4.00	4	%
		> 2.70	> 4.00	No overshoot allowed	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Stratix 10 devices.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions for Stratix 10 Devices—Preliminary

This table lists the steady-state voltage values expected for Stratix 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum (3)	Typical	Maximum (3)	Unit
V_{CC}	Core voltage power supply	–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (4)	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
		–E2L, –I2L	0.82	0.85	0.88	V
		–E3X, –I3X	0.77	0.8	0.83	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (4)	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
		–E2L, –I2L	0.82	0.85	0.88	V
		–E3X, –I3X	0.77	0.8	0.83	V

continued...

(2) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(3) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the power distribution network (PDN) tool for the additional budget for the dynamic tolerance requirements.

(4) SmartVID graded devices require the use of a configurable voltage regulator or system controller to receive the device's settings through the Power Management Bus (PMBus™) or Pulse-Width Modulation (PWM) interface for proper performance.

Symbol	Description	Condition	Minimum (3)	Typical	Maximum (3)	Unit
V_{CCIO_SDM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
$V_{CCPLLDIG\_SDM}$	Secure Device Manager (SDM) block PLL digital power supply	—	0.87	0.9	0.93	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	2.35	2.4	2.45	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCERAM}	Embedded memory and digital transceiver power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} (5)	Battery back-up power supply (For design security volatile key register)	—	1.14	—	1.89	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.7	1.8	1.9	V
		1.5 V	1.4	1.5	1.6	V
		1.2 V	1.14	1.2	1.26	V
V_{CCIO_UIB}	Power supply for the Universal Interface Bus between the core and embedded HBM2 memory	1.2 V	0.9	1.2	1.5	V
V_{CCM}	Power supply for the embedded HBM2 memory	—	2.375	2.5	2.625	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V

continued...

(3) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the power distribution network (PDN) tool for the additional budget for the dynamic tolerance requirements.

(5) If you do not use the design security feature in Stratix 10 devices, connect V_{CCBAT} to a 1.8 V power supply. Stratix 10 power-on reset (POR) circuitry monitors V_{CCBAT}.

Symbol	Description	Condition	Minimum (3)	Typical	Maximum (3)	Unit
V_I (6)	DC input voltage	3 V I/O	–0.3	—	3.6	V
		LVDS I/O	–0.3	—	2.46	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
t_{RAMP} (7)(8)(9)(10)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

(3) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the power distribution network (PDN) tool for the additional budget for the dynamic tolerance requirements.

(6) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(7) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

(8) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(9) To support AS fast mode, all power supplies to the Stratix 10 device must be fully ramped-up within 10 ms to the recommended operating conditions.

(10) To support AS normal mode, V_{CCIO_SDM} of the Stratix 10 device must be fully ramped-up within 10 ms to the recommended operating condition.

Transceiver Power Supply Operating Conditions

Table 5. Transceiver Power Supply Operating Conditions for Stratix 10 GX/SX L- and H-Tile Devices—Preliminary

Symbol	Description	Condition (11)	Minimum (12)	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$	Transmitter power supply	Chip-to-Chip (13) ≤ 17.4 Gbps Or Backplane (14) ≤ 12.5 Gbps	1.0	1.03	1.06	V
$V_{CCR\_GXB[L,R]}$	Receiver power supply	Chip-to-Chip (13) ≤ 17.4 Gbps Or Backplane (14) ≤ 12.5 Gbps	1.0	1.03	1.06	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.710	1.8	1.890	V

Table 6. Transceiver Power Supply Operating Conditions for Stratix 10 GX/SX/TX/MX E-Tile Devices—Preliminary

Symbol	Description	Minimum (15)	Typical	Maximum (15)	Unit
V_{CCERT}	Transceiver power supply	0.87	0.9	0.93	V
V_{CCERT_PLL}	Transceiver PLL power supply	0.87	0.9	0.93	V
V_{CCEHT}	Analog power supply (15)	1.067	1.1	1.133	V

continued...

(11) These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Stratix 10 GX/SX Devices for exact data rate ranges.

(12) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(13) Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} and V_{CCT_GXB} = 1.12 V ± 20 mV.

(14) Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

(15) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Minimum (15)	Typical	Maximum (15)	Unit
V_{CCL}	Periphery circuitry power supply	0.725	0.75	0.775	V
$V_{CCN2P5V\_IO}$	LVPECL REFCLK power supply	2.375	2.5	2.625	V
V_{CCR}	Transceiver high voltage power supply	1.71	1.8	1.89	V

Note: Most VCCR_GXB and VCCT_GXB pins associated with unused transceiver channels can be grounded on a per-tile basis to minimize power consumption. Refer to the *Stratix 10 GX, GT, and SX Device Family Pin Connection Guidelines* and the Intel® Quartus® Prime pin report for information about pinning out the package to minimize power consumption for your specific design.

Related Links

Stratix 10 GX, GT, and SX Device Family Pin Connection Guidelines

HPS Power Supply Operating Conditions

Table 7. HPS Power Supply Operating Conditions for Stratix 10 Devices—Preliminary

This table lists the steady-state voltage and current values expected for Stratix 10 system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Stratix 10 Devices table for the steady-state voltage values expected from the FPGA portion of the Stratix 10 SoC devices.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	–E2L, –I2L, –E3X, –I3X	0.91	0.94	0.97	V
		–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (16)	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
$V_{CCPLLDIG\_HPS}$	HPS PLL digital power supply	–E2L, –I2L, –E3X, –I3X	0.91	0.94	0.97	V

continued...

(15) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(16) SmartVID graded devices require the use of a configurable voltage regulator or system controller to receive the device's settings through PMBUS or PWM for proper performance.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
		–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (16)	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
V_{CCPLL_HPS}	HPS PLL analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Links

- Recommended Operating Conditions on page 6
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance - Preliminary on page 51

DC Characteristics

The pin capacitance specifications will be available in a future release of the *Stratix 10 Device Datasheet*.

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

I/O Pin Leakage Current

Table 8. I/O Pin Leakage Current for Stratix 10 Devices—Preliminary

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 9. Bus Hold Parameters for Stratix 10 Devices—Preliminary

Parameter	Symbol	Condition	V_{CCIO} (V)								Unit
			1.2		1.5		1.8		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 10. OCT Calibration Accuracy Specifications for Stratix 10 Devices—Preliminary

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
48-Ω, 60-Ω, 80-Ω, and 240-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%

continued...

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 3.0, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω setting)	POD12 I/O standard, V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω, 48-Ω, 80-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω R_T	Internal parallel termination with calibration (25-Ω setting)	V_{CCIO} = 1.5	–10 to +40	–10 to +40	–10 to +40	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%

OCT Without Calibration Resistance Tolerance Specifications

Table 11. OCT Without Calibration Resistance Tolerance Specifications for Stratix 10 Devices—Preliminary

This table lists the Stratix 10 OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8, 1.5	TBD	TBD	TBD	%
		V_{CCIO} = 1.2	TBD	TBD	TBD	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5	TBD	TBD	TBD	%
		V_{CCIO} = 1.2	TBD	TBD	TBD	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8	±25	±35	±40	%

Figure 1. Equation for OCT Variation Without Recalibration—Preliminary

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. For SDM and HPS, the configuration I/O and peripheral I/O are supported with weak pull-up and weak pull-down options.

Table 12. Internal Weak Pull-Up Resistor Values for Stratix 10 Devices—Preliminary

Symbol	Description	Condition (V)	Nominal Value	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Related Links

Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Links

Recommended Operating Conditions on page 6

Single-Ended I/O Standards Specifications

Table 13. Single-Ended I/O Standards Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{IL}(V)		V_{IH}(V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (17) (mA)	I_{OH} (17) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
1.8 V	1.71	1.8	1.89	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

(17) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 1.8- V LVCMOS specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 14. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.16	1.2	1.24	—	Internally calibrated	—	—	V_{CCIO}	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 15. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix 10 Devices—Preliminary

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (18)	I_{OH} (18)
	Min	Max	Min	Max	Max	Min	Max	Min	(mA)	(mA)
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	(0.7 – 0.15) × V_{CCIO}	(0.7 + 0.15) × V_{CCIO}	—	—

(18) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Differential SSTL I/O Standards Specifications

Table 16. Differential SSTL I/O Standards Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{X(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Max	Min	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(19)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IL(AC)})$	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$ + 0.15
SSTL-135	1.283	1.35	1.45	0.18	(19)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$ + 0.15
SSTL-125	1.19	1.25	1.31	0.18	(19)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$ + 0.15

Differential HSTL and HSUL I/O Standards Specifications

Table 17. Differential HSTL and HSUL I/O Standards Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	0.3	V_{CCIO} + 0.48	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} – V_{REF})$	$2(V_{REF} – V_{IH(DC)})$	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IH(AC)})$	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} +0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}

(19) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Differential I/O Standards Specifications

Table 18. Differential I/O Standards Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (20)		$V_{ICM(DC)}$ (V)			V_{OD} (V) (21) (22)			V_{OCM} (V) (21)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (23)	1.71	1.8	1.89	100	—	0.05	Data rate ≤700 Mbps	1.65	0.247	—	0.6	1.125	1.25	1.375
						1	Data rate >700 Mbps	1.6						
RSDS (24)	1.71	1.8	1.89	100	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (25)	1.71	1.8	1.89	200	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL (26)	1.71	1.8	1.89	300	—	0.6	Data rate ≤700 Mbps	1.7	—	—	—	—	—	—
						1	Data rate >700 Mbps	1.6						

Switching Characteristics

This section provides the performance characteristics of Stratix 10 core and periphery blocks.

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(20) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(21) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(22) The specification is only applicable to default V_{OD} setting.

(23) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0.05 V to 1.65 V for data rates below 700 Mbps.

(24) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.4 V.

(25) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.4 V to 1.325 V.

(26) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

L-Tile Transceiver Performance Specifications

Transceiver Performance for Stratix 10 GX/SX L-Tile Devices

Table 19. L-Tile Transmitter and Receiver Data Rate Performance, VCCR_GXB and VCCT_GXB Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Chip-to-Chip (27) (28)	1 Gbps to 17.4 Gbps (29)	1.0	1.03	1.06	V
Backplane (27) (30)	1 Gbps to 12.5 Gbps (29)	1.0	1.03	1.06	V

Table 20. L-Tile ATX PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	8.7	GHz
	Minimum Frequency	500	MHz

Table 21. L-Tile Fractional PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

(27) Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} and V_{CCT_GXB} = 1.12 V ± 20 mV.

(28) Chip-to-chip refers to transceiver links that are short reach and dont require advanced equalization such as decision feedback equalization (DFE).

(29) Stratix 10 transceivers can support data rates below 1 Gbps through over sampling.

(30) Backplane applications refer to ones which require advanced equalization, such as DFE enabled, to compensate for channel loss.

Table 22. L-Tile CMU PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2.450	GHz

Transceiver Specifications for Stratix 10 GX/SX L-Tile Devices

Table 23. L-Tile Reference Clock Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		50 (31)	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V

continued...

(31) The f_{MIN} is 29 MHz when the fPLL is used as a core PLL.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} =1.03 V	—	1.03	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) (32)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 MHz to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
$T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$	Max spread spectrum clocking (SSC) df/dt			0.75	

Table 24. L-Tile Transceiver Clock Network Maximum Data Rate Specifications—Preliminary

Clock Network	Maximum Performance (33)			Channel Span	Unit
	ATX	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x24	16	12.5	N/A	2 banks up and 2 banks down	Gbps

(32) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(33) The maximum data rate depends on speed grade.

Table 25. L-Tile Receiver Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute V_{MAX} for a receiver pin (34)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin (34)	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration (35)	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (35)	V_{CCR_GXB} = 1.03 V (36)	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins (37)	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{ICM} (AC and DC coupled) non-PCIe channels	V_{CCR_GXB} = 1.03 V	—	700	—	mV
	V_{CCR_GXB} = 1.12 V	—	750	—	mV

continued...

(34) The device cannot tolerate prolonged operation at this absolute maximum.

(35) DC coupling specifications are pending silicon characterization.

(36) Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} and V_{CCT_GXB} = 1.12 V ± 20 mV.

(37) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
V_{ICM} (AC and DC coupled) PCIe channels	V_{CCR_GXB} = 1.03 V	—	650	—	mV
	V_{CCR_GXB} = 1.12 V	—	650	—	mV
t_{LTR} (38)	—	—	—	1	ms
t_{LTD} (39)	—	4	—	—	µs
t_{LTD_manual} (40)	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (41)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR ppm tolerance	PCIe-only	-300	—	300	ppm
	All other protocols	-1000	—	1000	ppm

Table 26. L-Tile Transmitter Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O (42)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω

continued...

(38) t_{LTR} is the time required for the receiver CDR to lock to the input reference clock frequency after coming out of reset.

(39) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(40) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(41) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(42) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Stratix 10 transceivers.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.03 V	—	515	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 1.03 V	—	515	—	mV
Rise time (43)	20% to 80%	20	—	130	ps
Fall time (43)	80% to 20%	20	—	130	ps
Intra-differential pair skew (44)	TX V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	ps

Table 27. L-Tile Typical Transmitter V_{OD} Settings—Preliminary

Symbol	V_{OD} Setting	V_{OD}/V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}/V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70
	21	0.67
	20	0.63

continued...

(43) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(44) In QPI mode, if V_{CM} < 0.17 V, the input Vid must be greater than 100 mV. If V_{CM} > 0.17 V, the input Vid must be greater than 70 mV.

Symbol	V_{OD} Setting	V_{OD}/V_{CCT_GXB} Ratio
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

Table 28. L-Tile Transmitter Channel-to-channel Skew Specifications—Preliminary

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps

Table 29. Transceiver Clocks Specifications for Stratix 10 GX/SX L-Tile Devices—Preliminary

Clock	Value	Unit
`reconfig_clk`	≤ 125	MHz
`fixed_clk` for the RX detect circuit	250 ± 20%	MHz

For OSC_CLK_1 specifications, refer to the External Configuration Clock Source Requirements section.

Related Links

- External Configuration Clock Source Requirements on page 80
- PLLs and Clock Networks

H-Tile Transceiver Performance Specifications

Transceiver Performance for Stratix 10 GX/SX H-Tile Devices

Table 30. H-Tile Transmitter and Receiver Data Rate Performance, VCCR_GXB and VCCT_GXB Specifications—Preliminary

Channel	Symbol/Description	Transceiver Speed Grades			Minimum	Typical	Maximum	
		-1	-2	-3				Unit
GX (45) (46)	Chip-to-Chip	1 Gbps to 17.4 Gbps (47)	1 Gbps to 17.4 Gbps (47)	1 Gbps to 17.4 Gbps (47)	1.0	1.03	1.06	V
	Backplane	1 Gbps to 17.4 Gbps (47)	1 Gbps to 17.4 Gbps (47)	1 Gbps to 17.4 Gbps (47)	1.0	1.03	1.06	V
GXT (48)	Chip-to-Chip	1 Gbps to 28.3 Gbps (47)	1 Gbps to 26 Gbps (47)	1 Gbps to 17.4 Gbps (47)	1.10	1.12	1.14	V
	Backplane	1 Gbps to 28.3 Gbps (47)	1 Gbps to 26 Gbps (47)	1 Gbps to 17.4 Gbps (47)	1.10	1.12	1.14	V

Table 31. H-Tile ATX PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	14.15	13	8.7	GHz
	Minimum Frequency	500			MHz

(45) GX channels are the transceiver channels that run at datarates ≤ 17.4 Gbps.

(46) Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that require 1.12 V ± 20 mV, VCCR_GXB and VCCT_GXB = 1.12 V ± 20 mV.

(47) Stratix 10 transceivers can support data rates below 1 Gbps through over sampling.

(48) GXT channels are the transceiver channels that run at datarates ≤ 28.3 Gbps.

Table 32. H-Tile Fractional PLL Performance—Preliminary

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

Table 33. H-Tile CMU PLL Performance—Preliminary

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2.450	GHz

Transceiver Specifications for GX/SX H-Tile Devices

Table 34. H-Tile Reference Clock Specifications—Preliminary

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		50 (49)	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω

continued...

(49) The f_{MIN} is 29 MHz when the fPLL is used as a core PLL.

Symbol/Description	Condition	Min	Typ	Max	Unit
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} =1.03 V	—	1.03	—	V
	V_{CCR_GXB} = 1.12 V	—	1.12	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) (50)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 MHz to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
$T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$	Max SSC df/dt			0.75	

(50) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

Table 35. H-Tile Transceiver Clock Network Maximum Data Rate Specifications—Preliminary

Clock Network	Maximum Performance (51)			Channel Span	Unit
	ATX	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x24	16	12.5	N/A	2 banks up and 2 banks down	Gbps
GXT clock lines	28.3	N/A	N/A	4 GXT channels within the same transceiver bank and 2 from the bank above or 2 from the bank below. (52)	Gbps

Table 36. H-Tile Receiver Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute V_{MAX} for a receiver pin (53)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin (53)	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration (54)	—	—	—	1.6	V

continued...

(51) The maximum data rate depends on speed grade.

(52) If the upper ATX PLL in a bank is used, then the channel span includes two GXT channels from the bank above. If the lower ATX PLL in a bank is used, then the channel span includes two channels from the bank below.

(53) The device cannot tolerate prolonged operation at this absolute maximum.

(54) DC coupling specifications are pending silicon characterization.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (54)	V_{CCR_GXB} = 1.03 V, 1.12 V (55), (58)	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins (56)	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{ICM} (AC and DC coupled) (57)	V_{CCR_GXB} = 1.03 V (58)	—	700	—	mV
	V_{CCR_GXB} = 1.12 V (58)	—	750	—	mV
t_{LTR} (59)	—	—	—	1	ms
t_{LTD} (60)	—	4	—	—	µs
t_{LTD_manual} (61)	—	4	—	—	µs

continued...

(55) Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} = 1.12 V ± 20 mV.

(56) The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(57) Stratix 10 devices support DC coupling to other Stratix 10 devices and other devices operating under the Hybrid Memory Cube (HMC) specifications.

(58) For GXT channels, V_{CCR_GXB} must be 1.12 V. For GX channels, V_{CCR_GXB} must be 1.03 V. V_{CCR_GXB} must be 1.12 V for the transceiver on the side of the device when using GX and GXT channels together.

(59) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(60) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$t_{LTR\_LTD\_manual}$ (62)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR ppm tolerance	PCIe-only	-300	—	300	ppm
	All other protocols	-1000	—	1000	ppm

Table 37. H-Tile Transmitter Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O (63)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.03 V (64)	—	515	—	mV
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.12 V (64)	—	560		mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 1.03 V (64)	—	515	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 1.12 V (64)	—	560	—	mV

continued...

(61) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(62) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(63) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Stratix 10 transceivers.

(64) For GXT channels, V_{CCT_GXB} must be 1.12 V. For GX channels, V_{CCT_GXB} must be 1.03 V. V_{CCT_GXB} must be 1.12 V for the transceiver bank when using GX and GXT channels together within the same bank.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Rise time (65)	20% to 80%	20	—	130	ps
Fall time (65)	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	ps

Table 38. H-Tile Typical Transmitter V_{OD} Settings—Preliminary

Symbol	V_{OD} Setting	V_{OD}/V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}/V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53

continued...

(65) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Symbol	V_{OD} Setting	V_{OD}/V_{CCT_GXB} Ratio
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

Table 39. H-Tile Transmitter Channel-to-channel Skew Specifications—Preliminary

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps

Table 40. Transceiver Clocks Specifications for Stratix 10 GX/SX H-Tile Devices—Preliminary

Clock	Value	Unit
`reconfig_clk`	≤ 125	MHz
`fixed_clk` for the RX detect circuit	250 ± 20%	MHz

For OSC_CLK_1 specifications, refer to the External Configuration Clock Source Requirements section.

Related Links

External Configuration Clock Source Requirements on page 80

E-Tile Transceiver Performance Specifications

Transceiver Performance for Stratix 10 E-Tile Devices

Table 41. E-Tile Transmitter and Receiver Data Rate Performance Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Supported datarate(66)	NRZ	1		30	Gbps
	PAM-4	2		56(67)	Gbps

Transceiver Reference Clock Specifications

Table 42. E-Tile Reference Clock Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
I/O standard		LVPECL			
Termination voltage (Vtt)	2.5 V compliant	0.4	0.5	0.6	V
	3.3 V tolerant	1.04	1.3	1.56	V
Termination resistor (Rtt)		40	50	60	ohm
Differential voltage (Vdiff)		0.4	0.8	1.2	V
Input common mode voltage (Vcm)	2.5 V compliant, no internal termination resister	Vdiff/2		VCCN2P5V_IO-Vdiff/2	V
	2.5 V compliant, internal termination resister	VCCN2P5V_IO-1.6	VCCN2P5V_IO-1.3	VCCN2P5V_IO-1	V
	3.3 V tolerant, no internal termination resister	Vdiff/2		VCCN2P5V_IO-Vdiff/2	V
	3.3 V tolerant, internal termination resister	1.4	2	2.6	V
Absolute voltage		-0.5		2.8	V

(66) The supported datarate is for chip-to-chip and backplane links.

(67) Two channels are combined to support up to 56 Gbps.

Transmitter Specifications for Stratix 10 E-Tile Devices

Table 43. E-Tile Transmitter Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Transmitter differential output voltage peak-to-peak	No precursor/postcursor de-emphasis		0.965		V
Transmiter commom mode voltage			$V_{CCERT}/2$		V

Receiver Specifications for Stratix 10 E-Tile Devices

Table 44. E-Tile Receiver Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Receiver run length(68)				100(69)	symbols
DC input impedance		40		60	ohm
DC differential input impedance		80	100	120	ohm
Powered down DC input impedance	Receiver pin impendance when the receiver termination is powered down	100k			ohm
Electrical Idle detection voltage	-	65		175	mV
Differential termination	From DC to 100 Mhz	80	100	120	ohm
PPM tolerance	Allowed frequency mismatch between REFCLK and RX data			750	ppm

(68) No additional transition density requirements apply.

(69) The incoming data must be statistically DC-balanced.

Core Performance Specifications

Clock Tree Specifications

Table 45. Clock Tree Performance for Stratix 10 Devices—Preliminary

Parameter	Performance			Unit
	–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	
Programmable clock routing	1,100	900	780	MHz

PLL Specifications

Fractional PLL Specifications

Table 46. Fractional PLL Specifications for Stratix 10 Devices—Preliminary

These specifications are applicable when fPLL is used in core mode.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	—	29	—	800 (70)	MHz
f_{INPFD}	Input clock frequency to the phase frequency detector (PFD)	—	29	—	700	MHz
f_{VCO}	PLL voltage-controlled oscillator (VCO) operating range for transceiver applications	—	6	—	12.5	GHz
	PLL voltage-controlled oscillator (VCO) operating range for core applications	—	4.3	—	12.5	GHz
$t_{EINDUTY}$	Input clock duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal clock	—	—	—	1	GHz
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `reconfig_clk`	—	—	—	125	MHz

continued...

(70) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	Non-SmartVID	—	—	±50	ps
		SmartVID	—	—	±75	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} (71), (72)	Input clock cycle-to-cycle jitter	F_{REF} ≥ 100 MHz	—	—	0.13	UI (p-p)
		F_{REF} < 100 MHz	—	—	±650	ps (p-p)
t_{OUTPJ} (73)	Period jitter for clock output	F_{OUT} ≥ 100 MHz	—	—	600	ps (p-p)
		F_{OUT} < 100 MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} (73)	Cycle-to-cycle jitter for clock output	F_{OUT} ≥ 100 MHz	—	—	600	ps (p-p)
		F_{OUT} < 100 MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Links

Memory Output Clock Jitter Specifications on page 49
Provides more information about the external memory interface clock output jitter specifications.

(71) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(72) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(73) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Stratix 10 Devices table.

I/O PLL Specifications

Table 47. I/O PLL Specifications for Stratix 10 Devices—Preliminary

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–1 speed grade	10	—	1,100 (74)	MHz
		–2 speed grade	10	—	900 (74)	MHz
		–3 speed grade	10	—	750 (74)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	PLL VCO operating range	–1 speed grade	600	—	1,600	MHz
		–2 speed grade	600	—	1,434	MHz
		–3 speed grade	600	—	1,250	MHz
f_{CLBW}	PLL closed-loop bandwidth	—	0.5	—	10	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal clock (C counter)	–1 speed grade	—	—	1,100	MHz
		–2 speed grade	—	—	900	MHz
		–3 speed grade	—	—	750	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1 speed grade	—	—	800	MHz
		–2 speed grade	—	—	720	MHz
		–3 speed grade	—	—	650	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	Non-SmartVID	45	50	55	%
		SmartVID	42	50	58	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	5	ns

continued...

(74) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	200	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	—	10	—	—	ns
t_{INCCJ} (75)(76)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.15	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	±750	ps (p-p)
t_{OUTPJ_DC}	Period jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} (77)	Period jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (77)	Cycle-to-cycle jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)

(75) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(76) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(77) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Stratix 10 Devices table.

Related Links

Memory Output Clock Jitter Specifications on page 49
Provides more information about the external memory interface clock output jitter specifications.

DSP Block Specifications

Table 48. DSP Block Performance Specifications for Stratix 10 Devices—Preliminary

Mode	Performance			Unit
	–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	
Fixed-point 18 × 19 multiplication mode	1,000	771	667	MHz
Fixed-point 27 × 27 multiplication mode (78)	1,000	771	667	MHz
Fixed-point 18 × 18 multiplier adder mode (78)	1,000	771	667	MHz
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode (78)	1,000	771	667	MHz
Fixed-point 18 × 19 systolic mode	1,000	771	667	MHz
Complex 18 × 19 multiplication mode	1,000	771	667	MHz
Floating point multiplication mode	750	579	500	MHz
Floating point adder or subtract mode	750	579	500	MHz
Floating point multiplier adder or subtract mode	750	579	500	MHz
Floating point multiplier accumulate mode	750	579	500	MHz
Floating point vector one mode	750	579	500	MHz
Floating point vector two mode	750	579	500	MHz

(78) When `chainin` or `chainout` is enabled, the performance specifications for the following speed grades are as follows:
- –E1V and –I1V: 750 MHz
- –E2V, –E2L, –I2V, and –I2L: 578 MHz
- –E3V, –E3X, –I3V, and –I3X: 507 MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 49. Memory Block Performance Specifications for Stratix 10 Devices—Preliminary

Memory	Mode	Performance			
		–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	Unit
MLAB	Single port, all supported widths (×16/×32)	1,000	782	667	MHz
	Simple dual-port, all supported widths (×16/×32)	1,000	782	667	MHz
	Simple dual-port with read-during-write option	550	450	400	MHz
	ROM, all supported width (×16/×32)	1,000	782	667	MHz
M20K Block	Single-port, all supported widths	1,000	782	667	MHz
	Simple dual-port, all supported widths	1,000	782	667	MHz
	Simple dual-port, coherent read enabled	1,000	782	667	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	800	640	560	MHz
	Simple dual-port with ECC enabled, 512 × 32	600	480	420	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	1,000	782	667	MHz
	True dual port, all supported widths	600	480	420	MHz
	Simple quad-port, all supported widths	600	480	420	MHz
	ROM, all supported widths	1,000	782	667	MHz
eSRAM	Simple dual-port	500–750	500–700	500–640	MHz

Internal Temperature Sensing Diode Specifications

Table 50. Internal Temperature Sensing Diode Specifications for Stratix 10 Devices—Preliminary

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40 to 125 °C	±5 °C	No	1 KSPS	< 5 ms	11 bits	11 bits

Internal Voltage Sensor Specifications

Table 51. Internal Voltage Sensor Specifications for Stratix 10 Devices—Preliminary

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	8	—	Bit
Sampling rate		—	—	1.0 (79)	KSPS
Differential non-linearity (DNL)		—	—	±1	LSB
Integral non-linearity (INL)		—	—	±1	LSB
Input capacitance		—	—	40	pF
Clock frequency		—	—	550	MHz
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.5	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.25	V

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

(79) Pending silicon characterization.

High-Speed I/O Specifications

Table 52. High-Speed I/O Specifications for Stratix 10 Devices—Preliminary

When serializer/deserializer (SERDES) factor J = 3 to 10, use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40 (80)	10	—	800	10	—	700	10	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40 (80)	10	—	625	10	—	625	10	—	525	MHz
f_{HSCLK_OUT} (output clock frequency)		—	—	—	800 (81)	—	—	700 (81)	—	—	625 (81)	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate) (82)	SERDES factor J = 4 to 10 (83)(85) (84)	(85)	—	1600 (86)	(85)	—	1434 (86)	(85)	—	1250 (86)	Mbps

continued...

(80) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(81) This is achieved by using the PHY clock network.

(82) Requires package skew compensation with PCB trace length.

(83) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(84) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(85) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(86) Pending silicon characterization.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 3 (83)(85)(84)	(85)	—	(86)	(85)	—	(86)	(85)	—	(86)	Mbps
		SERDES factor J = 2, uses DDR registers	(85)	—	840 (86)(87)	(85)	—	(86)(87)	(85)	—	(86)(87)	Mbps
		SERDES factor J = 1, uses DDR registers	(85)	—	420 (86)(87)	(85)	—	(86)(87)	(85)	—	(86)(87)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	160	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.12	—	—	0.15	UI
	t_{DUTY} (88)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
	t_{RISE} & t_{FALL} (84)(89)	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	ps
	TCCS (88)(82)	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 (83)(85)(84)	—	—	1600	—	—	1434	—	—	1250	Mbps
		SERDES factor J = 3 (83)(85)(84)	—	—	(86)	—	—	(86)	—	—	(86)	Mbps
	f_{HSDR} (data rate) (without DPA) (82)	SERDES factor J = 3 to 10	(85)	—	(90)	(85)	—	(90)	(85)	—	(90)	Mbps

continued...

(87) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

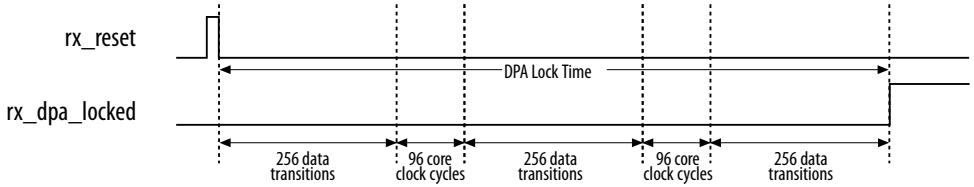
(88) Not applicable for DIVCLK = 1.

(89) This applies to default pre-emphasis and V_{OD} settings only.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 2, uses DDR registers	(85)	—	(87)	(85)	—	(87)	(85)	—	(87)	Mbps
		SERDES factor J = 1, uses DDR registers	(85)	—	(87)	(85)	—	(87)	(85)	—	(87)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

DPA Lock Time Specifications

Figure 2. DPA Lock Time Specifications with DPA PLL Calibration Enabled



(90) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

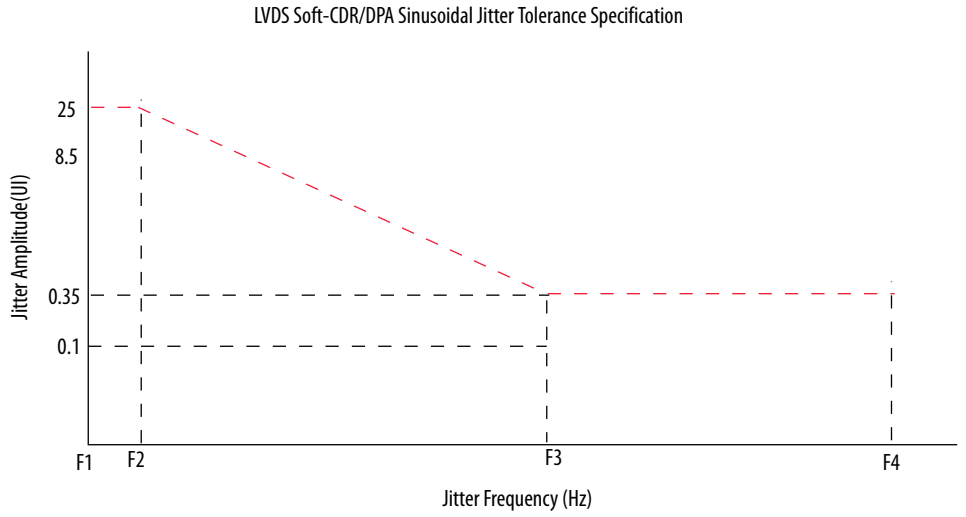
Table 53. DPA Lock Time Specifications for Stratix 10 Devices—Preliminary

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (91)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

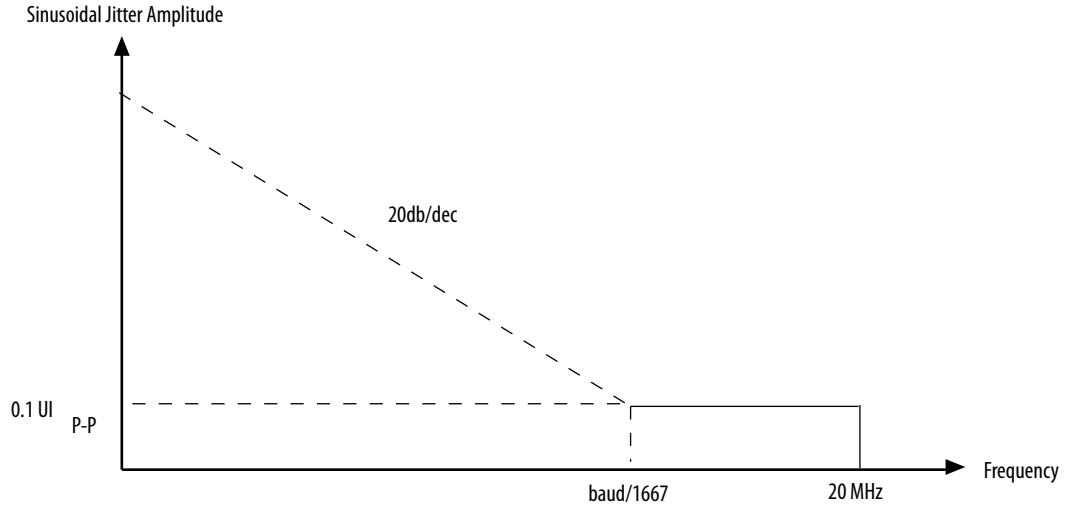


(91) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Table 54. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps—Preliminary

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.35
F4	50,000,000	0.35

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



DLL Range Specifications

Table 55. DLL Frequency Range Specifications for Stratix 10 Devices—Preliminary

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1,333 (92)	MHz
DLL reference clock input	Minimum 667 (93)	MHz

DQS Logic Block Specifications

Table 56. DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix 10 Devices—Preliminary

This error specification is the absolute maximum and minimum error.

Symbol	Performance			Unit
	–1 Speed Grade	–2 Speed Grade	–3 Speed Grade	
t_{DQS_PSERR}	4	6	8	ps

Memory Output Clock Jitter Specifications

Table 57. Memory Output Clock Jitter Specifications for Stratix 10 Devices—Preliminary

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

Clock Network	Parameter	Symbol	Performance			Unit
			–1 Speed Grade	–2 Speed Grade	–3 Speed Grade	
PHY clock	Clock period jitter	$t_{JIT(per)}$	58	58	58	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	58	58	58	ps
	Duty cycle jitter	$t_{JIT(duty)}$	58	58	58	ps

(92) In the SX device family, if the HPS EMIF is instantiated, the maximum speed for that instantiation is 1,066 MHz.

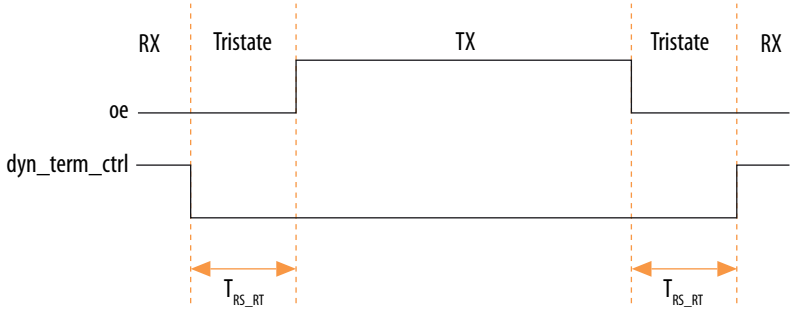
(93) To support interfaces below 667 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

OCT Calibration Block Specifications

Table 58. OCT Calibration Block Specifications for Stratix 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	TBD	—	ns

Figure 5. Timing Diagram for on oe and dyn_term_ctrl Signals



HPS Performance Specifications - Preliminary

This section provides hard processor system (HPS) specifications and timing for Intel Stratix 10 devices.

HPS Clock Performance - Preliminary

Table 59. Maximum HPS Clock Frequencies for Intel Stratix 10 Devices

Performance	VCCL_HPS (V)	MPU Frequency (MHz)	SDRAM Interconnect Frequency(94) (MHz)	L3 Interconnect Frequency (MHz)
–E1V, –I1V	SmartVID	1200	533	400
	0.9	1200	533	400
	0.94	TBD	533	400
–E2V, –I2V	SmartVID	1000	467	400
	0.9	1000	467	400
	0.94	1000	467	400
–E3V, –I3V	SmartVID	800	400	333
	0.9	800	400	333
	0.94	1000	400	400
–E2L, –I2L(95)	0.9	1200	467	400
	0.94	TBD	467	400
–E3X, –I3X (95)	0.9	1200	400	400
	0.94	TBD	400	400

Related Links

External Memory Interface Spec Estimator
Provides the specific details of the maximum allowed SDRAM operating frequency, which is twice the frequency of hmc_free_clk.

(94) `hmc_free_clk`

(95) Note that V_{CCL_HPS} can not be connected to SmartVID for –E2L, –I2L, –E3X, and –I3X devices.

HPS PLL Specifications - Preliminary

HPS PLL Input Requirements - Preliminary

Table 60. HPS PLL Input Requirements for Intel Stratix 10 Devices

The main HPS PLL receives its clock signals from the HPS_OSC_CLK pin. Refer to the *Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines* for information about assigning this pin.

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	TBD	—	50	PPM
Clock input duty cycle	45	50	55	%

HPS PLL Performance - Preliminary

Table 61. HPS PLL Performance for Intel Stratix 10 Devices

Description	Min	Max	Unit
Main PLL VCO output	—	3000	MHz
Peripheral PLL VCO output	—	3000	MHz
h2f_user0_clk (96)	—	500	MHz
h2f_user1_clk (96)	—	500	MHz

(96) The HPS PLL provides this clock to the FPGA fabric.

HPS SPI Timing Characteristics - Preliminary

Table 62. SPI Master Timing Requirements for Intel Stratix 10 Devices

You can adjust the input delay timing by programming the `rx_sample_dly` register.

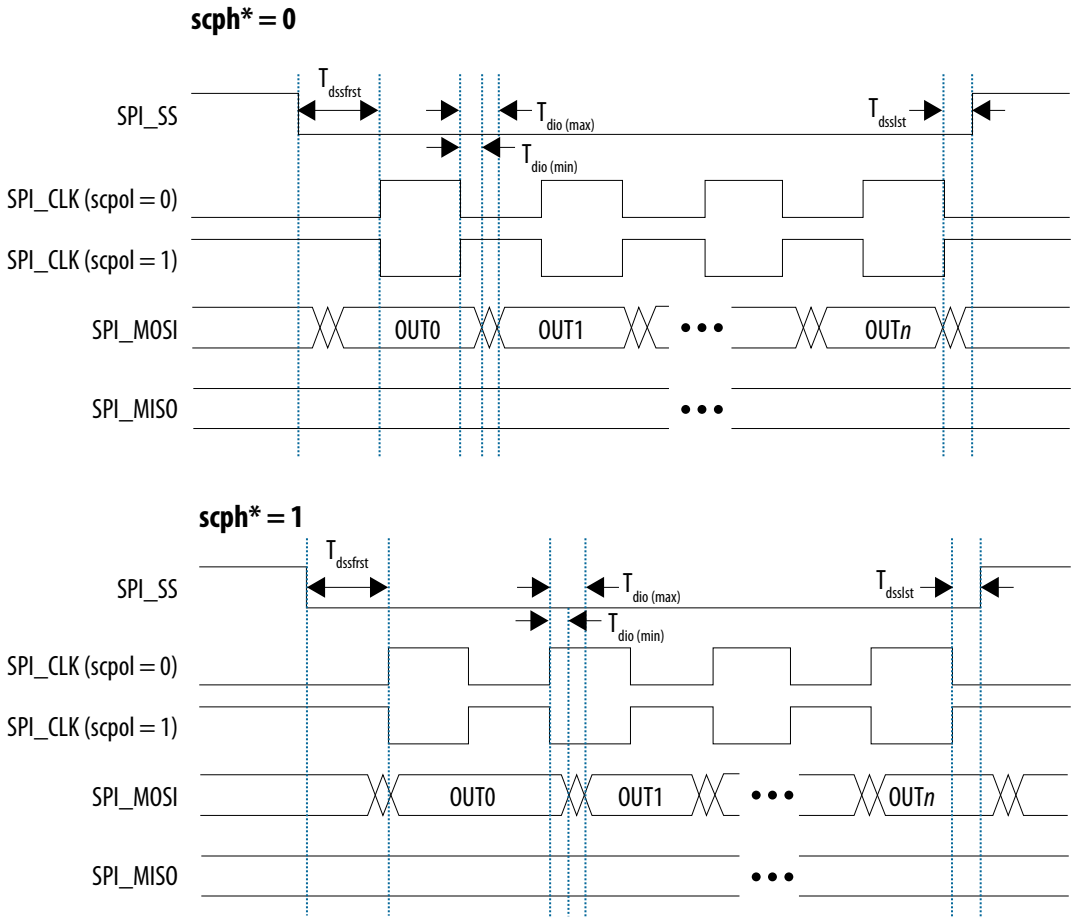
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	5	—	—	ns
T_{clk}	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_{ck_jitter}	SPIM_CLK output jitter	—	—	2	%
T_{dio}	Master-out slave-in (MOSI) output skew	–3	—	2	ns
$T_{dssfrst}$ (97)	SPI_SS_N asserted to first SPIM_CLK edge	$(1.5 \times T_{spi\_ref\_clk}) - 2$	—	—	ns
T_{dsslst} (97)	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} - 2$	—	—	ns
T_{su} (98)	SPIM_MISO setup time with respect to SPIM_CLK capture edge	$4.5 - (rx\_sample\_dly \times T_{spi\_ref\_clk})$ (99)	—	—	ns
T_h (98)	Input hold in respect to SPIM_CLK capture edge	$1.3 + (rx\_sample\_dly \times T_{spi\_ref\_clk})$	—	—	ns

(97) SPI_SS_N behavior differs depending on Motorola SPI, TI SSP or Microwire operational mode.

(98) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for TI SSP, the capture edge is the falling edge; for Microwire, the capture edge is the rising edge.

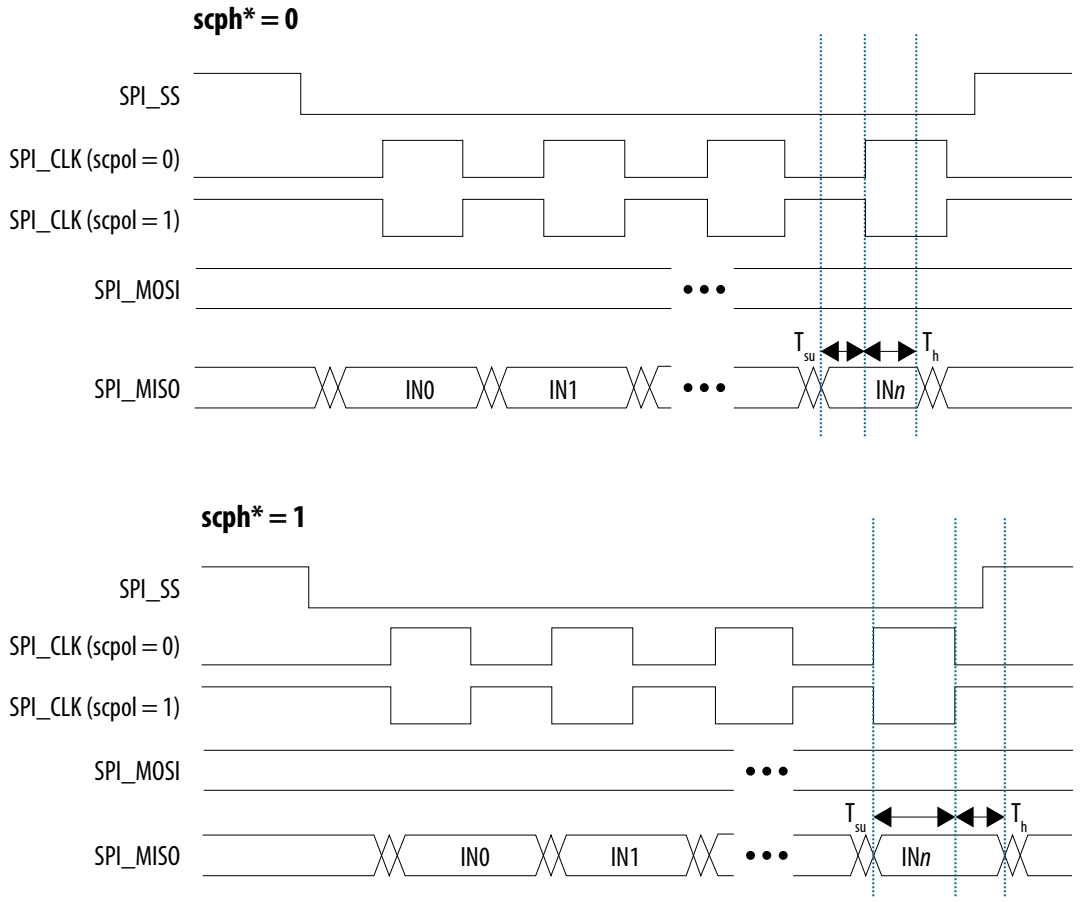
(99) Valid values of `rx_sample_dly` range from 1 to 64 (units are in $T_{spi\_ref\_clk}$ steps)

Figure 6. SPI Master Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 7. SPI Master Input Timing Diagram

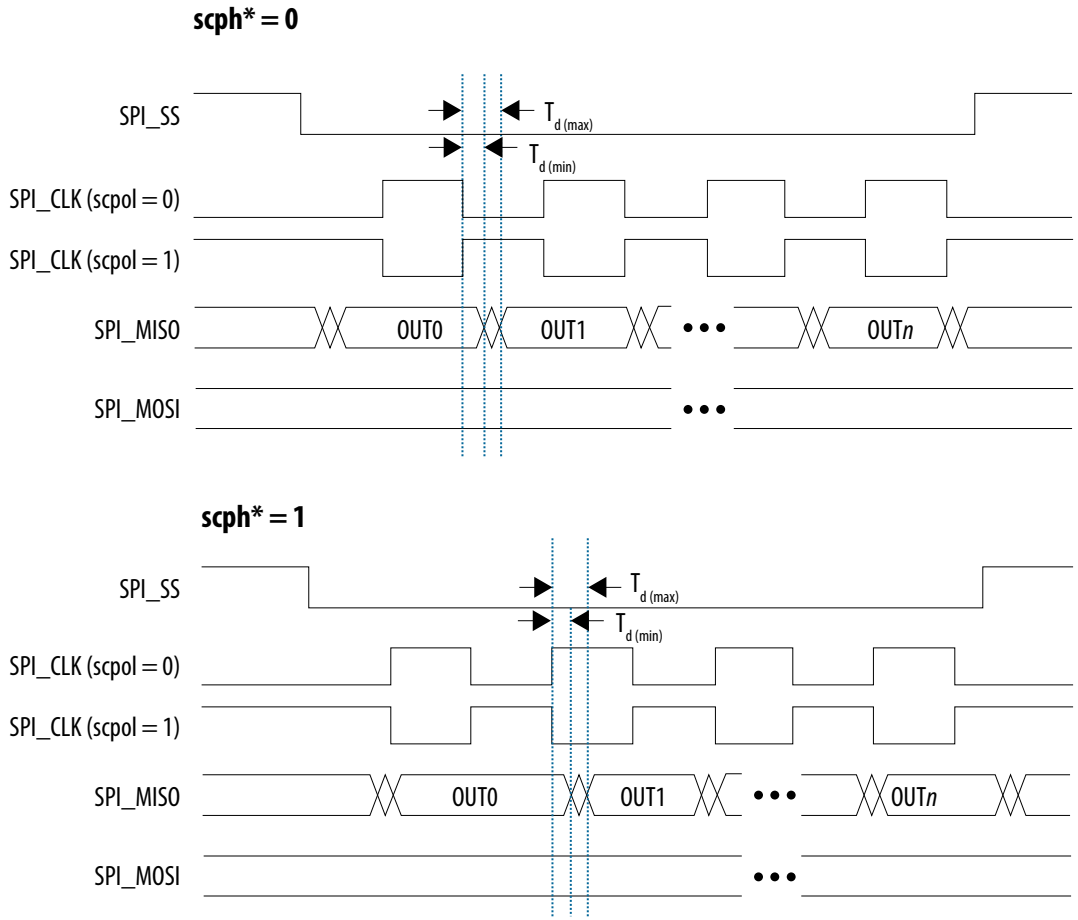


*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Table 63. SPI Slave Timing Requirements for Intel Stratix 10 Devices

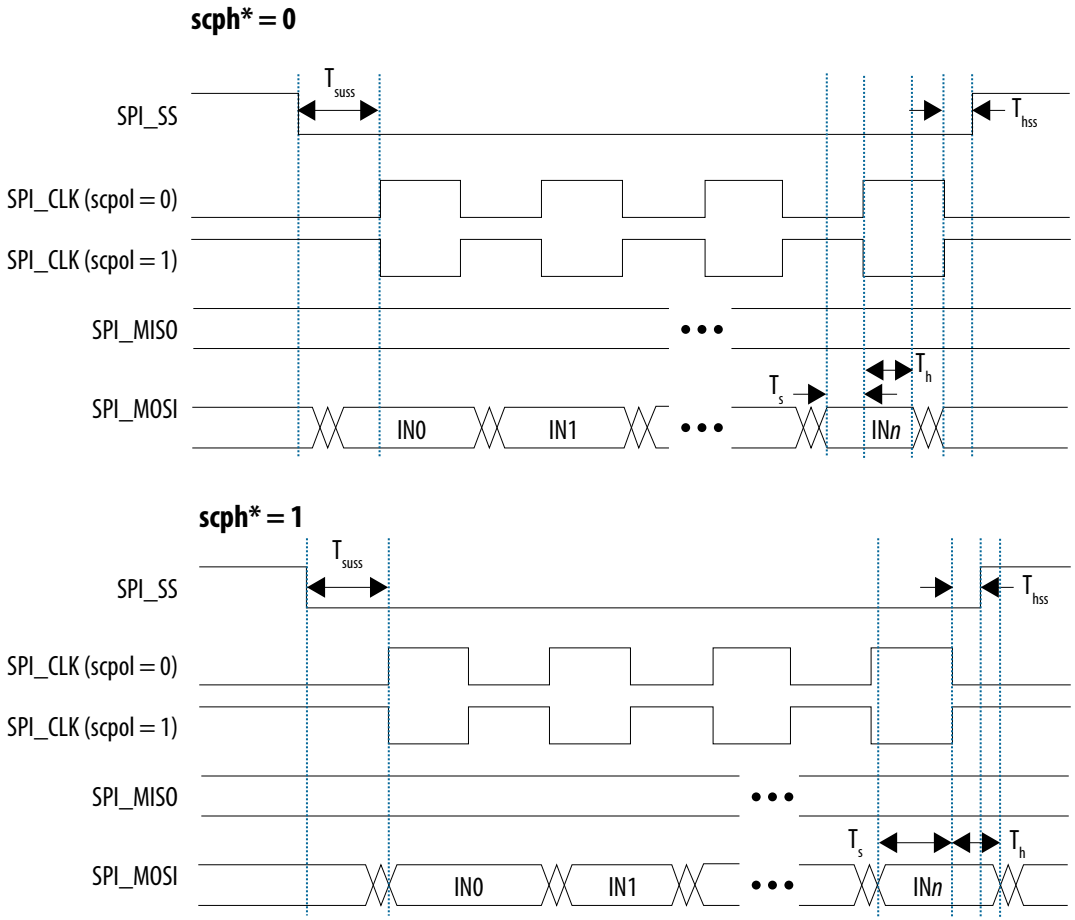
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	5	—	—	ns
T_{clk}	SPIM_CLK clock period	30	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_d	Master-in slave-out (MISO) output skew	$(2 \times T_{spi\_ref\_clk}) + 3$	—	$(3 \times T_{spi\_ref\_clk}) + 11$	ns
T_{su}	Master-out slave-in (MOSI) setup time	4	—	—	ns
T_h	Master-out slave-in (MOSI) hold time	0	—	—	ns
T_{suss}	SPI_SS_N asserted to first SPIM_CLK edge	$T_{spi\_ref\_clk} + 4$	—	—	ns
T_{hss}	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} + 4$	—	—	ns

Figure 8. SPI Slave Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 9. SPI Slave Input Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Related Links

SPI Controller

For more information about the SPI controller and timing, refer to the *SPI Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*

HPS SD/MMC Timing Characteristics - Preliminary

Table 64. Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Stratix 10 Devices

These timings apply to SD, MMC, and embedded MMC (eMMC) cards operating at 1.8 V.

Symbol	Description	Min	Typ	Max	Unit
T_{sdmmc_cclk}	SDMMC_CCLK clock period (Identification mode)	2500	—	—	ns
	SDMMC_CCLK clock period (SDR12)	40	—	—	ns
	SDMMC_CCLK clock period (SDR25)	20	—	—	ns
$T_{dutycycle}$	SDMMC_CCLK duty cycle	45	50	55	%
$T_{sdmmc\_cclk\_jitter}$	SDMMC_CCLK output jitter	—	—	2	%
T_{sdmmc_clk}	Internal reference clock before division by 4. Sourced by l4_mp_clk	5	—	—	ns
T_d	SDMMC_CMD/SDMMC_DATA[7:0] output delay (100)	T_{sdmmc_clk} × drvsel/2(101)	—	3 + (T_{sdmmc_clk} × drvsel/2) (101)	ns
T_{su}	SDMMC_CMD/SDMMC_DATA[7:0] input setup (102)	6 – (T_{sdmmc_clk} × smplsel/2)	—	—	ns
T_h	SDMMC_CMD/SDMMC_DATA[7:0] input hold (102)	0.5 + (T_{sdmmc_clk} × smplsel/2)	—	—	ns

None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

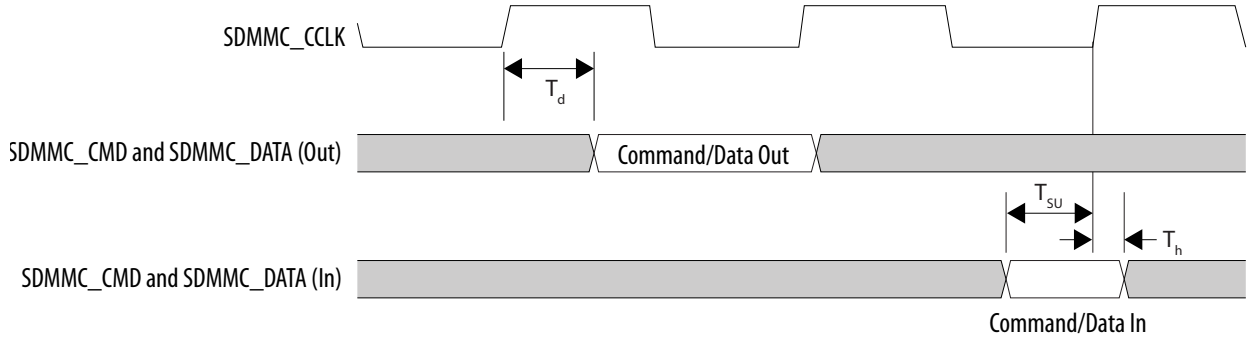
Note: SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

(100) When the drvsel bitfield in the sdmmc register is set to 3 (in the system manager) and the reference clock (l4_mp_clk) is 200 MHz for example, the output delay time is 7.5 to 10.5 ns.

(101) sdmmc_clk, sourced from l4_mp_clk, is the SD/MMC controller reference clock.

(102) When the smplsel bitfield in the sdmmc register is set to 2 (in the system manager) and the reference clock (l4_mp_clk) is 200 MHz for example, the setup time is 1 ns and the hold time is 5.5 ns.

Figure 10. SD/MMC Timing Diagram



Related Links

SD/MMC Controller

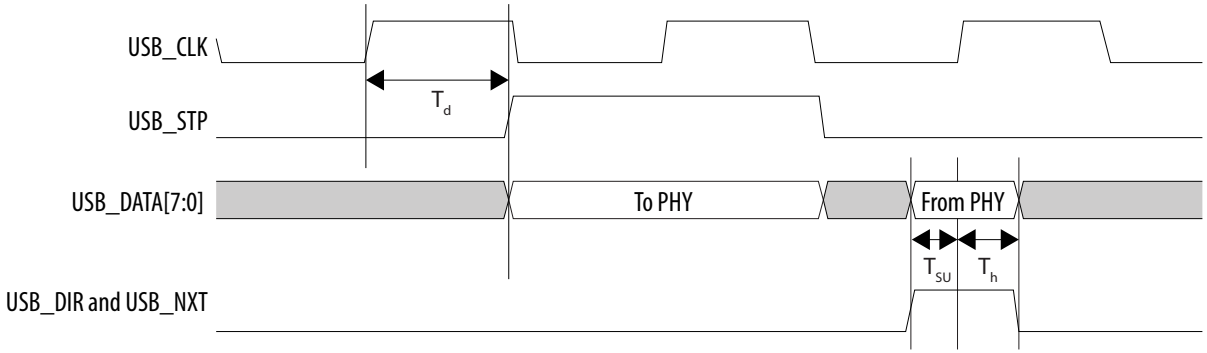
For more information about the SD/MMC controller and timing, refer to the *SD/MMC Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*

HPS USB UPLI Timing Characteristics - Preliminary

Table 65. USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/USB_DATA[7:0] output delay	1.5	—	7	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	3.5	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	0.5	—	—	ns

Figure 11. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

Related Links

USB 2.0 OTG Controller

For more information about the USB 2.0 OTG controller and timing, refer to the *USB 2.0 OTG Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*

HPS Ethernet Media Access Controller (EMAC) Timing Characteristics - Preliminary

Table 66. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	8 – 50 PPM	8	8 + 50 PPM	ns
T_{clk} (100Base-T)	TX_CLK clock period	40 – 50 PPM	40	40 + 50 PPM	ns
T_{clk} (10Base-T)	TX_CLK clock period	400 – 50 PPM	400	400 + 50 PPM	ns
$T_{dutycycle}$ (1000Base-T)	TX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$(10/100Base-T)	TX_CLK duty cycle	40	50	60	%
T_d (103) (104)	TXD/TX_CTL to TX_CLK output skew	–0.5	—	0.5	ns

Figure 12. RGMII TX Timing Diagram

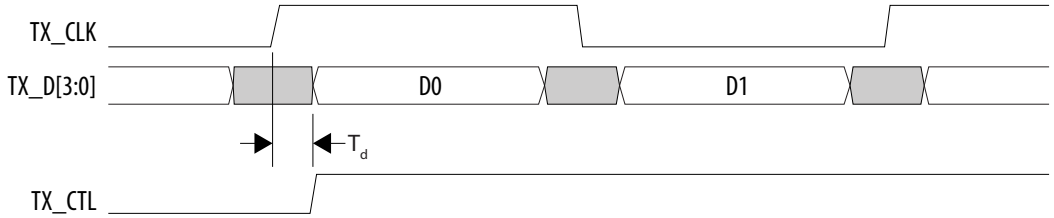


Table 67. RGMII RX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	8 - 50 PPM	8	8 + 50 PPM	ns
T_{clk} (100Base-T)	RX_CLK clock period	40 - 50 PPM	40	40 + 50 PPM	ns

continued...

(103) Rise and fall times depend on the I/O standard, drive strength, and loading. Intel recommends simulating your configuration.

(104) If you connect a PHY that does not implement clock-to-data skew, you can delay TX_CLK by 1.5—2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1-ns data-to-clock skew requirement.

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (10Base-T)	RX_CLK clock period	400 - 50 PPM	400	400 + 50 PPM	ns
$T_{dutycycle}$(1000Base-T)	RX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$(10/100Base-T)	RX_CLK duty cycle	40	50	60	%
T_{su}	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
T_h (105)	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

Figure 13. RGMII RX Timing Diagram

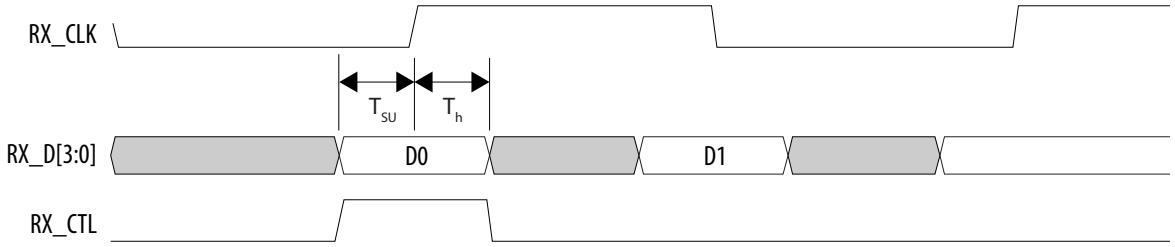


Table 68. Reduced Media Independent Interface (RMII) Clock Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	REF_CLK clock period, sourced by HPS TX_CLK	20 - 50 PPM	20	20 + 50 PPM	ns
	REF_CLK clock period, sourced by external clock source	20 - 50 PPM	20	20 + 50 PPM	ns
$T_{dutycycle\_int}$	Clock duty cycle, REF_CLK sourced by TX_CLK	35	50	65	%
$T_{dutycycle\_ext}$	Clock duty cycle, REF_CLK sourced by external clock source	35	50	65	%

Table 69. RMII TX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_d	TX_CLK to TXD/TX_CTL output data delay	2	—	10	ns

(105) If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX_CLK by 1.5-2 ns, using the HPS I/O programmable delay.

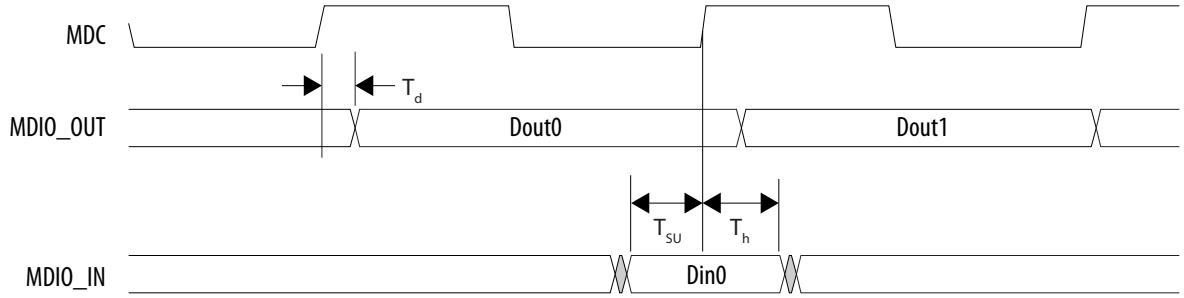
Table 70. RMII RX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{su}	RX_D/RX_CTL setup time	2	—	—	ns
T_h	RX_D/RX_CTL hold time	1	—	—	ns

Table 71. Management Data Input/Output (MDIO) Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	—	400	—	ns
T_d	MDC to MDIO output data delay	10	—	20	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 14. MDIO Timing Diagram



Related Links

Ethernet Media Access Controller

For more information about the Ethernet MAC and timing, refer to the *Ethernet Media Access Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*

HPS I²C Timing Characteristics - Preliminary

Table 72. I²C Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
T_{clk_jitter}	I2C clock output jitter	—	2	—	2	%
T_{HIGH} (106)	SCL high period	4 (107)	—	0.6 (108)	—	µs
T_{LOW} (109)	SCL low period	4.7 (110)	—	1.3 (111)	—	µs
$T_{SU;DAT}$	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
$T_{HD;DAT}$ (112)	Hold time for SCL to SDA data	0	3.15	0	0.6	µs
$T_{VD;DAT}$ and $T_{VD;ACK}$ (113)	SCL to SDA output data delay	—	3.45 (114)	—	0.9 (115)	µs

continued...

(106) You can adjust T_{high} using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(107) The recommended minimum setting for `ic_ss_scl_hcnt` is 440.

(108) The recommended minimum setting for `ic_fs_scl_hcnt` is 71.

(109) You can adjust T_{low} using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(110) The recommended minimum setting for `ic_ss_scl_lcnt` is 500.

(111) The recommended minimum setting for `ic_fs_scl_lcnt` is 141.

(112) $T_{HD;DAT}$ is affected by the rise and fall time.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
$T_{SU;STA}$	Setup time for a repeated start condition	4.7	—	0.6	—	µs
$T_{HD;STA}$	Hold time for a repeated start condition	4	—	0.6	—	µs
$T_{SU;STO}$	Setup time for a stop condition	4	—	0.6	—	µs
T_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	µs
$T_{scl:r}$ (116)	SCL rise time	—	1000	20	300	ns
$T_{scl:f}$ (116)	SCL fall time	—	300	6.54	300	ns
$T_{sda:r}$ (116)	SDA rise time	—	1000	20	300	ns
$T_{sda:f}$ (116)	SDA fall time	—	300	6.54	300	ns

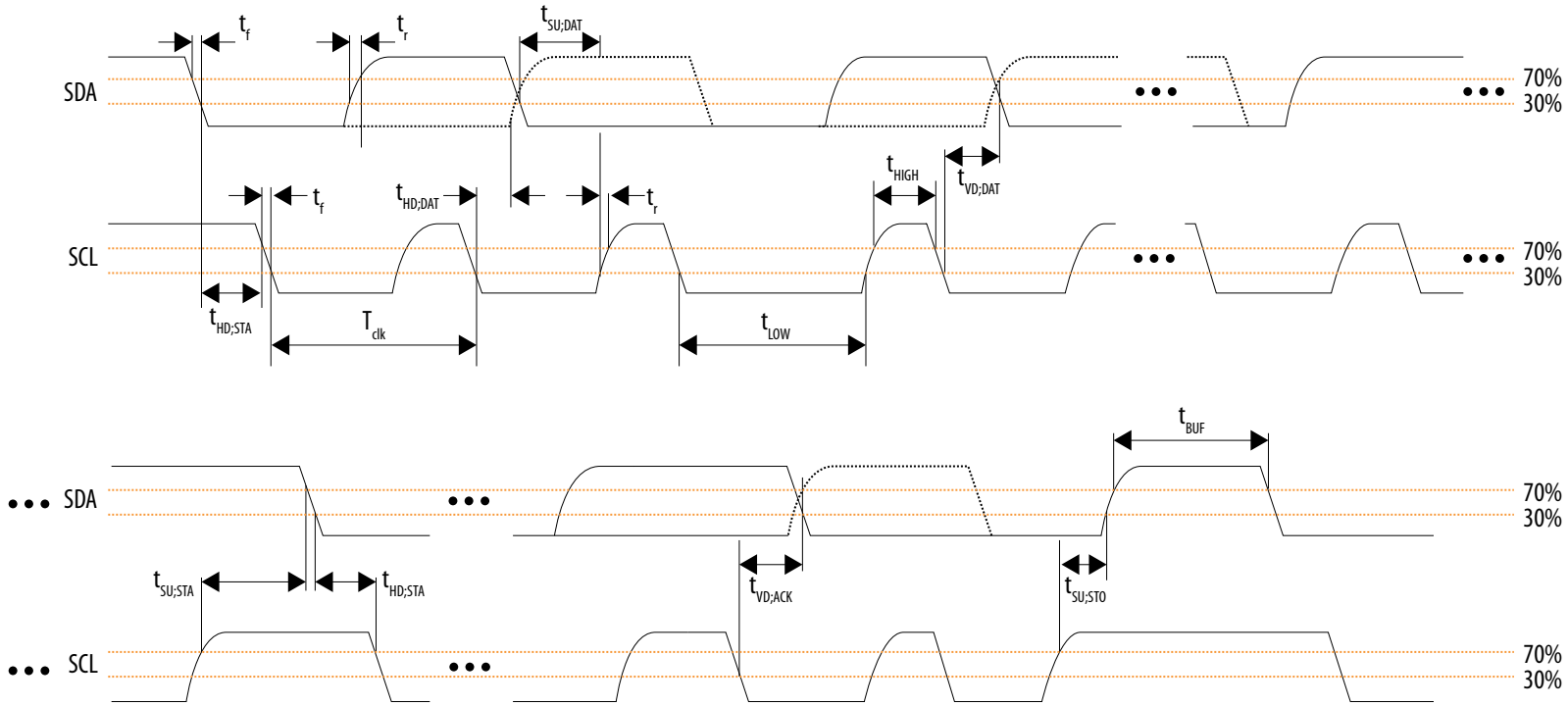
(113) $T_{VD;DAT}$ and $T_{VD;ACK}$ are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the `ic_sda_hold` register).

(114) Use maximum SDA_HOLD = 240 to be within the specification.

(115) Use maximum SDA_HOLD = 60 to be within the specification.

(116) Rise and fall time parameters vary depending on external factors such as the characteristics of the IO driver, pull-up resistor value, and total capacitance on the transmission line.

Figure 15. I²C Timing Diagram



Related Links

I²C Controller

For more information about the I²C controller and timing, refer to the *I²C Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*

HPS NAND Timing Characteristics - Preliminary

Table 73. NAND ONFI 1.0 Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Max	Unit
T_{WP} (117)	Write enable pulse width	10	—	ns
T_{WH} (117)	Write enable hold time	7	—	ns
T_{RP} (117)	Read enable pulse width	10	—	ns
T_{REH} (117)	Read enable hold time	7	—	ns
T_{CLS} (117)	Command latch enable to write enable setup time	10	—	ns
T_{CLH} (117)	Command latch enable to write enable hold time	5	—	ns
T_{CS} (117)	Chip enable to write enable setup time	15	—	ns
T_{CH} (117)	Chip enable to write enable hold time	5	—	ns
T_{ALS} (117)	Address latch enable to write enable setup time	10	—	ns
T_{ALH} (117)	Address latch enable to write enable hold time	5	—	ns
T_{DS} (117)	Data to write enable setup time	7	—	ns
T_{DH} (117)	Data to write enable hold time	5	—	ns
T_{WB} (117)	Write enable high to R/B low	—	200	ns
T_{CEA}	Chip enable to data access time	—	100	ns
T_{REA}	Read enable to data access time	—	40	ns
T_{RHZ}	Read enable to data high impedance	—	200	ns
T_{RR}	Ready to read enable low	20	—	ns

(117) This timing is software programmable. Refer to the *NAND Flash Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual* for more information about software-programmable timing in the NAND flash controller.

Figure 16. NAND Command Latch Timing Diagram

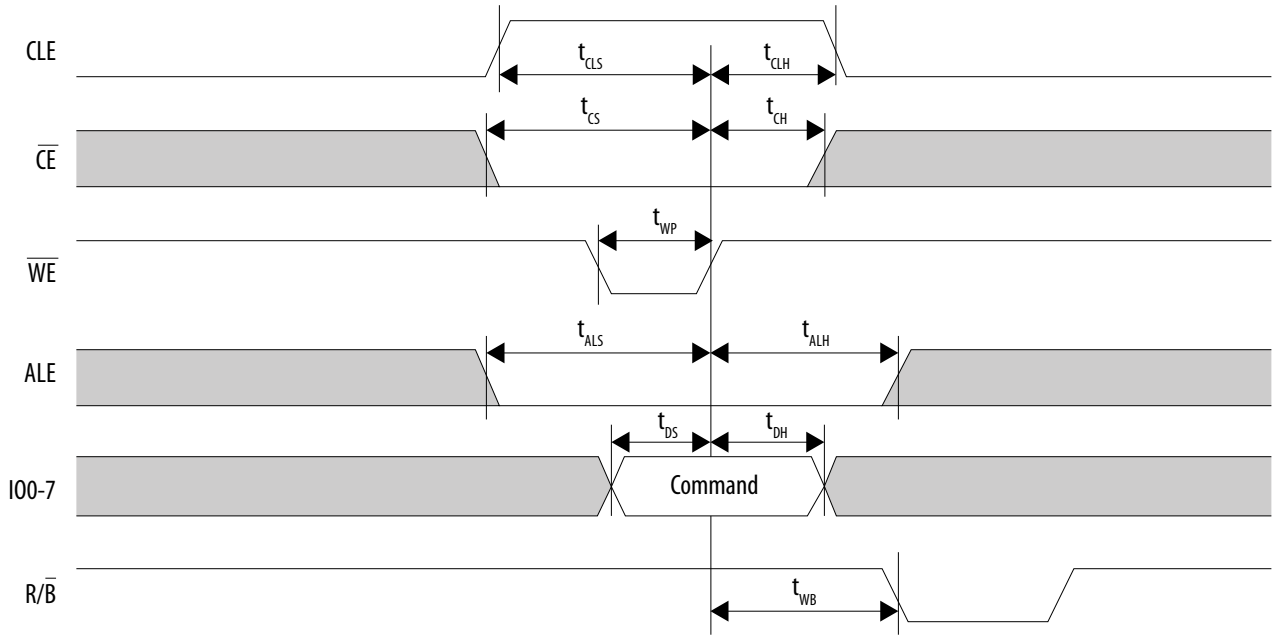


Figure 17. NAND Address Latch Timing Diagram

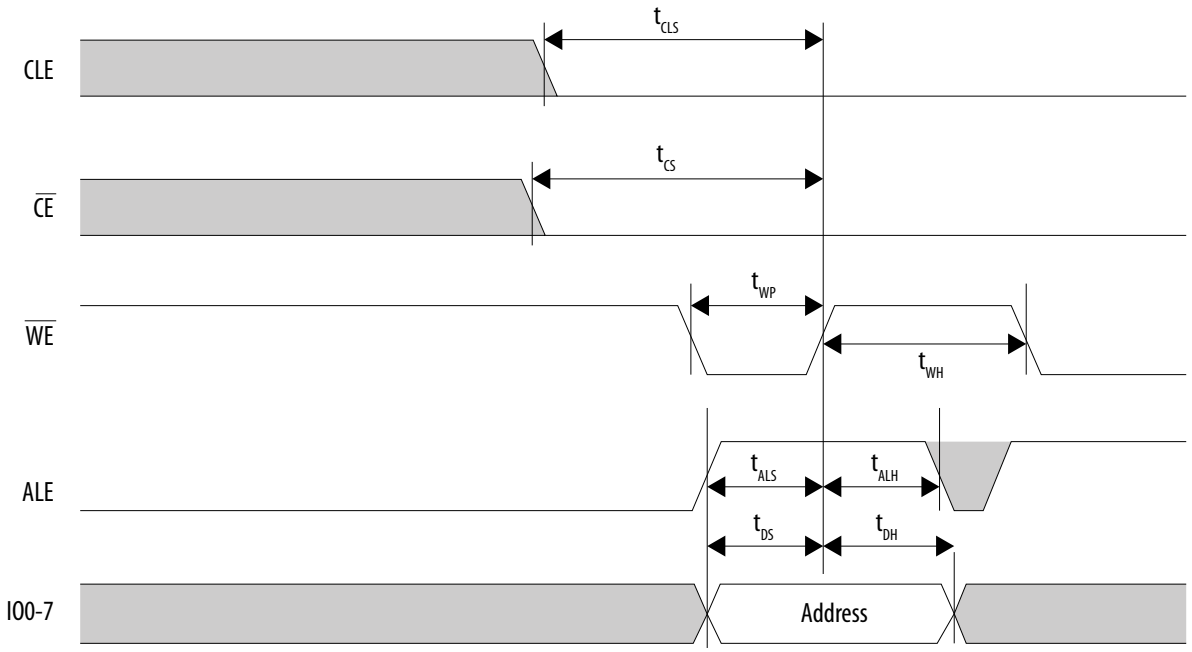


Figure 18. NAND Data Output Cycle Timing Diagram

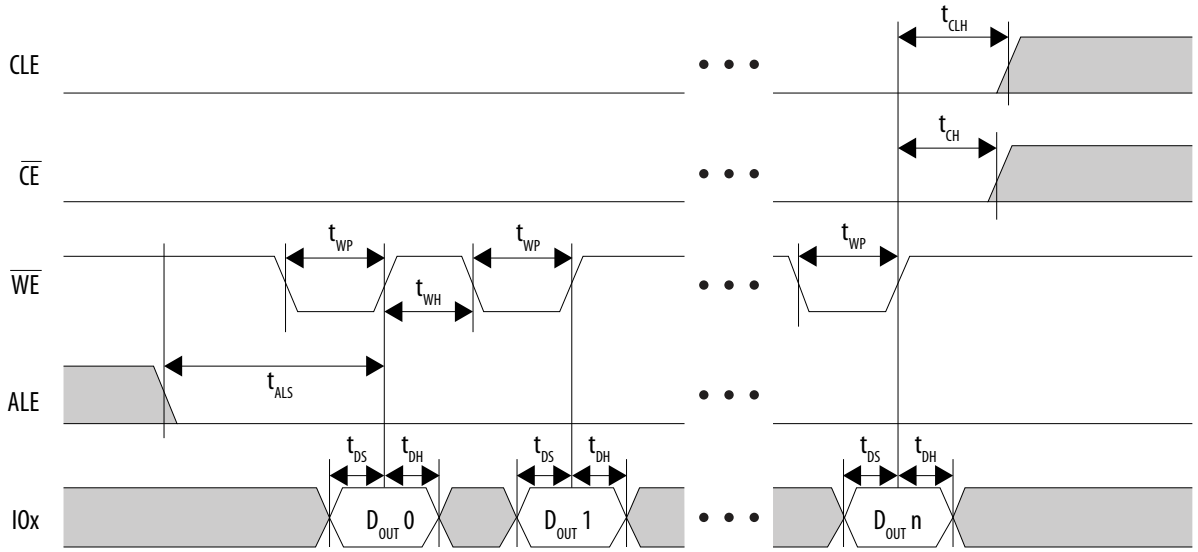


Figure 19. NAND Data Input Cycle Timing Diagram

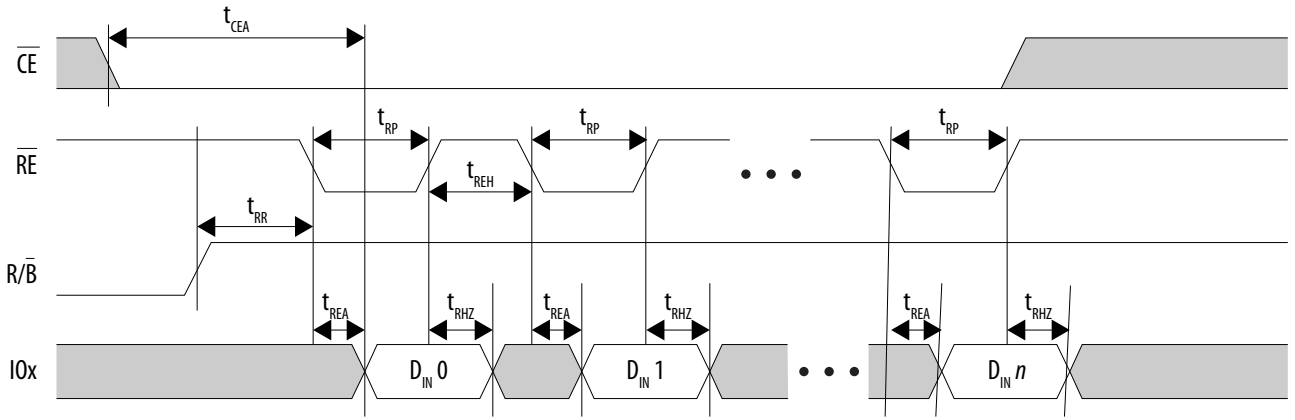


Figure 20. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

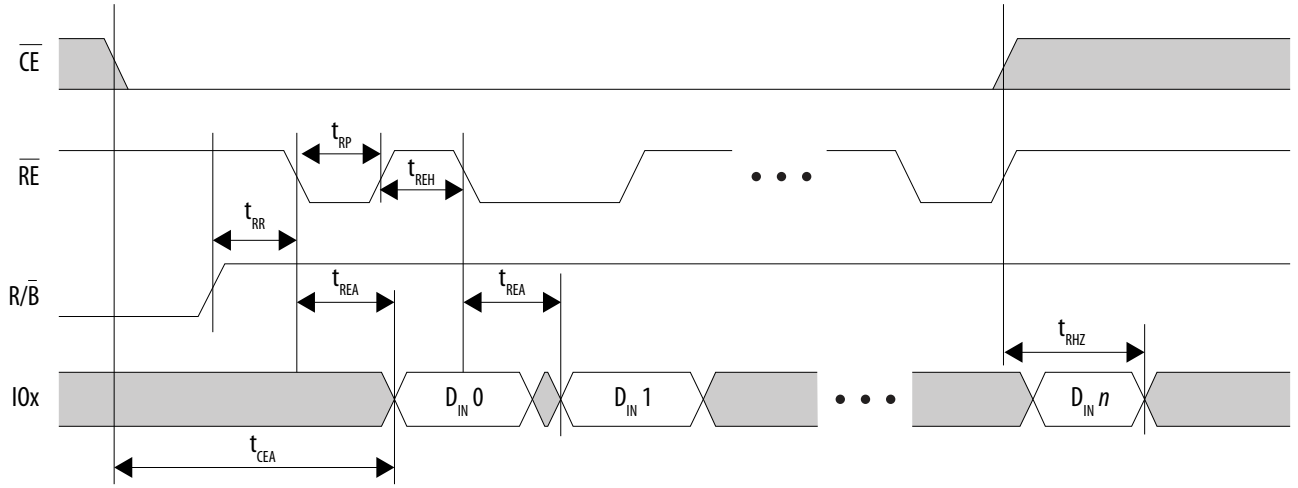


Figure 21. NAND Read Status Timing Diagram

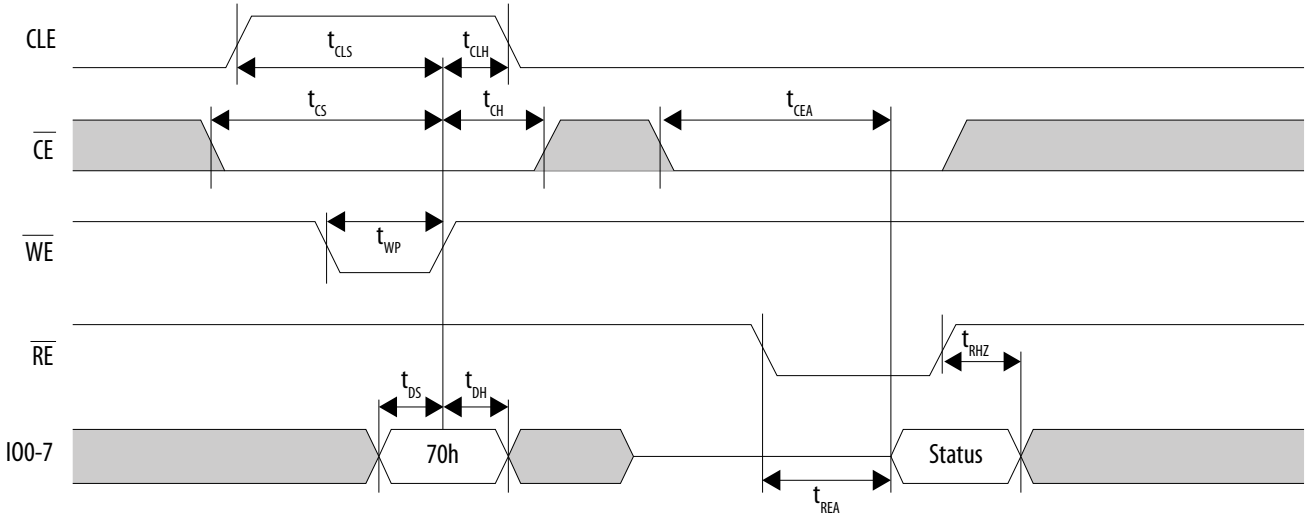
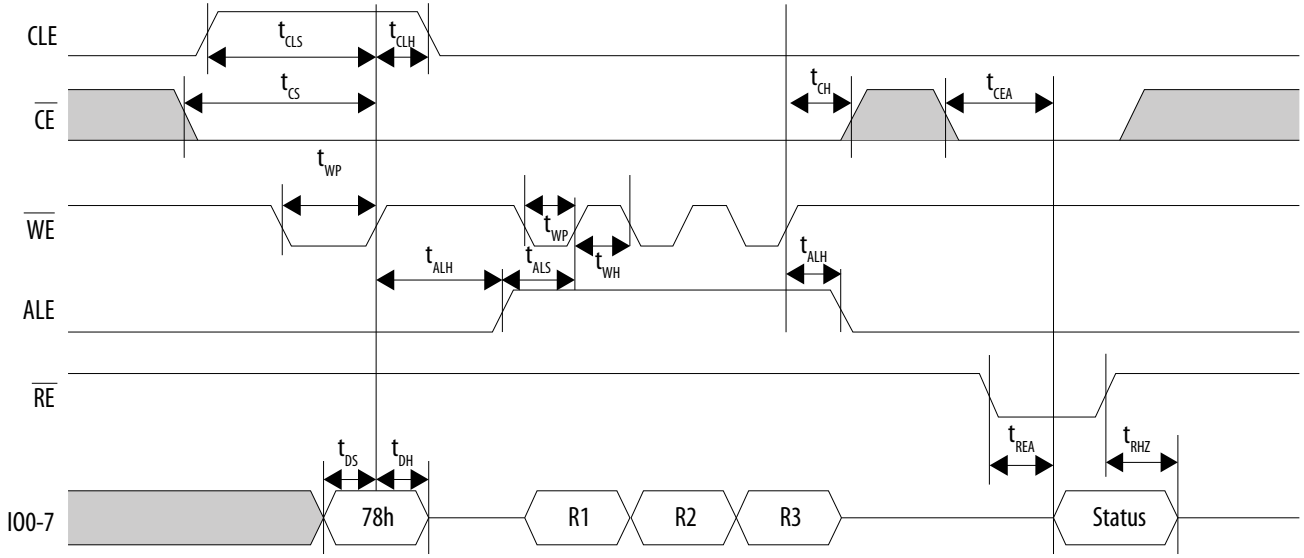


Figure 22. NAND Read Status Enhanced Timing Diagram



Related Links

NAND Flash Controller

Refer to the *NAND Flash Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual* for more information about the NAND flash controller and timing, particularly software-programmable timing.

HPS Trace Timing Characteristics - Preliminary

Table 74. Trace Timing Requirements for Intel Stratix 10 Devices

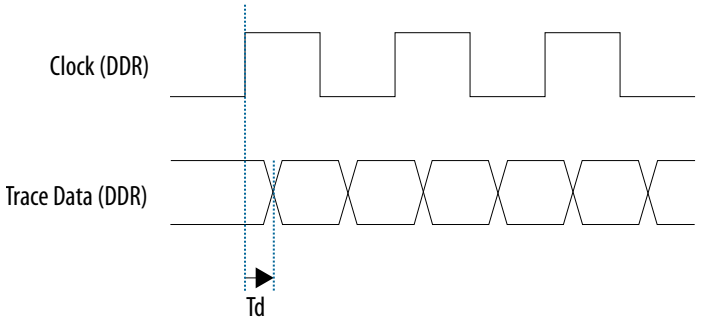
To increase the trace bandwidth, Intel recommends routing the trace interface to the FPGA in the HPS Qsys component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module datasheet for termination recommendations.

Most trace modules implement programmable clock and data skew, to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	Trace clock period	6.667	—	—	ns
T_{clk_jitter}	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
T_d	T_{clk} to D0–D15 output data delay	0	—	1.8	ns

Figure 23. Trace Timing Diagram



HPS GPIO Interface - Preliminary

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 µs (at 32 kHz). Any pulses shorter than 2 debounce clock cycles are filtered by the GPIO peripheral.

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.

Related Links

General-Purpose I/O Interface

For more information about the GPIO interface and timing, refer to the *General-Purpose I/O Interface* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual*

HPS JTAG Timing Characteristics - Preliminary

Table 75. HPS JTAG Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
t_{JCP}	TCK clock period	41.66	—	—	ns
t_{JCH}	TCK clock high time	20	—	—	ns
t_{JCL}	TCK clock low time	20	—	—	ns
t_{JPSU} (TDI)	TDI JTAG port setup time	5	—	—	ns
t_{JPSU} (TMS)	TMS JTAG port setup time	5	—	—	ns
t_{JPH}	JTAG port hold time	0	—	—	ns
t_{JPCO}	JTAG port clock to output	0	—	8	ns
t_{JPZX}	JTAG port high impedance to valid output	—	—	10	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	—	10	ns

HPS Programmable I/O Timing Characteristics - Preliminary

Table 76. Programmable I/O Delay for Intel Stratix 10 Device

Programmable Delay	Description	Min	Typ (118)	Max	Unit
0	Delay Step 1	TBD	TBD	TBD	ps
1	Delay Step 2	TBD	TBD	TBD	ps
2	Delay Step 3	TBD	TBD	TBD	ps
3	Delay Step 4	TBD	TBD	TBD	ps
4	Delay Step 5	TBD	TBD	TBD	ps
5	Delay Step 6	TBD	TBD	TBD	ps
6	Delay Step 7	TBD	TBD	TBD	ps
7	Delay Step 8	TBD	TBD	TBD	ps
8	Delay Step 9	TBD	TBD	TBD	ps
9	Delay Step 10	TBD	TBD	TBD	ps
10	Delay Step 11	TBD	TBD	TBD	ps
11	Delay Step 12	TBD	TBD	TBD	ps
12	Delay Step 13	TBD	TBD	TBD	ps
13	Delay Step 14	TBD	TBD	TBD	ps
14	Delay Step 15	TBD	TBD	TBD	ps
15	Delay Step 16	TBD	TBD	TBD	ps

You can program the number of delay steps by adjusting the I/O Delay register (`io0_delay` through `io47_delay` for I/Os 0 through 47).

(118) Each delay step is approximately 150 ps.

Configuration Specifications

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

Table 77. POR Delay Specification for Stratix 10 Devices

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16, AVST ×32, NAND, SD/MMC	12	20	ms
AS (Fast mode)	2	6.5	ms

External Configuration Clock Source Requirements

Table 78. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements—Preliminary

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency (119)	Powered by V_{CCIO_SDM}		25/100/125		MHz
Clock input jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

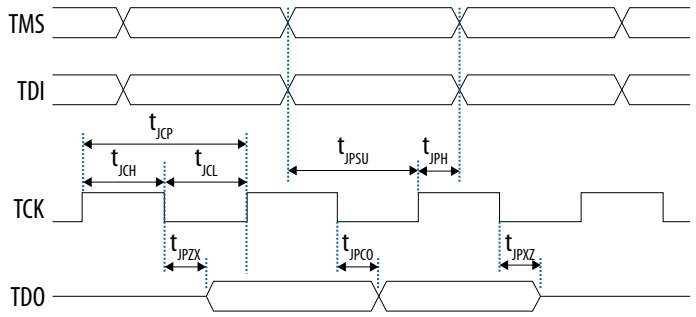
(119) The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. Other frequencies in the range are not supported.

JTAG Configuration Timing

Table 79. JTAG Timing Parameters and Values for Stratix 10 Devices—Preliminary

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCP}	TCK clock period	30, 167 (120)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	7	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Figure 24. JTAG Timing Diagram



(120) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.8 V when you perform the volatile key programming.

AS Configuration Timing

Table 80. AS Timing Parameters for Stratix 10 Devices—Preliminary

Intel recommends performing trace length matching for nCSO and AS_DATA pins to AS_CLK to minimize the skew. The maximum tolerance for skew between nCSO and AS_CLK is less than 200 ps. The tolerance for skew between AS_DATA and AS_CLK ranges between 200 ps – 400 ps.

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk}	AS_CLK clock period	7.52	—	—	ns
$T_{dutycycle}$	AS_CLK duty cycle	45	50	55	%
T_{dcsfrs}	AS_nCSO[3:0] asserted to first AS_CLK edge	4.21 (121)	—	6.05 (121)	ns
T_{dcslst}	Last AS_CLK edge to AS_nCSO[3:0] deasserted	5.18 (121)	—	7.03 (121)	ns
T_{do}	AS_DATA0 output delay	0	—	1.31	ns
T_{ext_delay} (122)	Total external propagation delay on AS signals	0	—	15	ns
T_{ext_skew}	Skew delay for AS_DATA signals	—	—	2	ns
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers	1	—	—	AS_CLK

(121) AS operating at maximum clock frequency = 133 MHz. The delay is larger when operating at AS clock frequency lower than 133 MHz.

(122) Text_delay = Tbd_clk + Tco + Tbd_data + Tadd
Tbd_clk: Propagation delay for AS_CLK between FPGA and flash device.
Tco: Output hold time of flash device.
Tbd_data: Propagation delay for AS_DATA bus between FPGA and flash device.
Tadd: Propagation delay for active/passive components on AS_DATA interfaces.

Figure 25. AS Configuration Serial Output Timing Diagram

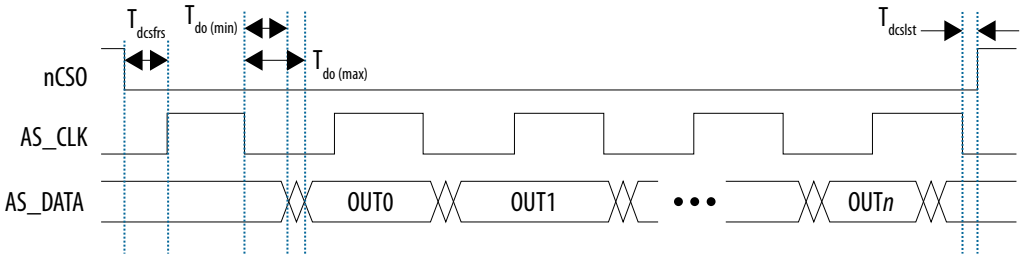
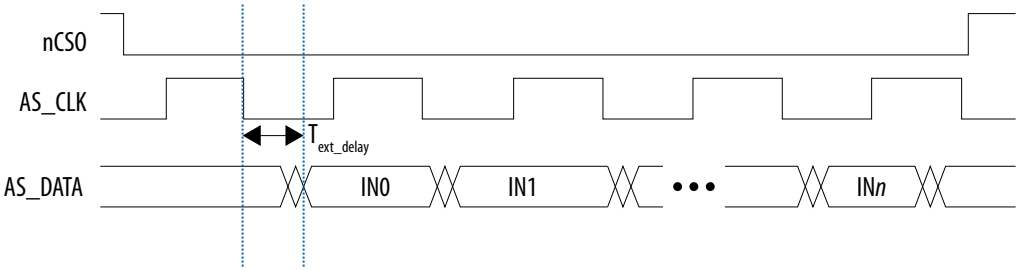


Figure 26. AS Configuration Serial Input Timing Diagram



Avalon-ST Configuration Timing

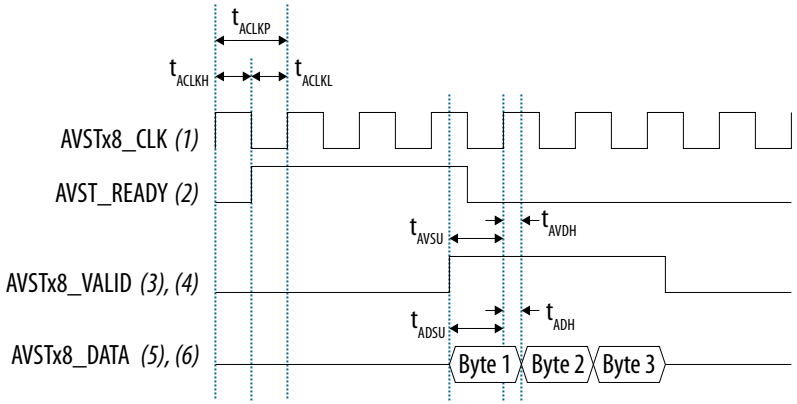
Table 81. Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Stratix 10 Devices—Preliminary

Symbol	Description	Minimum	Maximum	Unit
t_{ST0}	nSTATUS low pulse during configuration error	0.5	1.5	ms
t_{ACLKH}	AVST_CLK high time	3.6	—	ns
t_{ACLKL}	AVST_CLK low time	3.6	—	ns
t_{ACLKP}	AVST_CLK period	8	—	ns
t_{ADSU} (123)	AVST_DATA setup time before rising edge of AVST_CLK	5.5	—	ns

continued...

Symbol	Description	Minimum	Maximum	Unit
t_{ADH} (123)	AVST_DATA hold time after rising edge of AVST_CLK	0	—	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	5.5	—	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	—	ns

Figure 27. Avalon-ST Configuration Timing Diagram



Notes:

1. For Avalon-ST x16 and x32, this signal is AVST_CLK. These clocks must be running throughout the configuration (until CONF_DONE goes high).
2. AVST_READY is valid only when nSTATUS is high. AVST_READY is an asynchronous signal to AVSTx8_CLK.
3. For Avalon-ST x16 and x32, this signal is AVST_VALID.
4. The waveforms shows the interface signals with a host which uses ready latency =2. The AVSTx8_VALID signal is delayed from AVST_READY signal by 2 clock cycles.
5. For Avalon-ST x16 and x32, this signal is AVST_DATA[15:0] and AVST_DATA[31:0] respectively.
6. Host may send up to 6 more data after AVST_READY has de-asserted.

(123) Data sampled by the FPGA (sink) at the next rising clock edge.

NAND Configuration Timing

Table 82. NAND ONFI 1.0 Mode 0-5 Timing Requirements for Stratix 10 Devices—Preliminary

This table shows Mode 5 timing.

Symbol	Description	Minimum	Maximum	Unit
t_{WP}	Write enable pulse width	10	—	ns
t_{WH}	Write enable hold time	7	—	ns
t_{RP}	Read enable pulse width	10	—	ns
t_{REH}	Read enable hold time	7	—	ns
t_{CLS}	Command latch enable to write enable setup time	10	—	ns
t_{CLH}	Command latch enable to write enable hold time	5	—	ns
t_{CS}	Chip enable to write enable setup time	15	—	ns
t_{CH}	Chip enable to write enable hold time	5	—	ns
t_{ALS}	Address latch enable to write enable setup time	10	—	ns
t_{ALH}	Address latch enable to write enable hold time	5	—	ns
t_{DS}	Data to write enable setup time	7	—	ns
t_{DH}	Data to write enable hold time	5	—	ns
t_{CEA}	Chip enable to data access time	—	100	ns
t_{REA}	Read enable to data access time	—	40	ns
t_{RHZ}	Read enable to data high impedance	—	200	ns
t_{RR}	Ready to read enable low	20	—	ns
t_{WB}	Write enable high to R/B low	—	200	ns

Figure 28. NAND Command Latch Timing Diagram

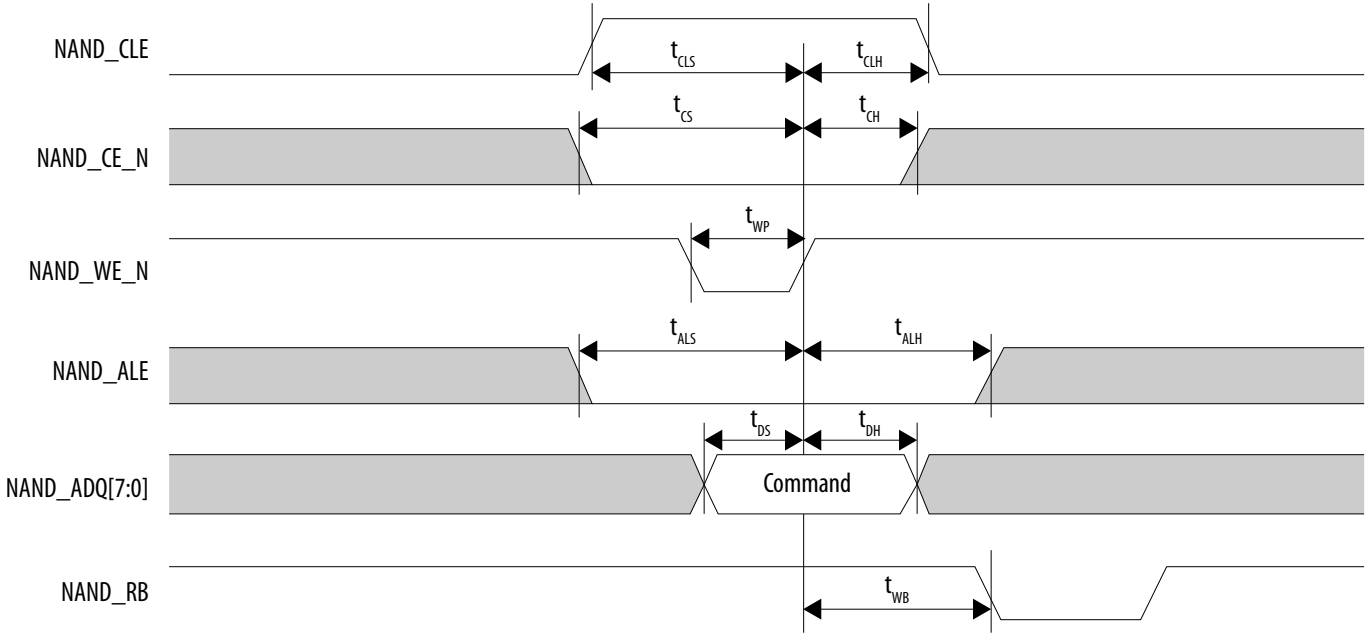


Figure 29. NAND Address Latch Timing Diagram

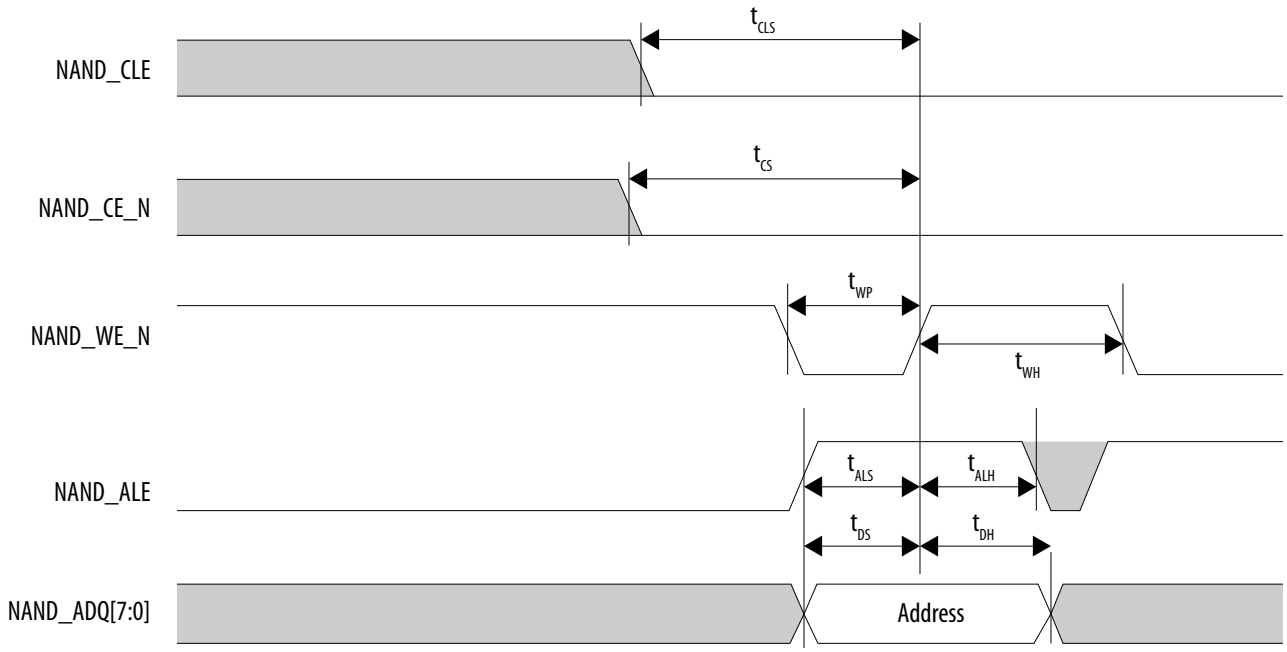


Figure 30. NAND Data Output Cycle Timing Diagram

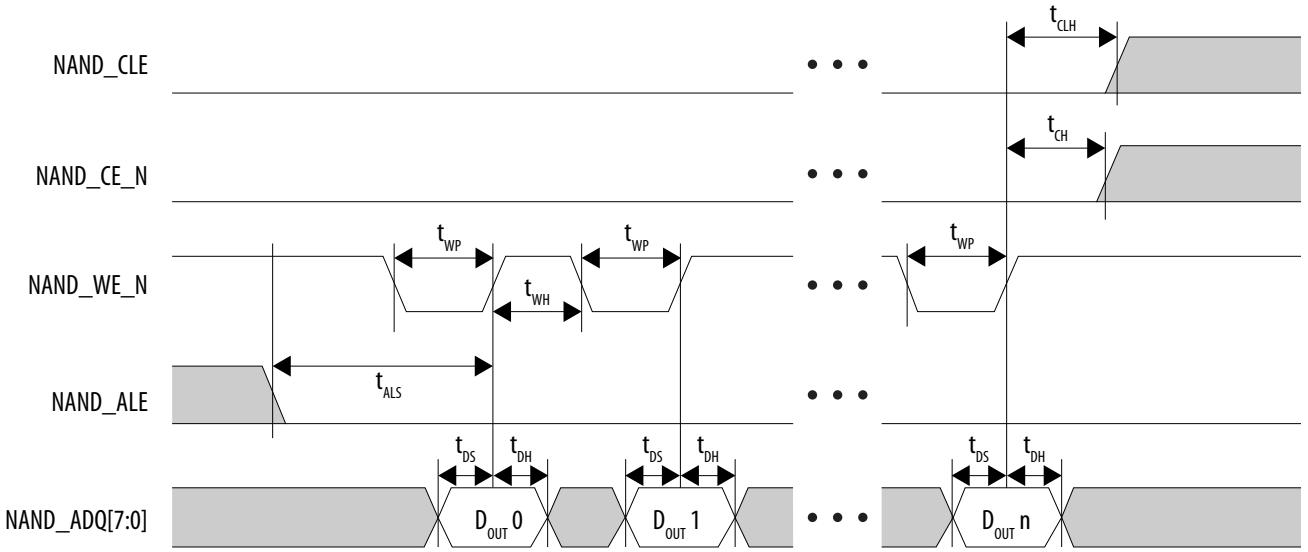


Figure 31. NAND Data Input Cycle Timing Diagram

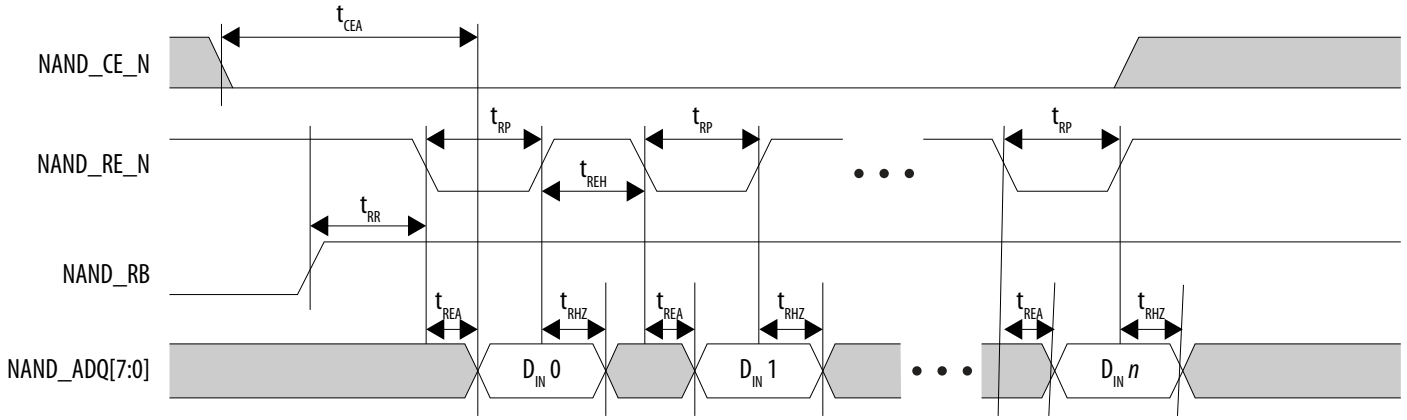


Figure 32. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

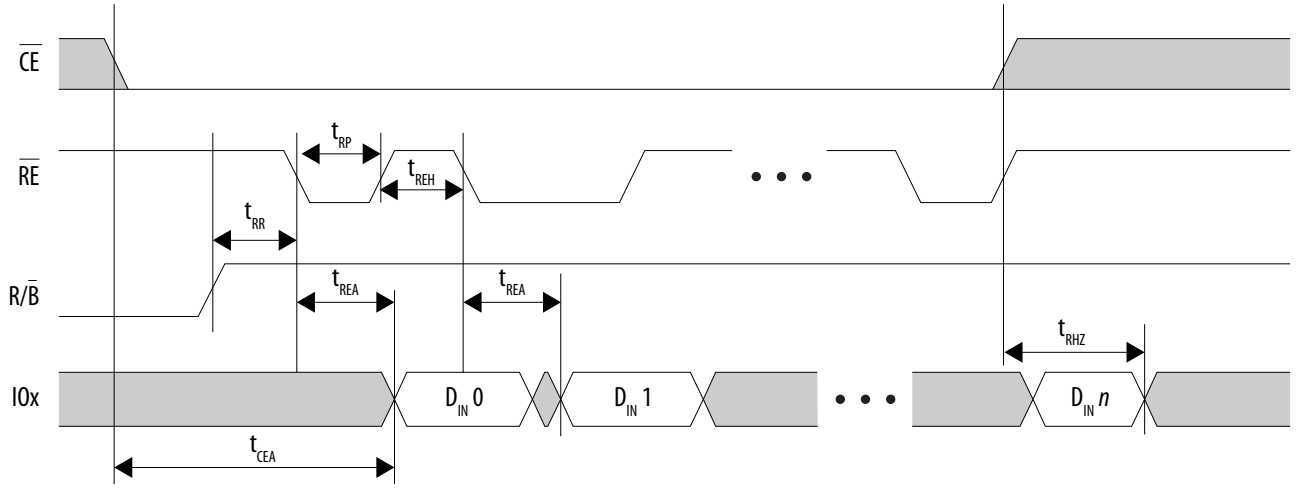


Figure 33. NAND Read Status Timing Diagram

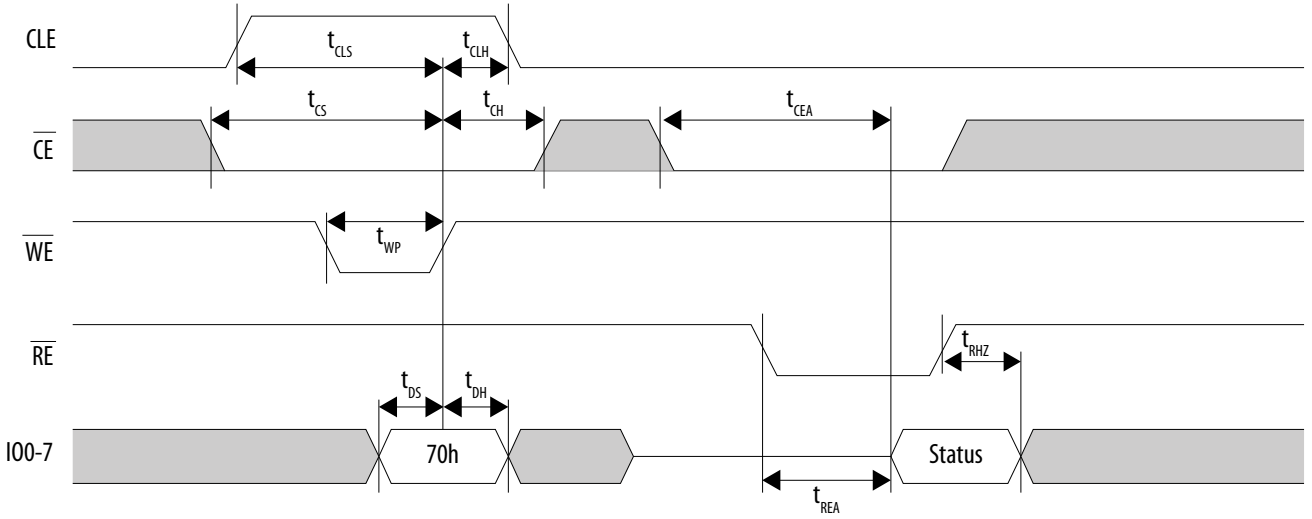
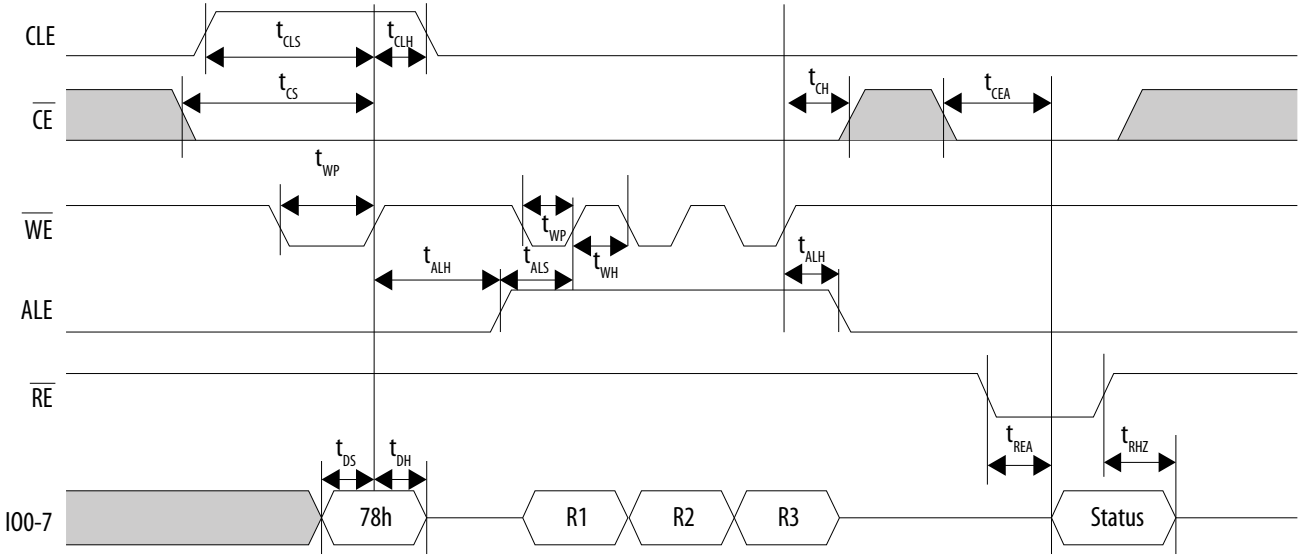


Figure 34. NAND Read Status Enhanced Timing Diagram

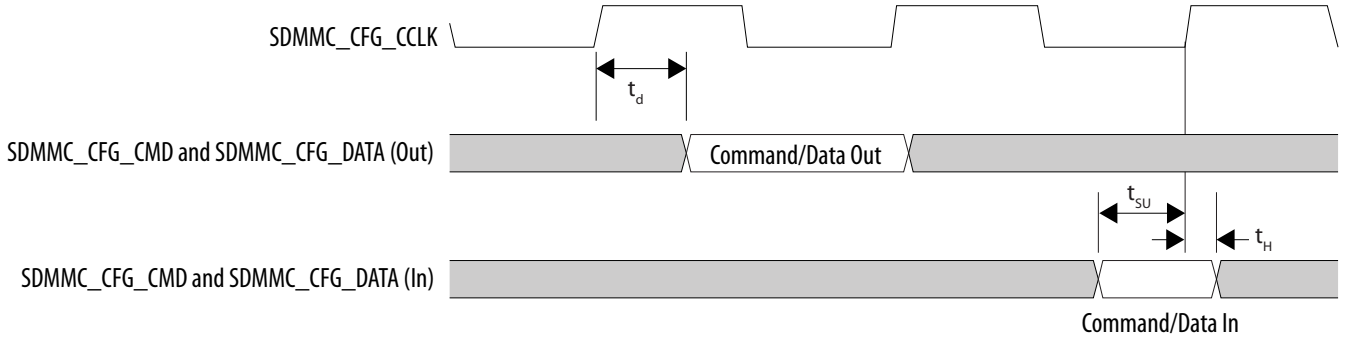


SD/MMC Configuration Timing

Table 83. SD/MMC Timing Parameters for Stratix 10 Devices—Preliminary

Symbol	Description	Minimum	Typical	Maximum	Unit
t_{SDCLKP}	SDMMC_CFG_CCLK clock period (Identification mode)	2,500	—	—	ns
	SDMMC_CFG_CCLK clock period (Standard SD mode)	40	—	—	ns
	SDMMC_CFG_CCLK clock period (High-speed SD mode)	20	—	—	ns
$t_{DUTYCYCLE}$	SDMMC_CFG_CCLK duty cycle	45	50	55	%
t_d	SDMMC_CFG_CMD/SDMMC_CFG_DATA output delay	7.3	—	10.1	ns
t_{SU}	SDMMC_CFG_CMD/SDMMC_CFG_DATA input setup	4.37	—	—	ns
t_H	SDMMC_CFG_CMD/SDMMC_CFG_DATA input hold	0	—	—	ns

Figure 35. SD/MMC Timing Diagram



Initialization

Table 84. Initialization Time for Stratix 10 Devices—Preliminary

Configuration Scheme	Maximum duration required for initialization
AS, AVST ×8, AVST ×16, AVST ×32, NAND, SD/MMC	2 ms (124)

Configuration Bit Stream Sizes

Table 85. Configuration Bit Stream Sizes for Stratix 10 Devices—Preliminary

This table shows the estimated configuration bit stream sizes of the EPCQ-L serial configuration device or external flash size before design compilation. The sizes are for compressed bit stream. The actual sizes may vary based on your design. The actual sizes may be equal or smaller than the bit stream sizes in this table.

Variant	Product Line	Compressed Configuration Bit Stream Size (Mbits)
Stratix 10 GX	GX 400, GX 650	79
	GX 850, GX 1100	133
	GX 1650, GX 2100	227

continued...

(124) This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.

Variant	Product Line	Compressed Configuration Bit Stream Size (Mbits)
	GX 2500, GX 2800	336
	GX 4500, GX 5500	448
Stratix 10 SX	SX 400, SX 650	79
	SX 850, SX 1100	133
	SX 1650, SX 2100	227
	SX 2500, SX 2800	336
	SX 4500, SX 5500	448

Minimum Configuration Time Estimation

Hyper Initialization is an option that can be enabled or disabled through the setting in the Intel Quartus Prime software to initialize or reset the HyperFlex registers to a known state at device configuration.

Maximum configuration time does not exceed 2× of the minimum configuration time.

Table 86. Minimum Configuration Time Estimation for Stratix 10 Devices (JTAG and Avalon-ST)—Preliminary

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]							
		JTAG		AVST ×8		AVST ×16		AVST ×32	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Stratix 10 GX	GX 400, GX 650	3000/3100	3000/3100	137/167	91/111	77/108	51/72	60/92	40/61
	GX 850, GX 1100	5300/5600	5300/5600	228/284	152/189	123/179	82/119	95/150	63/100
	GX 1650, GX 2100	9000/9500	9000/9500	377/426	251/284	197/248	131/165	107/158	71/105

continued...

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]							
		JTAG		AVST ×8		AVST ×16		AVST ×32	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
	GX 2500, GX 2800	13300/14000	13300/14000	551/620	367/413	284/354	189/236	150/221	100/147
	GX 4500, GX 5500	17600/18700	17600/18700	723/831	482/554	371/480	247/320	194/303	129/202
Stratix 10 SX	SX 400, SX 650	3000/3100	3000/3100	137/167	91/111	77/108	51/72	60/92	40/61
	SX 850, SX 1100	5300/5600	5300/5600	228/284	152/189	123/179	82/119	95/150	63/100
	SX 1650, SX 2100	9000/9500	9000/9500	377/426	251/284	197/248	131/165	107/158	71/105
	SX 2500, SX 2800	13300/14000	13300/14000	551/620	367/413	284/354	189/236	150/221	100/147
	SX 4500, SX 5500	17600/18700	17600/18700	723/831	482/554	371/480	247/320	194/303	129/202

Table 87. Minimum Configuration Time Estimation for Stratix 10 Devices (AS, NAND, and SD/MMC)—Preliminary

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]					
		AS ×4		NAND		SD/MMC	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Stratix 10 GX	GX 400, GX 650	284/315	189/210	366/396	244/264	366/396	244/264
	GX 850, GX 1100	450/506	300/337	597/653	398/435	597/653	398/435
	GX 1650, GX 2100	716/767	477/511	966/1017	644/678	966/1017	644/678

continued...

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]					
		AS ×4		NAND		SD/MMC	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
	GX 2500, GX 2800	1029/1100	686/733	1403/1472	935/981	1403/1472	935/981
	GX 4500, GX 5500	1338/1449	892/966	1800/1950	1200/1300	1800/1950	1200/1300
Stratix 10 SX	SX 400, SX 650	284/315	189/210	366/396	244/264	366/396	244/264
	SX 850, SX 1100	450/506	300/337	597/653	398/435	597/653	398/435
	SX 1650, SX 2100	716/767	477/511	966/1017	644/678	966/1017	644/678
	SX 2500, SX 2800	1029/1100	686/733	1403/1472	935/981	1403/1472	935/981
	SX 4500, SX 5500	1338/1449	892/966	1800/1950	1200/1300	1800/1950	1200/1300

I/O Timing

The Intel Quartus Prime Timing Analyzer provides accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

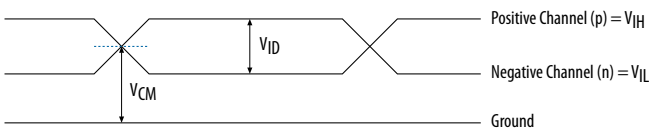
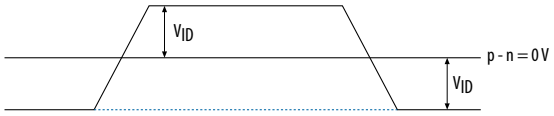
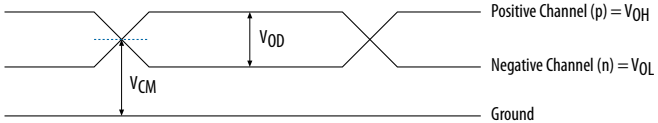
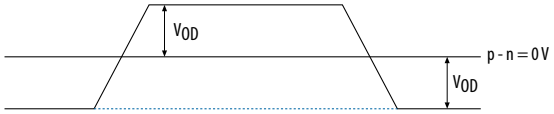
The I/O Timing specifications will be available in a future release of the *Stratix 10 Device Datasheet*.

Glossary

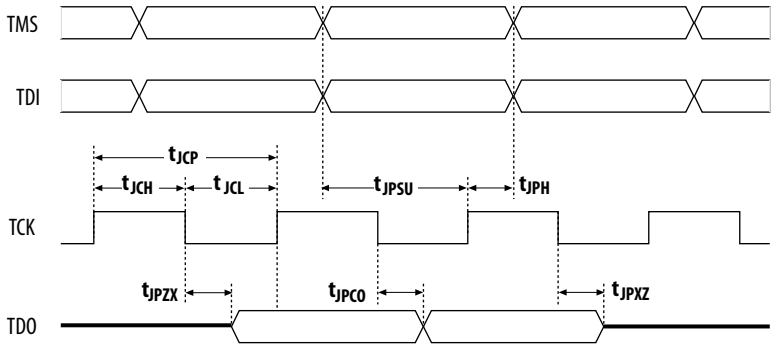
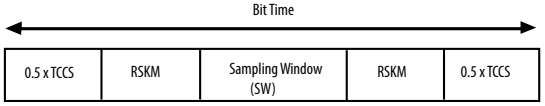
Table 88. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms

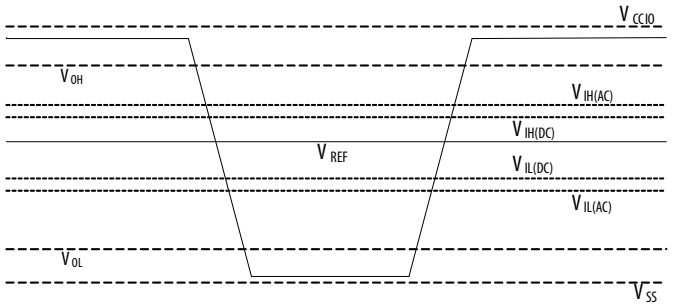
continued...

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the Stratix 10 device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

continued...

Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL.
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t_{RISE}	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.

continued...

Term	Definition
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage.
$V_{IL(DC)}$	Low-level DC input voltage.
V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage.
V_{IX}	Input differential cross point voltage.
V_{OX}	Output differential cross point voltage.
$V_{X(AC)}$	V_{IX} Input differential cross point voltage.
W	High-speed I/O block—Clock Boost Factor.

Document Revision History

Date	Version	Changes
August 2017	2017.08.04	• Clarified DLL operating frequency range in "DLL Range Specifications" • Clarified reference clock specifications in "HPS SPI Timing Characteristics"
May 2017	2017.05.08	• Updated description for V_{CCERAM} in Absolute Maximum Ratings for Stratix 10 Devices table. • Added Maximum Allowed Overshoot During Transitions for Stratix 10 Devices table. • Updated Recommended Operating Conditions for Stratix 10 Devices table. — Updated V_{CC}, V_{CCIO}, and V_{CCBAT} specifications. — Updated symbol from $V_{CCPFUSE\_SDM}$ to $V_{CCFUSEWR\_SDM}$. — Updated description for V_{CCERAM} and V_{CCIO_UIB} . — Added V_{CCM} specifications. — Added footnotes to t_{RAMP} and V suffix speed grades. • Removed table: Temperature Compensation for SmartVID for Stratix 10 Devices.

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Date	Version	Changes
		• Updated the note in the "Transceiver Power Supply Operating Conditions" section. • Updated HPS Power Supply Operating Conditions for Stratix 10 Devices table. — Updated V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ specifications. — Added footnote for SmartVID. • Updated footnote to I_{OL} and I_{OH} in Single-Ended I/O Standards Specifications for Stratix 10 Devices table. • Updated Differential I/O Standards Specifications for Stratix 10 Devices table. — Changed D_{MAX} to data rate. — Added a note to V_{OD}. • Updated t_{OUTPJ_DC} and t_{OUTCCJ_DC} specifications in I/O PLL Specifications for Stratix 10 Devices. • Changed the units of measure for the minimum frequency in the "L-Tile CMU PLL Performance" table. • Changed the units of measure for the minimum frequency in the "H-Tile CMU PLL Performance" table. • Updated t_{INCCJ} specification for F_{REF} < 100 MHz in the following tables: — Fractional PLL Specifications for Stratix 10 Devices — I/O PLL Specifications for Stratix 10 Devices • Added footnote to the following modes in DSP Block Performance Specifications for Stratix 10 Devices table: — Fixed-point 27 × 27 multiplication mode — Fixed-point 18 × 18 multiplier adder mode — Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode • Updated soft CDR mode specifications in High-Speed I/O Specifications for Stratix 10 Devices table. • Added POR specifications. • Updated T_{do} maximum specification in AS Timing Parameters for Stratix 10 Devices table. • Updated notes in Avalon-ST Configuration Timing Diagram. • Added description in NAND ONFI 1.0 Mode 0-5 Timing Requirements for Stratix 10 Devices table. • Updated t_{SU}, t_H, and t_d specifications in SD/MMC Timing Parameters for Stratix 10 Devices table. • Updated table title from "Initialization Clock Source Option and the Maximum Frequency for Stratix 10 Devices" to "Initialization Time for Stratix 10 Devices". • Updated description in Configuration Bit Stream Sizes for Stratix 10 Devices to mention that the actual sizes may be equal or smaller than the bit stream sizes in this table. • Updated description in Minimum Configuration Time Estimation section. • Removed AS ×1 specifications in Minimum Configuration Time Estimation for Stratix 10 Devices (AS, NAND, and SD/MMC) table. • Added Glossary. • Removed PowerPlay text from tool name.
February 2017	2017.02.17	Made the following changes:

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Date	Version	Changes
		• Added the "Transceiver Power Supply Operating Conditions for Stratix 10 GX/SX E-Tile Devices" table. • Added the "E-Tile Transceiver Performance Specifications" section. • Added the "Transceiver Performance forStratix 10 E-Tile Devices" section. • Added the "Transceiver Reference Clock Specifications" section. • Added the "Transmitter Specifications for Stratix 10 E-Tile Devices" section. • Added the "Receiver Specifications for Stratix 10 E-Tile Devices" section. • Updated the "AS Timing Parameters for Stratix 10 Devices" table. — Updated T_{dcsfrs} and T_{dcslst}. — Added T_{ext_delay} and T_{ext_skew}. — Removed T_{su} and T_{h}. • Updated AS Configuration Serial Input Timing Diagram.
December 2016	2016.12.09	Made the following changes: • Changed the max t_{LTR} value and unit of measure in the "L-Tile Receiver Specifications" table. • Made the following changes to the "Transceiver Clocks Specifications for Stratix 10 GX/SX L-Tile Devices" table: — Changed the value of the `reconfig_clk` signal — Added a new footnote to the GX channel — Changed the minimum values for the GXT channel • Changed the max t_{LTR} value and unit of measure in the "H-Tile Receiver Specifications" table. • Removed the QPI footnote from the "H-Tile Transmitter Specifications" table. • Changed the value of the `reconfig_clk` signal in the "Transceiver Clocks Specifications for Stratix 10 GX/SX H-Tile Devices" table. • Changed the minimum value of f_{INPFD} in the "Fractional PLL Specifications for Stratix 10 Devices" table.
October 2016	2016.10.31	Initial release.