

Xiang Pan
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Education

- **The Ohio State University** Columbus, OH
Ph.D. in Computer Science [Major GPA: 3.83/4.00] 09/2010 - 05/2017
 - Dissertation: “*Designing Future Low-Power and Secure Processors with Non-Volatile Memory*”
 - Committee: Radu Teodorescu (**Advisor**), Feng Qin, Christopher Stewart, Yinqian Zhang
- **Beijing University of Posts and Telecommunications** Beijing, China
B.E. in Computer Science [Major GPA: 88/100 (Top 5%)] 09/2006 - 07/2010

Industry Experience

- **Uber Technologies, Inc.** San Francisco, CA
Software Engineer 06/2018 - Present
 - Work on backend rider pricing serving and optimization. [**Skills:** Python, PyCharm, Git]
- **Qualcomm Technologies, Inc.** Austin, TX
Senior Engineer 04/2017 - 06/2018
 - Develop software simulator to model architectural features and performance of future Qualcomm Hexagon DSP Processor. [**Skills:** C++, C, Shell, GDB, Git, System Modeling/Analysis]
- **Samsung Austin R&D Center** Austin, TX
Software Engineering Intern 05/2015 - 08/2015
 - Build CPU power measurement software framework and conduct leakage power characterization and validation on Samsung Mongoose (Galaxy-S7) CPU. The developed framework has been used for future power measurements in Samsung. [**Skills:** C++, Assembly, Git, System Hacking/Debugging]
- **Hewlett-Packard Laboratories** Palo Alto, CA
Research Intern 05/2014 - 08/2014
 - Exploit architecture/OS support to design temperature variation aware Memristor memory scheduling policies to improve performance and energy efficiency. Proposed solution achieved 10% performance improvement and 27% energy reduction. [**Skills:** C++, QEMU, gem5, System Modeling/Analysis]
- **Hewlett-Packard Enterprise** Boise, ID
Software Engineering Intern 05/2013 - 08/2013
 - Build performance profiling software infrastructure for HP-3PAR storage disk array. The developed infrastructure has been used for identifying future embedded software performance bottlenecks in HP. [**Skills:** C++, Python, Shell, Performance Profiling]
- **Tsinghua University Microprocessor and SoC Technology R&D Center** Beijing, China
Research Intern 06/2009 - 06/2010
 - Optimize MESI protocol to be aware of data usage in all cache hierarchies to help improve cacheline replacement policy in the shared last level cache. Proposed solution achieved 14% performance improvement. [**Skills:** C++, Simics, CACTI, System Modeling/Analysis]
 - Develop ELF and PE loaders for a software-based CPU simulator. [**Skills:** C++]

Research Experience

- **Computer Architecture Research Lab @ Ohio State** Columbus, OH
Graduate Research Associate 09/2011 - 04/2017
 - *When Non-Volatile Caches Meet Cold Boot Attacks (04/2016 - 02/2017)*: Conduct proof-of-concept cold boot attacks on systems with non-volatile caches running AES disk encryption algorithms and design corresponding countermeasures. Proposed attacks have been successfully performed on real systems and the developed countermeasure solutions are 100% effective in defending those attacks with small performance overhead. [**Skills:** C++, C, gem5, AES, dm-crypt, Kernel Programming]

- *Using STT-RAM to Enable Energy-Efficient Near-Threshold Chip Multiprocessors (06/2013 - 09/2014)*: Implement a new NT-CMP architecture that uses STT-RAM to build all on-chip caches to save power; exploit greedy algorithm on the proposed architecture for better hardware resource management to further improve energy efficiency. Proposed design achieved 11% performance improvement and 32% energy reduction. [**Skills:** C++, Shell, Assembly, GDB, SESC, CACTI, McPAT, System Modeling/Analysis]
- *Linux Kernel Development (01/2013 - 04/2013)*: Several small projects include adding system calls, creating/reading/writing proc file system entries, modifying/adding thread schedulers, and checkpointing process memory data. [**Skills:** C, C++, Kernel Programming]
- *Using Non-Volatile Memory to Enable Fast Sleep/Wakeup of Idle Cores (03/2012 - 03/2013)*: Implement a low-power microprocessor framework that leverages STT-RAM to build a fast and low overhead checkpointing mechanism which enables fast shutdown and wake-up of cores without loss of their execution states to save power in various core idle scenarios. Proposed design achieved 34% energy reduction with less than 3% performance/area overhead. [**Skills:** C++, Shell, Assembly, GDB, SESC, CACTI, McPAT, System Modeling/Analysis]
- *Updating Power Models in SuperEScalar Simulator (01/2012 - 02/2012)*: Separate read/write energy from general access energy; use state-of-art power simulation tools to model dynamic power; add leakage and pipeline register power models. [**Skills:** C++, Python, SESC, CACTI, McPAT]
- *Characterizing and Eliminating Synchronization Induced Voltage Emergencies in Many-Core Processors (09/2011 - 11/2011)*: Develop a kernel module based software tool using Intel's Running Average Power Limit (RAPL) interface to obtain CPU power trace when running barrier synchronized multithreaded benchmarks on Intel Sandy Bridge i7 processor. [**Skills:** C++, C, Kernel Module Programming, Multithreading, Workload Analysis]
- *Reactive Core Acceleration for Power-Constrained Chip Multiprocessors (11/2010 - 08/2011)*: Compile PARSEC benchmarks for SESC simulator by rewriting benchmark pthread code using Linux Threads Library; design core acceleration algorithms to accelerate program execution and mitigate effects of process variation and application imbalance. Proposed design achieved 19% performance improvement and 23% energy-delay reduction. [**Skills:** C++, Compiler, Multithreading, SESC]

Selected Publications

- X. Pan**, A. Bacha, S. Rudolph, L. Zhou, Y. Zhang, R. Teodorescu “*NVCool: When Non-Volatile Caches Meet Cold Boot Attacks*”, ICCD-2018
- X. Pan**, A. Bacha, R. Teodorescu “*Respin: Rethinking Near-Threshold Multiprocessor Design with Non-Volatile Memory*”, IPDPS-2017
- X. Pan** and R. Teodorescu “*NVSleep: Using Non-Volatile Memory to Enable Fast Sleep/Wakeup of Idle Cores*”, ICCD-2014
- X. Pan** and R. Teodorescu “*Using STT-RAM to Enable Energy-Efficient Near-Threshold Chip Multiprocessors*”, PACT-2014 (Short Paper)
- T. Miller, R. Thomas, **X. Pan**, R. Teodorescu “*VRSync: Characterizing and Eliminating Synchronization Induced Voltage Emergencies in Many-Core Processors*”, ISCA-2012
- T. Miller, **X. Pan**, R. Thomas, N. Sedaghati, R. Teodorescu “*Booster: Reactive Core Acceleration for Mitigating the Effects of Process Variation and Application Imbalance in Low-Voltage Chips*”, HPCA-2012

Skills

Languages: C++, C, Python, Shell, Assembly, Parallel (Pthread, OpenMP, CUDA, MPI)

Systems: Linux (Kernel Programming), Android, Mac OS X, Windows, MapReduce, Hadoop

Tools: Architectural Simulators (SESC, gem5, Simics, CACTI, McPAT), GNU Development and Debug Tools, Performance Profiling Tools (Perf, OProfile, Ftrace), PyCharm, QEMU, LXC, Docker, Git, SVN, L^AT_EX