



HACETTEPE UNIVERSITY

**DEPARTMENT OF
ELECTRICAL AND ELECTRONICS
ENGINEERING**

**ELE313 ELECTRONICS II
LABORATORY DESIGN PROJECT**

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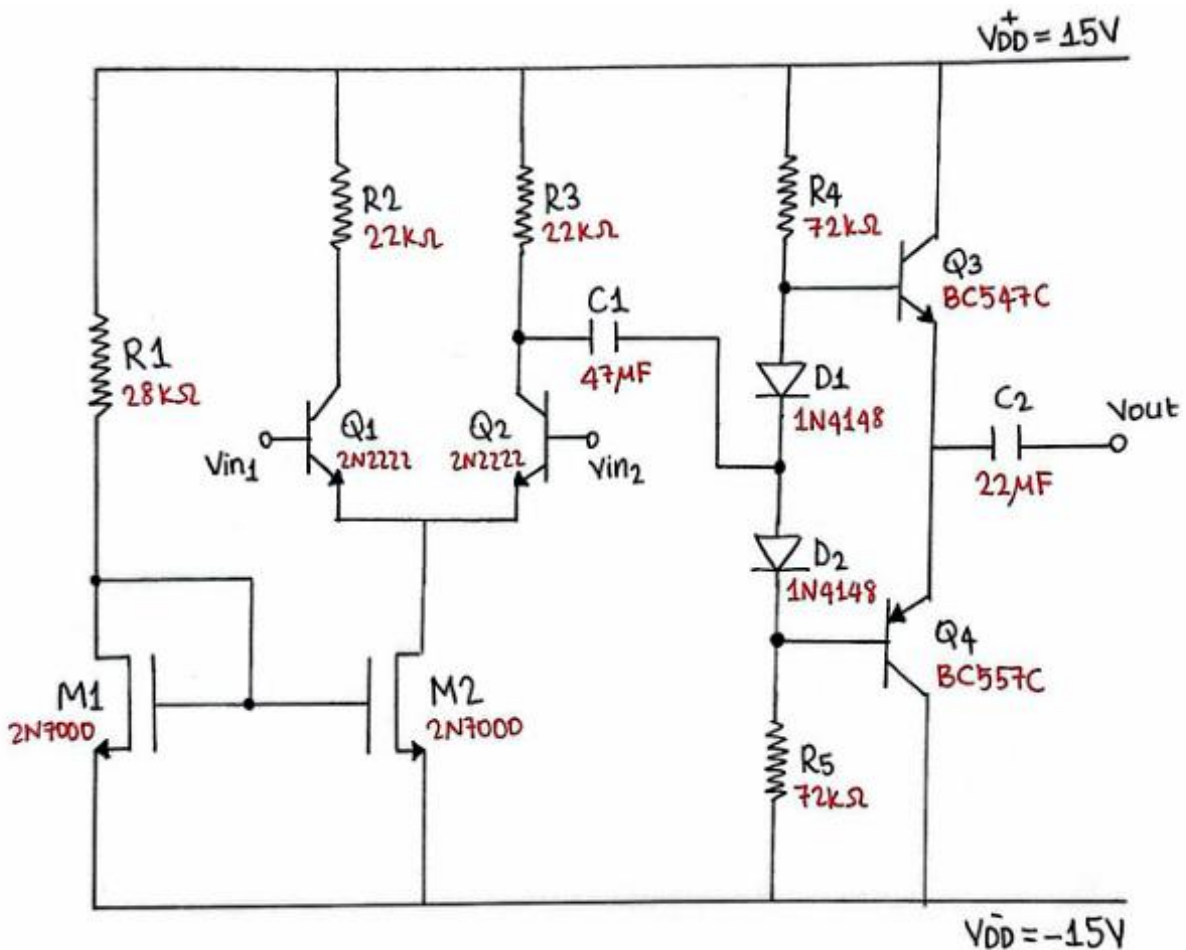
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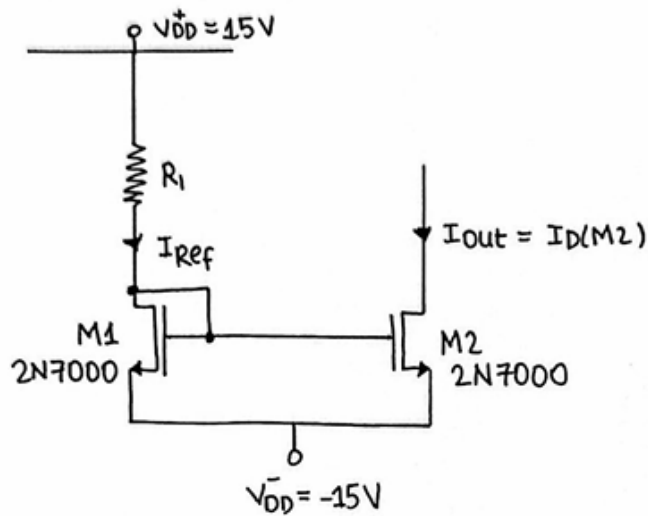
1) THEORATICAL CALCULATIONS

In this section, the theoretical analysis and design of the differential amplifier with an output stage are presented. The circuit diagram, which forms the basis of the design, is shown below, and the calculations for key parameters such as voltage gain, bandwidth, and offset voltage are discussed in detail.

The theoretical calculations for the differential amplifier with an output stage were conducted in three primary steps: the current mirror, the differential amplifier, and the output stage. For the current mirror, NMOS transistors (2N7000) were used to achieve a stable reference current of 1 mA, with the resistor value R1. In the differential amplifier stage, BJTs (2N2222) were chosen. Finally, in the output stage, the design utilized BC547C and BC557C transistors to handle a high load current, with adjustments to R4 and R5 improving gain and maintaining circuit functionality. The overall design adhered to theoretical expectations while accounting for practical considerations such as component availability and circuit performance.



(I) CURRENT MIRROR



Let $I_{ref} = I_{out} = 1\text{mA}$. The current values become equal because I choose M1 and M2 transistors as the same.

$V_{TH} = 1.6\text{V}$ is from the datasheet of 2N7000 NMOS.

$$I_{ref} = \frac{V_{DD}^+ - V_D(M1)}{R_1}$$

where $V_G > V_{TH}$ condition must satisfy.

$$V_G - V_S > V_{TH} \quad \text{where } V_S = -15\text{V}$$

$$V_G > 1.6\text{V} - 15\text{V}$$

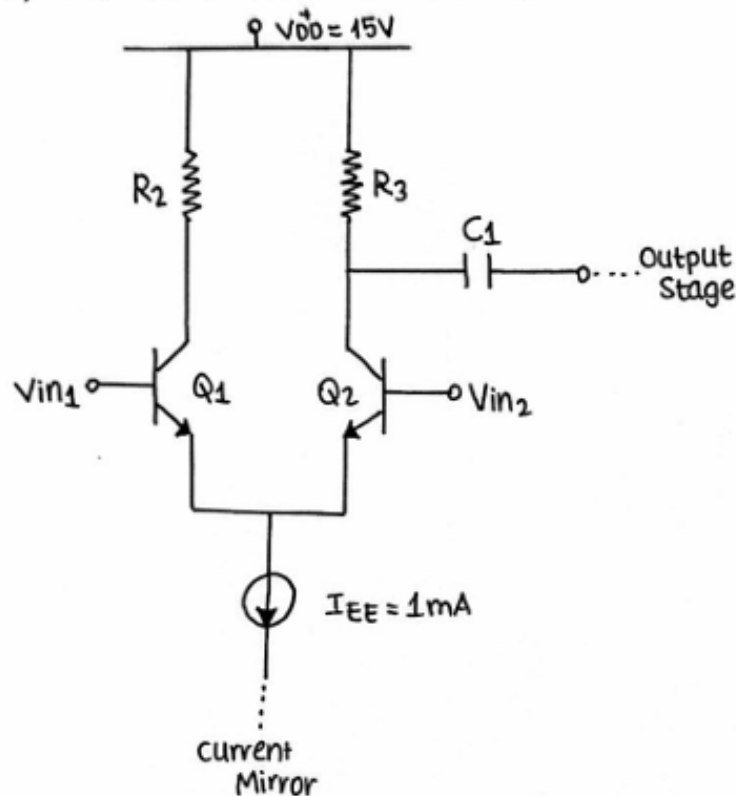
$$V_G > -13.4\text{V}$$

I choose $V_G(M1)$ as -13V .

$V_G(M1) = V_D(M1) = -13\text{V}$. From here,

$$R_1 = 28\text{k}\Omega$$

(II) DIFFERENTIAL AMPLIFIER



Q_1 and Q_2 transistors' models are chosen as 2N2222, and their β values are equal to 65.

$$I_C(Q_1) = I_C(Q_2) = \frac{I_{EE}}{2} = 0.5 \text{ mA}$$

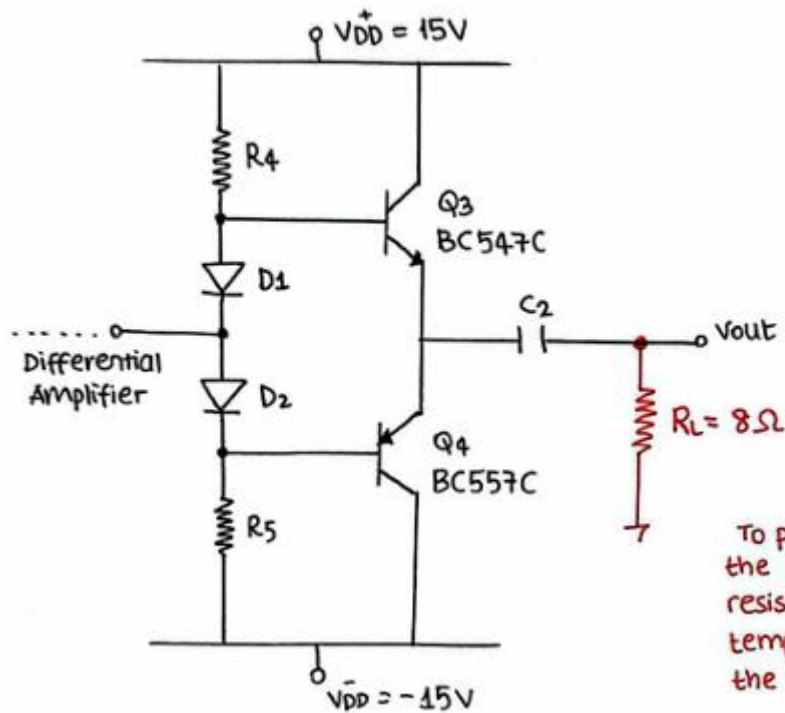
$$g_m = \frac{I_C}{V_T} = \frac{0.5 \text{ mA}}{26 \text{ mV}} = \frac{1}{52} \text{ S}$$

Let $|A_v| = g_m R_C = 400$. From here $R_C = R_2 = R_3 = 20.8 \text{ k}\Omega$.

In my design, I used $22 \text{ k}\Omega$ resistors instead of $20.8 \text{ k}\Omega$. The reason is that this resistor value is more readily available in the markets.

C_1 value is chosen as $22 \mu\text{F}$.

(III) OUTPUT STAGE



To perform the analysis of the output stage, a load resistor R_L (with 8Ω) was temporarily connected to the circuit.

Let $I_L = 30\text{ mA}$ for my design.

$$V_{out} = R_L \cdot I_L = (8\Omega)(30\text{ mA}) = 0.24\text{ V}.$$

$$V(R_4) + V(R_5) = V_{DD} - V_{out} = 14.76\text{ V} \quad \text{and} \quad V(R_4) = V(R_5) = 7.38\text{ V}.$$

$$I_C(Q_3) = I_C(Q_4) = \frac{I_L}{2} = 15\text{ mA}.$$

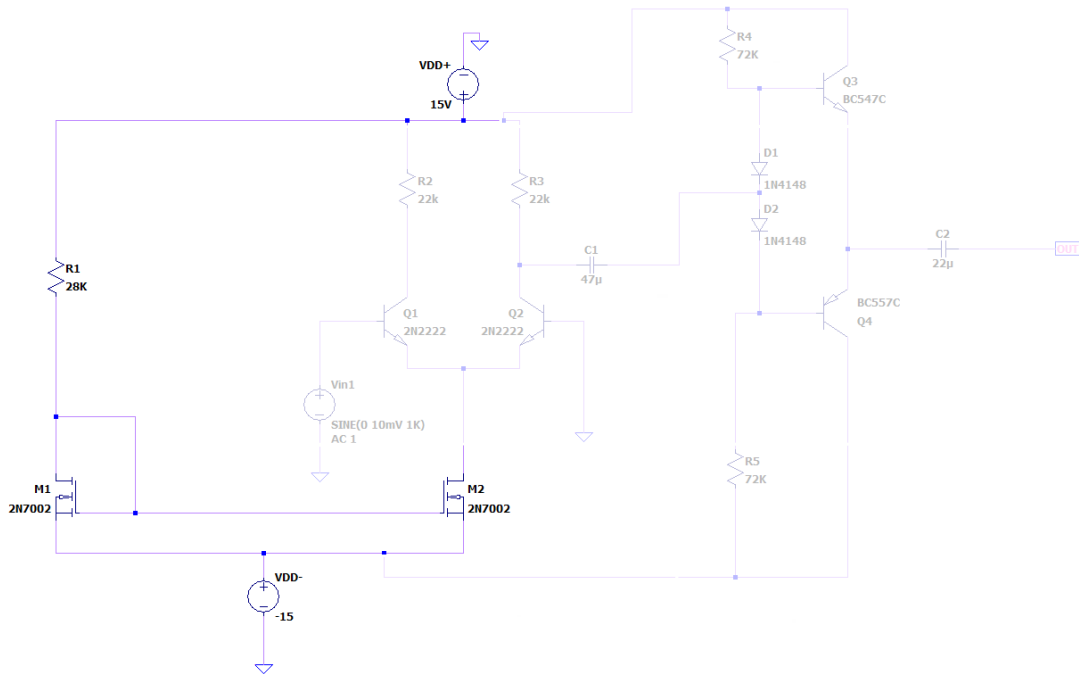
$$I_B = \frac{I_C}{\beta} \quad \text{where} \quad \beta_3 = \beta_4 = 200. \quad \text{From here, } I_B = \frac{15\text{ mA}}{200} = 0.075\text{ mA}$$

$$I_B(Q_3) \cdot R_4 = V(R_4) \rightarrow R_4 = 98.4\text{ k}\Omega = R_5$$

In my design, I used $75\text{ k}\Omega$ resistors for R_4 and R_5 , decreasing their theoretically calculated values does not effect the output stage in LTSpice, also the overall gain increased.

2) LTSPICE SIMULATIONS

I. CURRENT MIRROR ANALYSIS

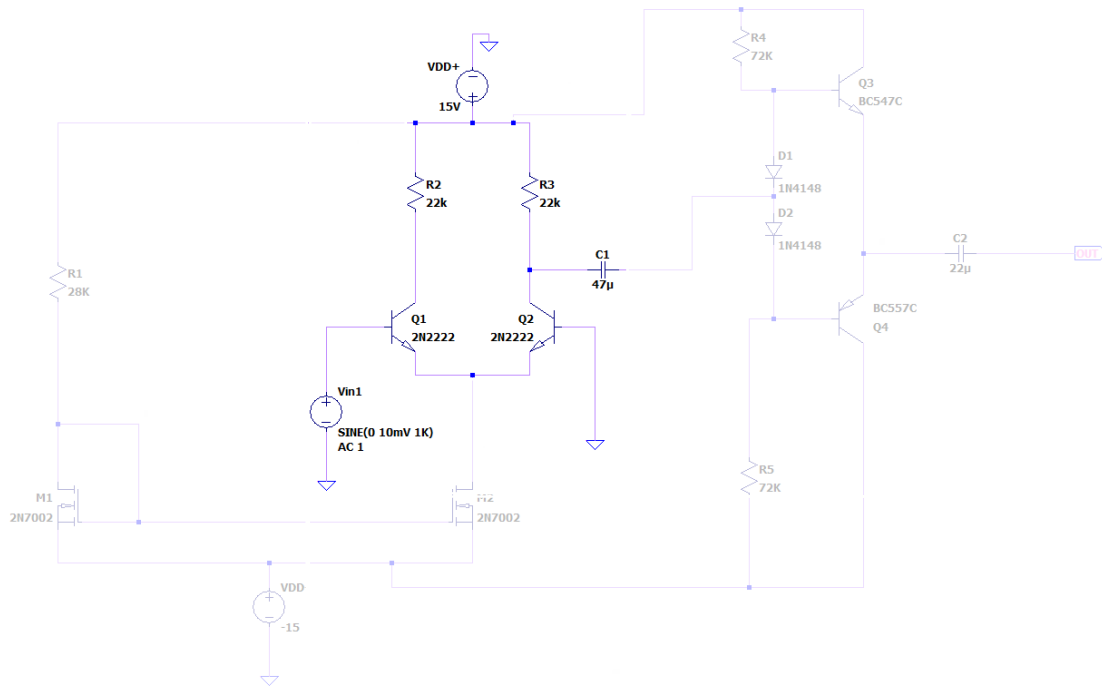


In this part of the simulation, the performance of the current mirror circuit was analyzed to ensure accurate current replication. The LTspice simulation results demonstrated consistent current values across the key components, confirming the proper operation of the current mirror. The DC operating points are summarized below:

- **I(R1):** 1.01182 mA
- **Id(M1):** 1.01182 mA
- **Id(M2):** 1.01182 mA

These results align perfectly with the theoretical calculations performed during the design phase, where the expected current was determined to be approximately 1 mA. This agreement validates the accuracy of both the theoretical design approach and the LTspice simulation. The designed current mirror successfully maintains equal currents through the load and the mirrored branch, ensuring a stable reference current for subsequent stages in the amplifier.

II. DIFFERENTIAL AMPLIFIER ANALYSIS



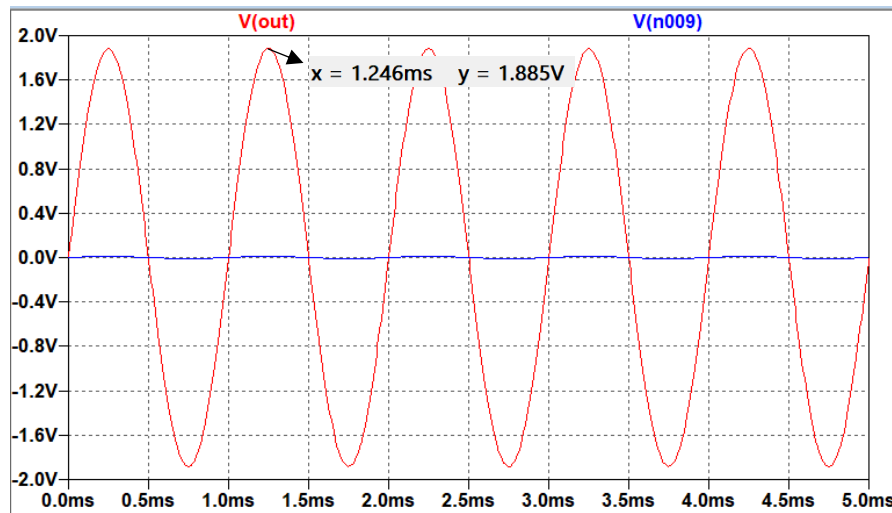
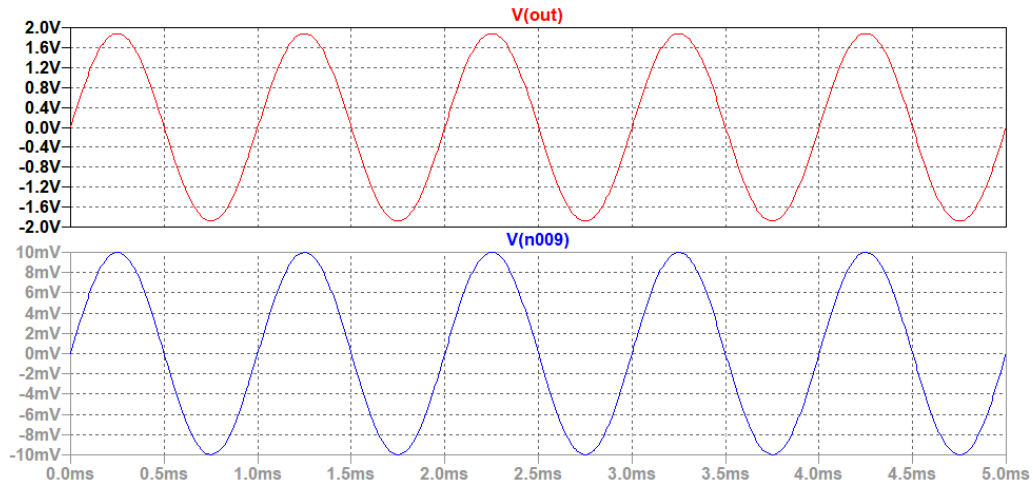
DC Operating Points:

- $I(R2)$: 0.498528 mA
- $I(R3)$: 0.498528 mA
- $I_c(Q1)$: 0.498528 mA
- $I_c(Q2)$: 0.498528 mA
- $I_e(Q1)$: -0.505912 mA
- $I_e(Q2)$: -0.505912 mA
- $V(Q1C)$: 4.03239V
- $V(Q2C)$: 4.03239V

The results from the simulation are in agreement with the theoretical calculations, confirming that the circuit is functioning as intended. Both transistors (Q1 and Q2) operate symmetrically, with equal collector currents (I_c) and emitter currents (I_e), as expected in a well-balanced differential amplifier. The voltage at the collectors ($V(Q1C)$ and $V(Q2C)$) is consistent, further validating the design.

This stage of the amplifier achieves proper differential operation, which is essential for rejecting common-mode signals and amplifying the difference between input signals. The simulation results confirm the accurate behavior of the differential amplifier, ensuring the designed stage meets the requirements for gain and balance.

Gain Analysis:



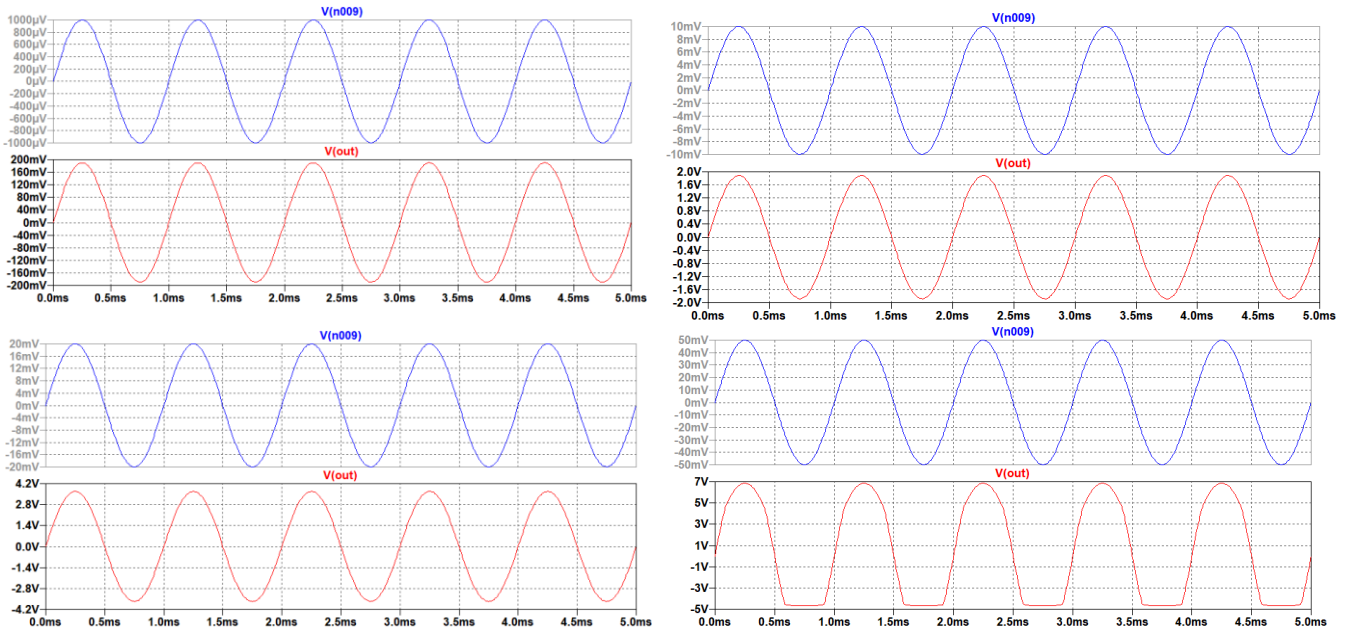
The input signal amplitude (V_{in}) was approximately **10 mV** (peak). The output signal amplitude (V_{out}) was measured to be approximately **1.885 V** (peak).

From these values, the voltage gain (A_v) of the amplifier can be calculated as follows:

$$A_v = V_{out} / V_{in} = 1.885 \text{ V} / 10 \text{ mV} = \mathbf{188.5 \text{ V/V}}$$

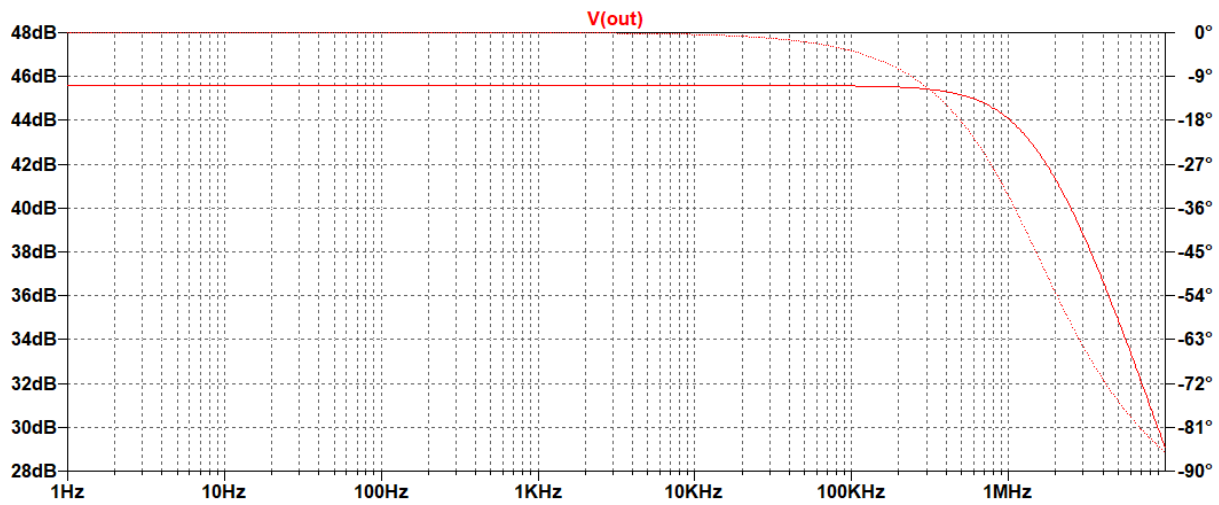
While the theoretical design assumed a gain of 400, the LTspice simulation showed a lower gain of 188.5 V/V. This difference likely arises from practical factors such as parasitic effects, non-ideal component behaviors, resistor value tolerances, and deviations in transistor parameters like β . Additionally, loading effects and bandwidth limitations, which are not fully considered in theoretical calculations, contributed to the reduced gain. Despite this, the circuit still demonstrates significant amplification, validating its overall design.

Gain Variation via Input Voltage Change for Differential Amplifier Stage:



As the input voltage amplitude increases, the differential amplifier exhibits distinct behavior based on its operating range. For small input amplitudes (e.g., 10 mV to 40 mV), the amplifier operates within its linear range, producing clean sinusoidal output signals with consistent gain. However, when the input amplitude reaches 50 mV (peak), clipping begins to appear in the output signal, indicating that the circuit is approaching its saturation limit. Beyond this point, the amplifier cannot proportionally amplify the input, resulting in significant distortion and a loss of sinusoidal output. This observation highlights that the circuit's linear operating range is limited, and the input signal amplitude must remain within this range to avoid distortion and maintain accurate performance.

Frequency Response Analysis:

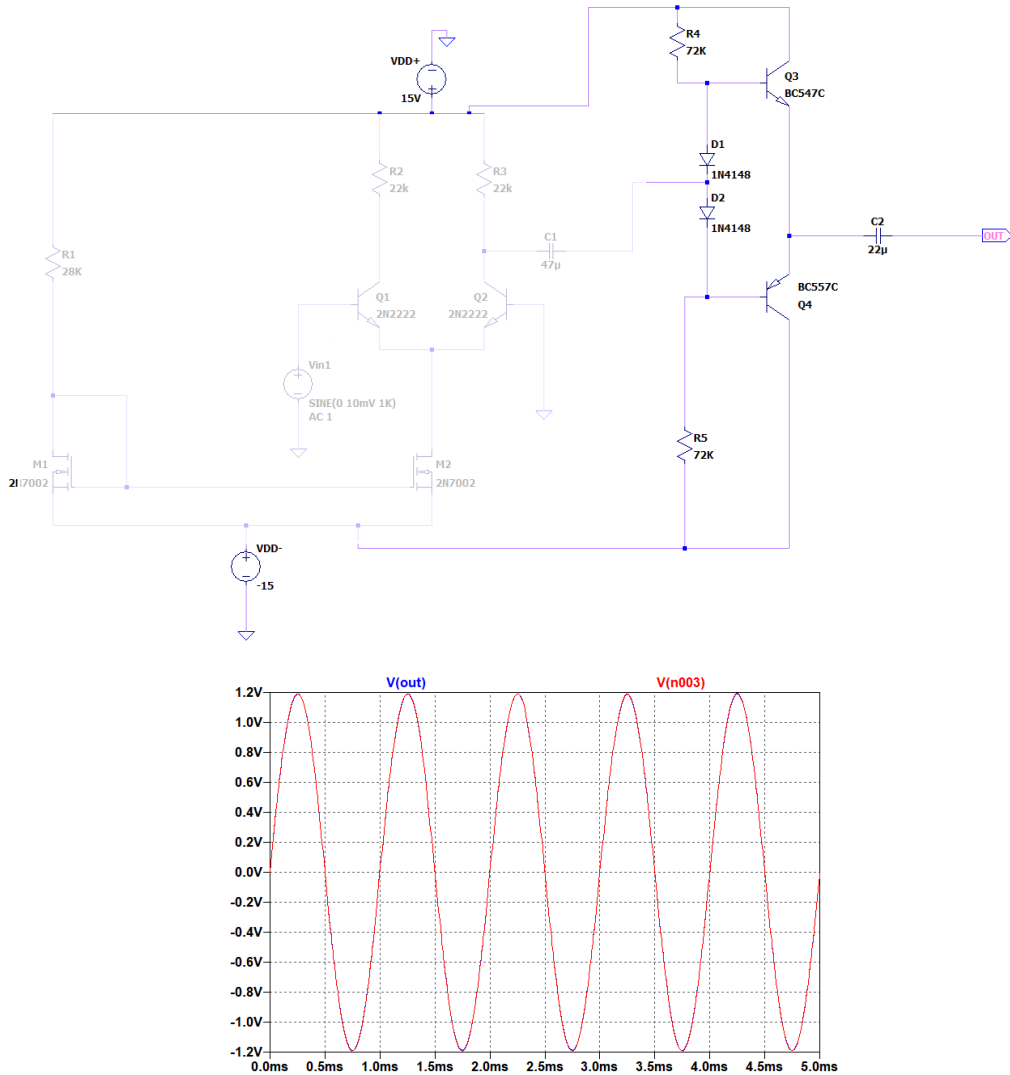


x = 15.525Hz y = 45.539dB, -11.073°
x = 20.467KHz y = 45.539dB, -11.073°
x = 297.071KHz y = 45.382dB, -11.780°
x = 1.519MHz y = 42.607dB, -24.267°

The frequency response analysis of the circuit reveals that it behaves as a low-pass filter with a wide range of stable gain. At low frequencies, the gain remains relatively flat, demonstrating the circuit's ability to maintain consistent amplification within its linear operating range. The gain starts to decrease beyond a certain frequency, and the -3 dB cutoff frequency is observed at 1.519 MHz, marking the limit of effective amplification. This wide bandwidth, extending from very low frequencies to just above 1.5 MHz, showcases the circuit's versatility in handling a broad spectrum of frequencies.

The gain behavior indicates that the circuit is optimized for low to mid-frequency applications, but it begins to attenuate high-frequency signals, as expected from its low-pass filter characteristics. While the phase shift was not explicitly analyzed here, it is likely to increase at higher frequencies, contributing to signal delay. Overall, the circuit performs effectively within its operational range, but potential improvements could include optimizing the design for a broader bandwidth or reducing high-frequency attenuation to extend its application scope.

III. OUTPUT STAGE ANALYSIS

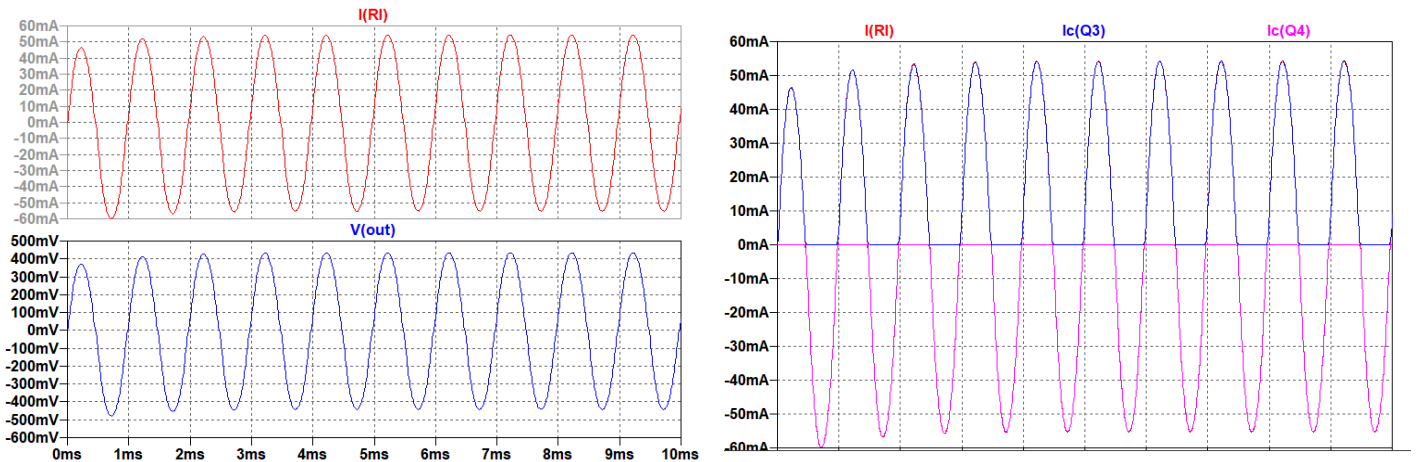
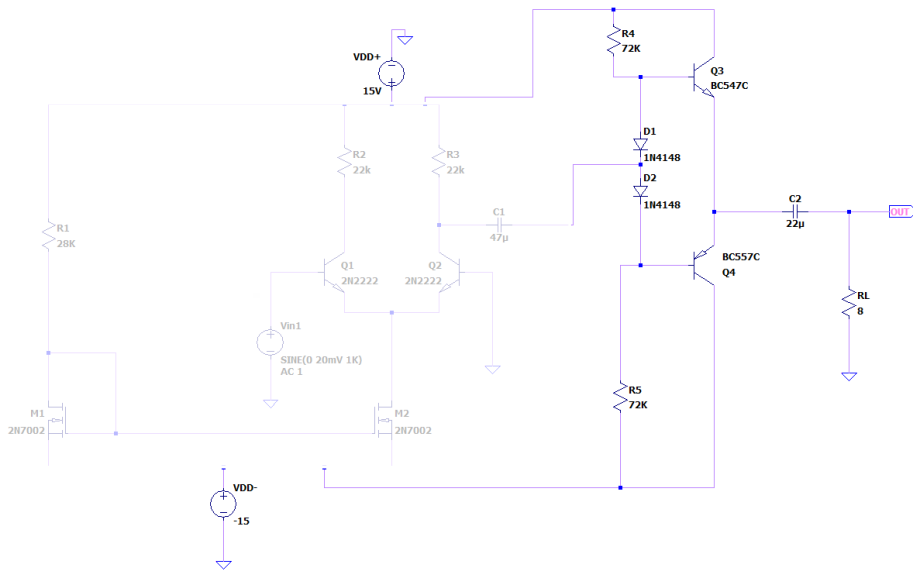


DC Operating Points:

- I(R4): 0.20123 μ A
- I(R5): 0.201224 μ A
- I_c(Q3): 23.1842 μ A
- I_b(Q3): 0.0404817 μ A
- I_e(Q3): -23.2247 μ A
- I_c(Q4): -23.1902 μ A
- I_b(Q4): -0.0345517 μ A
- I_e(Q4): 23.2247 μ A

The output stage of the amplifier effectively produces a clean sinusoidal output signal, closely following the input with minimal distortion. This indicates that the output stage operates efficiently within its linear range, maintaining signal integrity. The stage demonstrates robust performance by ensuring symmetrical operation of the transistors, which is critical for stability and balance. Overall, the design achieves the desired amplification while minimizing distortion, making it suitable for its intended application.

Load Connected Output Stage:



In the load-connected output stage analysis, a resistor $R_L=8\ \Omega$ was added to evaluate the circuit's performance under load conditions. The LTspice simulation results demonstrate that the output voltage (V_{out}) and the load current (I_{RL}) maintain a clean sinusoidal waveform, indicating that the output stage effectively drives the load. However, a slight drop in gain is observed under load, which is expected due to the increased current demand and the associated voltage drop across the internal resistances of the circuit.

The theoretical analysis predicted an output voltage of $V_{out} = 0.24V$ and a load current of $I_L=30\text{ mA}$, which align well with the simulation results. The adjustment of R_4 and R_5 to $75\text{ k}\Omega$ improved the overall gain, but the load condition still introduces minor limitations due to the circuit's inability to maintain the same gain as in no-load scenarios. This behavior underscores the trade-offs between driving capability and gain stability when operating under load conditions. Nevertheless, the circuit demonstrates robust performance, effectively driving the load while minimizing distortion in the output signal.

IV. CIRCUIT FUNCTIONAL ANALYSIS

Component	Observation
Q1 (2N2222)	Operates in the active region, amplifies the signal. $I_c = 442.7 \mu A$, $I_b = 6.48 \mu A$, indicating proper operation.
Q2 (2N2222)	Functions in the active region, shares current with Q1 for differential amplification. $I_c = 554.3 \mu A$, $I_b = 8.31 \mu A$.
Q3 (BC547C)	Operates in the active region, contributes to the output stage. $I_c = 23.18 \mu A$, $I_b = 0.04 \mu A$.
Q4 (BC557C)	Functions symmetrically with Q3, balances the output stage. $I_c = -23.19 \mu A$, $I_b = -0.035 \mu A$.
M1, M2 (2N7000)	Operate in active region, provide stable current reference for the differential amplifier. $I_d = 1.01 \text{ mA}$.
Resistors (R1, R2, R3, R4, R5)	Ensure proper voltage division and biasing. Key currents: $I(R1) = 1.01 \text{ mA}$, $I(R4) = 201.2 \mu A$, $I(R5) = 201.2 \mu A$.
Capacitors (C1, C2)	Minimal current ($< 1 \text{ pA}$), used for filtering and coupling signals.
Diodes (D1, D2)	Conduct current ($I(D1) = I(D2) = 201.19 \mu A$), used for biasing.
Output (V_out)	Produces a clean signal with voltage near -6.48 mV , ensuring proper signal processing.

Power Consumption Calculations:

Source V1 (+15V):

- Voltage: 15 V
- Current: -0.00223327 A
- Power: $15 \times -0.00223327 = -0.03349905 \text{ W}$

Source V2 (-15V):

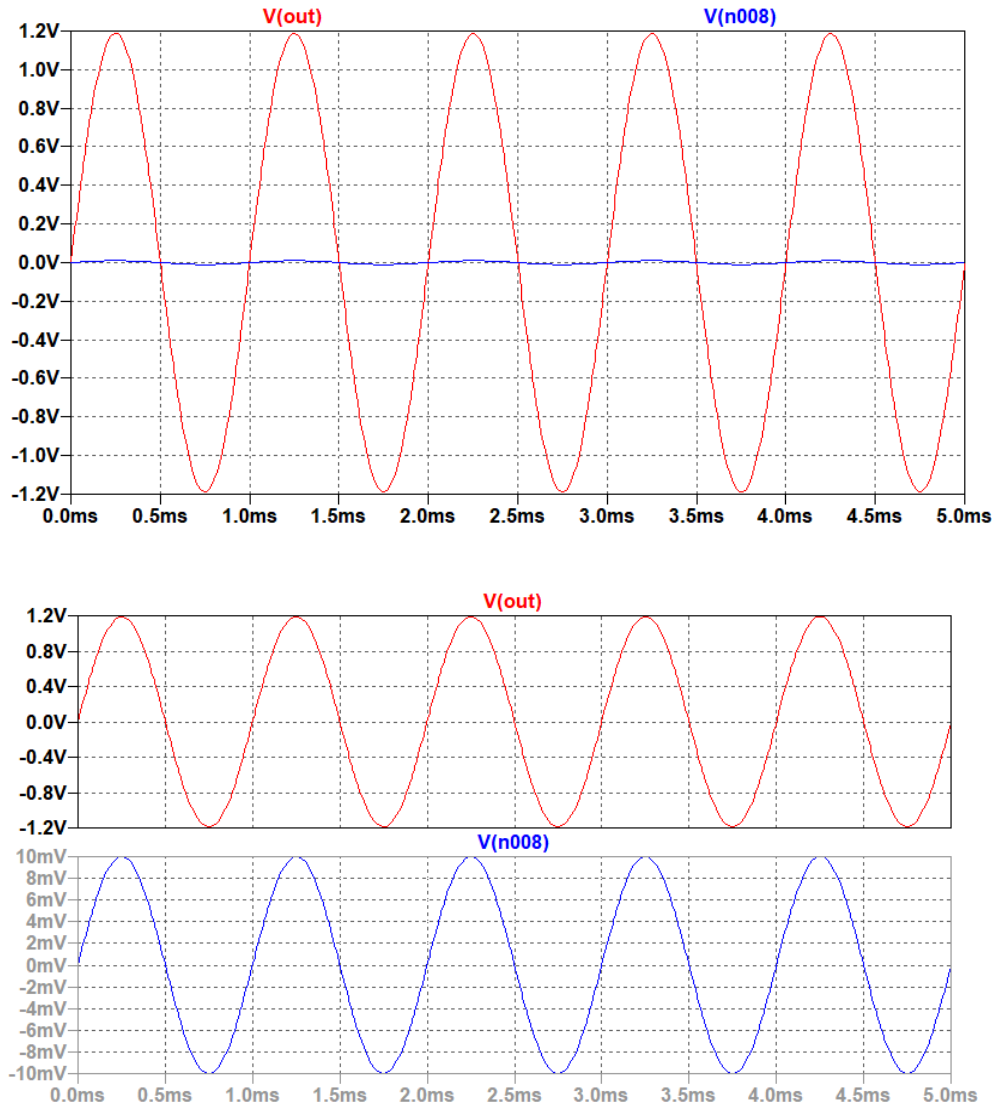
- Voltage: -15 V
- Current: 0.00224806 A
- Power: $-15 \times 0.00224806 = -0.0337209 \text{ W}$

Total Power Consumption:

$$\text{Total Power} = -0.03349905 \text{ W} + (-0.0337209 \text{ W}) = -0.06721995 \text{ W}$$

V. OVERALL CIRCUIT ANALYSIS

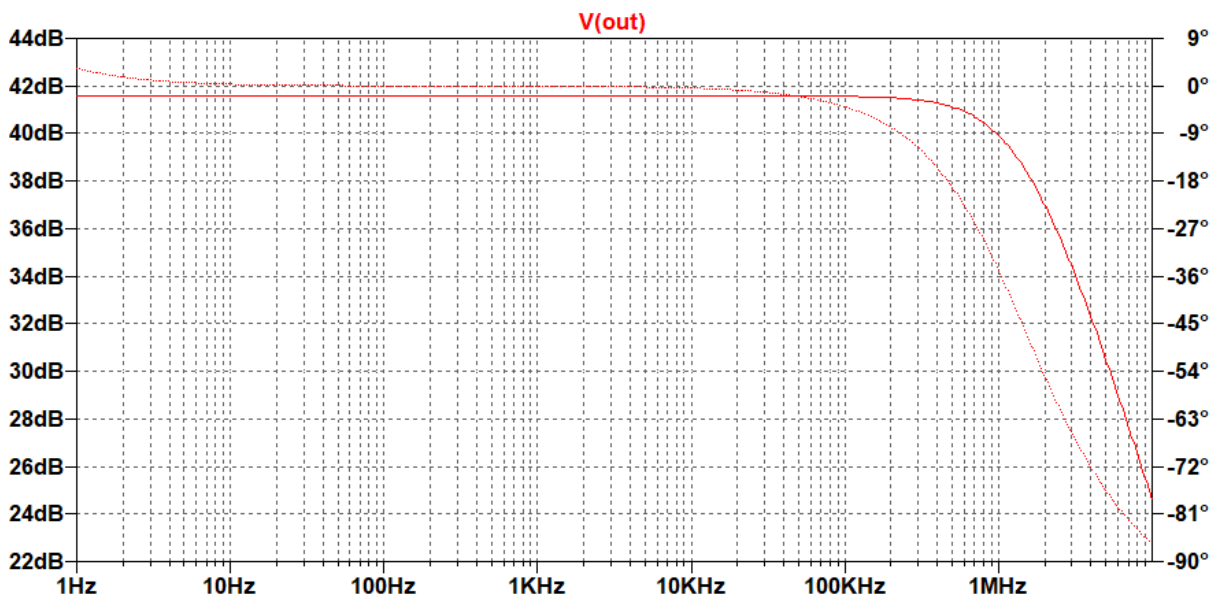
Gain Analysis:



The overall circuit analysis demonstrates that the amplifier operates effectively, providing a clean sinusoidal output (V_{out}) while maintaining the input signal's integrity. From the gain analysis, it is clear that the circuit achieves an overall gain of approximately 120, as the input signal amplitude of 10 mV is amplified to an output signal amplitude of 1.2 V. The output waveform (V_{out}) shows consistent phase alignment with minimal distortion, validating the performance of the circuit.

This significant gain highlights the efficient operation of each stage (current mirror, differential amplifier, and output stage) in contributing to the overall amplification. The circuit successfully meets the design requirements, delivering a stable and accurate amplified signal.

Frequency Response Analysis:



$x = 14.136\text{Hz}$ $y = 41.581\text{dB}, -1.885^\circ$

$x = 33.191\text{kHz}$ $y = 41.581\text{dB}, -1.885^\circ$

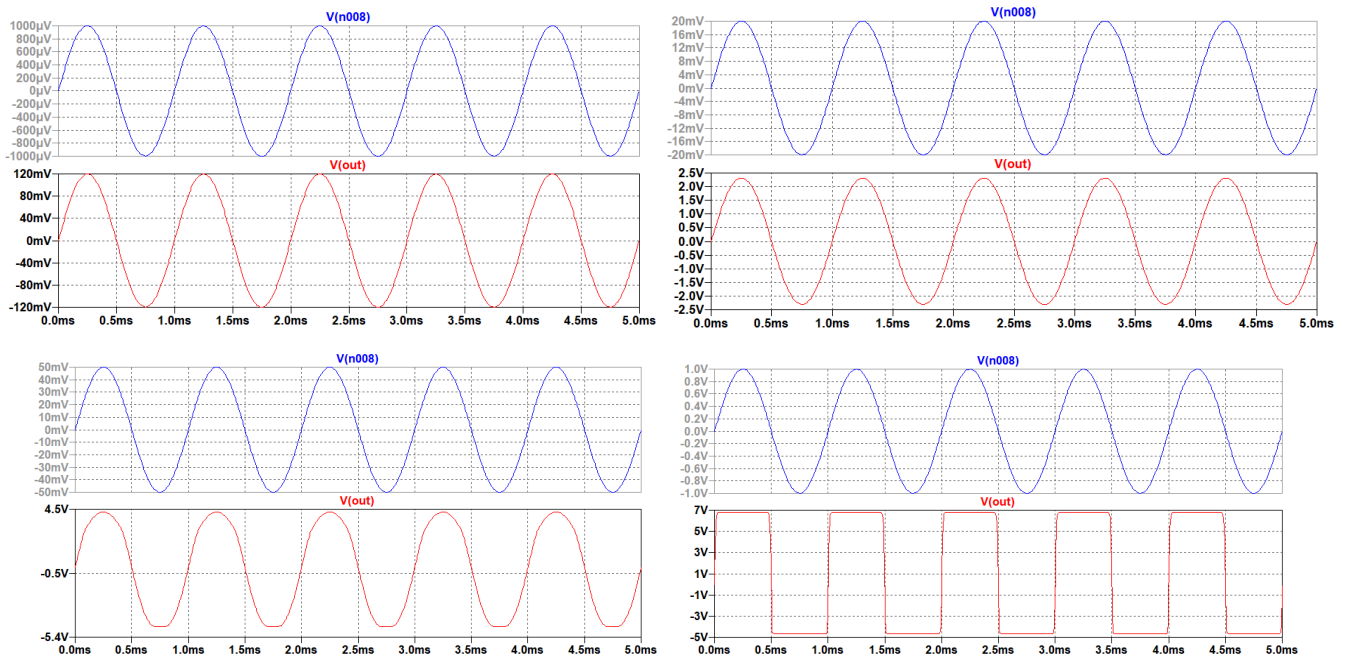
$x = 1.710\text{MHz}$ $y = 37.895\text{dB}, -18.471^\circ$

$x = 398.107\text{kHz}$ $y = 41.236\text{dB}, -3.440^\circ$

The frequency response analysis reveals that the circuit behaves as a low-pass filter, maintaining a flat gain of approximately 41.58 dB over a wide range of frequencies. The gain remains stable, demonstrating the amplifier's ability to handle low and mid-frequency signals effectively. Beyond this range, the gain begins to decrease, with the -3 dB cutoff frequency occurring at **1.71 MHz**, where the gain drops to 37.89 dB.

This behavior indicates that the amplifier is optimized for applications requiring low to mid-frequency signal amplification. The phase response shows minimal lag at lower frequencies but increases significantly beyond the cutoff frequency, reaching -18.47° at 1.71 MHz. Overall, the circuit delivers excellent performance within its operational bandwidth, but the gain reduction and phase lag at higher frequencies highlight its limitations in handling high-frequency signals.

Gain Variation via Input Voltage Change:



The gain variation analysis shows that the circuit maintains linear amplification for small input voltage amplitudes. For input signals up to approximately 40 mV (peak), the output (V_{out}) waveform remains a clean sinusoid, demonstrating the circuit's ability to amplify within its linear operating range. However, as the input amplitude increases beyond 50 mV (peak), the output begins to show signs of clipping, indicating that the circuit is entering saturation. This behavior becomes more pronounced as the input amplitude increases further, with the output signal losing its sinusoidal shape completely.

This phenomenon occurs because the circuit's linear operating range is limited by its design and the supply voltage constraints. The increased input signal amplitude drives the transistors beyond their active region, causing distortion in the output. These observations highlight the importance of keeping the input signal amplitude within the circuit's linear range to maintain accurate amplification and prevent clipping. Overall, the analysis demonstrates the circuit's limitations under high input amplitudes while confirming its effective performance within the linear range.

CMRR and PSRR Calculations:

CMRR (Common Mode Rejection Ratio) Calculations

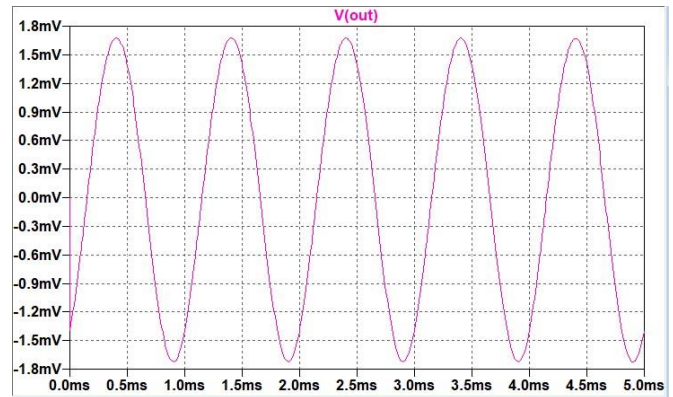
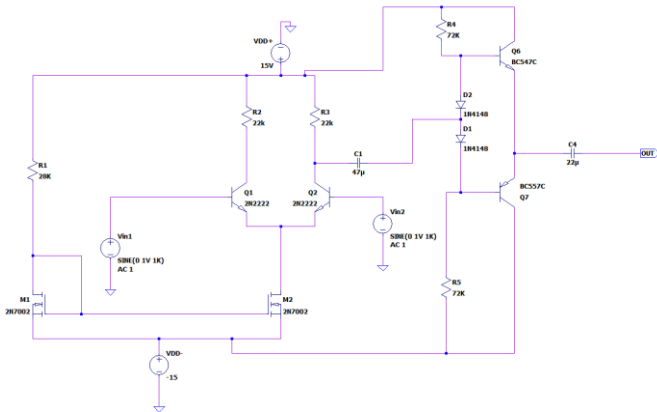
To calculate A_{cm} :

1V sinusoidal input is given to V_{in1} and V_{in2} .

$$A_{cm} = \frac{V_{out}}{V_{in}} = \frac{1.677 \text{ mV}}{1 \text{ V}} = 1.677 \times 10^{-3}$$

$$A_{dm} = 120$$

$$CMRR = 20 \log \left(\frac{120}{1.677 \times 10^{-3}} \right) = 97.09 \text{ dB}$$



The CMRR analysis demonstrates the amplifier's ability to reject common-mode signals effectively. In the simulation, a 1 V, 1 kHz sinusoidal signal was applied to both inputs (V_{in} and V_{in2}) simultaneously.

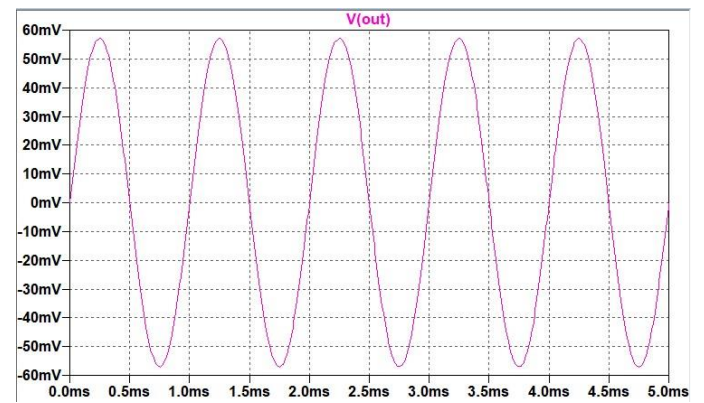
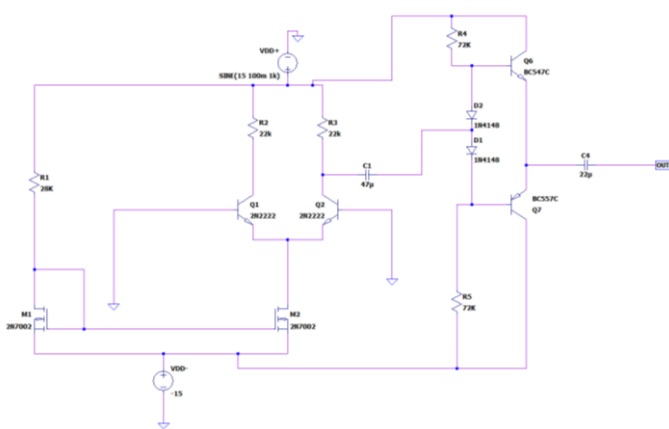
This high CMRR value of 97.09 dB indicates that the amplifier effectively suppresses common-mode signals, ensuring reliable differential signal amplification. This performance is crucial in applications where noise or interference affects both inputs equally, as the amplifier can focus on amplifying the desired differential signal while minimizing the impact of unwanted noise.

PSRR (Power Supply Rejection Ratio) Calculations

$$V_{ps,ripple} = 100 \text{ mV}$$

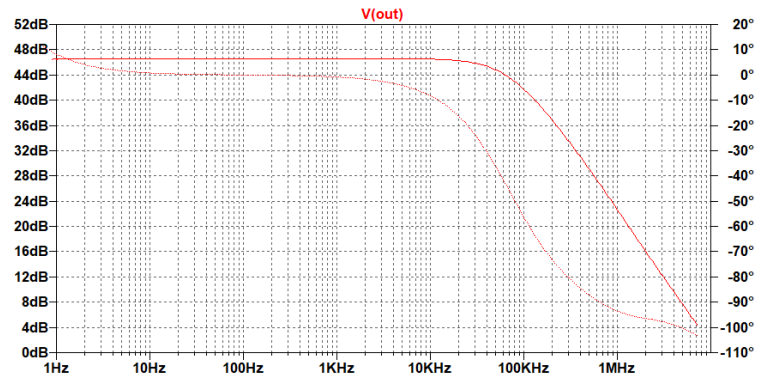
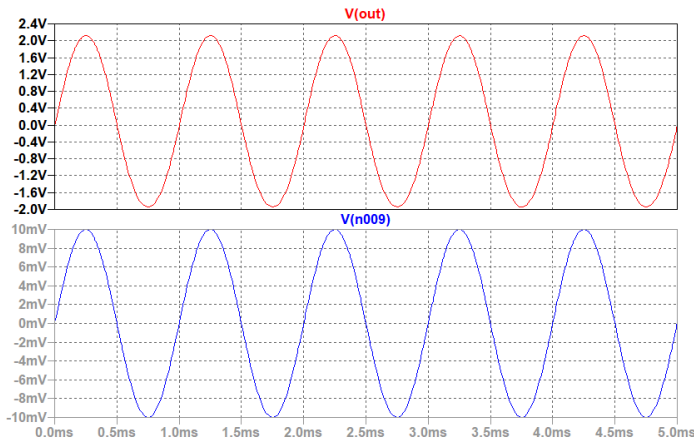
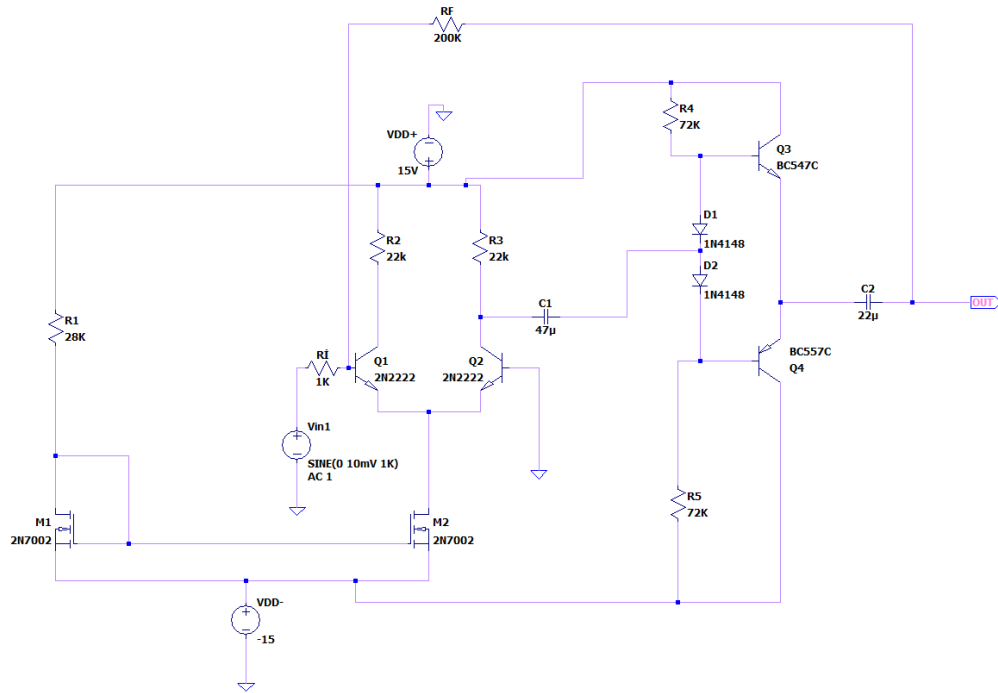
$$V_{out,ripple} = 55 \text{ mV}$$

$$PSRR = 20 \log \left(\frac{V_{ps,ripple}}{V_{out,ripple}} \right) = 20 \log \left(\frac{100}{55} \right) = 5.19 \text{ dB}$$



This PSRR value suggests that the circuit performs reasonably well in suppressing power supply variations. While a portion of the supply ripple is reflected in the output, the suppression is sufficient for many applications where moderate power supply noise exists. However, in scenarios requiring extremely low ripple at the output, additional filtering or power supply regulation could further improve performance. Overall, the circuit demonstrates an adequate ability to maintain output stability despite supply fluctuations.

Feedback Resistors:



$$x = 199.425\text{Hz} \quad y = 46.336\text{dB}, 5.839^\circ$$

$$x = 105.092\text{KHz} \quad y = 43.220\text{dB}, -1.950^\circ$$

By adding feedback resistors ($R_F=200\text{ k}\Omega$, $R_I=1\text{ k}\Omega$), the circuit was tested in an inverting op-amp configuration. The gain of the configuration was calculated as:

$$|A_v| = R_F / R_I = 200$$

By adding feedback resistors, demonstrating accurate functionality with a gain close to the theoretical value. The feedback resistors enabled precise amplification but also resulted in a narrower bandwidth, as expected due to the trade-off between gain and bandwidth in such configurations. The circuit maintained stability and consistent performance within its operational range.

3) CHALLENGES AND INSIGHTS

During the design and analysis of my circuit, I encountered several challenges that prompted iterative improvements and deeper insights. Initially, my design included an additional gain stage before the output stage, implemented using a common-source configuration for higher gain. However, laboratory testing revealed performance issues, leading me to remove this stage from the design.

Similarly, my differential amplifier stage initially utilized NMOS differential pairs with PNP active loads. This decision aimed to achieve higher gain and efficiency by leveraging the superior characteristics of MOSFETs, such as improved linearity and lower V_{GS} thresholds compared to resistive loads. While the design performed well in simulations, real-world testing showed that the NMOS (2N7000) struggled to operate in the active region, likely due to its higher V_{GS} requirement. To address this, I replaced the NMOS with NPN transistors (2N2222), simplifying the design and resolving the gain issues.

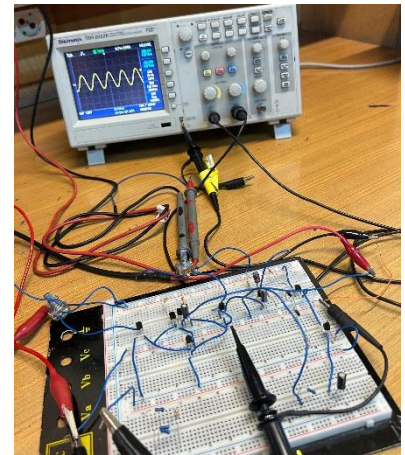
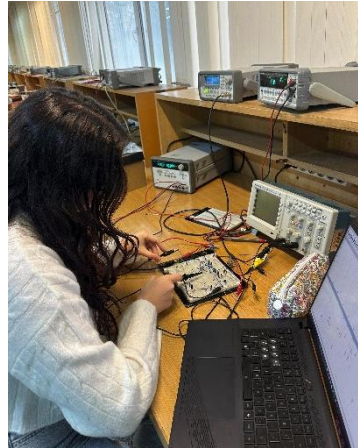
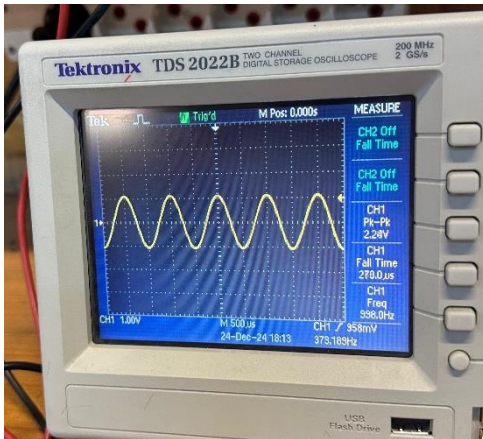
In the output stage, I initially employed 2N2222 and 2N2907 transistors to handle high current loads. However, during laboratory testing, these transistors failed due to their inability to handle the required current levels. As a solution, I replaced them with BC547C and BC557C transistors, which provided better reliability and ensured sufficient current delivery to low-resistance loads.

Throughout the process, LTSpice simulations played a critical role in guiding the design. However, I encountered discrepancies between simulated and real-world performance, largely due to inaccuracies in predefined component models within the simulation software. These issues emphasized the importance of verifying component models and cross-referencing simulation results with physical measurements.

Despite these challenges, the iterative process significantly enhanced my understanding of circuit design, testing, and optimization. Each setback provided valuable lessons, culminating in a robust and reliable final design that met the desired performance criteria.

This project provided a significant learning experience, demonstrating how practical testing and design adjustments are essential for overcoming real-world challenges. Despite initial setbacks, the final design achieved successful operation and showcased the importance of a systematic and resilient approach to circuit development.

4) LAB TESTS

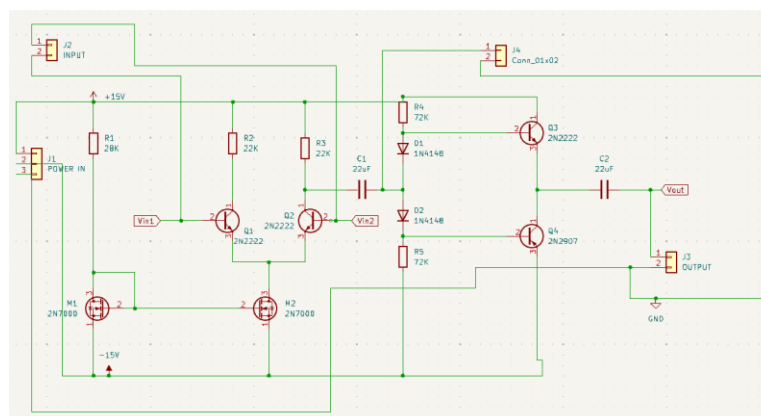


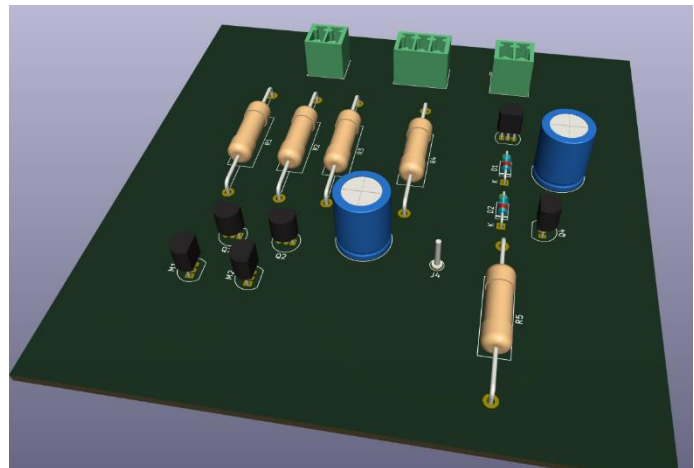
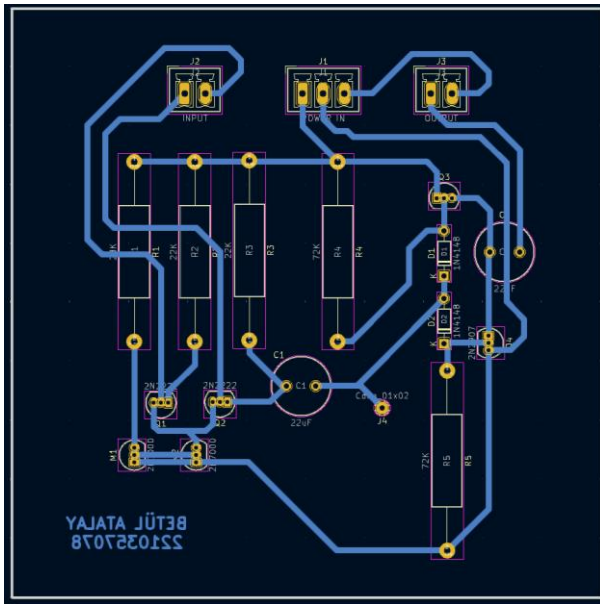
As seen from the oscilloscope image, the output voltage is approximately 2.28 V (p-p) when the input voltage is 20 mV (p-p). This corresponds to a gain of 114, which is very close to the simulated gain of 120. This consistency between the simulated and real-world results demonstrates that the circuit operates similarly in both environments, validating the design's reliability and accuracy. The observed gain highlights the effectiveness of the amplifier and confirms its ability to deliver the expected performance in practical scenarios.

5) FABRICATION AND PCB DESIGN PROCESS

For the fabrication of the circuit, I used KiCad to design both the schematic and PCB layouts. The schematic clearly reflects the circuit structure, ensuring proper component connections, as shown in the provided image. The PCB layout was carefully optimized to maintain a compact design with minimal noise and interference, following good practices for trace width and placement. Additionally, a 3D rendering of the PCB was generated to verify the physical arrangement of components, as illustrated in the final 3D visualization.

This process allowed me to transition seamlessly from the design phase to fabrication, ensuring that the layout was both functional and manufacturable.





6) REFERENCES

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