ELE 214

Electronics Laboratory - I

Multistage Amplifier Design and Fabrication

Term Project – Spring 2024

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PART 1

ANALYTICAL CALCULATIONS AND RESULTS

- **AMPLIFIER:**

An amplifier strengthens weak signals to make them more powerful, with different types including voltage amplifiers, current amplifiers, power amplifiers, and versatile operational amplifiers for tasks like amplification, filtering, and signal conditioning.

- **BUFFER STAGE:**

A buffer stage in an amplifier acts like a signal traffic cop. It keeps the input signal clean (high impedance) and strong (low impedance) for the next stage, preventing unwanted interactions like distortion and ensuring smooth operation.

- **EQUALIZER STAGE:**

The equalizer allows you to adjust the level of different frequencies within that amplified signal. Amplifiers increase the power of the entire audio signal, while equalizers allow adjustment of frequency levels within that amplified signal.

- **GAIN STAGE:**

The gain stage of an amplifier is the section where the signal is amplified, increasing its amplitude to a desired level for further processing or output.

- **MULTISTAGE AMPLIFIER:**

A multistage amplifier is an amplifier circuit that combines multiple single-stage amplifiers for increased overall signal amplification.

- **THE ROLE OF CAPACITOR IN AMPLIFIER DESIGN:**

In amplifier design, capacitors are used for coupling and bypassing: coupling capacitors block DC components while allowing AC signals to pass between stages, and bypass capacitors stabilize the voltage supply and filter out unwanted noise and AC ripple.

- **DIFFERENCES BETWEEN MOSFET AND BJT:**

MOSFET: Voltage-controlled device; having high input impedance; having faster switching speed; more power-efficient; better thermal stability; better suited for digital and high-frequency analog applications; generally easier to integrate into ICs.

BJT: Current-controlled device; having low input impedance; having slower switching speed; lesa power-efficient; more susceptible to thermal runaway; often preferred for analog amplification due to better linearity and gain characteristics; having more complex fabrication process.

2N2222 BJT:

Used for buffer stage.

Reason for Choice: With a low saturation voltage, the 2N2222 can efficiently operate in the saturation region, ensuring low voltage drops and minimal power loss in the buffer stage. Also it is widely available and provides a high input impedance and low output impedance.

Type: NPN

Transistor Parameters:

- Collector-Emitter Voltage (V_CEO): 40V
- Collector Current (I_C): 800mA
- DC Current Gain (h_FE): Typically 100-300 at I_C = 10mA
- Collector-Emitter Saturation Voltage (V_CE(sat)): Typically 0.3V at I_C = 500mA, I_B = 50mA
- Base-Emitter On Voltage (V_BE(on)): Typically 0.7V at I_C = 10mA

IRF510 MOSFET:

Used for gain stage.

Reason for Choice: The IRF510 boasts a high transconductance (gm), which translates to significant voltage gain in the amplifier stage.So, it can efficiently amplify the weak signal.

Type: N-channel power MOSFET

Transistor Parameters:

- Drain-Source Voltage (Vds): 100V
- Continuous Drain Current (Id): 5.6A (at 25°C)
- Gate Threshold Voltage (Vgs(th)): 2.0V to 4.0V
- Rds(on) (Drain-Source On-Resistance): 0.54Ω (at Vgs = 10V, Id = 4.0A)

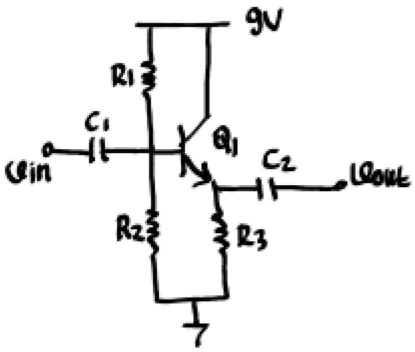
ANALYTICAL CALCULATIONS AND RESULTS

All the calculations given below have been made for these frequency values and gain:

- $\mathbf{f_{low}}$ = 780 Hz
- $\mathbf{f_{high}}$ = 12200Hz
- **Gain** = 8

The calculations that I wrote in handwriting are shown in the pictures below.

I. BUFFER STAGE CALCULATIONS



(i) I choose $R_1 = R_2$ for an appropriate biasing.

$$R_{in} = R_1 \,//\, R_2 \,//\, R_{in\text{-}BJT}$$

Calculating $R_{in\text{-}BJT} \approx \beta \cdot R_3$

$\beta = 100$ from datasheet and I choose $R_3 = 10k\Omega$

So, $R_{in\text{-}BJT} = 1M\Omega$

(ii) Quiescent current for R_1 and R_2 must be higher. I choose $R_1 = R_2 = 100k\Omega$.

With (i) and (ii):

$$R_{in} \approx 48k\Omega$$

(iii) $f_c = \dfrac{1}{2\pi (R_1 // R_2) C_1}$; $f_c = 780\,Hz$, $R_1 // R_2 = 50k\Omega$

$$f_c \leq 780Hz \rightarrow C_1 \geq 4nF$$

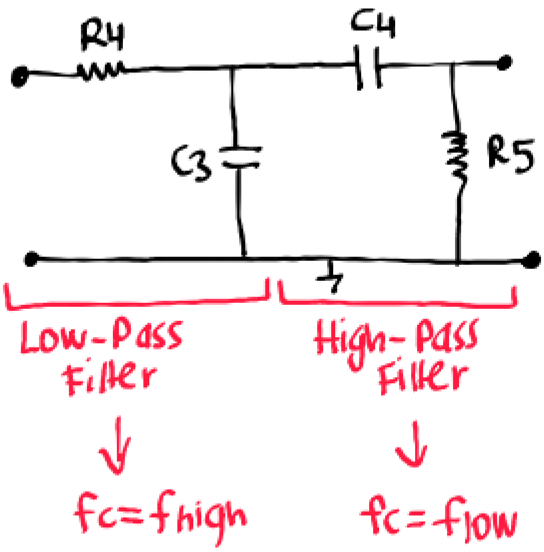
I choose $C_1 = 10\mu F$. This makes my buffer stage better.

(iv) $R_{out} \approx R_1 \,//\, \left(\dfrac{R_2 // R_3}{\beta} \right) \approx 476\Omega$

(v) With choosing C_2 as $100\mu F$, I observed better buffer stage. This capacitor is responsible for blocking the DC signal and allowing the 100mV AC signal.

Picture 1.1

II. EQUALIZER STAGE CALCULATIONS



for Low-Pass Filter:

$$12220\ \text{Hz} = \frac{1}{2\pi R_4 C_3} \rightarrow \begin{array}{l} R_4 = 1.3\text{k}\Omega \\ C_3 = 10\text{ nF} \end{array}$$

I choose lower value for C_3. This makes low-pass filtering better.

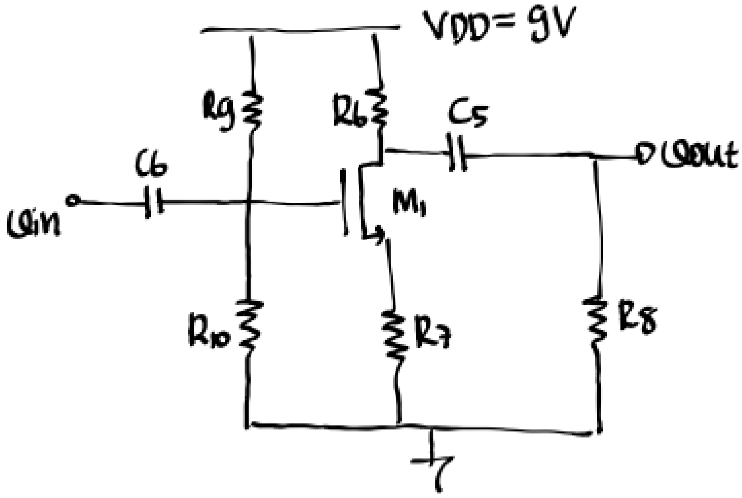
for High-Pass Filter:

$$780\ \text{Hz} = \frac{1}{2\pi R_5 C_4} \rightarrow \begin{array}{l} R_5 = 20.4\text{K}\Omega \\ C_4 = 10\text{nF} \end{array}$$

For R_4 and R_5 values, I use a potentiometer.

Picture 1.2

III. GAIN STAGE CALCULATIONS



$R_6 = R_D$
$R_7 = R_S$

(i) For voltage divider configuration, I choose R_9 and R_{10} values bigger i.e.

$$R_9 = R_{10} = 100\,k\Omega$$

(ii) Assume $I_D \approx 6mA$; $2V \leq V_{TH} \leq 4V$

Choose $V_{TH} = 3V$
$K = 8.25 \times 10^{-3}\, A/V^2$

$$I_D = K(V_{GS} - V_{TH})^2 \Rightarrow V_{GS} = 3.846V$$

(iii) For $V_D \approx 3V$,

$$R_D = \frac{V_D}{I_D} \approx 1k\Omega$$

(iv) $$|A_{cl}| = \frac{R_D}{\frac{1}{g_m} + R_S} \approx \frac{R_D}{R_S} = 8 \rightarrow R_S = 125\Omega$$

Picture 1.3

PART 2

1) BUFFER STAGE SIMULATION

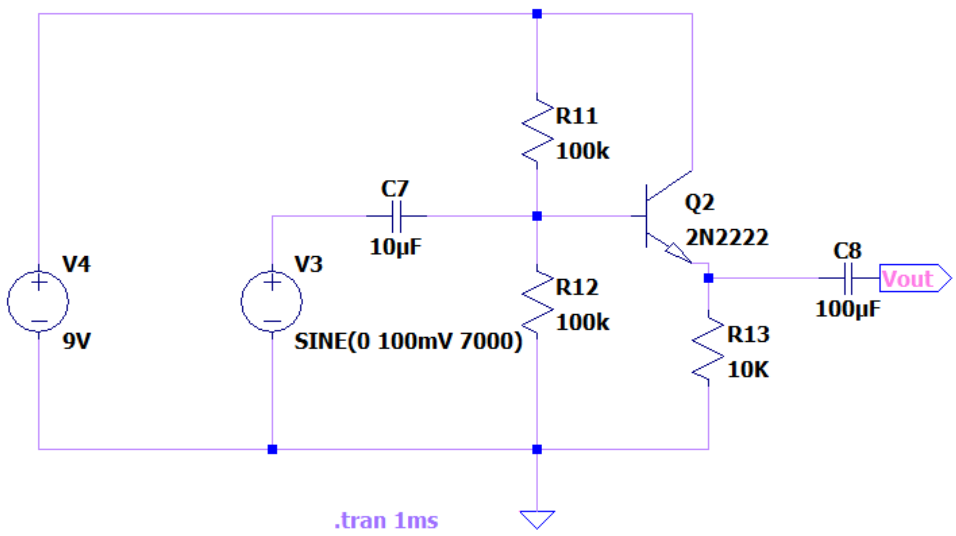
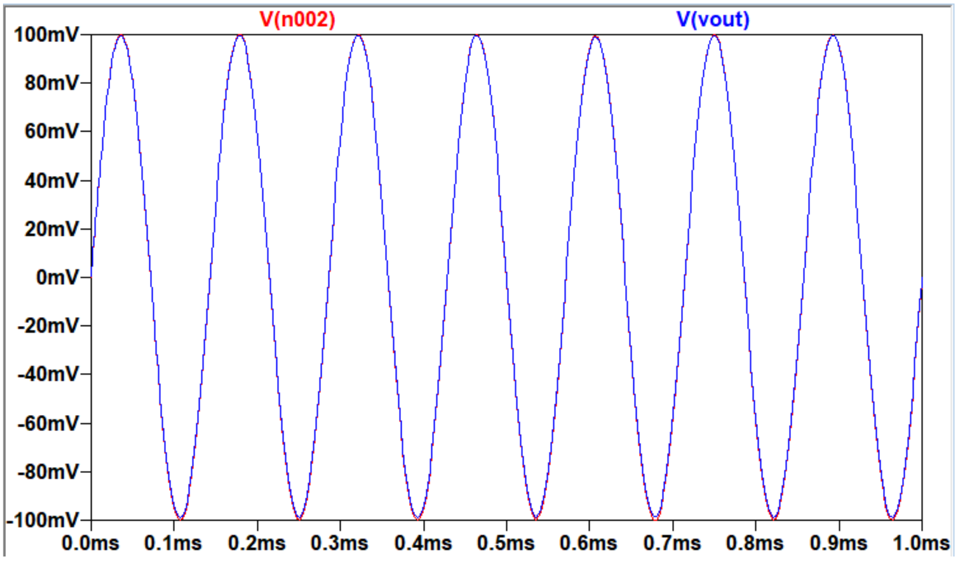
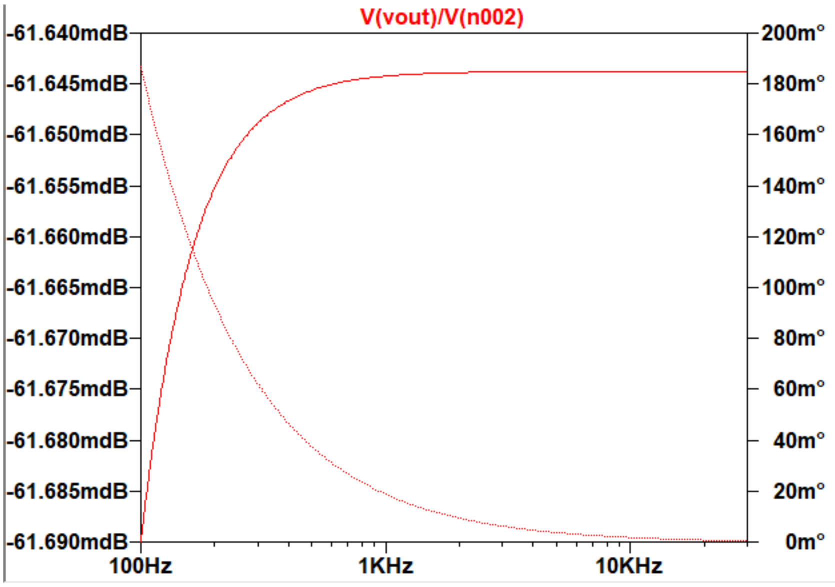


Figure 2.1



Graph 2.1

With choosing appropriate component values, I aimed that the gain should equal to 1. As seen in the Graph 2.1, Vout and Vin is almost equal and $Av \approx 1$.



Graph 2.2

Graph 2.2 shows the frequency response of the buffer stage.

2) EQUALIZER STAGE SIMULATION

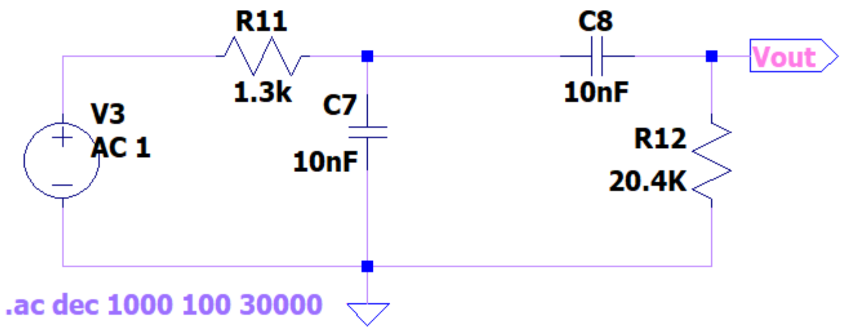
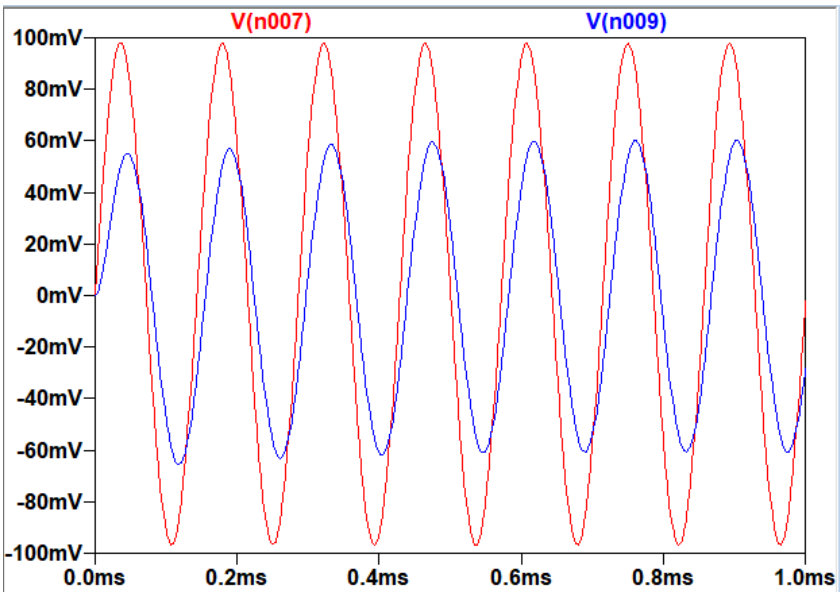
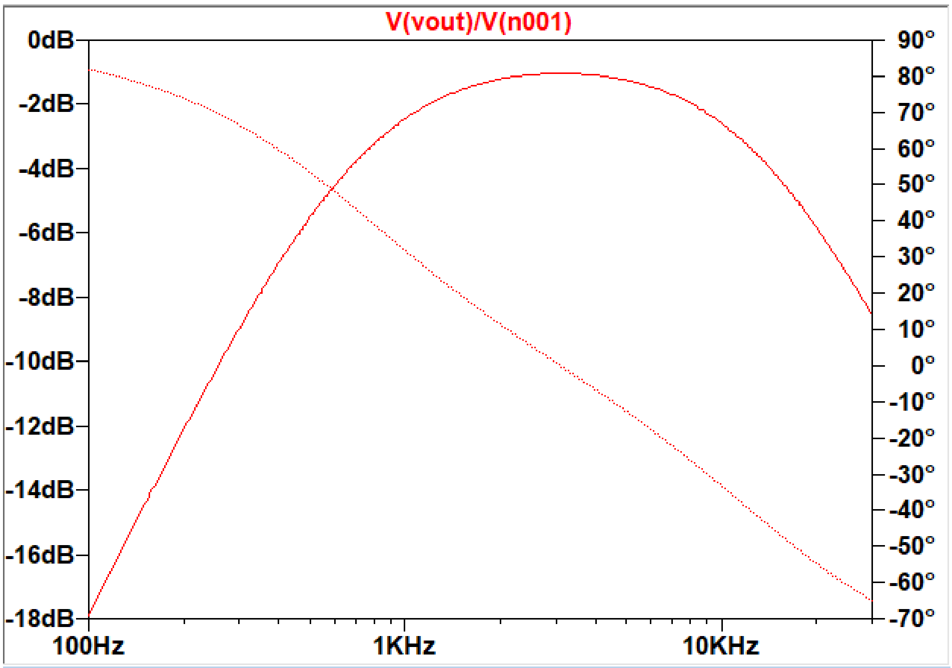


Figure 2.2



Graph 2.3



Graph 2.4

As seen in Figure 2.2, I set my equalizer circuit with bandpass filter. First part is low-pass filter which arranged for f_{high} = 12200Hz. Second part is high-pass filter which arranged for f_{low} = 780Hz. After the low-pass filter my gain stays constant, but after high-pass filter my gain decreases as expected as shown Graph 2.3. Red line indicates the output of the buffer stage and the blue one indicates the output of equalizer stage.

I tried different frequency values to test my equalizer stage. I observed that the gain decreases for frequencies which is lower than f_{low} = 780Hz and higher than f_{high} = 12200Hz. Graph 2.4 shows the bandpass filters frequency response and there exists a 80-degree phase difference within the bandwidth

3) GAIN STAGE SIMULATION

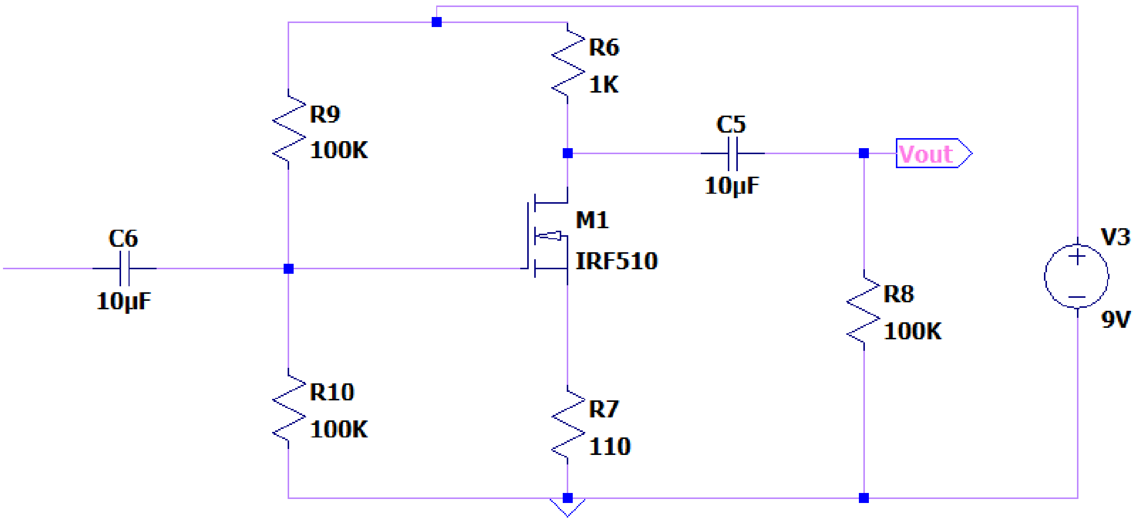
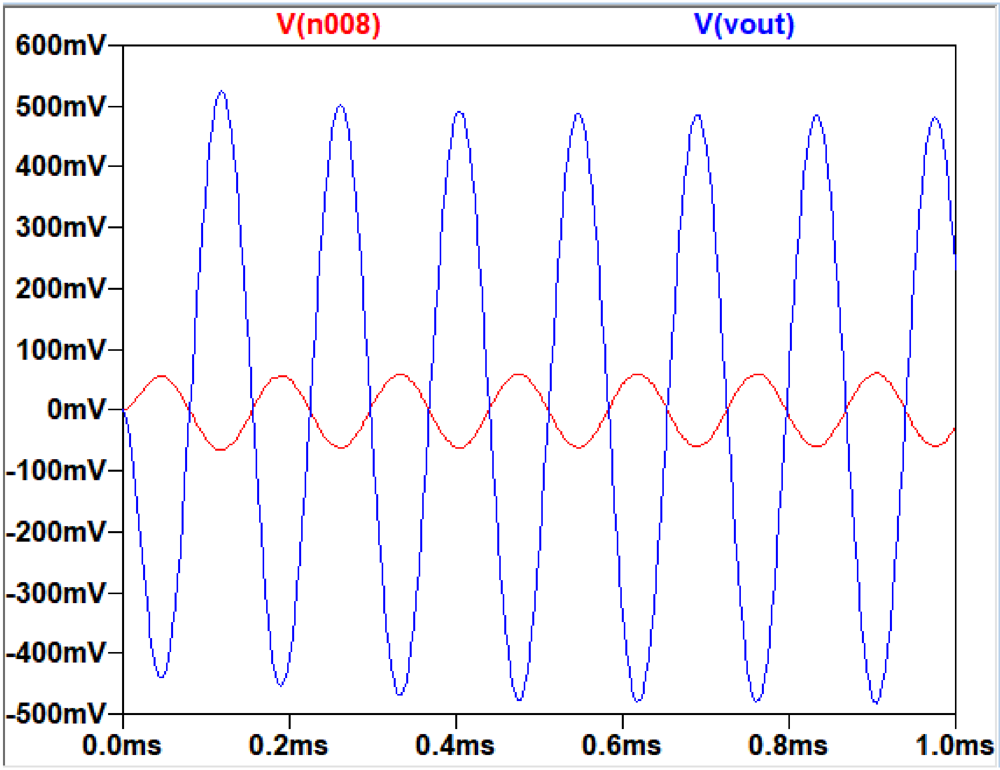
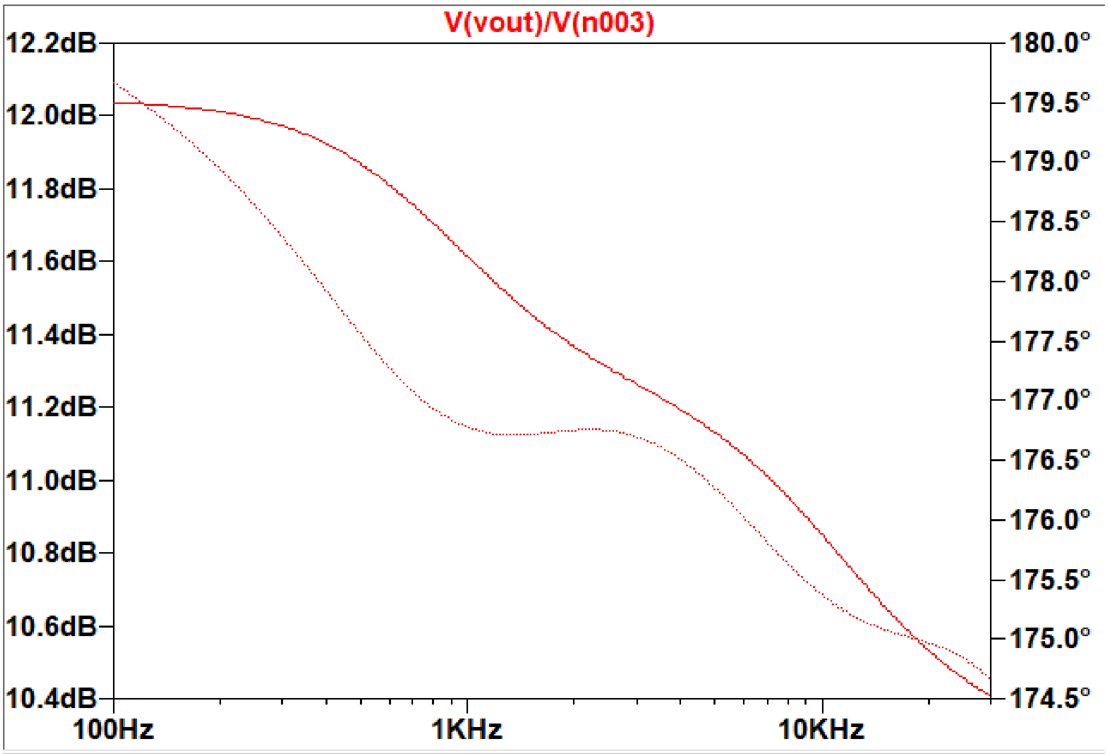


Figure 2.3



Graph 2.5



Graph 2.6

My gain must be 8. As seen in the Graph 2.5, input comes from the equalizer stage. It is approximately 60Mv. Output is observed from the C5 and its value is approximately 480Mv.

Gain = Vout/Vin = 480mV / 60mvV = 8.

4) MULTISTAGE AMPLIFIER SIMULATION

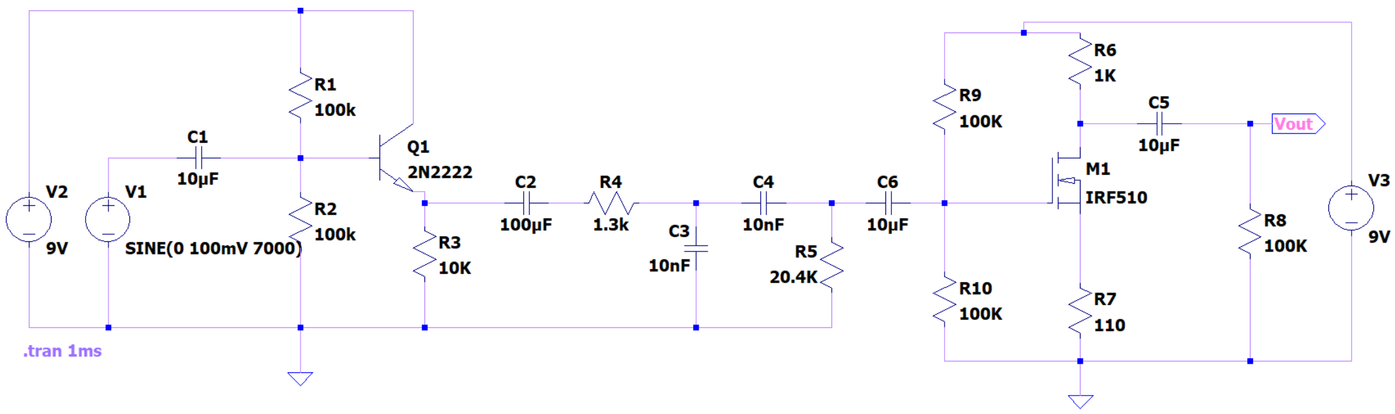
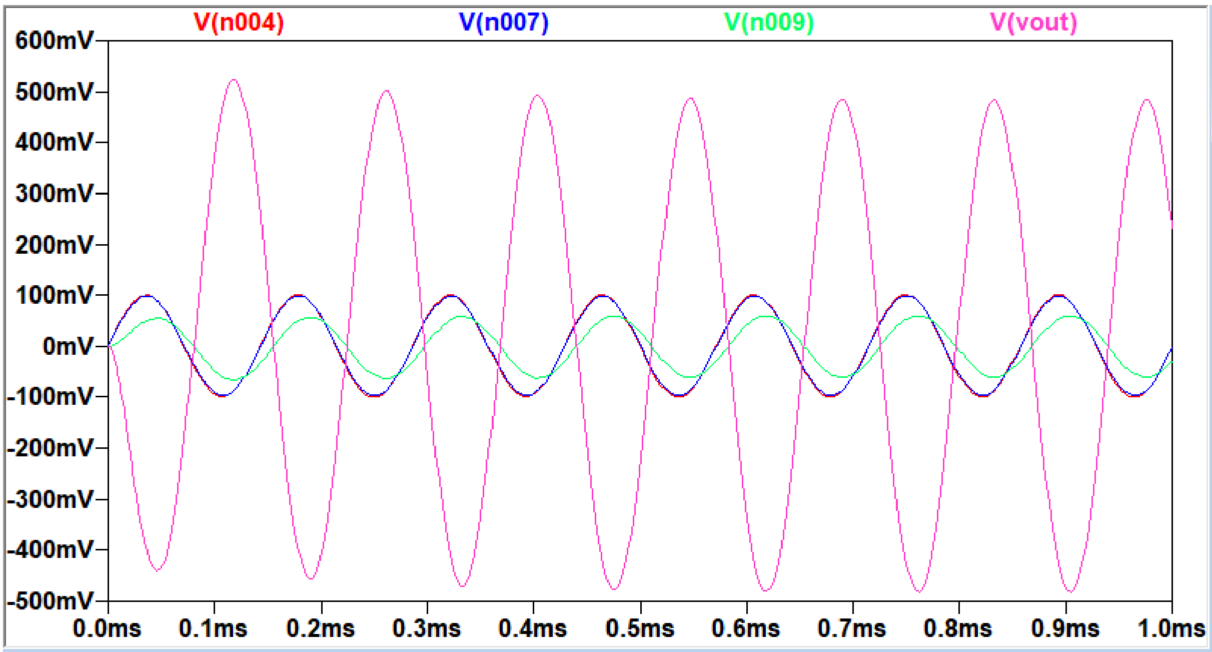


Figure 2.4

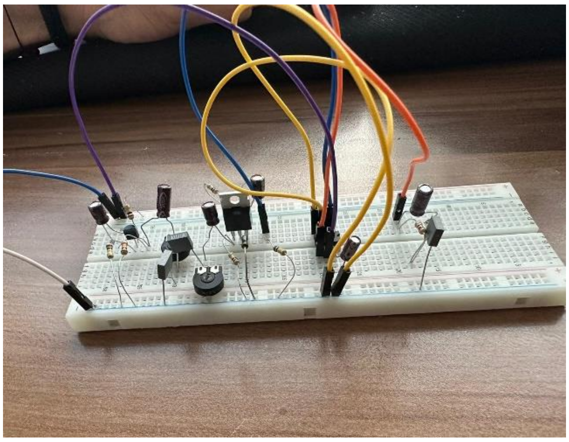


Graph 2.7

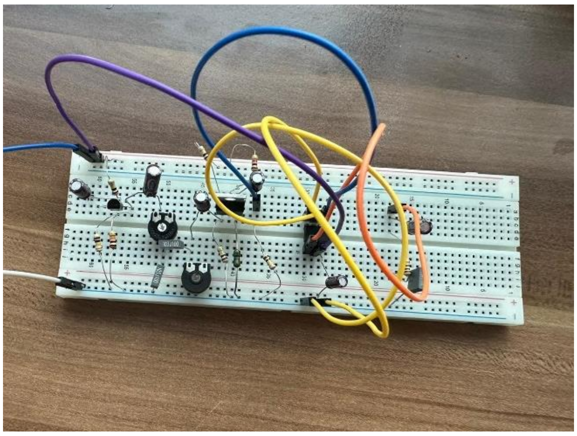
In the Graph 2.7, V(n004) (red line) indicates the input signal 100mV, V(n007) (blue line) is the output of the buffer stage and it is almost 100 mV, V(n009) (green line) is the output of the equalizer stage and it is 60 mV, and the last one V(vout) (pink line) is the output of the gain stage and approximately 480 – 500 mV.

PART 3

PHOTOS OF THE CIRCUIT ON BREADBOARD AND MEASUREMENTS

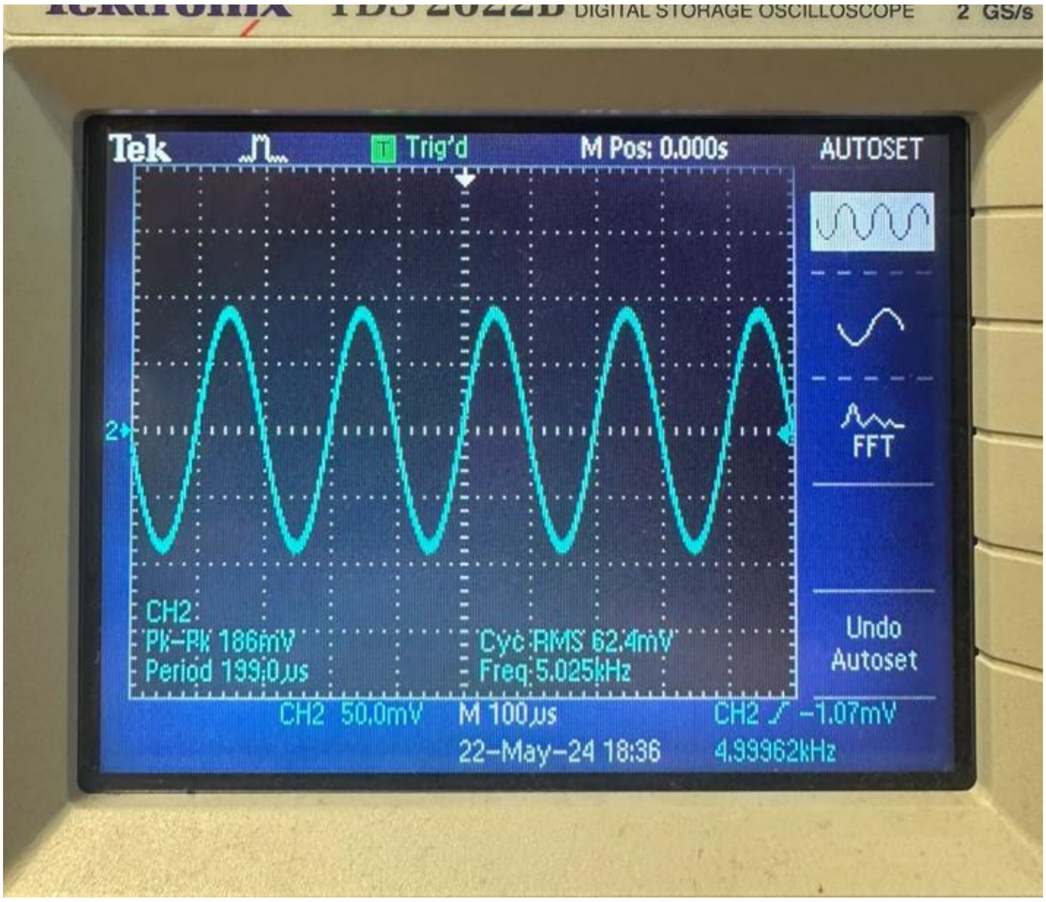


Picture 3.1



Picture 3.2

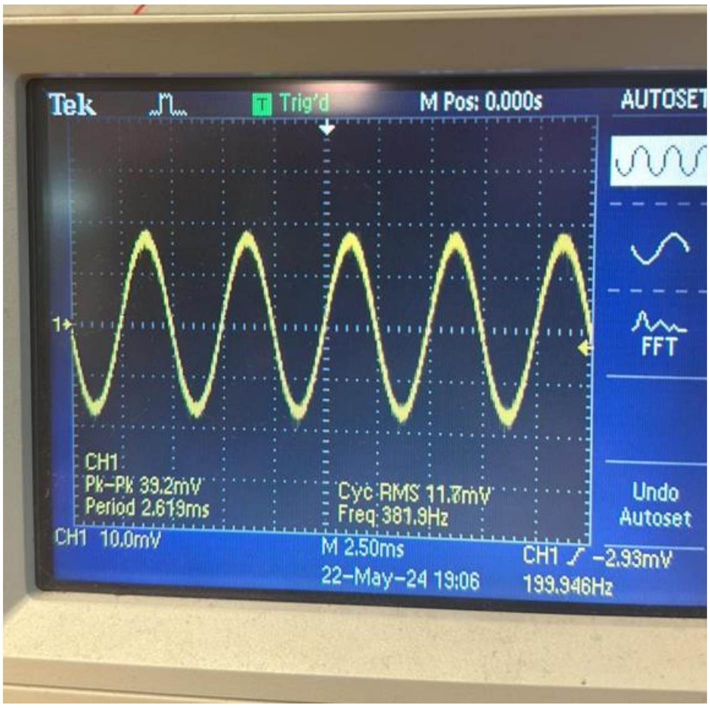
BUFFER STAGE:



Picture 3.3

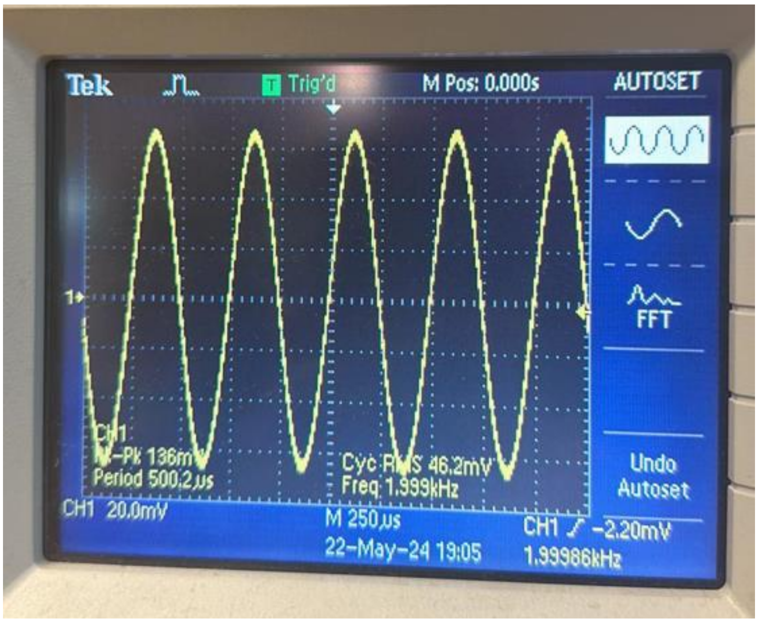
EQUALIZER STAGE:

- **f=200Hz:**



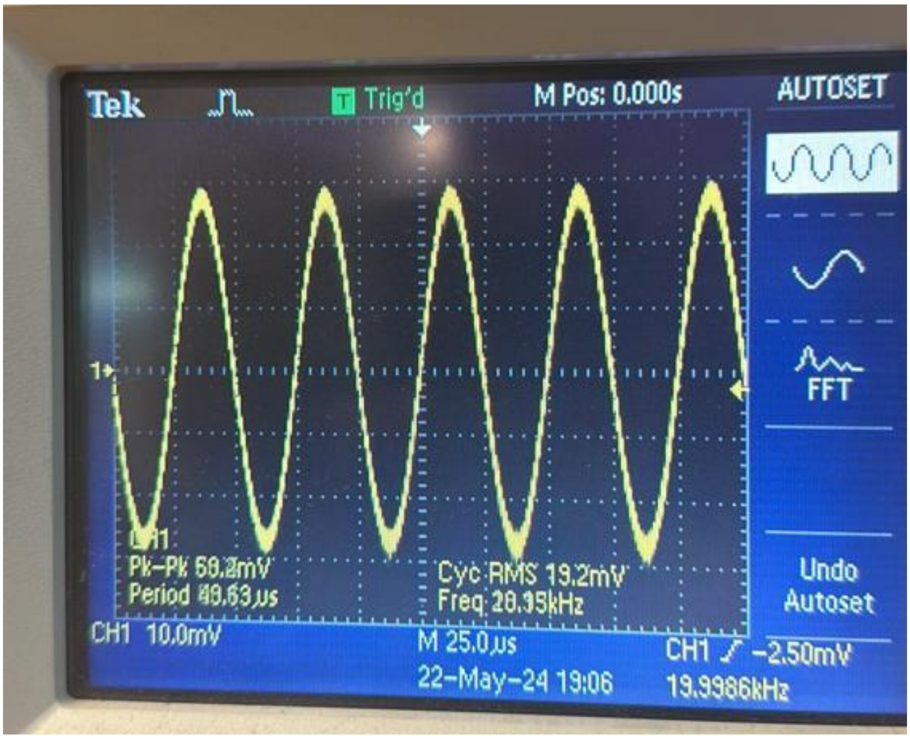
Picture 3.4

- **f = 2KHz:**



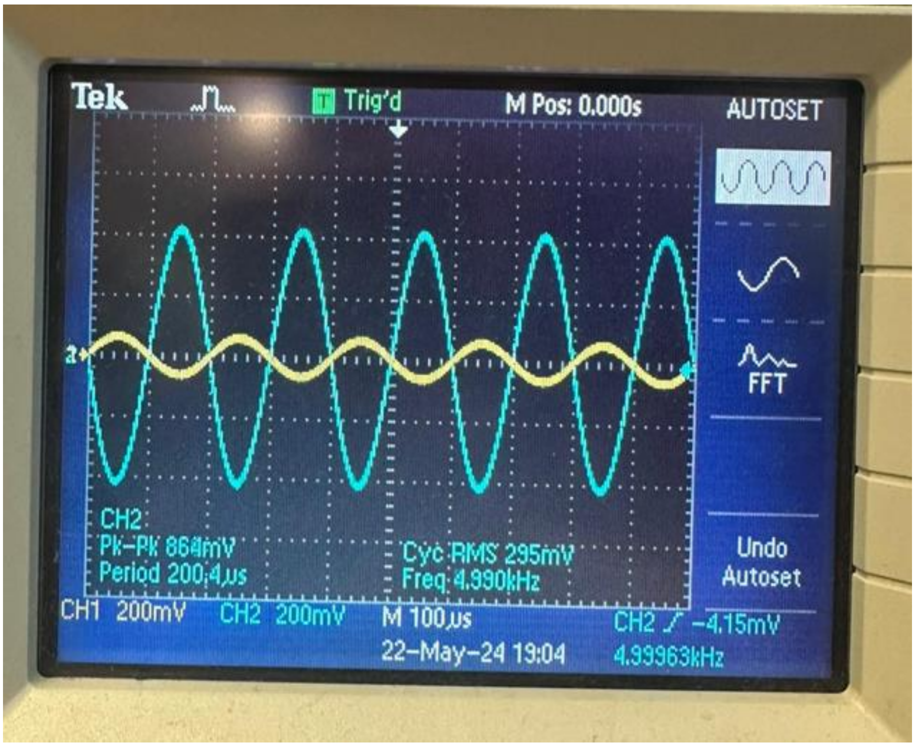
Picture 3.5

- **f=20KHz:**



Picture 3.6

GAIN STAGE:



Picture 3.7

CONCLUSION

In this project, I designed a multistage amplifier consisting of a buffer stage, an equalizer stage, and a gain stage. In the buffer stage, I used a 2N2222 BJT to fix the gain at 1. In the equalizer stage, I used a passive bandpass filter to adjust the frequency range, with the lowest frequency set at 780 Hz and the highest at 12.200 Hz. Finally, for the gain stage, I used an IRF510 MOSFET to achieve a gain of 8. I successfully completed all these stages as expected. Although there was some gain loss in the equalizer stage, my gain stage was able to amplify the output of this stage effectively. I tested my design in the electronics laboratory, and both my simulations and calculations were accurate.

LIST OF REFERENCES

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