Bevan Jebanesan Noble Anbunesan

Phone: (919) 438 9379 | Raleigh, NC | Email: <u>bevanjebanesan1@gmail.com</u> | www.linkedin.com/in/bevanjebanesan

EDUCATION

NC State University, Raleigh

Master of Science | Computer Engineering

• Coursework: ASIC and FPGA Design with Verilog, Microprocessor Architecture, Electronic System Level and Physical Design.

Anna University - Loyola ICAM College of Engineering and Technology, India

Aug 2021 – May 2025

Expected Graduation: May 2027

Bachelor of Engineering | Electronics and Communication Engineering

• Coursework: VLSI and Chip Design, Digital Systems Design, Embedded Systems and IOT Design

TECHNICAL SKILLS

- Technical: RTL design, Digital design, Timing constraints (SDC), CDC, Micro-Architecture
- Languages and Scripts: C, C++, Python, Verilog, System Verilog, TCL
- Tools: Altera Quartus Prime, Cadence (Virtuoso), Synopsys, AutoCAD, Git

PROJECT EXPERIENCE

C++ Cache & Memory Hierarchy Simulator

Aug 2025 – Oct 2025

- Designed a configurable two-level cache simulator (L1/L2) in C++ using command-line architecture parameters.
- Implemented write-back, write-allocate policies, LRU replacement, and dirty eviction tracking using bitwise tag/index extraction
- Debugged and resolved an issue where total reads were undercounted by isolating the discrepancy between read hits and trace-based read operations, improving result accuracy and validation consistency.
- Evaluated performance using SPEC CPU2006 memory access traces, measuring miss rates, memory traffic, and Average Access Time (AAT).
- Analyzed performance–area–energy tradeoffs using CACTI memory modeling to bridge architecture to hardware design insights.

C++ Branch Prediction Simulator

Ongoing

- Developing a branch prediction simulator in C++ to model bimodal, gshare, and hybrid predictors with configurable parameters.
- Implementing 2-bit saturating counters, a global branch history register, and a chooser table for dynamic prediction accuracy.
- Running simulations using SPEC CPU2006 branch traces to measure misprediction rates and evaluate predictor performance.
- Using Makefile automation and Gradescope validation to ensure correctness and efficient runtime.
- Exploring pipeline control hazards and correlation-based prediction techniques in modern CPU microarchitecture.

Verilog-based CNN Accelerator with DRAM Integration

Ongoing

- Developing a parameterized RTL CNN accelerator in SystemVerilog featuring a pipelined MAC array, on-chip SRAM buffers, and a DRAM controller for tiled feature-map access.
- Implementing fixed-point arithmetic, Leaky ReLU activation, and line-buffer-based convolution to optimize throughput and minimize off-chip bandwidth.
- Conducting synthesis and post-layout timing analysis to evaluate PPA tradeoffs, leveraging Synopsys Design Compiler and PrimeTime for constraint-driven optimization.

Accessible Communication System for Deaf Individuals

Jan 2025 - Apr 2025

- Spearheaded the design and development of a dual-interface communication system, improving accessibility for the deaf, and enabling real-time interactions with hearing individuals.
- Engineered a custom **ESP32-based wristband** with an OLED display and a vibration motor to deliver real-time, categorized notifications via Wi-Fi.
- Implemented a WebRTC-based video calling platform that features real-time Sign Language-to-Text (using CNN and MediaPipe) and Speech-to-Text (using Vosk API) transcription.
- Integrated a custom Android app to categorize incoming notifications and transmit them to the wristband based on user-defined modes.

IoT-Enabled Fire Detection and Alert System

Aug 2024 - Nov 2024

- Created a real-time, IoT-based fire detection and alert system using a Raspberry Pi 3B+ and a USB camera.
- Leveraged a custom HSV colour space model to precisely pinpoint fire regions based on predefined thresholds.
- Deployed an alert system that triggers an alarm, acquires geolocation data, and transmits real-time alerts to a designated webpage, specifying the fire's exact location.

RESEARCH AND PUBLICATIONS

IoT-Enabled Fire Detection and Alert System Leveraging HSV Thresholding.

- Publication: Journal of Ubiquitous Computing and Communication Technologies, Vol. 6, Issue 4, December 2024, pp. 338–352
- IoT-Enabled Fire Detection and Alert System Leveraging HSV Thresholding | IRO Journals