



Readout Chain Testing for ATLAS ITk Strip Detector

Kyle Beyer, kyle.beyer@cern.ch

Dylan Hatch, dylan.brown.hatch@cern.ch

Mentors: Richard Teuscher & Olivier Arnaez

11 Oct 2018



Agenda

Background

ATLAS & the Inner Detector
HL-LHC & ITk
ITk Design and Readout

Lab Testing of Hybrid Chips

Testing Setup
Progress & Goals

Acknowledgements

Background

ATLAS & the Inner Detector
HL-LHC & ITk
ITk Design and Readout

Lab Testing of Hybrid Chips

Testing Setup
Progress & Goals

Acknowledgements

Background

ATLAS & the Inner Detector
HL-LHC & ITk
ITk Design and Readout

Lab Testing of Hybrid Chips

Testing Setup
Progress & Goals

Acknowledgements

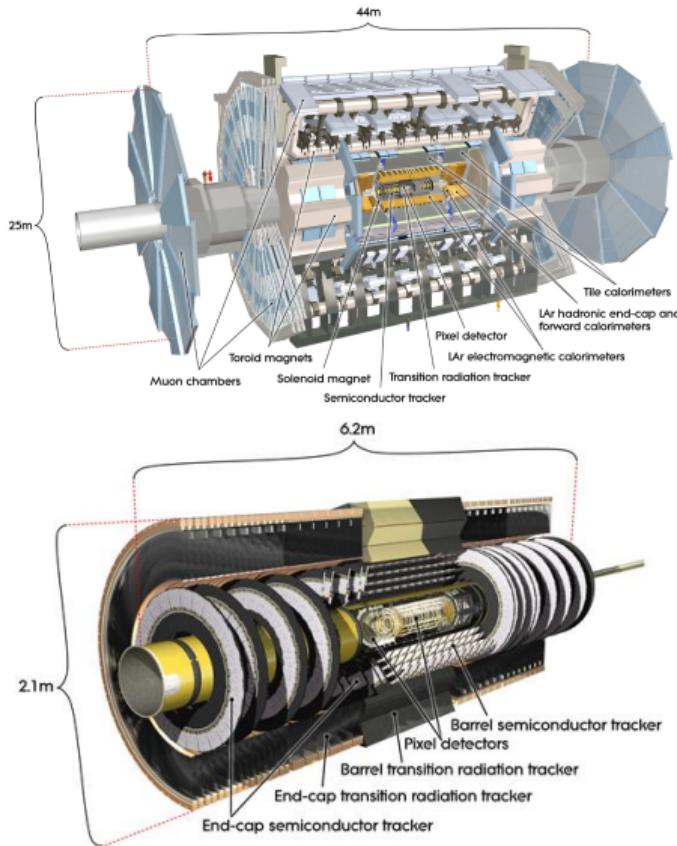
ATLAS & the Inner Detector

ATLAS Detector

- ▶ Inner Detector
- ▶ Calorimeters
- ▶ Muon Spectrometer

Inner Detector

- ▶ Pixel Detector (PIX)
- ▶ Semiconductor Tracker (SCT)
- ▶ Transition Radiation Tracker (TRT)



Background

ATLAS & the Inner Detector
HL-LHC & ITk
ITk Design and Readout

Lab Testing of Hybrid Chips

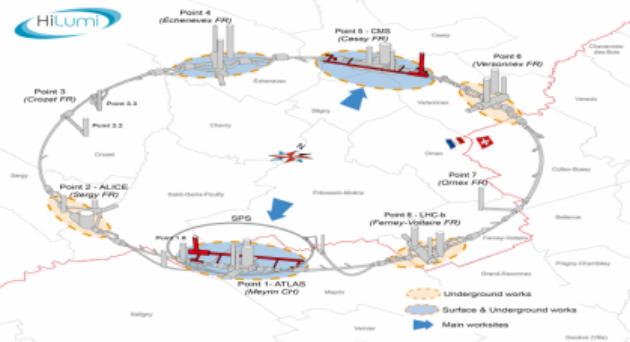
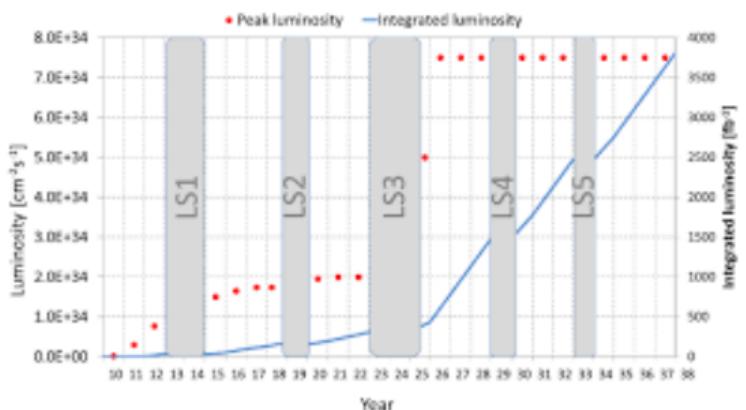
Testing Setup
Progress & Goals

Acknowledgements

High Luminosity LHC & ITk Upgrades

3x increase in instantaneous luminosity!

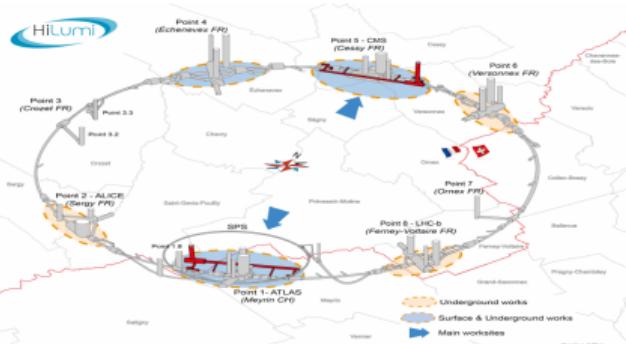
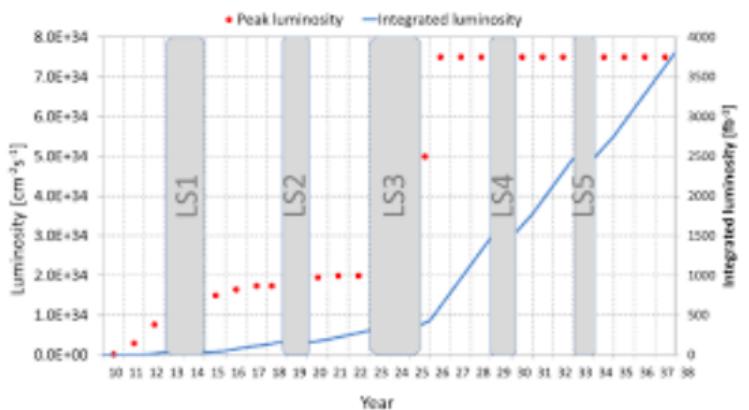
$$\blacktriangleright L = 2 \text{e}73 \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 7 \text{e}73 \text{ fb}^{-1} \text{ s}^{-1}$$



High Luminosity LHC & ITk Upgrades

3x increase in instantaneous luminosity!

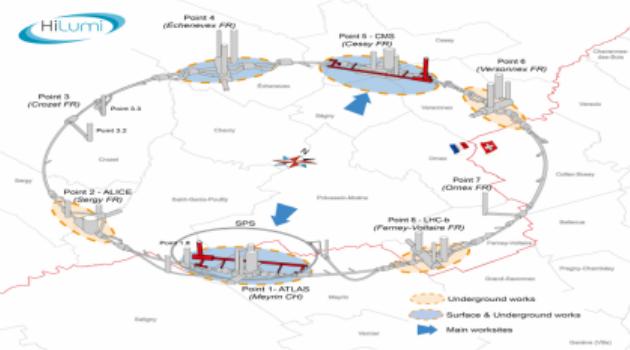
- $L = 2 \times 10^{33} \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 7 \times 10^{33} \text{ fb}^{-1} \text{ s}^{-1}$
- More particles, more problems



High Luminosity LHC & ITk Upgrades

3x increase in instantaneous luminosity!

$$\blacktriangleright L = 2\text{e}73 \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 7\text{e}73 \text{ fb}^{-1} \text{ s}^{-1}$$



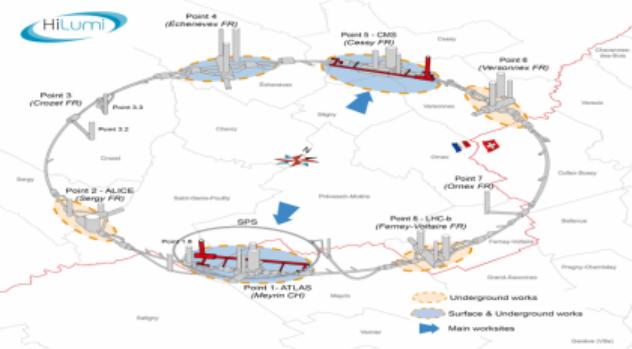
The inner detector has insufficient:

- ▶ radiation hardness
- ▶ granularity
- ▶ readout bandwidth
- ▶ trigger readout

High Luminosity LHC & ITk Upgrades

3x increase in instantaneous luminosity!

$$\blacktriangleright L = 2e73 \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 7e73 \text{ fb}^{-1} \text{ s}^{-1}$$



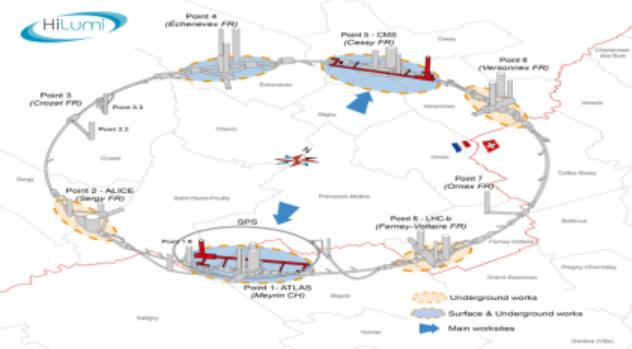
The inner detector has insufficient:

- radiation hardness: HL-LHC will deliver 4000 fb^{-1} integrated luminosity, ID PIX is designed for 400 fb^{-1} , ID SCT for 700 fb^{-1} , IBL for 800 fb^{-1}

High Luminosity LHC & ITk Upgrades

3x increase in instantaneous luminosity!

$$\blacktriangleright L = 2e73 \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 7e73 \text{ fb}^{-1} \text{ s}^{-1}$$



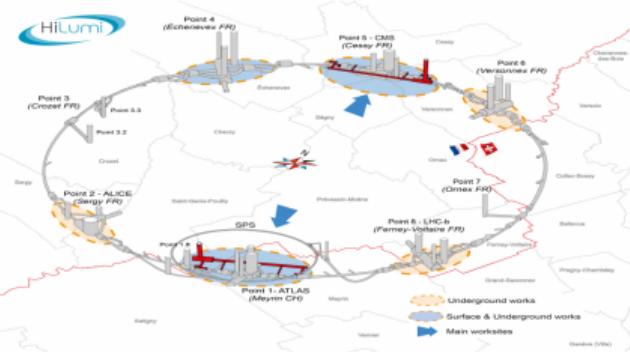
The inner detector has insufficient:

- granularity: Increasing fluence means higher granularity is needed to maintain performance; compensate for intrinsic dead time

High Luminosity LHC & ITk Upgrades

3x increase in instantaneous luminosity!

- ▶ $L = 2e73 \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 7e73 \text{ fb}^{-1} \text{ s}^{-1}$
- ▶ More particles, more problems



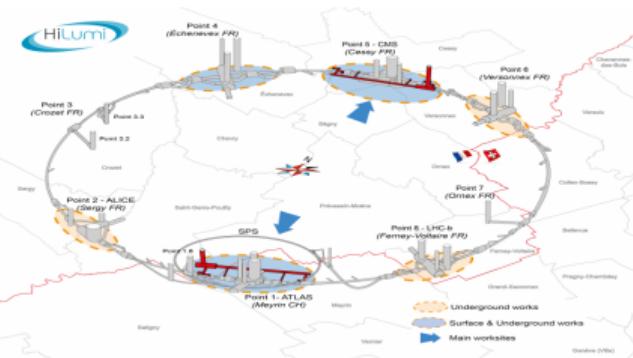
The inner detector has insufficient:

- ▶ readout bandwidth: HL-LHC will roughly quadruple ID designed bandwidth saturation

High Luminosity LHC & ITk Upgrades

x10 increase in instantaneous luminosity!

- $L = 1e73 \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 1e74 \text{ fb}^{-1} \text{ s}^{-1}$
- More particles, more problems



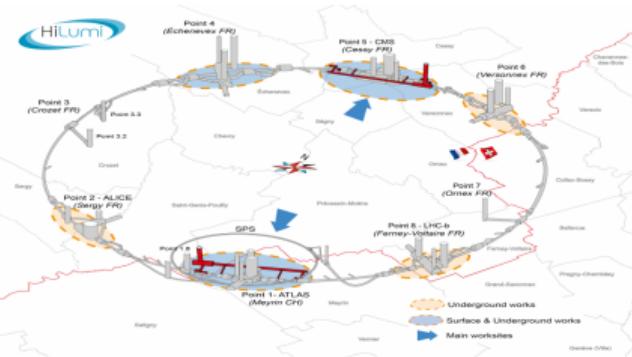
The inner detector has insufficient:

- trigger readout: readout chain must accomodate much higher hardware (level 1) trigger rate, and ideally include tracking info

High Luminosity LHC & ITk Upgrades

x10 increase in instantaneous luminosity!

- $L = 1e73 \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 1e74 \text{ fb}^{-1} \text{ s}^{-1}$
- More particles, more problems



Goal of ITk:

Same or better performance than ID in harsh environment of HL-LHC

Background

ATLAS & the Inner Detector

HL-LHC & ITk

ITk Design and Readout

Lab Testing of Hybrid Chips

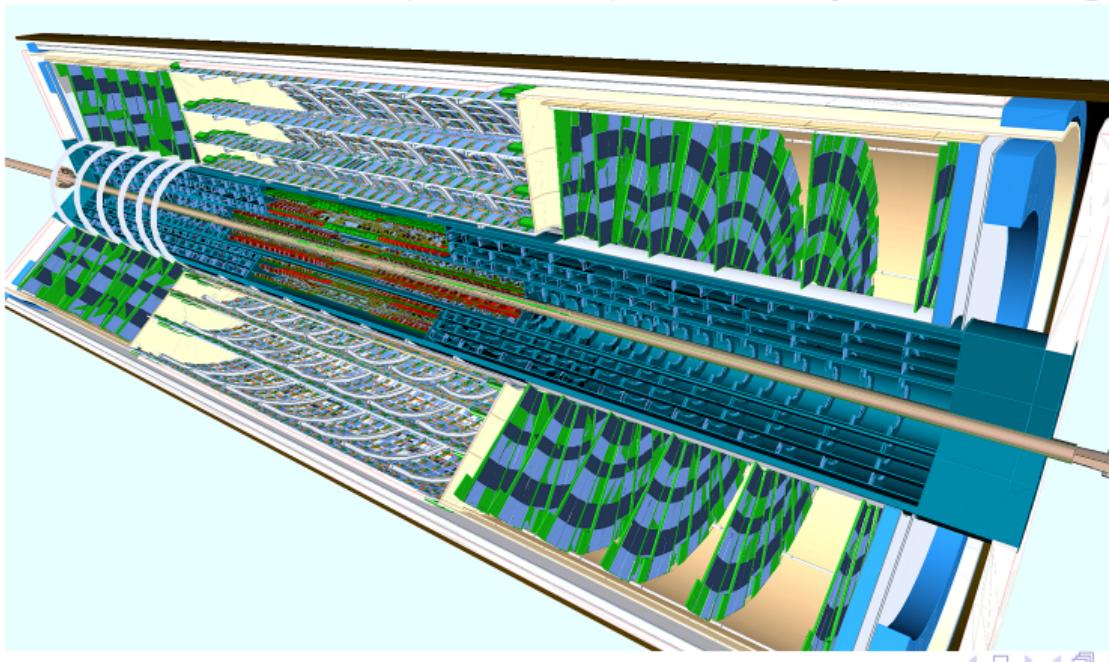
Testing Setup

Progress & Goals

Acknowledgements

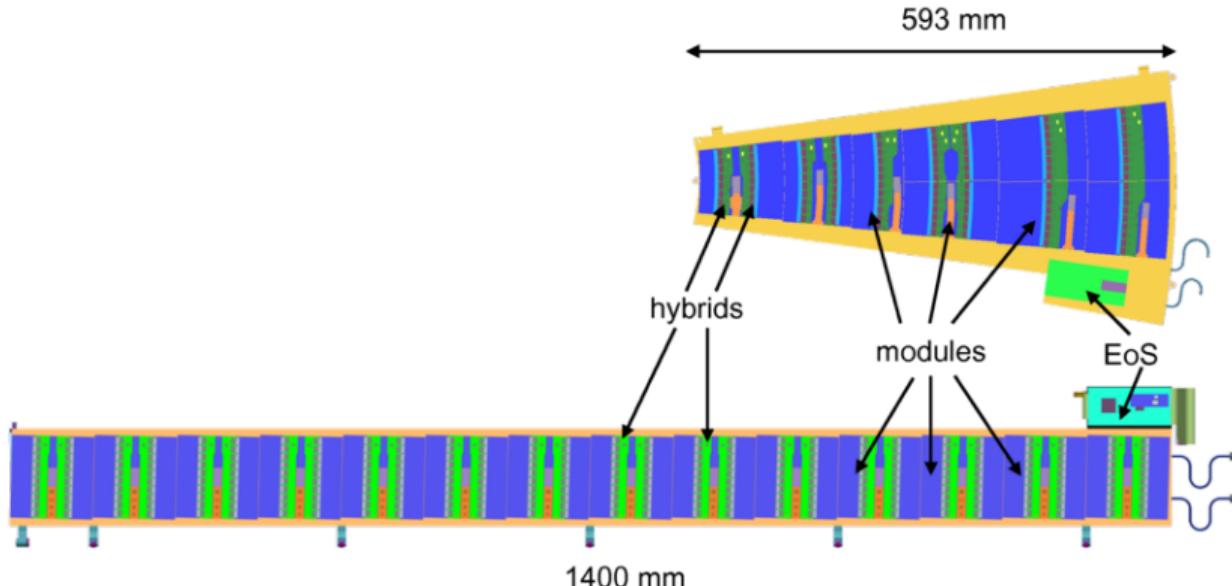
ITk design

- ▶ Pixel detector: 600M channels (80M in PIX): 5 barrel layers, encap system
- ▶ Strip detector: 70M channels (6M in SCT): 4 barrel layers, 6 EC rings



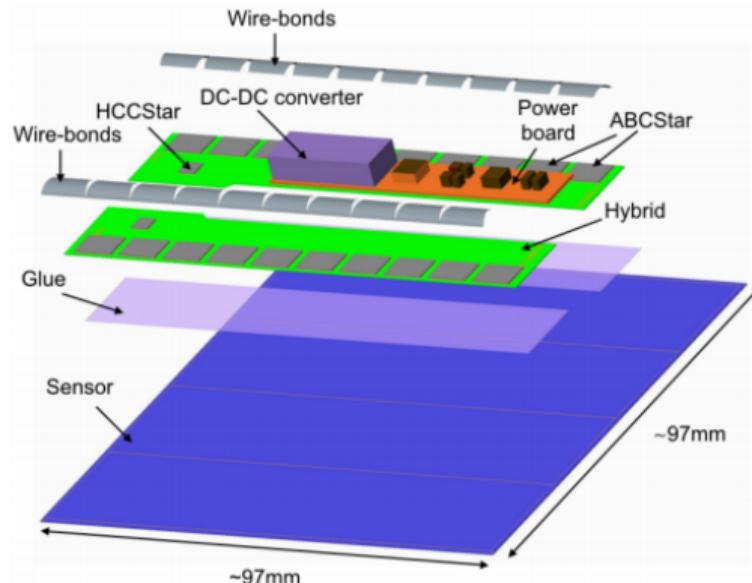
ITk Strip Detector

- ▶ Stave/petal: structure, cooling, power, electrical, etc.
- ▶ Module: silicon sensor + ASIC + readout hybrid + power board
- ▶ Hybrid: Flexible PCB with Hvbrid Controller Chip (HCC) to interface w/ ASIC



ITk Strip Detector Readout

- ▶ sensor → front-end ASIC for signal amplification shaping, & discrimination
- ▶ 10-12 ABC ASICs per hybrid; each ASIC reads out 256 ch
- ▶ Hybrid Controller Chip interfaces the stave/petal service bus & front-end ASICs



Background

ATLAS & the Inner Detector
HL-LHC & ITk
ITk Design and Readout

Lab Testing of Hybrid Chips

Testing Setup
Progress & Goals

Acknowledgements

Background

ATLAS & the Inner Detector
HL-LHC & ITk
ITk Design and Readout

Lab Testing of Hybrid Chips

Testing Setup
Progress & Goals

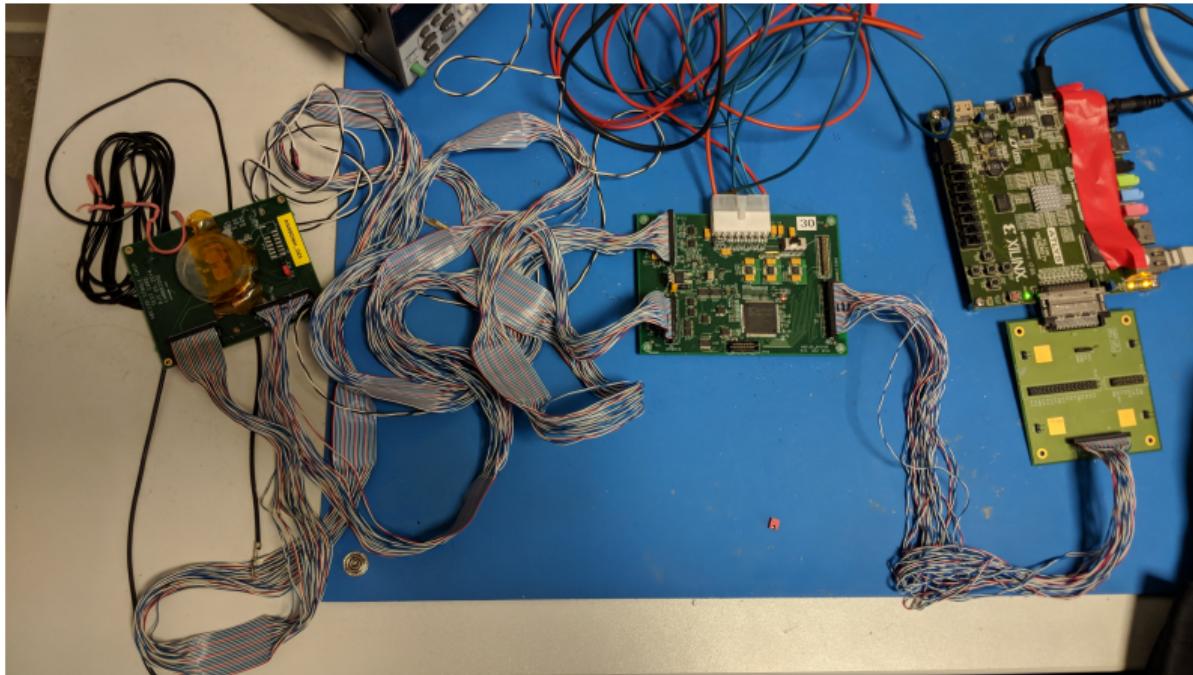
Acknowledgements

Our Setup



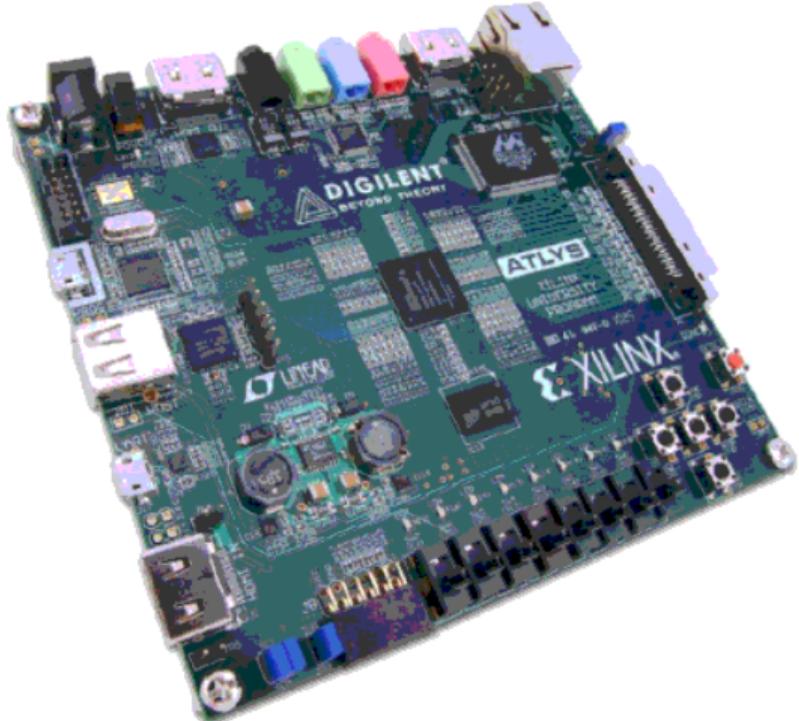
Simple but elegant.

Current DAQ Readout Chain



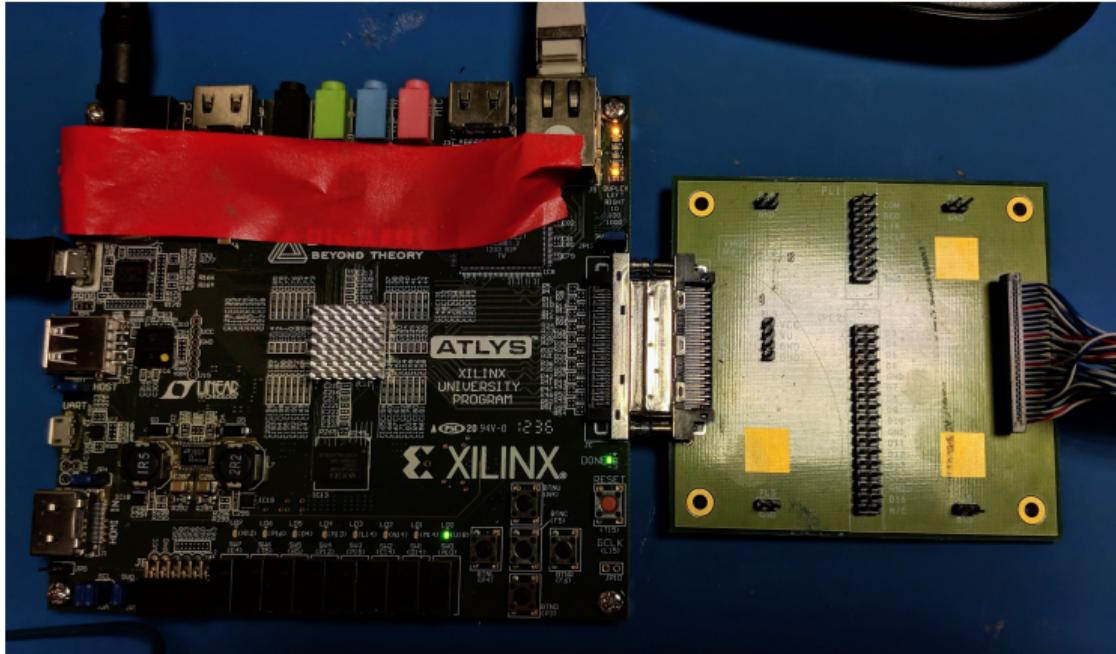
A look at the fully assembled single chip readout chain, ending in the ABC130 prototype test board.

ATLYS Board



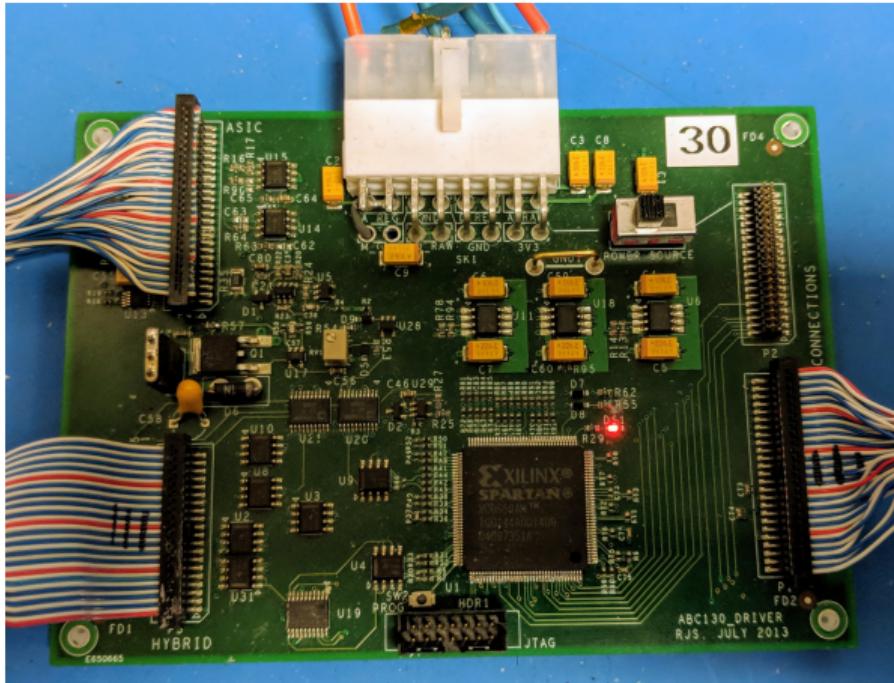
ATLYS is a low cost, widely available board that supports single chip, hybrid, and module tests.

Interface Connection



The ATLYS board is connected to its interface board, VMOD-IB.

Driver Board



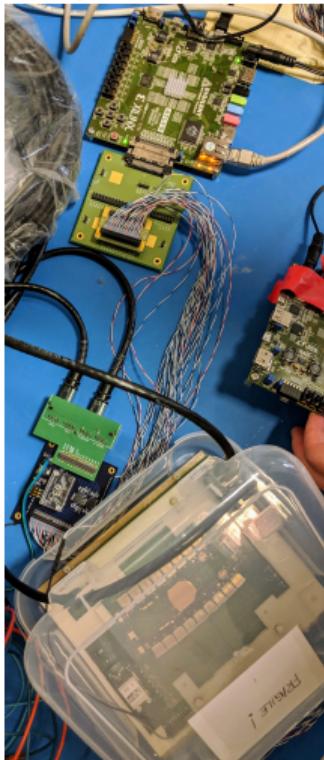
Orientation of the power,
ABC130, and ATLYS
connections.

ABC130 Single Chip Test Card



Test card, with connection to the driver board.

The Hybrid Setup



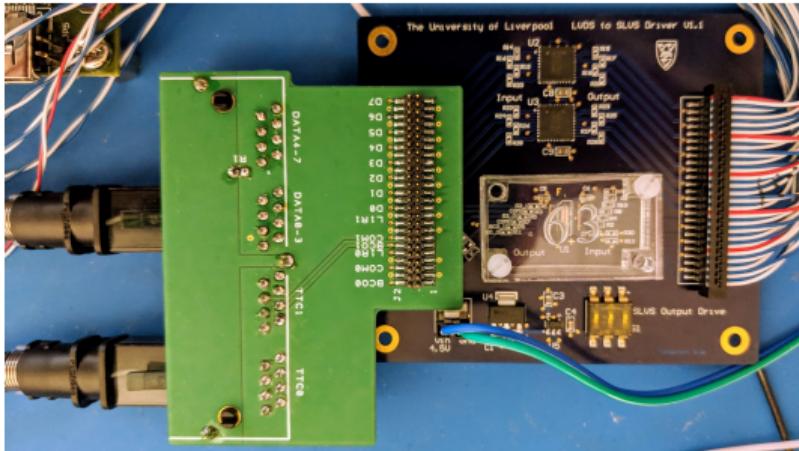
The fully assembled readout chain for the hybrid chip.

The Hybrid's ATLYS



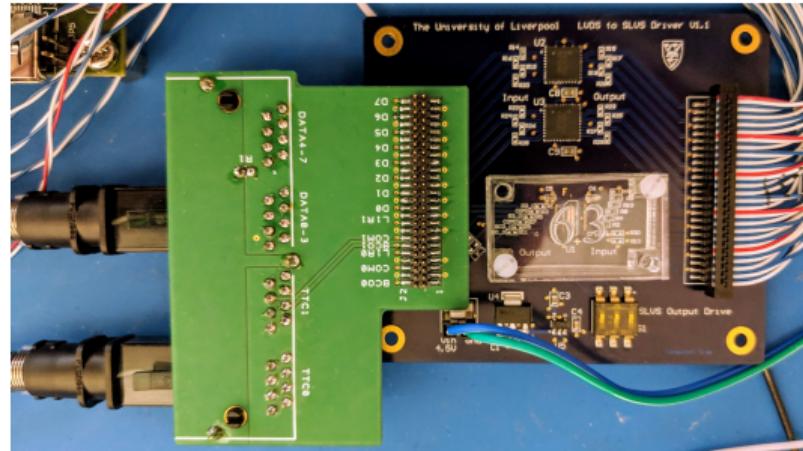
Another VMOD-IB connection to another ATLYS.

The Hybrid Driver Board



LVDS to SLVS driver board.

The Actual Hybrid Chip



The hybrid chip.

Background

ATLAS & the Inner Detector
HL-LHC & ITk
ITk Design and Readout

Lab Testing of Hybrid Chips

Testing Setup
Progress & Goals

Acknowledgements

Progress & Obstacles

Progress

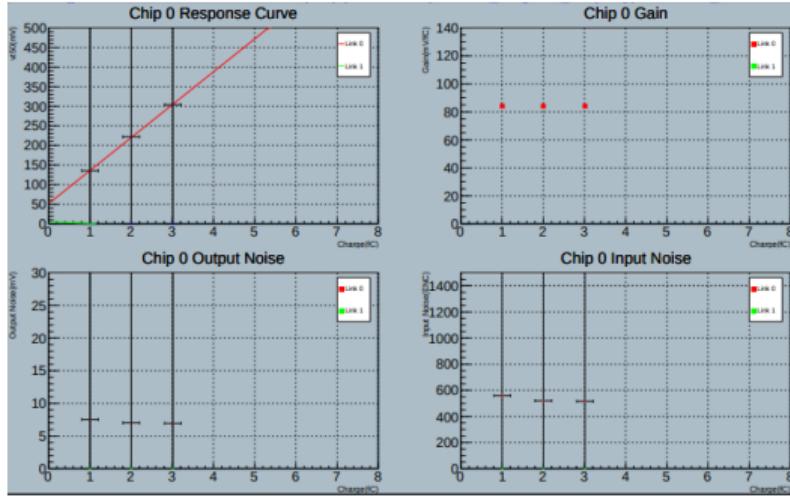
- ▶ Able to run correct versions of NI-VISA, NI-DAQMX Base, and NI-488.2 and communicate with devices
- ▶ Able to use the ITSDAQ software to run tests on actual chips
- ▶ Resolved 3-point voltage gain problem

Obstacles

- ▶ The cabling connections to both the power supply and the ABC chips have been very sensitive
- ▶ Firmware issues with the on the ATLYS connected to the hybrid chip

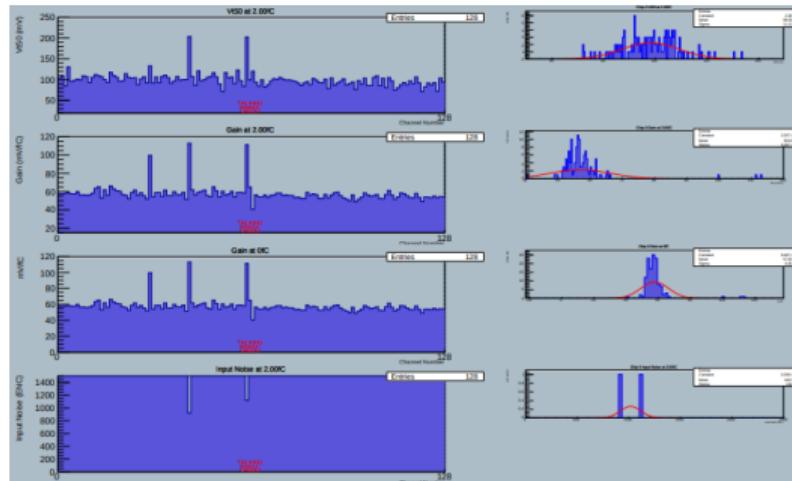
3 Point Gain Not Working

Measures gain & noise at 3 power supply currents



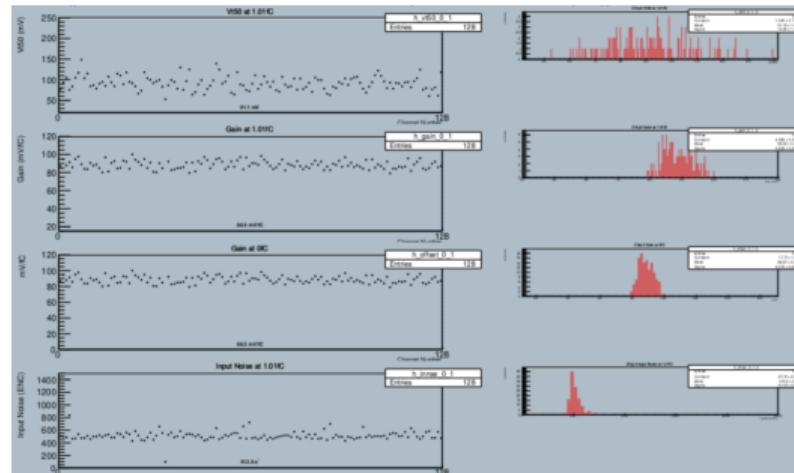
3 Point Gain Not Working

Measures gain & noise at 3 power supply currents



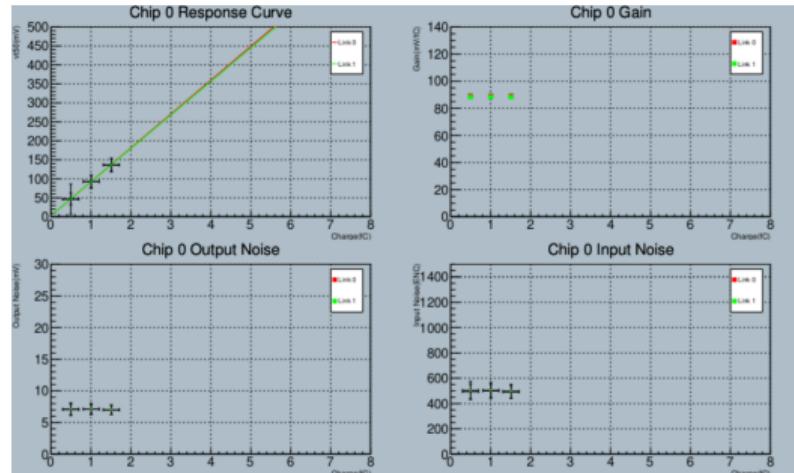
3 Point Gain Working

Measures gain & noise at 3 power supply currents



3 Point Gain Working

Measures gain & noise at 3 power supply currents



Goals

- ▶ Resolve ATLYS hybrid firmware issues
- ▶ Obtain a stable cabling setup
- ▶ Integrate FELIX chip (optical, rad-hardened comm protocol drivers) into readout chain

Background

ATLAS & the Inner Detector
HL-LHC & ITk
ITk Design and Readout

Lab Testing of Hybrid Chips

Testing Setup
Progress & Goals

Acknowledgements

Acknowledgements

We would like to acknowledge the University of Michigan Department of Physics, specifically Jean Krisch, Tom Schwarz, and Steven Goldfarb. We would also like to acknowledge the support of the Lounsbery foundation.





www.cern.ch