



# Readout System Enhancements for ATLAS ITk Project

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# Agenda

## Background

ATLAS & the Inner Detector  
HL-LHC & ITk  
ITk Design and Readout

## Lab Testing of Hybrid Chips

Testing Setup  
Progress & Goals

## Acknowledgements

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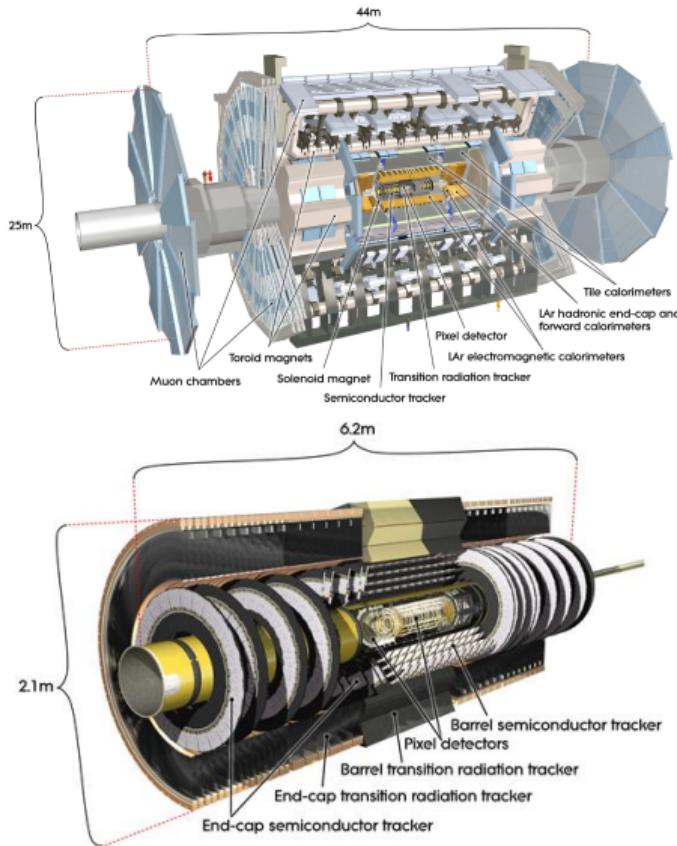
# ATLAS & the Inner Detector

## ATLAS Detector

- ▶ Inner Detector
- ▶ Calorimeters
- ▶ Muon Spectrometer

## Inner Detector

- ▶ Pixel Detector (PIX)
- ▶ Semiconductor Tracker (SCT)
- ▶ Transition Radiation Tracker (TRT)



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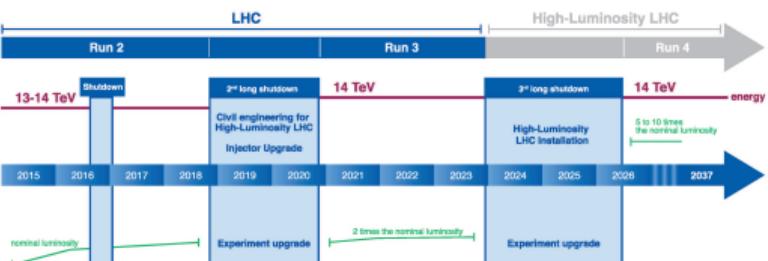
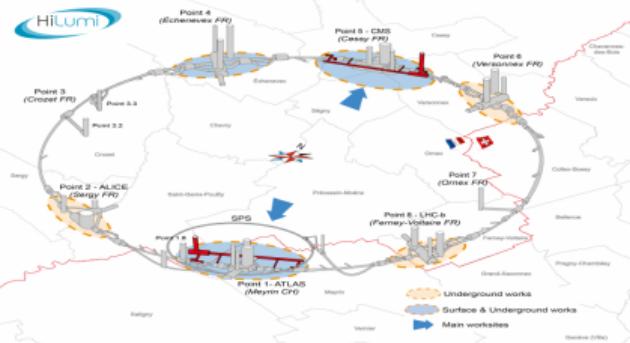
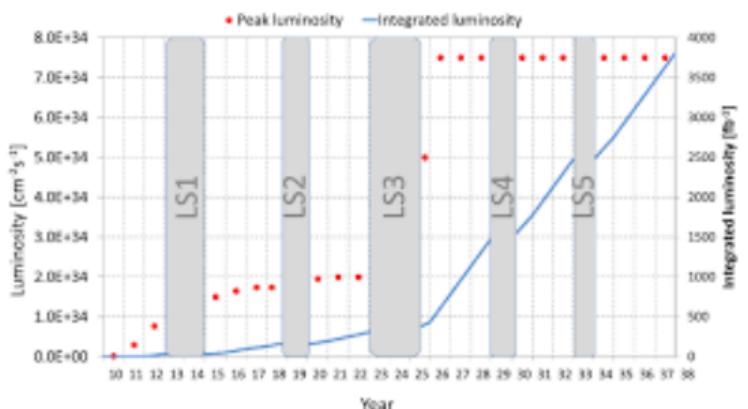
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# High Luminosity LHC & ITk Upgrades

x10 increase in instantaneous luminosity!

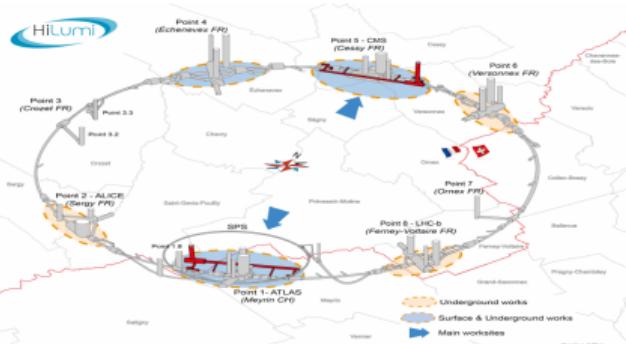
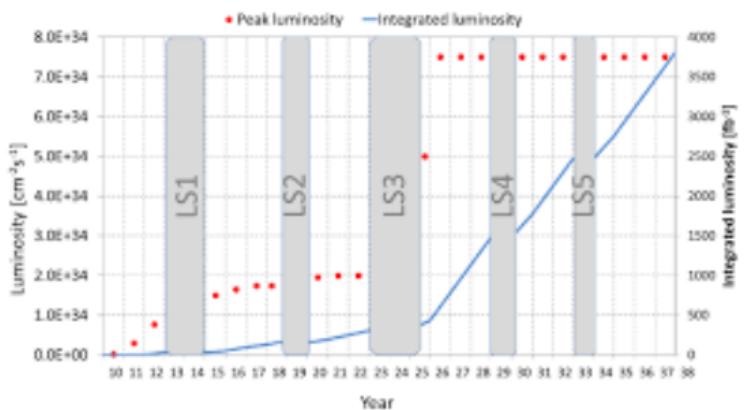
$$\blacktriangleright L = 1\text{e}73 \text{ fb}^{-1} \text{ s}^{-1} \rightarrow L = 1\text{e}74 \text{ fb}^{-1} \text{ s}^{-1}$$



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- More particles, more problems



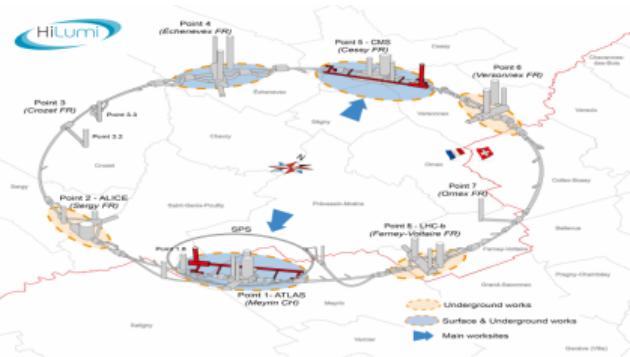
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The inner detector has insufficient:

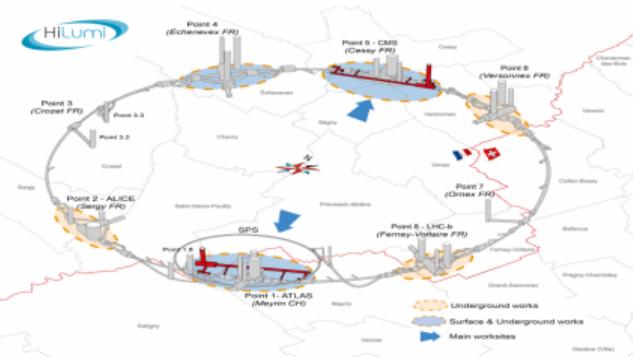
- radiation hardness
- granularity
- readout bandwidth
- trigger readout



# High Luminosity LHC & ITk Upgrades

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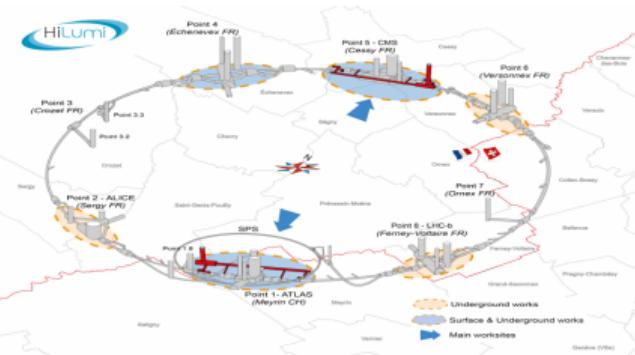
The inner detector has insufficient:

- radiation hardness: HL-LHC will deliver  $4000 \text{ fb}^{-1}$  fluence. ID PIX is designed for  $400 \text{ fb}^{-1}$ , ID SCT for  $700 \text{ fb}^{-1}$ , IBL for  $800 \text{ fb}^{-1}$

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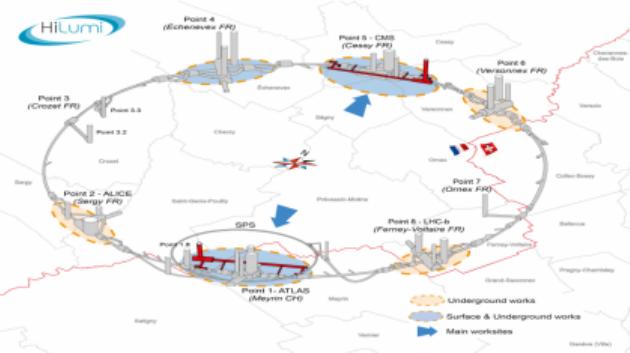
The inner detector has insufficient:

- granularity: Increasing fluence means higher granularity is needed to maintain performance; compensate for intrinsic dead time

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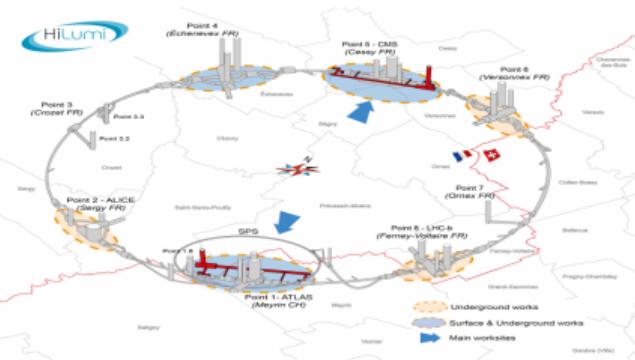
The inner detector has insufficient:

- ▶ readout bandwidth: HL-LHC will roughly quadruple ID designed bandwidth saturation

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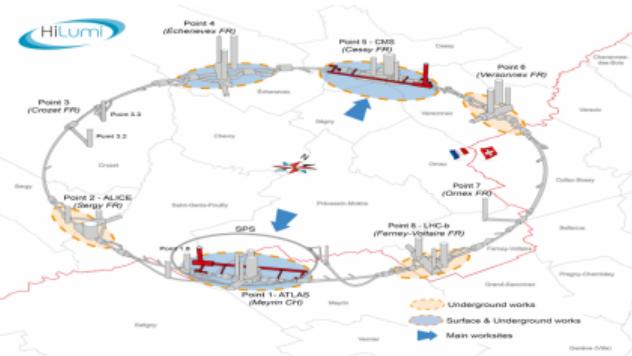
The inner detector has insufficient:

- ▶ trigger readout: readout chain must accomodate much higher hardware (level 1) trigger rate, and ideally include tracking info

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Goal of ITk:

Same or better performance than ID in harsh environment of HL-LHC

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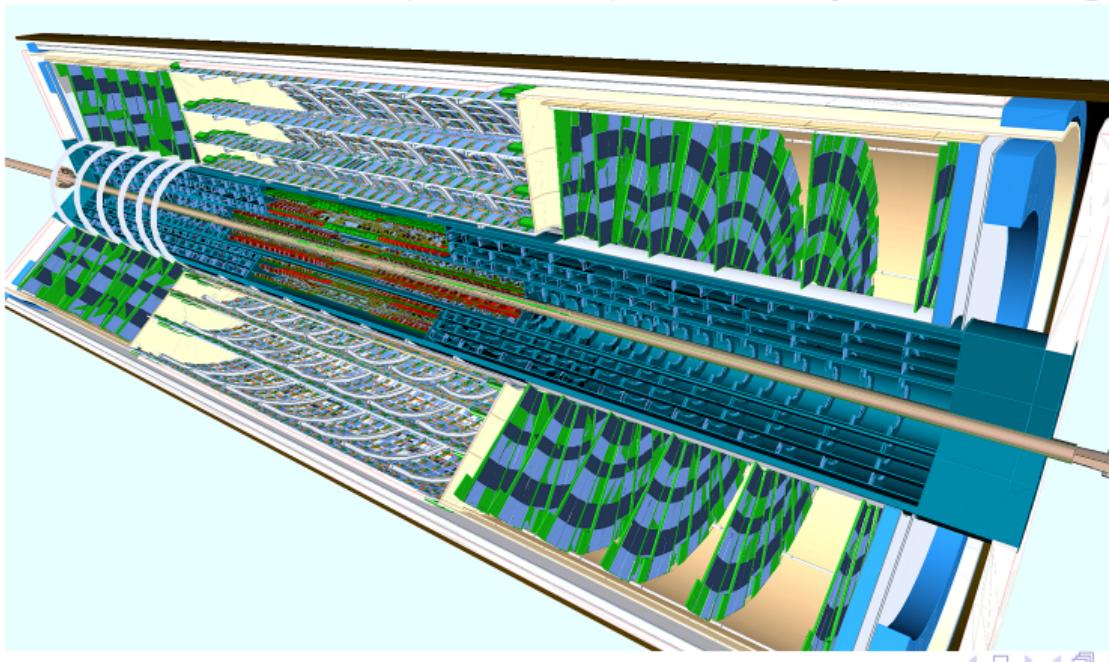
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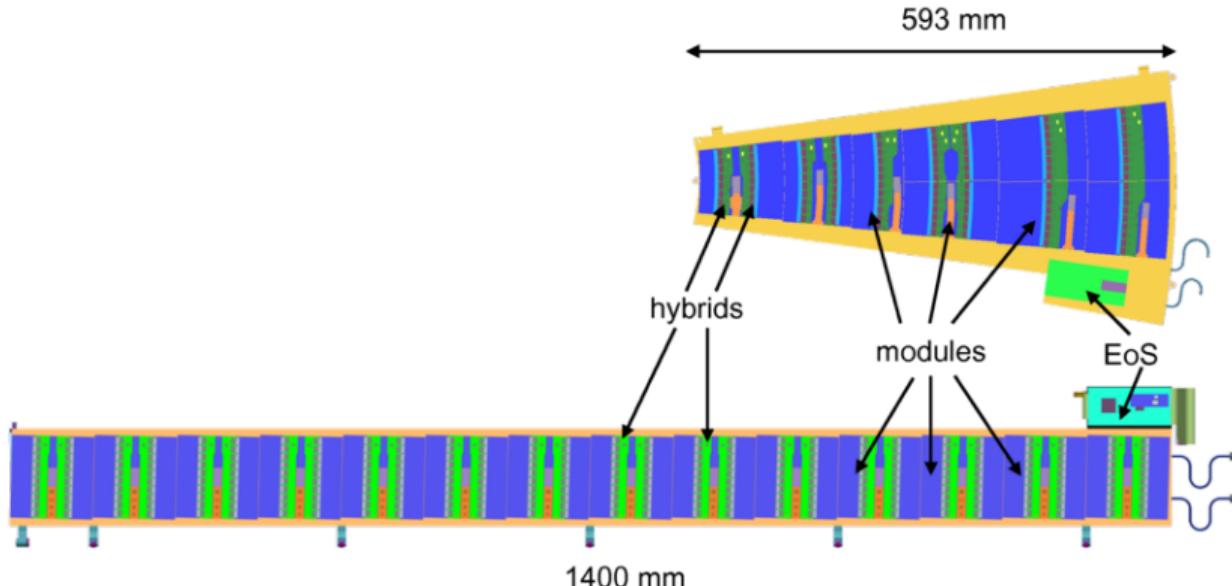
# ITk design

- ▶ Pixel detector: 600M channels (80M in PIX): 5 barrel layers, encap system
- ▶ Strip detector: 70M channels (6M in SCT): 4 barrel layers, 6 EC rings



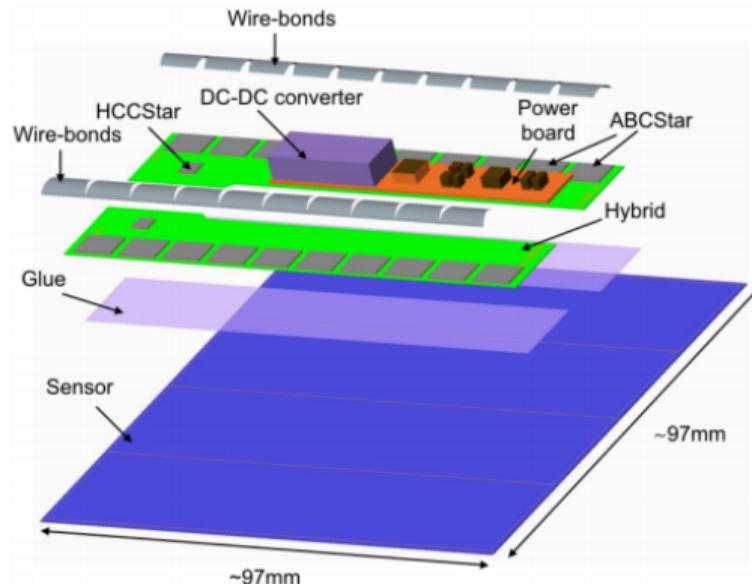
# ITk Strip Detector

- ▶ Stave/petal: structure, cooling, power, electrical, etc.
- ▶ Module: silicon sensor + ASIC + readout hybrid + power board
- ▶ Hybrid: Flexible PCB with Hvbrid Controller Chip (HCC) to interface w/ ASIC



# ITk Strip Detector Readout

- ▶ sensor → front-end ASIC for signal amplification shaping, & discrimination
- ▶ 10-12 ABC ASICs per hybrid; each ASIC reads out 256 ch
- ▶ Hybrid Controller Chip interfaces the stave/petal service bus & front-end ASICs



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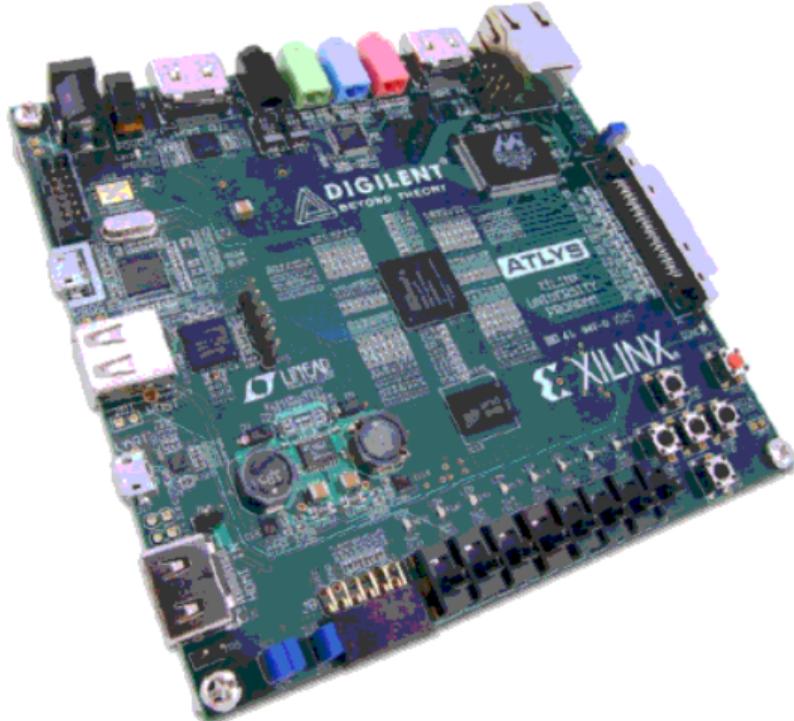
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# Current DAQ Readout Chain

images/readout\_chain.jpg

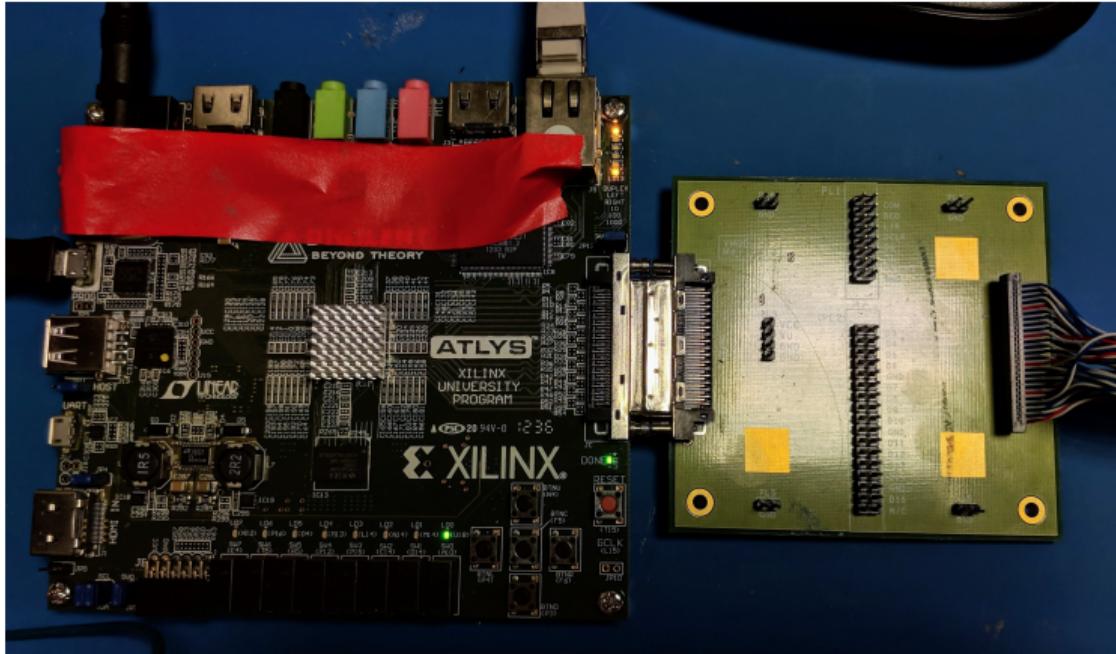
A look at the fully assembled readout chain.

# ATLYS Board



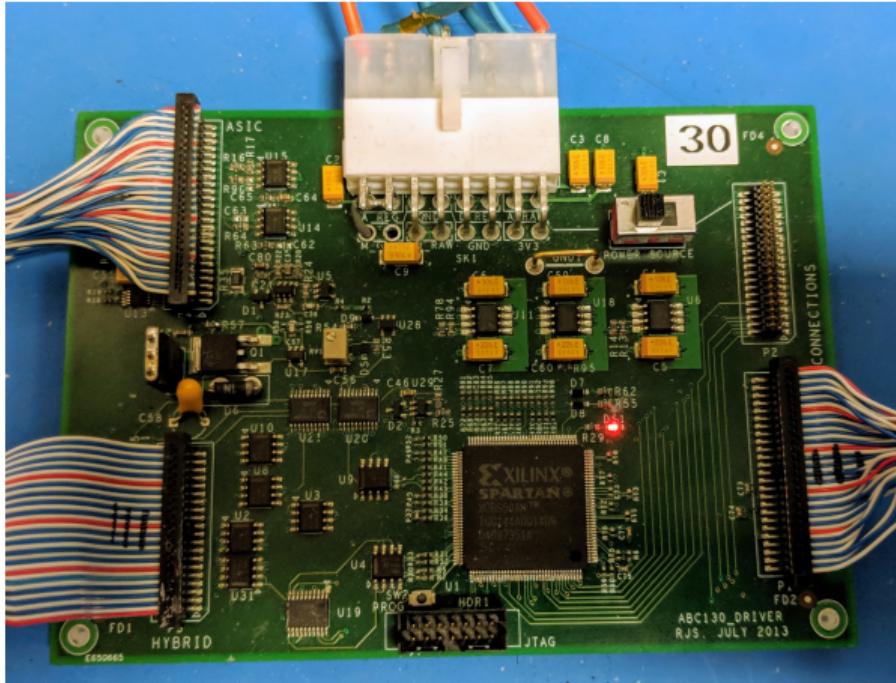
ATLYS is a low cost, widely available board that supports single chip, hybrid, and module tests.

# Interface Connection



The ATLYS board is connected to its interface board, VMOD-IB.

# Hybrid Board



Orientation of the power,  
ABC130, and ATLYS  
connections.

# ABC130 Single Chip Test Card



Test card, with connection to the Hybrid chip.

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# Progress & Obstacles

## Progress

- ▶ Preliminary tests with ITSDAQ software
- ▶ Able to run correct versions of NI-VISA, NI-DAQMX Base, and NI-488.2 and communicate with devices

## Obstacles

- ▶ We accidentally lost a configuration and register assignment file on a formatted Windows SSD.
- ▶ We have a segmentation violation in the GUI of the ITSDAQ software.
- ▶ NI-VISA instrument control software doesn't recognize our power supplies

# Goals

- ▶ Get ITSDAQ working
- ▶ Solve NI-VISA issues and run HV controller through ITSDAQ
- ▶ Integrate FELIX chip (optical, rad-hardened comm protocol drivers) into readout chain

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We would like to acknowledge the University of Michigan Department of Physics, specifically Jean Krisch, Tom Schwarz, and Steven Goldfarb. We would also like to acknowledge the support of the Lounsbury foundation.





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