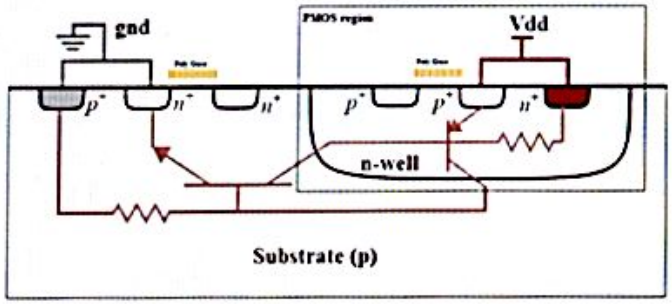
What is Latchup (CMOS)?

According to Wikipedia:

"A **latch-up** is a type of short circuit which can occur in an improperly designed integrated circuit (IC). More specifically, it is the inadvertent creation of a low-impedance path between the power supply rails of a MOSFET circuit, triggering a parasitic structure ....."



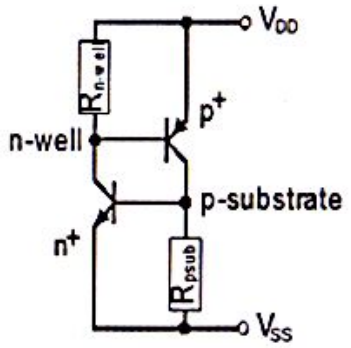
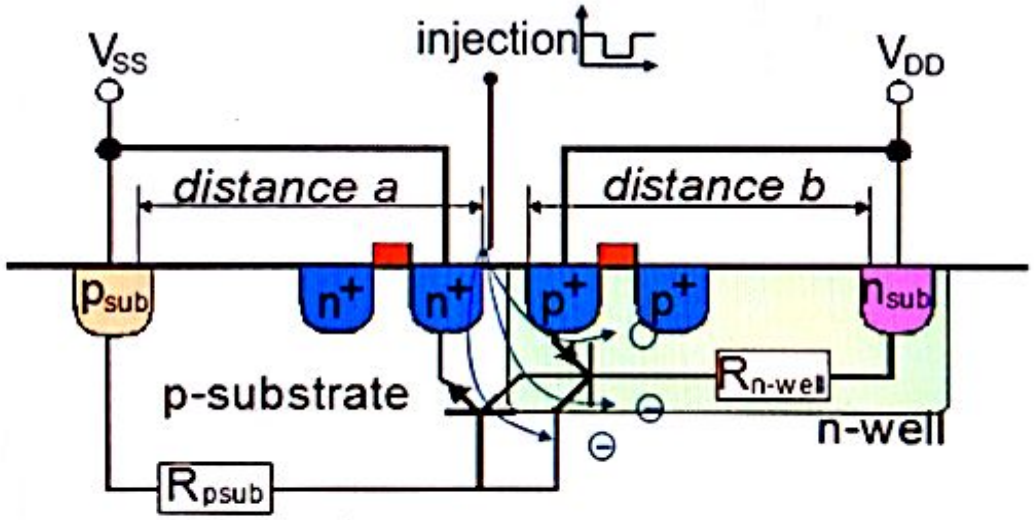
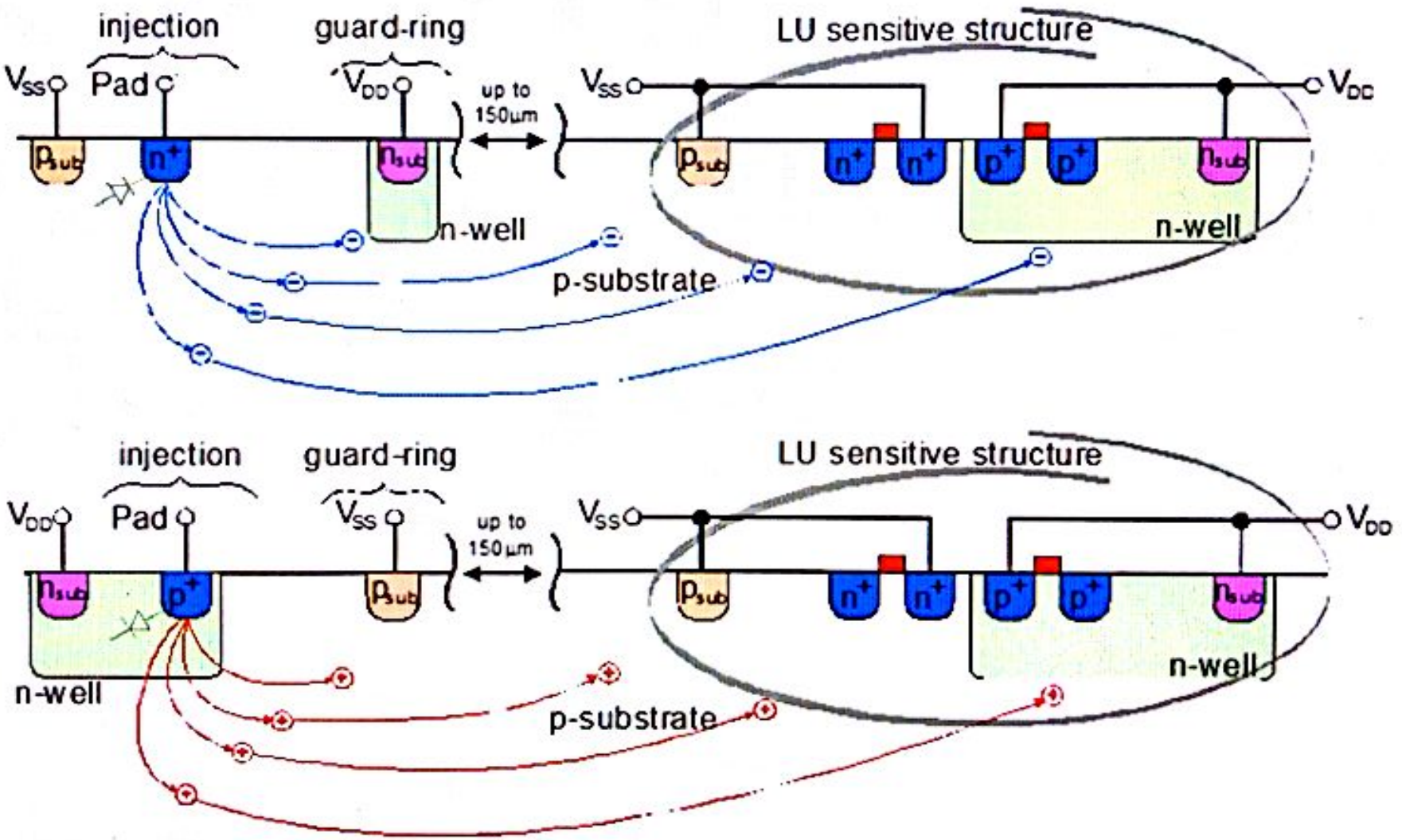


Fig: The Parasitic Thyristor

Internal LU



External LU



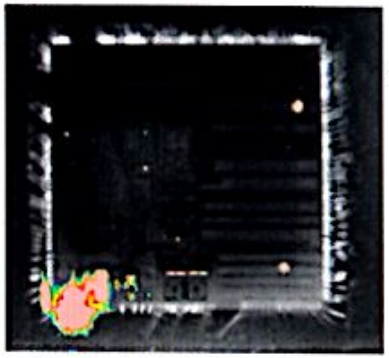
What Causes Latchup?

- Events during turning on and off (overshoot, undershoot)
- Interfering pulses
- Signal-reflection at mismatched interfaces
- Long metal lines work as inductances
- Improper power on sequencing (e.g. signals before supply turning on)
- SEL (high energy photons/α particles/cosmic rays)
- Transient spikes exceeding the bias voltage

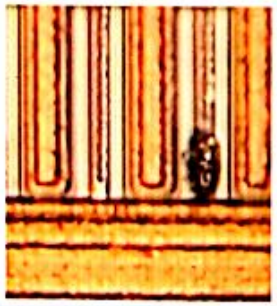
Why do we need to test for Latchup?

- Physical damage to the active components & IC interconnects
- Leads to very high power consumption
- External power supply may break down
- Reliable operation of the IC & the system cannot be guaranteed

Consequences of Latch Up



>70mA current



Damaged interconnect

Damaged junction

Strategy to prevent LU

- Prevention measures at technology development
- Rules for circuit design & layout (e.g. Guard rings)
- Physical verification methodology targeting LU
- **LU testing & detection at IC qualification (DFT + Testing)**
- Application notes for customers e.g. For power sequencing

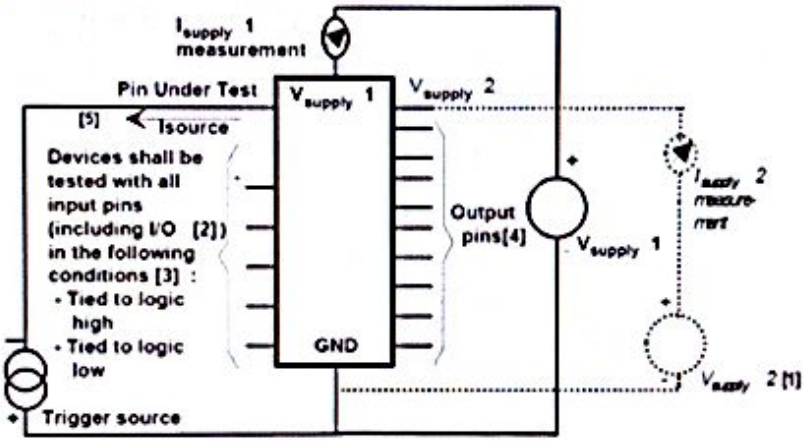
JEDEC LU Testing Standard : EIA/JESD78

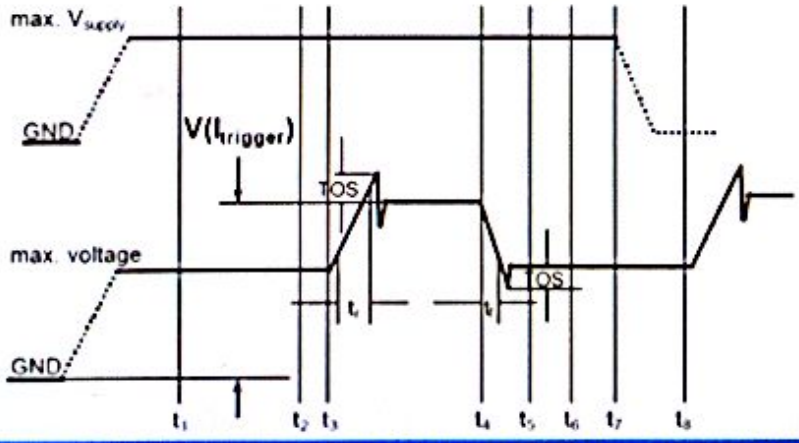
class	test type	untested pins	temp	Vsupply	test conditions	failure criteria
I	I-test	max logic high	room temp	max operating voltage	± 100 mA	
		max logic low				1.4 x Inom
	over-voltage test	max logic high			1.5 x max Vsupply	
		max logic low				
II	I-test	max logic high	max ambient operating temperature	max operating voltage	± 100 mA	
		max logic low				1.4 x Inom
	over-voltage test	max logic high			1.5 x max Vsupply	
		max logic low				

If Inom <=25mA then Inom+10mA

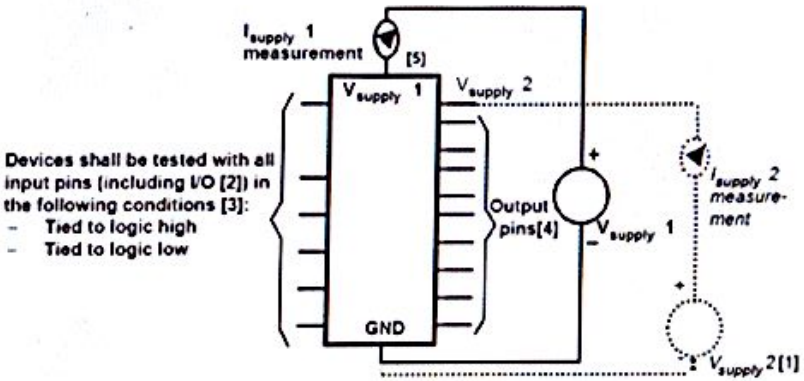
If Inom <=25mA then Inom+10mA

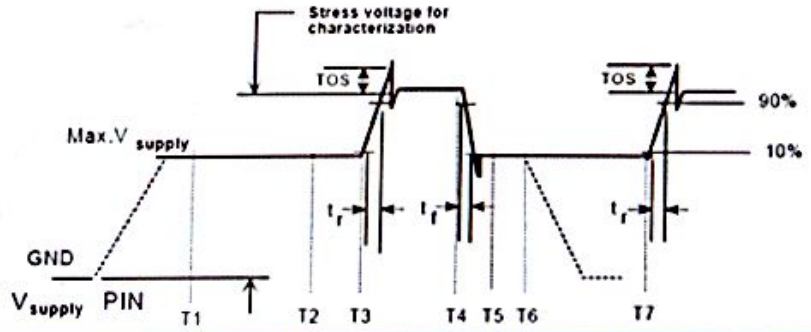
Current(I) Test: Setup & Waveforms



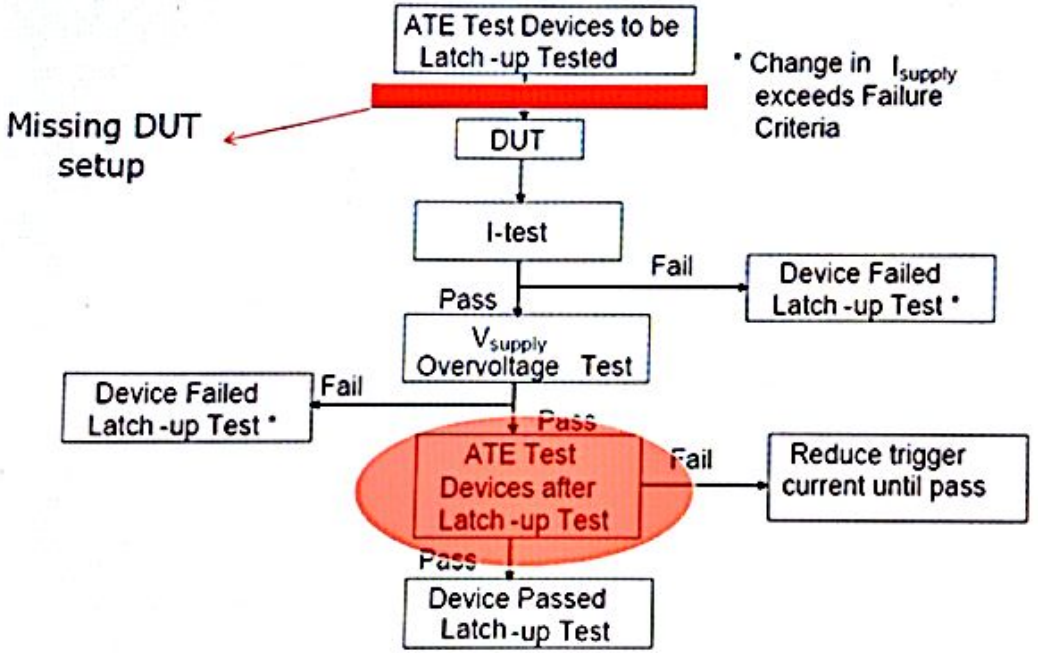


Over Voltage Test: Setup & Waveforms





LU TEST FLOW



DUT setup for LU

- Device should be in power down mode
- All power supplies should be available and proper power sequence should be applied
- Possibility to inject 100mA into IO/O diffusion & current should flow into the substrate
- Worst case : IO/O pins are tri-stated/high Z
- If some pins cannot be tri-stated, these have to be documented & device should be tested by putting these pins to logic high/low
- State of device should not change during application of stress

Strategy for LU Test Mode

- Have a dedicated pin for power down mode/LU test mode
- Provide a simple 0/1 to the pin to activate the LU test mode
- If not possible to have a dedicated pin simple / complex vectoring is required for power down mode & tri-stating IO's

Click to add notes

Issues for LU Testing

- Power down pin is often not available
- Vectoring is far too complex for the LU tester
- Other limitations for LU tester
- No feedback if the device is in the correct mode
- On chip LDOs complicate the situation
- Many IO pins do not go to tri-state
- Large currents > 100mA on some supplies
- SiP with multiple dies & supply levels makes situation worse (e.g. XG726G (DBB + PMU + LP DRAM)

LU Tester Limitations

- Only 5 supply channels available
- No time dependant stepping (PMU => core)
- Vector file size limited to 256kb
- Only 1 level for a high can be supported for the vectors
- No loops possible, no repetition factor in the vector file is allowed
- Only one (internal) clock possible in tester from 1.2kHz up to 20MHz with fixed values (special timing info useless)

LU test mode

- Implement a LU-test mode in the design.
- This LU-test mode may be entered by simple programming of the chip via the JTAG interface.
- Keep the pattern to less than 256k.
- LU-mode has to be checked on functional Tester before deliver to Reliability Test Center.
- If the device goes into the LU-mode it has to switch one pin to high.

Configuration of digital blocks

- All power supplies should be available
- All power switches (both VDD/VSS) should be conducting i.e. circuits should be supplied
- All IO/I/O pins should be tri-stated
- Digital blocks should have minimum activity to keep currents low enough to detect a LU event.

Configuration of analog blocks

- All power supplies should be available
- All power switches (both VDD/VSS) should be conducting i.e. circuits should be supplied
- All analog IO/I/O pins should be tri-stated if possible. If not possible they have to be documented
- Analog blocks should have minimum activity to keep currents low enough to detect a LU event
- Pins which have to support current injections higher than JEDEC (100mA) have to be specified
- Pins which should not be tested e.g. Coils with one end connected to GND or reference outputs e.g. VREF (cap to ground)have to be specified

Configuration of power supply pins

- All power supplies should be available
- All power switches (both VDD/VSS) should be conducting i.e. circuits should be supplied
- The voltage level at the supply during the I test should be the highest operating voltage (Vmax)

Configuration of LDO's

- All LDO outputs should be available & should be turned on in proper sequence
- All LDO outputs should programmed to the highest possible operating voltages (Vmax)
- For all external LDO outputs, list of passive components (e.g. Caps) & their values should be specified for preparation of the LU board.
- The LDO outputs may be skipped from overvoltage LU test if they have a capacitor to ground in application
- For internal LDO's there should be a possibility to check if they are programmed to the highest voltages

Summary

- LU testing & DF(LU)T is a very important part of IC design
- Most of the LU testing issues can be overcome by synergy between designer engineer, DFT engineer, LU expert & the LU test engineer
- "Prevention is better than cure"
- Future challenges: SiP with multiple dies (DBB, PMU, connectivity, memory...)

Click to add notes

References

- http://en.wikipedia.org/wiki/Latchup
- EIA/JESD78D : JEDEC LU standard