# Chip-Scale package (CSP)

Table of Contents

[Chip-Scale package (CSP) 1](#_Toc508808456)

**[Types of chip scale packages](#_Toc508808457)** [1](#_Toc508808457)

[Package development 2](#_Toc508808458)

[FCCSP 3](#_Toc508808459)

[General info 3](#_Toc508808460)

[Assembly flow 4](#_Toc508808461)

[Bump type 5](#_Toc508808462)

[Application 6](#_Toc508808463)

[eWLB 6](#_Toc508808464)

[WLCSP 8](#_Toc508808465)

[Encapsulation Provides Increased Reliability and Durability 8](#_Toc508808466)

[Reference 9](#_Toc508808467)

A **chip scale package** or **chip-scale package** (**CSP**) is a type of [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) package.[[1]](https://en.wikipedia.org/wiki/Chip-scale_package#cite_note-1)

Originally, CSP was the acronym for *chip-size packaging.* Since only a few packages are chip size, the meaning of the acronym was adapted to *chip-scale packaging*. According to [IPC](https://en.wikipedia.org/wiki/IPC_(electronics))’s standard J-STD-012, *Implementation of Flip Chip and Chip Scale Technology*, in order to qualify as chip scale, the package must have an area no greater than 1.2 times that of the [die](https://en.wikipedia.org/wiki/Die_(integrated_circuit)) and it must be a single-die, direct surface mountable package. Another criterion that is often applied to qualify these packages as CSPs is their ball pitch should be no more than 1 mm.

The die may be mounted on an [interposer](https://en.wikipedia.org/wiki/Interposer) upon which pads or balls are formed, like with [flip chip](https://en.wikipedia.org/wiki/Flip_chip) [ball grid array](https://en.wikipedia.org/wiki/Ball_grid_array) (BGA) packaging, or the pads may be etched or printed directly onto the [silicon wafer](https://en.wikipedia.org/wiki/Silicon_wafer), resulting in a package very close to the size of the silicon die: such a package is called a [wafer-level package](https://en.wikipedia.org/wiki/Wafer-level_packaging) (WLP) or a wafer-level chip-scale package (WL-CSP). WL-CSP had been in development since 1990s, and several companies begun volume production in early 2000, such as [Advanced Semiconductor Engineering (ASE)](https://en.wikipedia.org/wiki/ASE_Group)

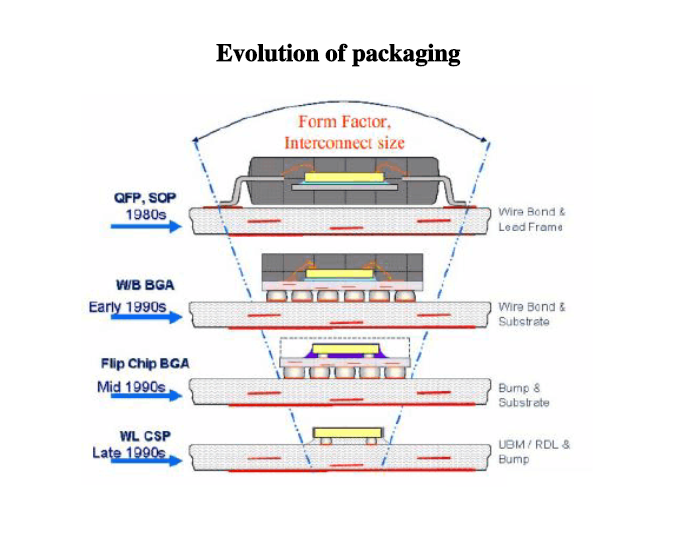
## **Types of chip scale packages**

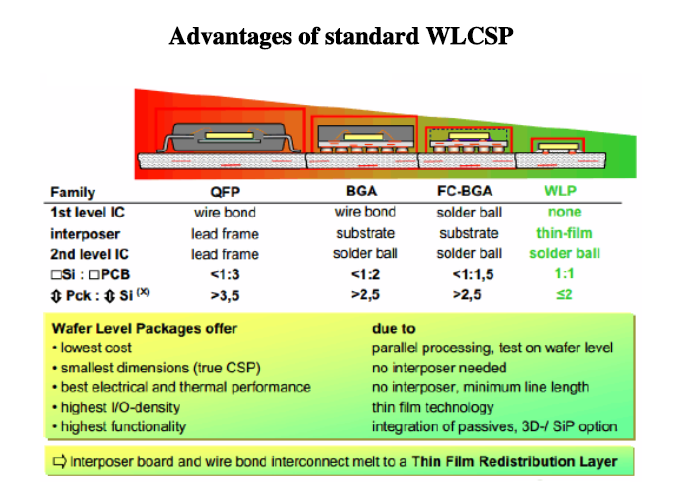
Chip scale packages can be classified into the following groups:

1. Customized leadframe-based CSP (LFCSP)
2. Flexible substrate-based CSP
3. Flip-chip CSP (FCCSP)
4. Rigid substrate-based CSP
5. Wafer-level redistribution CSP (WL-CSP)

## Package development

Below diagram shows how package technology develop to support populating more bump/ball with package size shrinking, also consider thermal dissipation, IO fan out, package reliability…etc.



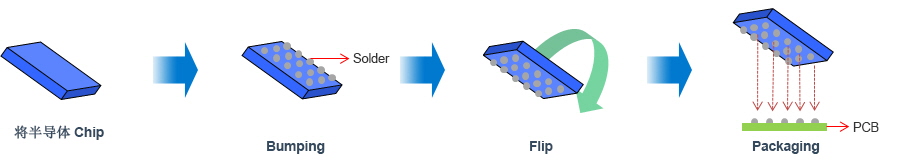


## FCCSP

**半导体芯片不是通过引线键合方式与基板连接，而是在倒装的状态下通过凸点与基板互连，因此而被称为“FCCSP”(Flip Chip Chip Scale Package)。**

### General info

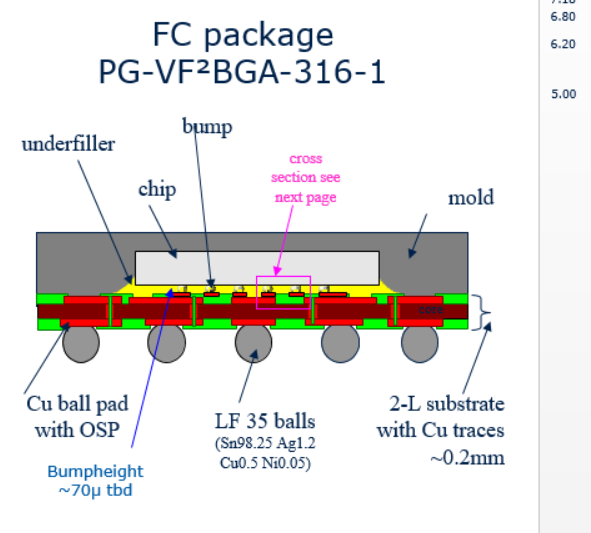
与Wire bonding不同，在半导体(chip)上用Area Array形成Input / Output，翻转(Flip)后，与PCB进行连接。



与采用金线（Gold Wire）键合方式的WBCSP相比，FCCSP的电信号路径更短，生成更多输入/输出端（Input/Output），可适用于高密度半导体。

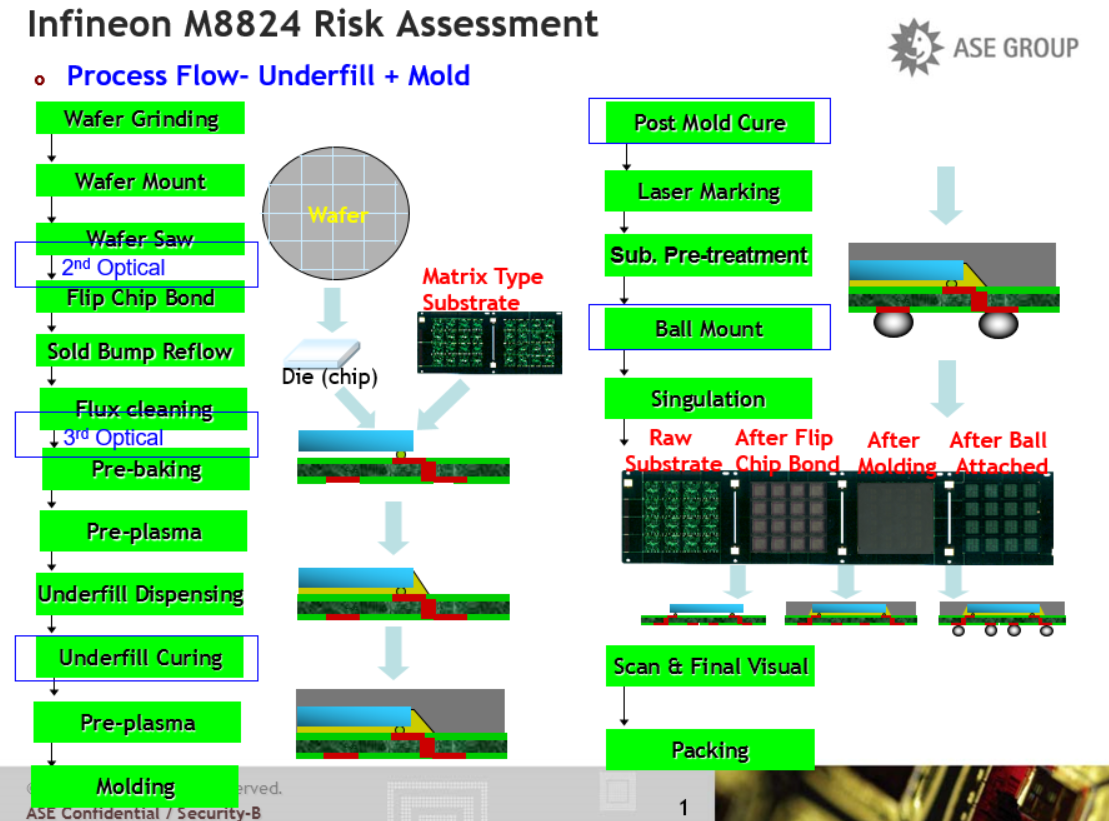


Below is one package example to show detail FCCSP structure.



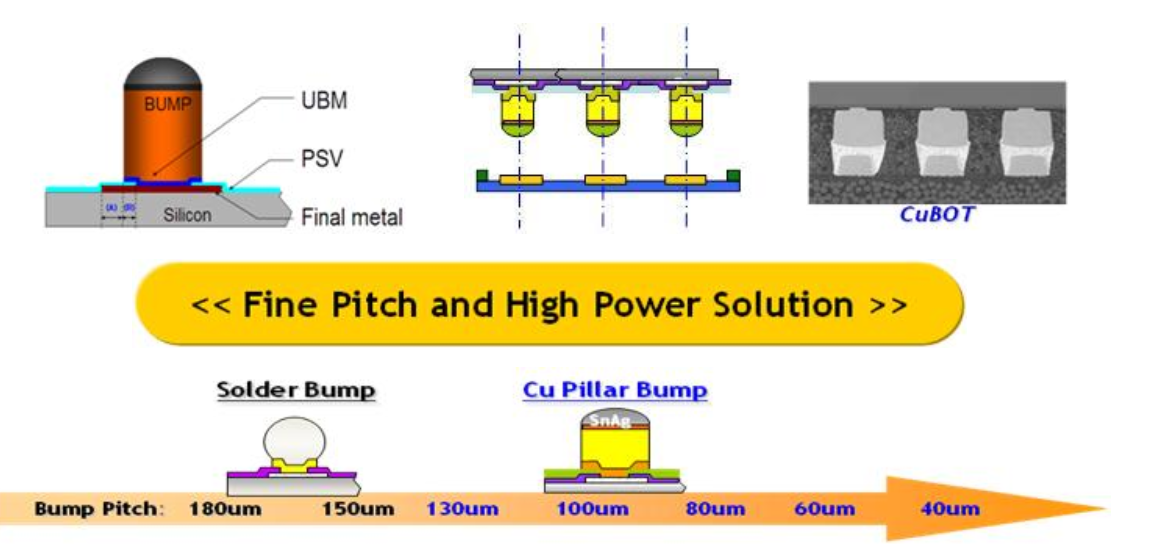
### Assembly flow

Take ASE example FCCSP assembly flow is below:

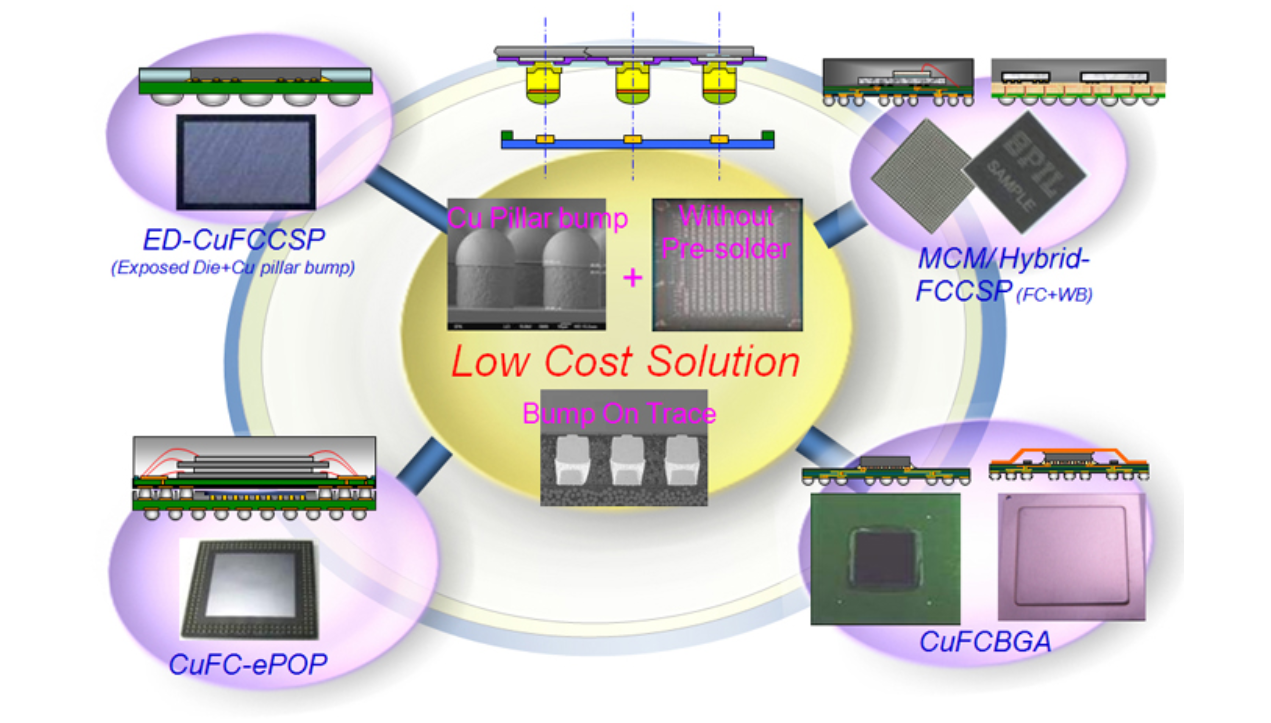


### Bump type

|  |
| --- |
| <http://www.spil.com.tw/technology/?u=4>  Cu Pillar bump is the main stream and BOT( bump on trace) technology is widely used.  **Benefits:** |
| • Lead free solution for RoHS requirement • High current and EM capability(at least 3X better than LF solder bump ) • Fine pitch (high I/O density) with B.O.T. (Bump On Trace) Higher device performance leads to more input/output connections per IC, while miniaturization requires smaller/ thinner packaging, leading to smaller, closer spaced connections. |



### Application



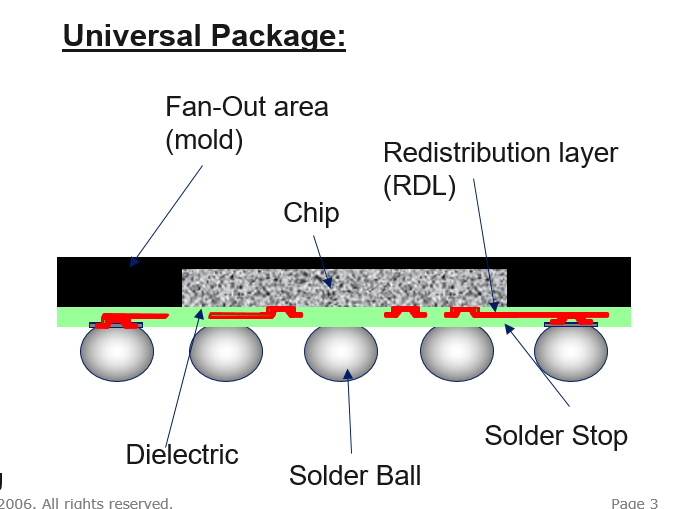
## eWLB

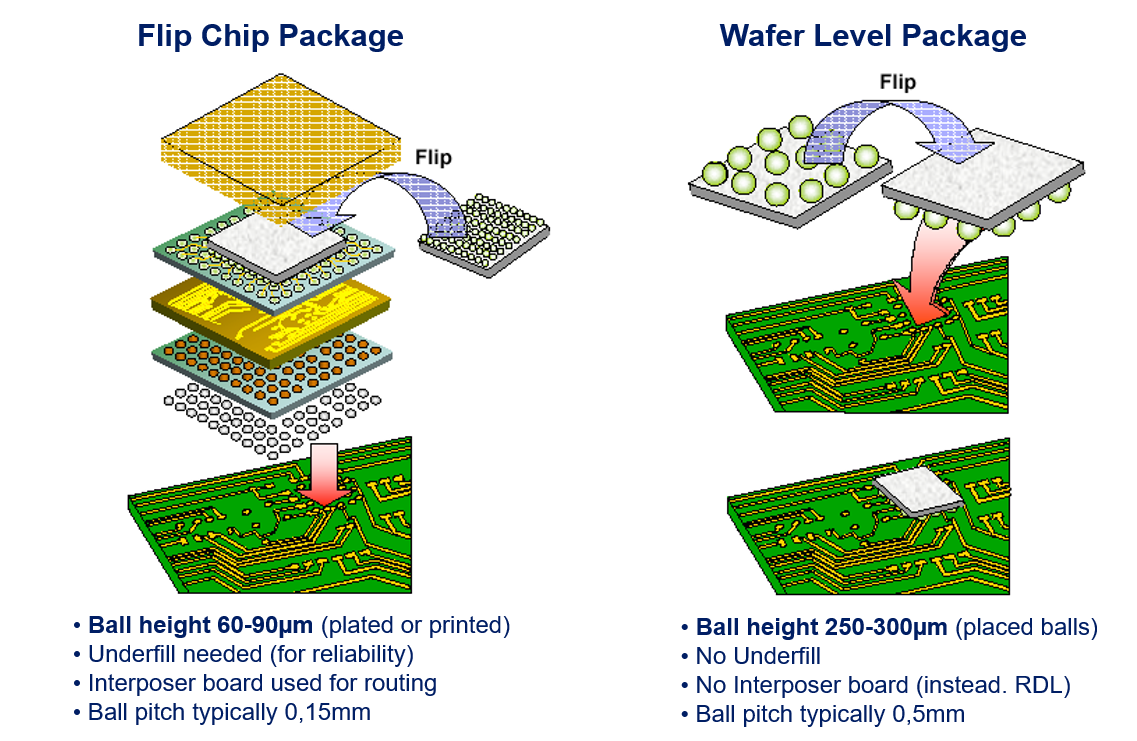
eWLB is also called **“embedded Wafer Level  Ball Grid Array”**. It use fan-out wafer level packaging (FOWLP) solution.

|  |  |
| --- | --- |
| **What is FO-WLP:** | |
| Fan-Out Wafer Level Package (FO-WLP) has been developed to offer additional space for routing higher number of I/O on top of silicon chip area and extending the package size with so-called the fan-out process which cannot be possibly applied in conventional Fan-In Wafer Level Package (FI-WLP). | |
| http://www.spil.com.tw/technology/images/9_01.png |  |

Below diagram compare the difference between Flip chip and Wafer level Package.

* No under fill and interposer board





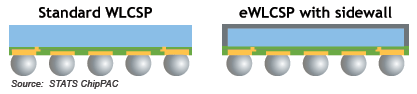
## WLCSP

**Wafer-level packaging** (**WLP**) is the technology of packaging an [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) while still part of the [wafer](https://en.wikipedia.org/wiki/Wafer_(electronics)), in contrast to the more conventional method of slicing the wafer into individual circuits (dice) and then packaging them. WLP is essentially a true [chip-scale package](https://en.wikipedia.org/wiki/Chip-scale_package) (CSP) technology, since the resulting package is practically of the same size as the die.[[1]](https://en.wikipedia.org/wiki/Wafer-level_packaging#cite_note-Semiconductor_International-1) Wafer-level packaging allows integration of wafer fab, packaging, test, and burn-in at wafer level in order to streamline the manufacturing process undergone by a device from silicon start to customer shipment.

WLCSP is also called fan-in Wafer Level Chip Scale Packaging solutions.

### Encapsulation Provides Increased Reliability and Durability

The basic structure of WLCSP has an active surface with polymer coatings and bumps with bare silicon exposed on the remaining sides and back of the die.  As the industry transitions to more advanced node products, the exposed silicon that is inherent in the WLCSP design becomes more of a concern due to the fragile dielectric layers. As mobile device manufacturers tighten technical specifications to achieve new levels of reliability in their end products, more stringent inspections and product durability are required. STATS ChipPAC offers customers a solution called [encapsulated Wafer Level Chip Scale Package (eWLCSP)](http://www.statschippac.com/packaging/packaging/waferlevel/~/link.aspx?_id=6449432A389F49989F2AC53AA0653957&_z=z) which features a back and sidewall coating on the die for an increased level of durability and reliability over traditional WLCSP designs. The thin polymer casing on the back and four sidewalls of the die, providing mechanical robustness and resistance to chipping, cracking and handling damage, as well as improved long term reliability compared to traditional bare die WLCSP.



## Reference



<https://en.wikipedia.org/wiki/CSP>

<https://en.wikipedia.org/wiki/Wafer-level_packaging>

<http://www.statschippac.com/packaging/packaging/waferlevel/wlcsp.aspx>

<http://www.spil.com.tw/technology/?u=9>