

Rev. Level	Date	ECO	Change DRI	Revision Description
F	2/3/16	0005548512	D. Leiser	Added Section 6.2.9 Monotonic Board Bending

Board Level Reliability Testing (BLRT) and Qualification – External

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1.0 REFERENCE DOCUMENTS

- JEDEC 22 – A104A: Operating Life 1000 hours
- JES-D22-A101C: Steady State Temperature Humidity Bias Life Test
- JESD-22-B104C: Mechanical Shock
- IPC/JEDEC – 9702: Cyclical Board Bending

2.0 DEFINITIONS

- ACF:** Anisotropic Conductive Film
- BGA:** Ball Grid Array
- BLRT:** Board Level Reliability Testing
- CTE:** Coefficient of Thermal Expansion
- CM:** Contract Manufacturer
- CSP:** Chip Scale Package
- DOE:** Design of Experiment
- DOE:** Design of Experiment
- DFM:** Designed for Manufacturing
- ENIG:** Electroless Nickel/Immersion Gold
- IC:** Integrated Circuit or Interconnect
- LGA:** Land Grid Array
- MEMS:** Microelectromechanical System
- NSMD:** Non-Solder Mask Defined
- OSP:** Organic Solderability Preservatives
- PCB:** Printed Circuit Board
- QFN:** Quad-Flat No-leads
- SMD:** Surface Mount Device or Solder Mask Defined
- SMT:** Surface Mount Technology
- TSV:** Through Silicon Via
- UBM:** Under-Bump Metallization

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3.0 SCOPE

This document defines Apple's expectations for the BLRT process conducted by the IC package vendor, including actions by the vendor that will trigger BLRT qualification/requalification.

4.0 PURPOSE

- To provide guidelines and specifications on SMD device and test board requirements for conducting board level reliability testing (BLRT) to determine the solder joint interconnect reliability using daisy-chained test packages.
- To ensure IC package robustness and vendor integrity, hence upgrading the reliability of Apple, Inc. products.
- To mechanically constrain the IC package to a PCB per Apple specifications and subject this IC – board assembly to mechanical and environmental stresses.

5.0 BACKGROUND

New IC packages are being used in Apple's next generation of products. These IC packages require qualification/requalification by either:

- Structural similarity to previous qualified IC packages or package types previously qualified by Apple may be used to qualify new packages in certain conditions.

Or

- Board Level Reliability Testing (Section 6.2.3). The test plan in this section establishes the fatigue reliability of solder pads and 2nd level interconnects.

Note: New IC package design and new fabrication processes will *ALWAYS* require BLRT testing.

6.0 IC DEVICE OR PROJECT REQUIREMENTS

6.1 Criteria

- The product must be BLRT verified if *ANY* of the criteria shown in Table 6.1 apply.
- The product must be BLRT verified if supplier's BLRT test conditions do not meet Apple's specifications as shown in Table 6.3.

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Table 6.1 Package Changes Requiring BLRT Validation

Criteria	Description	Requires Requalification if...
New IC Package	Package type not previously qualified by Apple	New Package Design
Package Type	Standard Packages (e.g., BGA, CSP, QFN, bare die, Passives)	Different
Wafer	Composition (Si, SiGe, GaAs), UBM stack, passivation	Different
Die Back Process	Die back etch (Edge Trench, TSV, MEMS), die thickness, back metal, metal thickness	Different
Die Bump	Composition (eutectic, Pb-free, Au, Cu), bump deposition (e.g., E-plate, Immersion Ag, stud bump), stand off height, diameter, pitch, high melt solder attached to low melt solder, reworked balls	Different
Substrate	Composition (ceramic, FR-4, Flex, Lead Frame), layer count, thickness, pad size, pad type, pad metal finish, solder mask	Different
Die Assembly (1st level)	Flip chip, Wire bond (Au, Cu), ACF bonding, solder reflow	Different
Encapsulation	No underfill, underfill, molded underfill, conformal coat, over mold compound (composition, CTE, Tg)	Different
Die Bonding Material	Organic, solder paste, preform	Different
Sub Assembly	Sub assemblies (metal lid, heat sink, 3D packages, embedded ICs/passives in PCBs)	Different
Solder Paste/Flux	Composition	Different
BGA / LGA (2nd Level)	Composition (eutectic, Pb-free), Pad type (SMD/NSMD), pad size, pad finish (ENIG, OSP) stand off height, diameter, pitch, high melt solder attached to low melt solder, reworked balls	Different
Solder Reflow	Reflow temperature profile, atmosphere	Different
BGA Encapsulation	No underfill, underfill, edge bond glue, UV cure glue (composition, CTE, Tg)	Different
Identification Marking Process	Laser engraving on die surface or package	Different
Package Body Size	Length, width and thickness	Larger
Die size	Length, width, and thickness	Larger

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6.2 PCB Test Board Requirements for Packages Requiring BLRT

Table 6.2 General PCB Guidelines for BLRT Boards for Qualification

Item	Description
1. Test Monitoring	The test board should be monitored with a daisy chain loop. All solder joints on the package should be monitored during the test.
2. Test Board Size	The board size depends on package size. Board must be designed for Stress Test requirements including the location and offset of the concentric holes. See Section 6.2.1 for details.
3. Package Placement	Center of test board.
4. Number of IC Packages on Test Board	1
5. Board Thickness	0.80 mm ± 10%
6. Board Material	Halogen-free low-Dk (Dk range of 3.2 to 3.8 @ 1 GHz) type laminate and pre-preg with minimum Tg of 145°C and minimum Td of 320°C
7. Soldermask	Minimum soldermask thickness of 4 µm and maximum thickness of 29 µm, with the height difference between an exposed metallized area and the upper surface of the soldermask immediately adjacent to the metallized area not to exceed 20 µm.
8. Pad Diameter	1:1 ratio between Cu pads on package vs. PCB
9. Surface Finish	OSP
10. Layer Count	10
11. Underfill	None required for test purposes
12. Solderpaste	SAC Alloy solderpaste to be used for component assembly to PCB.
13. Solder Reflow	See Figure 6.3.
14. Copper Trace/Space	Standard PCB specification.
15. Daisy Chain Requirements	All component terminations must be daisy chained. Refer to Section 6.2.2.
16. Mechanical Test Board	See Figure 6.1 for details on typical mechanical test board.
17. Fixture Mounting Hole Pattern	Mechanical holes are drilled along the two diagonal (orthogonal directions) on the PCB. The hole-to-hole spacing = 9.0 mm, measured along the diagonal directions. The holes must also lie along the circumference of concentric circles (imaginary), having the same geometric as that of PCB, with the package at the center. No holes should be present within the keep out circular zone around the package. Diameter of the keep out circle = 3 x package size.
18. PCB & Connector Hole Sizes	3.2 mm (fixture hole), 1.14 mm (Connector hole)
19. Connector	20-pin connector is used on test board for monitoring daisy chains. Recommended part number for the connector is: 998-2660. 20 Pin Connectors: Through-Hole, High Temp Part Number: N2520-6002UB, Manufactured by 3M Company

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6.2.1 Test Board Design Specification

The following drawings can be used to design and fabricate a test board for BLRT. Replace the chip size shown in the figure with the appropriate chip size used for the Apple test board. The hole diameter is 3.2 mm, and the connector hole diameter is 1.14 mm. Typical board uses a 20-pin connector in order to monitor multiple daisy chains. For testing additional daisy chains, a second connector can be used.

- For small IC packages refer to Figure 6.1.
- For larger IC packages refer to Figure 6.2.

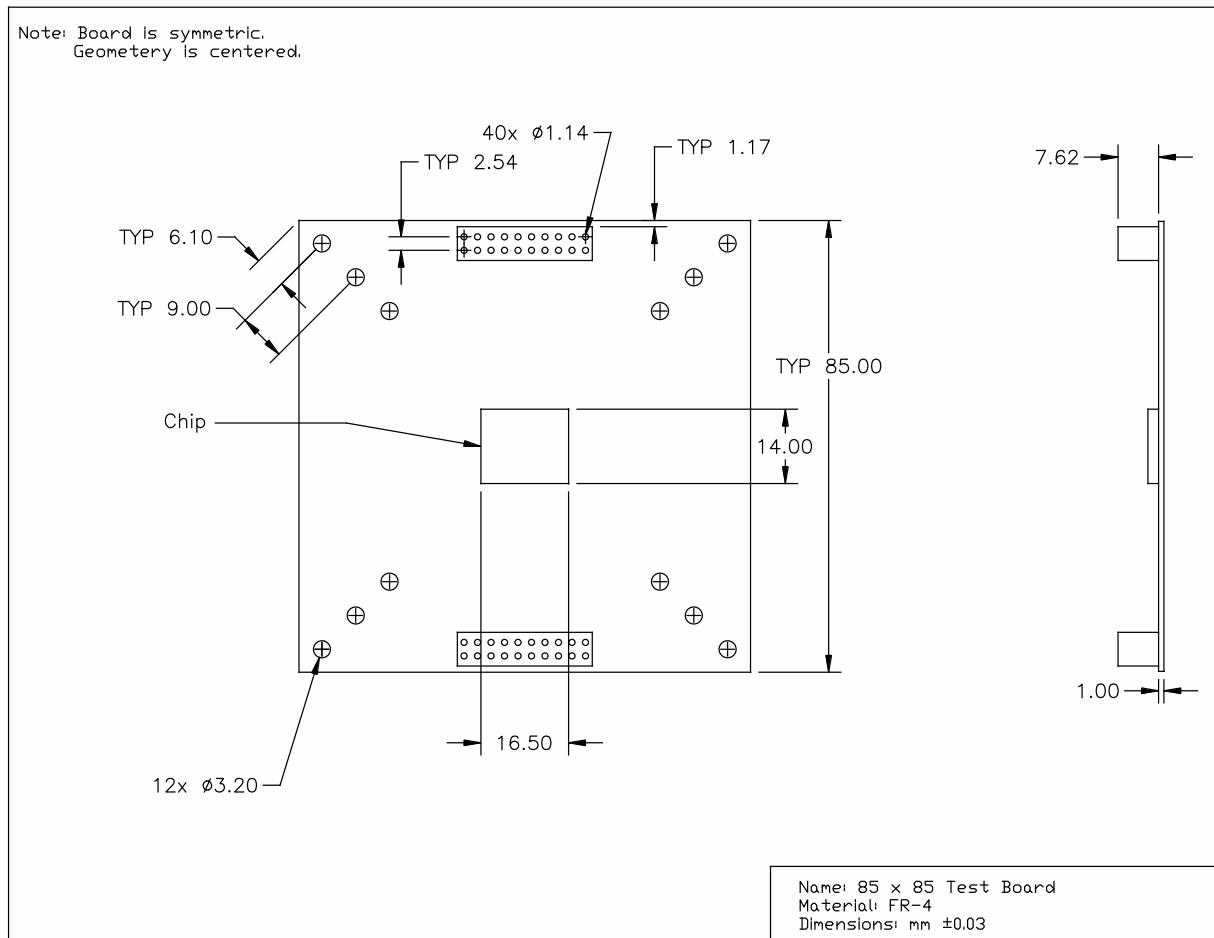


Figure 6.1 CAD Drawing for Test Board Design for BLRT (for Small IC Packages)

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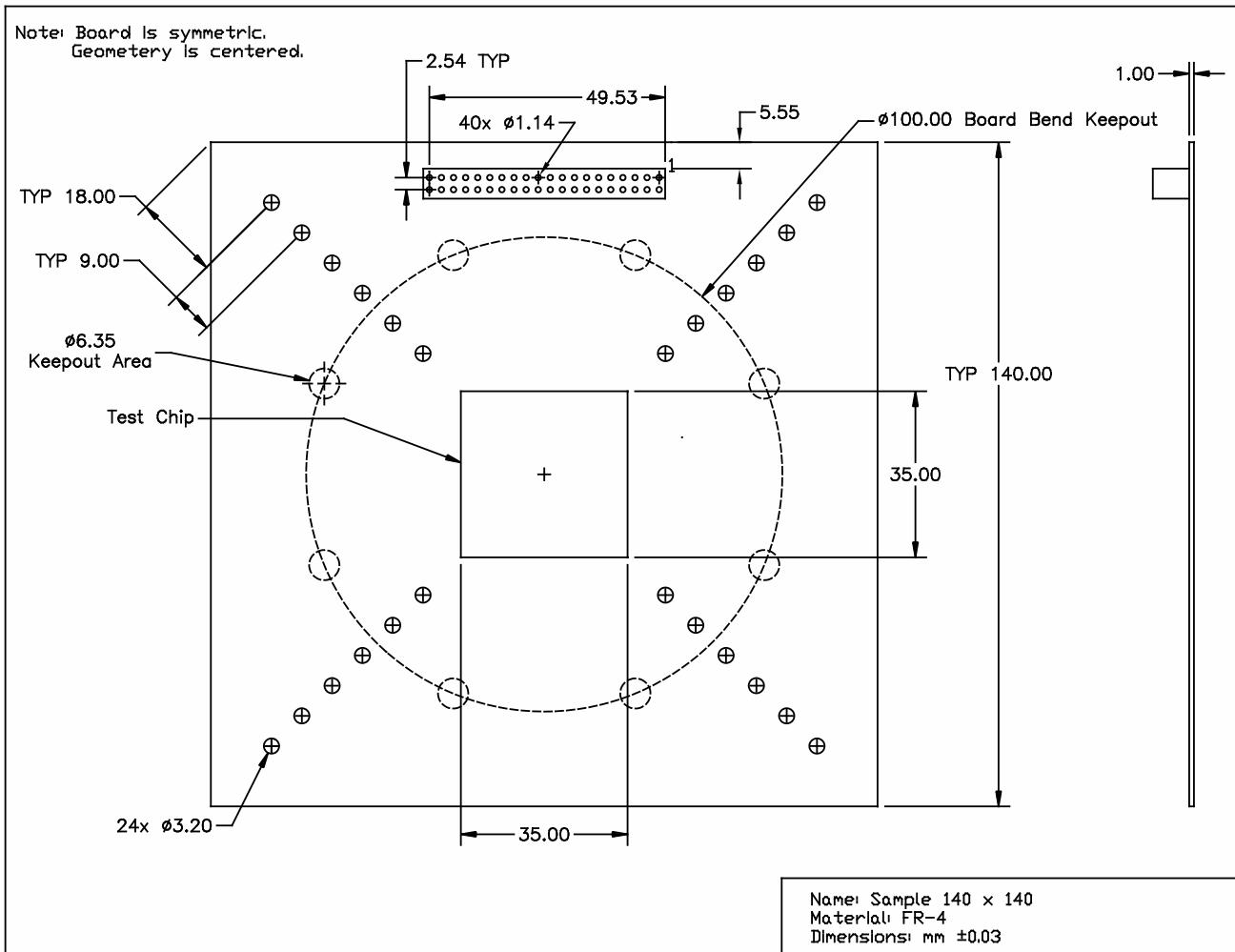


Figure 6.2 CAD Drawing for Test Board Design for BLRT (for Large IC Packages)

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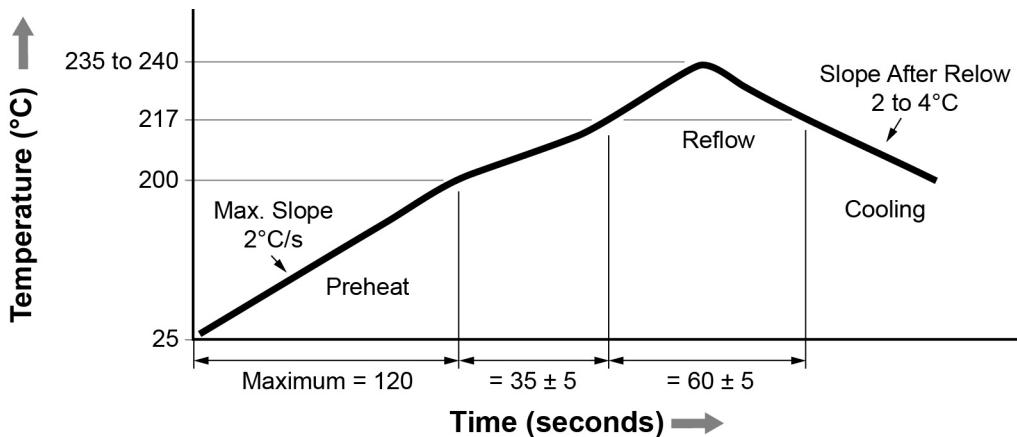


Figure 6.3 Reflow Profile for Pb-free Solder

6.2.2 Daisy Chain Schemes for the BLRT Boards

Although daisy chain structures can be made in a number of ways, simple straight chains (as shown in Figure 6.4) are preferred in order to facilitate inspection of solder joint failures using BGA cross-sections. Following are the guidelines used for preparing daisy chain structures for test boards.

In all configurations:

- All solder bumps in the package must be daisy chained for pass/fail test.
- Bump pairs must be shorted using Cu traces on both the package side and the PCB side.
- All daisy chains must be straight lines.
- Separate daisy chains must be used in alternate columns of each daisy chain.
- Each daisy chain must include test points on both the top and bottom side of the PCB.
- The input and output end of each daisy chain must be attached to a connector pin.
- Ground pin connections must be included in the design.
- Termination pairs (connected in the package design) must be similarly connected in the test PCB

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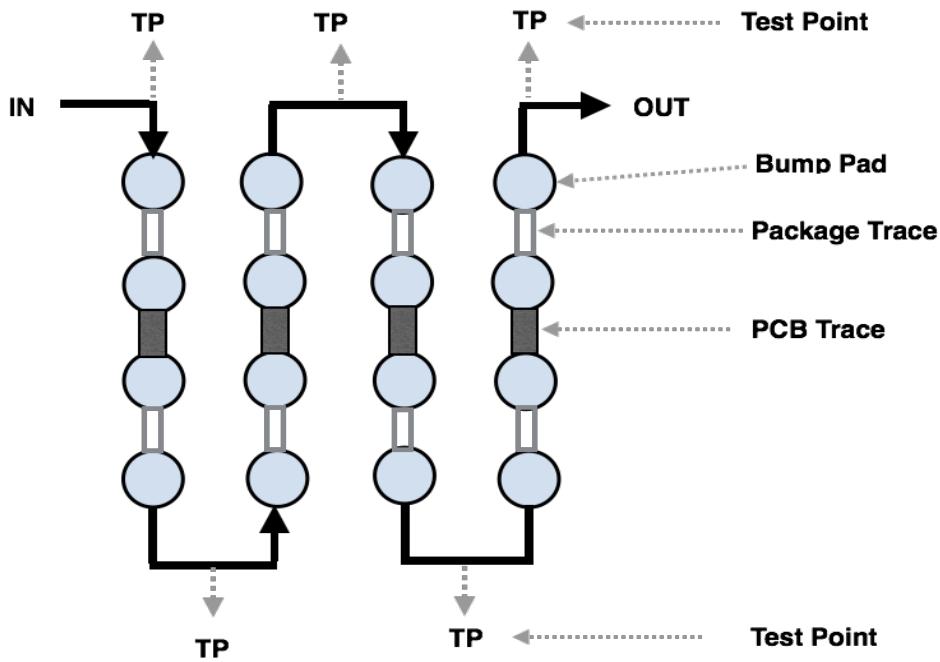


Figure 6.4 Daisy Chain Schematic for Opens

6.2.3 BLRT Stress Qualification Requirements

When a daisy-chained package is mounted on the PCB, a complete circuit is formed, which allows continuity testing. The circuit includes the solder balls, the metal pattern on the die, the bond wires, and the PCB traces.

The entire package or only a quadrant may be interconnected and tested.

Thermal cycling, vibration, and strain tests are used to predict behavior and reliability.

Apple may also require additional testing including analysis of failure samples. Refer to Section 7.0.

Note: The sample size is per single configuration. A larger sample size may be needed depending upon the number of configurations used in the DOE test matrix.

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**Table 6.3 Reliability Test and Qualification Plan for IC Packages on Test Boards
(Using Daisy Chained Chips)**

Stress Test	Stress Condition	Number of Assembly Lots	Sample Size per Lot	Duration	Fail Criteria	Reference
1. Thermal Cycling (air to air)	-40°C to 85°C, 20°C/min ramp, 23 min soak Functional test every 100 Cycles	3	33	1000 Cycles or failure	0F / 33 ≤ 90% resistance increase	JESD22-A104
2. Temperature and Humidity Dwell	85°C / 85% RH Functional test every 100 Hours	3	33	1000 Hours or failure	0F / 33 ≤ 90% resistance increase	JESD22-A101
3. Random Vibration	Level: 5G Frequency Range: 5 Hz to 500 Hz Axes: X, Y, Z Sine test sweep parameters: 5G, 1mm pk - pk, 47Hz, 5 to 500 Hz Board supported by only four mounting points	3	33	30 Minutes per Axis	0F / 33 ≤ 90% resistance increase	JESD22-B103
4. Mechanical Shock	Impact Profile: 10kG Shock Profile: 1/2 sine wave Shocks: 3 per package orientation Package Orientations: +X, -X, +Y, -Y, +Z, -Z Functional test after each orientation	3	33	0.25 ms per impact	0F / 33 ≤ 90% resistance increase	JESD22-B104
5. Monotonic Bending	Instron push to fail, 4-point board bending. Instron Speed: 2 mm/min Package Orientation: -Z axis Measure PCB strain at 1st package fail	3	33		Strain at 1st package fail > 5000 µE	JEDEC-9702

- Lots are defined as samples made at different time intervals, or samples processed by different fabs.
- Sample size will increase if different configs / variables are present (e.g. UF vs. no UF).

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6.2.4 Thermal Cycling

Note: The component's temperature may vary from the ambient temperature of the chamber.

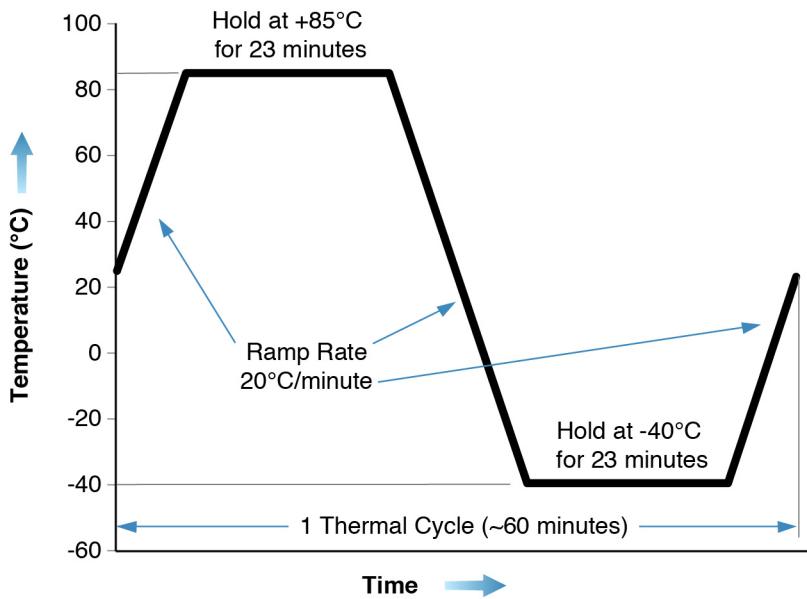


Figure 6.5 Thermal Cycling Profile

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6.2.5 Temperature and Humidity Dwell

If functional inspection requires removal from the chamber, use non-condensing ramp profiles to and from 85°C / 85% RH.

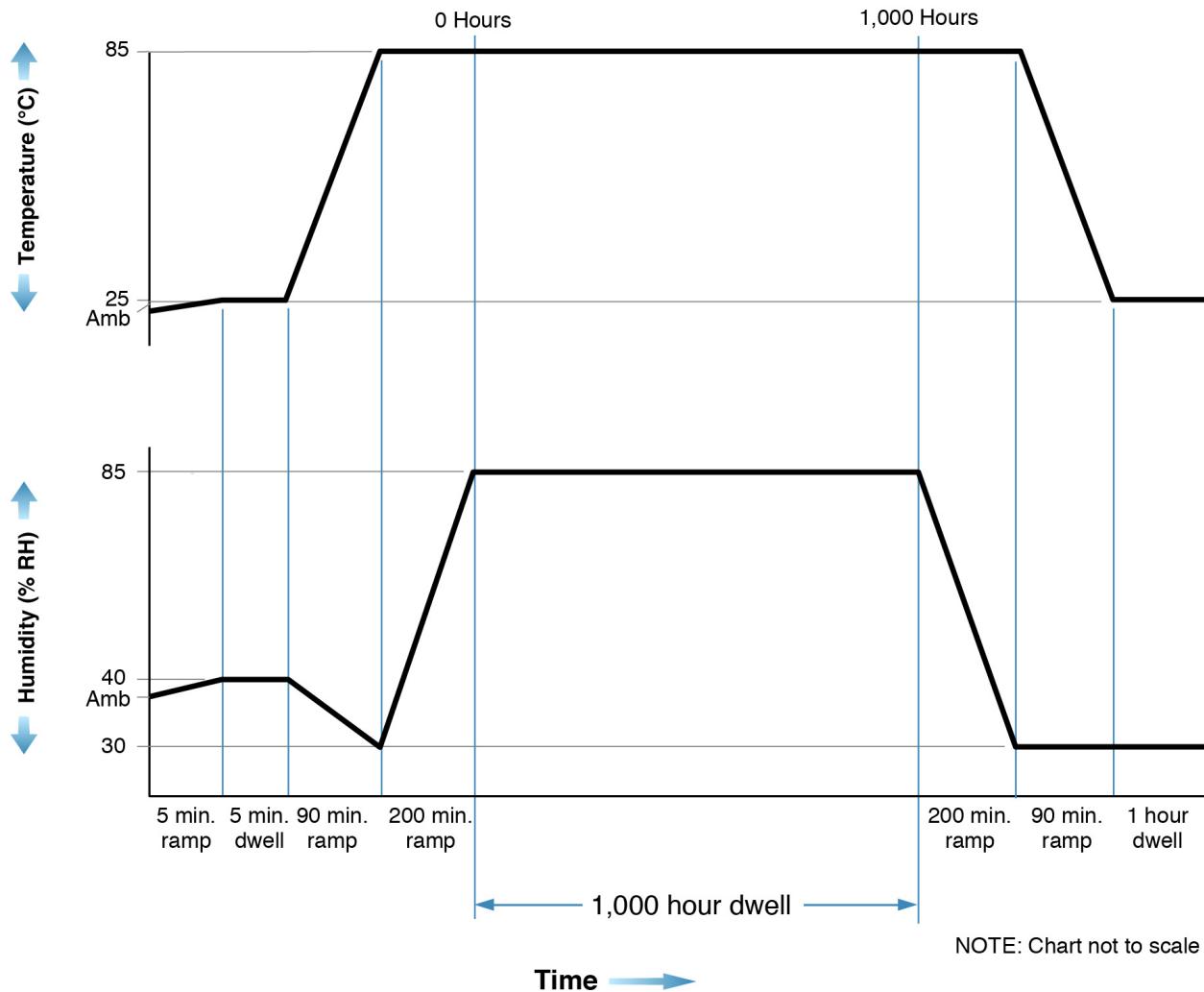


Figure 6.6 Temperature and Humidity Dwell Profile

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6.2.6 Random Vibration

Ideally, the test board should only be supported by 4 outside mounting points (refer to Outer posts) Larger PCBs may also require inner posts for support. Refer to Section 6.2 for additional information about the test board requirements.

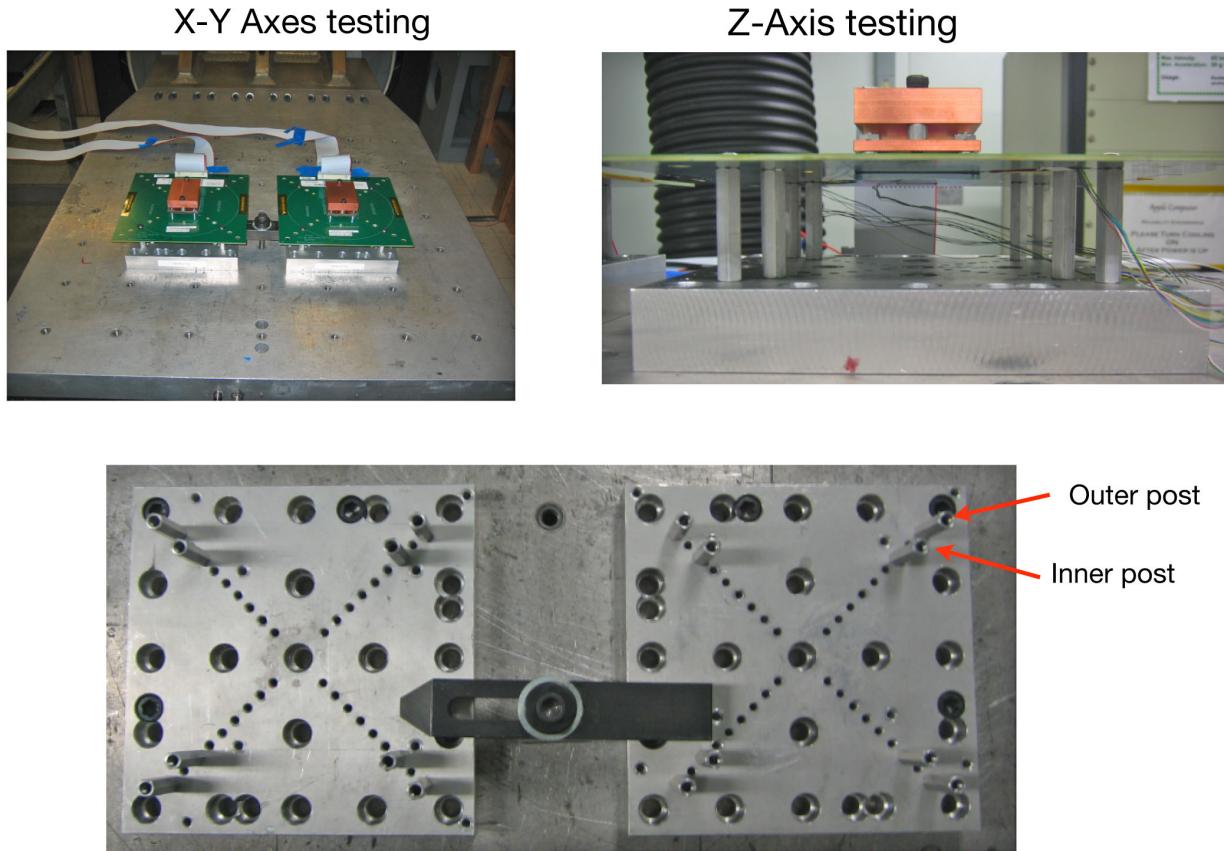


Figure 6.7 Random Vibration Setup

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Table 6.4 3G Random Vibration

G RMS	PSD (g²/Hz)	Frequency Range (Hz)	Duration per axis (Minutes)	Axis	Default UUT Orientation
5.0	0.0503	5 to 500	30	X, Y, Z	Top Surface Up

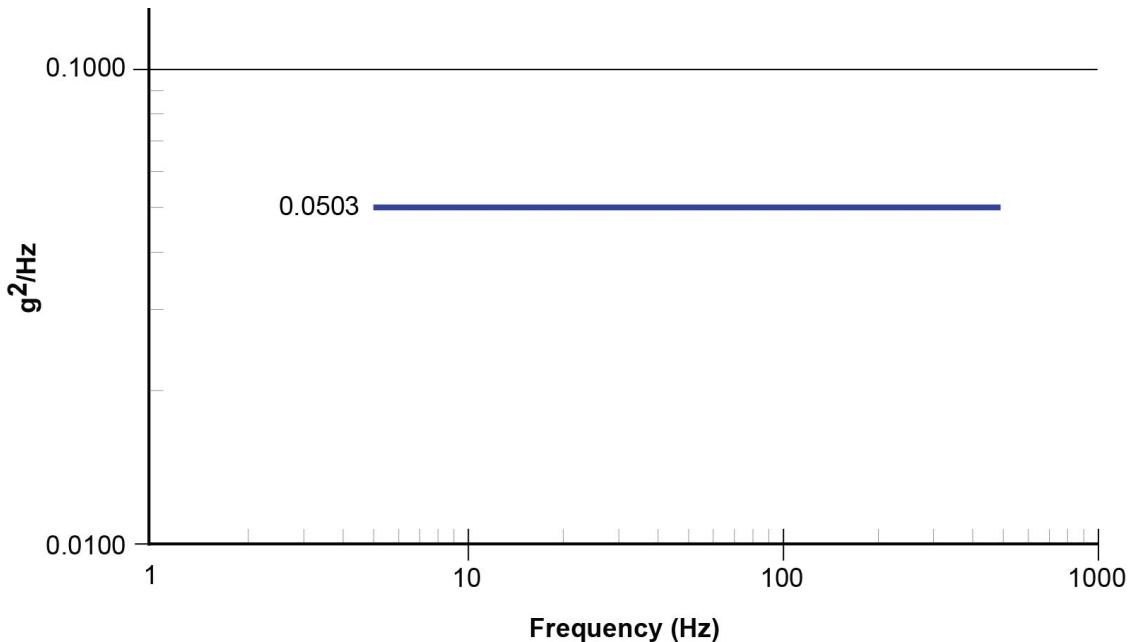


Figure 6.8 PSD for 3G Vibration

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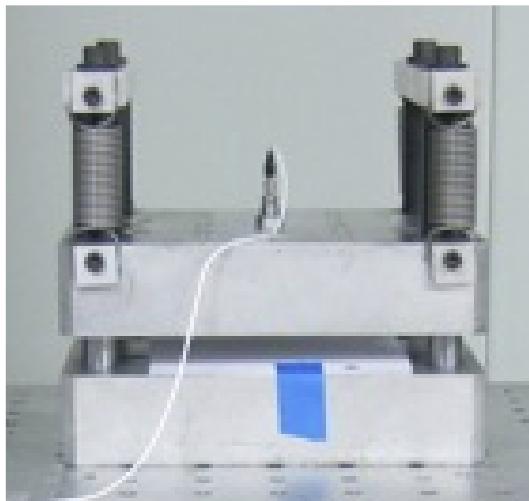
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6.2.7 Mechanical Shock

The shock response on the IC package is measured by directly attaching an Accelerometer (e.g., Meggitt 22) on top of the package using a quick set epoxy adhesive. Any rapid cure epoxy that can cure at room temperature and provide adequate adhesion strength to the package surface can be used.

6.2.7.1 Board Fixture

The following fixture can be used to allow drop testing in both the horizontal and vertical direction. The Dual Mass Shock Amplifier (DMSA) tool, supplied by Lansmont, is typically used for performing mechanical shock testing at 10,000 G. Figure 6.9 shows DMSA units (of different sizes) that are capable of producing shock pulses with a very high acceleration ($\sim 10,000$ G or so) and very short durations (< 1 ms).



6" x 9"



16" x 16"

Figure 6.9 DMSA Tools of Different Sizes for High G Shock Testing

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Figure 6.10 shows the experimental setup using PCB mounted on the DMSA tool for conducting the mechanical shock testing (at 10,000 G level). Using this setup, the test PCB can be mounted in the +/-Z directions (+Z refers to device facing up), and (-Z refers to facing the device down). A custom made metal plate fixture is used for mounting the test PCB by means of 8 metal posts (e.g. 4 inner screws and 4 outer screws, as shown in the Figure 6.10). The metal plate fixture is further attached to the DMSA base by using large screws.

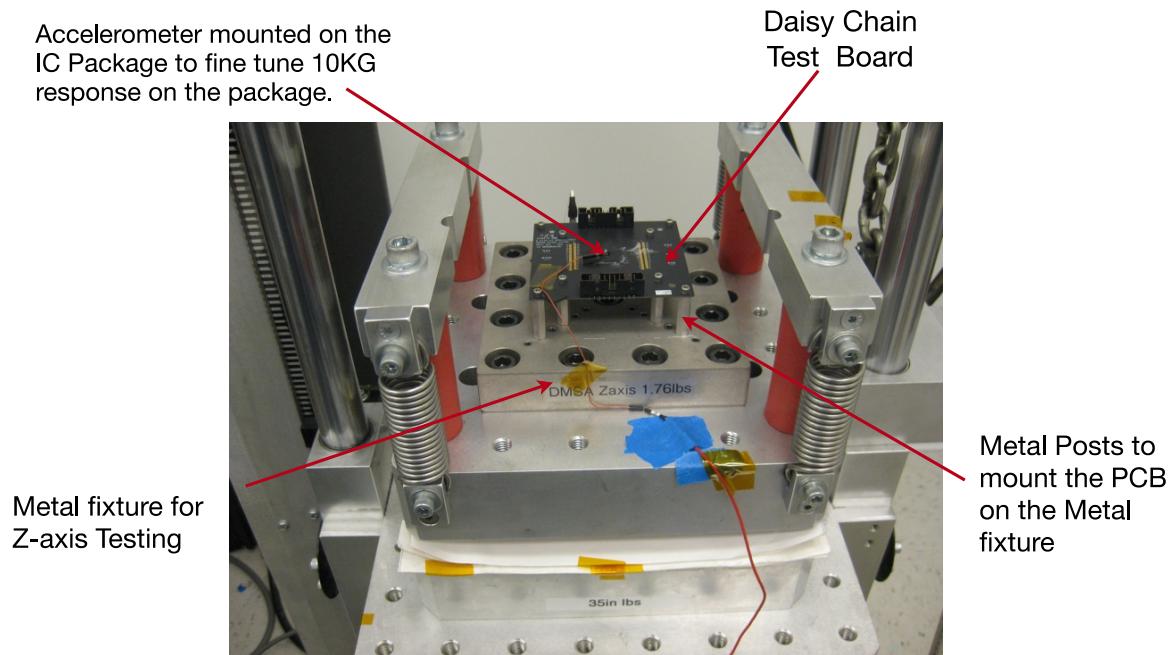


Figure 6.10 DMSA Tool Set Up for Mechanical Shock Testing at 10,000 G Level

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6.2.7.2 Stiffener

Use a polyurethane stiffener under the board, in order to reduce board deflection during 10,000 G shock testing and optimize the shock response to an acceptable level.

The thickness of the stiffener is the same as the gap height.

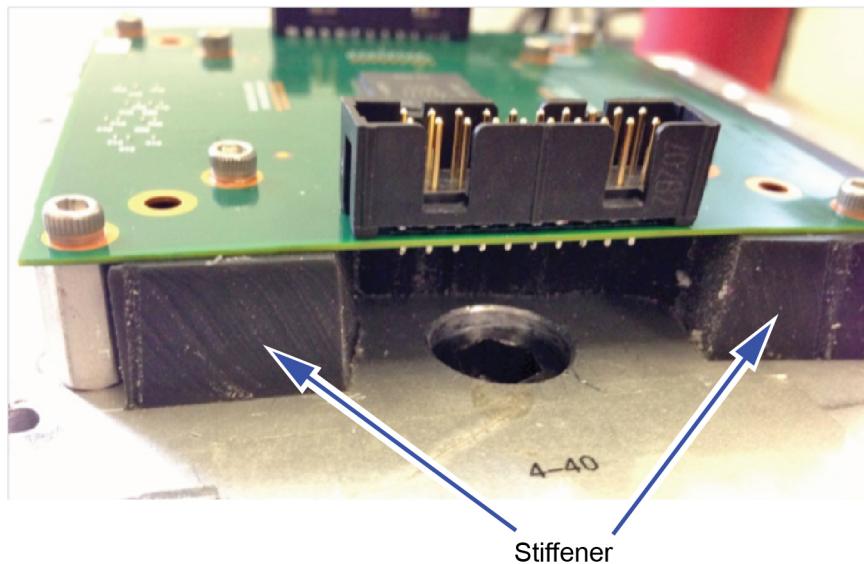


Figure 6.11 Stiffener Used Below the Test Boards to Optimize Shock Response

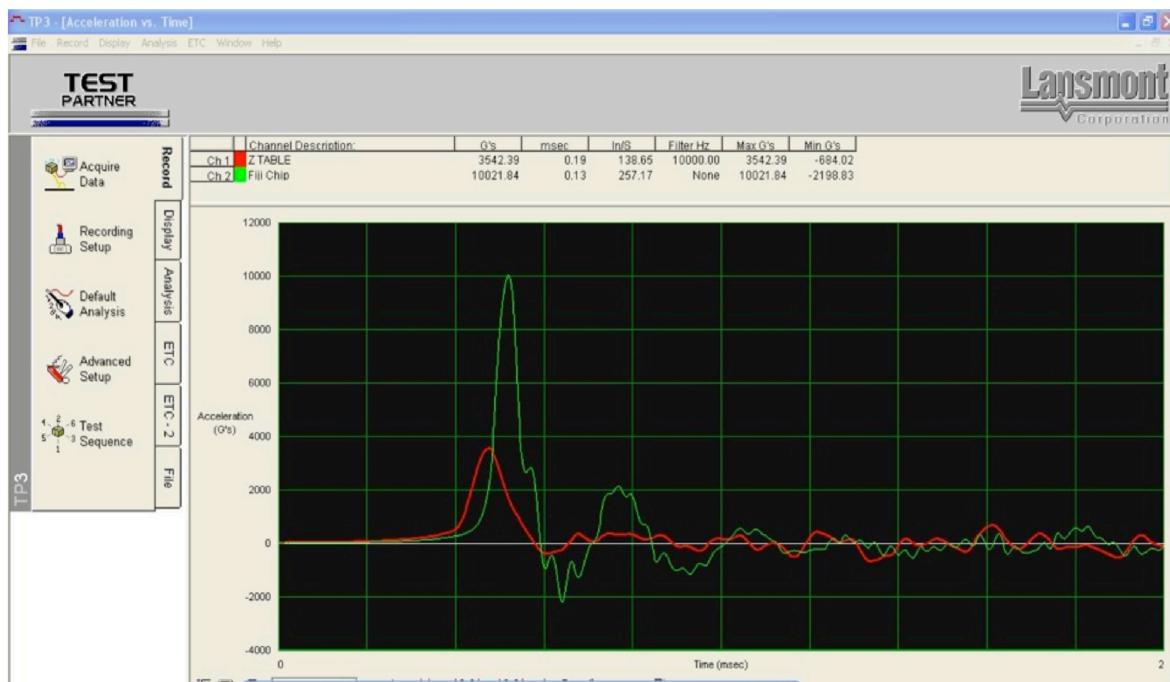
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6.2.7.3 Shock Pulse Response

The shock response must be optimized until a clean “bell shaped” trace appears on the display as shown in Figure 6.12.



Note: The green curve indicates shock response measured on top of the IC package and the red curve denotes the shock response measured on the shock table.

Figure 6.12 10,000 G Shock Response Curves

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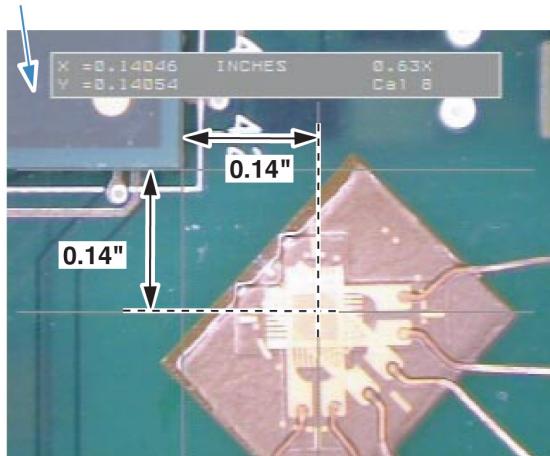
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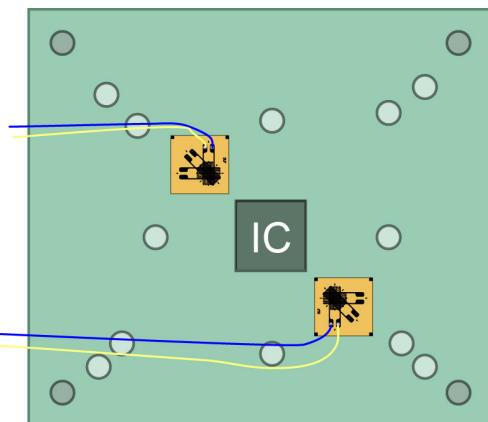
6.2.8 Strain Gage Attachment to BLRT Board

Strain gages should be placed at two locations, near diagonally opposite corners of the package. The board mounted Rosette should be located 5 mm diagonally out from the corner of the package. The 45° center grid of the strain gauge should be aligned to the package diagonal. The 0° and 90° grids should be square with the edges of the board. PCB Manufacturing strain is specified at 500 μE .

PCB Component
Under Strain Test



Offset from the component edge 0.14"



0° axis in the same orientation on both strain gages

Figure 6.13 Strain Gage Placement on the Test Board

6.2.9 Monotonic Board Bending

Board level package solder connections are typically more susceptible to fracture with increased strain rate. Monotonic bend (or non-reversing, bend-to-fail) characterization is intended to measure fracture resistance to flexural loading during non-cyclic board assembly and test operations. The test method needs the following tools:

- Universal tester (Instron) capable of tensile/compressive loading using controlled linear motion of cross head assembly. A load cell capable of measuring force up to 500 N is attached to the Instron.
- Four point bend assembly fixture with 4 cylindrical bars and rounded contact surfaces must be used to support the specimen or test board. The test board is placed on two anvils or rollers, and symmetrically loads the specimen on the opposite surface with two anvils or rollers. The load span or the distance between the top vs. bottom anvils is maintained at 1:2 ratio.
- Strain gages are attached along the two diagonally opposite corners of the IC package and the strain values must be measured during the bend testing.

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- The board should be oriented with the package facing downwards.
- A data acquisition system (DAQ), which is capable of measuring the daisy chains for resistance or voltage changes must be used for pass/fail criteria.
- Instron speed is maintained at 2 mm/min.

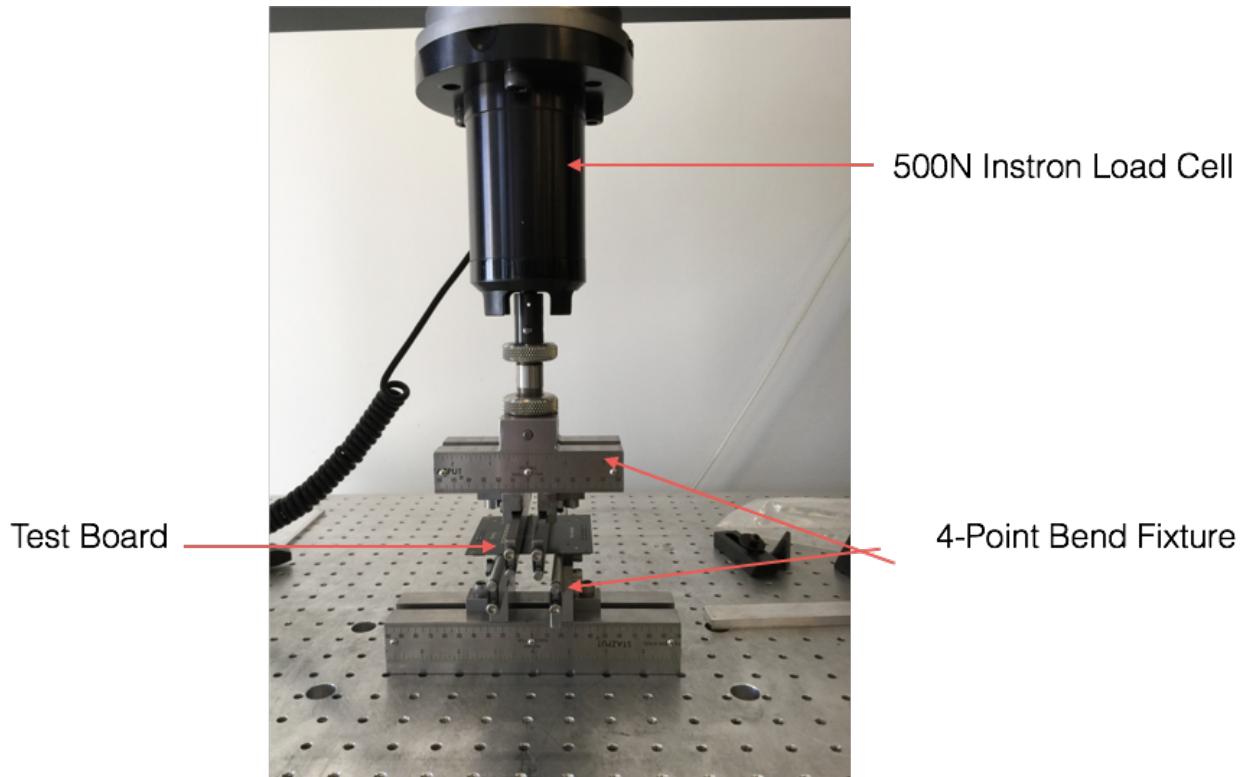


Figure 6.14 Monotonic Board Bending Test Setup, Using Instron and 4-point Bend Fixture

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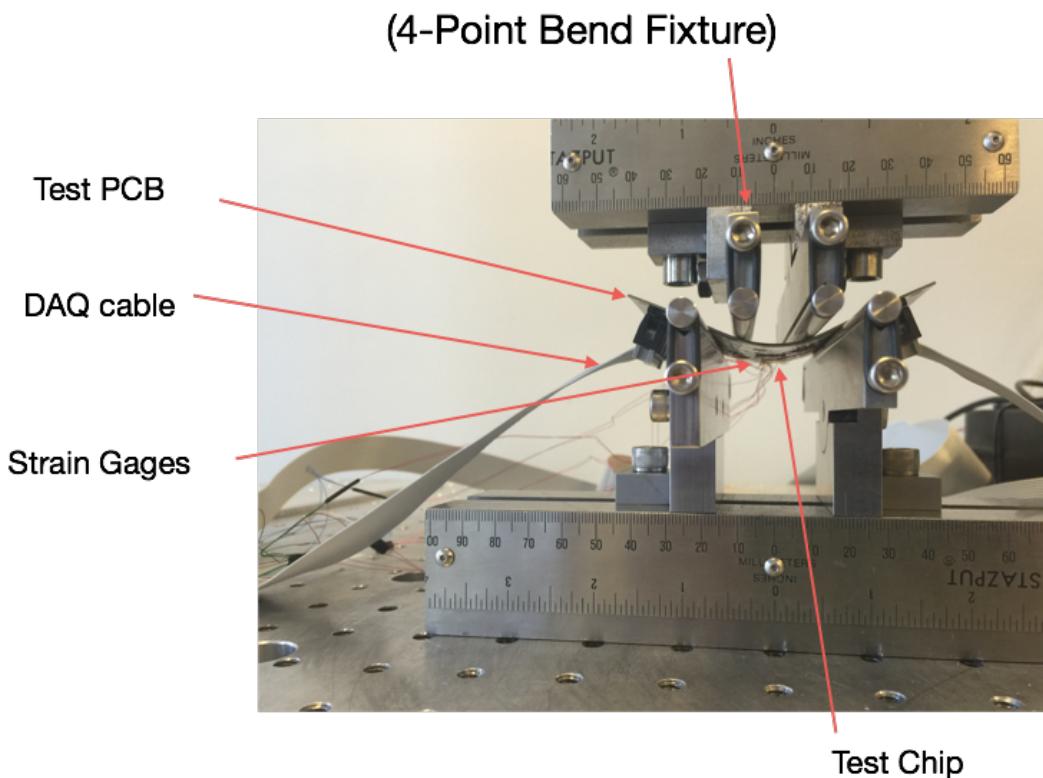


Figure 6.15 Close Up View of the 4-point Bend Fixture with the Sample Board

7.0 FAILURE ANALYSIS REQUIREMENTS

Failure analysis should be completed on failed samples to locate the solder joint disjunction. Apple may request specific FA procedures including:

- Dye and Pry: The sample is soaked in under vacuum in a liquid dye that penetrates into existing micro cracks or under open solder balls. After the dye dries the SMD is “priced” off the PCB and the solder balls are inspected for the presence of the staining that indicates problem areas. This method will reveal defects in the solder ball to pad interface after cross-sectioning.
- Cross-Sectioning: Cutting along the axis of interest, mechanical polishing, and etching.
- Scanning Electron Microscope Inspection: High magnification inspection looking for cracks and fracture surfaces, bond failures, and physical defects in the cross-sections. Used to determine the bonding failure level.

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8.0 REVISION HISTORY

Rev. Level	Date	ECO	Approver	Approval	Revision Description
A	7/1/13	0002115891	S. Darbha	See Agile	Initial Document
B	9/23/13	0002331471	S. Darbha	See Agile	Updated language in scope/purpose
C	6/2/14	0002855679	S. Darbha	See Agile	General updates, additional qualification requirements
D	6/2/14	0002856043	S. Darbha	See Agile	Remove reference to vibe 080 from table 3
E	10/31/2014	0003387191	S. Darbha	See Agile	Updates to Table 6.2 and Table 6.3, Section 6.2.2
F	2/3/2016	0005548512	S. Darbha	See Agile	Add Section 6.2.9 Monotonic Board Bending

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