LAB 4 REPORT

Design module has inputs serial_in, reset, enable, CLK100MHZ, and configure, and outputs out and led. It also has a number of internal registers and variables that are used to store intermediate values during operation.
“mod_first_bit”, “mod_second_bit”, “mod_third_bit”, and “mod_fourth_bit” are internal registers in the lab4_design module that are used to keep track of the state of the process that updates the value of the state variable. They are used to sequence the update process, with each bit of the input serial_in being added to the state variable in turn.

The module is designed to perform the following tasks:

- Increment a counter on every rising edge of the CLK100MHZ signal, but only if enable is high and reset is low.
- Check the value of the configure input and set the cnt_out output high when the counter reaches a particular value, depending on the value of configure.
- Update the value of a state variable on every rising edge of cnt_out, by taking the value of serial_in and adding it to the state, modulo 7. This is done in a sequence, with each bit of serial_in being added in turn.
- Toggle the value of the led output on every rising edge of cnt_out, but only if enable is high.
- Reset the counter to zero on every rising edge of cnt_out, but only if enable is high.

The update process works as follows:
There are four possible outputs for mod7: 0,1,2 and 4. We obtain this values and then calculate the new result according to that:

- On the first rising edge of cnt_out, mod_first_bit is set to 0 and mod_second_bit is set to 1. The value of serial_in is added to state, modulo 7.
- On the next rising edge of cnt_out, mod_second_bit is set to 0 and mod_third_bit is set to 1. The value of serial_in is added to state, modulo 7.
- On the next rising edge of cnt_out, mod_third_bit is set to 0 and mod_fourth_bit is set to 1. The value of serial_in is added to state, modulo 7.
- On the next rising edge of cnt_out, mod_fourth_bit is set to 0 and mod_first_bit is set to 1. The value of serial_in is added to state, modulo 7.

This process then repeats, with the update to state occurring on every rising edge of cnt_out and the value of serial_in being added to state in sequence.

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