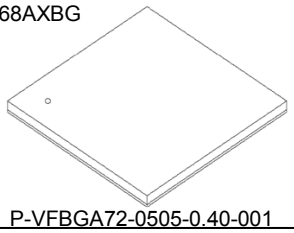
CMOS Digital Integrated Circuit Silicon Monolithic

TC358768AXBG/TC358778XBG

Mobile Peripheral Devices

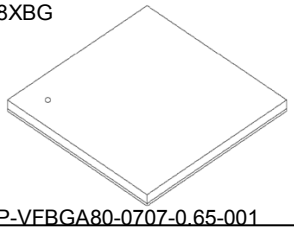
TC358768AXBG



P-VFBGA72-0505-0.40-001

Weight: 32.0 mg (Typ.)

TC358778XBG



P-VFBGA80-0707-0.65-001

Weight: 66.1 mg (Typ.)

Overview

Parallel Port to MIPI® DSI (TC358768AXBG/TC358778XBG) is a bridge device that converts RGB to DSI. All internal registers can be access through I^2C or SPI.

Features

- DSI-TX Interface
  - ✧ MIPI® DSI compliant (Version 1.02.00– June 28, 2010)
    - Support DSI Video Mode data transfer
    - DCS Command for panel register access
  - ✧ Supports up to 1 Gbps per data lane
  - ✧ Supports1,2,3 or 4 data lanes
  - ✧ Supports video data formats
    - RGB888/666/565
- RGB Interface
  - ✧ Supports data formats
    - 24-bit data bus
      - ➢ RGB888/666/565 data formats
  - ✧ Up to 166 MHz input clock
  - ✧ Support VSYNC/HSYNC polarity option (default LOW)
  - ✧ Support DE polarity option (default High)
- I^2C/SPI Slave Interface (Option to select either I^2C or SPI interface)
  - ✧ I^2C Interface (when CS=L)
    - Support for normal (100KHz), fast mode (400 kHz) and Special mode (1 MHz)
    - Configure all TC358768AXBG/TC358778XBG internal registers
    - Writing to DCS registers will trigger DCS Command transmits over DSI
  - ✧ SPI interface (when CS =H)
    - SPI interface support for up to 25 MHz operation.
    - Configure all TC358768AXBG/TC358778XBG internal registers
    - Writing to DCS registers will trigger DCS Command transmits over DSI
- GPIO signals
  - ✧ 2 GPIO signals
    - Two GPIO signals can be configured as SPI signals (SPI_SS and SPI_MISO)
    - Or One GPIO signal can be configured as Interrupt output signal, INT.
- System
  - ✧ Clock and power management support to achieve low power states.
- Power supply inputs
  - ✧ Core and MIPI® D-PHY: 1.2V
  - ✧ I/O: 1.8V – 3.3V
- Typical Power Consumption
  - ✧ WXGA @60fps: Pixel Clk: 74.25 MHz, DSIClk: 312 MHz ➔ 66.7 mW
  - ✧ 1080P @60fps: Pixel Clk: 148.5 MHz, DSIClk: 471 MHz ➔ 91.4 mW
  - ✧ Power Down Condition is achieved by turning off clock sources: PClk and RefClk.

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REFERENCES

1. MIPI DSI, "mipi_DSI_specification_v01-02-00, June 28, 2010"
2. MIPI DCS “DRAFT mipi_DCS_specification_v01-02-00_r0-02, December 2008”
3. MIPI D-PHY, “mipi_D-PHY_specification_v01-00-00, May 14, 2009"
4. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Overview

The Parallel Port to MIPI® DSI (TC358768AXBG/TC358778XBG) is a bridge device that converts RGB to DSI. All internal registers can be access through I^2C or SPI.

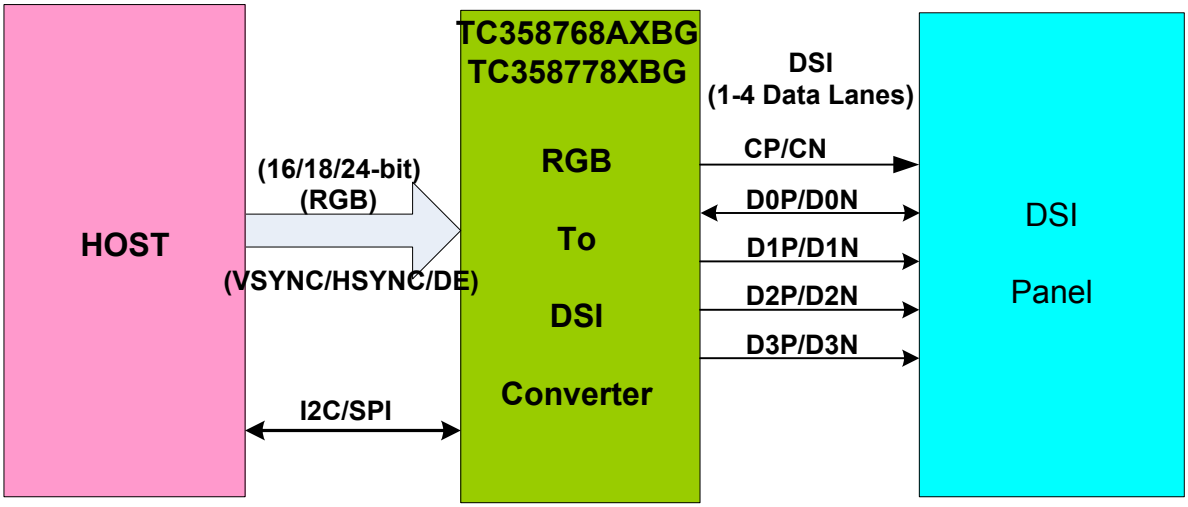


Figure 1.1 System Overview with TC358768AXBG/TC358778XBGin RGB to DSI-TX

2. Features

Below are the main features supported by TC358768AXBG/TC358778XBG.

- DSI-TX Interface
  - ✧ MIPI® DSI compliant (Version 1.02.00– June 28, 2010)
    - Support DSI Video Mode data transfer
    - DCS Command for panel register access
  - ✧ Supports up to 1 Gbps per data lane
  - ✧ Supports1,2,3 or 4 data lanes
  - ✧ Supports video data formats
    - RGB888/666/565
- RGB Interface
  - ✧ Supports data formats
    - 24-bit data bus
      - ➢ RGB888/666/565 data formats
  - ✧ Up to 166 MHz input clock
  - ✧ Support VSYNC/HSYNC polarity option (default LOW)
  - ✧ Support DE polarity option (default High)
- I^2C/SPI Slave Interface (Option to select either I^2C or SPI interface)
  - ✧ I^2C Interface (when CS=L)
    - Support for normal (100 kHz), fast mode (400 kHz) and Special mode (1 MHz)
    - Configure all TC358768AXBG/TC358778XBG internal registers
    - Writing to DCS registers will trigger DCS Command transmits over DSI
  - ✧ SPI interface (when CS =H)
    - SPI interface support for up to 25 MHz operation.
    - Configure all TC358768AXBG/TC358778XBG internal registers
    - Writing to DCS registers will trigger DCS Command transmits over DSI
- GPIO signals
  - ✧ 2 GPIO signals
    - Two GPIO signals can be configured as SPI signals (SPI_SS and SPI_MISO)
    - Or One GPIO signal can be configured as Interrupt output signal, INT.
- System
  - ✧ Clock and power management support to achieve low power states.
- Power supply inputs
  - ✧ Core and MIPI® D-PHY: 1.2 V
  - ✧ I/O: 1.8 V to 3.3 V

- Typical Power Consumption
  - ✧ WXGA @60fps: Pixel Clk: 74.25 MHz, DSIClk: 312 MHz ➔ 66.7 mW
  - ✧ 1080P @60fps: Pixel Clk: 148.5 MHz, DSIClk: 471 MHz ➔ 91.4 mW

	VDDC	VDDIO	VDDMIPI	Total Power	
	1.2 V	3.3 V	1.2 V		
1080P Video	42.8 mA	0. 4 mA	32.3 mA		
	51.36 mW	1.32 mW	38.76 mW	91.44	mW
WXGA Video	34.71 mA	0.167 mA	20.36 mA		
	41.652 mW	0.551 mW	24.432 mW	66.64	mW
Power Down w/o PCLK, RefClk	0. 074 mA	0. 025 mA	0. 004 mA		
	0. 089 mW	0. 0825 mW	0. 0048 mW	176.1	µW

  - ✧ Power Down Condition is achieved by turning off clock sources: PClk and RefClk.

3. External Pins

3.1. TC358768AXBG pinout description

TC358768AXBG resides in BGA72 pin packages. The following table gives the signals of TC358768AXBG and their function.

Table 3.1 TC358768AXBG Functional Signal List

Group	Pin Name	I/O	Type	Function	Note
System: Reset & Clock (4)	RESX	I	Sch	System reset input, active low	
	REFCLK	I	N	Reference clock input (6MHz - 40MHz)	
	MSEL	I	N	Mode Select 1'b0: Test mode 1'b1: Normal mode	
	CS	I	N	Configuration Select - When CS=L, enable I^2C interface - When CS=H, enable SPI interface	
MIPI-DSI (10)	MIPI_CP		PHY	MIPI-DSI clock positive	
	MIPI_CN		PHY	MIPI-DSI clock negative	
	MIPI_D0P		PHY	MIPI-DSI Data 0 positive	
	MIPI_D0N		PHY	MIPI-DSI Data 0 negative	
	MIPI_D1P		PHY	MIPI-DSI Data 1 positive	
	MIPI_D1N		PHY	MIPI-DSI Data 1 negative	
	MIPI_D2P		PHY	MIPI-DSI Data 2 positive	
	MIPI_D2N		PHY	MIPI-DSI Data 2 negative	
	MIPI_D3P		PHY	MIPI-DSI Data 3 positive	
	MIPI_D3N		PHY	MIPI-DSI Data 3 negative	
I2C (2)	I2C_SCL	OD	Sch	I^2C serial clock or SPI_SCLK	4 mA
	I2C_SDA	OD	Sch	I^2C serial data or SPI_MOSI	4 mA
Parallel Port IF (28)	PD[23:0]	I	N	Parallel Port Input Data Note: PD[23:16] can be configure to be GPIO[10:3]	
	VSYNC	I	N	Parallel port VSYNC signal	
	HSYNC	I	N	Parallel port HSYNC signal	
	DE	I	N	Parallel Port DE signal	
	PCLK	I	N	Parallel Port Clock signal	
GPIO (2)	GPIO[2:1]	I/O	N	GPIO[2:1] signals - (GPIO[1] option to become SPI_SSor INT signal) - (GPIO[2] option to become SPI_MISO signal)	4 mA
POWER (9)	VDDC (1.2 V)	NA		VDD for Internal Core (3)	
	VDDIO (1.8 V-3.3 V)	NA		VDDIO is for IO power supply (4)	
	VDD_MIPI (1.2 V)	NA		VDD for the MIPI (2)	
GROUND (17)	VSS	NA		Ground	

3.2. TC358768AXBG BGA72 Pin Count Summary

Table 3.2 TC358768AXBG BGA 72 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
MIPI-DSI	10	
I2C IF	2	
GPIO	2	
Parallel Port IF	28	
POWER	9	IO, MIPI and Core Power
GROUND	17	
TOTAL	**72**	

3.3. TC358778XBG pinout description

TC358778XBG resides in BGA80 pin packages. The following table gives the signals of TC358778XBG and their function.

Table 3.3 TC358778XBG Functional Signal List

Group	Pin Name	I/O	Type	Function	Note
System: Reset & Clock (4)	RESX	I	Sch	System reset input, active low	
	REFCLK	I	N	Reference clock input (6MHz - 40MHz)	
	MSEL	I	N	Mode Select 1'b0: Test mode 1'b1: Normal mode	
	CS	I	N	Configuration Select - When CS=L, enable I^2C interface - When CS=H, enable SPI interface	
MIPI-DSI (10)	MIPI_CP		PHY	MIPI-DSI clock positive	
	MIPI_CN		PHY	MIPI-DSI clock negative	
	MIPI_D0P		PHY	MIPI-DSI Data 0 positive	
	MIPI_D0N		PHY	MIPI-DSI Data 0 negative	
	MIPI_D1P		PHY	MIPI-DSI Data 1 positive	
	MIPI_D1N		PHY	MIPI-DSI Data 1 negative	
	MIPI_D2P		PHY	MIPI-DSI Data 2positive	
	MIPI_D2N		PHY	MIPI-DSI Data 2negative	
	MIPI_D3P		PHY	MIPI-DSI Data 3positive	
	MIPI_D3N		PHY	MIPI-DSI Data 3 negative	
I2C IF (2)	I2C_SCL	OD	Sch	I^2C serial clock or SPI_SCLK	4 mA
	I2C_SDA	OD	Sch	I^2C serial data or SPI_MOSI	4 mA
Parallel Port IF (28)	PD[23:0]	I	N	Parallel Port Input Data Note: PD[23:16] can be configure to be GPIO[10:3]	
	VSYNC	I	N	Parallel port VSYNC signal	
	HSYNC	I	N	Parallel port HSYNC signal	
	DE	I	N	Parallel Port DE signal	
	PCLK	I	N	Parallel Port Clock signal	
GPIO (2)	GPIO[2:1]	I/O	N	GPIO[2:1] signals - (GPIO[1] option to become SPI_SSor INT signal) - (GPIO[2] option to become SPI_MISO signal)	4 mA
POWER (9)	VDDC (1.2V)	NA		VDD for Internal Core (3)	
	VDDIO (1.8V - 3.3V)	NA		VDDIO is for IO power supply (4)	
	VDD_MIPI (1.2V)	NA		VDD for the MIPI (2)	
GROUND (25)	VSS	NA		Ground	

3.4. TC358778XBG BGA80 Pin Count Summary

Table 3.4 TC358778XBG BGA 80 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
MIPI-DSI	10	
I2C IF	2	
GPIO	2	
Parallel Port IF	28	
POWER	9	IO, MIPI and Core Power
GROUND	25	
TOTAL	**80**	

3.5. TC358768AXBG Pin Layout

A1	A2	A3	A4	A5	A6	A7	A8	A9
VSS	PD17	PD19	PD21	PD23	GPIO2	I2C_SCL	MSEL	VSS
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**
VDDC	PD16	PD18	PD20	PD22	GPIO1	I2C_SDA	RESX	VDDIO
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**
PD15	PD14	VSS	VSS	VSS	VSS	VDD_MIPI	MIPI_D3P	MIPI_D3N
D1	**D2**	**D3**				**D7**	**D8**	**D9**
PD13	PD12	VSS				VSS	MIPI_D2P	MIPI_D2N
E1	**E2**	**E3**				**E7**	**E8**	**E9**
VSS	VSS	VDDC				VDD_MIPI	MIPI_CP	MIPI_CN
F1	**F2**	**F3**				**F7**	**F8**	**F9**
VSS	VSS	VSS				VSS	MIPI_D1P	MIPI_D1N
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**
PD11	PD10	VDDIO	VSS	VSS	VDDIO	VDDIO	MIPI_D0P	MIPI_D0N
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**
VDDC	PD8	PD6	PD4	PD2	PD0	PCLK	DE	CS
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**
VSS	PD9	PD7	PD5	PD3	PD1	REFCLK	VSYNC	HSYNC

Figure 3.1 TC358768AXBG 72-Pin Layout (Top View)

3.6. TC358778XBG Pin Layout

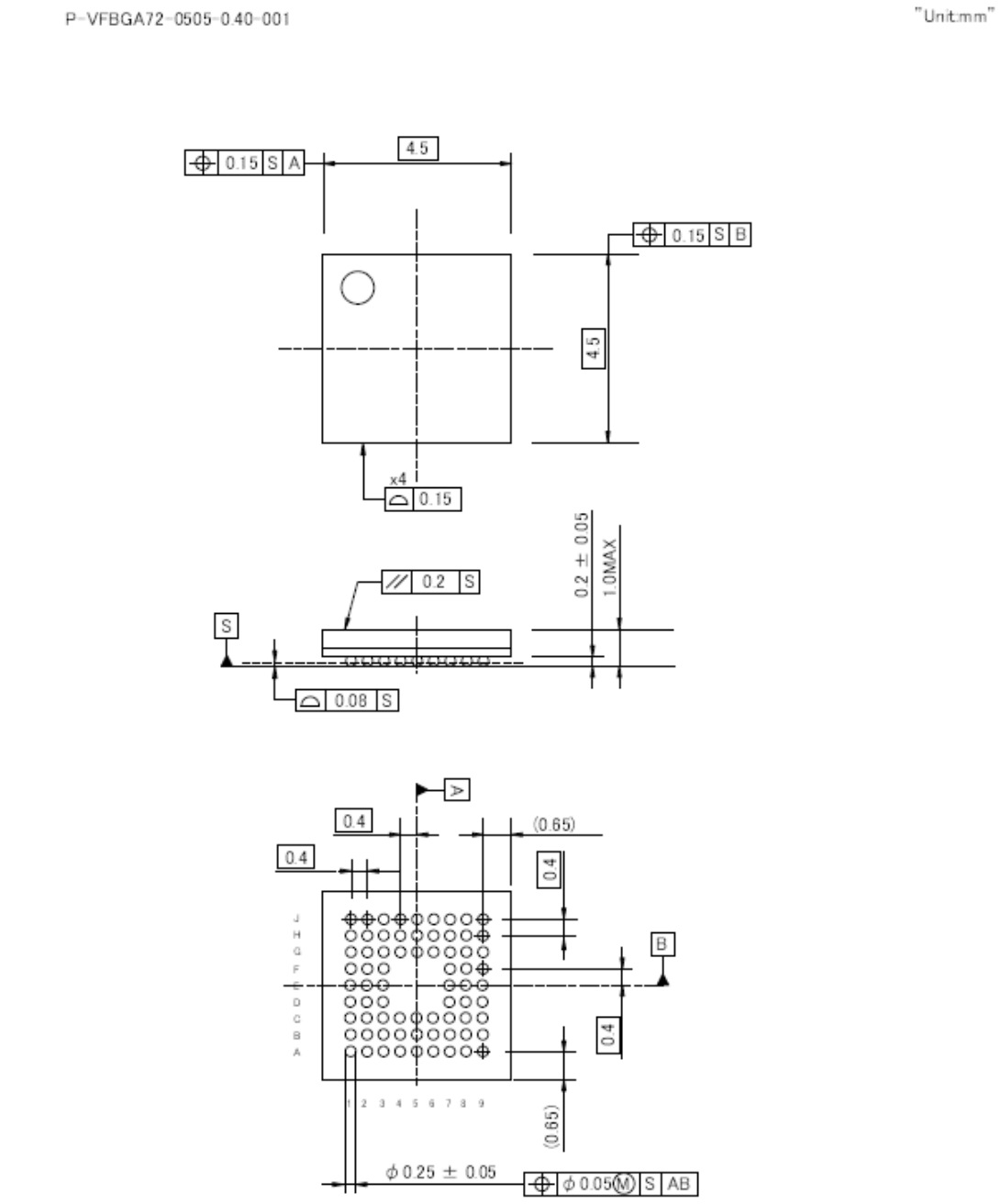
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
VSS	PD17	PD19	PD21	PD23	GPIO2	VDDC	I2C_SCL	MSEL	VSS
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
VDDC	PD16	PD18	PD20	PD22	GPIO1	VSS	I2C_SDA	RESX	VDDIO
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
PD15	PD14							MIPI_D3P	MIPI_D3N
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
PD13	PD12		VSS	VSS	VSS	VSS		MIPI_D2P	MIPI_D2N
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
PD11	PD10		VSS	VSS	VSS	VSS		VSS	VDD_MIPI
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
PD9	PD8		VSS	VSS	VSS	VSS		MIPI_CP	MIPI_CN
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
PD7	PD6		VSS	VSS	VSS	VSS		MIPI_D1P	MIPI_D1N
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
VDDIO	VSS							VSS	VDD_MIPI
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
PD4	PD2	PD0	VSS	VSS	PCLK	DE	CS	MIPI_D0P	MIPI_D0N
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
PD5	PD3	PD1	VDDC	VDDIO	REFCLK	VSYNC	HSYNC	VDDIO	VSS

Figure 3.2 TC358778XBG 80-Pin Layout (Top View)

4. Package

4.1. TC358768AXBG Package

The packages for TC358768AXBG is described in the figure below.



Weight: 32.0 mg (Typ.)

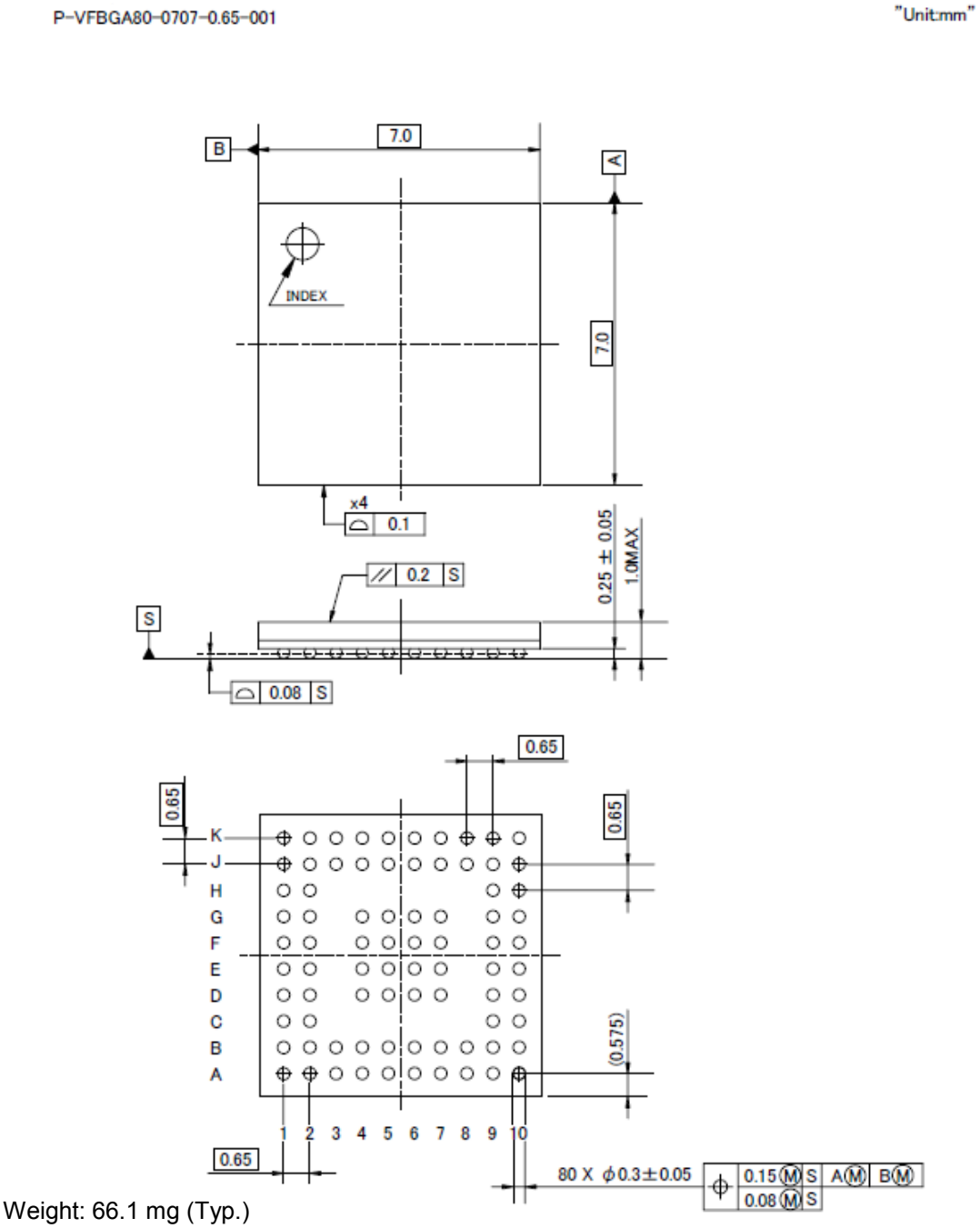
Figure 4.1 TC358768AXBG P-VFBGA72-0505-0.40-001 package

Table 4.1 TC358768AXBG P-VFBGA72-0505-0.40-001 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.4 mm	-
Solder ball height	0.15 mm	0.2 mm	0.25 mm
Package dimension	-	4.5 × 4.5 mm^2	-
Package height	-	-	1.0 mm

4.2. TC358778XBG Package

The package for TC358778XBG is described in the figure below.



Weight: 66.1 mg (Typ.)

Figure 4.2 TC358778XB P-VFBGA80-0707-0.65-001 package

Table 4.2 P-VFBGA80-0707-0.65-001 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Solder ball height	0.20 mm	0.25 mm	0.30 mm
Package dimension	-	7.0 × 7.0 mm^2	-
Package height	-	-	1.0 mm

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS= 0V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2V – MIPI PHY)	VDD_MIPI	-0.3 to +1.8	V
Input voltage (DSI IO)	V_{IN_DSI}	-0.3 to VDD_MIPI+0.3	V
Output voltage (DSI IO)	V_{OUT_DSI}	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO+0.3	V
Junction temperature	Tj	125	^oC
Storage temperature	Tstg	-40 to +125	^oC

5.2. Operating Condition

VSS= 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	1.65	1.8	1.95	V
Supply voltage (3.3V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – MIPI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	Ta	-30	+25	+85	^oC
Supply Noise Voltage	V_{SN}	-	-	100	mV_{pp}

5.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input Note1	V_{IH}	0.7 VDDIO	-	VDDIO	V
Input voltage, Low level input Note1	V_{IL}	0	-	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note1,2	V_{IHS}	0.7 VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note1,2	V_{ILS}	0	-	0.3 VDDIO	V
Output voltage High level Note1, Note2 **(Condition: I_{OH} = -0.4 mA)**	V_{OH}	0.8 VDDIO	-	VDDIO	V
Output voltage Low level Note1, Note2 **(Condition: IOL = 2 mA)**	V_{OL}	0	-	0.2 VDDIO	V
Input leak current, High level (Normal IO or Pull-up IO) (Condition: V_{IN} = +VDDIO, VDDIO = 3.6 V)	I_{ILH1} Note3	-10	-	10	μA
Input leak current, High level (Pull-down IO) (Condition: V_{IN} = +VDDIO, VDDIO = 3.6 V)	I_{ILH2} Note3	-	-	100	μA
Input leak current, Low level (Normal IO or Pull-down IO) (Condition: V_{IN} = 0 V, VDDIO = 3.6 V)	I_{ILL1} Note4	-10	-	10	μA
Input leak current, Low level (Pull-up IO) (Condition: V_{IN} = 0 V, VDDIO = 3.6 V)	I_{ILL2} Note4	-	-	200	μA

Note 1: Each power source is operating within recommended operation condition.

Note 2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note 3: Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note 4: Normal pin or Pull-down IO pin applied VSSIO (0V) to Vin (input voltage)

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.11	2014-05-28	Newly released

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