+5V   SlicePcbCon   +3V3

XSYS_MSEL	MSEL	A1
XSYS_TDM	TMS	A3
XSYS_TDSRC	TDO	A4
	PRSNT	A5
	CD1	A6
	CD2	A7
	CD3	A8
XSYS_XL_UP0		A9
		A10
XSYS_XL_UP1		A11
	CD4	A12
	CD5	A13
		A14
	CD6	A15
RST_N_ID		A16
	CD7	A17
	CD8	A18

A1 B1
A2 5V B2
A3 GND B3
A4 B4
GND 3V3 B5
A6 B6
A7 B7
A8 GND B8
A9 B9
GND B10
A11 B11
A12 B12
A13 B13
GND CLK B14
A15 B15
A16 GND B16
RST B17
A18 B18

S1

B1	DEBUG_N	XSYS_DEBUG_N
B2	TCK	XSYS_TCK
B3	TDI	XSYS_TDSNK
B6	DD1	
B7	DD2	
B9		XSYS_XL_DN1
B10	DD3	
B11		XSYS_XL_DN0
B12	DD4	
B13	DD5	
B14		CLK
B15	DD6	
B17	DD7	
B18	DD8	

GND   GND

Connector "A", the master board connector. On XP-SKC-L2 this is
the right-topmost "Square" slice connector.

The goal of this small board to daizy chain two devboards, which originally have
no capable connectors. Basically this board is similar to XA-SK-XTAG2 board just
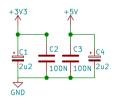revers direction in connectors wise.

REVIEW THIS:
I were double-checked the TDI/TDO thing...
But better to check it multiple times, before PCB mfg. :)

Findings:
  -SlicePcbCon part A16, A17 pins are mixed, at least
   pin signs?
  -Sys CLK pin is not used by XSYS connector.

CONN_PWR_B +5V

J1

TP1

J6

XSYS_MSEL	3	4	
XSYS_TDSRC	5	6	XSYS_XL_UP1
XSYS_TDM	7	8	
XSYS_TCK	9	10	XSYS_XL_UP0
XSYS_DEBUG_N	11	12	
XSYS_TDSNK	13	14	XSYS_XL_DN0
XSYS_RST_N	15	16	
XSYS_UART_RX	17	18	XSYS_XL_DN1
XSYS_UART_TX	19	20	

CONN_02X10

GND

Connector "B" for the slave xmos board direction. Can be an XA-SK-XTAG2 small
connector board too, or other dev boards with XSYS connector.
Jtag and Xlink bus are connected. PWR can be separable. Uart is connected to J7.

Please check the C/PMOD connectors data lines,
following to some XMOS port-with specific
strategy, if there can be any... And digilent PMODs
typical pin usage can be a point of view.
I mean, we can still route the pins now anyway.
How is the best?

J4

CD1	1	2	CD2
CD3	3	4	CD4
CD5	5	6	CD6
CD7	7	8	CD8
	9	10	
	11	12	

CONN_02X06

CONN_PWR_C +3V3

J2   GND   GND

J5

DD1	1	2	DD2
DD3	3	4	DD4
DD5	5	6	DD6
DD7	7	8	DD8
	9	10	
	11	12	

CONN_02X06

CONN_PWR_D +3V3

J3   GND   GND

Two Xilinx /Digilent CMOD, PMOD connectors. 3V3 line can be disconnected
by jumper. 8 gpio pin, gnd, pwr. Plant 2x6 male pins for connecting to CMOD
(devboards). In case of use a PMOD, we need to plant female conn here.
When connecting to PMOD/CMOD, be careful ! The power side need to be on
the same pins. But the data pins will be mirrored on vertical axis.
Double-check it: D1 vs D2...

+3V3   +5V

C1   C2   C3   C4
2u2 100N 100N 2u2

GND

CONN_UART

	3	XSYS_UART_TX
	2	XSYS_UART_RX
	1	

J7   GND

uart is not conneted by default, because no documentation mentioned
the official XMOS pin for that on Square slice connector, furthermore
XA-SK-XTAG2 board miss the uart connection at all.

JTAG and XLINK (and UART) connection between
Slice kit main boards and XCore 200 MC Audio Board

U Connector slice for xmos devboards
MYND-ideal ltd
Sheet: /
File: xmos_cpld.sch
Title: XMOS U Conn 1
Size: A4   Date: 2017-06-02   Rev: 1v0
KiCad E.D.A. kicad 4.0.6   Id: 1/1