

Brian Faure RUE#9150003563 DLD Hw #7

Design 4 Variable Parity Func. (1 for odd # bits)

a.) Truth Table

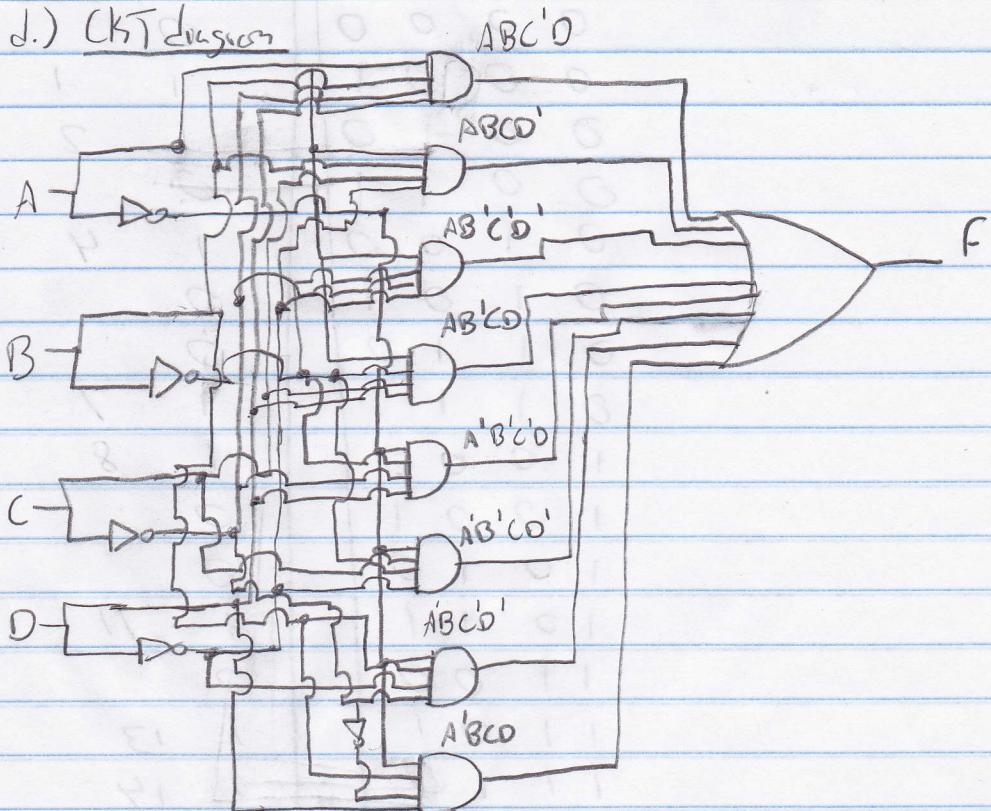
A	B	C	D	F (odd # "1" bits)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

b.) K-map  $F = \Sigma(1, 2, 4, 7, 8, 11, 13, 14)$

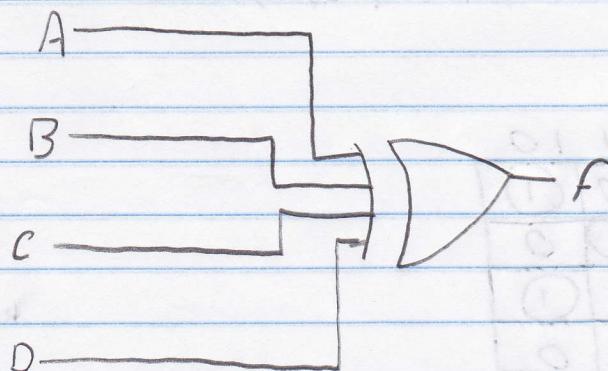
AB		00	01	11	10
CD	00	0	1	0	1
01	1	0	1	0	
11	0	1	0	1	
10	1	0	1	0	

C.) From Truth Table:  $F = A'B'C'D + A'B'CD' + A'BC'D' + A'BCD$   
 $+ ABC'D + ABCD' + AB'C'D' + AB'CD$

d.) CKT diagram



e.) From Truth Table:  $F = A \oplus B \oplus C \oplus D$



Binary Pg 2

$$\begin{array}{r} \text{S1} \\ A = 1101 \\ B = 1011 \\ \hline 0100 \end{array}$$

a) Adding numbers S (2)

a.) Adding

$$\begin{array}{r} \text{S1} \\ A = 1101 \\ + B = + 1011 \\ \hline 01000 \text{ w/Carry=1} \end{array}$$

$$\boxed{\begin{array}{l} \text{Sum} = 1000 \text{ w/ carry out of 1} \\ = 11000 \end{array}}$$

$$\begin{array}{r} \text{S2} \\ A = 1001 \\ + B = + 1101 \\ \hline 0110 \text{ w/Carry=1} \end{array}$$

$$\boxed{\begin{array}{l} \text{Sum} = 0110 \text{ w/ carry out of 1} \\ = 10110 \end{array}}$$

b.) Full Subtract

$$\begin{array}{r} \text{S1} \\ A = \\ - B = \begin{array}{r} | \\ 1101 \\ - 1011 \\ \hline 0010 \end{array} \end{array}$$

$$\boxed{\text{Diff} = 0010}$$

$$\begin{array}{r} \text{S2} \\ A = \\ - B = \begin{array}{r} | | \\ 01001 \\ - 01101 \\ \hline 1100 \end{array} \end{array}$$

$$\boxed{\begin{array}{l} \text{Diff} = 1100 \\ 0011 \\ + 0001 \\ \hline 0100 = -4 \end{array}}$$

C.) 2 comp Addition

$$\begin{array}{r}
 \text{S1} \\
 A - B = 0100 \\
 +(-B) \quad \quad \quad +1 \\
 \hline
 0101
 \end{array}
 \quad
 \begin{array}{r}
 \text{S1} \\
 A 1101 \\
 +(-B) = 10101 \\
 \hline
 0010
 \end{array}
 \quad
 \boxed{\text{Diff} = 0010}$$

$$\begin{array}{r}
 \text{S2} \\
 -B = 1101 \\
 \rightarrow 0010 \\
 +1 = 0011
 \end{array}
 \quad
 \begin{array}{r}
 \text{S2} \\
 A 1001 \\
 +(-B) = +0011 \\
 \hline
 1100
 \end{array}$$

$$\boxed{\text{Diff} = 1100} \\
 \rightarrow 001110 \\
 +1 = 0100$$

\* Chapter 6 \*

[6.19] For the 74x138, G2A & G2B Q all the outputs are active low so they correspond to active high inside the actual device

G1	G2A	G2B	C	B	A	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	x	x	x	x	x	0	0	0	0	0	0	0	0
x	0	x	x	x	x	0	0	0	0	0	0	0	0
x	x	0	x	x	x	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	1
1	1	1	0	0	1	0	0	0	0	0	0	1	0
1	1	1	0	1	0	0	0	0	0	0	0	0	0
1	1	1	0	1	1	0	0	0	0	0	1	0	0
1	1	1	1	0	0	0	0	0	0	1	0	0	0
1	1	1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0	0	0	0

Pg 3

[6.29] Algebraic Expression for  $S_3$  assume  $C_0=0$

$$C_1 = X_0 Y_0 \quad C_2 = X_1 Y_1 + (X_0 Y_0 (X_1 \oplus Y_1))$$

$$C_3 = X_2 Y_2 + ((X_1 Y_1 + (X_0 Y_0 (X_1 \oplus Y_1))) \cdot (X_2 \oplus Y_2))$$

$$S_3 = X_3 \oplus Y_3 \oplus C_3$$

$$= X_3 \oplus Y_3 \oplus [X_2 Y_2 + ((X_1 Y_1 + (X_0 Y_0 (X_1 \oplus Y_1))) \cdot (X_2 \oplus Y_2))]$$

[6.30] Because the 4th Multiplexer is the last to receive its correct carry-in, its outputs will take by far the longest...

Carry-in to 1st Multiplexer  $C_{out} = 22\text{ns}$

$C_{out}$  to 2nd  $C_{out} = 22\text{ns}$

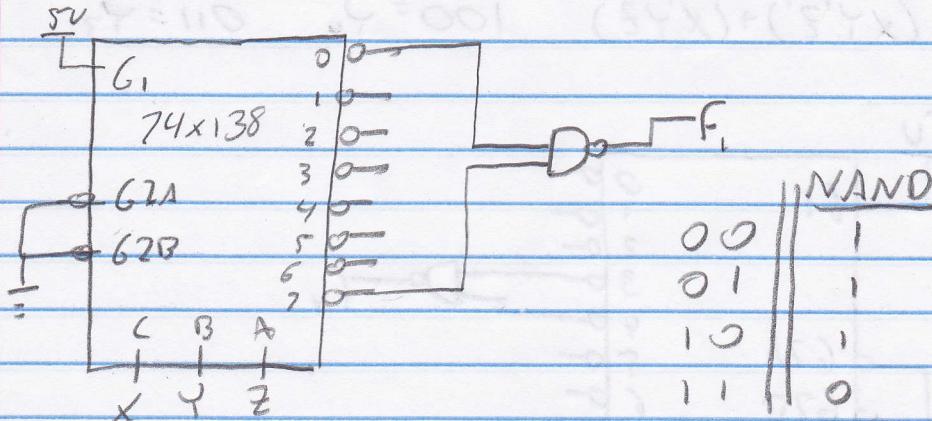
2nd  $C_{out}$  to 3rd  $C_{out} = 22\text{ns}$

3rd  $C_{out}$  to Any  $S_{out} = 24\text{ns}$

$$22+22+22+24 = 90\text{ns}$$

\* - It will take at most  $90\text{ns}$  to receive S12 thru S15 \*

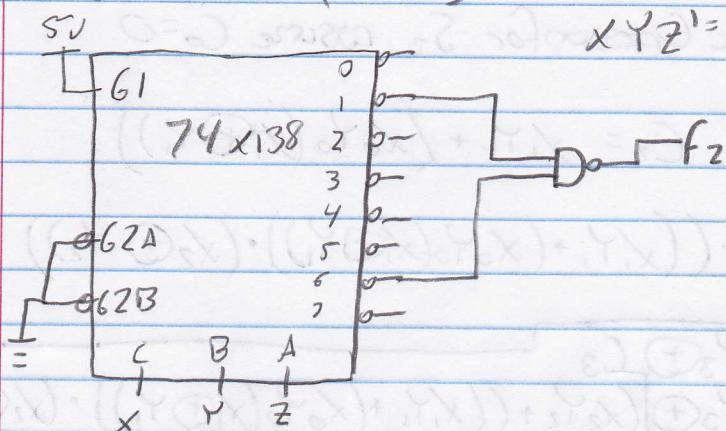
[6.43]  $F_1 = (X'Y'Z') + (XYZ)$



$$f_2 = (x' y' z) + (x y z')$$

$$x' y' z = 001 = y_1$$

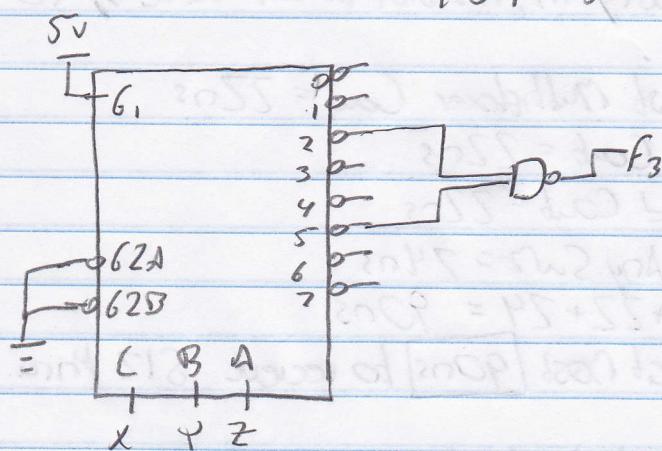
$$x y z' = 110 = 6 = y_6$$



$$f_3 = (x' y z') + (x y' z)$$

$$010 = 2 = y_2$$

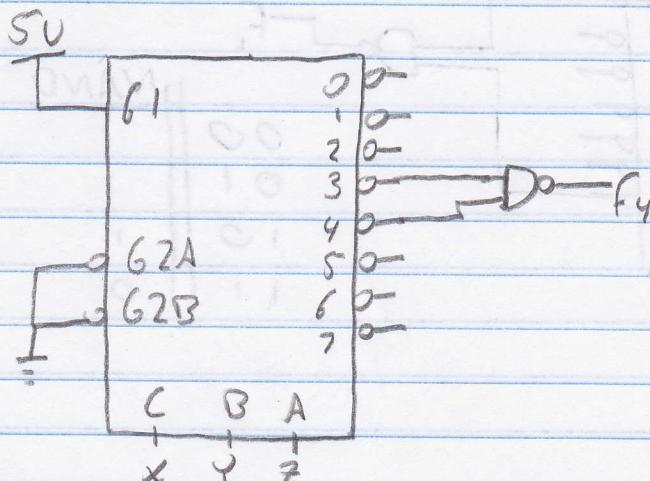
$$101 = 5 = y_5$$



$$f_4 = (x y' z') + (x' y z)$$

$$100 = y_4$$

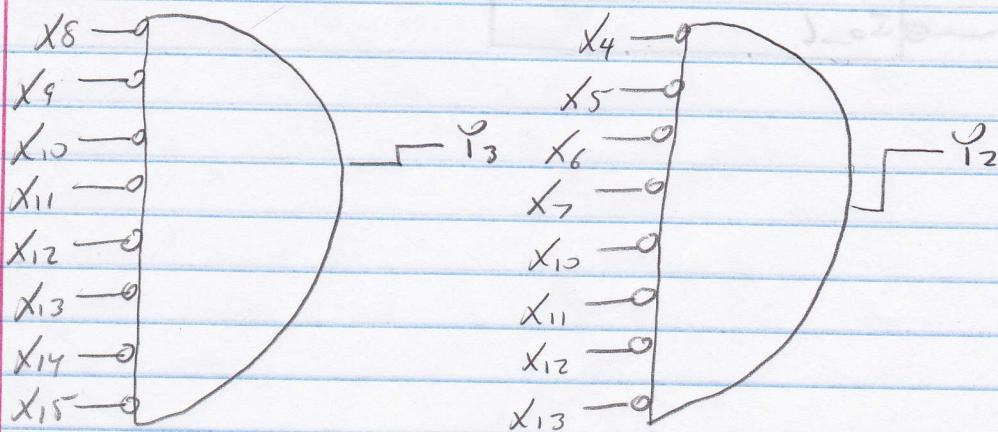
$$011 = y_3$$

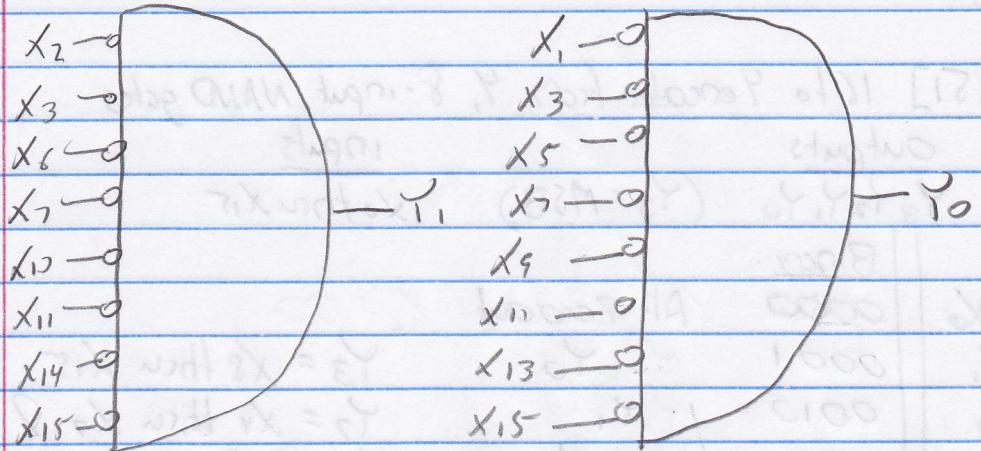


Pg 4

[6.51] 16-to 4 encoder from 4, 8-input NAND gates

	<u>Outputs</u>	<u>Inputs</u>
	$Y_3 Y_2 Y_1 Y_0$ ( $Y_3 = \text{MSB}$ )	$x_0 \text{ thru } x_{15}$
	<u>Binary</u>	
$x_0$	0000	All Zeros
$x_1$	0001	$Y_0$
$x_2$	0010	$Y_1$
$x_3$	0011	$Y_1 Y_0$
$x_4$	0100	$Y_2$
$x_5$	0101	$Y_2 Y_0$
$x_6$	0110	$Y_2 Y_1$
$x_7$	0111	$Y_2 Y_1 Y_0$
$x_8$	1000	$Y_3$
$x_9$	1001	$Y_3 Y_0$
$x_{10}$	1010	$Y_3 Y_1$
$x_{11}$	1011	$Y_3 Y_1 Y_0$
$x_{12}$	1100	$Y_3 Y_2$
$x_{13}$	1101	$Y_3 Y_2 Y_0$
$x_{14}$	1110	$Y_3 Y_2 Y_1$
$x_{15}$	1111	$Y_3 Y_2 Y_1 Y_0$





- All inputs into the nand gates are active low and all outputs are active high

[6.83]

