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#1) Det T_{pd} for the following...

a.) S_0 Read Backwards → XOR & AND & INV. & NOR

30ns 20ns 10ns 10ns

$30+20+10+10 = 50+20 =$ **70ns Delay for S_0**

b.) S_1 XOR, AND, OR, INV., NAND

$30+20+20+10+10 = 50+40 =$ **90ns for S_1**

c.) S_2 XOR, AND, OR, INV., NAND

$30+20+20+10+10 =$ **90ns for S_2**

d.) S_3 XOR, AND, OR, INV, INV

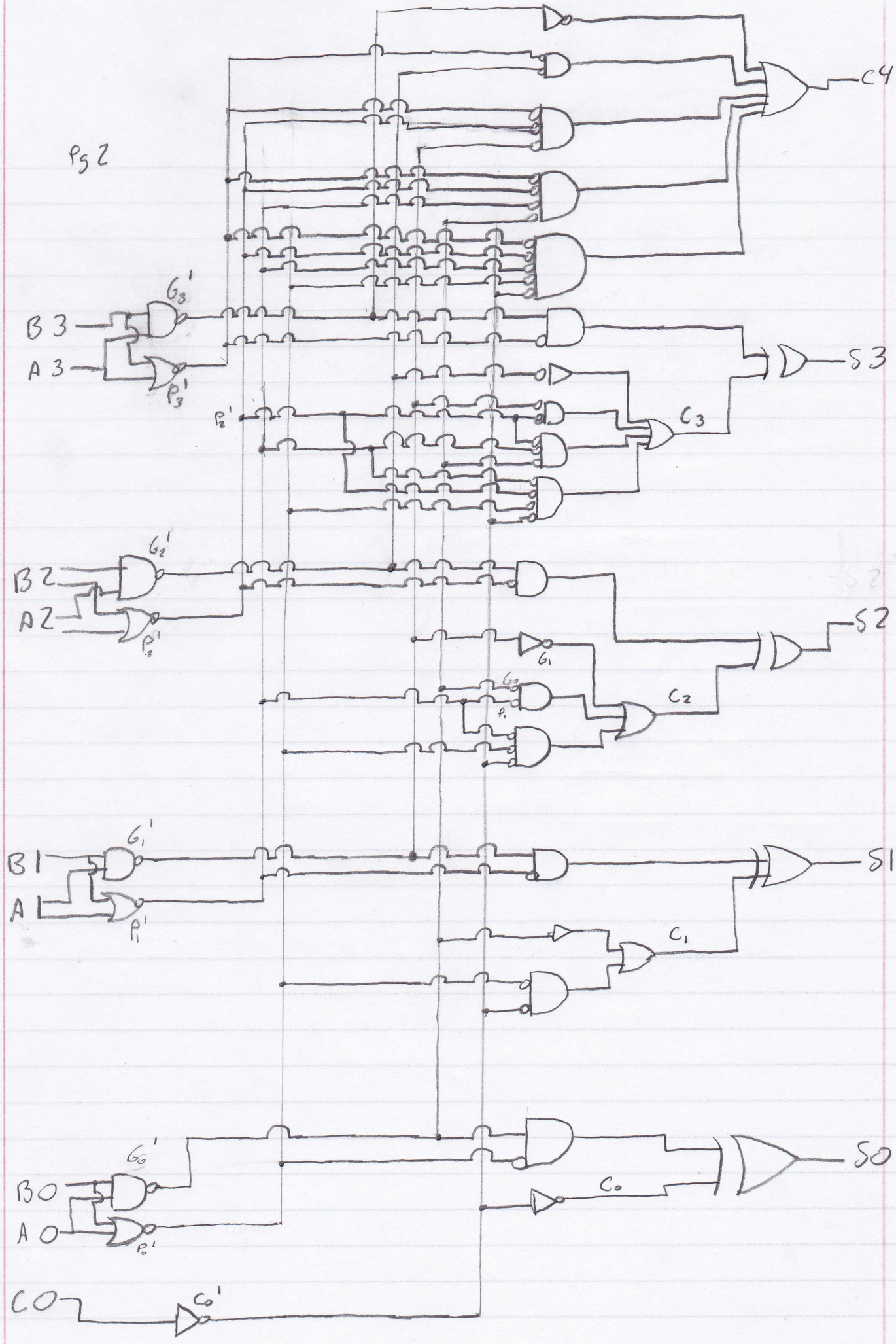
$30+20+20+10+10 =$ **90ns for S_3**

e.) C_4 AND, OR, INV., INV.

$20+20+10+10 =$ **60ns Delay for C_4**

#2) Draw Logic Circuit for the folbwing...

$$C_1 = g_0 + (P_0 C_0)$$
$$C_2 = g_1 + (P_1 g_0) + (P_1 P_0 C_0)$$
$$C_3 = g_2 + (P_2 g_1) + (P_2 P_1 g_0) + (P_2 P_1 P_0 C_0)$$
$$C_4 = g_3 + (P_3 g_2) + (P_3 P_2 g_1) + (P_3 P_2 P_1 g_0) + (P_3 P_2 P_1 P_0 C_0)$$


P5 2
C4
G3'
B 3
A 3
P3'
P2'
C3
S3
G2'
B 2
A 2
P2'
G1
G0
P1
C2
S2
G1'
B 1
A
P1'
C1
S1
G0'
B 0
A 0
P0'
C0
S0
C0
C0'

#3) Determine T_{pd} for Circuit designed in problem #2
- Inv, NAND, NOR = 10ns
- AND, OR = 20ns
- XOR = 30ns

a.) S_0 → XOR, AND, Inv., NOR
$30 + 20 + 10 + 10 =$ **70ns Delay for S_0**

b.) S_1 → XOR, OR, AND, Inv, Inv
$30 + 20 + 20 + 10 + 10 =$ **90ns Delay S_1**

c.) S_2 → XOR, OR, AND, Inv, Inv
$30 + 20 + 20 + 10 + 10 =$ **90ns S_2**

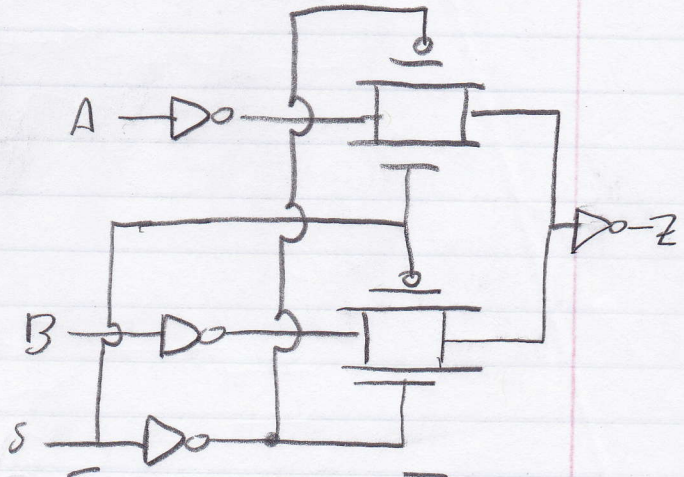
d.) S_3 → XOR, OR, AND, Inv, Inv
$30 + 20 + 20 + 10 + 10 =$ **90ns S_3**

e.) C_4 → OR, AND, Inv, Inv
$20 + 20 + 10 + 10 =$ **60ns for C_4**

#4) Textbook Problems:

[6.68]

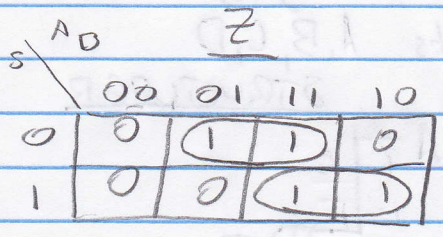
A	B	S	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



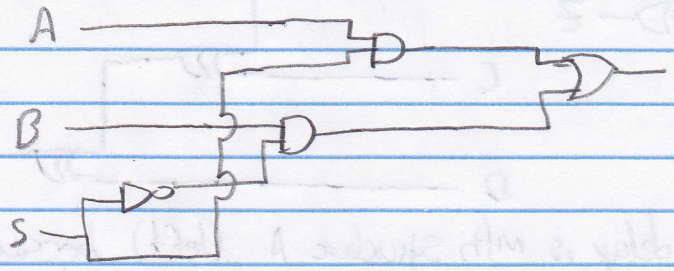
When S = 0, Z = B
When S = 1, Z = A

Pg 4

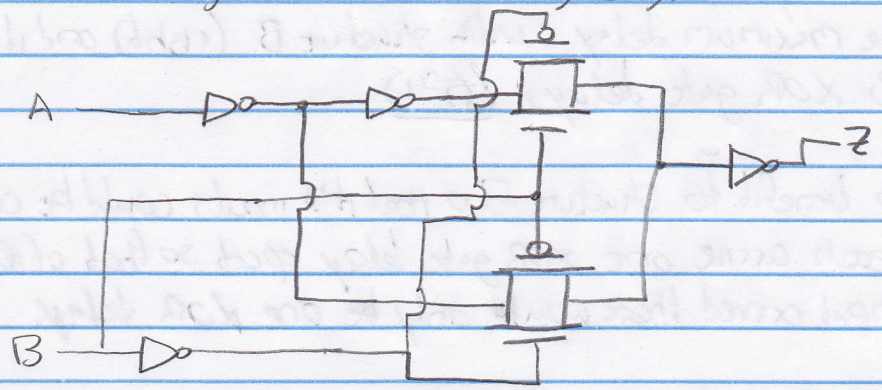
(S=0, Z=B S=1, Z=A)



$Z = (BS') + (AS)$



[6.69] Logic function for following diagram



When B=0, 2nd transmission gate is flowing and Z = A
When B=1, 1st transmission gate is flowing and Z = A'

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

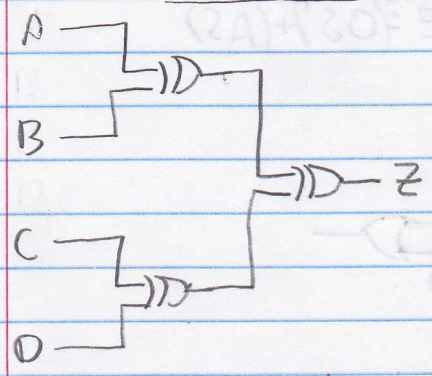
B=0, Z=A
B=1, Z=A'

$A \oplus B$

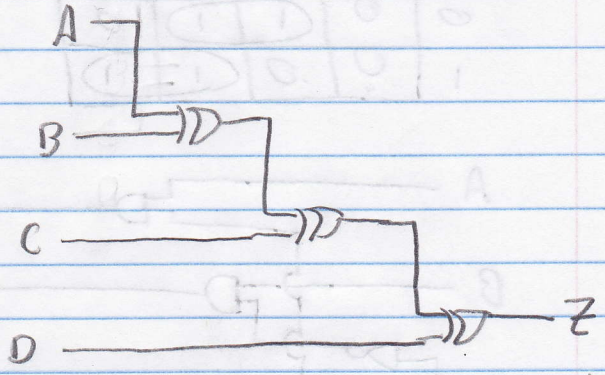
[6.82] 2^n inputs → $2^n - 1$ XOR gates

- Say there are four inputs A, B, C, D

STRUCTURE A



STRUCTURE B



- The minimum delay is with structure A (left) because it's inputs are balanced so there are only 2 or $n/2$ XOR gate delays
- The maximum delay is with structure B (right) and it has 3 XOR gate delays $(n-1)$

- The benefit to structure B is that it's inputs could be arranged to each arrive one XOR gate delay apart so that after the D input arrived there would only be one XOR delay.

[6.100] Logic Expression for S3... $g_i = X_i Y_i$ $p_i = X_i + Y_i$

→ $(B3 \cdot A3)'(B3 + A3) \oplus C_3$ (zero)

$C_3 = p_2 \cdot (g_2 + p_1) \cdot (g_2 + g_1 + p_0) \cdot (g_2 + g_1 + g_0 + C_0)$

→ $C_3 = (A2+B2)(A2B2+A1+B1)(A2B2+A1B1+A0+B0)(A2B2+A1B1+A0B0)$

$$S3 = (B3A3)'(B3+A3) \oplus \ldots$$
$$\ldots (A2+B2)(A2B2+A1+B1)(A2B2+A1B1+A0+B0)(A2B2+A1B1+A0B0)$$

$S3 = A3 \oplus B3 \oplus C3$

P. 5

→ compared to binary addition

$C_3 = P_2 \cdot (G_2 + C_2)$ $C_2 = P_1 \cdot (G_1 + C_1)$ $C_1 = P_0 G_0$

	A_3	A_2	A_1	A_0
+	B_3	B_2	B_1	B_0
			$G_2 \oplus A_1 \oplus B_1$	$A_0 \oplus B_0$

→ $A_0 B_0 = G_0$ → $P_0 = A_0 + B_0$

→ $G_1 = A_1 B_1$ → $C_0 = ZERO$

→ $P_1 = A_1 + B_1$

→ $G_2 = A_2 B_2$ $S_3 = A_3 \oplus B_3 \oplus (P_2 \cdot (G_2 + C_2))$

→ $P_2 = A_2 + B_2$

$S_3 = (A_2 + B_2) \cdot (A_2 B_2 + A_1 + B_1)(A_2 B_2 + A_1 B_1 + A_0 + B_0)$
$(A_2 B_2 + A_1 B_1 + A_0 B_0) \oplus A_3 \oplus B_3$ ✓