

Brian Faure DLD Hw #5 Due Oct. 21, 2014 RUId: 150003563

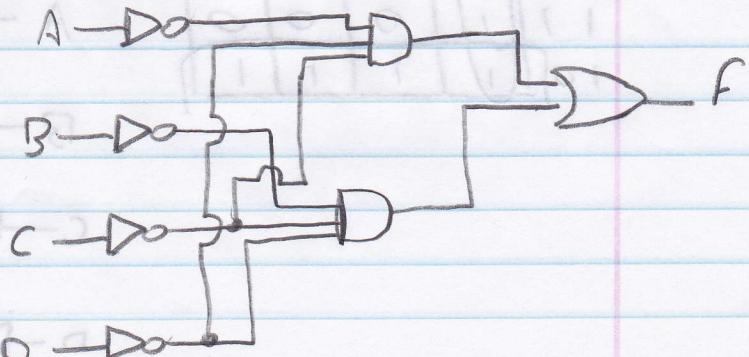
[3.11]

	A	B	C	D	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Z
0	0	0	0	0	0	1	0	1	0	1	0	1	1
1	0	0	0	1	0	1	0	1	1	1	0	0	0
2	0	0	1	0	0	0	1	0	1	0	0	1	0
3	0	0	1	1	0	1	0	1	1	0	1	0	0
4	0	1	0	0	0	1	1	0	0	1	0	1	1
5	0	1	0	1	0	1	0	1	1	1	0	0	0
6	0	1	1	0	0	0	1	1	0	0	0	1	0
7	0	1	1	1	0	1	1	0	1	0	1	0	0
8	1	0	0	0	1	0	0	1	0	1	0	1	0
9	1	0	0	1	1	0	0	1	1	0	0	1	0
10	1	0	1	0	1	0	1	0	0	1	1	0	0
11	1	0	1	1	1	0	0	1	1	0	1	0	0
12	1	1	0	0	1	0	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	0	1	0	0	0	0
14	1	1	1	0	1	0	1	0	0	0	1	1	0
15	1	1	1	1	1	0	1	0	1	0	1	0	0

$$Z = Q_2 Q_6 Q_4' Q_1' \quad F = \sum_{ABC} (0, 4, 8)$$

AB	CD
00	00011110
01	00010000
11	00000000
10	00000000

$$F = A'C'D + B'C'D'$$



Pg 2 INR 1105 15.60 w/o 24 w/o Q10 w/o Q11

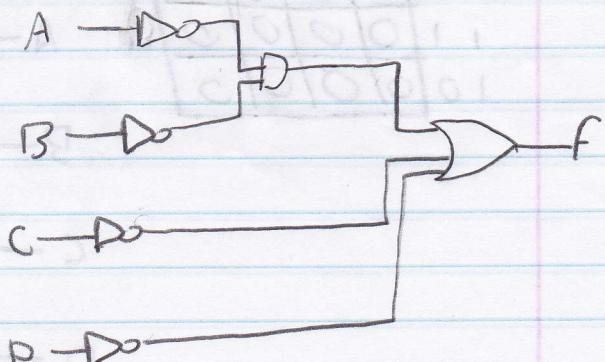
[3,12]	A	B	C	D	<u>Q₁</u>	<u>Q₂</u>	<u>Q₃</u>	<u>Q₄</u>	<u>Q₅</u>	<u>Q₆</u>	<u>Q₇</u>	<u>Q₈</u>	Z	
0	0	0	0	0	0	1	0	1	0	1	0	1	0	1
1	0	0	0	1	0	1	0	1	0	1	1	0	0	1
2	0	0	1	0	0	0	0	0	1	1	0	0	1	0
3	0	0	1	1	0	0	1	0	1	0	0	1	0	0
4	0	1	0	0	0	1	0	1	0	0	1	0	1	1
5	0	1	0	1	0	1	1	1	0	0	1	1	0	1
6	0	1	1	0	0	0	1	0	0	1	0	0	1	1
*7	0	1	1	1	0	0	1	1	0	1	0	1	0	0
8	1	0	0	0	1	0	0	0	1	0	0	1	0	1
9	1	0	0	1	0	0	0	1	0	1	1	0	0	1
10	1	0	1	0	1	0	0	1	0	1	0	0	1	1
*11	1	0	1	1	0	1	0	0	1	0	1	0	0	1
12	1	1	0	0	1	0	1	0	0	1	0	1	1	1
13	1	1	0	1	0	0	1	0	0	1	1	0	1	1
14	1	1	1	0	1	1	0	1	0	1	0	0	1	1
*15	1	1	1	1	0	1	0	1	0	1	0	1	0	0

$$F = \sum_{ABCD} (0, 1, 2, 3, 4, 5, 6, 8, 9, 10, 12, 13, 14)$$

AB

CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	0	0	0
10	1	1	1	1

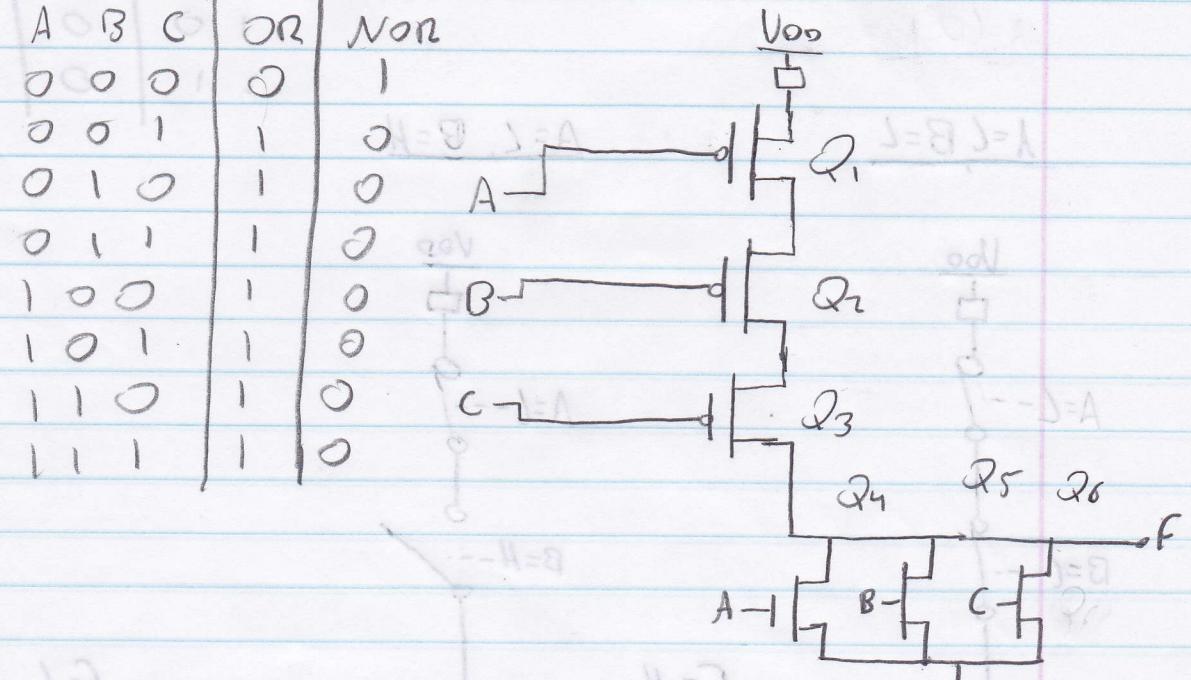
$$F = A'B' + D' + C'$$



Pg 31 | 8 A

[3.13] 3-input CMOS NOR gate \rightarrow 

A	B	C	OR	NOR
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0



A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	F
0	0	0	1	1	1	0	0	0	1
0	0	1	1	1	0	0	0	1	0
0	1	0	1	0	1	0	1	0	0
0	1	1	1	0	0	0	1	1	0
1	0	0	0	1	1	1	0	0	0
1	0	1	0	1	0	1	0	1	0
1	1	0	0	0	1	1	1	0	0
1	1	1	0	0	0	1	0	1	0

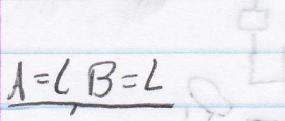
Pg 4

[3.14]

Switch network for 2-input CMOS nor gate

A	B	Not	Or
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

$$A = L \quad B = L$$



$$A = L, B = H$$



$$\begin{array}{c} V_{DD} \\ \text{---} \\ | \\ \text{---} \\ A = L \\ | \\ \text{---} \\ | \\ \text{---} \\ B = L \end{array}$$

$$A = L - -$$

$$B = L - -$$

$$\begin{array}{c} F = H \\ \text{---} \\ | \\ \text{---} \\ A = L \\ | \\ \text{---} \\ | \\ \text{---} \\ B = L \end{array}$$

$$A = H \quad B = L$$

$$\begin{array}{c} V_{DD} \\ \text{---} \\ | \\ \text{---} \\ A = H \\ | \\ \text{---} \\ | \\ \text{---} \\ B = L \end{array}$$

$$A = H - -$$

$$B = L - -$$

$$F = L$$

$$A = H - -$$

$$B = L - -$$

$$A = H \quad B = L$$

$$A = H - -$$

$$B = L - -$$

$$F = L$$

$$\begin{array}{c} V_{DD} \\ \text{---} \\ | \\ \text{---} \\ A = L \\ | \\ \text{---} \\ | \\ \text{---} \\ B = H \end{array}$$

$$A = L - -$$

$$B = H - -$$

$$F = L$$

$$\begin{array}{c} A = H \\ | \\ \text{---} \\ | \\ \text{---} \\ B = H \end{array}$$

$$A = H - -$$

$$B = H - -$$

$$F = L$$

$$A = H - -$$

$$B = H - -$$

$$A = H \quad B = H$$

$$A = H - -$$

$$B = H - -$$

$$F = L$$

$$A = H - -$$

$$B = H - -$$

$$A = H \quad B = H$$

$$A = H - -$$

$$B = H - -$$

$$F = L$$

$$A = H - -$$

$$B = H - -$$

$$A = H \quad B = H$$

$$A = H - -$$

$$B = H - -$$

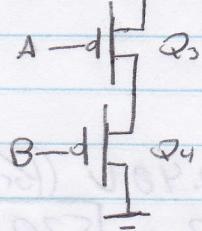
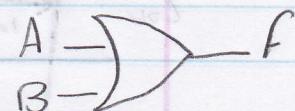
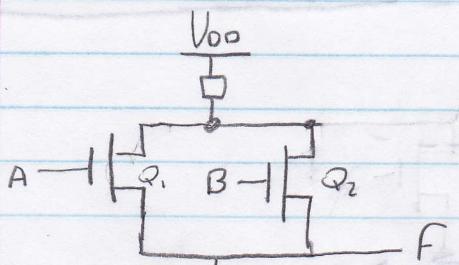
$$F = L$$

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[3.15]

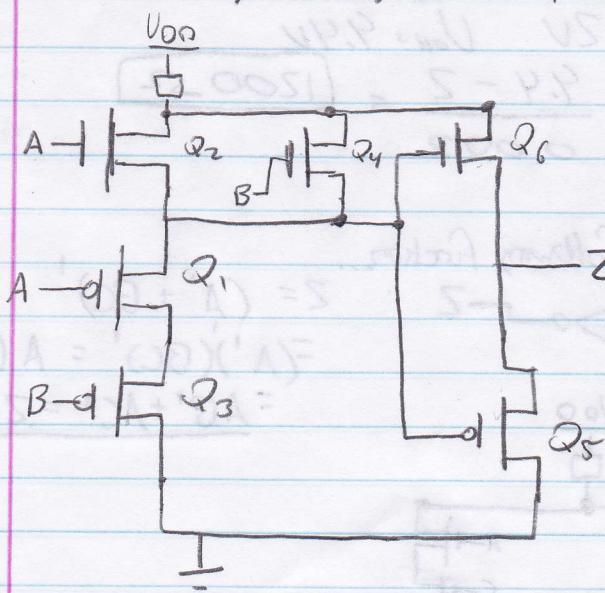
Circuit Diagram, Function Table, logic symbol (MOS OR gate)

A	B	OR
0	0	0
0	1	1
1	0	1
1	1	1



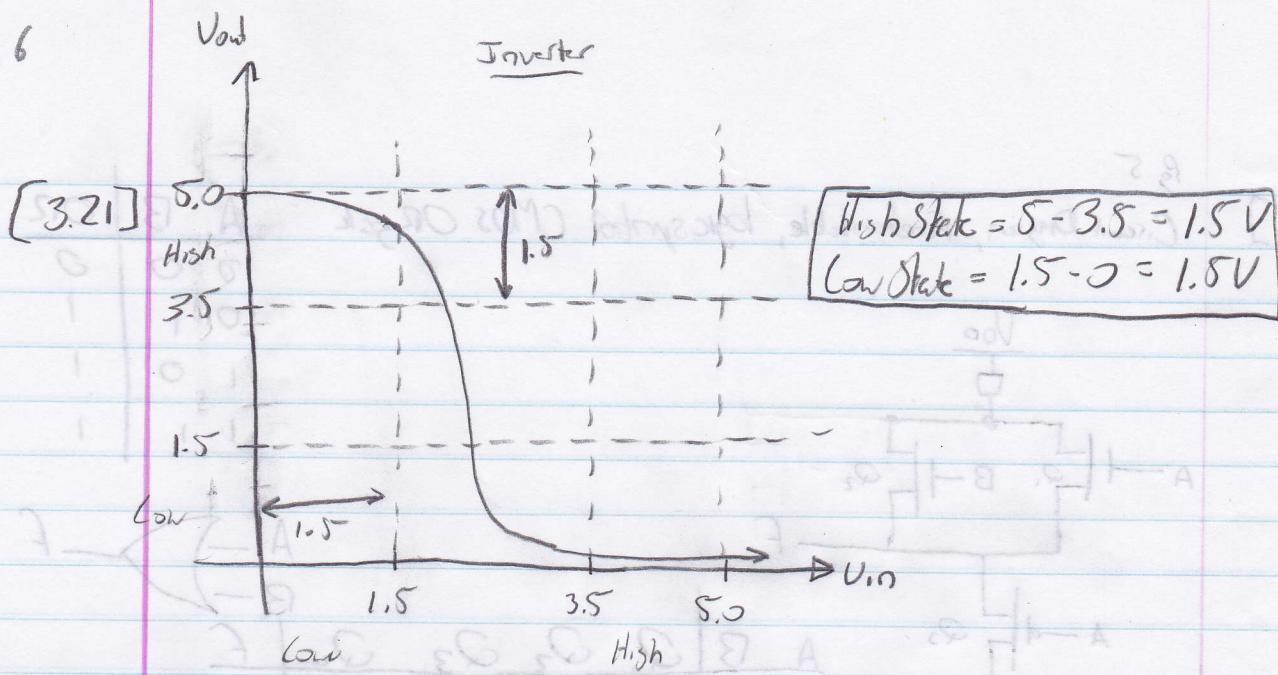
A	B	Q ₁	Q ₂	Q ₃	Q ₄	F
0	0	0	0	1	1	0
0	1	0	1	1	0	1
1	0	1	0	0	1	1
1	1	1	1	0	0	1

Now same style as Fig 3-19 (All mosfets become pmos & vice versa)



A	B	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	F
0	0	1	0	1	0	1	0	0
0	1	1	0	0	1	0	1	1
1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	1

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[3.40] $V_{CEO} = 2V \quad I_{CEO} = 0.005 \quad V_{OL} = 0.40V$ (~~For TA & Prof~~)

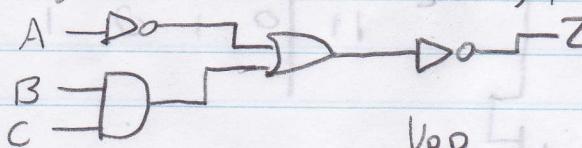
$$R = \frac{V_{CC} - V_{OL} - V_{CEO}}{I_{CEO}} = \frac{5 - 0.40 - 2}{0.005} = 520\Omega$$

$V_{CC} = 5V$

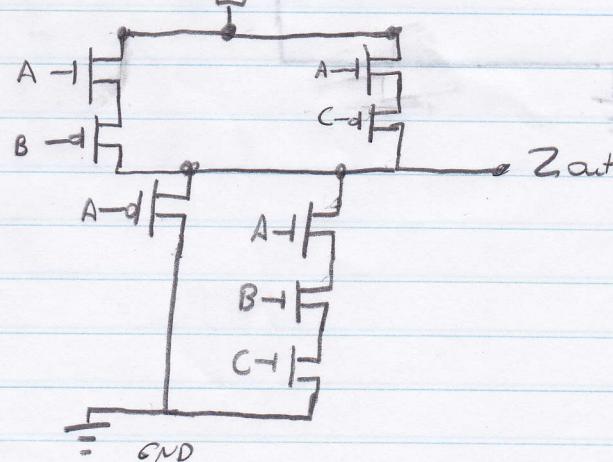
[3.41] $I_{CEO} = 0.002A \quad V_{CEO} = 2V \quad V_{OH} = 9.4V$

$$R = \frac{V_{OH} - V_{CEO}}{I_{CEO}} = \frac{9.4 - 2}{0.002} = 1200\Omega$$

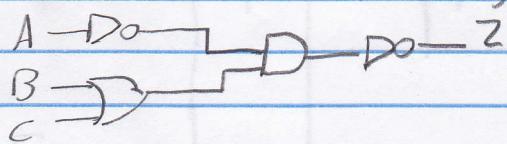
[3.59] Design CMOS circuit with following function..



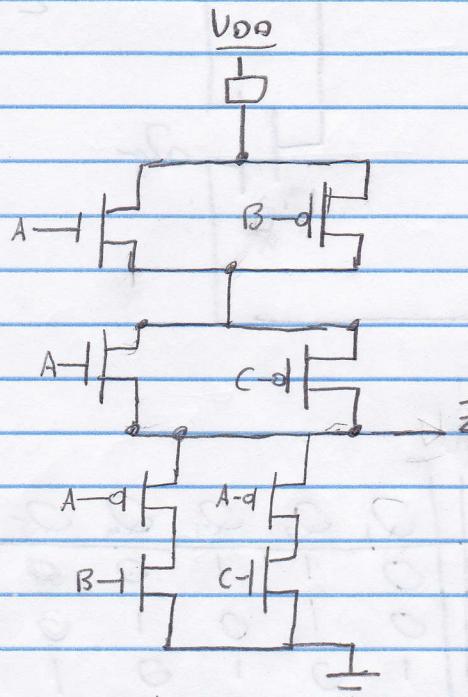
$$\begin{aligned} Z &= (A' + BC)' \\ &= (A')'(BC)' = A(B'C') \\ &= AB' + AC' = Z \end{aligned}$$



[3.60] Design CMOS circuit w/ following function...



$$\begin{aligned} Z &= (A'(B+C))' \\ &= (A'B + A'C)' \\ &= (A'B)'(A'C)' \\ &= (A+B')(A+C') = Z \end{aligned}$$



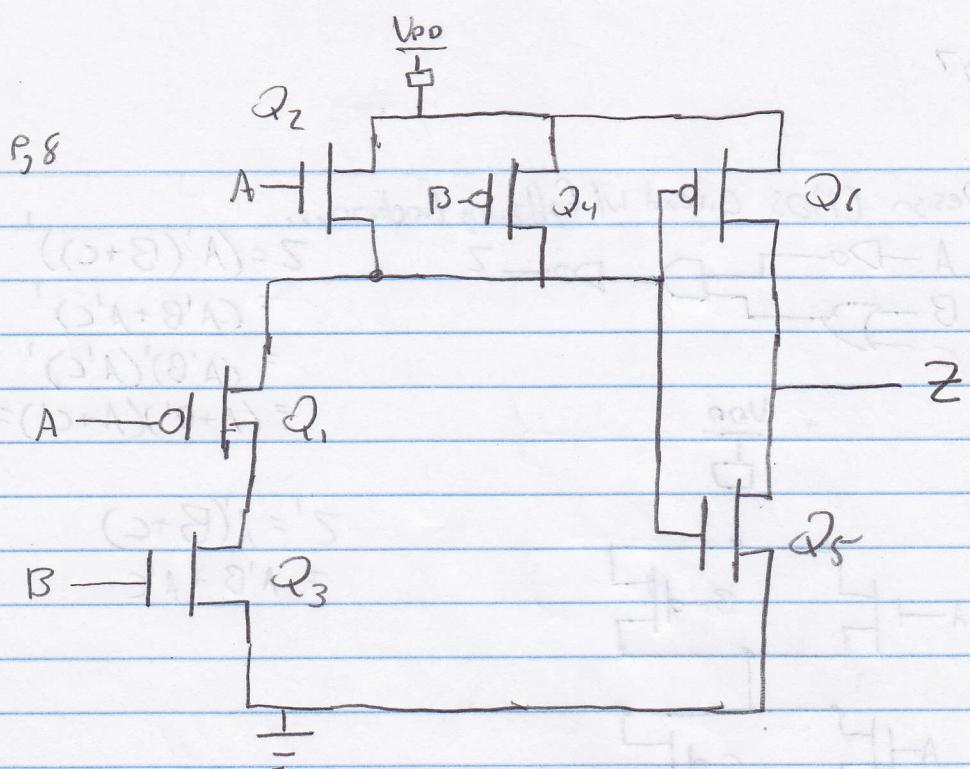
$$\begin{aligned} Z' &= A'(B+C) \\ &= A'B + A'C \end{aligned}$$

[3.61]

A	B	Z
0	0	0
0	1	1
1	0	0
1	1	0

$$Z = A'B \quad \text{Symbol} \rightarrow A \rightarrow \text{Do} \rightarrow D \rightarrow Z$$

A	B	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Z
00	0	1	0	0	1	1	0	0
01	1	1	0	1	0	0	1	1
10	0	0	1	0	1	1	0	0
11	1	0	1	1	0	1	0	0

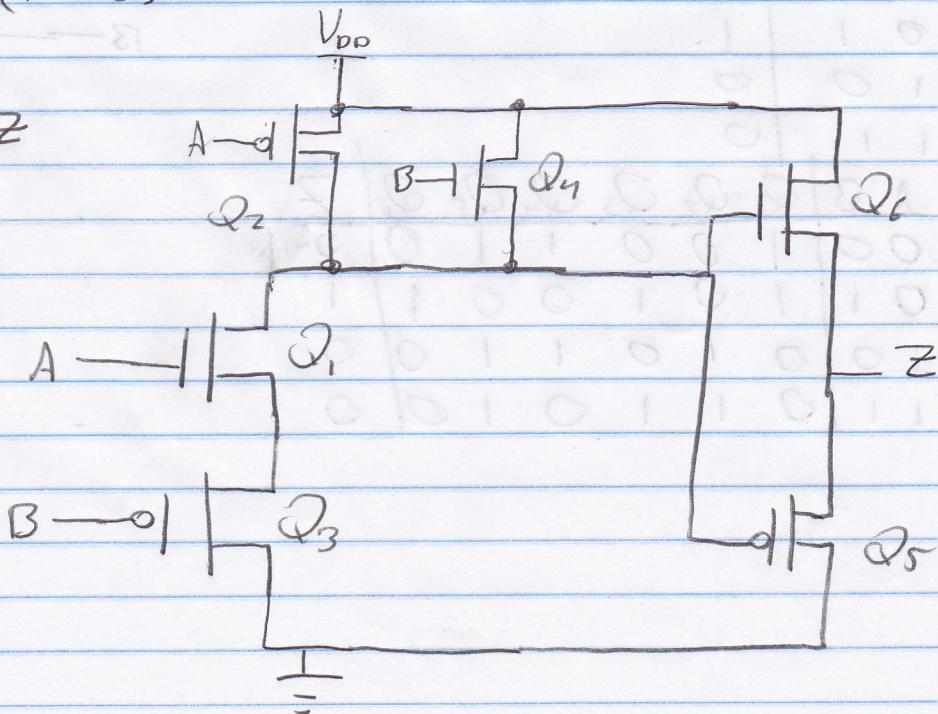
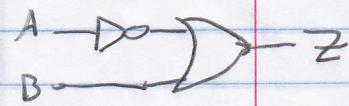


$$[3.12] \quad A \mid B \mid Z \quad Z = (AB')'$$

A	B	Z
0	0	1
0	1	1
1	0	0
1	1	1

A	B	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Z
0	0	0	0	1	1	0	1	1
0	1	0	1	0	1	0	1	1
1	0	1	0	1	0	1	0	0
1	1	1	0	1	0	1	0	0

$$Z = (A' + B)$$



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[3.78] $R = 390 \Omega$ $V_{out} = 0.3V$ $V_{OH} = 4.4V$ $I = \frac{4.4 - 1.6 - 0.3}{390}$

$V_{CEO} = 1.6V$

$I = 6.41mA$

$P = 16.024mW$