74AHC245; 74AHCT245

Octal bus transceiver; 3-state

Rev. 05 — 28 April 2009

Product data sheet

1. General description

The 74AHC245; 74AHCT245 is a high-speed Si-gate CMOS device.

The 74AHC245; 74AHCT245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74AHC245; 74AHCT245 features an output enable input (\overline{OE}), for easy cascading, and a send and receive direction control input (DIR).

OE controls the outputs so that the buses are effectively isolated.

2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - ◆ For 74AHC245: CMOS level
 - ◆ For 74AHCT245: TTL level
- ESD protection:
 - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
 - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

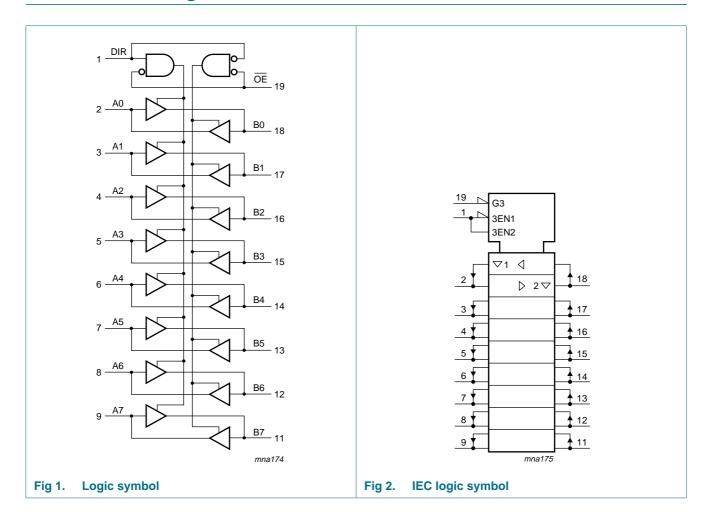
3. Ordering information

Table 1. Ordering information

Type number	Package									
	Temperature range	Name	Description	Version						
74AHC245D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads;	SOT163-1						
74AHCT245D			body width 7.5 mm							
74AHC245PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads;	SOT360-1						
74AHCT245PW			body width 4.4 mm							
74AHC245BQ	–40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced	SOT764-1						
74AHCT245BQ	_		very thin quad flat package; no leads; 20 terminals; body $2.5 \times 4.5 \times 0.85$ mm							



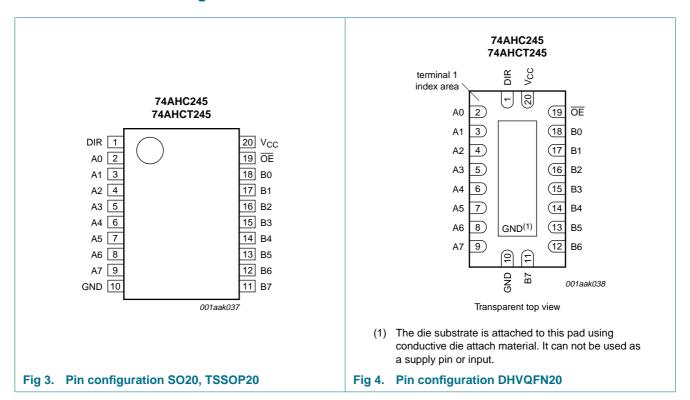
4. Functional diagram



© NXP B.V. 2009. All rights reserved.

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

74AHC AHCT245 5

Table 2.	i ili description	
Symbol	Pin	Description
DIR	1	direction control input
A0	2	data input/output
A1	3	data input/output
A2	4	data input/output
А3	5	data input/output
A4	6	data input/output
A5	7	data input/output
A6	8	data input/output
A7	9	data input/output
GND	10	ground (0 V)
B7	11	data input/output
B6	12	data input/output
B5	13	data input/output
B4	14	data input/output
B3	15	data input/output
B2	16	data input/output

Product data sheet Rev. 05 — 28 April 2009 3 of 16

Table 2. Pin description ...continued

Symbol	Pin	Description
B1	17	data input/output
В0	18	data input/output
ŌĒ	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function table[1]

Control		Input/output				
OE	DIR	An	Bn			
L	L	A = B	inputs			
L	Н	inputs	B = A			
Н	Χ	Z	Z			

[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_1 < -0.5 V$	<u>[1]</u> –20	-	mA
l _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> –20	+20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I _{GND}	ground current		–75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[2] -	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SO20 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Table 5.	Operating conditions					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74AHC2	45					
V_{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V
74AHCT	245					
V_{CC}	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC2	45									
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL} LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V	
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = -50 \mu A$; $V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu\text{A}; V_{CC} = 3.0 \text{V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		I_{O} = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
l _l	input leakage current	$V_1 = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to 5.5 V}$	-	-	0.1	-	1.0	-	2.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL};$ $V_O = V_{CC} \text{ or GND};$ $V_{CC} = 5.5 \text{ V}$	-	-	±0.25	-	±2.5	-	±10.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
Cı	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF
74AHCT	245									
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	8.0	-	0.8	-	0.8	V
V _{OH} HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$									
	output voltage	$I_{O} = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_O = 50 \mu A$	-	0	0.1	-	0.1	-	0.1	V
		$I_{O} = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	±0.25	-	±2.5	-	±10.0	μА
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
ΔI_{CC}	additional supply current	per input pin; $V_{I} = V_{CC} - 2.1 \text{ V};$ other pins at V_{CC} or GND; $I_{O} = 0 \text{ A}; V_{CC} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions			25 °C		-40 °C	-40 °C to +85 °C		to +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC2	45										
t _{pd}	propagation delay	An to Bn; Bn to An; see Figure 5	[2]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		$C_{L} = 15 \text{ pF}$		-	5.0	8.4	1.0	10.0	1.0	10.5	ns
		$C_L = 50 pF$		-	6.5	11.9	1.0	13.5	1.0	15.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		$C_{L} = 15 pF$		-	3.5	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50 pF$			5.0	7.5	1.0	8.5	1.0	9.5	ns
t _{en}	enable time	OE to An; OE to Bn; signal name DIR; see Figure 6	[3]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		C _L = 15 pF		-	6.5	13.2	1.0	15.5	1.0	16.5	ns
		$C_L = 50 pF$		-	9.0	16.7	1.0	19.0	1.0	21.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C _L = 15 pF		-	4.0	8.5	1.0	10.0	1.0	11.0	ns
		$C_L = 50 pF$		-	5.0	10.6	1.0	12.0	1.0	13.5	ns
t _{dis}	disable time	OE to An; OE to Bn; signal name DIR; see Figure 6	<u>[4]</u>								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		$C_{L} = 15 pF$		-	7.5	12.5	1.0	15.5	1.0	16.0	ns
		$C_L = 50 pF$		-	10.0	15.8	1.0	18.0	1.0	20.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		$C_L = 15 pF$		-	4.5	7.8	1.0	9.2	1.0	10.0	ns
		$C_L = 50 pF$		-	6.0	9.7	1.0	11.0	1.0	12.5	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	<u>[5]</u>	-	12	-	-	-	-	-	pF
74AHCT	245; V _{CC} = 4.	5 V to 5.5 V									
t _{pd}	propagation delay	An to Bn; Bn to An; see Figure 5	[2]								
		$C_L = 15 pF$		-	3.5	7.7	1.0	8.5	1.0	10.0	ns
		$C_L = 50 pF$		-	4.5	8.7	1.0	9.5	1.0	11.0	ns
t _{en}	enable time	OE to An; OE to Bn; signal name DIR; see Figure 6	[3]								
		C _L = 15 pF		-	5.0	13.8	1.0	15.0	1.0	17.5	ns
		$C_L = 50 pF$		-	6.0	14.8	1.0	16.0	1.0	18.5	ns
74AHC_AHCT24	45_5								© N	IXP B.V. 2009. All righ	nts reserved.

8 of 16

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C	
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{dis} disable time		OE to An; OE to Bn; signal name DIR; see Figure 6								
		$C_L = 15 pF$	-	5.0	14.4	1.0	15.5	1.0	18.0	ns
		C _L = 50 pF	-	6.0	15.4	1.0	16.5	1.0	19.5	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz};$ [5] $V_I = \text{GND to } V_{CC}$	-	15	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] t_{en} is the same as t_{PZL} and t_{PZH} .
- [4] t_{dis} is the same as t_{PLZ} and t_{PHZ} .
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz;

 $f_o = output frequency in MHz;$

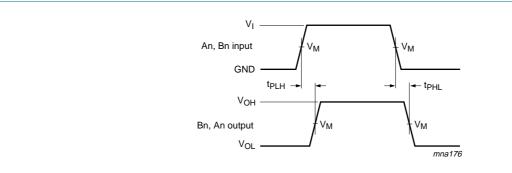
C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.

10.1 Waveforms



Measurement points are given in Table 8.

 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Input to output propagation delays

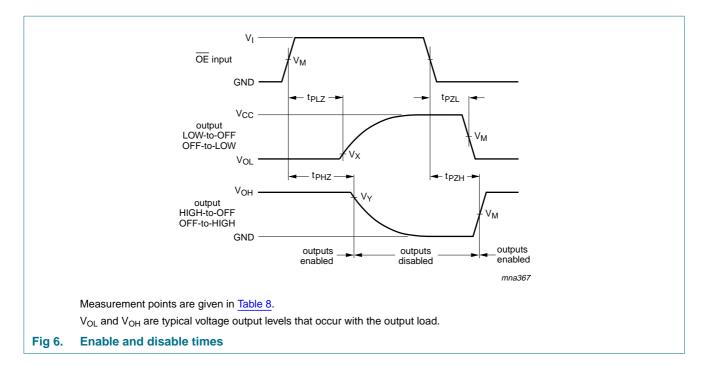
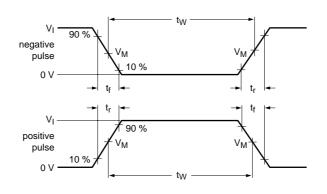
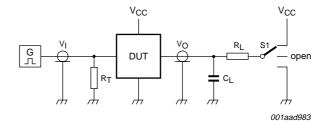


Table 8. Measurement points

Туре	Input	Output						
	V _M	V _M	V _X	V _Y				
74AHC245	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V _{OL} + 0.3 V	$V_{OH} - 0.3 V$				
74AHCT245	1.5 V	$0.5 \times V_{CC}$	V _{OL} + 0.3 V	$V_{OH} - 0.3 V$				





Test data is given in Table 9.

Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 7. Load circuitry for measuring switching times

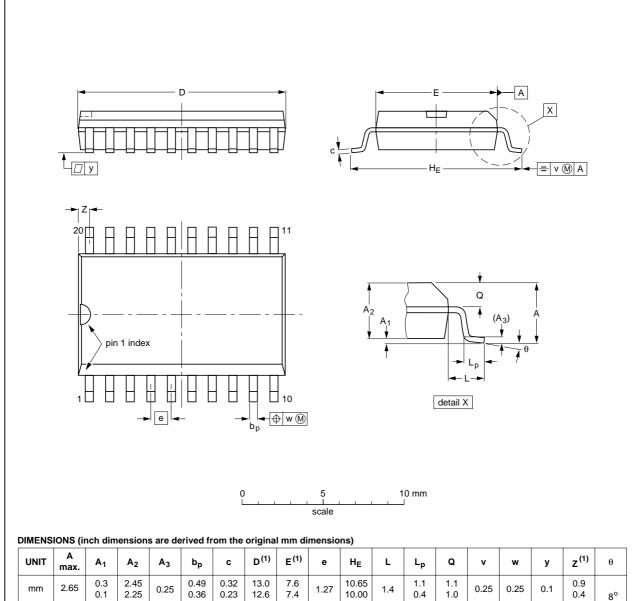
Table 9. Test data

Туре	Input		Load	Load		S1 position		
	VI	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
74AHC245	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}	
74AHCT245	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}	

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	C	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Ø	٧	w	у	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016		0.01	0.01	0.004	0.035 0.016	0°

Note

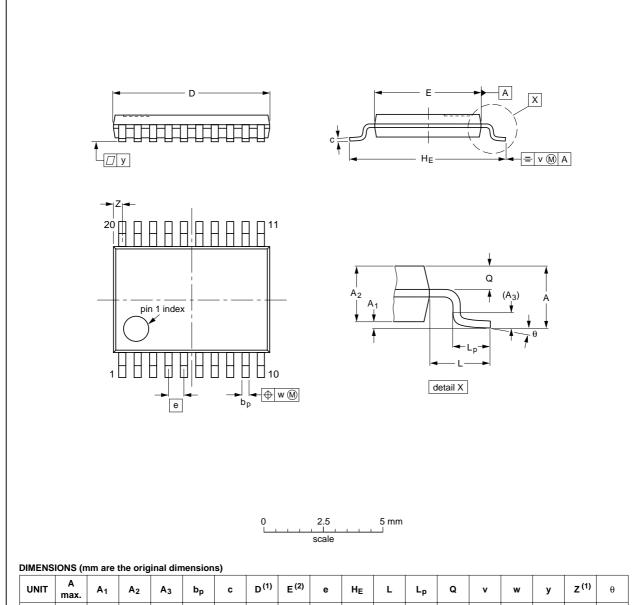
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT163-1	075E04	MS-013				99-12-27 03-02-19	

Fig 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

	REFER	EUROPEAN	ISSUE DATE			
IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
	MO-153				99-12-27 03-02-19	
-	IEC	IEC JEDEC		IEC JEDEC JEITA	IEC JEDEC JEITA PROJECTION	

Fig 9. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm SOT764-1

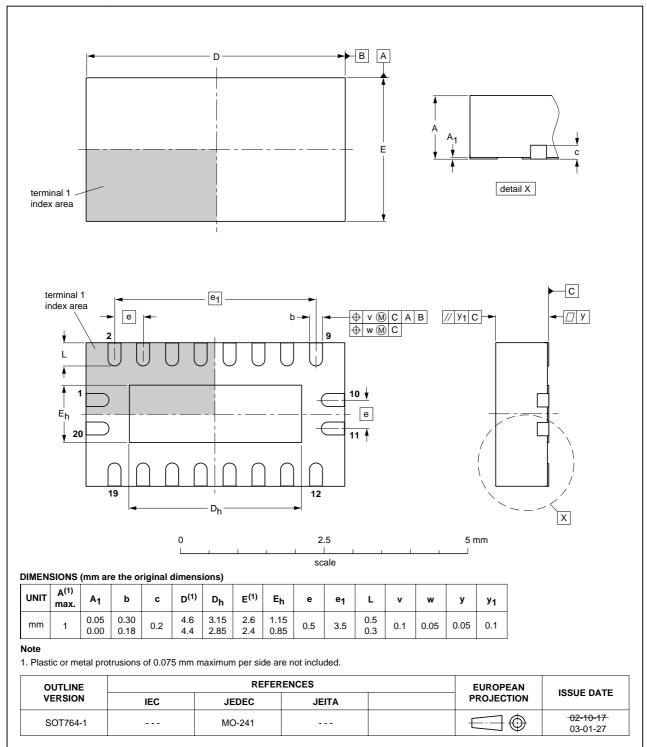


Fig 10. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT245_5	20090428	Product data sheet	-	74AHC_AHCT245_4
Modifications:	 Section 3: D 	HVQFN20 package added		
	Section 7: d	erating values added for DI	HVQFN20 package.	
	• <u>Section 11</u> :	outline drawing added for D	HVQFN20 package.	
74AHC_AHCT245_4	20080425	Product data sheet	-	74AHC_AHCT245_N_3
74AHC_AHCT245_N_3	20070925	Product data sheet	-	74AHC_AHCT245_2
74AHC_AHCT245_2	19990928	Product specification	-	74AHC_AHCT245_1
74AHC_AHCT245_1	19980921	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

14.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

14.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

15. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

16. Contents

1	General description
2	Features
3	Ordering information
4	Functional diagram 2
5	Pinning information 3
5.1	Pinning
5.2	Pin description
6	Functional description 4
7	Limiting values 4
8	Recommended operating conditions 5
9	Static characteristics 5
10	Dynamic characteristics
10.1	Waveforms
11	Package outline
12	Abbreviations14
13	Revision history
14	Legal information
14.1	Data sheet status
14.2	Definitions
14.3	Disclaimers
14.4	Trademarks15
15	Contact information
16	Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

