74AHC86; 74AHCT86

Quad 2-input EXCLUSIVE-OR gate Rev. 02 — 15 November 2007

Product data sheet

General description 1.

The 74AHC86; 74AHCT86 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74AHC86; 74AHCT86 provides a 2-input exclusive-OR function.

2. **Features**

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V_{CC}
- For 74AHC86 only: operates with CMOS input levels
- For 74AHCT86 only: operates with TTL input levels
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

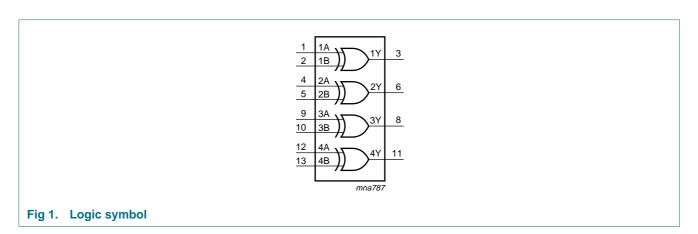
Ordering information 3.

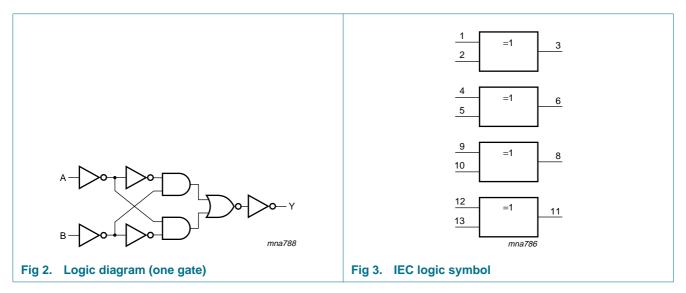
Table 1. **Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74AHC86D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads;	SOT108-1
74AHCT86D			body width 3.9 mm	
74AHC86PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1
74AHCT86PW			body width 4.4 mm	
74AHC86BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced	SOT762-1
74AHCT86BQ	_		very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85$ mm	



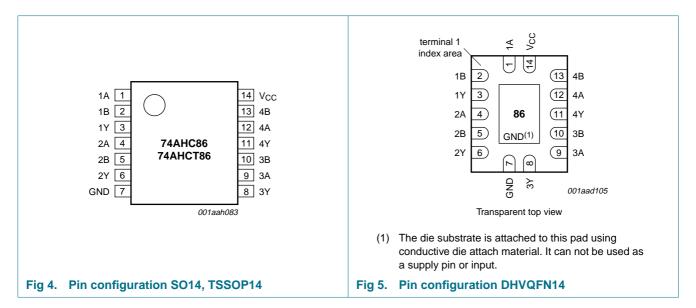
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data outputs
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input nA	Input nB	Output nY
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

[1] H = HIGH voltage level;L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

					-
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V}$	<u>[1]</u> –20	-	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> _	±20	mA
lo	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$			
	SO14 package		[2] -	500	mW
	TSSOP14 package		[3] _	500	mW
	DHVQFN14 package		<u>[4]</u> _	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC	86		74AHC	T86		Unit
			Min	Тур	Max	Min	Тур	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	0	-	5.5	V
V_{O}	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise	V_{CC} = 3.3 V \pm 0.3 V	-	-	100	-	-	-	ns/V
	and fall rate	$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	-	-	20	ns/V

^[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

^[3] Ptot derates linearly with 5.5 mW/K above 60 °C.

^[4] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
For type	74AHC86									
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	٧
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_{O} = -50 \mu\text{A}; V_{CC} = 2.0 \text{V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu\text{A}; V_{CC} = 3.0 \text{V}$	2.9	3.0	-	2.9	-	2.9	-	٧
		$I_O = -50 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	٧
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.8	-	3.70	-	٧
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
l _l	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Cı	input capacitance		-	3.0	10	-	10	-	10	pF
Co	output capacitance		-	4.0	-	-	-	-	-	pF
For type	74AHCT86									
V _{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_{O} = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_0 = -8.0 \text{ mA}$	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V

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Table 6. Static characteristics ...continued Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
II	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
Δl _{CC}	additional supply current	per input pin; $V_{I} = V_{CC} - 2.1 \text{ V; } I_{O} = 0 \text{ A;}$ other pins at V_{CC} or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance		-	3	10	-	10	-	10	pF
C _O	output capacitance		-	4.0	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics *GND = 0 V; For test circuit see Figure 7.*

Symbol	Parameter	Conditions			25 °C		–40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			N	/lin	Typ[1]	Max	Min	Max	Min	Max	
For type	74AHC86		ľ						'		
t _{pd}	propagation	nA, nB to nY; see Figure 6	[2]								
	delay	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$									
		C _L = 15 pF		-	4.8	11.0	1.0	13.0	1.0	14.0	ns
		C _L = 50 pF		-	6.8	14.5	1.0	16.5	1.0	18.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C _L = 15 pF		-	3.4	6.8	1.0	8.0	1.0	8.5	ns
		C _L = 50 pF			4.8	8.8	1.0	10.0	1.0	11.0	ns
C _{PD}	power dissipation capacitance	$C_L = 50 \text{ pF}; f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	[3]	-	10.0	-	-	-	-	-	pF

 Table 7.
 Dynamic characteristics ...continued

GND = 0 V; For test circuit see Figure 7.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C t	o +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
For type	74AHCT86		,								
t _{pd}	propagation	nA, nB to nY; see Figure 6	[2]								
•	delay	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$									
		C _L = 15 pF		-	3.4	6.9	1.0	8.0	1.0	9.0	ns
		$C_L = 50 pF$		-	4.9	8.8	1.0	10.0	1.0	11.0	ns
C_{PD}	power dissipation capacitance	$C_L = 50 \text{ pF}; f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	[3]	-	12.0	-	-	-	-	-	pF

- [1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz, f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms

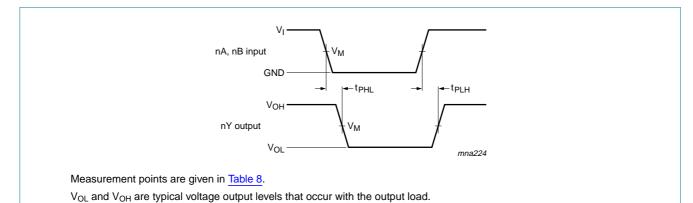
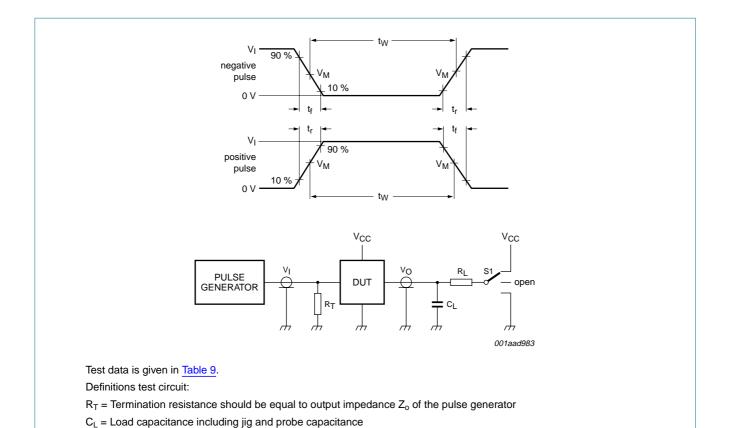


Fig 6. Propagation delay input (nA, nB) to output (nY)

Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74AHC86	0.5V _{CC}	0.5V _{CC}
74AHCT86	1.5 V	0.5V _{CC}



S1 = Test selection switch

Fig 7. Load circuitry for switching times

R_L = Load resistor

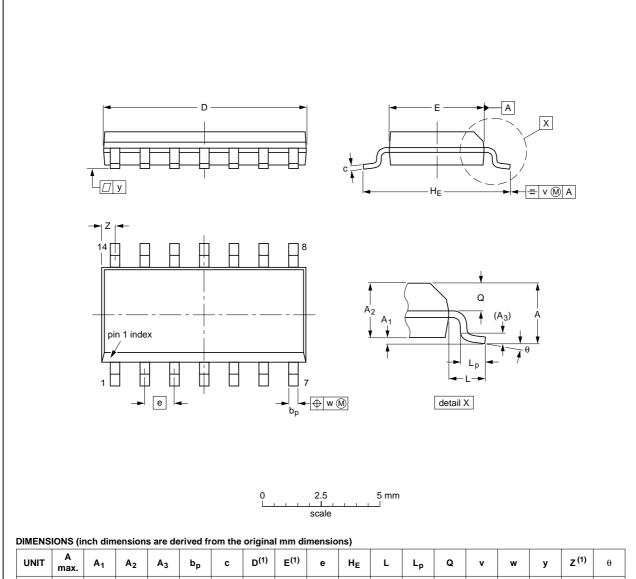
Table 9. Test data

Туре	Input		Load		S1 position		
	VI	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
74AHC86	V_{CC}	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}
74AHCT86	3.0 V	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	ø	v	w	у	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

Note

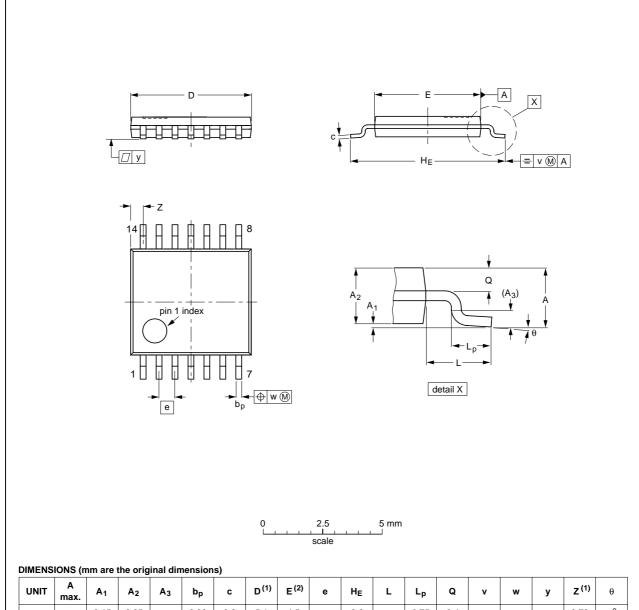
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



_																			
	UNIT	A max.	A ₁	A ₂	А3	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
	mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT402-1		MO-153			99-12-27 03-02-18	

Fig 9. Package outline SOT402-1 (TSSOP14)

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

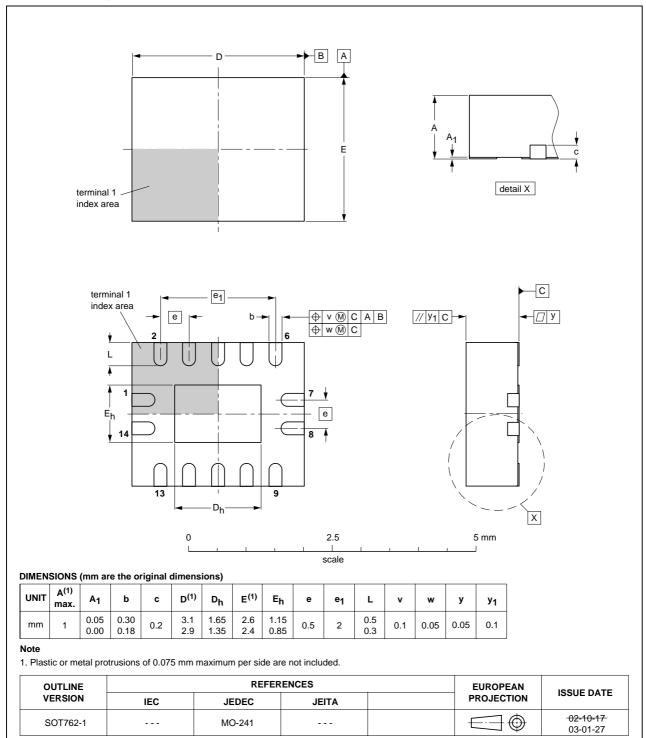


Fig 10. Package outline SOT762-1 (DHVQFN14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT86_2	20071115	Product data sheet	-	74AHC_AHCT86_1
Modifications:		f this data sheet has been NXP Semiconductors.	redesigned to comply v	vith the new identity
	 Legal texts h 	ave been adapted to the no	ew company name whe	ere appropriate.
	 Section 3: DI 	HVQFN14 package added.		
	• Section 7: de	erating values added for DH	IVQFN14 package.	
	• <u>Section 12</u> : c	outline drawing added for D	HVQFN14 package.	
74AHC_AHCT86_1	19990917	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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