# 74AHC377; 74AHCT377

Octal D-type flip-flop with data enable; positive-edge trigger

Rev. 02 — 12 June 2008 Product data sheet

### 1. General description

The 74AHC377; 74AHCT377 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC377; 74AHCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock input (CP) loads all flip-flops simultaneously when the data enable input ( $\overline{E}$ ) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. The  $\overline{E}$  input is only required to be stable one set-up time prior to the LOW-to-HIGH transition for predictable operation.

For versions associated with the 74AHC377; 74AHCT377, refer to the following:

- For the master reset version, see 74AHC273; 74AHCT273
- For the transparent latch version, see 74AHC373; 74AHCT373
- For the 3-state version, see 74AHC374; 74AHCT374

### 2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V<sub>CC</sub>
- Ideal for addressable register applications
- Data enable for address and data synchronization
- Eight positive-edge triggered D-type flip-flops
- Input levels:
  - ◆ For 74AHC377: CMOS level
  - ◆ For 74AHCT377: TTL level
- ESD protection:
  - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

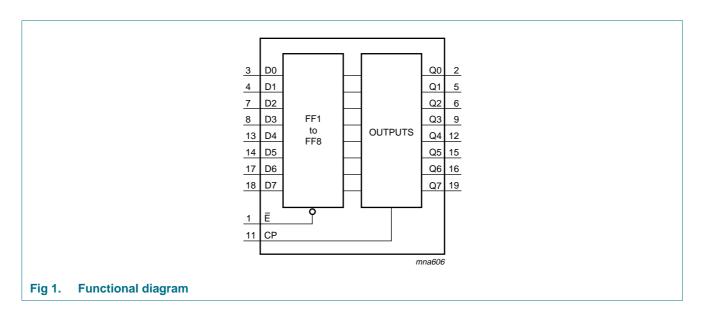


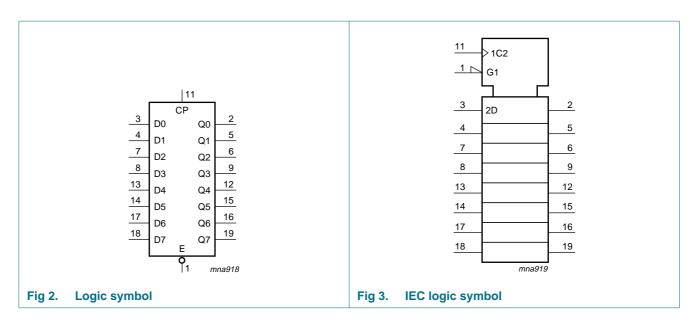
## 3. Ordering information

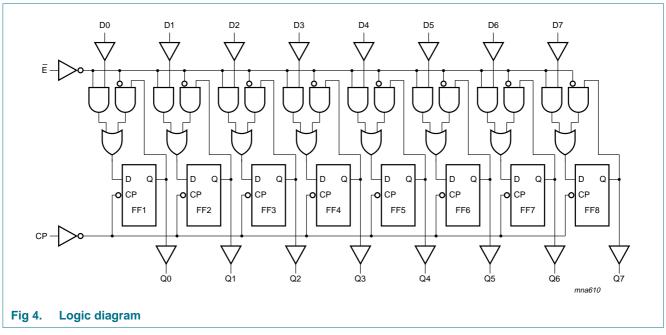
Table 1. Ordering information

Type number	Package								
	Temperature range Name		Description	Version					
74AHC377									
74AHC377D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1					
74AHC377PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1					
74AHCT377									
74AHCT377D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1					
74AHCT377PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1					

## 4. Functional diagram

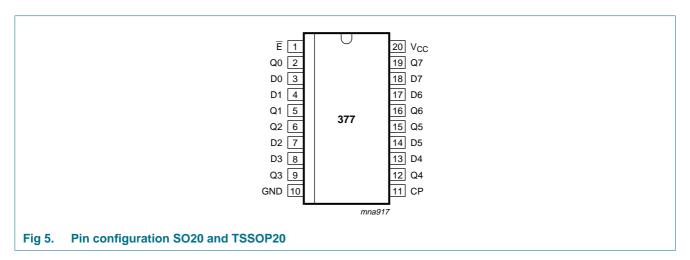






## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Ē	1	data enable input (active LOW)
Q0	2	flip-flop output
D0	3	data input
D1	4	data input
Q1	5	flip-flop output
Q2	6	flip-flop output
D2	7	data input
D3	8	data input
Q3	9	flip-flop output
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
Q4	12	flip-flop output
D4	13	data input
D5	14	data input
Q5	15	flip-flop output
Q6	16	flip-flop output
D6	17	data input
D7	18	data input
Q7	19	flip-flop output
$V_{CC}$	20	supply voltage

## 6. Functional description

Table 3. Function table [1]

Operating mode	Control		Input	Output
	Ē	СР	Dn	Qn
Load 1	I	1	h	Н
Load 0	I	1	I	L
Hold (do nothing)	h	1	X	no change
	Н	X	X	no change

<sup>[1]</sup> H = HIGH voltage level;

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;

L = LOW voltage level;

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;

↑ = LOW-to-HIGH CP transition;

X = don't care.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_{I}$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_1 < -0.5 \text{ V}$	<u>[1]</u> –20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	[ <u>1]</u> –20	+20	mA
$I_{O}$	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
$I_{CC}$	supply current		-	+75	mA
$I_{\text{GND}}$	ground current		<b>-75</b>	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[2] _	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup> For SO20 packages: above 70 °C the value of  $P_{tot}$  derates linearly at 8 mW/K. For TSSOP20 packages: above 60 °C the value of  $P_{tot}$  derates linearly at 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5.** Operating conditions

	operating containents					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74AHC3	77					
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	$V_{CC}$	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V
74AHCT	377					
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	$V_{CC}$	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V

### 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC3	77					'				
$V_{IH}$	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
011	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_{O} = -50 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_{O} = -50 \mu A; V_{CC} = 3.0 V$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_{O}$ = 8.0 mA; $V_{CC}$ = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	1
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
Cı	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
74AHCT	377									
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	8.0	-	0.8	-	0.8	V
0	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_O = -50 \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_0 = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	$V_I = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to 5.5 V}$	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
Δl <sub>CC</sub>	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other pins at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	–40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC3	77								•	
t <sub>pd</sub>	propagation	CP to Qn; see Figure 6								
	delay	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		C <sub>L</sub> = 15 pF	-	5.6	12.8	1.0	15.0	1.0	16.0	ns
		C <sub>L</sub> = 50 pF	-	8.0	16.0	1.0	18.0	1.0	20.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		C <sub>L</sub> = 15 pF	-	3.9	9.0	1.0	10.5	1.0	11.5	ns
		C <sub>L</sub> = 50 pF	-	5.6	10.5	1.0	12.0	1.0	13.5	ns
f <sub>max</sub>	maximum	see Figure 6								
	frequency	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		C <sub>L</sub> = 15 pF	80	125	-	70	-	70	-	MHz
		C <sub>L</sub> = 50 pF	50	75	-	45	-	45	-	MHz
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		C <sub>L</sub> = 15 pF	125	175	-	110	-	110	-	MHz
		C <sub>L</sub> = 50 pF	85	120	-	75	-	75	-	MHz
$t_W$	pulse width	CP HIGH or LOW; see Figure 6								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
t <sub>su</sub>	set-up time	Dn, E to CP; see Figure 7								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	4.5	-	-	4.5	-	4.5	-	ns
t <sub>h</sub>	hold time	Dn, E to CP; see Figure 7								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	-	-	1.5	-	1.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	ns
$C_{PD}$	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ [3]	-	20	-	-	-	-	-	pF

#### Table 7. **Dynamic characteristics** ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHCT	377; V <sub>CC</sub> = 4.5	5 V to 5.5 V								
t <sub>pd</sub>	propagation delay	CP to Qn; see Figure 6 [2]								
		C <sub>L</sub> = 15 pF	-	4.0	9.0	1.0	10.5	1.0	11.5	ns
		$C_L = 50 pF$	-	5.7	10.5	1.0	12.0	1.0	13.5	ns
max	maximum frequency	see Figure 6								
		C <sub>L</sub> = 15 pF	90	140	-	80	-	80	-	MHz
		$C_L = 50 pF$	85	130	-	75	-	75	-	MHz
t <sub>W</sub>	pulse width	CP HIGH or LOW; see Figure 6	5.0	-	-	5.0	-	5.0	-	ns
t <sub>su</sub>	set-up time	Dn, $\overline{E}$ to CP; see Figure 7	4.5	-	-	4.5	-	4.5	-	ns
t <sub>h</sub>	hold time	Dn, $\overline{E}$ to CP; see Figure 7	2.0	-	-	2.0	-	2.0	-	ns
$C_{PD}$	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ 3	-	23	-	-	-	-	-	pF

<sup>[1]</sup> Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3 \text{ V}$  and  $V_{CC} = 5.0 \text{ V}$ ).

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$$
 where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

**Product data sheet** 

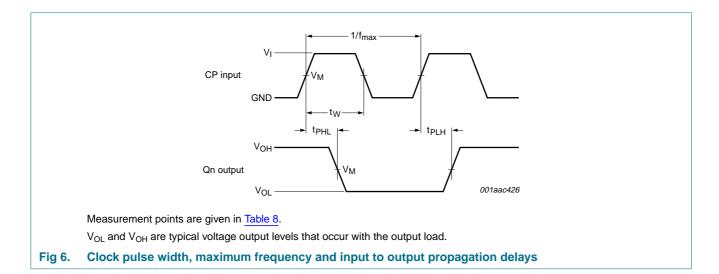
N = number of inputs switching;

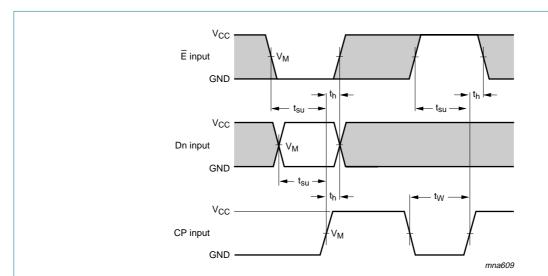
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

9 of 16

<sup>[2]</sup>  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

### 11. Waveforms





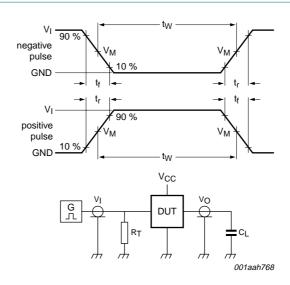
Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 7. Data set-up and hold times

Table 8. Measurement points

Туре	Input	Output	
	V <sub>M</sub>	V <sub>M</sub>	
74AHC377	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	
74AHCT377	1.5 V	$0.5 \times V_{CC}$	



Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $C_L$  = load capacitance including jig and probe capacitance.

Fig 8. Load circuitry for measuring switching times

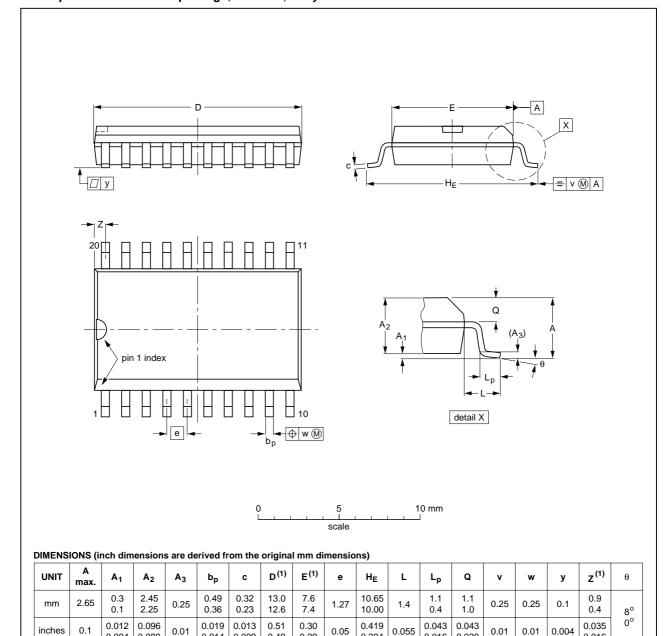
Table 9. Test data

Туре	Input		Load	Test	
	VI	t <sub>r</sub> , t <sub>f</sub>	CL		
74AHC377	V <sub>CC</sub>	≤ 3.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>	
74AHCT377	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>	

## 12. Package outline

#### SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



## Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014

0.009

OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE	
	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT163-1	075E04	MS-013			<del>99-12-27</del> 03-02-19

0.394

0.039

0.016

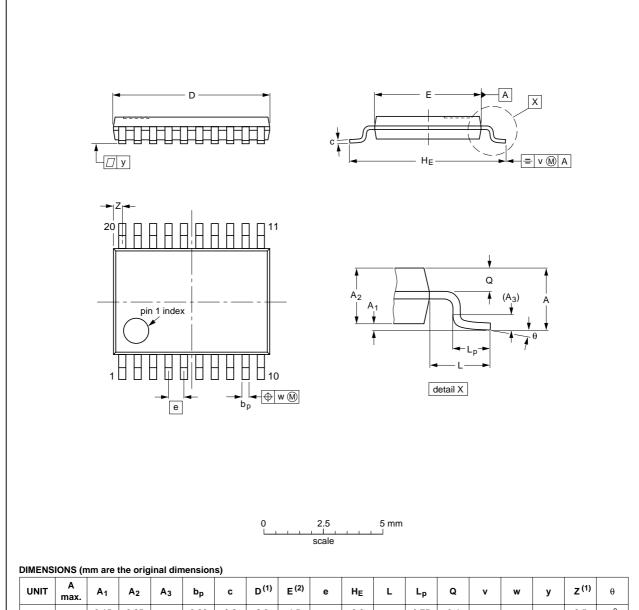
Package outline SOT163-1 (SO20) Fig 9.

0.004

0.089

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



_							٠-,												
	UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(2)</sup>	е	HE	L	Lp	Q	v	w	у	z <sup>(1)</sup>	θ
	mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT360-1		MO-153				<del>99-12-27</del> 03-02-19	
	<u> </u>	<u> </u>			·		

Fig 10. Package outline SOT360-1 (TSSOP20)

## 13. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

## 14. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74AHC_AHCT377_2	20080612	Product data sheet	-	74AHC_AHCT377_1				
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>							
	<ul> <li>Legal texts</li> </ul>	have been adapted to the	new company name whe	re appropriate.				
	• <u>Table 6</u> : the	conditions for input leakage	ge current have been cha	inged.				
74AHC_AHCT377_1	20000815	Product specification	-	-				

## 74AHC377; 74AHCT377

Octal D-type flip-flop with data enable; positive-edge trigger

## 15. Legal information

#### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <a href="http://www.nxp.com">http://www.nxp.com</a>.

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