74AHC594; 74AHCT594

8-bit shift register with output register Rev. 02 — 9 June 2008

Product data sheet

General description 1.

The 74AHC594; 74AHCT594 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC594; 74AHCT594 is an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (SHCP and STCP) and direct overriding clears (SHR and STR) are provided on both the shift and storage registers. A serial output (Q7S) is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

Features 2.

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Wide supply voltage range from 2.0 V to 5.5 V
- 8-bit serial-in, parallel-out shift register with storage
- Independent direct overriding clears on shift and storage registers
- Independent clocks for shift and storage registers
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Input levels:
 - ◆ For 74AHC594: CMOS level
 - ◆ For 74AHCT594: TTL level
- ESD protection:
 - HBM EIA/JESD22-A114E exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
 - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Serial-to parallel data conversion
- Remote control holding register

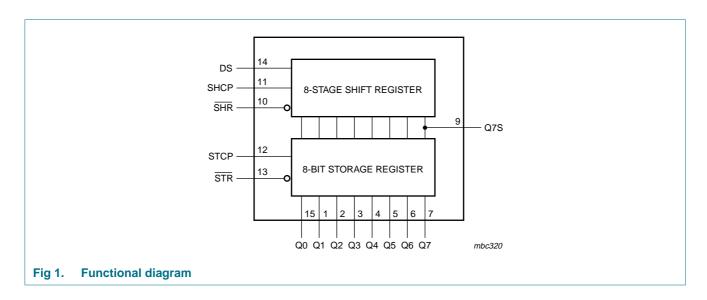


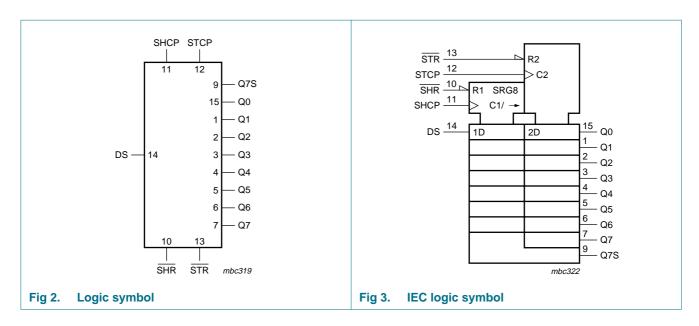
4. Ordering information

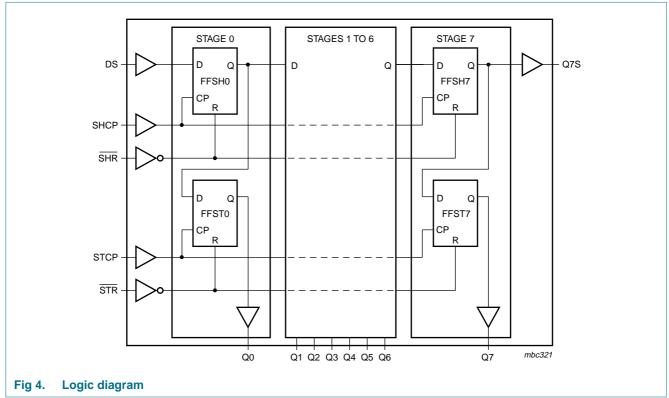
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC594		'		
74AHC594D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC594DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74AHC594PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHC594BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5\times3.5\times0.85$ mm	SOT763-1
74AHCT594				
74AHCT594D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT594DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74AHCT594PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHCT594BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5\times3.5\times0.85$ mm	SOT763-1

5. Functional diagram

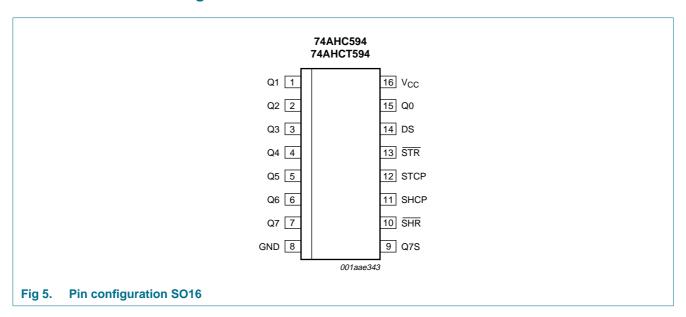


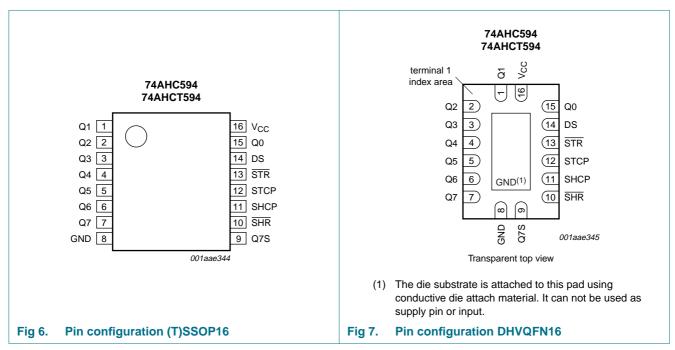




6. Pinning information

6.1 Pinning





6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q1	1	parallel data output
Q2	2	parallel data output
Q3	3	parallel data output
Q4	4	parallel data output
Q5	5	parallel data output
Q6	6	parallel data output
Q7	7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
SHR	10	shift register reset input (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
STR	13	storage register reset input (active LOW)
DS	14	serial data input
Q0	15	parallel data output
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table [1]

Input					Outpu	t	Function
SHCP	STCP	SHR	STR	DS	Q7S	Qn	
Χ	Χ	L	Χ	Χ	L	NC	a LOW-state on SHR only affects the shift register
Χ	Χ	Χ	L	Χ	NC	L	a LOW-state on STR only affects the storage register
X	\uparrow	L	Н	Χ	L	L	empty shift register loaded into storage register
↑	X	Н	X	Н	Q6S	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
Χ	\uparrow	Н	Н	Χ	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	1	Н	Н	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

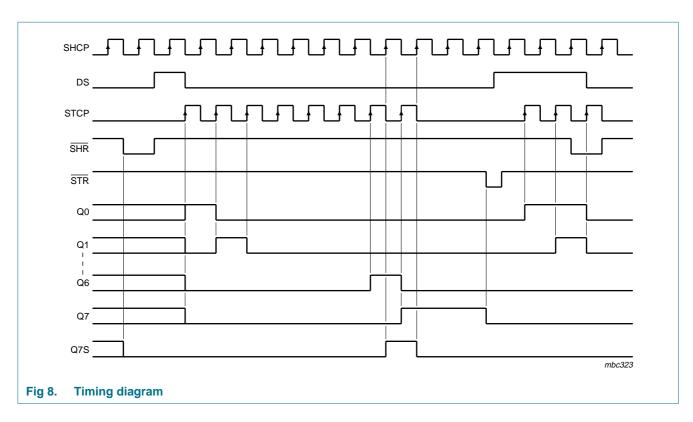
[1] H = HIGH voltage state;

L = LOW voltage state;

 \uparrow = LOW to HIGH transition;

X = don't care;

NC = no change;



8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_1 < -0.5 V$	<u>[1]</u> –20	-	mA
I _{OK}	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$	<u>[1]</u> –20	+20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I_{GND}	ground current		–75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	[2] _	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K. For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K. For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74AHC594	l .					
V_{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V
74AHCT5 9	94					
V_{CC}	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C 1	o +85 °C	–40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC5	94	'								
V_{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = -50 \mu A$; $V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu A$; $V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_{O} = 4 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_{O} = 8 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	–40 °C t	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
C _I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
74AHCT	594									
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	8.0	-	0.8	-	0.8	V
V_{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = -50 \mu A$; $V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O} = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	$I_O = 50 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
II	input leakage current	$V_1 = 5.5 \text{ V or GND};$ $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μΑ
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other pins at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 15.

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C to	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC5	94									
t_{PLH}		SHCP to Q7S; see Figure 9								
	propagation delay	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
	delay	$C_L = 15 pF$	-	5.2	8.5	2.2	9.7	2.2	10.6	ns
		$C_L = 50 pF$	-	7.4	11.5	3.0	13.2	3.0	14.3	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 pF$	-	3.8	6.3	1.7	7.2	1.7	7.8	ns
		$C_L = 50 pF$	-	4.8	8.0	2.4	9.1	2.4	10.0	ns

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 15.

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	–40 °C t	o +125 °	CUni
			Min	Typ[1]	Max	Min	Max	Min	Max	
	•	STCP to Qn; see Figure 10								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		C _L = 15 pF	-	5.1	8.3	2.3	9.5	2.3	10.6	ns
		C _L = 50 pF	-	7.3	11.9	3.3	13.6	3.3	14.7	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		C _L = 15 pF	-	3.5	5.7	1.8	6.5	1.8	7.1	ns
		C _L = 50 pF	-	4.8	7.8	2.6	9.0	2.6	9.8	ns
PHL	HIGH to LOW	SHCP to Q7S; see Figure 9								
	propagation	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
	delay	C _L = 15 pF	-	5.5	8.9	2.3	10.2	2.3	11.0	ns
		C _L = 50 pF	-	7.4	12.1	3.0	13.9	3.0	15.1	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		C _L = 15 pF	-	4.1	6.7	1.9	7.6	1.9	8.2	ns
		C _L = 50 pF	-	5.4	8.8	2.5	10.1	2.5	11.0	ns
		STCP to Qn; see Figure 10								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		C _L = 15 pF	-	5.5	9.1	2.4	10.4	2.4	11.3	ns
		C _L = 50 pF	-	7.3	12.0	3.2	13.8	3.2	15.0	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		C _L = 15 pF	-	3.7	6.0	1.9	6.9	1.9	7.5	ns
		C _L = 50 pF	-	5.2	8.5	2.6	9.7	2.6	10.5	ns
		SHR to Q7S; see Figure 13								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		C _L = 15 pF	-	5.7	9.5	2.3	10.8	2.3	11.7	ns
		C _L = 50 pF	-	7.5	12.2	3.6	14.0	3.6	15.2	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		C _L = 15 pF	-	4.1	6.7	2.0	7.6	2.0	8.2	ns
		C _L = 50 pF	-	5.4	8.8	2.8	10.1	2.8	11.0	ns
		STR to Qn; see Figure 14								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.8	9.6	2.8	11.0	2.8	12.0	ns
		C _L = 50 pF	-	7.7	12.5	3.8	14.4	3.8	15.6	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.1	7.2	2.2	8.2	2.2	8.9	ns
		C _L = 50 pF	-	5.4	9.4	3.0	10.7	3.0	11.6	ns
max	maximum frequency	SHCP or STCP; see Figure 9 and 10								
		V _{CC} = 3.0 V to 3.6 V	80	125	-	70	-	65	-	M
		V _{CC} = 4.5 V to 5.5 V	90	170	_	80	-	70		M

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 15.

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	-40 °C t	o +125 °C	Uni
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _W	pulse width	SHCP and STCP HIGH or LOW; see Figure 9 and 10								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	6.0	-	-	6.5	-	7.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.5	-	-	6.0	-	6.5	-	ns
		SHR and STR HIGH or LOW; see Figure 13 and 14								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	5.0	-	-	5.0	-	5.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.0	-	-	5.2	-	5.7	-	ns
t _{su}	set-up time	DS to SHCP; see Figure 11								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.5	-	-	3.5	-	4.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	3.0	-	-	3.0	-	3.5	-	ns
		SHR to STCP; see Figure 12								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	8.0	-	-	9.0	-	9.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.0	-	-	5.0	-	5.5	-	ns
		SHCP to STCP; see Figure 10								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	8.0	-	-	8.5	-	9.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.0	-	-	5.0	-	5.5	-	ns
t _h	hold time	DS to SHCP; see Figure 11								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	-	-	1.5	-	2.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.5	-	ns
t _{rec}	recovery time	SHR to SHCP; see Figure 13								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	4.2	-	-	4.8	-	5.3	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.9	-	-	3.3	-	3.8	-	ns
		STR to STCP; see Figure 14								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	4.6	-	-	5.3	-	5.8	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	3.2	-	-	3.7	-	4.3	-	ns
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	2] -	55	-	-	-	-	-	pF
74AHCT	594; V _{CC} = 4.5	V to 5.5 V								
t _{PLH}	LOW to HIGH	SHCP to Q7S; see Figure 9								
	propagation	C _L = 15 pF	-	3.8	6.3	1.7	7.2	1.7	7.8	ns
	delay	C _L = 50 pF	-	4.8	8.0	2.2	9.1	2.2	9.9	ns
		STCP to Qn; see Figure 10								
		C _L = 15 pF	-	3.5	5.7	1.8	6.5	1.8	7.1	ns
		C _L = 50 pF	-	4.6	7.7	2.6	8.8	2.6	9.6	ns

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 15.

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	–40 °C t	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{PHL}	HIGH to LOW	SHCP to Q7S; see Figure 9								
	propagation delay	C _L = 15 pF	-	4.1	6.7	1.8	7.6	1.8	8.3	ns
	delay	$C_L = 50 pF$	-	5.4	8.8	2.4	10.1	2.4	11.0	ns
		STCP to Qn; see Figure 10								
		C _L = 15 pF	-	3.7	6.1	1.9	6.9	1.9	7.2	ns
		$C_L = 50 \text{ pF}$	-	5.2	8.5	2.6	9.7	2.6	10.5	ns
		SHR to Q7S; see Figure 13								
		$C_L = 15 pF$	-	4.3	7.0	2.4	8.0	2.4	8.7	ns
		$C_L = 50 \text{ pF}$	-	5.4	8.8	2.7	10.1	2.7	11.0	ns
		STR to Qn; see Figure 14								
		$C_L = 15 pF$	-	4.5	7.4	2.3	8.4	2.3	9.2	ns
		$C_L = 50 pF$	-	5.7	9.4	3.1	10.7	3.1	11.7	ns
f _{max}	maximum frequency	SHCP or STCP; see Figure 9 and 10	90	160	-	80	-	70	-	MHz
t_{VV}	pulse width	SHCP and STCP HIGH or LOW; see Figure 9 and 10	5.5	-	-	6.0	-	6.5	-	ns
		SHR and STR HIGH or LOW; see Figure 13 and 14	5.2	-	-	5.5	-	6.0	-	ns
t _{su}	set-up time	DS to SHCP; see Figure 11	3.0	-	-	3.0	-	3.5	-	ns
		SHR to STCP; see Figure 12	5.0	-	-	5.0	-	5.5	-	ns
		SHCP to STCP; see Figure 10	5.0	-	-	5.0	-	5.5	-	ns
t _h	hold time	DS to SHCP; see Figure 11	2.0	-	-	2.0	-	2.5	-	ns
t _{rec}	recovery time	SHR to SHCP; see Figure 13	2.9	-	-	3.3	-	3.8	-	ns
		STR to STCP; see Figure 14	3.4	-	-	3.8	-	4.3	-	ns
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	<u>-</u>	55	-	-	-	-	-	pF

^[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

 f_0 = output frequency in MHz;

C_L = output load capacitance in pF;

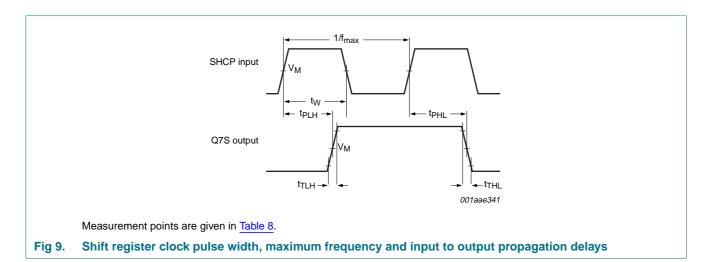
V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$ = sum of the outputs.

^[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

12. Waveforms



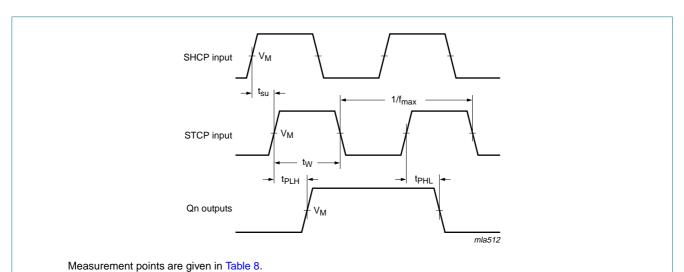
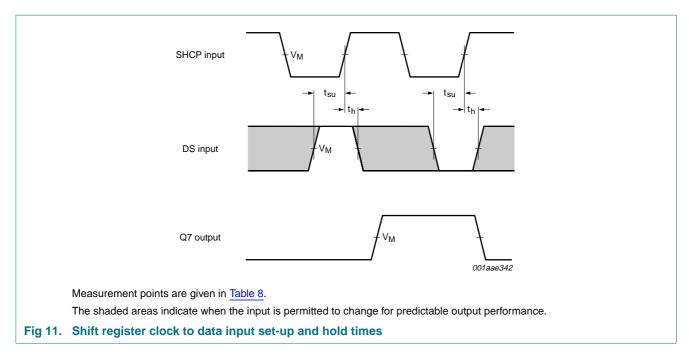
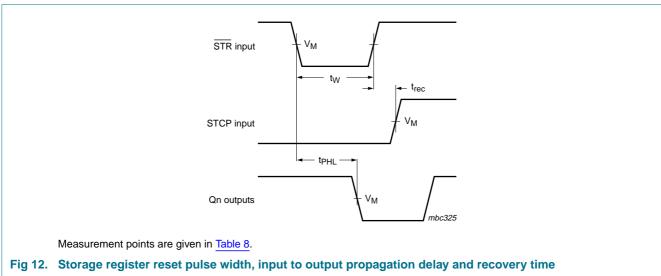
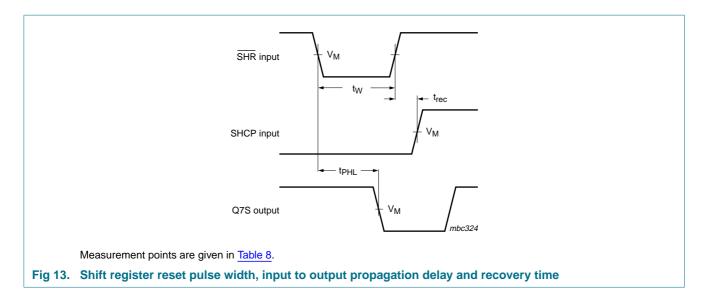


Fig 10. Shift register clock to storage register clock set-up time and storage clock pulse width, maximum frequency and input to output propagation delays







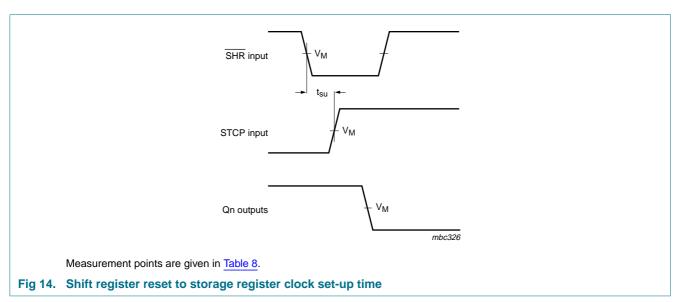
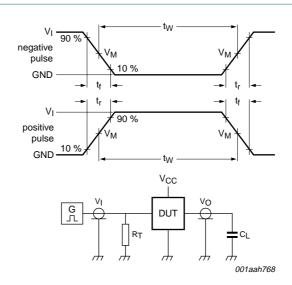


Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74AHC594	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT594	1.5 V	$0.5 \times V_{CC}$



For test data see Table 9.

Definitions for test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

 C_L = Load capacitance including jig and probe capacitance.

Fig 15. Load circuitry for measuring switching times

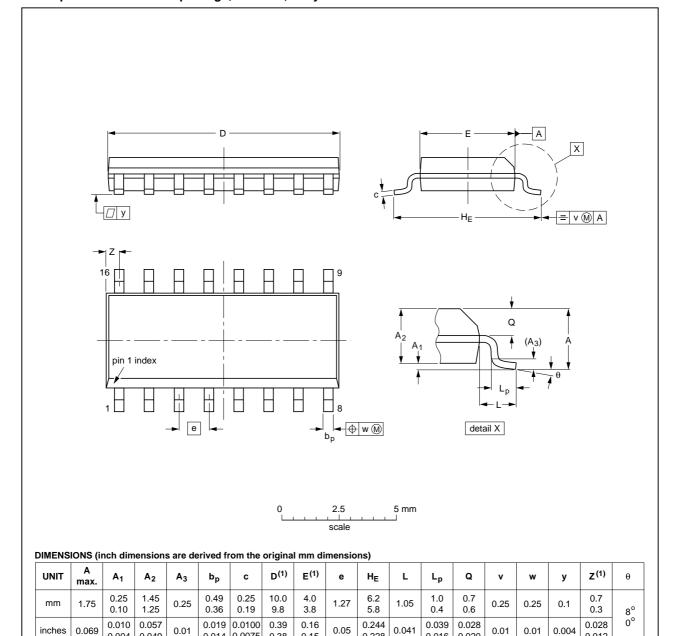
Table 9. Test data

Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74AHC594	V _{CC}	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74AHCT594	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

0.014 0.0075

0.38

0.15

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	IEC JEDEC		PROJECTION	ISSUE DATE	
SOT109-1	076E07	MS-012			99-12-27 03-02-19	

0.228

0.020

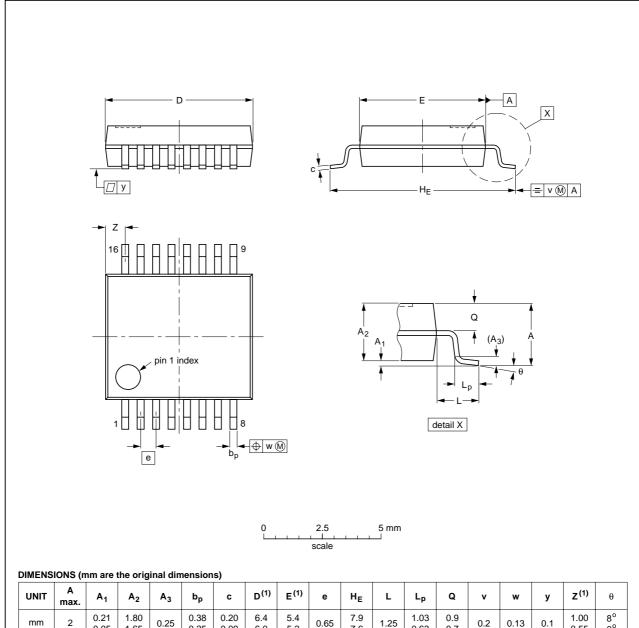
Fig 16. Package outline SOT109-1 (SO16)

0.004

0.049

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



-				3			-,												
	UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
	mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

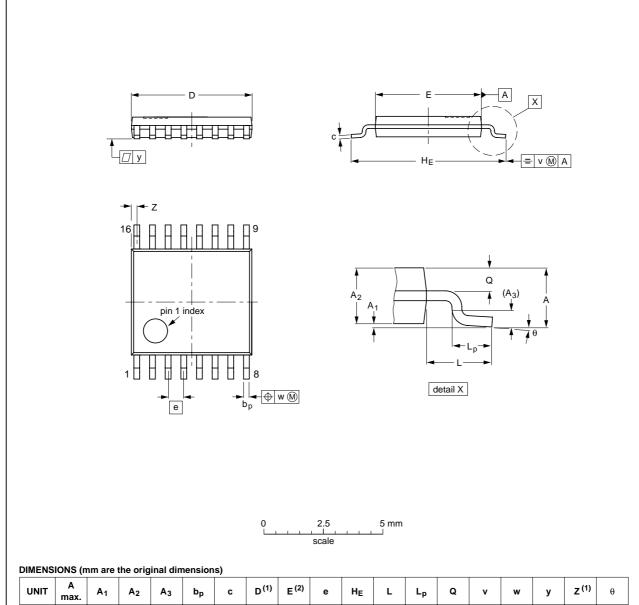
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE	
SOT338-1		MO-150			99-12-27 03-02-19	

Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



_							-,												
	UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
	mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				99-12-27 03-02-18	
						00 02 10	

Fig 18. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

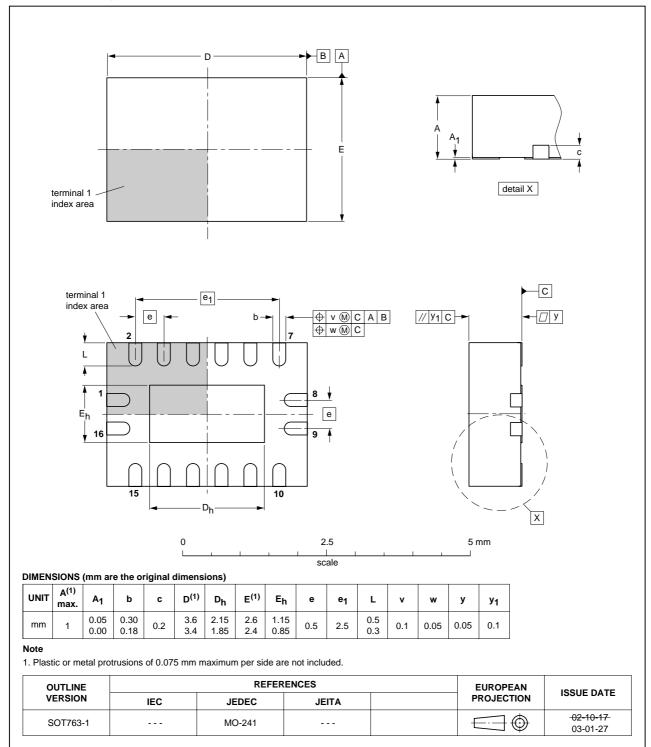


Fig 19. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
74AHC_AHCT594_2	20080609	Product data sheet	-	74AHC_AHCT594_1			
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 						
 Legal texts have been adapted to the new company name where appropriat 							
	• <u>Table 6</u> : the	conditions for input leakage c	urrent have been cha	anged.			
74AHC_AHCT594_1	20060704	Product data sheet	-	-			

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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