COMPUTER ARCHITECTURE PROJECT- DESIGN OF MULTICYCLE PROCESSOR

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ALL the instructions asked in the project are working

Following are the instructions for each type: -

R Type Addition - 8110, 8220, 8501, 8C31, 8DC4, 8653, 8800, 8650, 8700

R Type Subtraction – C314, E3DC

I Type Addition – A13A, A214, 9607, 970F, 98FF

I Type Subtraction – E324, D704, D601

Shift Logical Left – 0371, 0731

Shift Logical Right – 0712, 0612

Shift Arithmetic Right – 0143, 0813

R Type Logical NAND – B632, B800

R Type Logical OR – F860, F770

I Type Logical NAND – 75AE, 78FF

I Type Logical OR – 6800, 6700

Branch Equal to – 4351(once taken and once not taken), 4178 (not taken)

Branch Not Equal to – 5188(not taken)

Jump – 3002, 3FF3

Load Word – 1800, 1401

Store Word – 2400, 2001

GitHub Repo Link – https://github.com/bg-1902/16_bit_RISC

FSM and DataPath – https://drive.google.com/drive/folders/1B_ubkJINQ-xDvcZyn4YsRJs0fIQs0SoC