



AN1052: Selecting a FET For Use With the Si875x Driver

The Si875x enables creating custom solid state relay (SSR) configurations. Supporting customer-selected external FETs, the Si875x combines robust isolation technology with a FET driver to form a complete, isolated, switch. Versatile inputs provide digital CMOS pin control (Si8751) or diode emulation (Si8752) to best suit the application, plus flexible outputs to support driving ac or dc load configurations. A floating secondary side dc voltage source is unnecessary as the product generates its own self contained gate drive output voltage, reducing cost, size, and complexity.

KEY FEATURES OR KEY POINTS

- Selecting for threshold voltage.
- Selecting for switching characteristics.
- Selecting for breakdown voltage.
- Selecting for drain current.
- An example calculation.

1. Introduction

This application note describes how to select a suitable FET to use with the new Si875x FET driver device. Since the suitability of the FET is not dominated by requirements of the Si875x, the selection process mostly depends on the application requirements. This process involves considering several FET parameters, such as threshold voltage, switching characteristics, breakdown voltage, and drain current.

2. Selection Process

2.1 Threshold Voltage

The threshold voltage parameter of a FET is the voltage between the gate and source at which the current begins to flow between the drain and the source. This parameter describes the voltage at which the current just begins to flow. To make the operation of the FET most efficient, the gate needs to be driven to a voltage a few volts higher than the threshold voltage.

The voltage output from the Si875x is somewhat dependent on temperature, forward diode current, in the case of the Si8752, and resistance between the TT pin and ground, in the case of the Si8751. However, it is typically within the range of 8 V to 12 V (see the Si875x datasheet for actual minimum and maximum values). The threshold voltage of the chosen transistor needs to be significantly below this. For most devices, the threshold voltage is typically less than 5 V and this parameter is usually not an issue.

2.2 Switching Characteristics

The switching characteristics of a FET usually determine how fast the application can be switched on and off. Applications such as switching power supplies and power inverters often have switching frequencies higher than 100 kHz. The Si875x is intended for applications with switching frequencies at or below 7.5 kHz. The amount of time it takes the Si875x to drive its output voltage to 90% of the final value is typically determined by the forward diode current, in the case of the Si8752, the resistance between the TT pin and ground, in the case of the Si8751, and the capacitance presented to the output by the FET gate.

The most appropriate way to determine how much capacitance the FET presents to the output of the Si875x is to consult the datasheet for the FET device and find a parameter called Total Gate Charge (Qg). This value, divided by the output voltage of the Si875x device, will describe the total capacitance presented to the output of the Si875x. This value can then be used to get the turn on time of the Si875x from the datasheet for the Si875x.

For example, if a FET datasheet states that the Qg of a device is 6 nC and the Si875x output voltage is 10 V, then it can be expected that the Si875x output will see a capacitive load of about 600 pF. Using the figure below, it can be determined that an Si8751 with a TT resistance of 10 k ohms will take about 500 μ sec to reach 90% of its full output value with a 600 pF load. The Si8752, with a diode current of 5 mA, would take about 800 μ sec to reach 90% with the same 600 pF load.

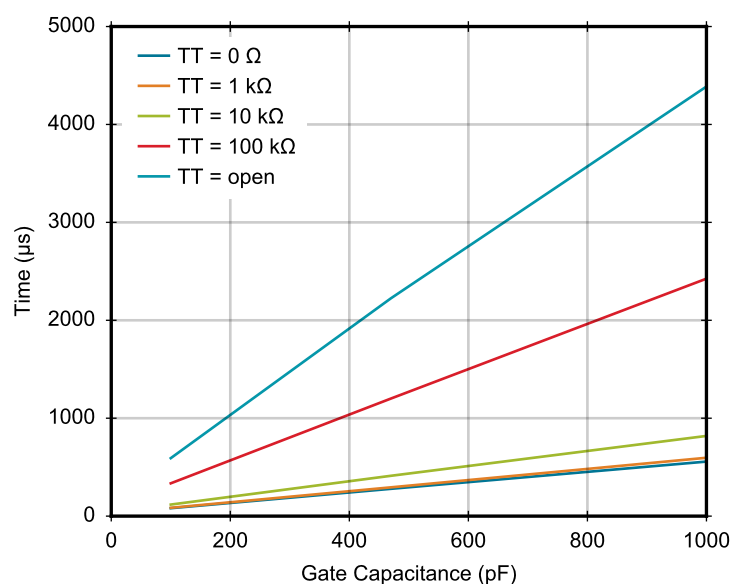


Figure 2.1. Si8751 Typical Turn-On Time vs. Capacitance and TT (90% of Output)

2.2.1 Notes

If the Si875x driver is used to switch two FET devices in an AC application, the total gate charge of both devices must be added together to get the correct capacitive load.

As long as the output voltage of the Si875x is higher than the threshold voltage of the FET device, the Si875x will be able to turn the FET on and off regardless of the total gate charge.

2.3 Breakdown Voltage

The breakdown voltage rating (BVDSS) describes how much voltage the FET can “hold off” when in the off state. It describes how much voltage can be applied between the source and the drain, while the device is off, before its structures begin to break down and the current begins to flow. If this rating is exceeded, it can cause immediate, permanent, damage to the FET. The device used in the application needs to have a voltage rating at least as high as the expected voltage the device needs to withstand in the off condition. Switching circuits inevitably have some degree of voltage transients during switching that can damage the FET. The chosen FET needs to be able to tolerate those transients or be protected against them using some type of clamping circuitry.

2.4 Drain Current

The drain current rating (I_D) describes how much current the FET can tolerate when in the on state. The FET datasheet states the value of the parameter for the device. However, more detailed issues must be taken into consideration. The drain current rating is often specified at two or more temperatures. These temperatures usually refer to the case temperature of the device and the ambient temperature the device. The rating decreases with increasing temperature.

While the drain current specification can give an indication of the capabilities of the FET, the rating in the datasheet is extremely dependent on very specific conditions that may or may not exist in the intended application. It is usually better to perform a complete thermal analysis to determine if the device is suitable for the application. Exceeding these specifications also causes failure as it can cause the package construction to delaminate and melt the surrounding circuitry.

A thermal analysis can be done to determine the maximum current the FET can handle without the temperature of the internal structures (junction temperature) exceeding the maximum allowed temperature. To do this, the amount of temperature difference between the junction and either the case or the ambient environment is calculated. Typically, one would determine the temperature difference between the junction and the case of the device if a heatsink is going to be used. Otherwise, the temperature difference between the junction and the ambient temperature is determined.

To do this analysis, maximum junction temperature (T_{jmax}), thermal resistance (θ_{ja}) and the power being dissipated in the device package (P_d) are taken into consideration. The relationship between the junction temperature (T_j), ambient temperature (T_a), and power dissipation is given as follows:

Equation 1:

$$T_j = T_a + P_d \times \theta_{ja}$$

This equation provides the temperature of the junction in the FET for any given ambient temperature and power dissipation.

When the FET is on, the assumption is that it is being driven into the triode region of operation, which means that the device is as “on” as it can be. Therefore, the drain to source current is no longer limited by the gate to source voltage. Instead, it is limited by the intrinsic resistance of the drain to source channel and the voltage across the device. This value can be determined from the FET datasheet as R_{DSon} . Given that this parameter is essentially resistive, the power being dissipated by the device is the same as the power calculation for a resistor:

Equation 2:

$$P_d = I_d^2 \times R_{DSon}$$

Where I_d is the drain current flowing through the device. This can be substituted into equation 1 to get:

Equation 3:

$$T_j = T_a + I_d^2 \times R_{DSon} \times \theta_{ja}$$

To determine what the maximum amount of current the device can conduct, equation 3 can be modified by substituting T_j with T_{jmax} and rearranged to get:

Equation 4:

$$I_{dmax} = \text{SQRT} \left(\frac{T_{jmax} - T_a}{R_{DSon} \times \theta_{ja}} \right)$$

This value is the maximum amount of drain current the device can conduct and still have its junction temperature at or below the maximum allowed. This value needs to be larger than the amount of current the device will be expected to conduct in the application.

A FET device that is suitable for the application needs to have a threshold voltage, V_{gsth} , that is lower than the output voltage of the Si875x driver; a breakdown voltage, $BVDSS$, that is greater than any voltage the device will experience in the application, including transients; and have a maximum drain current, I_d , that is greater than any current the device is expected to conduct, including transients. In addition, the maximum switching speed is determined by the total gate charge, Q_g , of the FET.

2.5 Example

In this example, there is a 100 W resistive load in a 150 V system to be switched. The application needs to operate up to 85 °C ambient temperature.

The first step is the device voltage. The FET needs to have a BVDSS greater than 150 V.

The current needed to be conducted can be found by dividing the power of the load by the system voltage:

Equation 5:

$$I = \frac{100W}{150V} = 0.667A$$

The device must be capable of conducting at least 0.667 amps when on and withstanding at least 150 V when off.

Most manufacturers of FET's have parametric search engines on their web sites. This makes it easier to see a number of devices sorted by parameters that are of interest. For this example, the Fairchild website (now part of On Semiconductor) was chosen. Navigating to <https://www.fairchildsemi.com/products/discretes/fets/>, a product line is found of N-channel FET's with BVDSS less than or equal to 250 V. Because a little margin between our application voltage and our device voltage is desirable, this product line is selected.

Using the search tools on that site, one device found is the FDD6N25. It states that the BVDSS is 250V, RDSon is 1.1 Ω, and the θja is 110 °C/W.

It can be seen that the voltage rating for this device is more than adequate for this application. Next, the thermal analysis is done to see if it can handle the current. From the datasheet for the FDD6N25, the maximum junction temperature is found to be Tjmax = 150 °C.

Using equation 4:

$$I_{dmax} = \text{SQRT} \left(\frac{150^{\circ}C - 85^{\circ}C}{1.1\text{ohm} \times 110 \frac{^{\circ}C}{W}} \right) = 0.733A$$

Note that the maximum ambient temp of 85°C is used for Ta. This means that the device can handle 0.733 A before over heating the junction at the maximum application ambient temperature. This is about 66mA more than the application requires. Since the example stated the load is resistive, there is not likely to be much transient behavior.

One thing that can be done is to rearrange equation 4 such that the maximum ambient temperature the application is able to tolerate given a drain current of 0.667 A.

Equation 6:

$$T_a = T_{jmax} - I_d^2 \times R_{DSon} \times \theta_{ja}$$

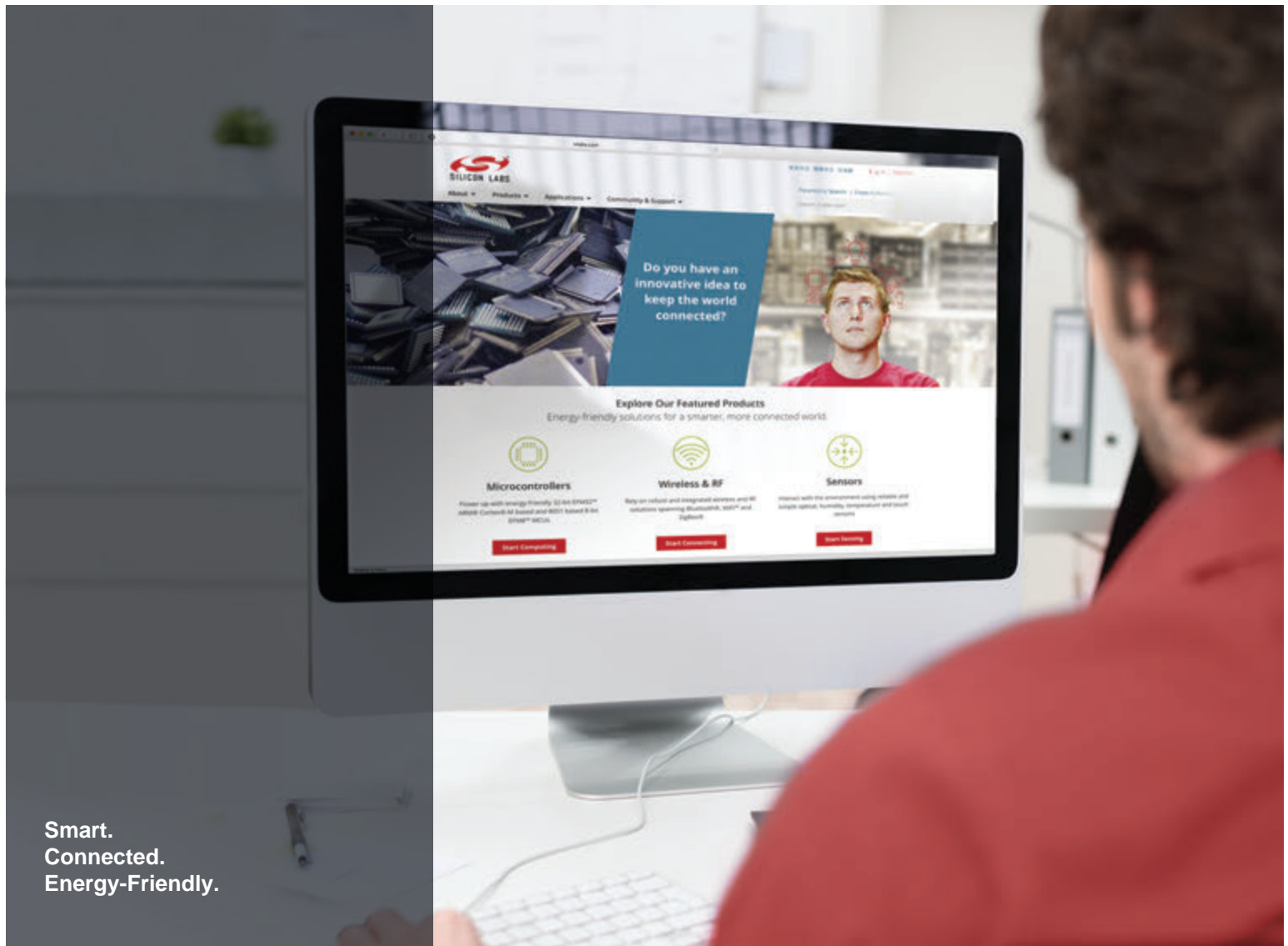
Substituting the values gives us:

$$T_a = 150^{\circ}C - (.667A)^2 \times 1.1\text{ohm} \times 110 \frac{^{\circ}C}{W} = 96.2^{\circ}C$$

This means with a drain current of 0.667 amps, the chosen FET's junction temp will remain below 150 °C as long as the ambient temperature remains below 96.2 °C. Therefore, this FET meets the application requirements.

3. Conclusion

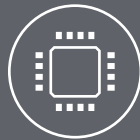
This application note describes a process to determine a suitable FET device for an application using the Si875x FET driver device. Additionally, it shows that the most important parameters of the FET, such as breakdown voltage and drain current are dictated by the application and not the Si875x driver itself.



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