

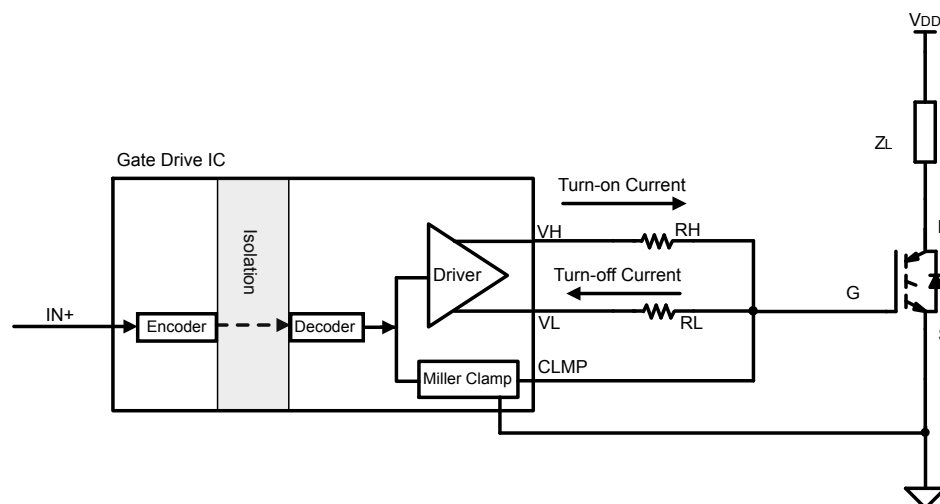
AN1009: Driving MOSFET and IGBT Switches Using the Si828x

The Si828x products integrate isolation, gate drivers, fault detection protection, and operational indicators into one package to drive IGBTs and MOSFETs as well as other gated power switch devices. Most Si828x products (except the Si8286) have three separate output pins to provide independent rise and fall time settings and low impedance clamping to suppress Miller voltage spikes. This application note provides guidance for selecting the external components necessary for operation of the driver. Although this application note discusses the topic of driving IGBTs and MOSFETs, users can apply the same concepts for driving other gate-based power switches, such as SiC (Silicon Carbide).

The figure below depicts an isolated gate drive circuit with three output pins for driving the gate of the IGBT. Input signals from the IN+ pin are RF encoded to transmit across the isolation barrier, and the RF signal is decoded back to its original signal format on the secondary side to connect to the driver input. The driver has three output pins. The VH pin provides positive drive current to turn the IGBT on while the VL pin provides sinking current to turn the IGBT off. The VH and VL pins are connected to the gate of the IGBT through the RH and RL resistors. The CLMP pin is connected to the gate of the IGBT directly to provide a low-impedance clamp between the IGBT Gate and Source terminals during the off time. This low-impedance CLMP connection prevents the high Miller current from generating voltage spikes that might be higher than V_{th} and turn the IGBT on during the off period. The following sections will explain the operation of the gate drive circuits in more detail.

KEY FEATURES

- Simple Driver with One Output
- Driver with Independent Rise and Fall
- Driver with Miller Clamp
- Driver Power Dissipation
- Gate Resistor Calculations
- DESAT Detection and Protection
- Half-Bridge Shoot-Through Current
- Example Design



1. IGBT and MOSFET Gate Drive Models

The figure below shows the simple driver with one output pin driving the gate of a MOSFET through the gate resistor R_g . Since both gate charging and discharging current levels are determined by R_g , the rise and fall times are the same. This driver model works well for applications where independent rise and fall time is not necessary and the Miller current generated by the dV/dt at the MOSFET Drain terminal through the parasitic C_{GD} is small, hence a Miller clamp is not needed.

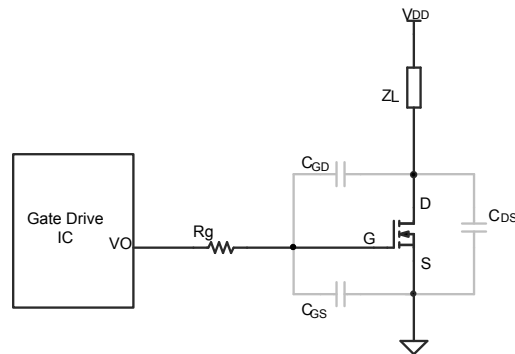


Figure 1.1. Simple Driver Model

The figure below illustrates a driver with separated VH and VL (separate output high and output low) pins that allows independent setting of the switch's turn ON and OFF times. This capability is quite helpful in half-bridge configuration ([Figure 2.3 Half-Bridge Circuit with Three-Output-Pins Driver on page 4](#)) where the speed of the turn ON and OFF are aligned to minimize shoot-through current (see section 2.1). The low-impedance Miller clamping pin (CLMP) attenuates the Miller voltage spikes and renders the driver with three output pins more suitable for driving high power MOSFET/IGBT with larger input gate C_{GS} and C_{DS} capacitances.

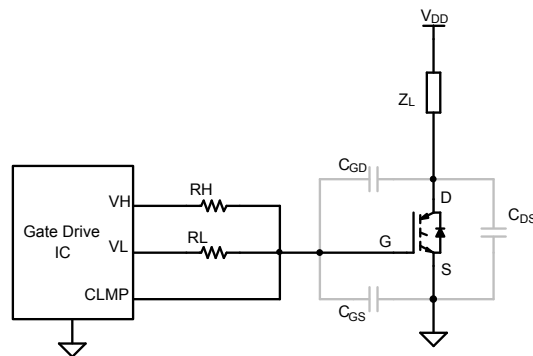


Figure 1.2. Driver Model with Three Output Pins

The following figure demonstrates an option for the Simple Driver circuit to achieve independent control of the rise and fall times by the use of the steering diode. It is recommended to use 100 V, 1 A fast diode, similar to an ES1B diode, to ensure adequate turn-off speed and meet the operational voltage-current requirements of the driver circuit. Note that since the turn off current flows through both R_H and R_L , adjustment to the R_L value is required to ensure the desired turn-off transition time (see [3.1 Calculating \$R_H\$, \$R_L\$ Gate Resistors](#)).

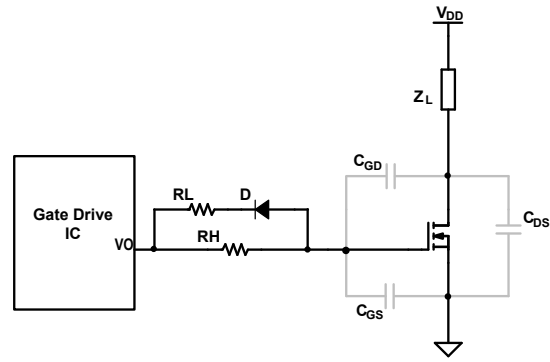


Figure 1.3. Simple Driver with Independent Rise and Fall Times

2. Switching Characteristics

Since IGBTs and MOSFETs are gated power switch devices there is no gate current flow during the ON and OFF states, and the voltage level at the gate controls the device between the ON and OFF states. However, there are parasitic capacitors between gate to source (C_{GS}) and gate to drain (C_{GD}) that require rapid charging and discharging during switching. The figure below provides graphical presentation for the gate voltage and current characteristics.

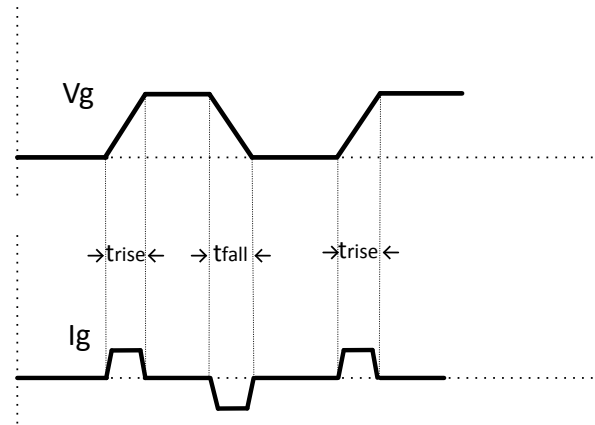


Figure 2.1. Gate Current during Switching

Turning the power switch ON and OFF requires current flow to charge and discharge the gate capacitors. Power switch datasheets provide the total gate charge (Q_{total}) required to switch a device between the ON and OFF state. The larger the available gate current, the less time it takes to provide the switching gate charge. Equation 1 defines the relationship between the gate current I_g , the total gate charge Q_{total} , and the switching transition time t .

$$Q_{total} = I_g \times t \quad \text{or} \quad I_g = \frac{Q_{total}}{t}$$

Equation 1. Gate Charge, Gate Current over Transition Time

From the above equation, it is easy to see that the switching time can be reduced with higher gate current. The figure below illustrates faster switching time (compared to the figure above) with higher gate current.

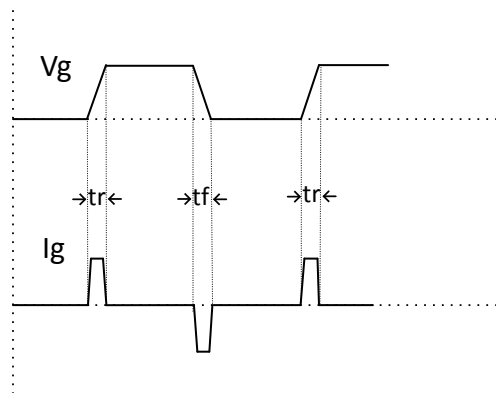


Figure 2.2. Higher Gate Current Reduces Switching Time

2.1 Coordinating RH and RL Values to Minimize Shoot-Through Current

The following figure illustrates a half-bridge power circuit with three-output-pin drivers. This type of power circuit can suffer shoot-through current (current created when both QH and QL are ON) if driven by complementary (+IN, -IN) input signals and having the same values for RH and RL.

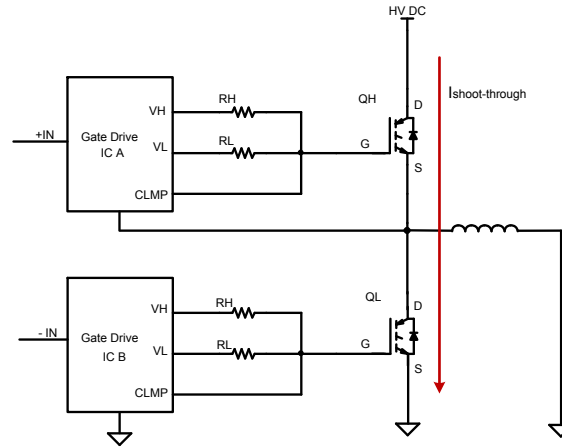


Figure 2.3. Half-Bridge Circuit with Three-Output-Pins Driver

Moreover, power devices are not idealistic switches and the transition between ON and OFF states does not occur cleanly. There is a period, during the switching transition when both switches are in the half-on and half-off state. This condition allows current from the HV-DC rail to flow directly through both QH and QL to ground (see figure above). Shoot-through current dissipates excessive amounts of power in the switching devices since it flows directly across the high voltage dc rail. This is part of switching loss and should be minimized for robust operation.

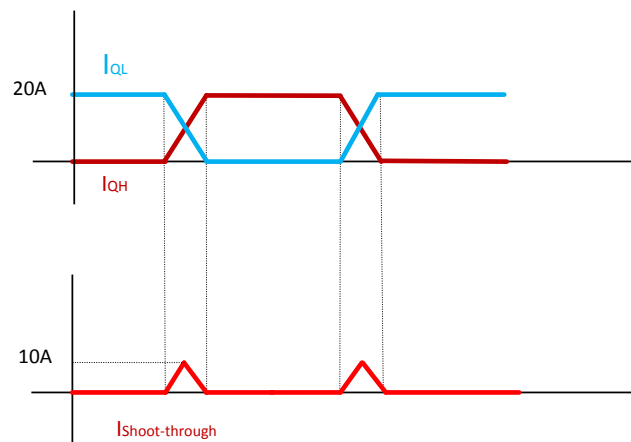


Figure 2.4. Shoot-Through Current at Switching, $R_H = R_L$

One method to minimize shoot through current is to turn the switches on slowly and to turn them off quickly. This method ensures that one device is closer to a complete turned-off state before the other one is turned on. This method can be easily implemented with the 3-output-pin driver by having larger RH and smaller RL resistor values. A large RH value reduces the charging current to the gate capacitor and lengthens the turn-on time while the smaller RL value speeds up the turn-off time. The figure below illustrates a smaller shoot-through current using this method where $R_H \gg R_L$.

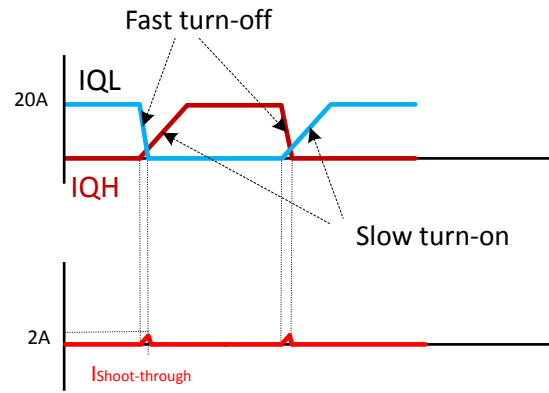


Figure 2.5. Lower Shoot-Through Current, $R_H \gg R_L$

Notice that this $R_H \gg R_L$ method for minimum shoot-through current can also be implemented on the simple driver with one output pin by adding a steering diode to the gate circuit (see [Figure 1.3 Simple Driver with Independent Rise and Fall Times on page 2](#)).

3. Turn-On Characteristics

In the MOSFET circuit in [Figure 1.2 Driver Model with Three Output Pins on page 1](#), the gate capacitances, C_{GS} and C_{GD} , need to be charged to a critical voltage level (bringing V_{GS} toward V_{th}) to initiate I_{DS} current flow (t_0 – t_1 in the figure below). The I_{DS} increases rapidly as V_{GS} goes above V_{th} (t_1 – t_2 in the figure below) and it reaches its maximum current level when V_{GS} reaches a voltage point that generates $I_{DS-max} = V_{DD} / Z_L$.

After the I_{DS} reached its maximum level at t_2 , the V_{DS} voltage drops rapidly resulted in a large dV/dt at the Drain terminal. This dV/dt sinks large current flow from of the gate of the device through C_{GD} . This is the Miller current flow and the dV/dt effectively “amplifies” the current through C_{GD} . The driver’s current must counter the Miller current and results in a constant voltage (almost constant) level at the gate during the Miller current flow period (t_2 to t_3). The dV/dt at the Drain terminal ends at t_3 when the V_{DS} reaches $V_{DS-min} = R_{on} \times I_{DS-max}$. From this point on, any further increase in gate voltage does not affect the drain to source current and the driver current continues to charge C_{GS} and C_{GD} toward the driver’s V_{DRV} voltage level.

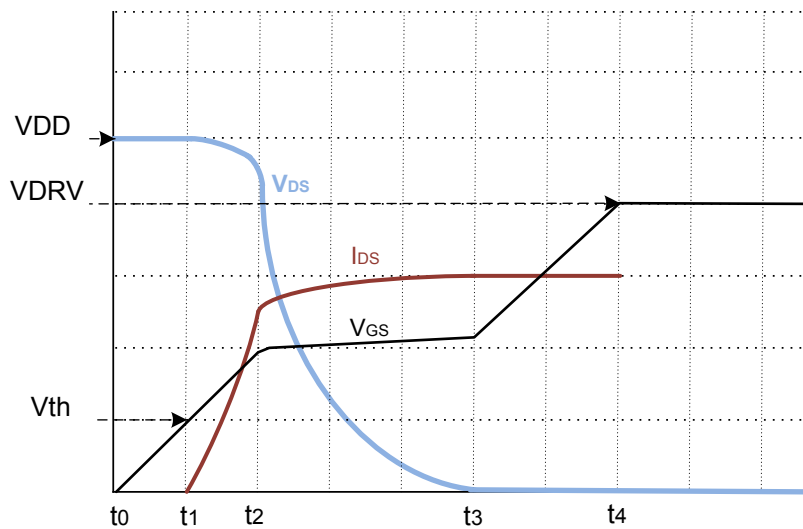


Figure 3.1. Turn-On Characteristics

The figure below provides the relationship between the gate voltage V_{GS} and the gate charge Q_g during the turn on switching transition. Notice that this curve looks similar to the V_{GS} vs. time curve in the above figure.

- Between t_0 – t_1 – t_2 : The gate current charges C_{GS} , C_{GD} and the gate voltage V_{GS} increases linearly.
- Between t_2 – t_3 : The gate current charges C_{GS} and mainly the larger C_{GD_M} Miller cap (C_{GD} with the presence of dV/dt at the Drain terminal). The driver current is sourcing the Miller current and results in no increase in the V_{GS} voltage.
- Between t_3 – t_4 : The gate current charges C_{GS} , C_{GD} , and V_{GS} increases linearly.

This V_{GS} vs. Q_g curve is unique for each power switch device and is available in the power switching device’s data sheet. It is an important parameter as it is used to calculate the values of the R_H , and R_L gate resistors as will be illustrated in an example later in this application note.

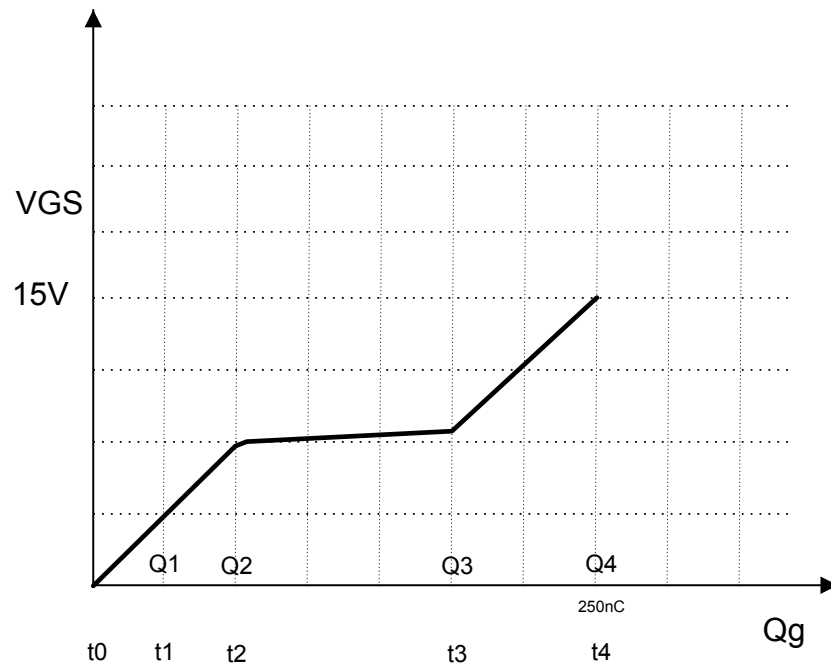


Figure 3.2. V_{GS} vs. Gate Charge

3.1 Calculating RH, RL Gate Resistors

The switching transition time depends on how quickly the total gate charge Q_g is delivered, which in turn, depends on the amplitude of the gate current. Therefore, transition times (t_{rise} and t_{fall}) can be controlled by selecting the values of the gate resistors to a desired gate current levels. From Equation 1 and the information in the above figure, the gate current required to switch the power device between the ON and OFF states can be approximated:

$$I_{g_on} = \frac{Q_g}{t_{rise}}; I_{g_off} = \frac{Q_g}{t_{fall}}$$

Equation 2. Gate Current

Notice that for the driver with three output pins, the gate turn-on (I_{g_on}) and turn-off current (I_{g_off}) can be different for applications with different rise, and fall time requirements. For the driver with one output pin (see front page figure), the rise and fall times are the same since both charging and discharging currents flow through the same R_g resistor.

The RH can be calculated using Ohm's law and the driver's operating voltage V_{DDB} (VDRV)

$$RH = \frac{V_{DDB}}{I_{g_on}}$$

Equation 3. RH Resistor

The power switch turn-off process is the reverse of the turn-on phenomenon. The gate charge built up during the turn-on transition must be removed to bring the power device to a fully off state. The gate voltage from the ON state is equal to V_{DDB} (sustained by the gate capacitors). This voltage level needs to "discharge" to 0V to turn off the power device.

$$RL = \frac{V_{DDB}}{I_{g_off}}$$

Equation 4. RL Resistor

The calculation for RL in the simple driver circuit with steering diode in Figure 3 requires additional adjustment to reflect the fact that the turn off current flows through both RH and RL. Using the calculated RL value from Equation 4, the actual RL value can be derived from the parallel equation for RH and RL.

$$RL_{adjusted} = \frac{RL \times RH}{RH - RL}$$

Equation 5. Adjusted for RL Circuit in Figure 1.3 Simple Driver with Independent Rise and Fall Times on page 2

3.2 RH, RL Power Dissipation

In [Figure 1.2 Driver Model with Three Output Pins on page 1](#), the current flows through resistors RH and RL to charge and discharge the gate capacitors. Depending on the switching frequency, VDDB voltage level, and the total gate charge of the power switch device, the power dissipation on these gate resistors must be considered. Therefore, proper package selections are required to ensure that the resistors can handle the power dissipation appropriately. Power dissipation on the gate resistors occurs only during the turn-on and turn-off transitions.

Upon turn-on, current flows from VDDB through the R_{OH} (Si828x internal source impedance) and RH resistors (see figure below) to charge the gate capacitor, C_g . At the end of the turn-on transition, the voltage at the gate capacitor reached the VDDB level. Half of the total charging energy from VDDB is stored in the gate capacitor and the other half is dissipated on the gate resistors RH and R_{OH} . The power dissipation on the resistor is split between R_{OH} and RH proportionally to their resistance.

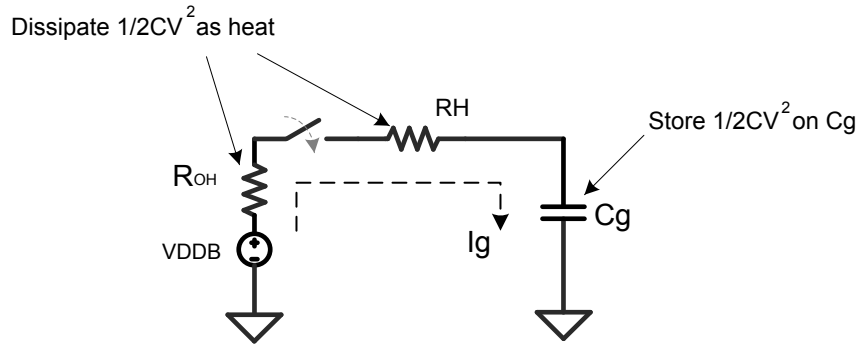


Figure 3.3. R_g Turn-On Power Dissipation

$$P_{RH} = \frac{1}{2} f C_g V_{DDB}^2 \left\{ \frac{RH}{R_{OH} + RH} \right\} = \frac{1}{2} f Q_g V_{DDB} \left\{ \frac{RH}{R_{OH} + RH} \right\}$$

Equation 6. RH Power Dissipation

Upon turn-off, current flows from C_g through RL and R_{OL} to ground (see figure below) to discharge the C_g stored energy (from turn on). The voltage on C_g begins at VDDB voltage level and ends at ground voltage level, and all stored capacitive energy is dissipated on resistors RL and R_{OL} .

$$P_{RL} = \frac{1}{2} f Q_g V_{DDB} \left\{ \frac{RL}{R_{OL} + RL} \right\}$$

Equation 7. RL Power Dissipation

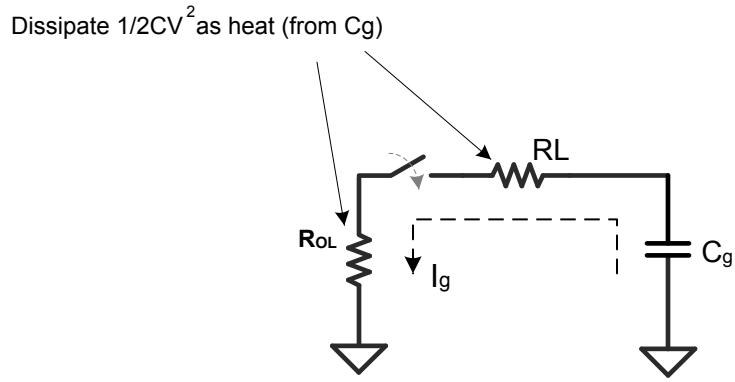


Figure 3.4. Rg Turn-Off Power Dissipation

For the driver circuit with only one R_g gate resistor (see front-page figure), both turn-on and turn-off current flow through the same R_g resistor. The power dissipation on R_g is the sum of the turn-on and turn off power.

$$P_{Rg} = \frac{1}{2} f C_g V_{DDB}^2 \left\{ \frac{R_g}{R_{OH} + R_g} \right\} + \frac{1}{2} f C_g V_{DDB}^2 \left\{ \frac{R_g}{R_{OL} + R_g} \right\}$$

The above equation can be simplified as follows:

$$P_{Rg} = \frac{1}{2} f C_g V_{DDB}^2 \left\{ \frac{R_g}{R_{OH} + R_g} + \frac{R_g}{R_{OL} + R_g} \right\}$$

where $C_g = Q_{total}/V_{DDB}$

Equation 8. Rg Power Dissipation

4. Driver's Power Dissipation Consideration

When all the driver's external gate component values are calculated, it is important to review the total power dissipation of the driver's package to make sure that the device's maximum junction temperature is not exceeded while operating within the desired temperature range. The power equations for the drivers are provided in the data sheet and repeated here for convenience.

Si8285, Si8286, Si8287:

$$PD = (VDDA)(IDDA) + (VDDB)(IDDB) + f \times Q_{int} \times VDDB + \frac{1}{2} \left(f \right) \left(Q_{IGBT} \right) \left(VDDB \right) \left[\frac{R_{OH}}{R_{OH} + R_H} + \frac{R_{OL}}{R_{OL} + R_L} \right]$$

Si8281–Si8284:

$$PD = (VDDA)(IDDA) + 1.05(VDDB)(IDDB) + 1.05 \times f \times Q_{int} \times VDDB + \frac{1.05}{2} \left(f \right) \left(Q_{IGBT} \right) \left(VDDB \right) \left[\frac{R_{OH}}{R_{OH} + R_H} + \frac{R_{OL}}{R_{OL} + R_L} \right]$$

Note: The dc-dc circuit adds 5% higher power dissipation to the Si8281-84 packages.

Note: For system with -VSSB use the same equations but substitute VDDB=(VDDB + VSSB) to account for VSSB power source.

Where (Si8285 bias current data):

PD is the total Si828x device power dissipation (W).

IDDA is the input-side maximum bias current (6.5 mA).

IDDB is the driver die maximum bias current (4.5 mA).

Q_{int} is the internal parasitic charge (3 nC).

VDDA is the input-side VDD supply voltage (2.7 to 5.5 V).

VDDB is the total driver-side supply voltage (VDDB + VSSB: 12.5 to 30 V).

f is the IGBT/MOSFET switching frequency (Hz).

R_H is the V_H external gate resistor, R_L is the V_L external gate resistor (R_H = R_L = R_g if using R_g only).

R_{OH} is the RDS(ON) of the driver pull-up switch: (2.48 Ω).

R_{OL} is the RDS(ON) of the driver pull-down switch: (0.86 Ω).

Equation 9. Driver's Power Equations

The maximum driver's junction temperature can be calculated given the maximum operating ambient temperature and the driver thermal resistance in the data sheet.

$$T_j = PD \times \theta_{ja} + T_A$$

Where:

$$T_j < 150^\circ\text{C}$$

$$\theta_{ja} = 60^\circ\text{C/W (Si8285, Si8286)}$$

$$\theta_{ja} = 60^\circ\text{C/W (Si8281–Si8284)}$$

$$T_A = 125^\circ\text{C (maximum temperature range: -40 to 125}^\circ\text{C)}$$

Equation 10. Junction Temperature

5. DESAT Detection and Soft Shutdown Control

The Si828x has a comparator with its input connected to the DSAT pin to monitor the power switch VCE voltage during on time (when VH is in the high state) to ensure that the power switch is fully on ($V_{DS} < 7\text{ V}$). The DSAT pin is connected to the Collector of the switching device through a diode, and the R_{DSAT} resistor (see the figure below), thus the voltage at the DSAT pin is approximately the same as the voltage at the collector of the switching device with respect to VMID.

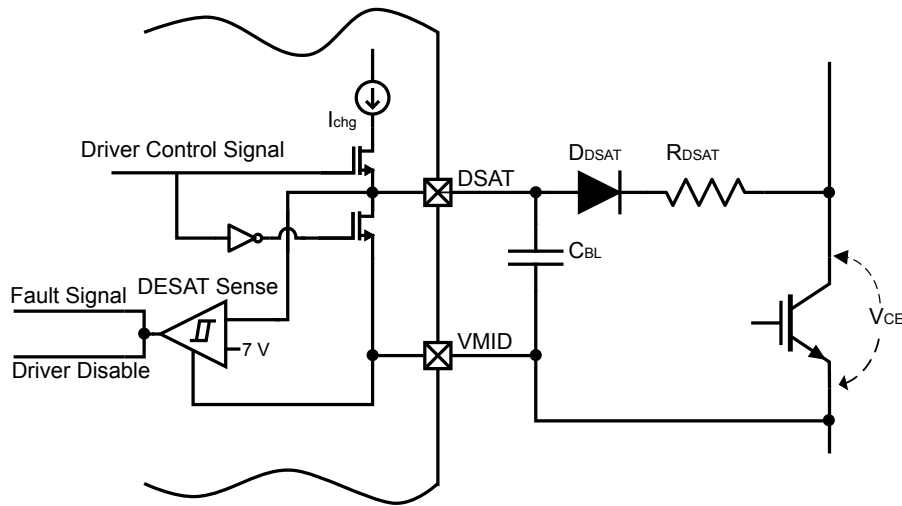


Figure 5.1. DESAT Circuit

If the voltage on the DSAT pin exceeds 7 V during on-time, the Si828x shuts down the output (turn off VH PMOS after t_{FLT} delay; see the figure below) and initiates soft shutdown (after $t_{DSAT\ to\ SS}$ delay) to protect the power switch.

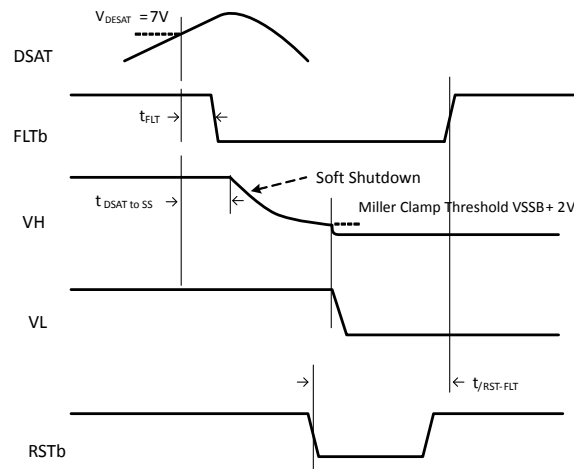


Figure 5.2. DESAT and Soft Shutdown

The internal soft shutdown NMOS is connected to the same VH pin (see the figure below). It has higher impedance ($R_{ss} = 30\ \Omega$) compared to the NMOS at the VL pin ($1\ \Omega$). Due to the presence of the parasitic inductance in the loop, turning the power switch off too quickly under a high fault current condition can generate a high voltage spike at the power switch collector. To avoid the high turn-off voltage spike, only the soft shutdown NMOS is turned on under DSAT shutdown (while the VL NMOS is kept in the off state). The gate capacitance of the power switch is discharged through the R_H and the internal R_{ss} at a much lower rate to allow the power switch to dissipate residual energy from the circuit's parasitic inductance under high fault current condition.

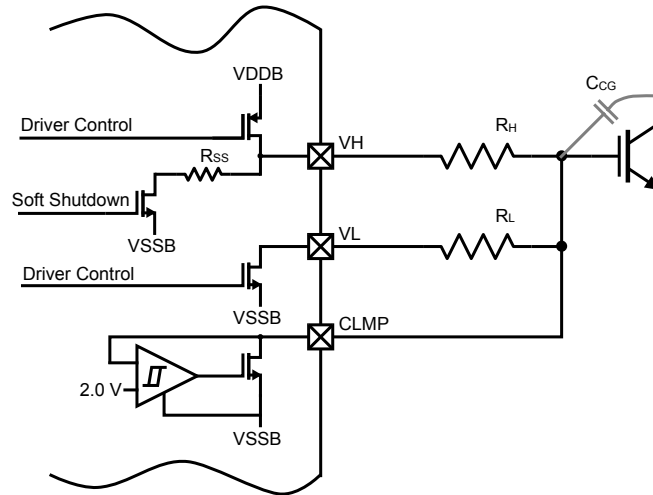


Figure 5.3. Driver Outputs

The internal R_{ss} ($30\ \Omega$) and a $R_H = 20\ \Omega$ provide a typical soft shutdown duration of $2\ \mu s$ (for $250\ nC$ of total gate charge, Q_g .) If a longer soft shutdown period is required, steering diode (ES1B or similar) can be added to the VH pin to allow installation of a larger external soft shutdown resistor (see figure below).

$$t_{ssd} = 5 \times R \times C$$

where $R = R_{ss} + R_H$ (no steering diode) or $R = R_{ss} + R_{EX_SS}$ (with steering diode) and $C = Q_g / V_{DDB}$

Equation 11. Soft Shutdown Timing

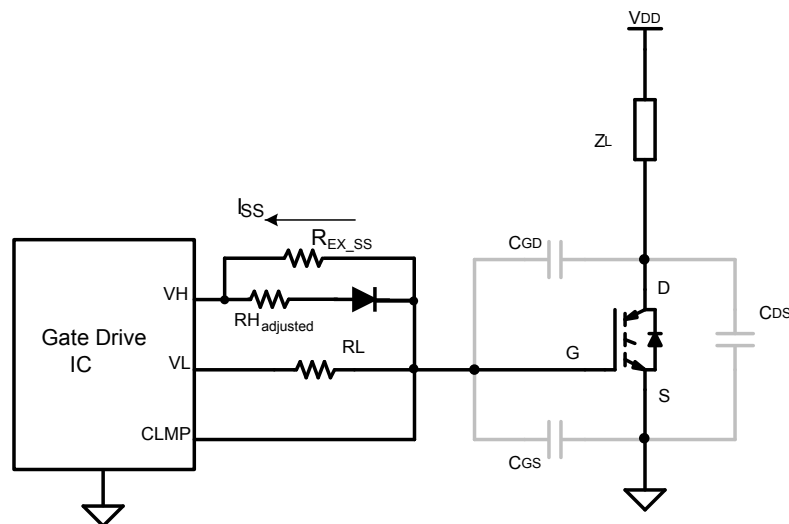


Figure 5.4. External Soft Shutdown Resistor

Since the turn-on gate current in the above figure flows through both R_{EX_SS} and R_H , the value of the $R_{H_adjusted}$ can be derived from the parallel equation for R_H and R_{EX_SS} .

$$R_{H_adjusted} = \frac{R_H \times R_{EX_SS}}{R_{EX_SS} - R_H}$$

Equation 11. Adjusted R_H for Driver with SS Steering Diode

5.1 Miller Clamp

[Figure 5.3 Driver Outputs on page 13](#) includes the internal block diagram for the CLMP pin. The internal CLMP NMOS is activated during the off period and when the voltage at the CLMP goes below 2 V. The internal CLMP comparator has hysteresis to ensure stable turn on under noisy conditions. To minimize the Miller voltage spike, it is recommended to connect the CLMP pin directly to the gate of the power switching device so that the low impedance internal NMOS CLMP driver can secure the gate directly to VSSB.

6. DSAT Fault Indication and Fault Reset

Right after the DSAT condition is detected ($V_{DSAT} > 7V$), the fault indication is propagated toward the FLTb pin and arrives after the TDSAT delay (see [Figure 5.2 DESAT and Soft Shutdown on page 12](#)). The DESAT fault condition can be cleared by bringing the RSTb pin low for a minimum duration of 50 ns. Notice that the RSTb input is level-sensitive reset logic and keeping RSTb low, continues to reset the driver output. The recommended fault condition clearing sequence is to bring the input signals at the IN pins to low logic level and then pulse the RSTb pin low for a minimum duration of 50 ns. The driver is now ready to drive the power switch with input signals from the IN pins.

7. DSAT Blanking Timer Control

Due to delay when it is turned on, the VDS voltage of the power switch can stay at the high voltage VDD level for a while (see [Figure 3.1 Turn-On Characteristics on page 6](#), t₀–t₂) and only transition low after the IDS current reached its maximum level. This means that the VDS voltage can be as high as a few hundreds of volts (VDD) for some time after the driver output has gone high. This high voltage at the DSAT pin can trigger the DSAT detection. To alleviate this false premature DSAT detection event, an external capacitor C_{BL} can be used to set the blanking period according to Equation 12.

$$C_{BL} = t_{Blanking} \times \frac{I_{chg}}{V_{DSAT}}$$

Where:

V_{DSAT} = 7 V (Si828x internal comparator)

I_{chg} = 250 μA (Si8286)

I_{chg} = 1 mA (other Si828x)

Equation 12. Blanking Cap CBL

In most applications, the switching transition period is typically around a couple hundred nanoseconds. Therefore, recommended blanking period is 3 μs to provide ample delay for the VDS to reach to its low on-time voltage level. The Si828x recommended blanking capacitor values are calculated as shown in the equation below.

$$\text{Si8286: } C_{BL} = 3 \times 10^{-6} \times \frac{250 \times 10^{-6}}{7} = 100 \text{ pF}$$

$$\text{Other Si828x: } C_{BL} = 3 \times 10^{-6} \times \frac{1 \times 10^{-2}}{7} = 390 \text{ pF}$$

Note: It is possible to change the C_{BL} value to accommodate a specific blanking delay.

8. Design Example

Design a half-bridge power circuit using N-Channel MOSFETs with the following operating conditions:

1. $I_{max} = 20\text{ A}$, $HVDC = 400\text{ V}$
2. $V_{DS-on} < 1\text{ V}$ at 20 A to minimize loss
3. Rise time = 400 ns , Fall time = 200 ns
4. $F_{sw} = 200\text{ kHz}$

Solution:

1. Select a MOSFET with $V_{DSS} = 650\text{ V}$ for an approximate 40% voltage margin while operating at $HVDC = 400\text{ V}$. The MOSFET data sheet provides the V_{GS} vs total gate charge as shown in [Figure 3.2 \$V_{GS}\$ vs. Gate Charge on page 7](#) and a similar figure as shown below provides the MOSFET output characteristic V_{DS} vs. I_{DS} .
2. Select the Si8285 driver with separated V_H and V_L pin to handle independent 400 ns rise and 200 ns fall times.

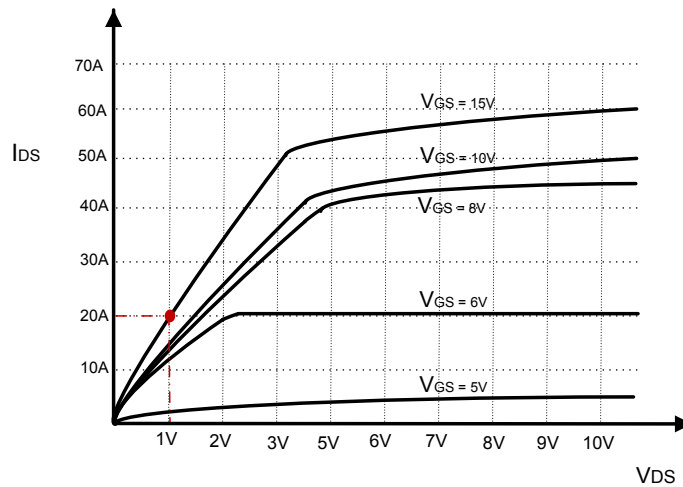


Figure 8.1. MOSFET Output Characteristics @ $T_j = 125\text{ }^{\circ}\text{C}$

3. Applying the given information from items 1 and 2 to the figure above, we see that the circuit would need $V_{DDB} = V_{GS} = 15\text{ V}$ to achieve 20 A with voltage drop $V_{DS} = 1\text{ V}$.
4. [Figure 3.1 Turn-On Characteristics on page 6](#) indicates that it requires a total switching charge of $Q_g = 250\text{ nC}$ to drive the V_{GS} from 0 V to 15 V .
5. Calculations.

From [Equation 2](#):

$$I_{g_on} = \frac{Q_g}{t_{rise}}; I_{g_off} = \frac{Q_g}{t_{fall}}$$

$$I_{g_on} = \frac{250\text{ nC}}{400\text{ ns}} = 0.625\text{ A}; I_{g_off} = \frac{250\text{ nC}}{200\text{ ns}} = 1.25\text{ A}$$

From [Equation 3](#), calculate R_H :

$$R_H = \frac{V_{DDB}}{I_{g_on}}$$

$$R_H = \frac{15\text{ V}}{0.625\text{ A}} = 24\text{ }\Omega$$

From Equation 6, calculate RH power dissipation:

$$P_{RH} = \frac{1}{2} f Q_g V_{DDB} \left\{ \frac{R_H}{R_{OH} + R_H} \right\}$$

$$P_{RH} = \frac{1}{2} 200 \text{ kHz} \times 250 \text{ nC} \times 15 \text{ V} \times \left\{ \frac{24}{2.48 \Omega + 24 \Omega} \right\} = 340 \text{ mW}$$

Select resistor package SMD 1210 for RH resistor to handle up to 0.5 W of power.

From Equation 4, calculate RL:

$$R_L = \frac{V_{DDB}}{I_{g_off}}$$

$$R_L = \frac{15 \text{ V}}{1.25 \text{ A}} = 12 \Omega$$

From Equation 7, calculate RL power dissipation:

$$P_{RH} = \frac{1}{2} 200 \text{ kHz} \times 250 \text{ nC} \times 15 \text{ V} \times \left\{ \frac{12 \Omega}{0.84 \Omega + 12 \Omega} \right\} = 350 \text{ mW}$$

Select resistor package SMD 1210 for RL resistor to handle up to 0.5 W of power

From Equation 9, calculate Si8285 power dissipation:

$$PD = (V_{DDA})(I_{DDA}) + (V_{DDB})(I_{DDB}) + f \times Q_{int} \times V_{DDB} + \frac{1}{2} \left(f \right) \left(Q_{IGBT} \right) \left(V_{DDB} \right) \left[\frac{R_{OH}}{R_{OH} + R_H} + \frac{R_{OL}}{R_{OL} + R_L} \right]$$

Note the following information from the Si8285 data sheet:

- PD is the total Si828x device power dissipation (W).
- IDDA is the input-side maximum bias current (= 6.5 mA).
- IDDB is the driver die maximum bias current (= 4.5 mA).
- Q_{int} is the internal parasitic charge (= 3 nC).
- VDDA is the input-side VDD supply voltage (= 3.3 V).
- VDDB is the total driver-side supply voltage (= VGS = 15 V).
- f is the IGBT switching frequency (Hz) (= 200 kHz).
- RH is the VH external gate resistor (= 24 Ω and 12 Ω).
- R_{OH} is the RDS(ON) of the driver pull-up switch (= 2.48 Ω).
- R_{OL} is the RDS(ON) of the driver pull-down switch (= 0.86 Ω).

$$PD = (3.3)(0.0065) + (15)(0.0045) + 200,000 \times 3 \times 15 + \frac{1}{2} \left(200,000 \right) \left(250 \right) \left(15 \right) \left[\frac{2.6}{2.6 + 2.4} + \frac{0.8}{0.8 + 12} \right]$$

$$PD = 158 \text{ mW}$$

From Equation 10, calculate the junction temperature at the maximum device's recommended ambient temperature of 125 °C:

$$T_{jmax} = PD \times \theta_{ja} + T_A$$

$$T_{jmax} = (0.158 \times 60) + 125 = 134.5 \text{ °C}$$

This junction temperature is below the maximum Si828x junction temperature of 150 °C, and thus it is safe to operate at this power level.

DSAT Blanking Circuit: Using the standard 3 μs DSAT blanking circuit for Si8285 driver with CBL = 390 pF, R_DSAT = 100 Ω, and ES1J for 600 V D_DSAT diode.

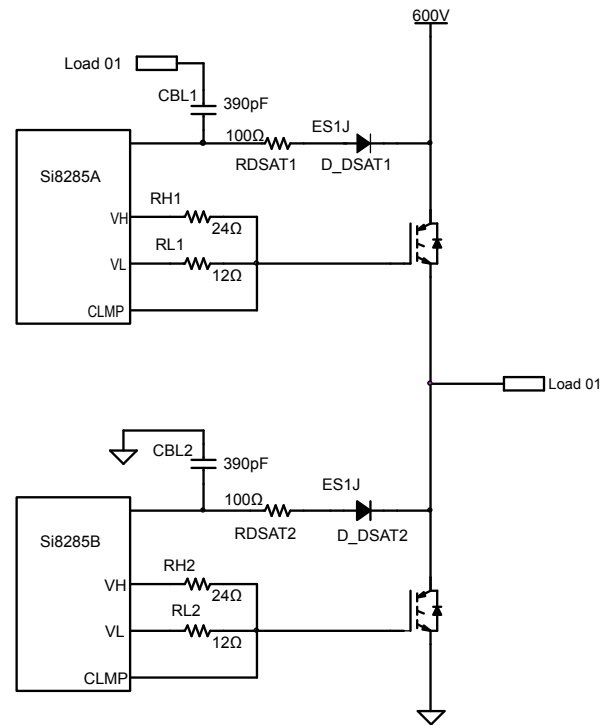
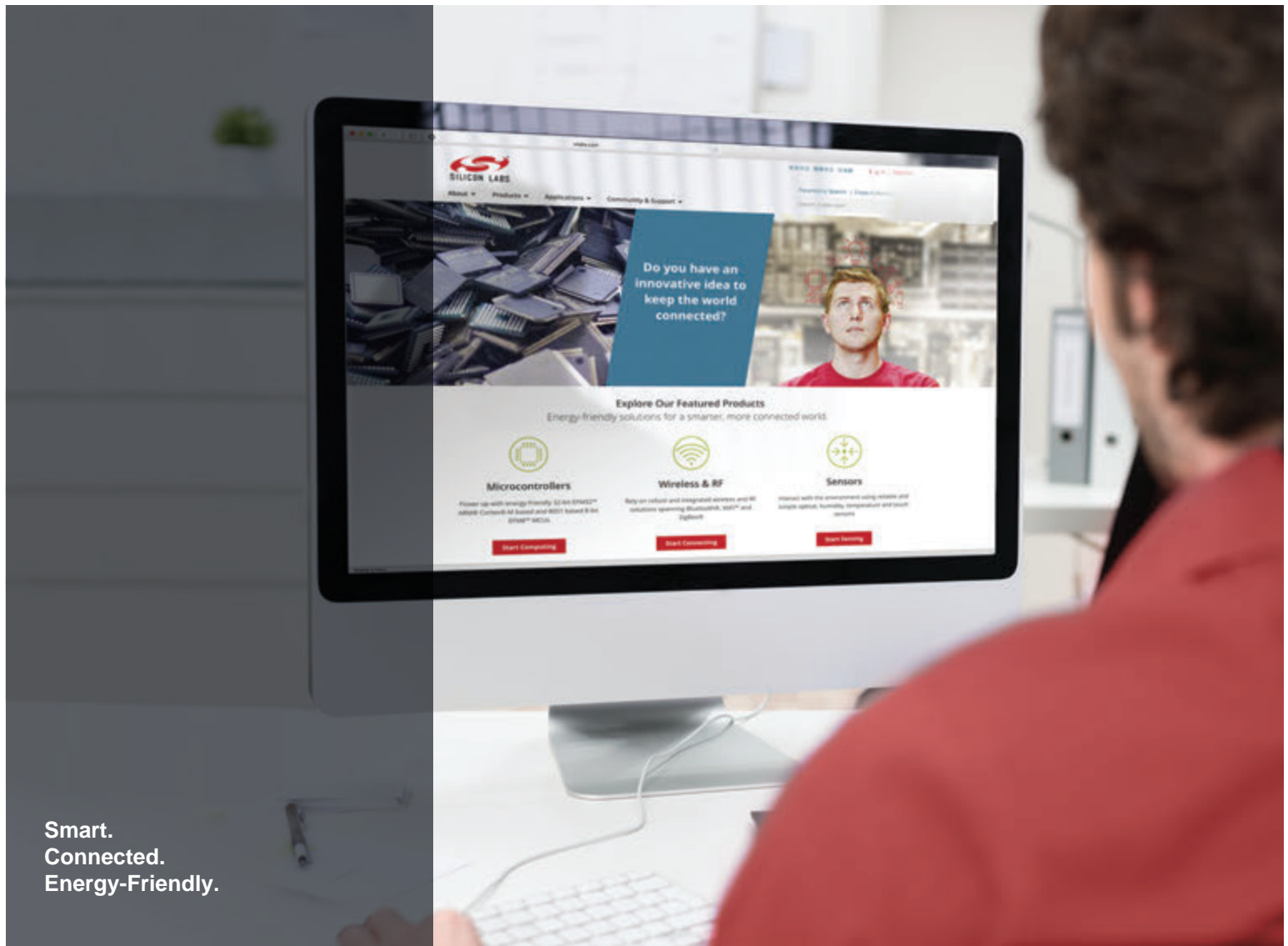


Figure 8.2. Half-Bridge MOSFET Gate Example Circuit

9. Conclusion

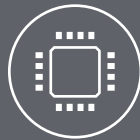
In conclusion, this application note has provided users with an overview of gate power circuit and step-by-step calculations for the values of the external passive components, R_H , R_L , C_{BL} , etc. used with the Si828x ISODrivers. The gate resistor (R_H , R_L) values are calculated based on the total gate charge required to transition the power switch between the ON and OFF states. Since the total gate charge value in the power device data sheet is for a typical device, it does not account for the variation between the power switches as well as the specific PCB trace impedances. Nevertheless, the gate resistor calculations in this application note provides a good approximation, and some fine tuning may be necessary to achieve optimized switching performance. The various control and protection features of the Si828x family have been discussed, and a half-bridge power circuit example has been provided.



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