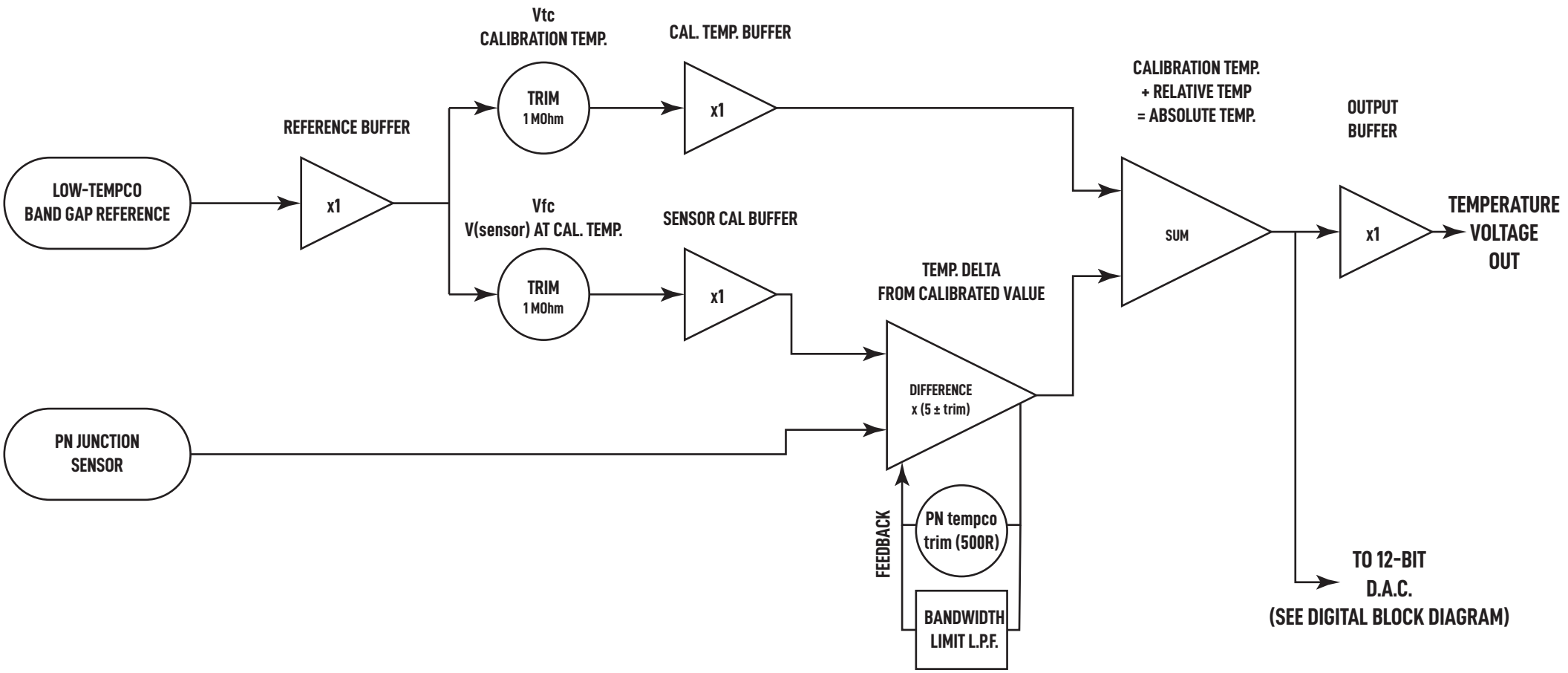
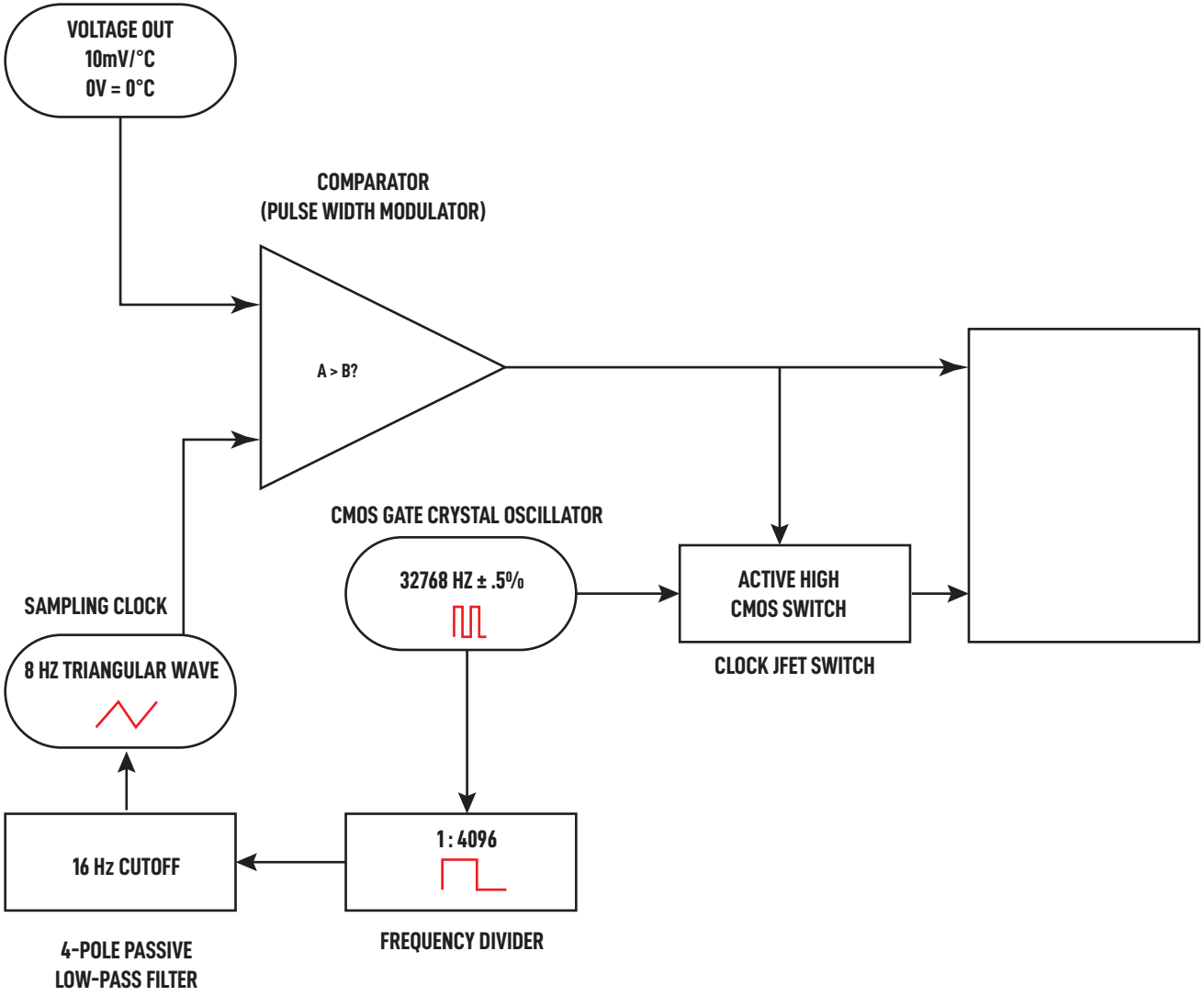
SYSTEM BLOCK DIAGRAM
ANALOG SIGNAL PATH



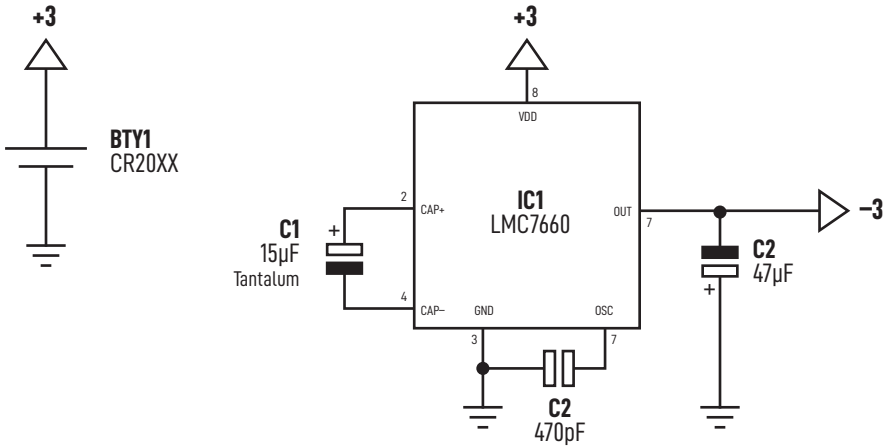
SYSTEM BLOCK DIAGRAM

13-BIT ANALOG-DIGITAL CONVERTER

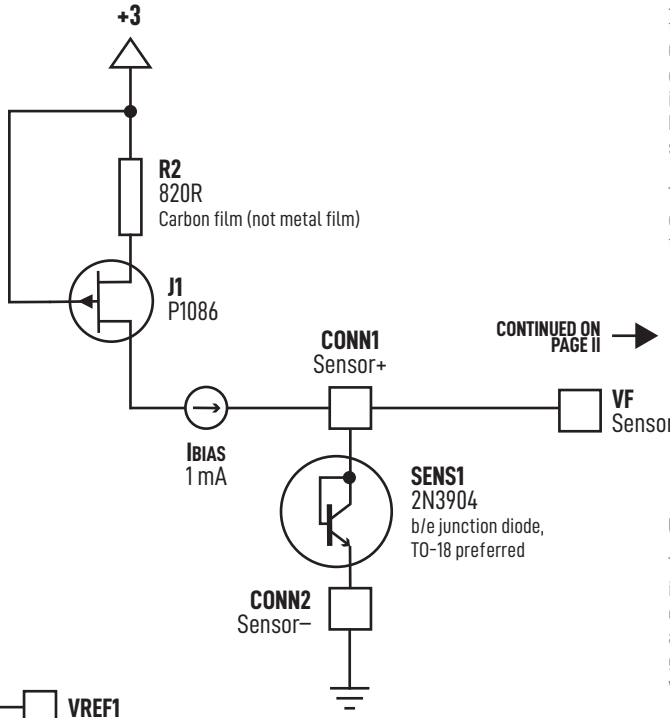


SCHEMATIC – PAGE I
SUPPLIES, CALIBRATION & SENSOR

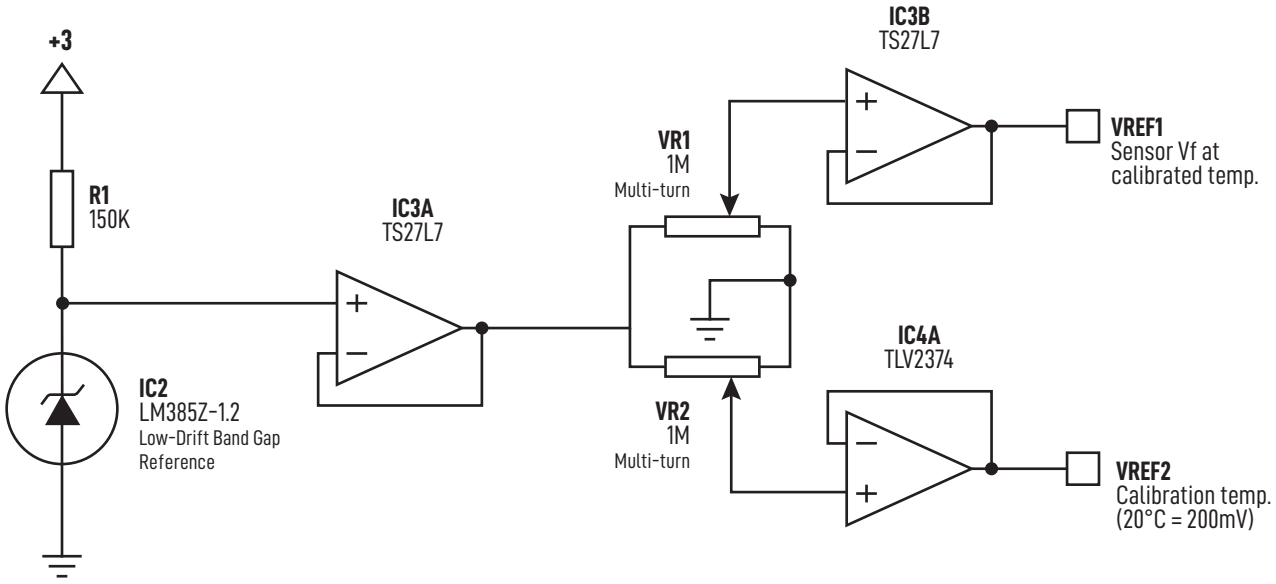
Power supply (+3/Gnd/–3)



Sensor drive



Reference and calibration voltages



SENSOR DEVICE CHOICE

JFETs have a negative temperature coefficient; their transconductance decrease with increased temperature. Carbon film resistors, too, have a negative temperature coefficient, causing a decrease in resistance - or an increase in conductance. Therefore, the two temperature coefficients balance out making the sensor drive constant current source stable across use ambient temperatures.

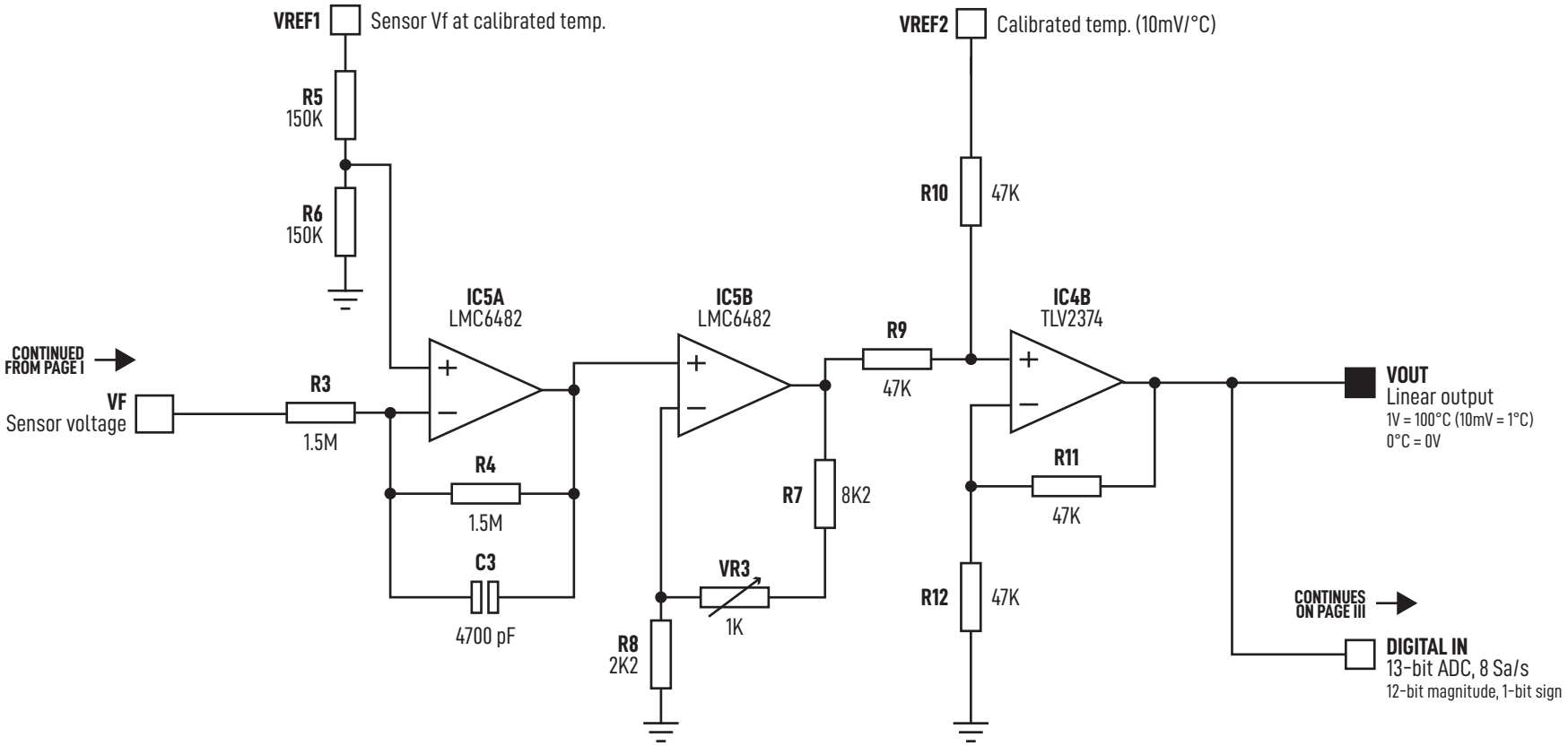
TO-18 devices are preferred for the sensor transistor diode (over TO-92s) since their metal case permit superior thermal contact to the sensing junction.

CALIBRATION GUIDE

The calibration is two–part; first, the ambient temperature is measured, and **VR2** adjusted so **VREF2** (measured at the op amp output) is equal to T_{AMB} * 10mV/°C. Then, **VR1** is adjusted so that **VREF1** = **VF**. Thus, the sensor value at a given temperature and the temperature are the calibration values. Do not touch **SEN1** at any point during the calibration.

SCHEMATIC – PAGE II

ANALOG SCALE/OFFSET & OUTPUT DRIVE



BANDWIDTH CONTROL

Including **C3** in the feedback loop creates a single-pole (-6dB/oct.) low pass filter with a cutoff frequency of approximately 20Hz, which reduces high frequency noise in the measurement.

SENSOR TEMPCO TRIM

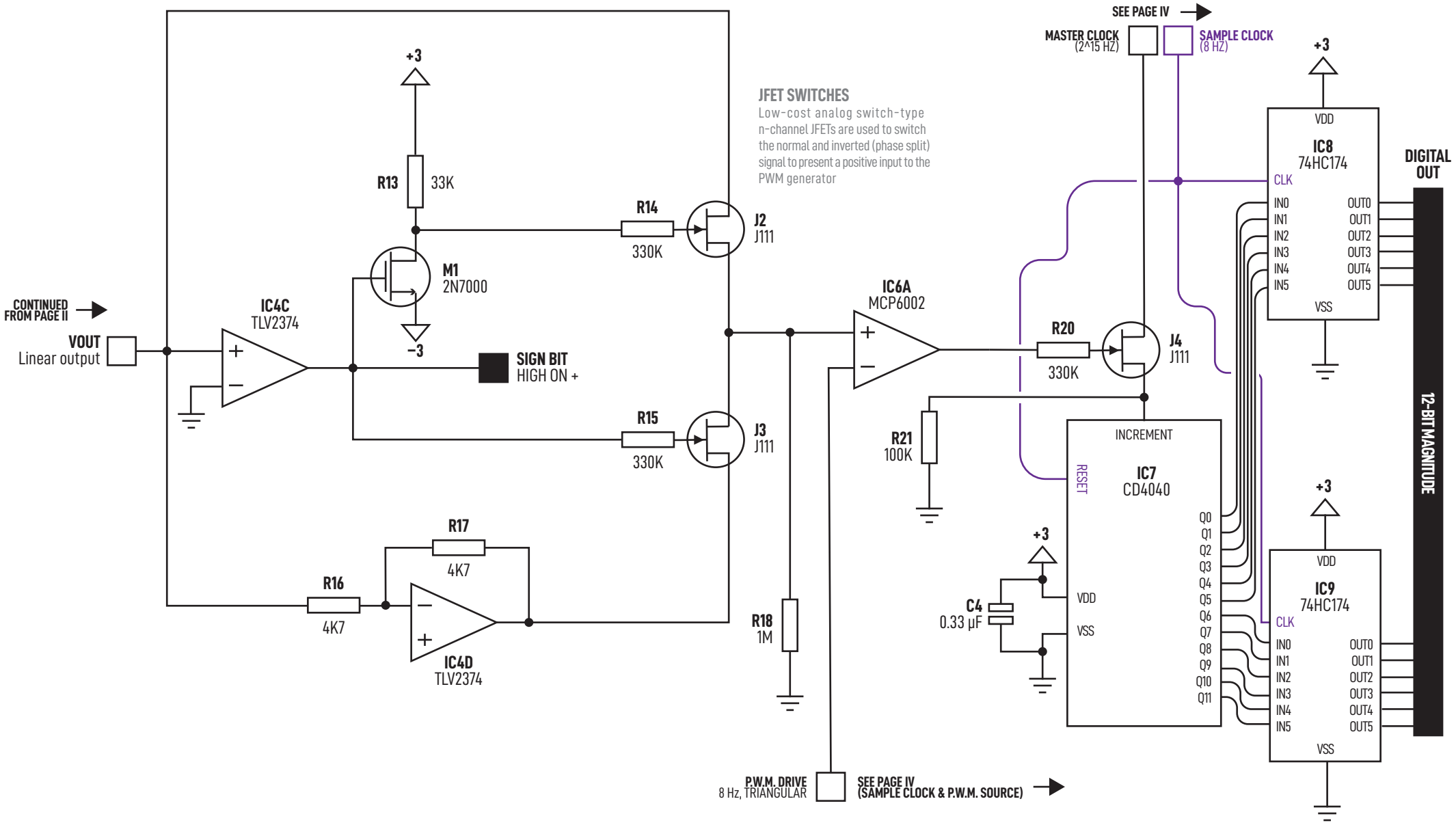
Sensor temperature coefficient trimmable from –2.12 mV/°C to –1.93 mV/°C using **VR3**

AMPLIFIER OFFSET VOLTAGES

No actual op amp is ideal; therefore, each device has an input offset voltage that is added (or subtracted) to the input. This offset is amplified equally with the input. Therefore, the lowest-offset device (**IC5**, with a typical offset of 100µV) is used for subtracting the sensor voltage from **VREF1** and multiplying this by ~5 (trimmable), giving a maximal offset of ~500µV in the gain stage, corresponding to ±0.05°C, without specific trimming of **VREF1** to adjust for the offset voltage of **IC5A/B**.

SCHEMATIC – PAGE III

ANALOG-DIGITAL CONVERTER & DRIVE



SCHEMATIC – PAGE IV
CLOCKS & PWM DRIVE SIGNAL