Bharath Kumar Gajula

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Education

University of Florida, M.S. in Electrical and Computer Engineering Aug 2023 – May 2025
GPA: 3.53/4.00
Relevant Coursework: Reconfigurable computing, VLSI, AVLSI, Computer Architecture, Future of Microelectronics Technology, CAD for Hardware Security, Hands-on Hardware Security, Semiconductor Fabrication Lab, Formal Verification Methods.

B V Raju Institute of Technology, B.Tech in Electronics and Communication Engineering Jul 2017 – Jun 2021
GPA: 3.72/4

Technical Skills

HDL/RTL: SystemVerilog, Verilog, VHDL, FSMs, CDC, DFT, Low Power Design
Verification: Testbenches, UVM, Assertions (SVA), Code/Functional Coverage, Constrained Random Testing
EDA Tools: Cadence Virtuoso, Synopsys VCS, ModelSim, Vivado
Programming: Python, C, C++, TCL, LabVIEW
Platforms: Zedboard/Zynq FPGA, AWS, Azure

Experience

University of Florida, Graduate Research Assistant Jan 2025 – Present
- Architected a suite of Verilog/SystemVerilog modules supporting FPGA-based cryptographic identity validation and secure SVID issuance, aligned with SPIFFE protocols for multi-tenant isolation.
- Synthesized secure boot and attestation RTL logic with eFUSE key access, AIK signature generation, and workload hash computation; achieved 100% functional coverage.
- Orchestrated the integration of SPIRE agent plugins on FPGA hosts using Docker, SystemVerilog assertions, and bitstream signing logic; Fortified design confidentiality with sub-18% latency overhead.

Infor, Associate Software Engineer, DevOps Apr 2021 – Aug 2023
- Automated CI/CD processes using Python, accelerating deployment cycles by 50% and reducing manual intervention.
- Contributed to a 12-member team, delivering infrastructure enhancements that improved system reliability and scalability.
- Streamlined CI/CD workflows using Jenkins and Docker, allowing consistent containerized deployments and reducing build failures by 35%.

BVRIT, Undergraduate Research Scholar – Project SATYAM May 2019 – May 2020
- Integrated a structured real-time posture dataset with a back-end LabVIEW verification system, enabling consistent pattern validation and improving data processing efficiency by 30%.
- Applied pattern recognition techniques in LabVIEW to optimize posture detection logic, reducing false positives, and improving real-time response speed by 35%.

Projects

Constrained-Random Verification of FPGA RTL with AXI Protocol and UVM Framework Mar 2025 – May 2025
- Developed and verified complex FPGA subsystems using UVM methodology, implementing reusable sequences, monitors, and scoreboards for protocol checking, achieving 95% functional coverage and catching critical corner-case bugs pre-silicon.
- Built constrained-random and directed test-benches for AXI-based DUTs, employing System Verilog assertions and functional coverage models to validate data integrity, interface behavior, and protocol compliance across multiple simulation scenarios.

Formal Verification of the Binary Adder Aug 2024 – Dec 2024
- Designed and verified a parameterized bit-vector adder through ACL2, targeting edge cases like carry overflow
- Verified logical consistency across diverse conditions through formal theorem-proving techniques.
- Automated scenario generation for comprehensive state coverage

Fault-Tolerant Security Fabric on FPGA Jan 2024 – May 2024
- Implemented TMR-based fault-tolerant logic with dynamic reconfiguration on FPGA
- Achieved >90% functional coverage and identified failure modes via fault injection and regression.
- Synthesized secure logic with minimal area and timing overhead

4x2 SRAM Array Design Aug 2023 – Dec 2023
- Designed a full-custom 4x2 SRAM layout in Cadence with integrated decoder, precharge, and sense amp modules.
- Verified design using DRC, LVS, and transient analysis; ensured seamless integration of all support blocks.

1D Convolution Accelerator on Zedboard Aug 2023 – Dec 2023
- Built pipeline convolution accelerator with DMA-AXI integration on Zynq FPGA
- Enhanced performance by 3x through optimized memory handling and dataflow design
- Validated implementation through RTL simulation and hardware-in-the-loop testing

Explored RISC-V Architecture Using gem5 Simulator Aug 2023 – Dec 2023
- Simulated and analyzed RISC-V, x86, and ARM processor architectures using gem5, evaluating performance metrics under varying micro-architectural configurations, including L1/L2 cache hierarchies and custom workloads.
- Identified bottlenecks in RISC-V performance through verification of execution traces and architectural behavior, implementing workload-based cache tuning and comparing functional correctness across ISAs to validate micro-architectural optimizations.