EE 618: CMOS Analog VLSI Design

Assignment 2

Student Name: Bhuvansh Goyal
Roll Number: 22B3908
Instructor: Prof. Rajesh Zele
Submission Date: 10 Sep 2025

Contents

1 Design Specifications

The objective of this assignment is to design a Common Source PMOS Amplifier with a resistive load using the GPDK 45nm technology. The complete circuit is illustrated in Figure **??**. The core amplifier block, highlighted in red, must be designed to meet the following performance specifications:
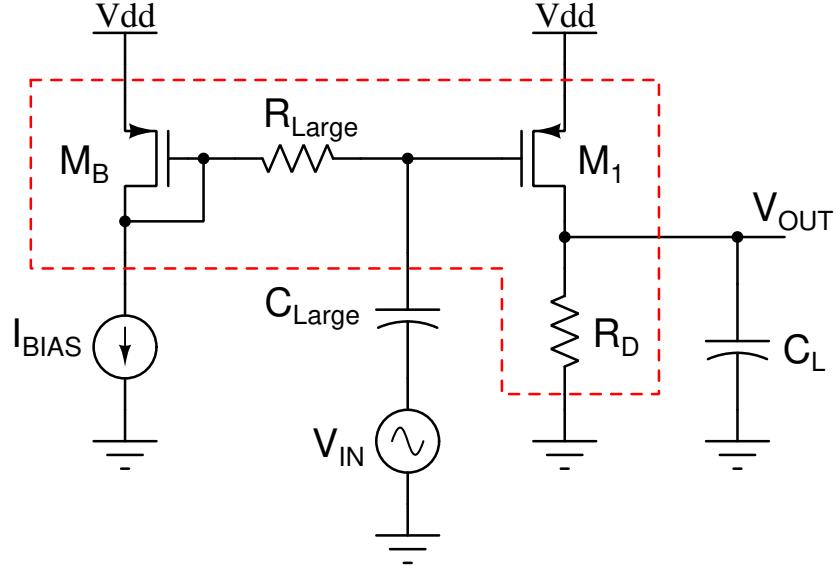

Figure 1: Circuit diagram of the Common Source PMOS Amplifier. The core amplifier cell to be designed is highlighted in red.

The target performance metrics and operating conditions are:

- **DC Gain** ($A_{v,DC}$): $\geq 18\,\text{dB}$

- **3dB Cut-off Frequency** (f_{3dB}): $\geq 4\,\text{MHz}$

- **DC Output Voltage** ($V_{OUT,DC}$): $900 \pm 50\,\text{mV}$

- **Power Dissipation** (P_{diss}): $\leq 0.6\,\text{mW}$

The amplifier is to be designed with the following fixed parameters:

- **Supply Voltage** (V_{DD}): $1.8\,\text{V}$

- **Bias Current** (I_{BIAS}): $20\,\mu\text{A}$

- **Load Capacitance** (C_L): $10\,\text{pF}$

2 Hand Calculations

Hand calculations were performed to determine the initial design values based on the given specifications. This included extracting process parameters and applying small-signal analysis to obtain design constraints.

2.1 Process Parameter Extraction

The values of $\mu_p C_{ox}$ and λ for the GPDK 45 nm PMOS transistor were obtained from DC simulations using the testbench in Figure **??**. These were read directly from the device operating point data.
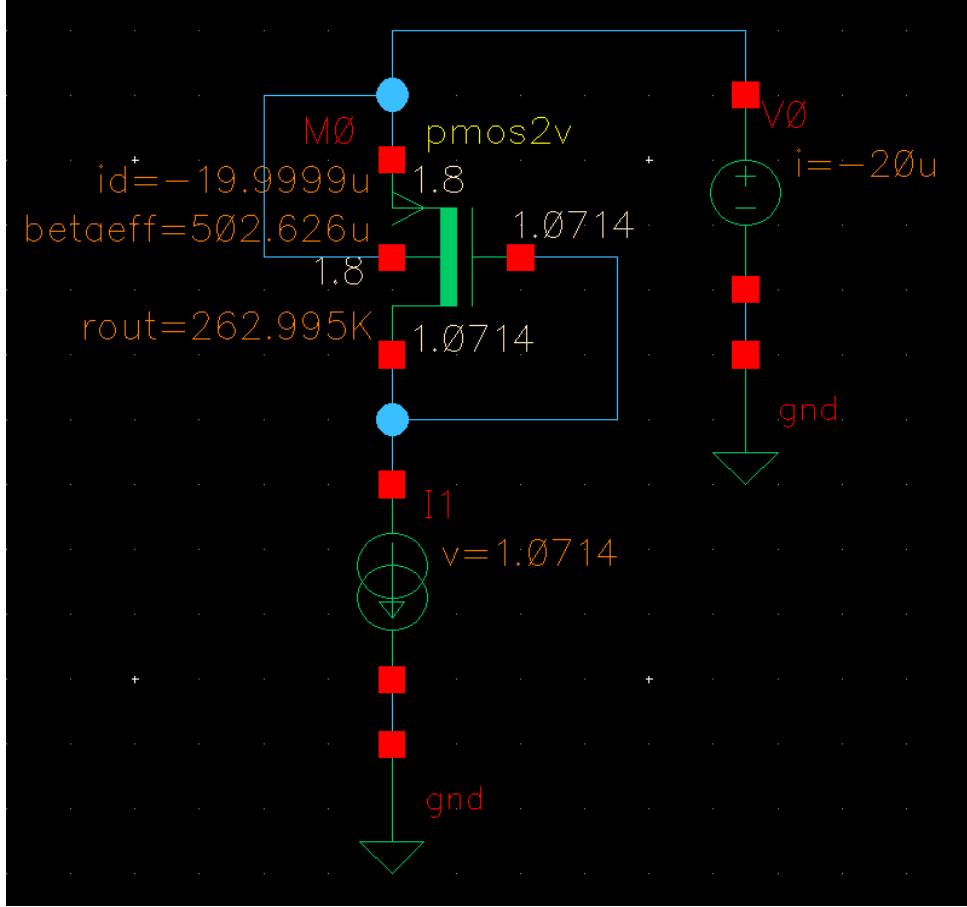

Figure 2: DC testbench for PMOS parameter extraction.

The extracted values are:

- $\mu_p C_{ox} \approx 200\,\mu\text{A/V}^2$

- $\lambda \approx 0.2\,\text{V}^{-1}$

2.2 Small-Signal Analysis and Design Constraints

The small-signal model of transistor M1 (Figure **??**) was used to derive the amplifier transfer function. The intrinsic capacitances of the PMOS are neglected since the load capacitance C_L is dominant.
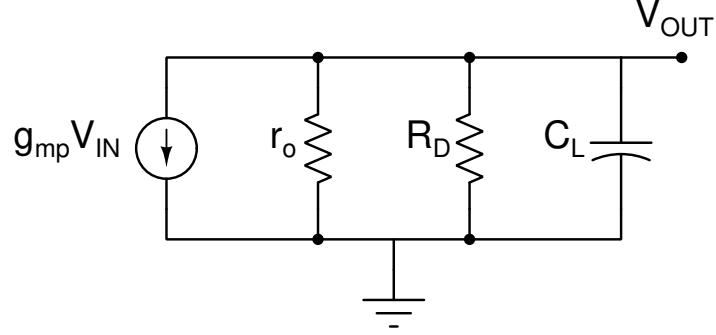
Figure 3: Small-signal model of M1.

The gain transfer function is

$$A_v(s) = \frac{-g_{mp}\,(r_o \parallel R_D)}{1 + sC_L(r_o \parallel R_D)}. \tag{1}$$

2.2.1 DC Gain Constraint

For $s = 0$, the DC gain is

$$\begin{aligned}
|A_{v,DC}| = g_{mp}\,(r_o \parallel R_D) &\geq 10^{18/20} \\
&\geq 7.94 \approx 8 \tag{2}
\end{aligned}$$

2.2.2 3dB Frequency Constraint

The $3\,\mathrm{dB}$ frequency is

$$f_{3dB} = \frac{1}{2\pi C_L(r_o \parallel R_D)}.$$

For $C_L = 10\,\mathrm{pF}$ and $f_{3dB} \geq 4\,\mathrm{MHz}$,

$$\begin{aligned}
(r_o \parallel R_D) &\leq \frac{1}{2\pi \times 10^{-11} \times 4 \times 10^6} \\
&\leq 3.98\,\mathrm{k\Omega} \approx 4\,\mathrm{k\Omega}. \tag{3}
\end{aligned}$$

We take

$$(r_o \parallel R_D) = 3.8\,\mathrm{k\Omega} \tag{4}$$

for further calculations.

2.2.3 DC Gain Constraint

From the DC gain constraint, we have

$$\begin{aligned}
g_{mp} &\geq \frac{8}{3.8\ \mathrm{k\Omega}} \\
&\geq 2\,\mathrm{mS}. \tag{5}
\end{aligned}$$

2.2.4 Output Voltage and Drain Current

Using the output DC voltage requirement,

$$I_{SD} = \frac{0.9}{R_D}. \tag{6}$$

The small-signal output resistance is

$$r_o = \frac{1}{\lambda I_{SD}} = \frac{R_D}{\lambda \cdot 0.9}.$$

Substituting the values of λ and r_o into Equation **??** gives

$$R_D = 4.484\,\text{k}\Omega \approx 4.5\,\text{k}\Omega.$$

Using this R_D in Equation **??**, the drain current is

$$I_{SD} = \frac{0.9}{4.5\text{ k}\Omega} \approx 200\,\mu\text{A}.$$

2.2.5 Transistor Sizing

The transconductance of a PMOS transistor in saturation is

$$g_{mp} = \sqrt{2I_{SD}\mu_p C_{ox}\frac{W}{L}}.$$

Using the requirement $g_{mp} \geq 2\,\text{mS}$ and the calculated drain current $I_{SD} = 200\,\mu\text{A}$, we obtain

$$W \geq 21.76\,\mu\text{m} \approx 22\,\mu\text{m}.$$

The channel length was chosen as $L = 400\,\text{nm}$.

For transistor M_B, which carries one-tenth the current of M_1, the width scales proportionally:

$$W_B = 0.1 \times W_{M1} \approx 2.2\,\mu\text{m}.$$

2.3 Final Component Values

Based on the derived constraints and the design specifications (particularly $V_{OUT,DC} = 0.9\,\text{V}$ and $I_D = 200\,\mu\text{A}$ for M1), the final component values were calculated. The load resistor R_D was chosen to set the DC output voltage. The aspect ratio of the main amplifier transistor M1 was then determined to meet the DC gain requirement, while the bias transistor MB was sized to mirror the reference current.

The final calculated values are summarized in Table **??**.

Table 1: Final Component Values from Hand Calculations

| Component	Parameter	Value
Amplifier PMOS (M1)	Width (W)	22 μm
	Length (L)	400 nm
Bias PMOS (MB)	Width (W)	2.2 μm
	Length (L)	400 nm
Load Resistor (R_D)	Resistance	4.5 kΩ
Bias Resistor (R_{Large})	Resistance	7.5 kΩ
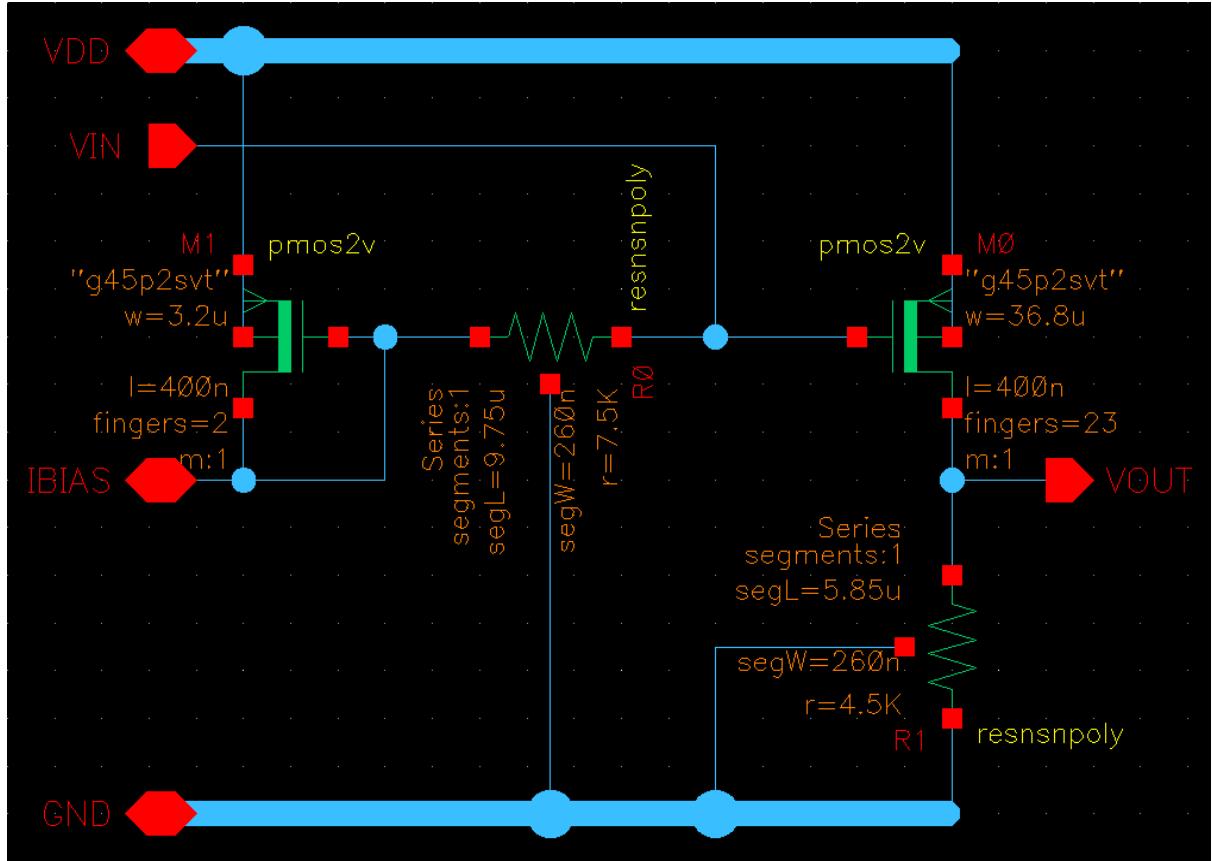
3 Schematic

Figure 4: Amplifier schematic with annotated device sizes.

The final transistor widths in the implemented design are larger than the hand-calculated values. This adjustment was necessary because the effective $\mu_p C_{ox}$ (observed in M1) decreased to approximately $160\,\mu\text{A}/\text{V}^2$, requiring wider devices to achieve the specified drain current.

4 DC Analysis
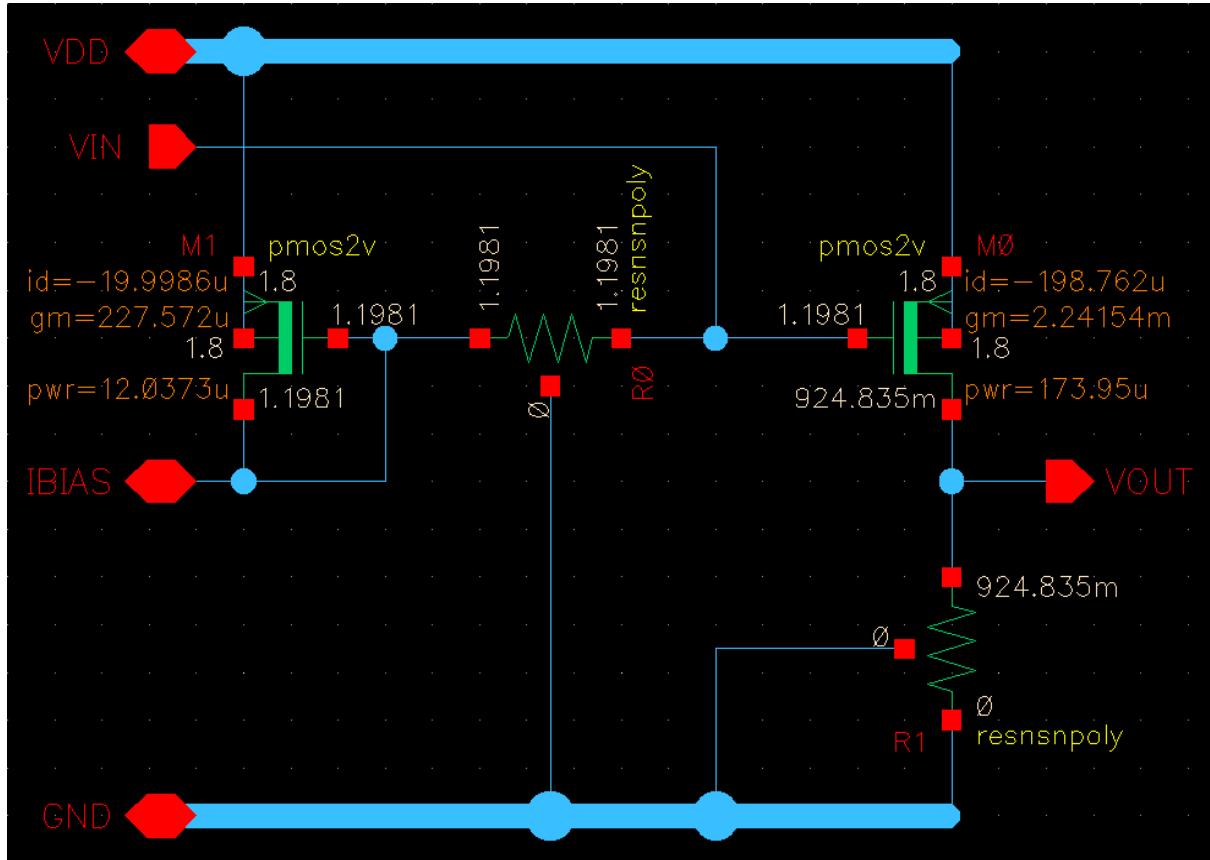
Figure 5: DC operating point analysis of the amplifier.

The total power consumption of the amplifier was calculated as:

$$P_{\text{total}} = 12.0373 \ \mu\text{W} + 173.95 \ \mu\text{W} + (0.924835 \times 198.762 \ \mu\text{W}) \approx 0.37 \ \text{mW}.$$

5 AC Analysis
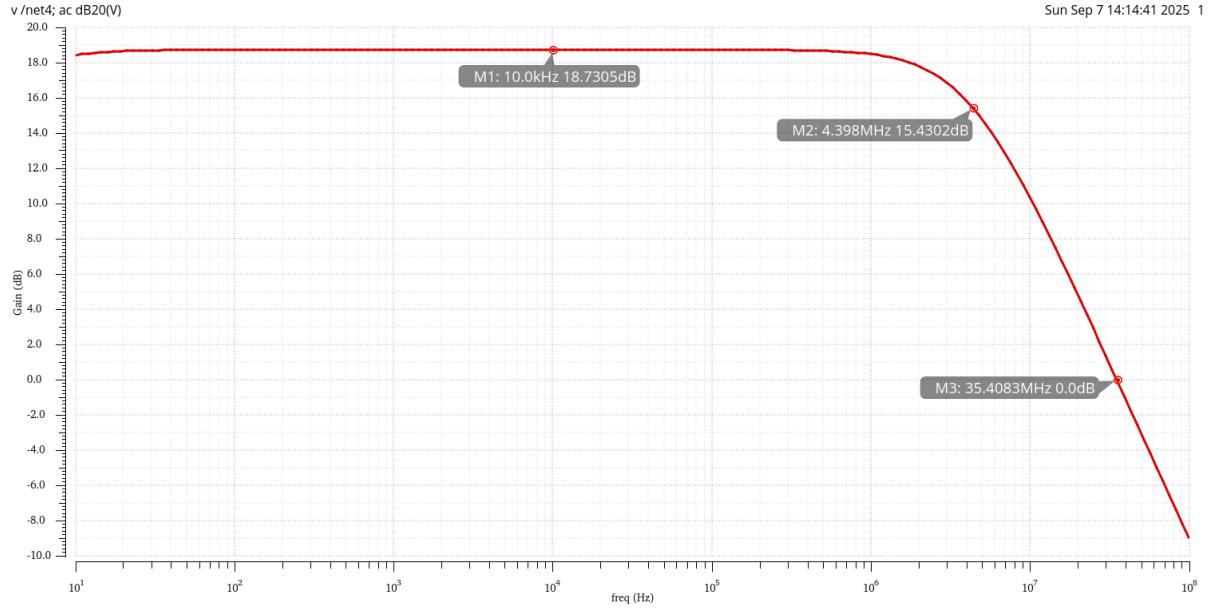
Figure 6: AC frequency response of the amplifier.

From the AC sweep results shown in Figure **??**, the following key parameters were obtained:

- Gain at $10\,\mathrm{kHz}$: $18.7305\,\mathrm{dB}$

- $3\,\mathrm{dB}$ cutoff frequency: $4.398\,\mathrm{MHz}$

- Unity-gain frequency: $35.4083\,\mathrm{MHz}$

6 Transient Analysis
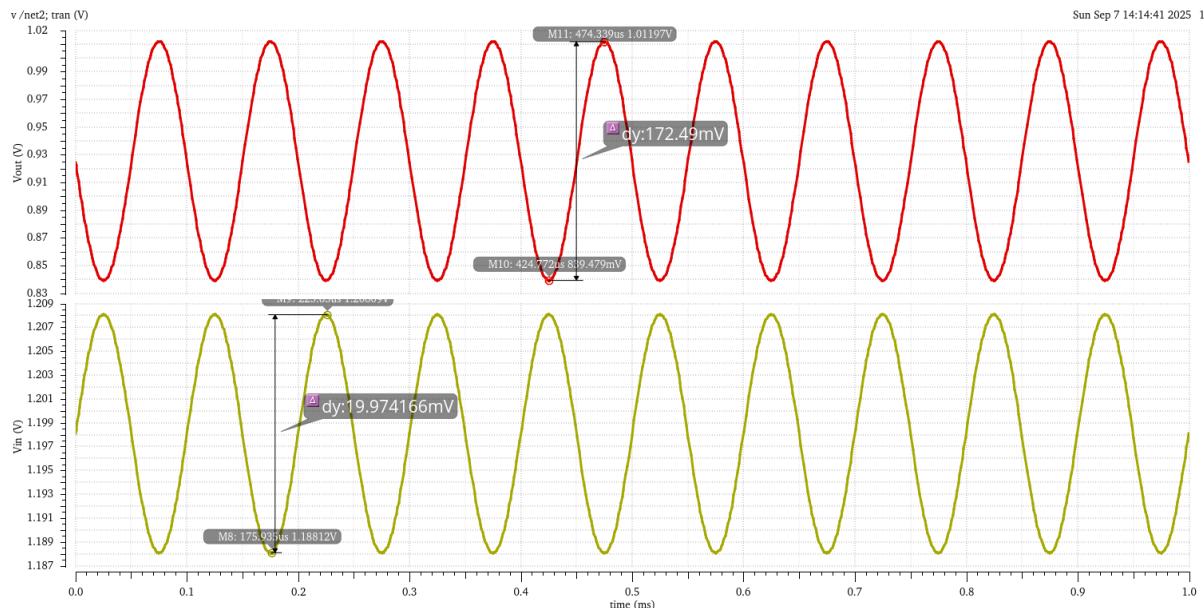
Figure 7: Transient response of the amplifier.

From the transient simulation shown in Figure **??**, the measured peak-to-peak values are:

- $V_{\text{out,pp}} = 172.49\,\text{mV}$

- $V_{\text{in,pp}} = 20\,\text{mV}$

The corresponding voltage gain is

$$A_v = \frac{V_{\text{out,pp}}}{V_{\text{in,pp}}} = \frac{172.49}{20} \approx 8.625 \quad (18.71\,\text{dB}).$$

7 Corner Analysis

Corner simulations were performed for six process corners: *Typical*, *Fast*, and *Slow*, each at 0°C and 100°C. The corresponding AC and transient analysis results are shown below.

7.1 AC Analysis
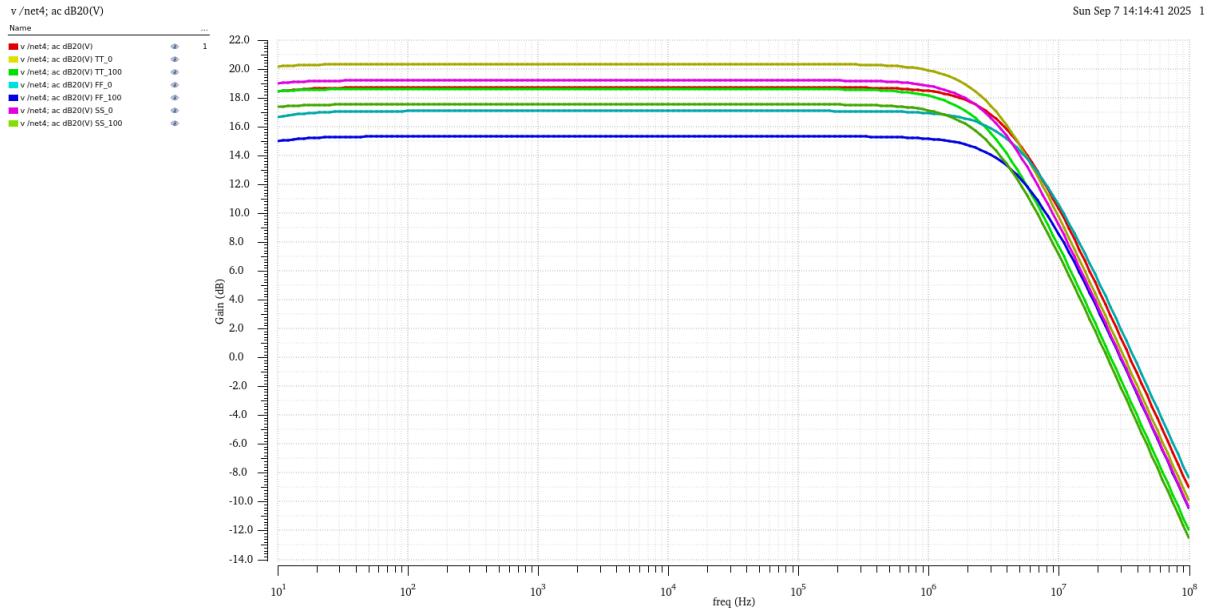
Figure 8: AC analysis plots for all corner cases (Typical, Fast, Slow at 0°C and 100°C).

7.2 Transient Analysis
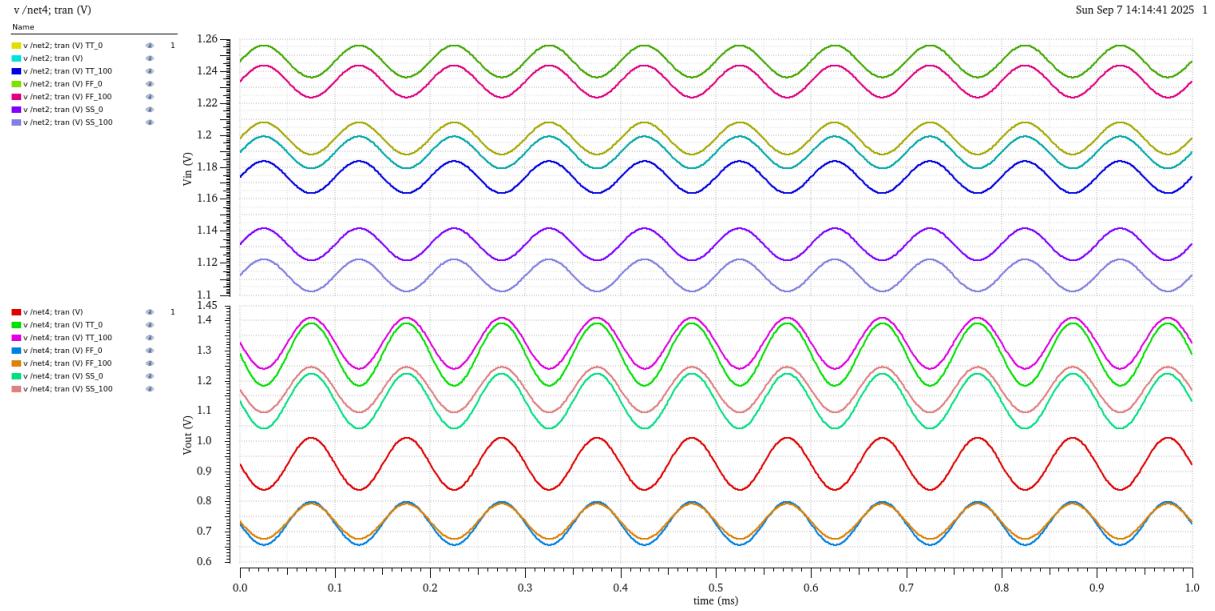
Figure 9: Transient analysis plots for all corner cases (Typical, Fast, Slow at 0°C and 100°C).

## 8 Layout
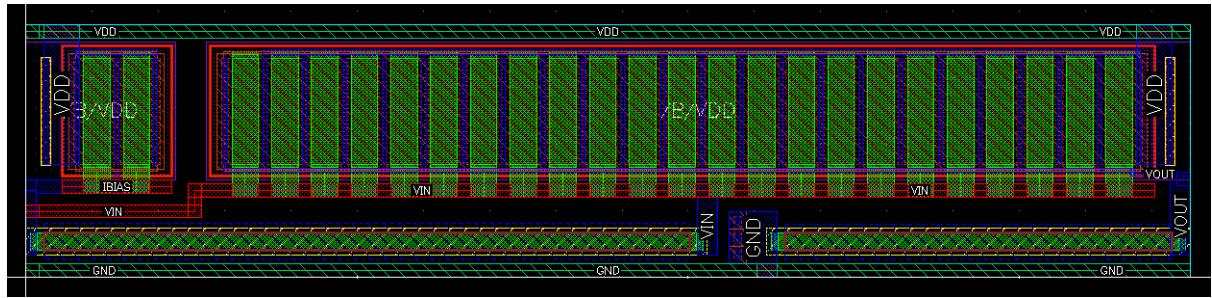
Figure 10: Layout of the designed amplifier.

## 8.1 Clean DRC and LVS
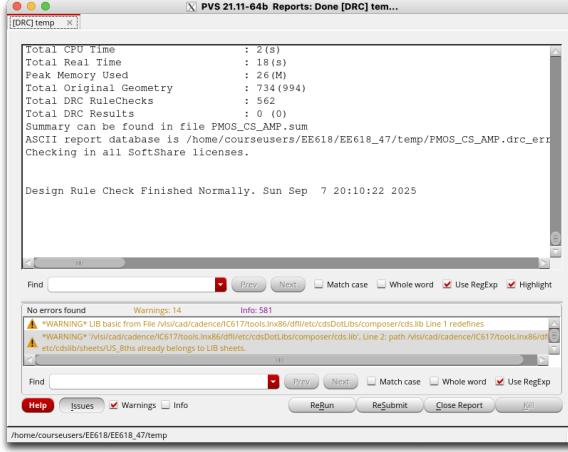
Figure 11: Clean DRC check.
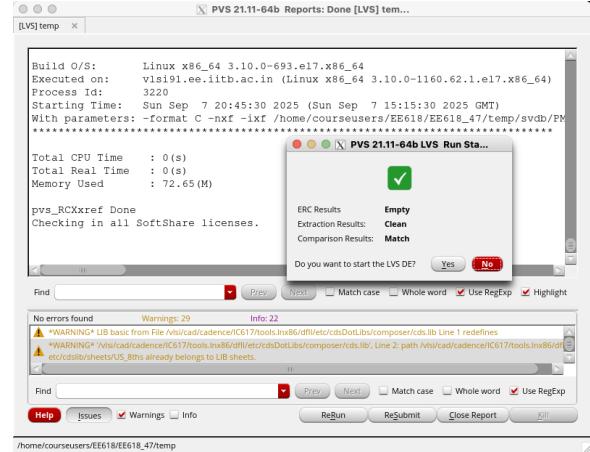
Figure 12: Clean LVS check.

9 PEX Analysis

9.1 AC Analysis
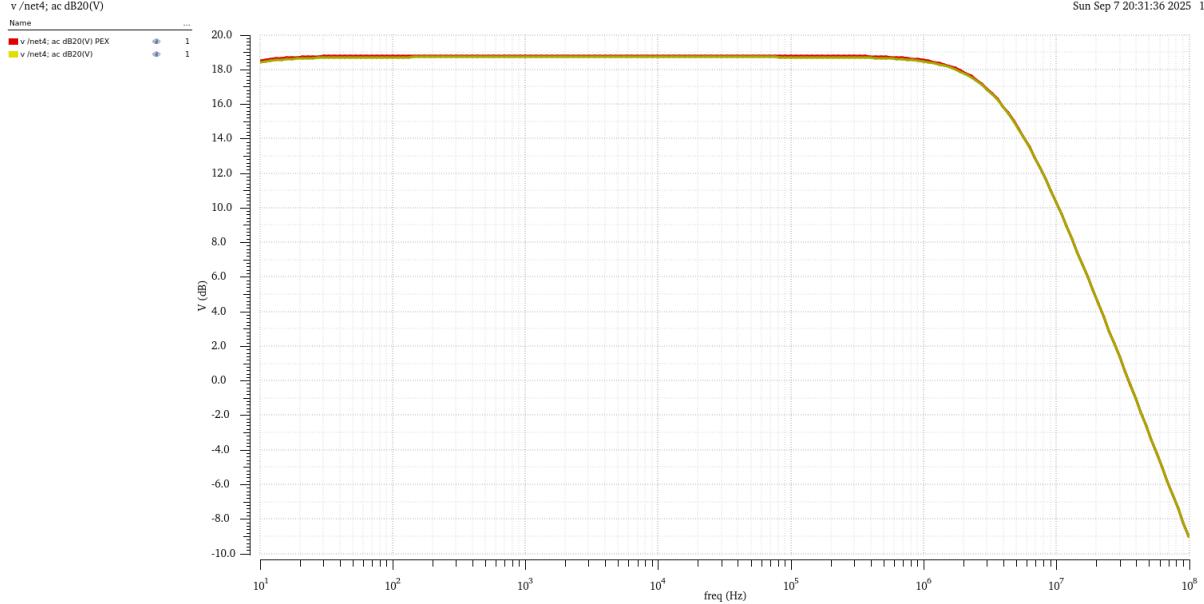
Figure 13: AC analysis after post-layout extraction (PEX).

The DC gain after PEX was measured as 18.81 dB, compared to 18.73 dB before PEX.

9.2 Transient Analysis
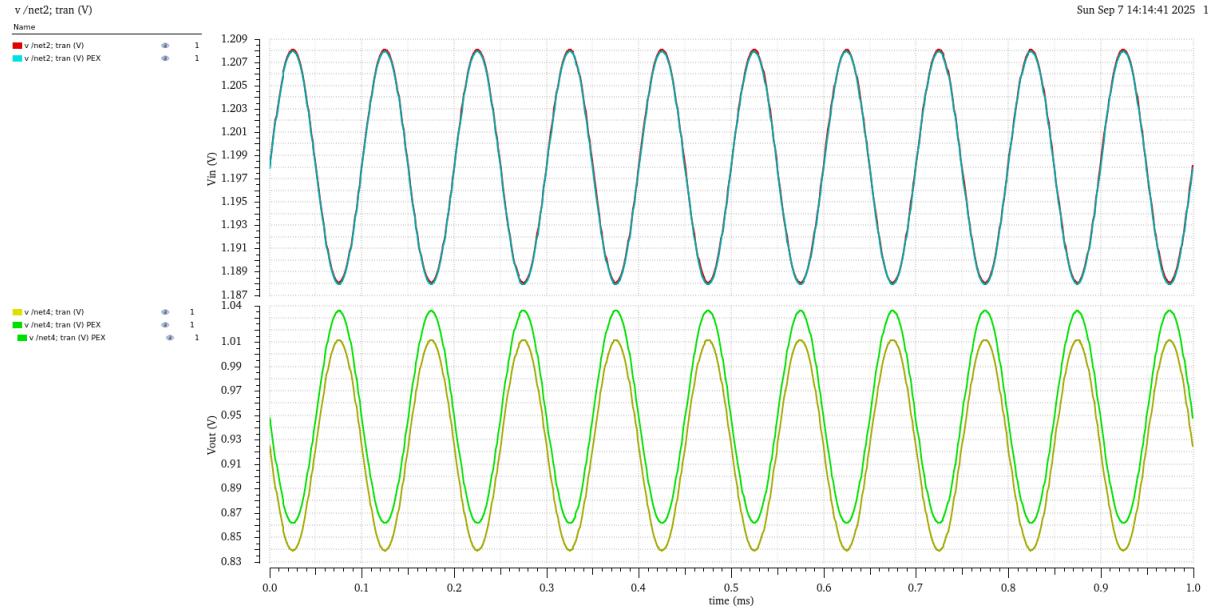
Figure 14: Transient analysis after post-layout extraction (PEX).

The output peak-to-peak voltage after PEX was 174 mV, compared to 172 mV before PEX.