CMOS XOR Gate

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Theory of Operation

- When A is high, and B is low the output Y is high
- When both A and B are high, the output Y is 0
- An XOR gate differs from a simple OR gate, which would output high if both A and B were high

A	B	A’	B’	Y
0	0	1	1	0
1	0	0	1	1
0	1	1	0	1
1	1	0	0	0

Circuit Design Equations

Y = A XOR B

Y = AB’ + A’B

Pull Up:

Y = AB’ + A’B

Pull Down:

Y’ = (AB’ + A’B)’

Y’ = (AB’)’ * (A’B)’

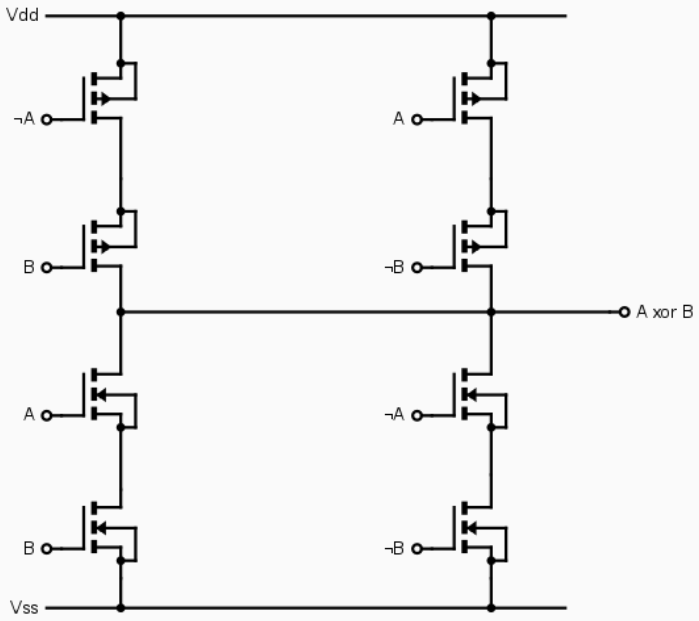
Y’ = (A’+B) * (A+B’)

Y’ = (A*A’) + (B*’A’) +

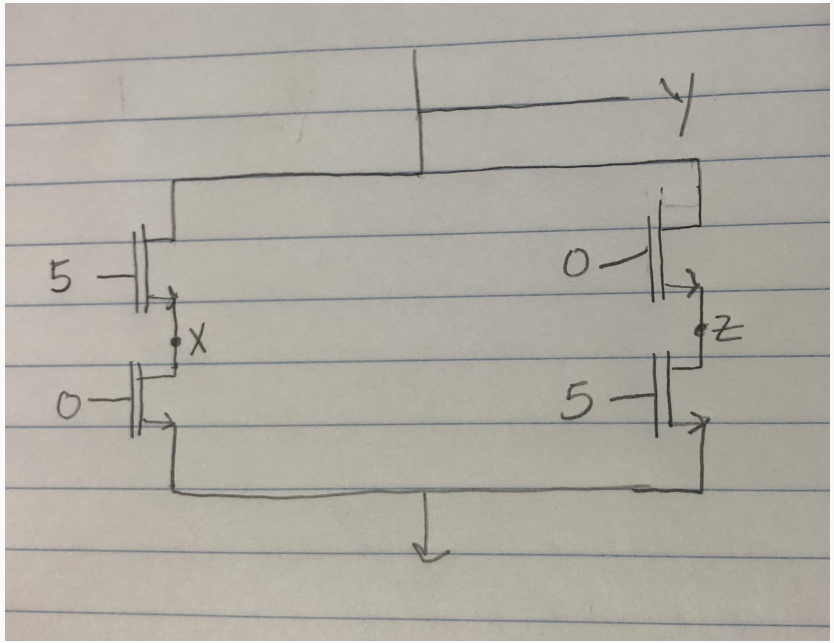
(B*A) +(B*B’)

Y’ = (A*B) + (A’*B’)

CMOS XOR Gate

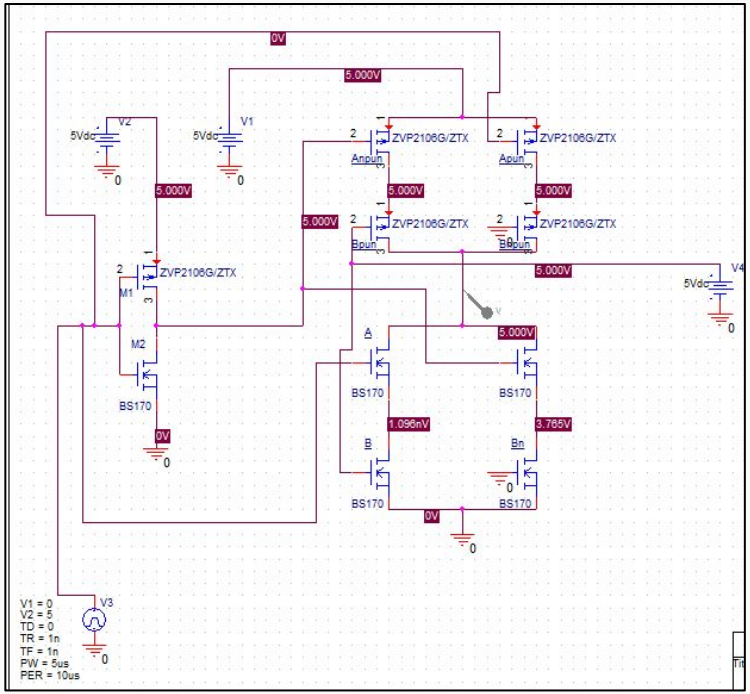


Voltages Across the MOSFETS



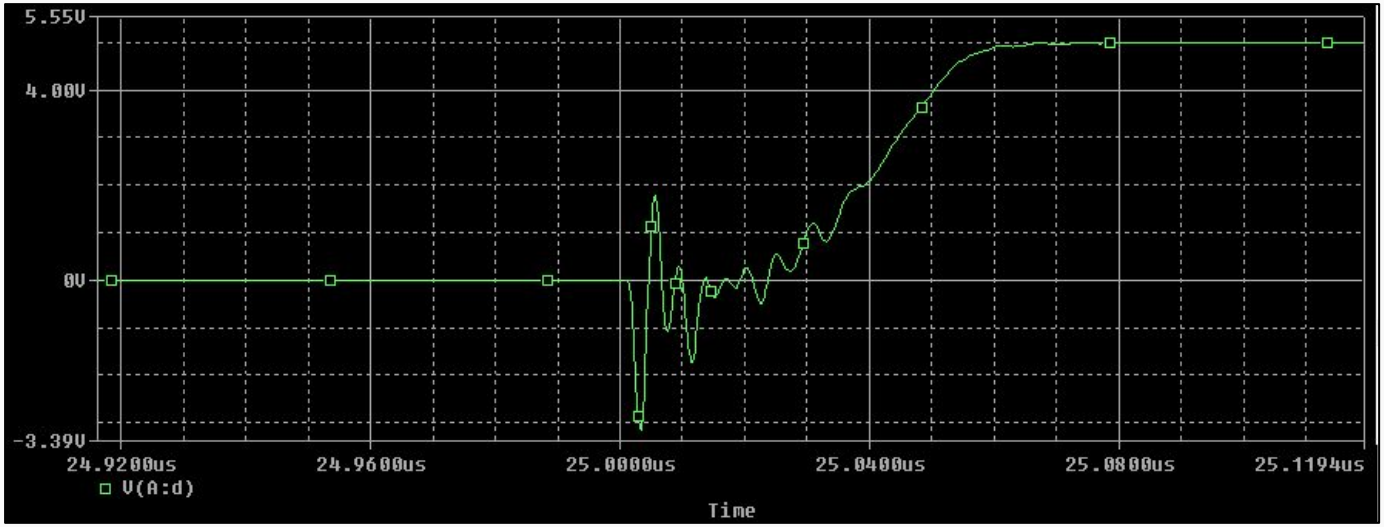
X	Z
5 V	0 V

SPICE Simulations



Active Pull-Up Network

Active Pull-Up Transient Time Response



Specifications::

- 5 us pulse width
- 10 us period time
- 100 us run time

Propagation time:

- 0.04 us

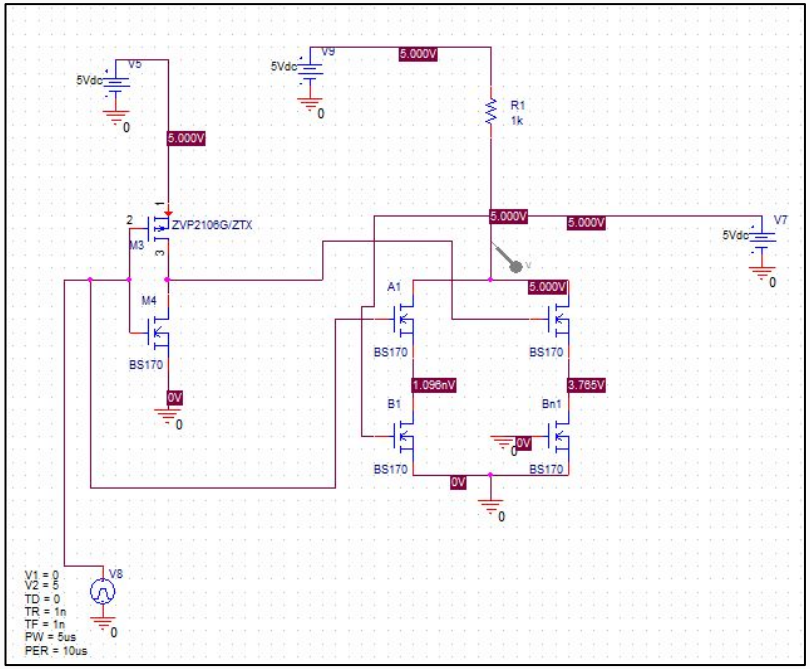
Specifications:

1. 50 us pulse width
2. 100 us period time
3. 1000 us run time

Propagation delay:

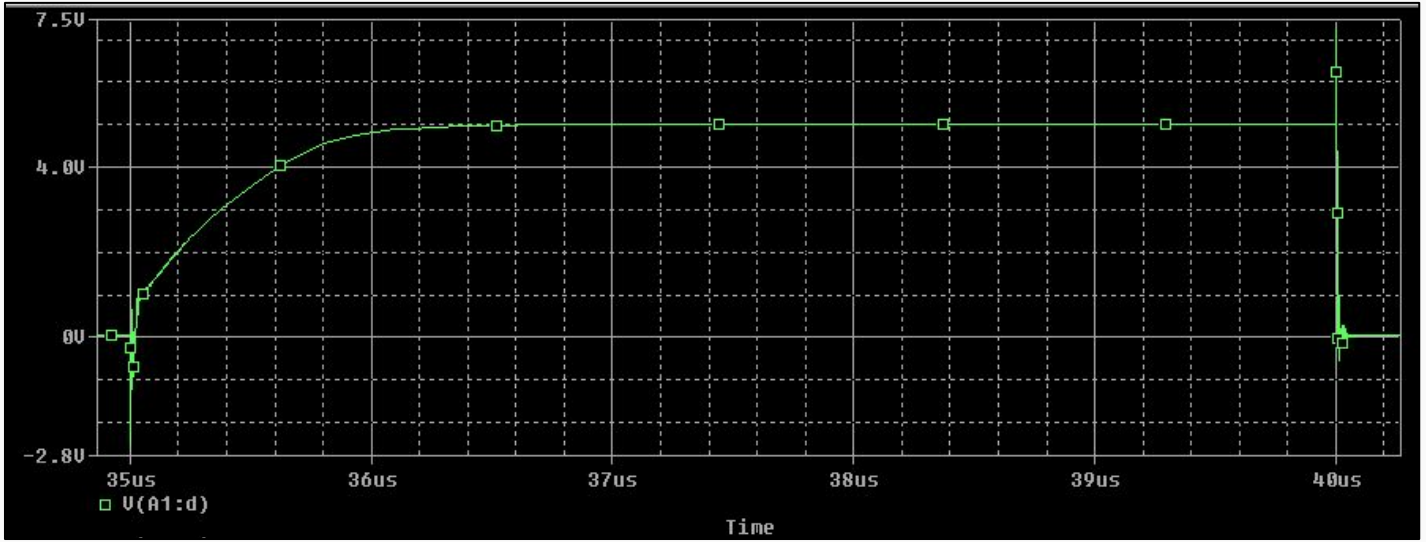
- 0.04 us

SPICE Simulations Continued



Resistive Pull-Up Network

Transient Time Response 1k Ohms

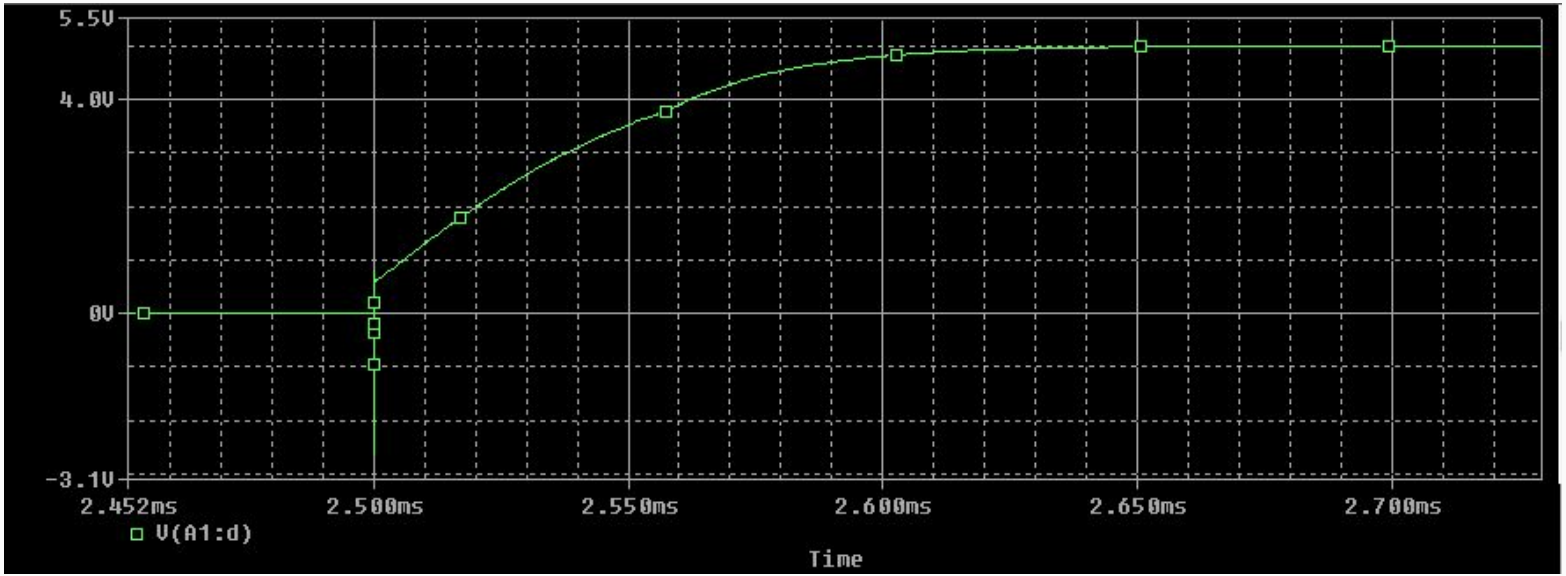


Specifications:

- 5 us pulse width
- 10 us period time
- 100 us run time

Propagation delay:

- 0.5 us



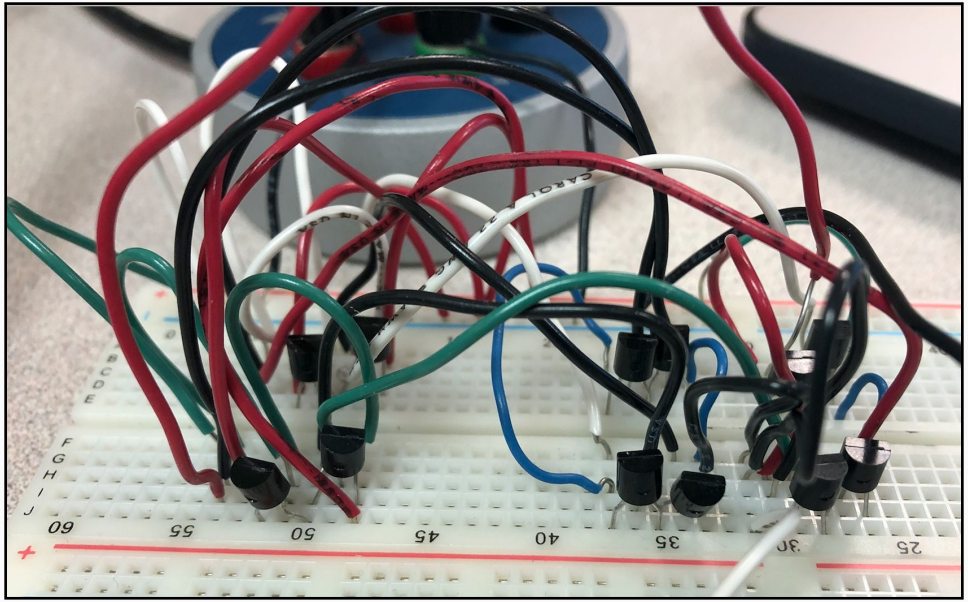
Specifications:

- 500 us pulse width
- 1000 us period time
- 10000 us run time

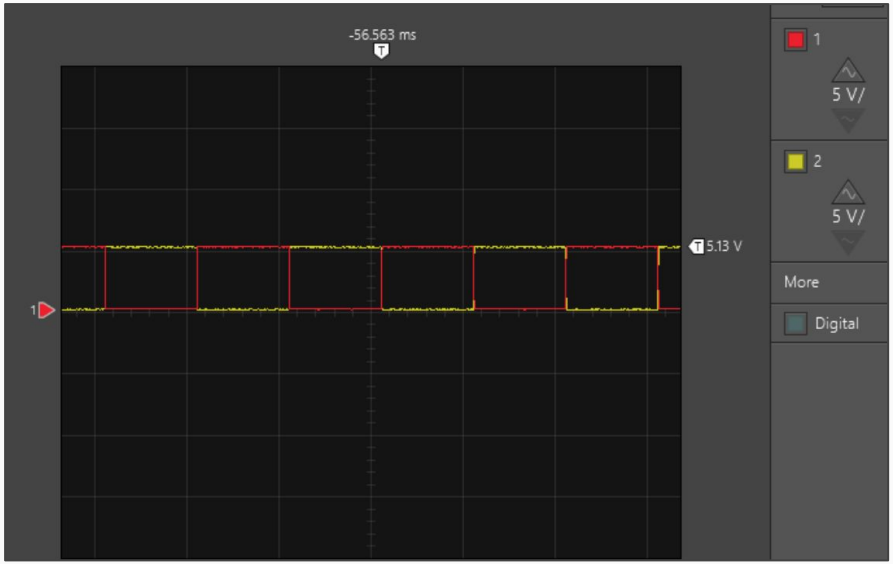
Propagation Delay:

- 0.55 us

Circuit Constructed



Results



A	B	A’	B’	Y
0 V	0 V	5 V	5 V	.109 V
5 V	0 V	0 V	5 V	5.01 V
0 V	5 V	5 V	0 V	5.01 V
5 V	5 V	0 V	0 V	.109 V

Observations and Analysis

- Measured truth table aligns with theoretical truth table
- When voltage at the resistor is 0, the voltage = 5-0 so the power is 5^2/R
- When voltage at the resistor is 5, the voltage = 5-5 so the power is 0