XOR Gate Using CMOS Logic

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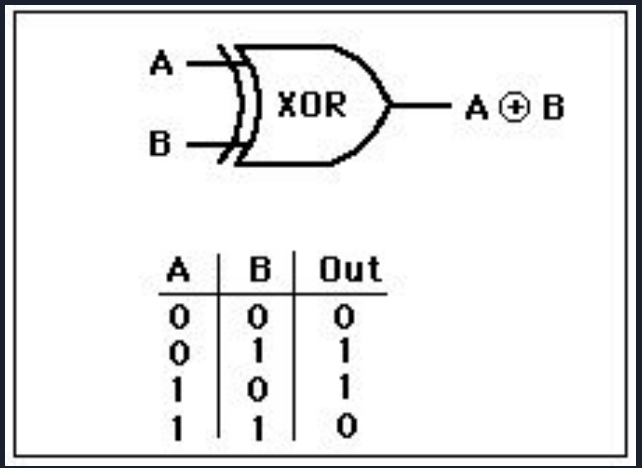
ELC 383

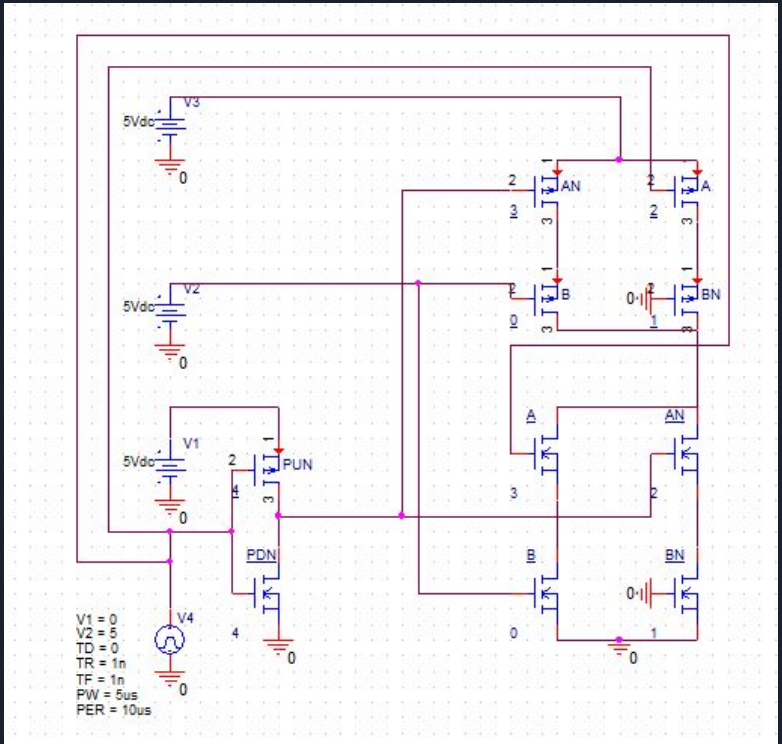
XOR Gate Background

- Either A or B high will output high
- Both A and B high will output low
- Both A and B low will output low



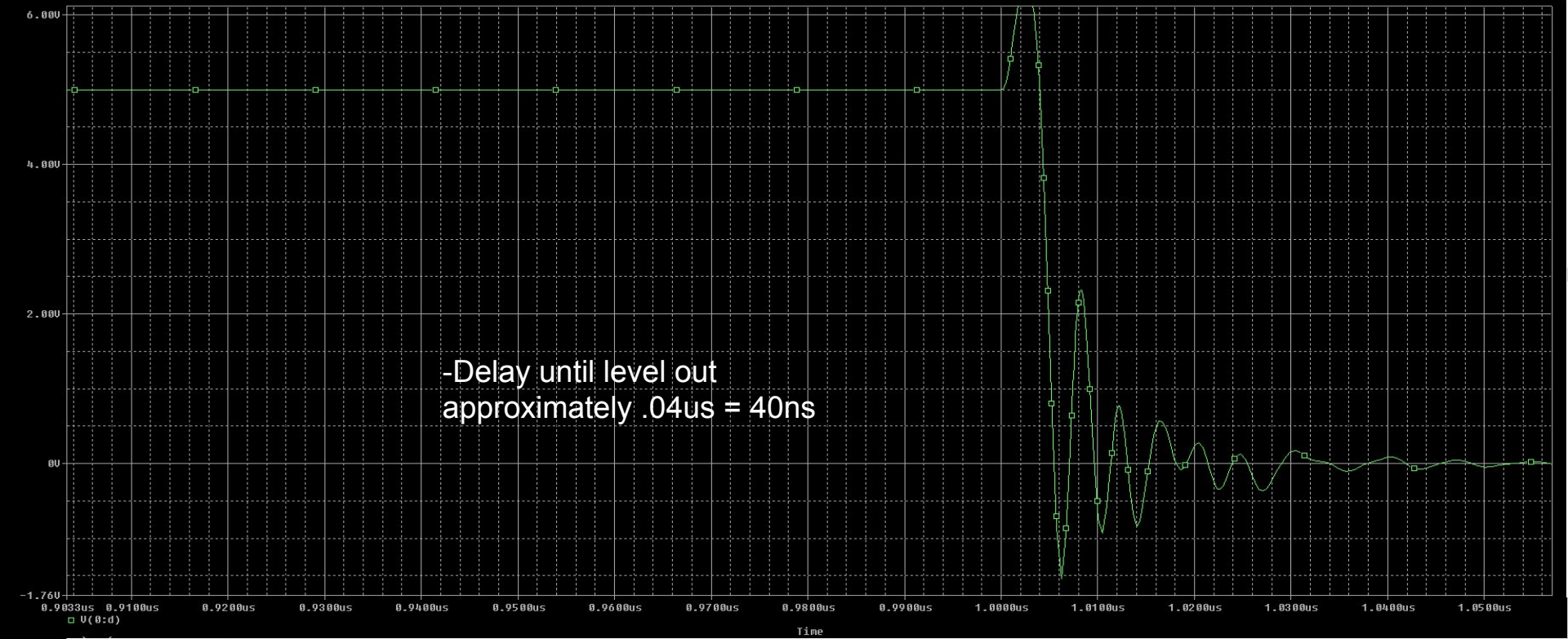
A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

PSPICE CMOS Circuit Design

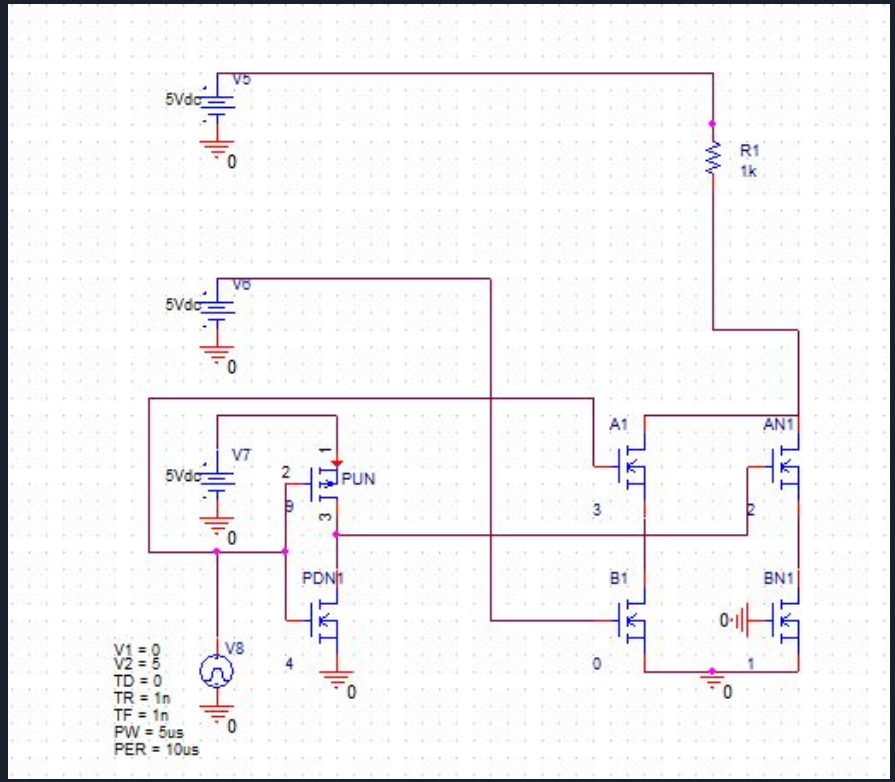


Simulation Results (Active Pull Up - Rising Edge)

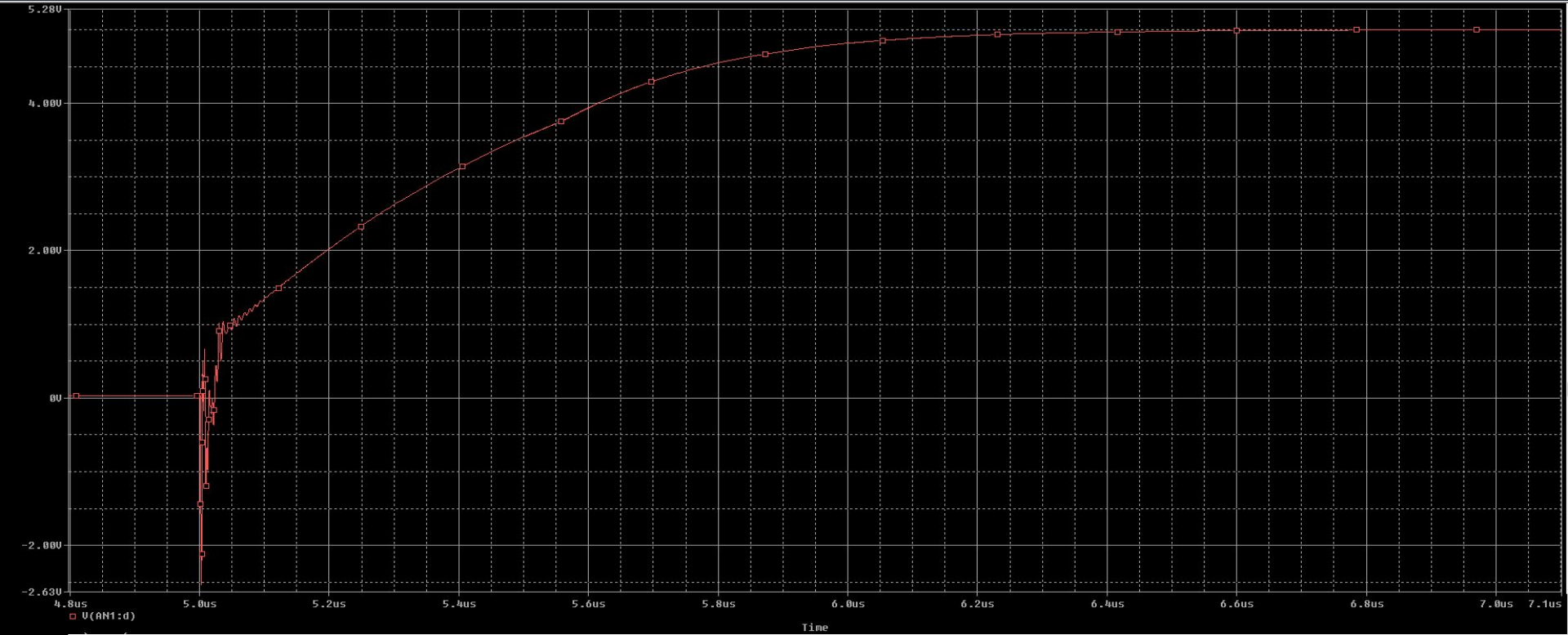
Simulation Results (Active Pull Up - Falling Edge)



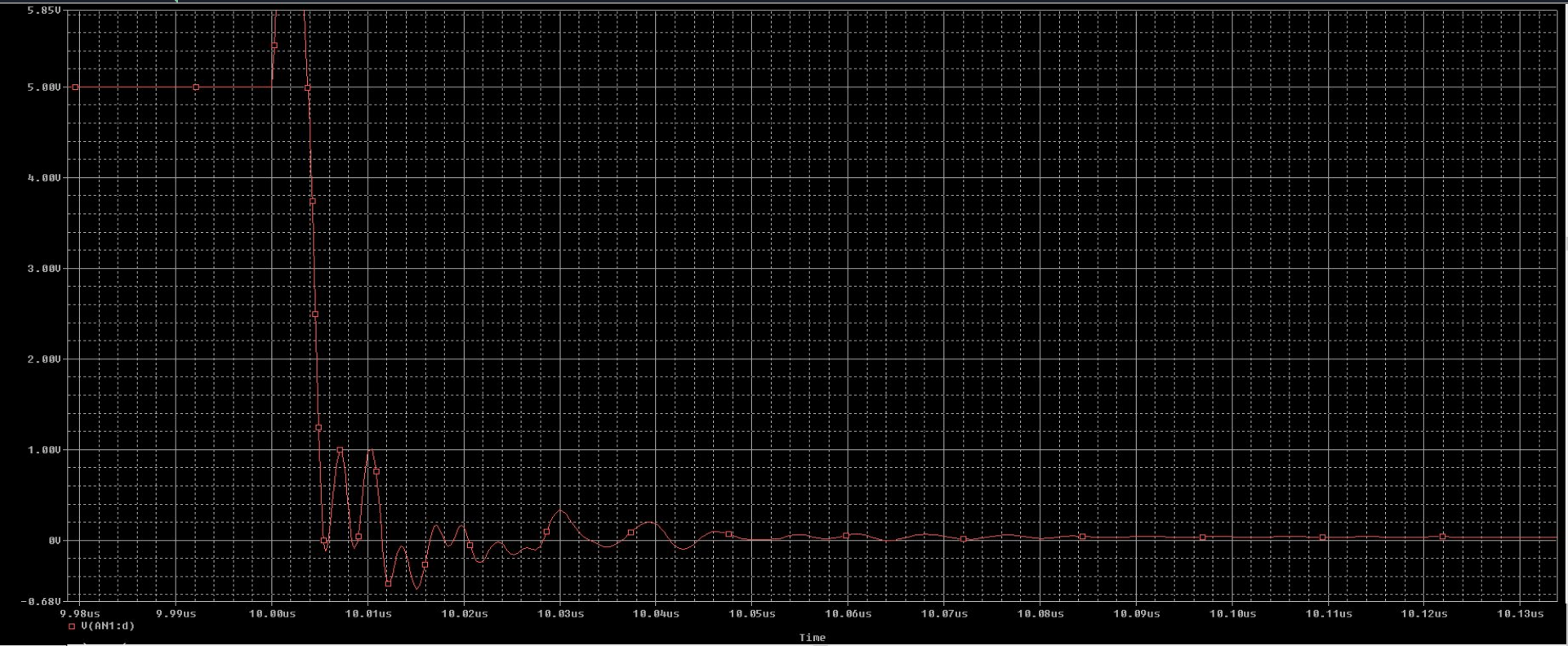
PSPICE RTL Circuit Design



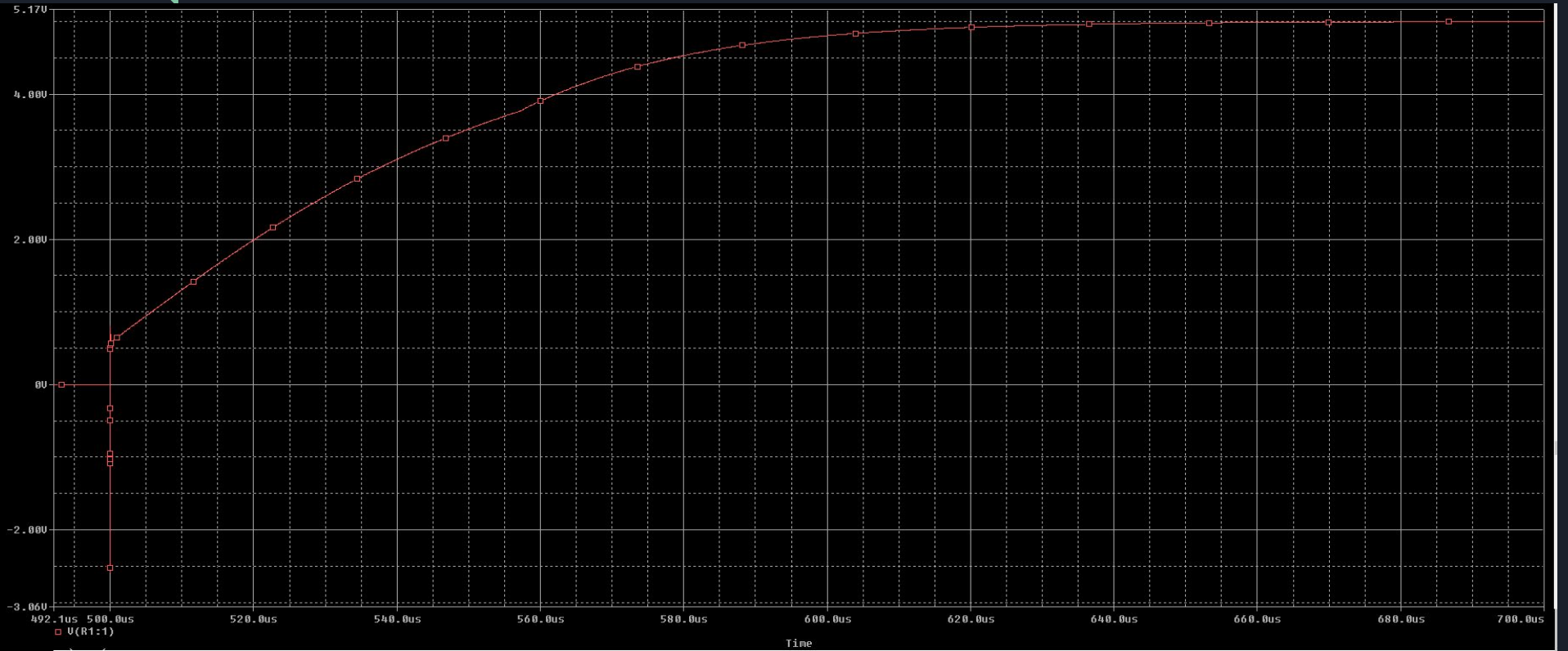
Simulation Results (Resistive pull up Rising edge 1k)



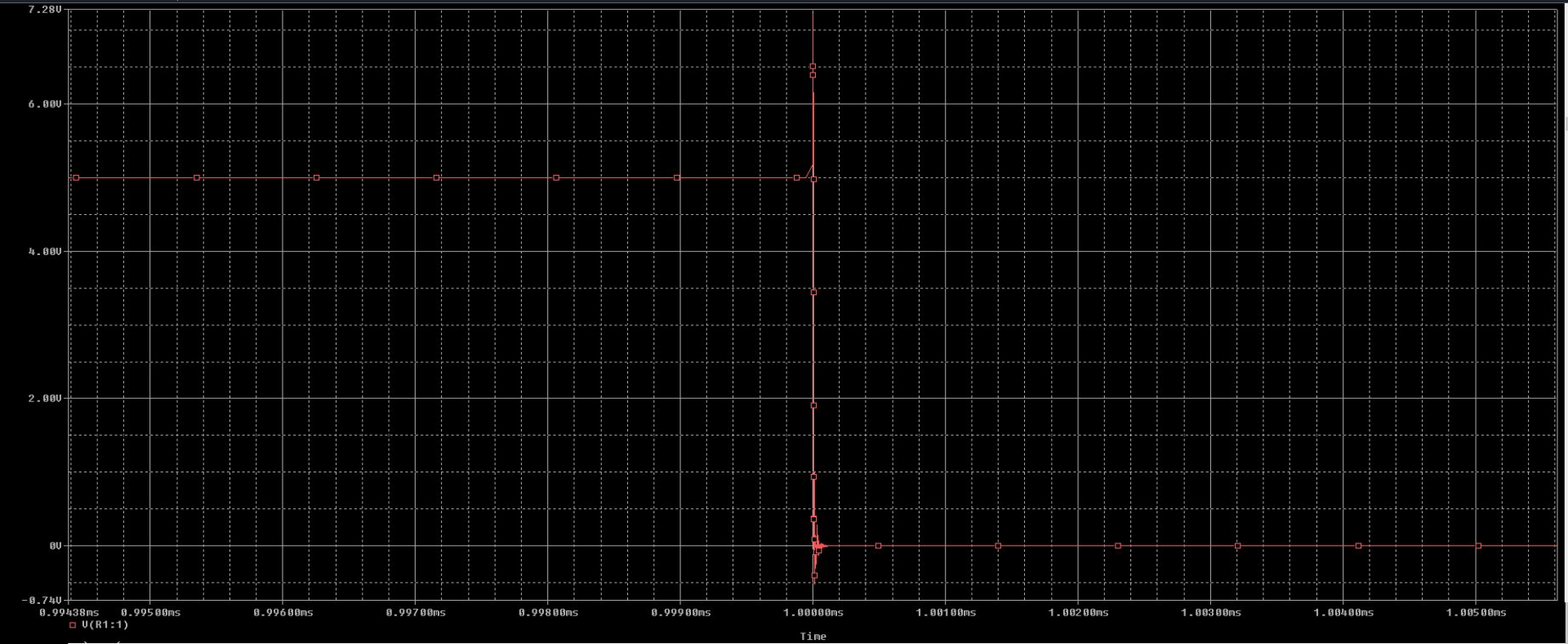
Simulation Results (Resistive pull up Falling edge 1k)



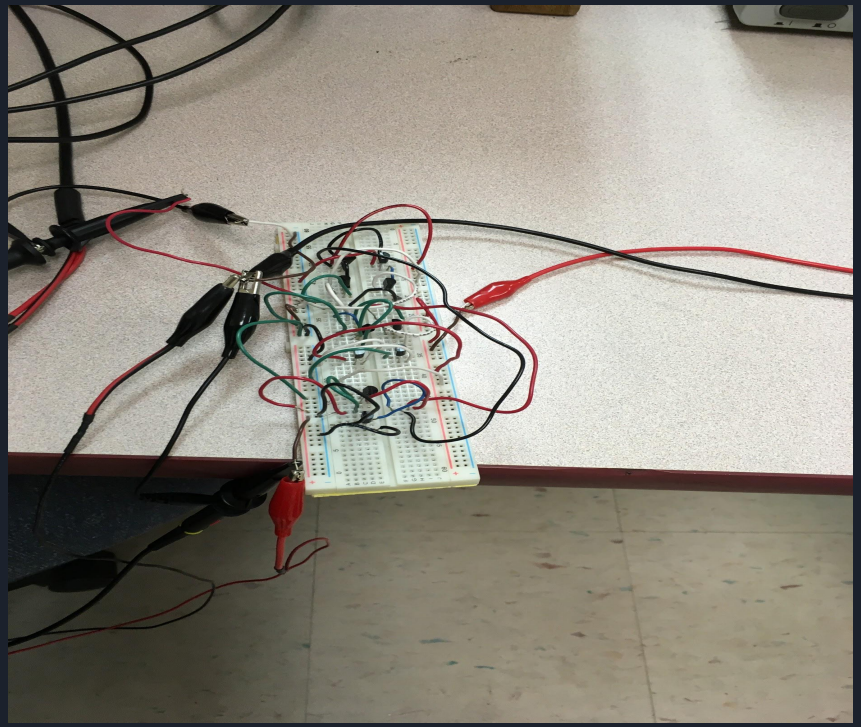
Simulation Results (Resistive pull up Rising edge 100k)



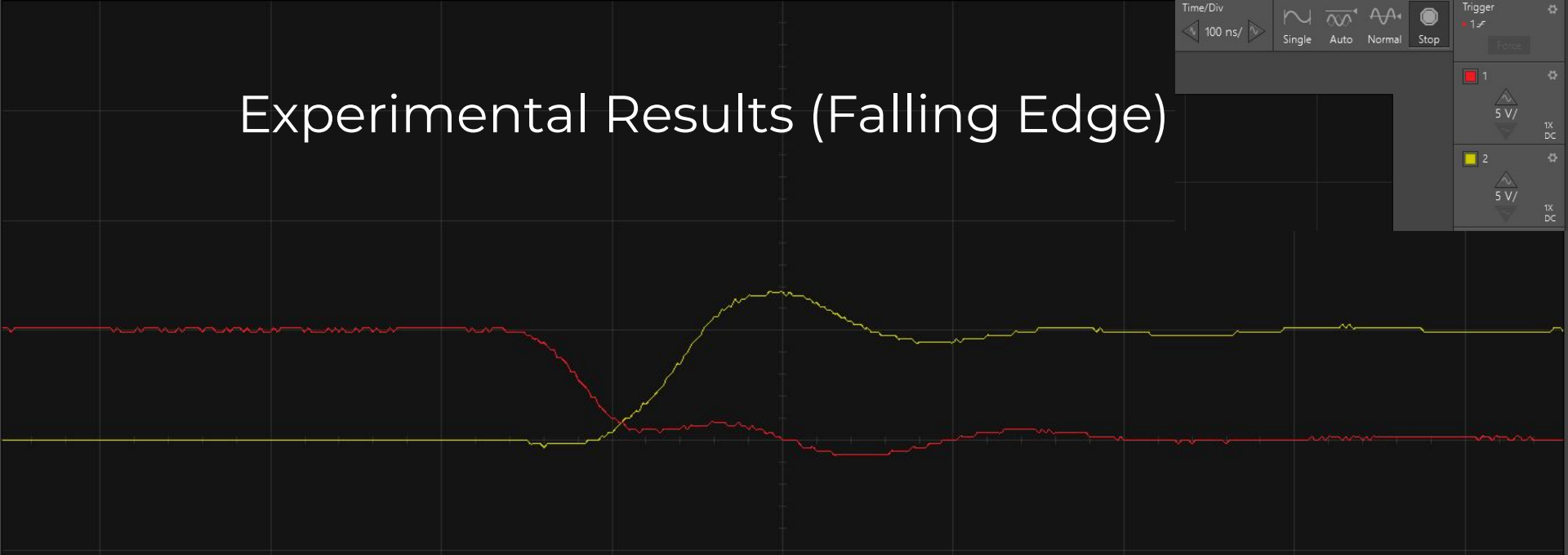
Simulation Results (Resistive pull up Falling edge 100k)



Breadboard Design

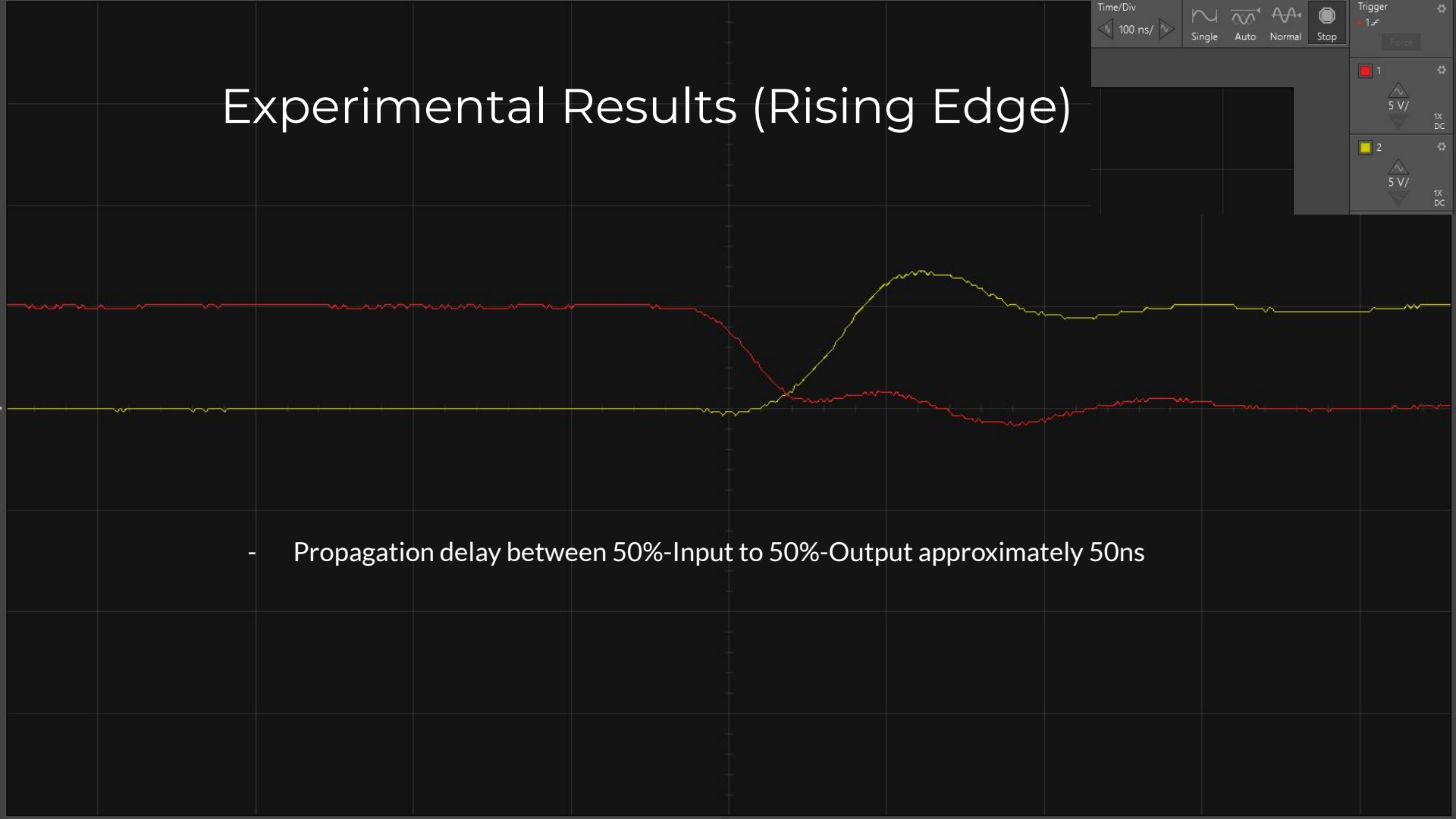


Experimental Results (Falling Edge)



- Propagation delay between 50%-Input to 50%-Output approximately 50ns

Experimental Results (Rising Edge)



- Propagation delay between 50%-Input to 50%-Output approximately 50ns