A Sub-threshold Variation-tolerant 16-channel FIR Filter Core for Hearing Aids

EECS 627

Group 6

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Overview

- Motivation
- Novelty & Value
- Specifications
- FIR Algorithm & Golden Brick Model
- Top Level Architecture
- Circuit Design & Analysis:
  - On-chip Switched-Capacitor DC-DC Converter
  - Sub-threshold 8T SRAM
  - Global Corner Detection
- Verification
- Floor Plan
- Results

Motivation

- Motivation:
  - Design of a low-power FIR filter core ASIC for Implantable hearing aids.

- Design Considerations:
  - Energy Constrained:
    - Battery-powered => Minimize Energy/FIR operation
  - Small Form-Factor:
    - Reduce package size, eliminate large off-chip components.
  - Global Process Variation tolerance:
    - Correlate critical-path delay with global process variation, reduce design-time margining.

- Key Metrics: Power, Reliability and Area while maintaining the required throughput.

Novelty and Value

- **Novelty**:
  - Custom dual-banked ultra-low leakage sub-threshold 8T SRAM.
  - On-Chip Switched Capacitor DC-DC Converter for Multi-VDD.
  - Global Corner detector and controller to set on-chip supply.

- **Improvements over Previous designs**:
  - Low power consumption permits integrated DC-DC converter
    - reduces packaging size, cost and complexity.
  - Banked SRAM improves memory BW, small area overhead.
  - Reduction in the energy consumed by the SRAM during Read and Write operations.
  - On chip corner detection circuit for calibrating supply voltage at Power-On.

Specifications

- Input Data: 16 kHz sampled 16-bit Discrete Time data from ADC *
- Output Data: 16 channel 16-bit filtered data to output DACs *
- Core Area: < $1mm^2$
- Core Frequency: 910 kHz
- Core Supply Voltages: 0.28 V , 0.33 V, 0.38 V
- Battery-Supply: 1.2 V
- Operating Temperature: 37^oC
- 2kb 8T SRAM operating at subthreshold
- Process: IBM® 0.13um 8-metal CMOS , ARM Artisan® Standard Cell Library

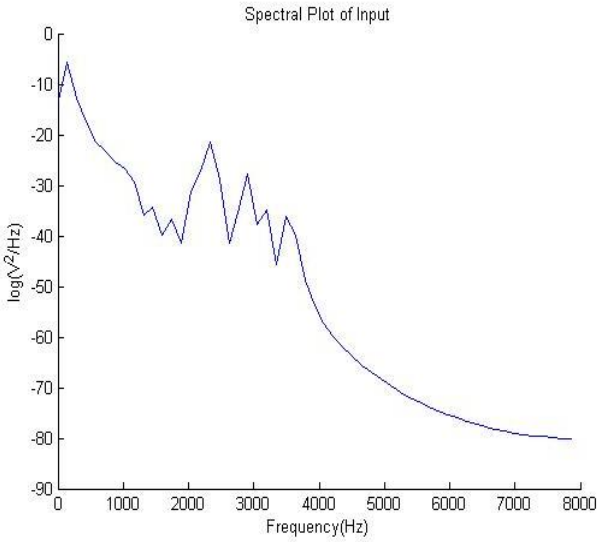
* ADC/DAC not implemented in this chip.

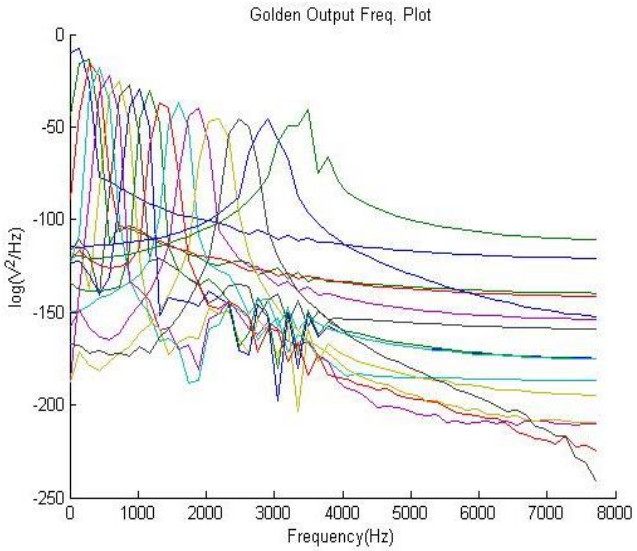
Algorithm and Model

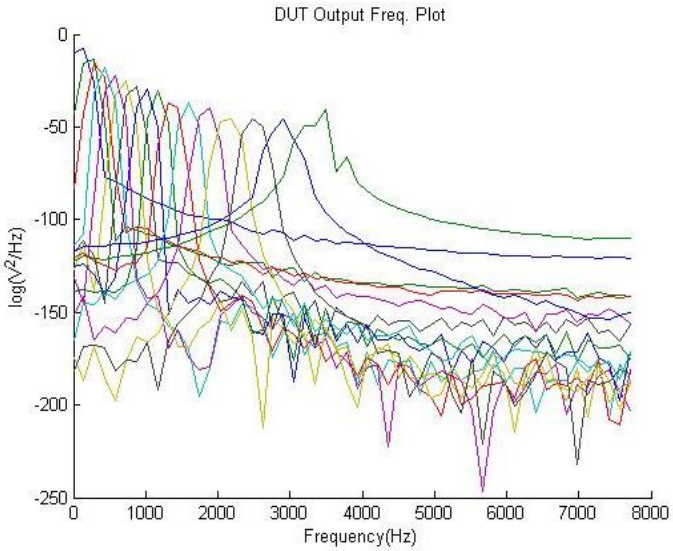
- FIR Operation: Convolves input data pairs with filter coefficient vector *h*

$$y[n] = \sum_{i=1}^{N/2} h[i] * \{x[n-i] + x[n-N-i]\}$$

- 16-Channel Band Pass FIR Filters across human speech frequency range.
- Golden Brick – 16-bit fixed-point model using MATLAB & Simulink FDA tool.



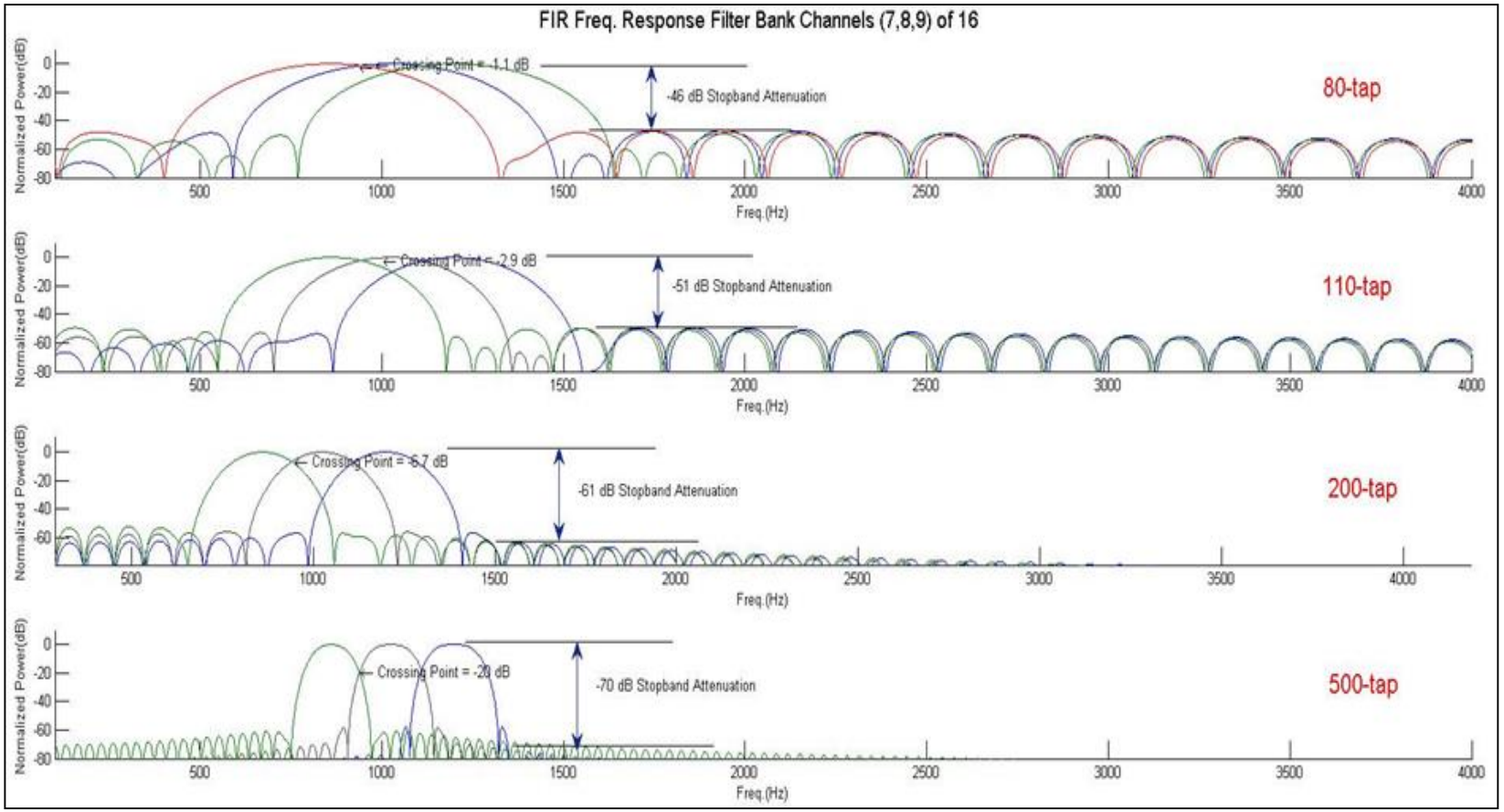




MATLAB Simulation of 16 channel FIR Filter & HDL Implementation with same input stimulus

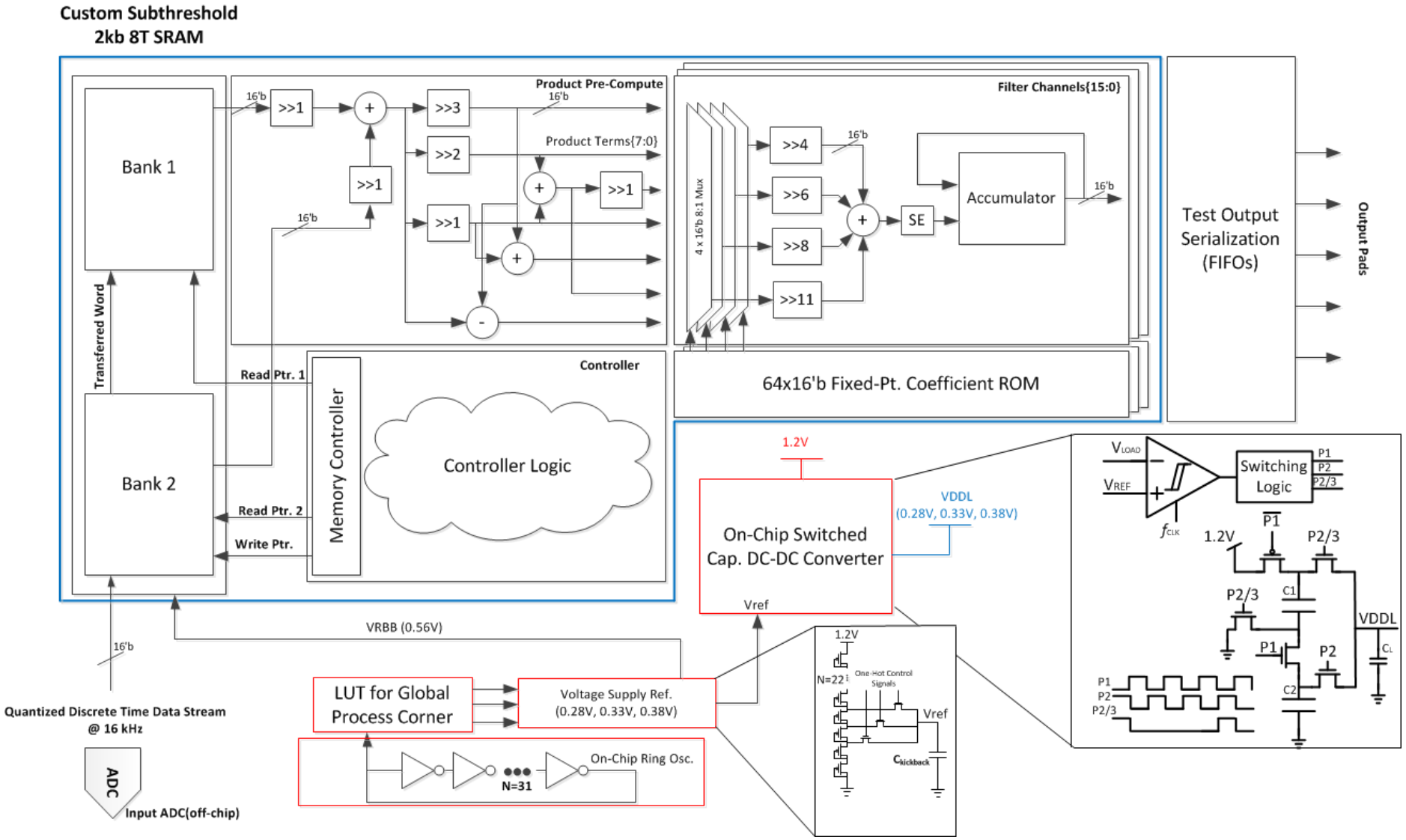
Algorithm and Model

- FIR Filter Response: >50 dB of Stop-band Attenuation and 3 dB crossover attenuation
- Filter Order < Max. Core Clock Frequency/16 kHz Sampling Frequency

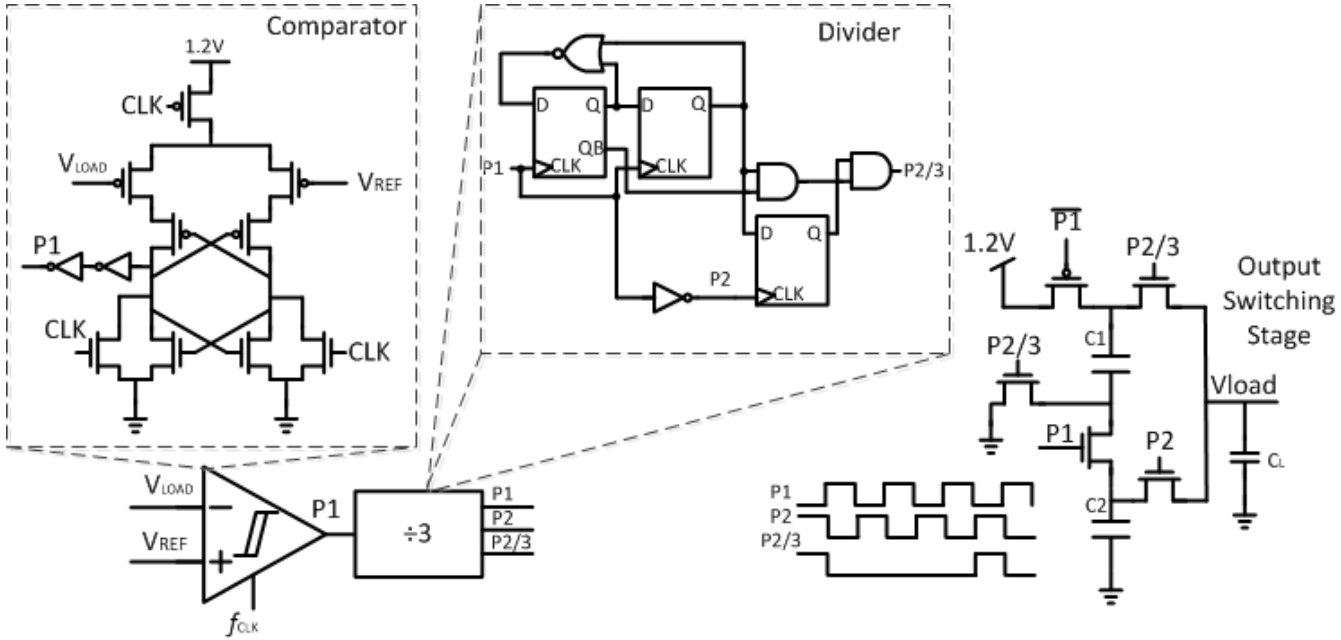


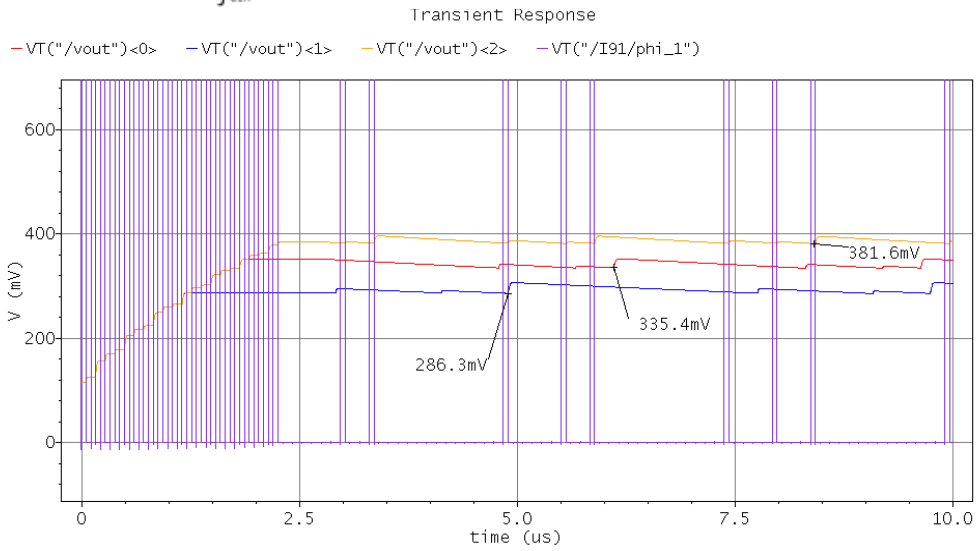
Filter response for various orders

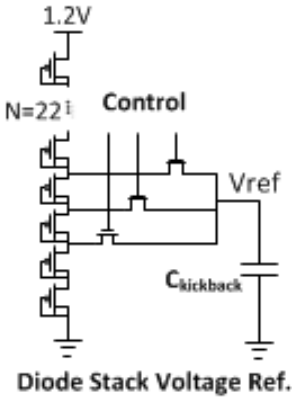
Top-level Architecture



On-Chip DC-DC Converter

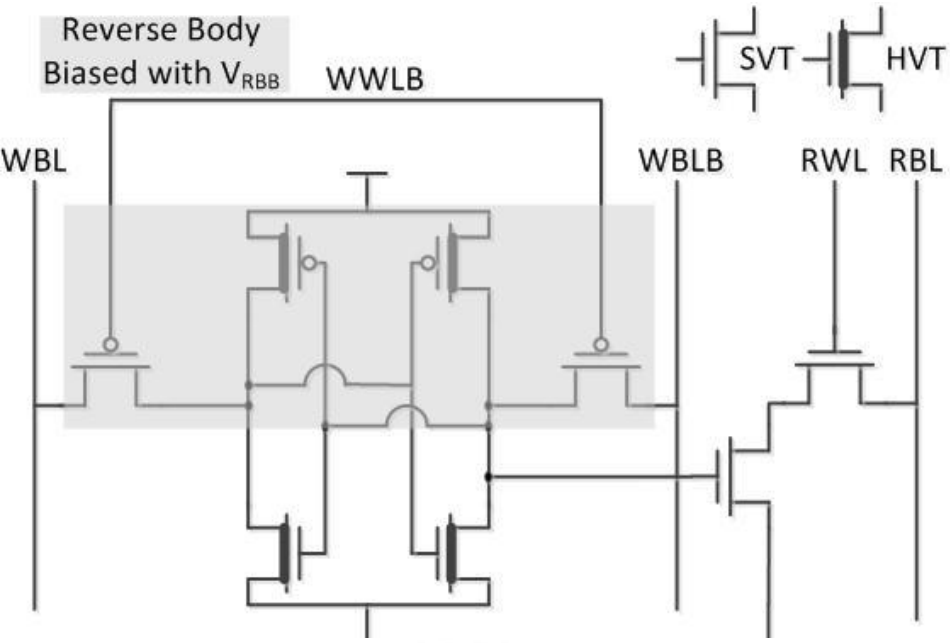


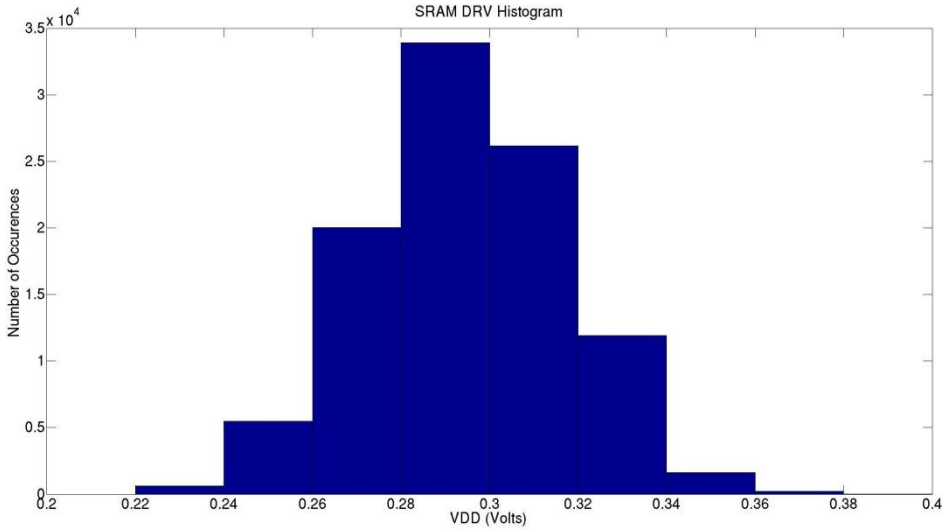




- Regulates V_{LOAD}
- Sources of Loss:
  - Charge-transfer switching loss
  - Bottom-plate sampling loss
  - MOS capacitor leakage
- $C_{kickback}$ reduces supply kickback noise
- Recharge pulses only when falls V_{LOAD} below V_{REF}
- Switching Efficiency: 46%(0.28V) – 55%(0.38V)

SRAM



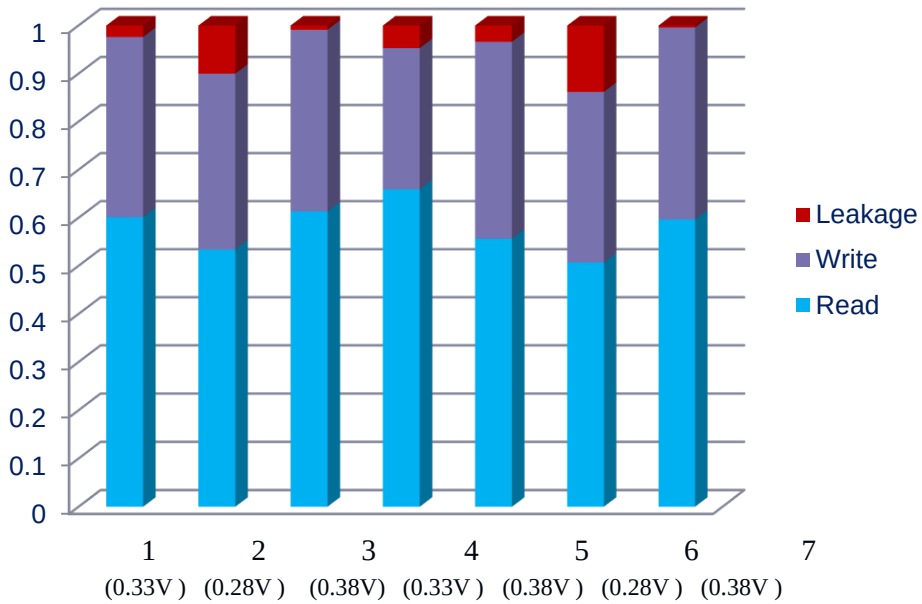


- ***Cross Coupled Invertors**** – HVT Transistors for low leakage.
- ***SVT PMOS Access Transistor*** – larger ON current.
- ***2T Read Buffer*** – SVT transistors for fast read.
- ***Reverse Body Bias**** – low leakage.
- *Address Decoder* – Dynamic logic.

Height	1.54 µm
Width	4.26 µm
Area	6.5604 µm^2
Leakage (1 Bit-Cell)	0.93 pW
Avg. Energy/bit (Read)	15.996 fJ
Avg. Energy/bit (Write)	9.978 fJ
Aspect Ratio	2.766

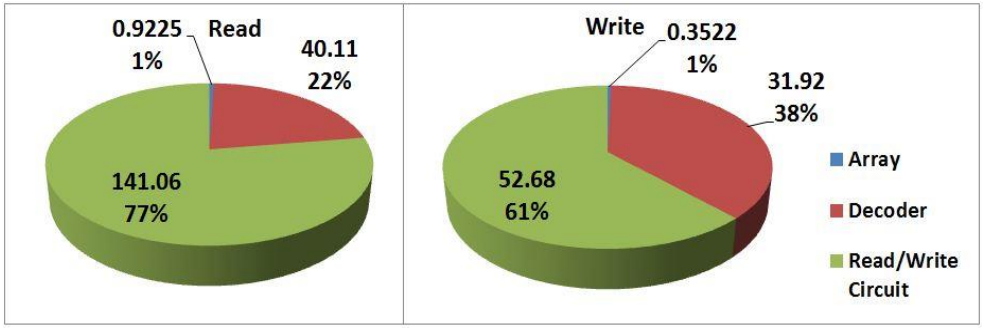
**Daeyeon Kim et al. "A 1.85fW/bit Ultra Low Leakage 10T SRAM with Speed Compensation Scheme," Circuits and Systems (ISCAS), 15-18 May 2011.*

Analysis: SRAM

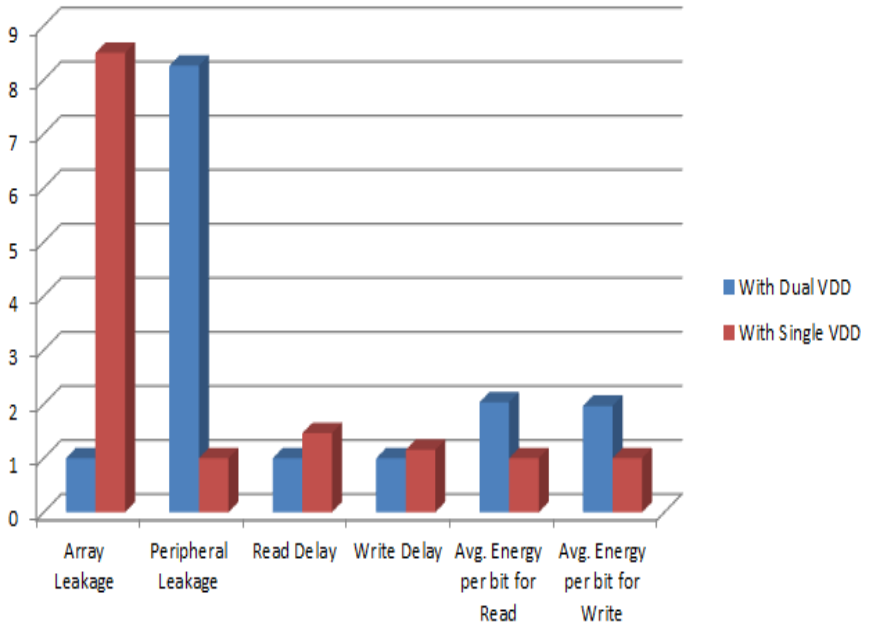


Normalized energy consumption (per bit) at various corners with corresponding V_{DD}

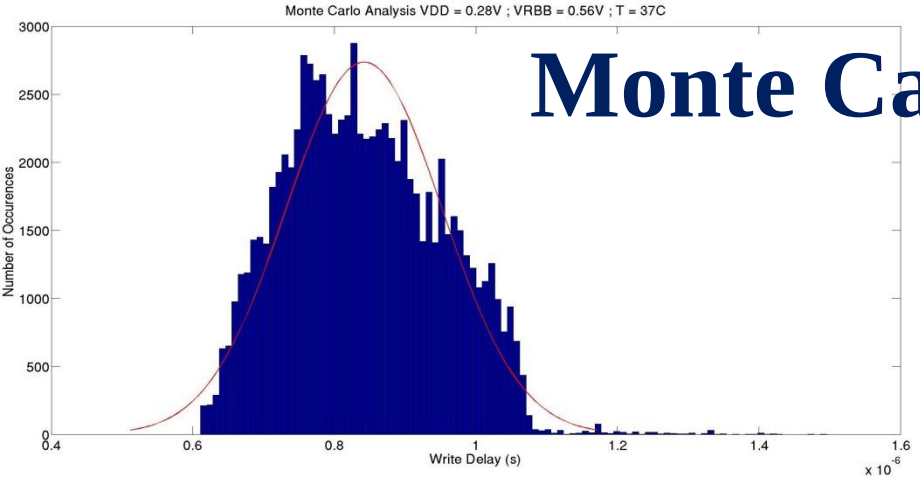
Array Size	56 words x 16 bits
SRAM Height	131.54 µm
SRAM Width	116.55 µm
Array Efficiency	~74%
V_{DD}	0.28V/0.33V/0.38V
V_{RBB}	0.56V
Access Scheme	1R/1W

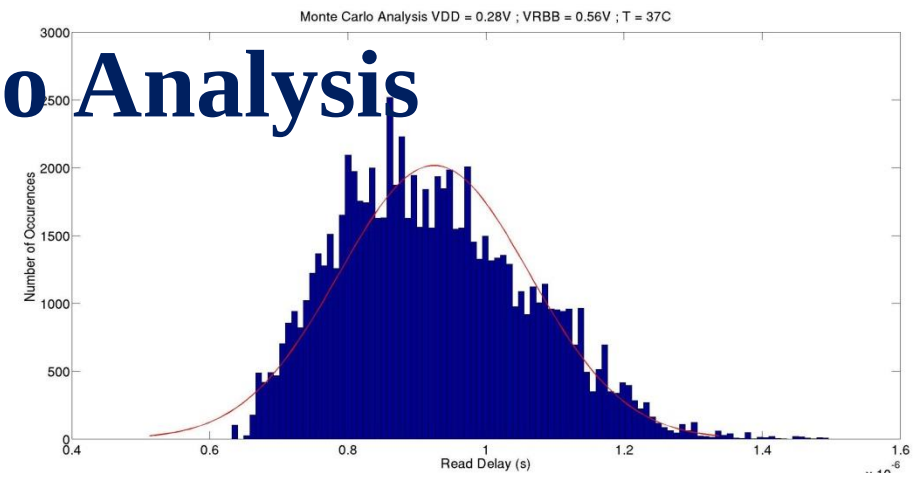


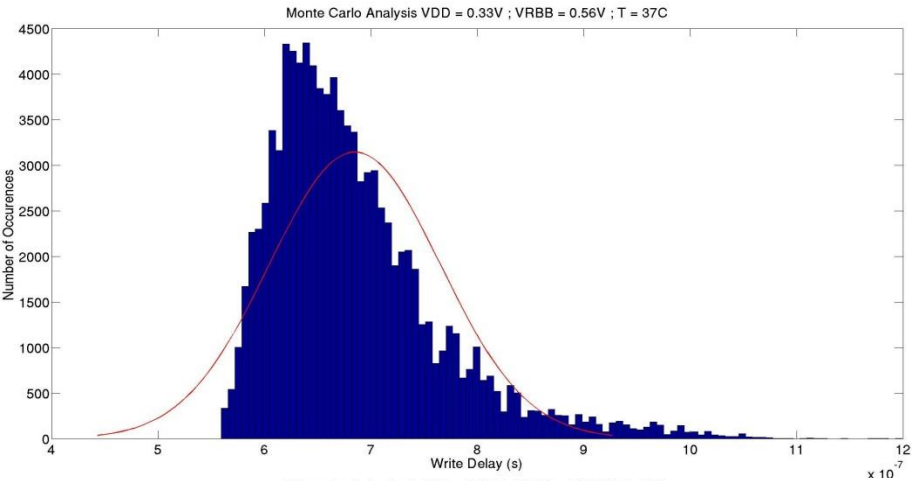
Energy consumed by various SRAM components (Entire Array) in fJ

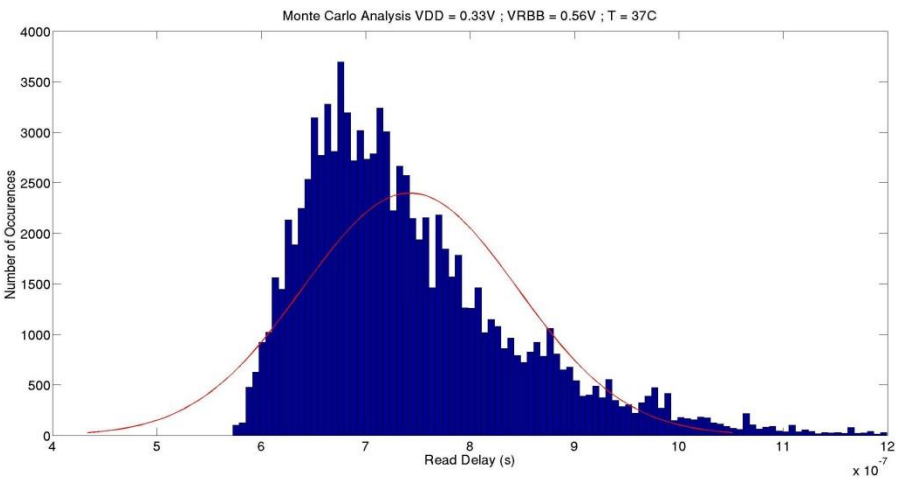


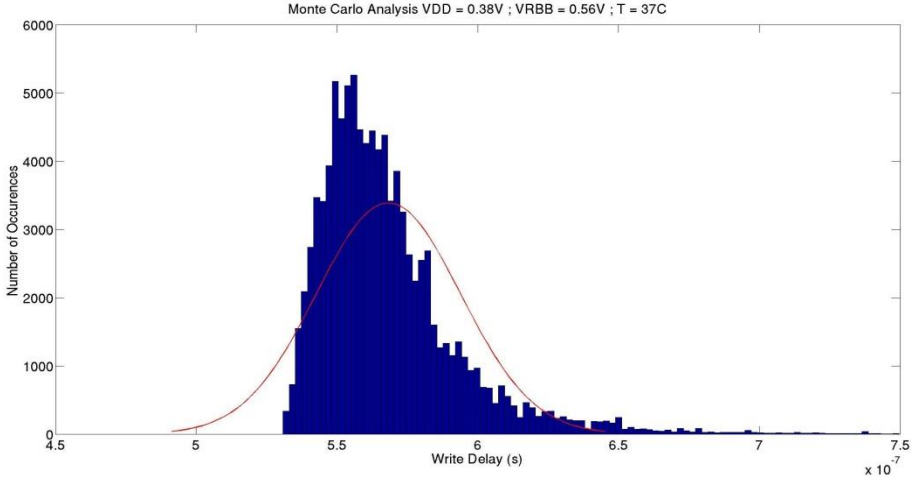
Monte Carlo Analysis

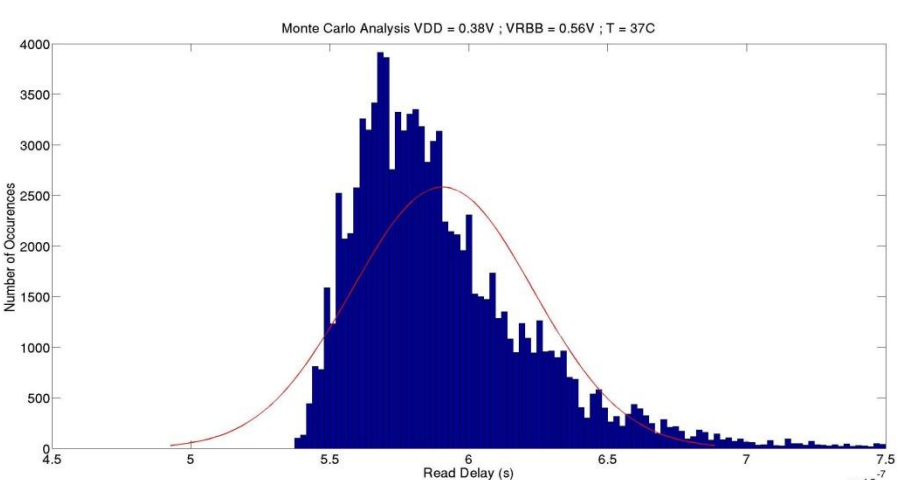




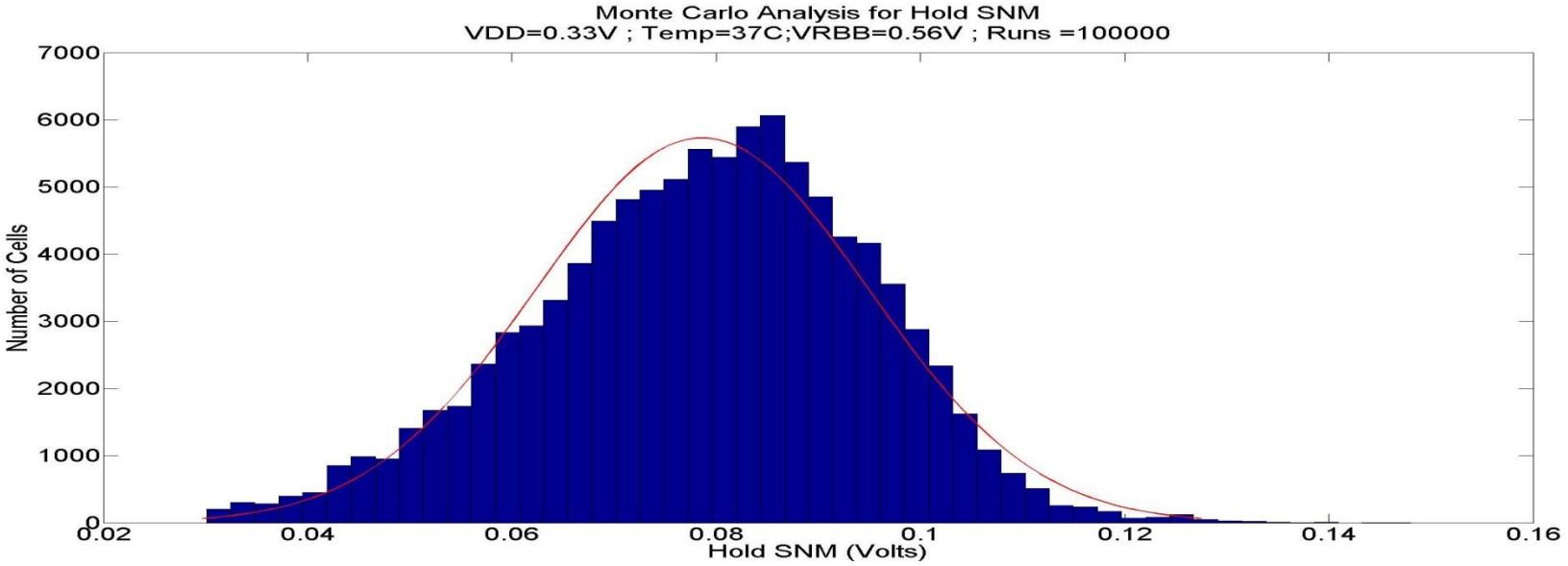


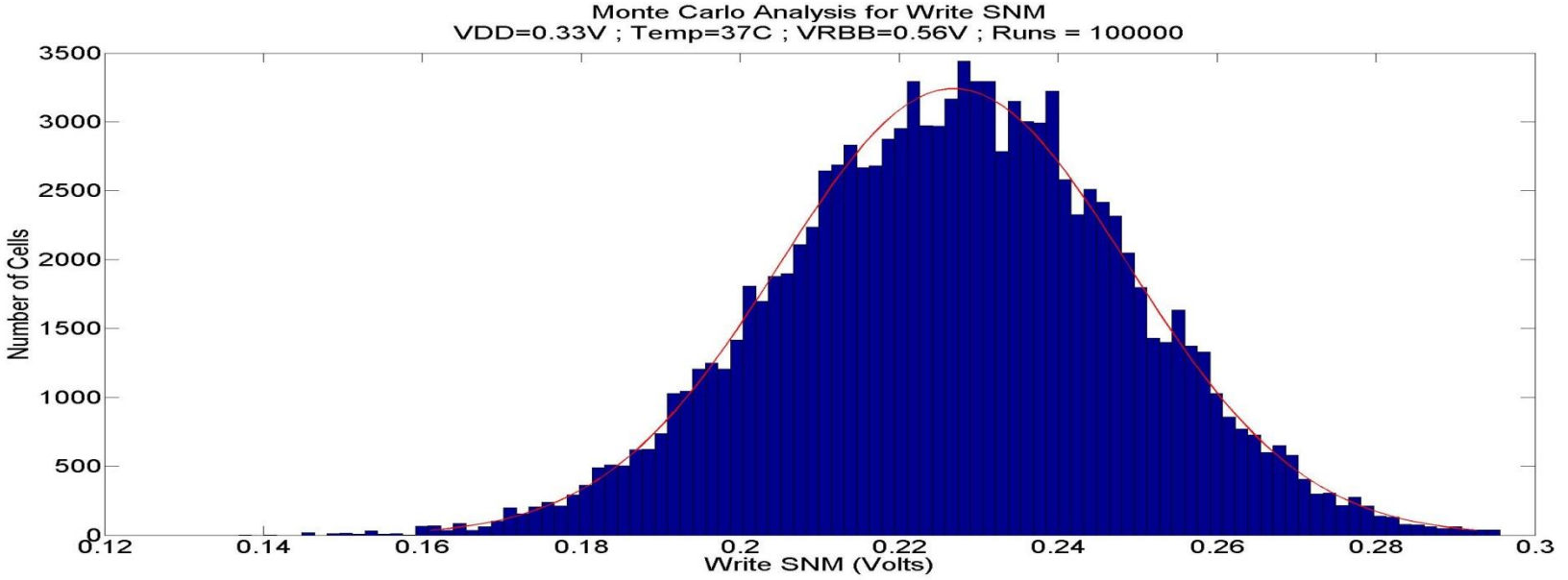




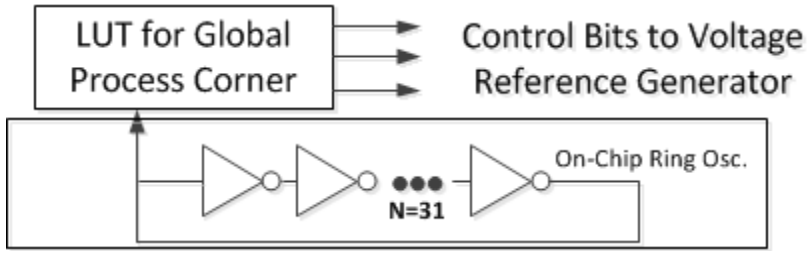


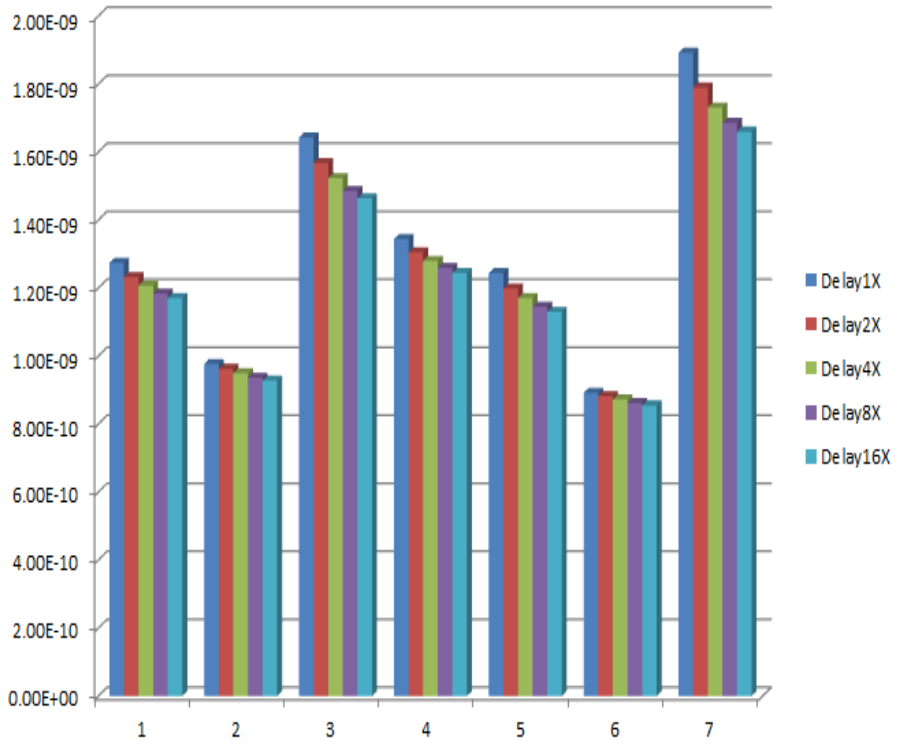
Monte Carlo Analysis





Corner Detection



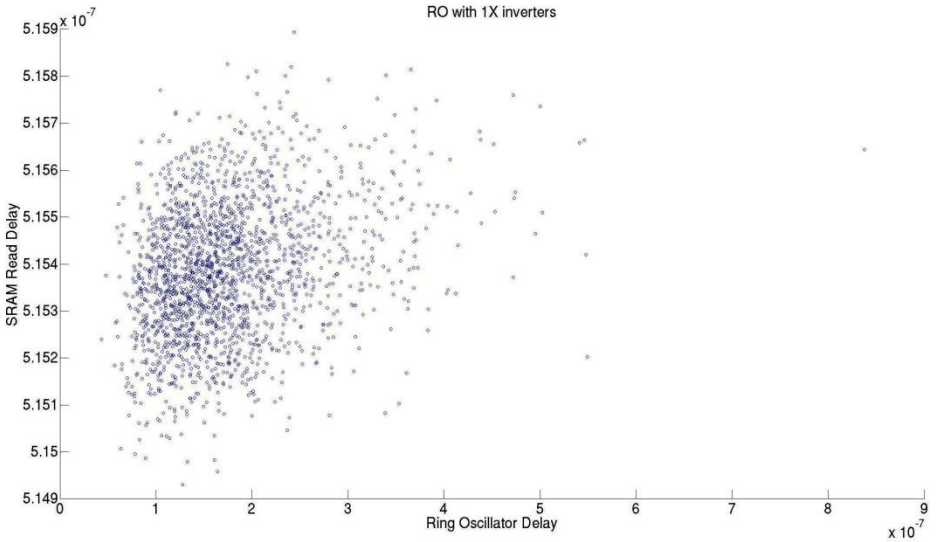


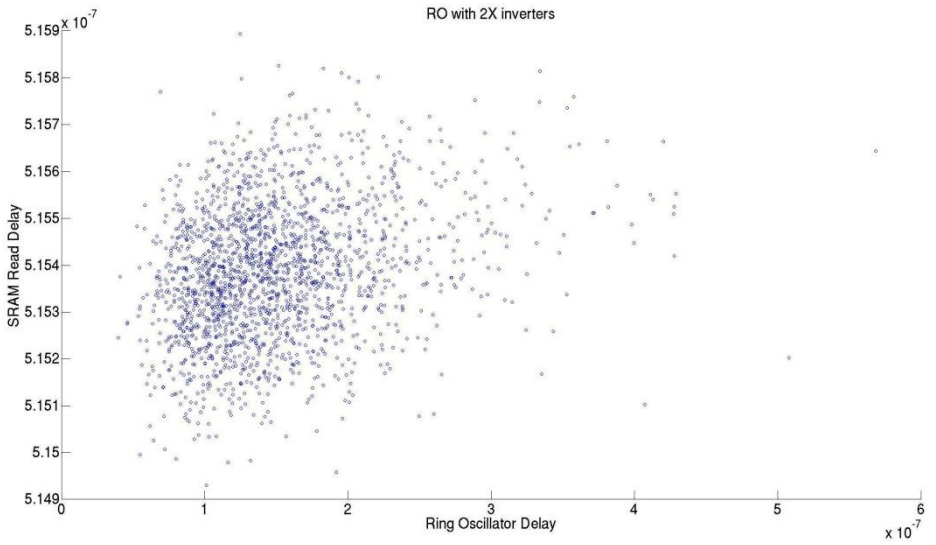
Delay variation across Global Corners

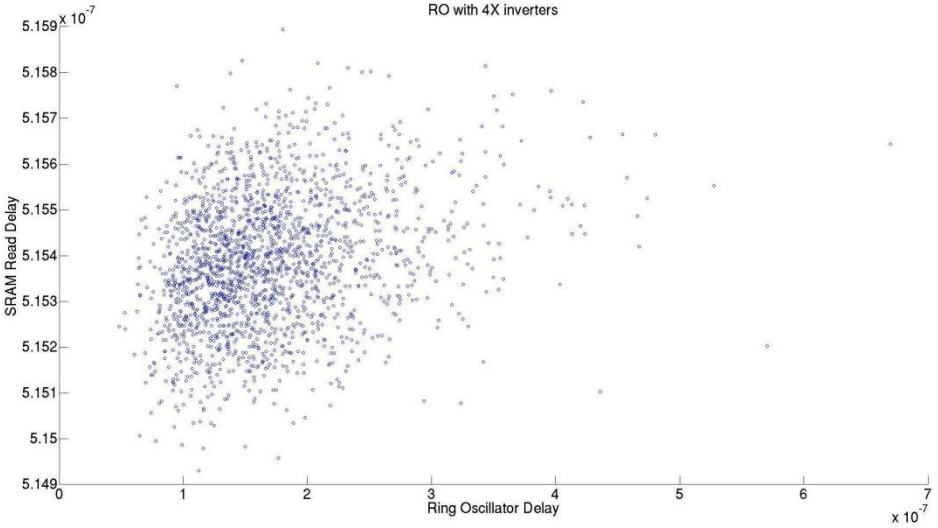
- Target inter-die variations -
  - Fixed workload.
  - Temperature invariant (~37^{o}C)
  - Primary sources of variation can be:
    - device ageing
    - Ldi/dt
    - IR.

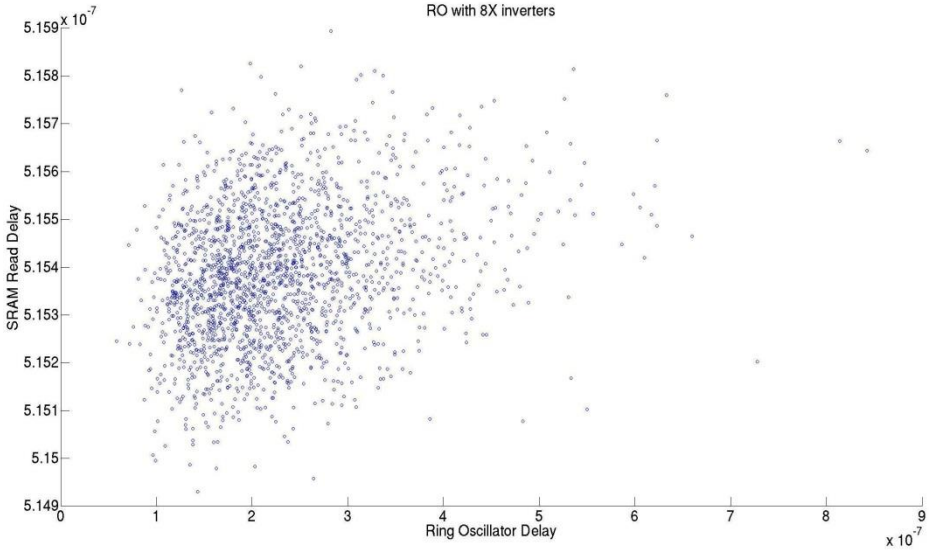
- ***Ring Oscillator*** **– 31 Stages , 4x Sized.**
- ***Controller*** **- 10 Bit Counter with a reset.**
- ***Power Domain*** **– Powered by 1.2 V supply.**
- ***Reset*** **- keep this signal high for 2 clock cycles until the controller does the calibration and sends the control signal to the DC-DC converter.**
- ***Testing Time*** **- Requires only 2 clock cycles to calibrate the chip (one clock cycle to detect the corner, one clock to set the reference).**

Global Variation Correlation: RO vs Critical Path





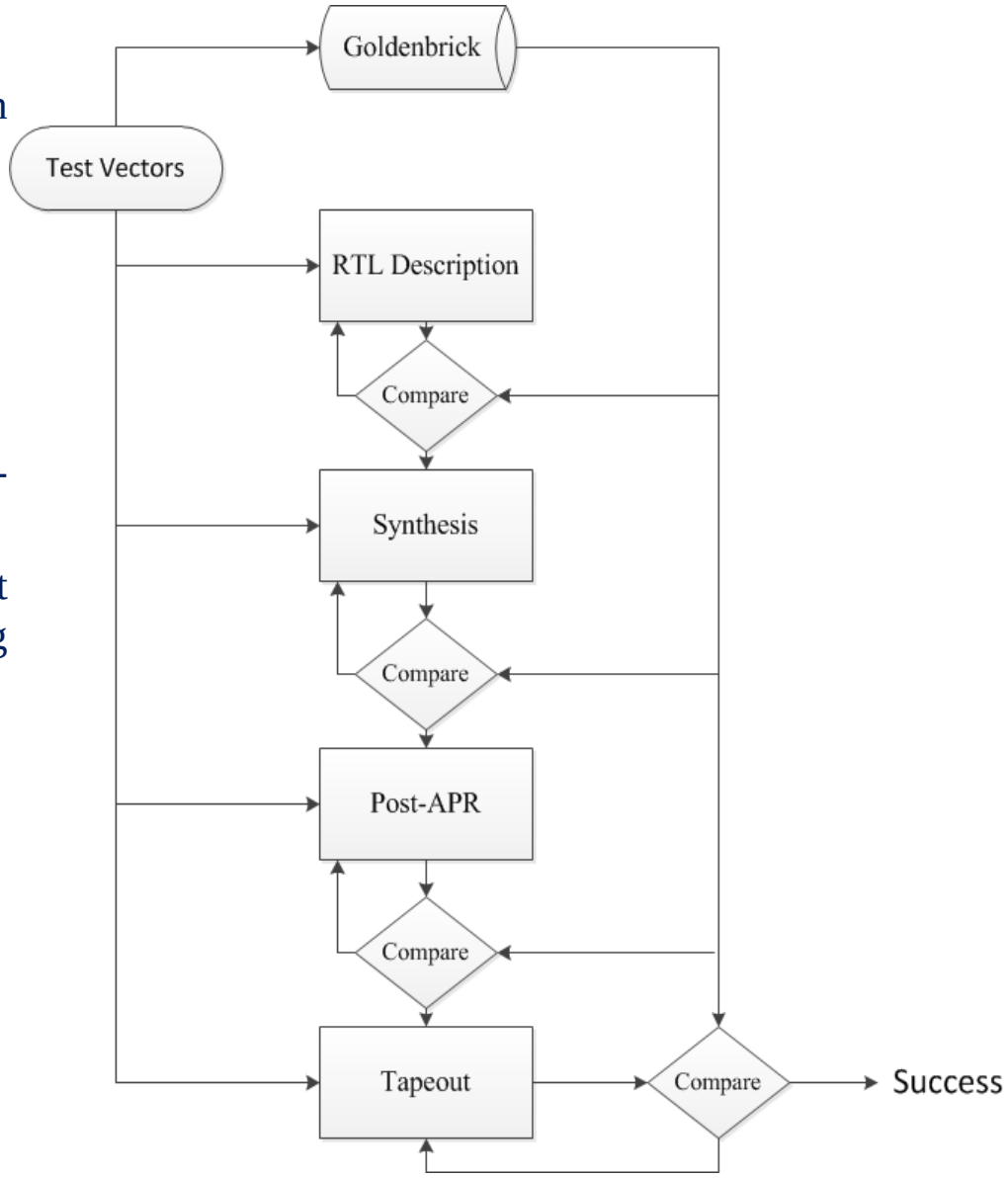




Verification

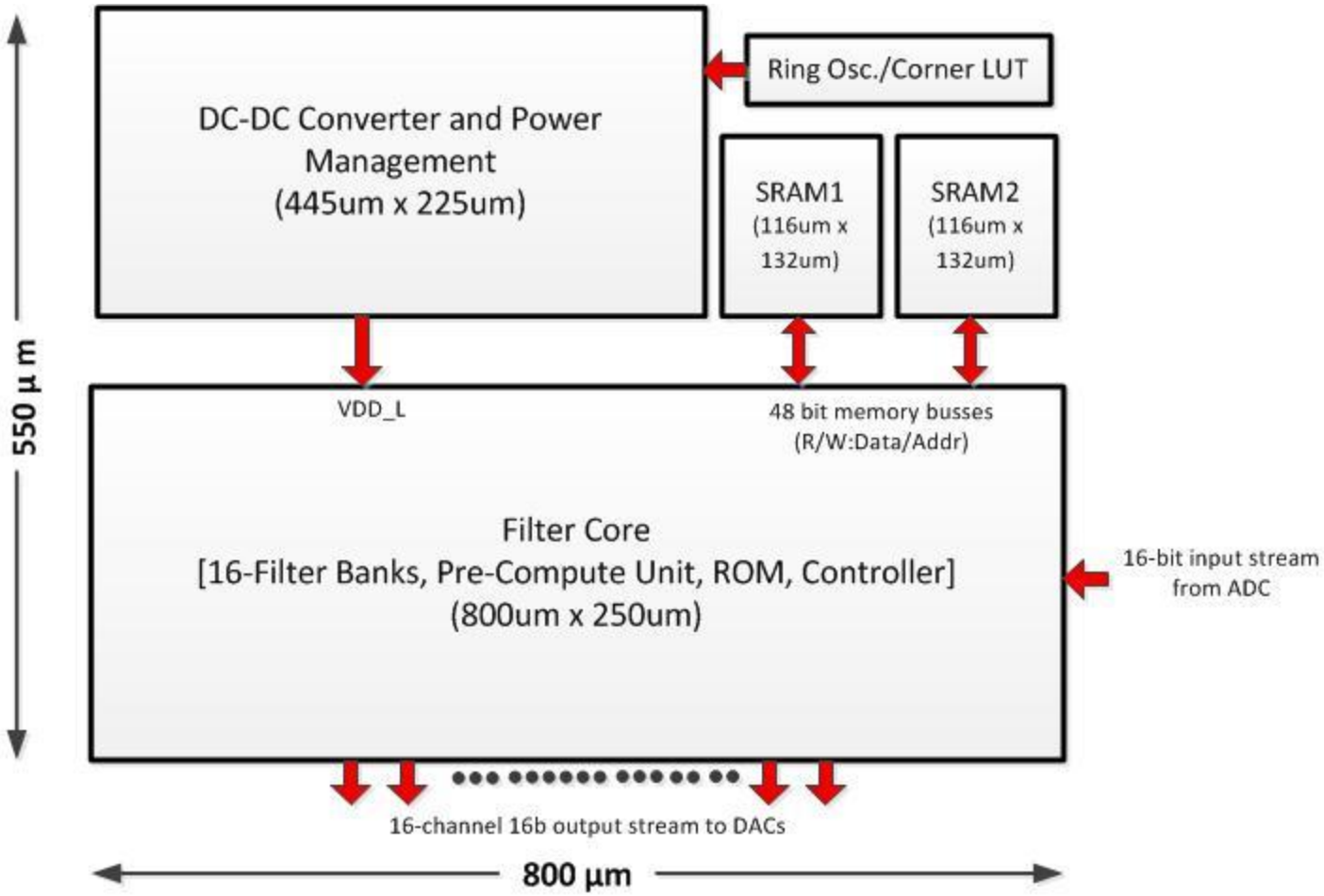
- Data representation –
  - Input/Output/Coefficients of FIR are in fixed-point decimal representation.
  - Input/Coefficients – 16bits (Q15).
  - Output – 16bits (Q15).

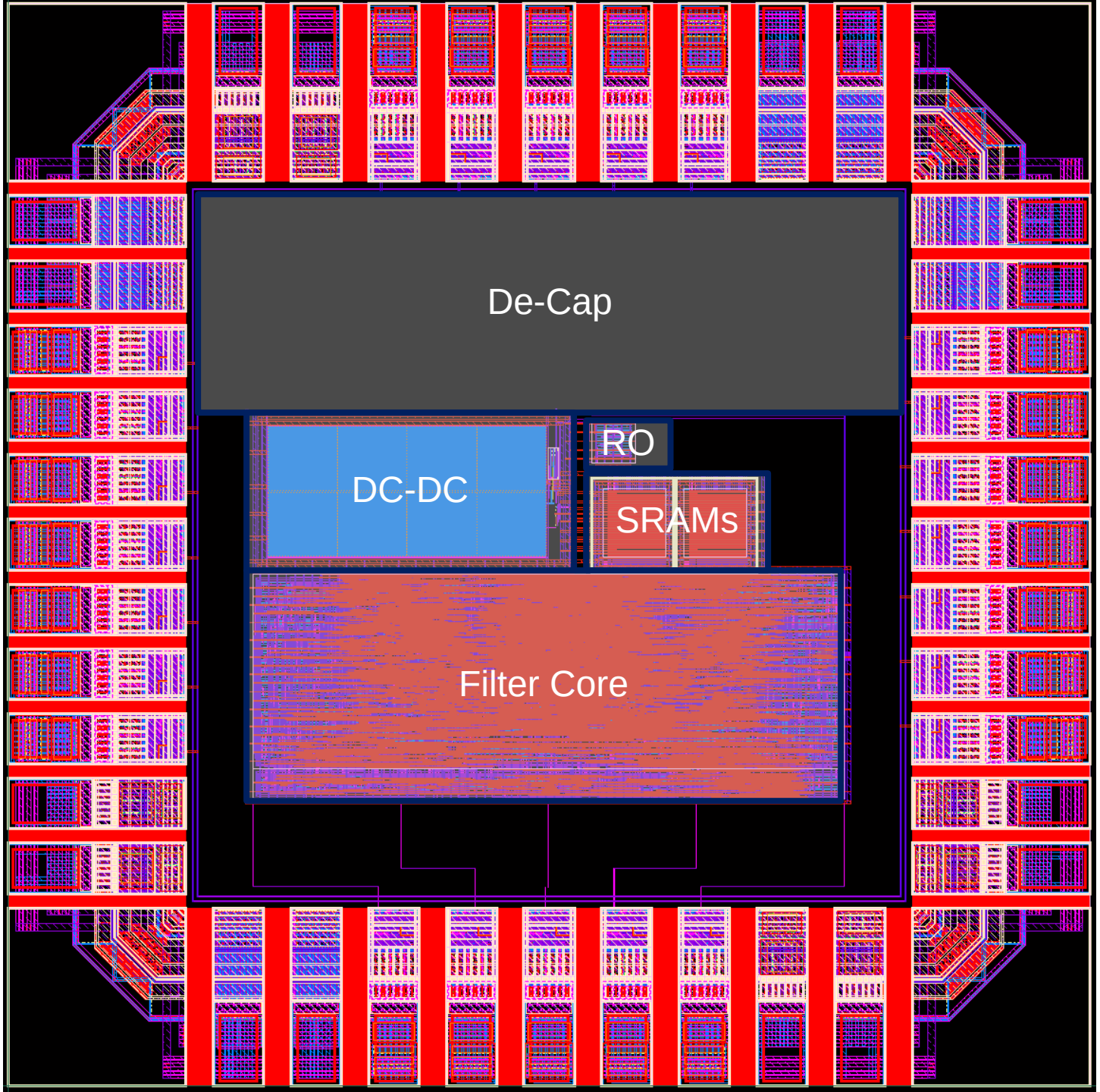
- Test of functionality
  - Input test vectors generated from real-time signals using MATLAB.
  - Compare the Behavioral Model output with the MATLAB Golden brick fixing an allowable error rate.



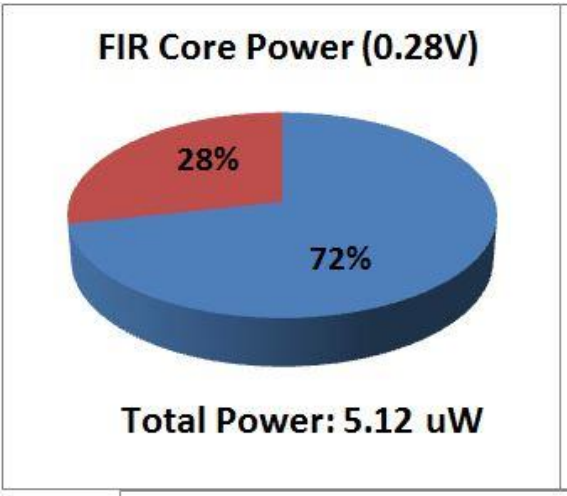
Floor plan/Layout

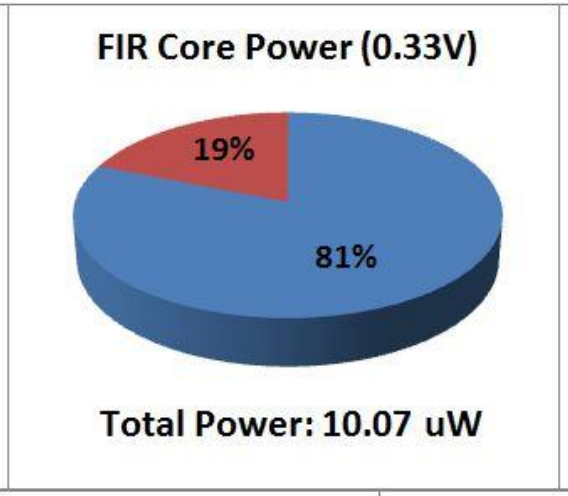
- Core Area – 0.45 mm^2

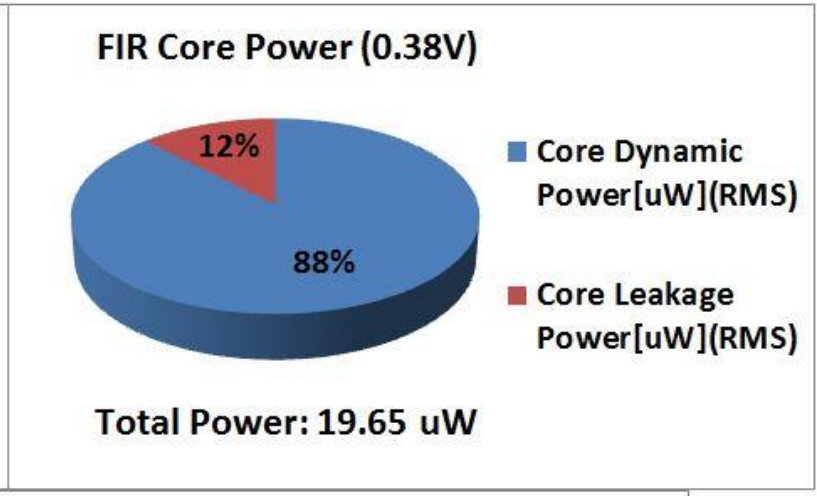


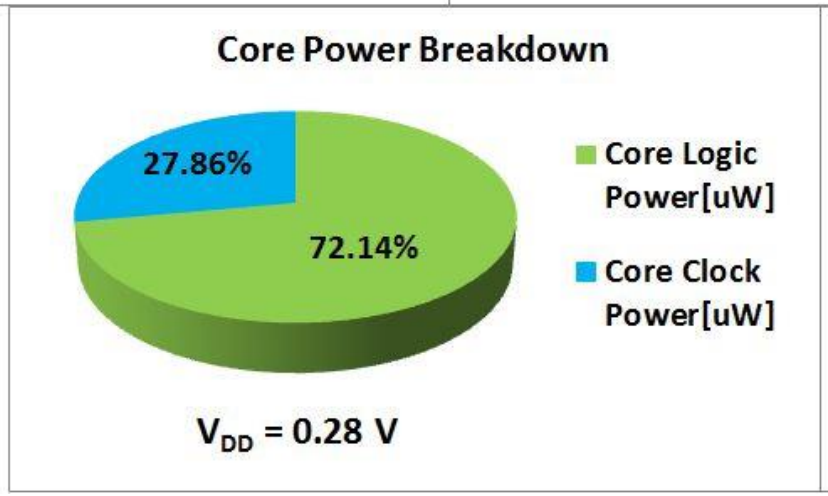

De-Cap
DC-DC
RO
SRAMs
Filter Core

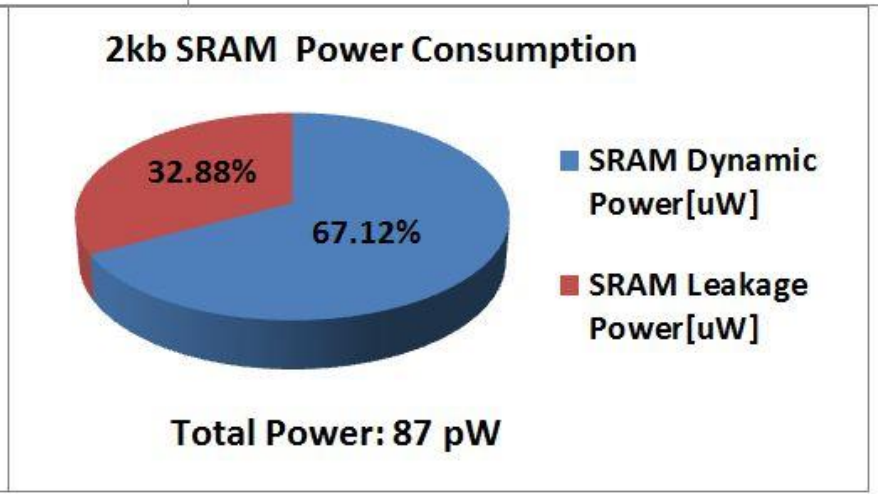
Results : Power



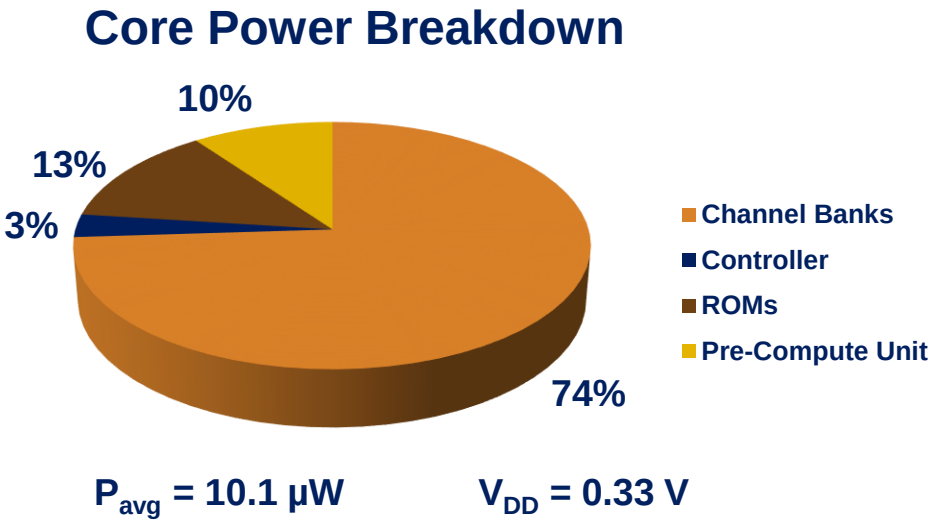


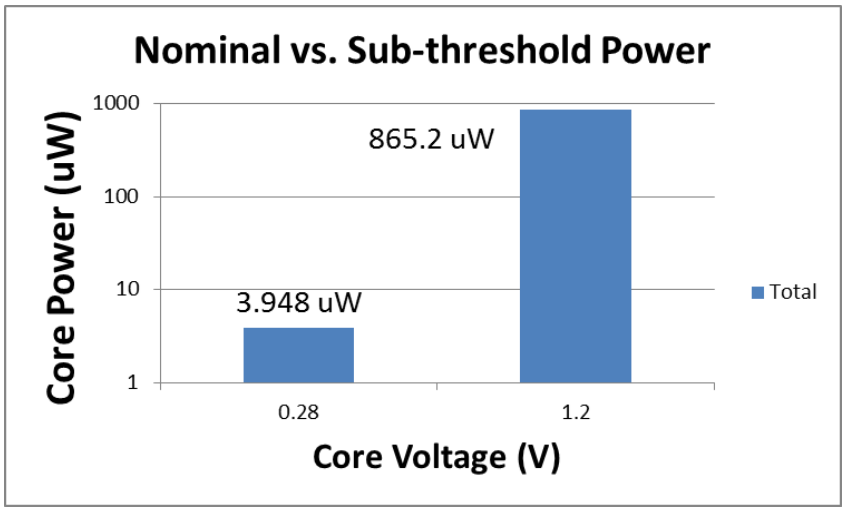






Results: Power





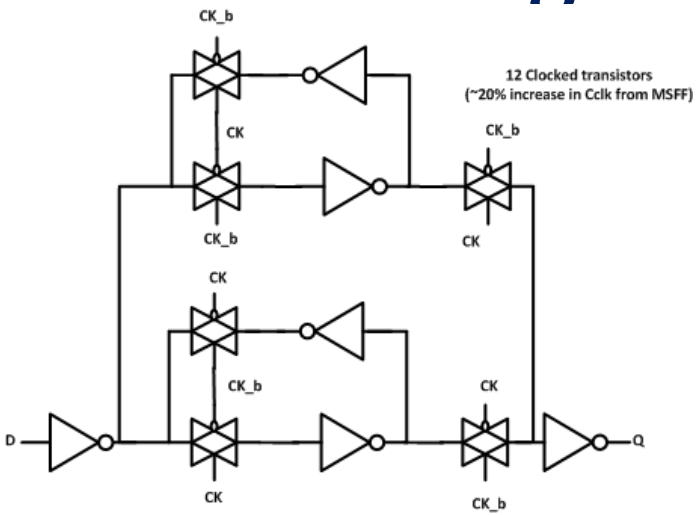
Comparison to Previous Subthreshold FIR Cores

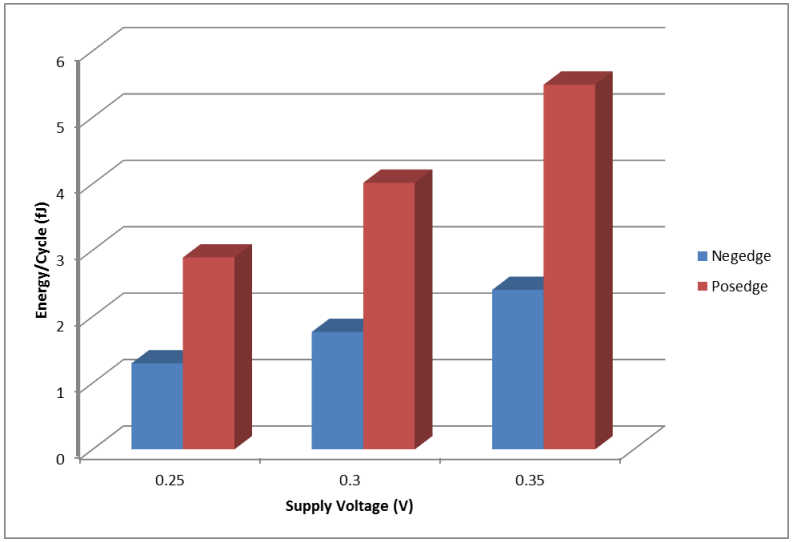
Design	Supply Voltage (V_{DD})	Process Node	Filter Order/ Word Length	Avg. Power	Core Freq. (f_{clk})	Energy/FIR operation
Chong et. al	0.3 V	65 nm	109th/16b	10.4 µW	960 kHz	0.6 nJ
Myeong-Eun Hwang et. al	85 mV – 1.2 V	130 nm	8th/8b	40 nW	240 Hz	1.33 nJ
Proposed Design	**0.28 V – 0.38 V**	**130 nm**	**109th/16b**	**5.1 µW – 19.7 µW**	**910 kHz**	**0.31 nJ – 1.19 nJ**

Thank You!

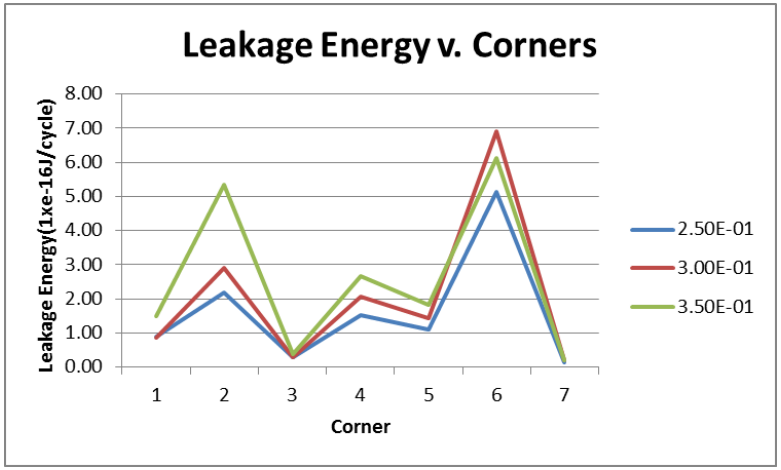
Backup

Dual Edge Triggered Flip-Flop





- Fixed-throughput means no clock-gating and relatively high activity factor.
- DETFF can reduce clock power up to ~30%.
- Implementation Plan: Integrate within filter bank module to compare relative improvement.
- Initially thought of using this but since Clock power was < 30% of total power and we would end up saving lesser than what we would spend in bringing this up!

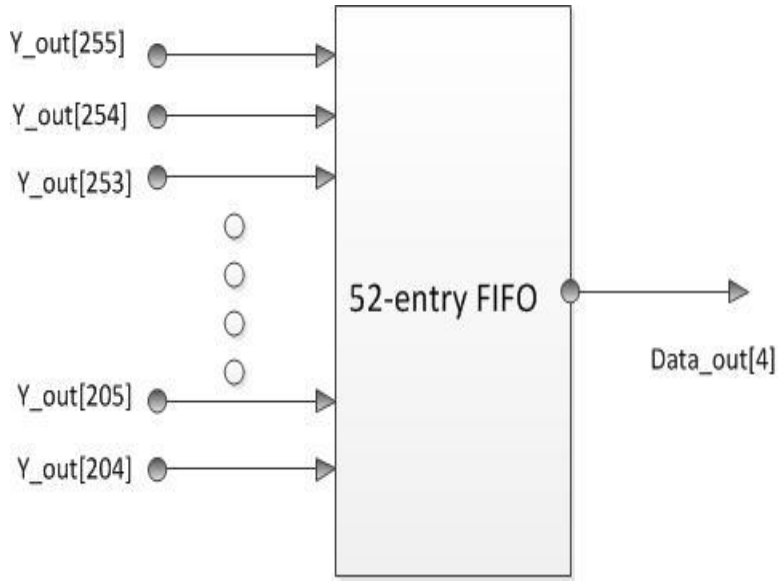


Output FIFO

Problem :

256 output data signals of top module : y_out[255:0] – Need too much pads !

Solution : use output FIFOs, 5 output FIFOs : need only 5 pads !



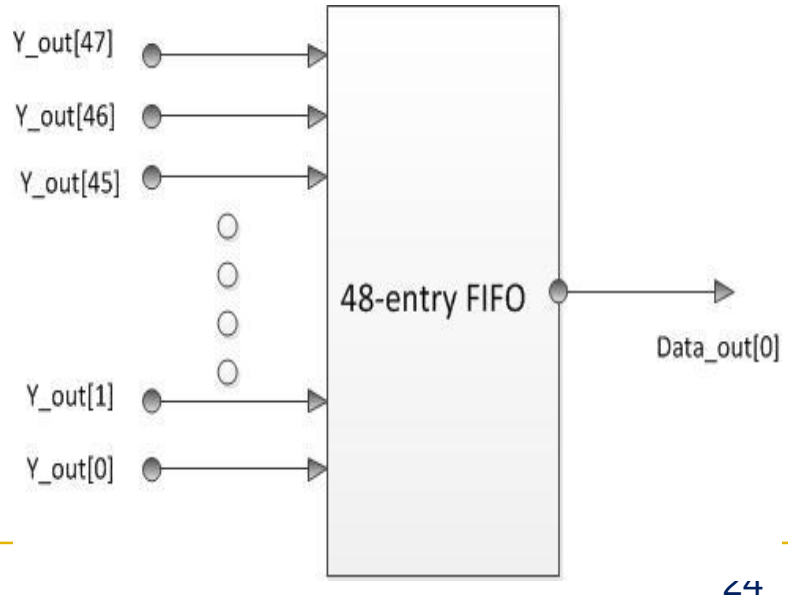
Output data signals change every 56 clock cycles

fifo style I : 4 52 entries FIFOs

fifo style II : 1 48 entries FIFO

Write to the fifo at a time, read the data to pad every clock cycle

- **length : 820 µm**
- **width : 42 µm**
- **area : 34,440 µm^2**



Future Work

- Future Work:
  - Implement ADC/DACs on-chip to integrate system.
  - Integrate low-power on-chip PLL for local clock generation.

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