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MT8735 LTE Tablet Application Processor

Technical Brief

Version: 1.4
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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
0.1	2014-09-01	MingTe Lin	Initial draft
0.2	2014-.9-30	MingTe Lin	Updated package type.
0.9	2014-10-27	MingTe Lin	Updated DRAM freq to 640MHz.
1.0	2014-12-18	Polo Tseng	Update ordering information
1.1	2015-01-07	MingTe Lin	Updated Table 2-1,2-8 and 2-9.
1.2	2015-03-18	MingTe Lin	Modified eMMC spec from 5.1 to 5.0.
1.3	2015-08-03	CS Chao	Updated Table 2-21. AUXADC specifications.
1.4	2015-10-29	MingTe Lin	Fixed some typo, removed features optical zoom and Galileo

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Preface

Acronyms for register types

R/W	For both read and write access
RO	Read only
RC	Read only. After the register bank is read, every bit that is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be set to 1. Data bits that are LOW(0) have no effects on the corresponding bit.
W1C	Write only. When data bits are written to the register bank, every bit that is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits that are LOW(0) have no effects on the corresponding bit.

1 System Overview

The MT8735 device (see Figure 1-1), with integrated Bluetooth, FM, WLAN and GPS modules, is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable LTE smart device applications,. The chip integrates Quad-core ARM® Cortex-A53 operating up to 1.3GHz, an ARM® Cortex-R4 MCU and powerful multi-standard video codec. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays and MMC/SD cards.

The application processor, an Quad-core ARM® Cortex-A53 MPCore™ equipped with NEON engine offers processing power necessary to support the latest OpenOS along with its demanding applications such as web browsing, email, GPS navigation and games.
All are viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration.

The multi-standard video accelerator and an advanced audio subsystem are also integrated to provide advanced multimedia applications and services such as streaming audio and video, a multitude of decoders and encoders.

An ARM® Cortex-R4, DSP, and 2G and 3G coprocessors combined provide a powerful modem subsystem capable of supporting LTE Cat 4, Category 24 HSDPA downlink and Category 7 HSUPA uplink data rates, Category 14 TD-HSDPA downlink and Category 6 TD-HSUPA uplink, as well as Class 12 GPRS, EDGE. Supports cdma2000 HRPD/1xEV-DO Revision 0 and A (3.1Mbps for forward link and 1.8Mbps for reverse link).

MT8735 also embodies wireless communication device, including WLAN, Bluetooth and GPS. With four advanced radio technologies integrated into one single chip, MT8735 provides the best and most convenient connectivity solution in the industry.

The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces the PCB layout resource.

1.1 Highlighted Features Integrated in MT8735

- Quad-core ARM® Cortex-A53 MPCore™ operating at 1.3GHz
- LPDDR3 up to 3GB, 640MHz
- LTE Cat 4 (150Mbps)
- CDMA200 HEPD/ 1xEV-DO Revision 0 and A.
- Embedded connectivity system including WLAN/BT/FM/GPS
- Resolution up to WXGA (1,280*800) OpenGL ES 3.0 3D graphic accelerator
- ISP supports 13MP@30fps.
- H.264 1080p @ 30fps encoder
- Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)

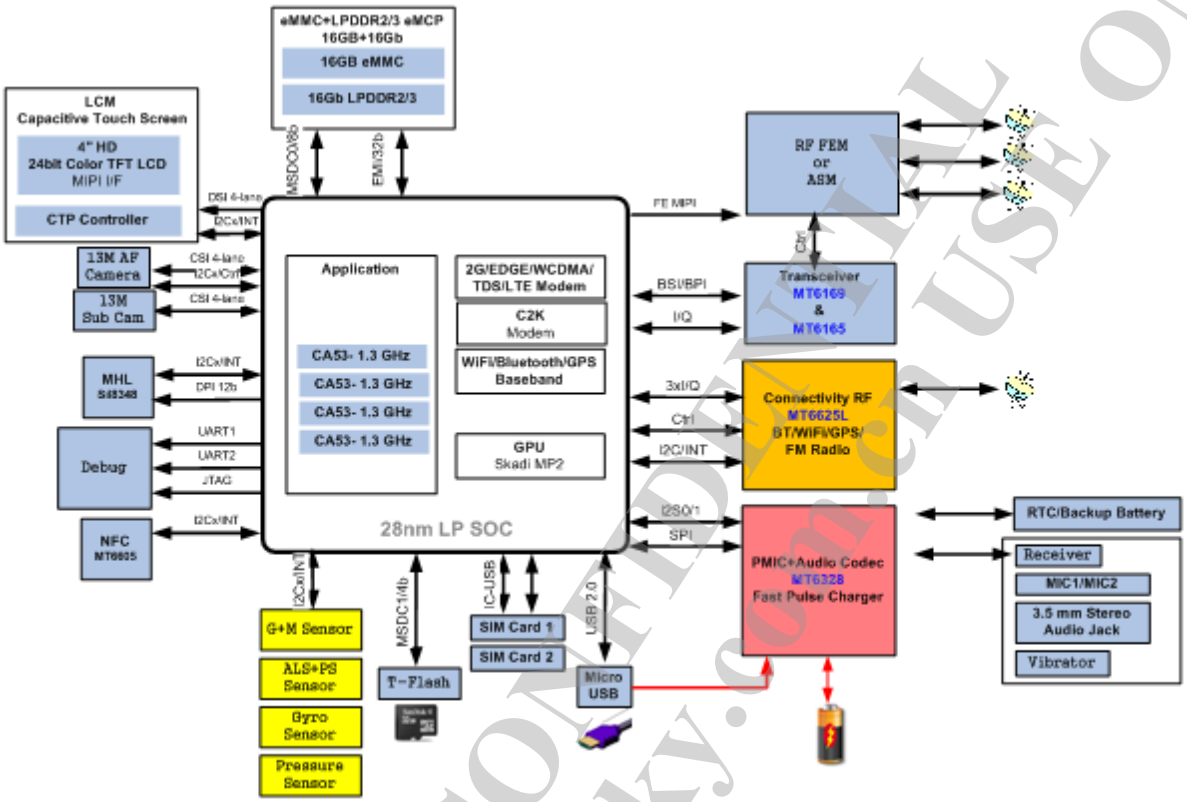


Figure 1-1. High-level MT8735 functional block diagram

1.2 Platform Features

- **General**
  - Tablet, two MCU subsystems architecture
  - eMMC boot support
  - Supports LPDDR-2/LPDDR-3

- **AP MCU subsystem**
  - Quad-core ARM® 1.3Ghz Cortex-A53 MPCoreTM
  - NEON multimedia processing engine with SIMDv2/VFPv4 ISA support
  - 32KB L1 I-cache and 32KB L1 D-cache
  - 512KB unified L2 cache
  - DVFS technology with adaptive operating voltage from 0.85V to 1.25V

- **MD MCU subsystem**
  - ARM® Cortex-R4 processor with max. 600MHz operation frequency
  - 64KB I-cache, 64KB D-cache
  - 512KB TCM (tightly-coupled memory)
  - Coresonic DSP for running LTE modem tasks, with max. 300MHz operation frequency
  - FD216 DSP for running modem/voice tasks, with max. 250MHz operation frequency
  - High-performance AXI and AHB bus
  - General DMA engine and dedicated DMA channels for peripheral data transfer
  - Watchdog timer for system error recovery
  - Power management for clock gating control
- **MD external interfaces**
  - Dual SIM/USIM interface
  - Interface pins with RF and radio-related peripherals (antenna tuner, PA, etc.)

- **Security**
  - ARM® TrustZone® Security
  - Hardware Crypto Engine support

- **External memory interface**
  - LPDDR2/3 up to 3GB
  - Single channel with 32-bit data bus width
  - Memory clock up to 640MHz
  - Self-refresh/partial self-refresh mode
  - Low-power operation
  - Programmable slew rate for memory controller's IO pads
  - Dual rank memory device
  - Advanced bandwidth arbitration control

- **Peripherals**
  - USB2.0 HS/FS support
  - eMMC5.0
  - 4 UART for debugging and applications
  - SPI master for external device
  - 4 I2C to control peripheral devices, e.g. CMOS image sensor, LCM or FM receiver module
  - Max. 5 PWM channels (depending on system configuration/IO usage)
  - I2S for connection with optional external hi-end audio codec
  - GPIOs
  - 3 sets of memory card controllers supporting SD/SDHC/MS/MSPRO/MMC and SDIO2.0/3.0 protocols

- **Operating conditions**
  - Core voltage: 1.15V
  - I/O voltage: 1.8V/2.8V/3.3V
  - Memory: 1.2V
  - LCM interface: 1.8V
  - Clock source: 26MHz, 32.768kHz

- **Package**
  - Type: VFBGA
  - 12.6mm*12.6mm
  - Height: Max. 0.9mm
  - Ball count: 641 balls
  - Ball pitch: 0.4mm

1.3 Modem Features

- **LTE**
  - FDD: Up to 150Mbps downlink, 50Mbps uplink
  - TDD: Up to 150Mbps downlink, 50Mbps uplink
  - 1.4 to 20MHz RF bandwidth
  - 2*2 downlink SU-MIMO; 4*2 downlink SU-MIMO
  - IPv6, QoS
  - Inter-RAT capabilities with HSPA+, EDGE and applicable backward-compatible modes
  - SNOW3G/ZUC cipher offload engine

- **3G UMTS FDD supported features**
  - 3G modem supports most main features in 3GPP Release 7 and Release 8
  - CPC (DTX in CELL_DCH, UL DRX DL DRX), HS-SCCH-less, HS-DSCH
  - Dual cell operation
  - MAC-ehs
  - 2 DRX (receiver diversity) schemes in URA_PCH and CELL_PCH
  - Uplink Cat. 7 (16QAM), throughput up to 11.5Mbps
  - Downlink Cat. 24 (64QAM, dual-cell HSDPA), throughput up to 42.2Mbps
  - Fast dormancy
  - ETWS
  - Network selection enhancements

- **TD-SCDMA**
  - CDMA/HSDPA/HSUPA baseband
  - TD-SCDMA Bands 34, 39 & 40 and Quad band GSM/EDGE
  - Circuit-switched voice and data; packet-switched data
  - 384/384Kbps class in UL/DL for TD-SCDMA
  - TD-HSDPA: 2.8Mbps DL (Cat.14)
  - TD-HSUPA: 2.2Mbps UL (Cat.6)
  - F8/F9 ciphering/integrity protection

- **Radio interface and baseband front-end**
  - High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
  - 10-bit D/A converter for Automatic Power Control (APC)
  - Programmable radio Rx filter with adaptive gain control
  - Dedicated Rx filter for FB acquisition
  - Baseband Parallel Interface (BPI) with programmable driving strength
  - Supports multi-band

- **GSM modem and voice CODEC**
  - Dial tone generation
  - Noise reduction
  - Echo suppression
  - Advanced side-tone oscillation reduction
  - Digital side-tone generator with programmable gain
  - 2 programmable acoustic compensation filters
  - GSM quad vocoders for adaptive multi-rate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
  - GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
  - GPRS GEA1, GEA2 and GEA3 ciphering
  - Programmable GSM/GPRS/EDGE modem
  - Packet switched data with CS1/CS2/CS3/CS4 coding schemes
  - GSM circuit switch data
  - GPRS/EDGE Class 12
  - Supports SAIC (Single Antenna Interference Cancellation) technology
  - VAMOS (Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec

- **CDMA2000**
  - Supports cdma2000 1xRTT (release 1 and Advanced) and cdma2000 HRPD/1xEV-DO Revision 1 and A.
  - Hybrid operation between 1x and HEPD
  - Simultaneous hybrid dual receiver (SHDR) support.
  - Supports maximum 1x data rates of 153.6kbps for forward and reverse links and DO data rates of 3.1Mbps for forward link and 1.8Mbps for reverse link.
  - Supports 1x Diversity.

1.4 Connectivity Features

MT8735 includes four wireless connectivity functions:

- WLAN
- Bluetooth
- GPS
- FM Receiver

The RF parts of those four blocks are placed on chip MT6625. With four advanced radio technologies integrated on one chip, MT8735/MT6625 is the best and most convenient connectivity solution in the industry,MT8735 implementing advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It supports single antenna sharing among 2.4 GHz Bluetooth, 2.4GHz/5GHz WLAN and 1.575 GHz for GPS. The enhanced overall quality is achieved for simultaneous voice, data and audio/video transmission on mobile phones and Media Tablets. The small footprint with low-power consumption greatly reduces PCB layout resource. MT8735 also supports 802.11ac WLAN in advanced assorted with MT6630.

- **Supports integrated Wi-Fi/Bluetooth/GPS**
  - Single antenna for Bluetooth and WLAN/GPS/Bluetooth
  - Self calibration
  - Single TCXO and TMS for GPS, BT and WLAN
  - Best-in-class current consumption performance
  - Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (e.g. transmit window and duration that take into account protocol exchange sequence, frequency, etc.)
- **Wi-Fi**
  - Dual-band (2.4GHz/5Ghz) single stream 802.11 a/b/g/n MAC/BB/RF
  - 802.11 d/h/k compliant
  - Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (hardware)
  - QoS: WFA WMM, WMM PS
  - 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
  - Supports 802.11w protected managed frames
  - Supports Wi-Fi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
  - Supports Wi-Fi HotSpot 2.0
  - Integrated 2.4GHz PA with max. 19dBm CCK output power and 5GHz PA with max. 17dBm OFDM 54Mbps output power
  - Typical Rx sensitivity with companion chip modem: -75dBm at 11g 54Mbps mode and -75.5dBm at 11a 54Mbps mode
  - Per packet TX power control
- **Bluetooth**
  - Bluetooth specification v2.1+EDR
  - Bluetooth specification 3.0+HS compliance
  - Bluetooth v4.0 Low Energy (LE)
  - Integrated PA with 6dBm (class 1) transmit power
  - Typical Rx sensitivity with companion chip modem: GFSK -92.5dBm, DQPSK -91.5dBm, 8-DPSK -86dBm
  - Best-in-class BT/Wi-Fi coexistence performance
  - Up to 4 piconets simultaneously with background inquiry/page scan
  - Supports Scatternet
  - Packet Loss Concealment (PLC) function for better voice quality

  - Low-power scan function to reduce power consumption in scan modes

- **GPS**
  - GPS/Glonass/Beidou/QZSS tri-band reception concurrently
  - Supports SBAS (Satellite-Based Augmentation Systems): WAAS/MSAS/EGNOS/GAGAN
  - Best-in-class sensitivity performance
    - -165 dBm tracking sensitivity
    - -163 dBm hot start sensitivity
    - -148 dBm cold start sensitivity
    - -151 dBm warm start sensitivity
  - AGPS sensitivity is 6dB design margin over 3GPP
  - Full A-GPS capability (E911/SUPL/EPO/HotStill)
  - Active interference cancellation for up to 12 in-band tones
  - Supports both TCXO and TMS (Thermister Crystal) clock source
  - 5Hz update rate

- **FM**
  - 65-108MHz with 50kHz step
  - RDS/RBDS
  - Digital stereo demodulator
  - Simplified digital audio interface (I2S)
  - Stereo noise reduction
  - Audio sensitivity 2dBμVemf (SINAD=26dB)
  - Audio SINAD 60dB
  - Anti-jamming
  - Integrated short antenna

- **WBT IPD**
  - Integrated matching network, balance band-pass filter, GPS-WBT diplexer
  - Fully integrated in one IPD die
  - Single and dual antenna operation

- **GPS IPD**
  - Integrated high-pass type matching network and 5th-order ellipse low-pass filter
  - Fully integrated in one IPD die
  - Single and dual antenna operation

1.5 Multimedia Features

- **Display**
  - Portrait panel resolution up to WXGA (1,280*800)
  - MIPI DSI interface (4 data lanes)
  - MiraVisionTM for picture quality enhancement
  - Embedded LCD gamma correction
  - True colors
  - 4 overlay layers with per-pixel alpha channel and gamma table
  - Single and dual antenna operation, spatial and temporal dithering
  - Side-by-side format output to stereo 3D panel in both portrait and landscape modes
  - Color enhancement
  - Adaptive contrast enhancement
  - Image/video/graphic sharpness enhancement
  - Dynamic backlight scaling
  - Wide gamut

- **Graphics**
  - 3D graphic accelerator capable of processing 100M tri/sec and 900M pixel/sec @ 450 MHz
  - Support API standards OpenGL ES 1.1/2.0/3.0, OpenCL 1.0/1.1/1.2 and DirectX9

- **Image**
  - Integrated image signal processor supports 13MP@30fps.
  - Electronic image stabilization
  - Video stabilization
  - Preference color adjustment
  - Noise reduction
  - Multiple frame noise reduction for image capture
  - Temporal noise reduction for video recording
  - Lens shading correction
  - Auto sensor defect pixel correction
  - Supports AE/AWB/AF
  - Edge enhancement (sharpness)
  - Face detection and visual tracking
  - Video face beautification
  - Zero shutter delay image capture
  - Captures full size image when recording video (up to 13M sensors)
  - 2 MIPI CSI-2 high-speed camera serial interfaces; both are 4 data lane
  - PIP (picture in picture), [13MP + 5MP]@15fps
  - Hardware JPEG encoder: Baseline encoding with 130M pixel/sec. Continuous shot with 96M pixel/sec
  - Supports YUV422/YUV420 color format and EXIF/JFIF format

- **Video**
  - H.264 decoder: Baseline 1080p @ 30fps/40Mbps
  - H.264 decoder: Main/high profile 1080p @30fps/40Mbps
  - Sorenson H.263/H.263 decoder: 1080p @ 30fps/40Mbps
  - MPEG-4 SP/ASP decoder: 1080p @ 30fps/40Mbps
  - DIVX4/DIVX5/DIVX6/DIVX HD/XVID decoder: 1080p @ 30fps/40Mbps
  - H.264 encoder: High profile 1080p @ 30fps

- **Audio**
  - Audio content sampling rates supported: 8kHz to 192kHz
  - Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/Stereo
  - Interfaces supported: I2S, PCM
  - External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz.

  - 4-band IIR compensation filter to enhance loudspeaker responses
  - Proprietary audio post-processing technologies: BesLoudness(MB-DRC), BesSurround, Android built-in post processing
  - Audio encoding: AMR-NB, AMR-WB, AAC, OGG, ADPCM
  - Audio decoding: WAV, MP3, MP2, AAC, AMR-NB, AMR-WB, MIDI, Vorbis, APE, AAC-plus v1, AAC-plus v2, FLAC, WMA, ADPCM

- **Speech**
  - Speech codec (FR, HR, EFR, AMR FR, AMR HR and Wide-Band AMR)
  - CTM
  - Noise reduction
  - Noise suppression
  - Noise cancellation
  - Dual-MIC noise cancellation
  - Echo cancellation
  - Echo suppression
  - Dual-MIC voice tracking
  - Dual-MIC sound recording w/o Wind Noise Rejection
  - MagiLoudness (enhances the voice clarity based on near end environment noise)
  - MagiClarity (maximizes loudness while controlling the maximum receiver output power; feed-forward receiver protection)
  - Compensation filter and digital gain for both uplink and downlink paths

1.6 General Description

MediaTek's MT8735 is a highly integrated LTE System-on-Chip (SoC) which incorporates advanced features, e.g. LTE cat.4, Octa HMP core operating at 1.3GHz, 3D graphics (OpenGL|ES 3.0), 13M camera ISP, LPDDR3-640 Mbps, WXGA display and 1080p video codec. MT8735 helps tablet manufacturers build high-performance LTE tablet with PC-like browser, 3D gaming and cinema class home entertainment experiences.

The World-leading Technology!
Based on MediaTek's world-leading mobile chip SoC architecture with advanced 28nm process, MT8735 is the brand-new generation tablet SoC integrating MediaTek LTE modem, Quad-core ARM® Cortex-A53 MPCore™, 3D graphics and high-definition 1080p video decoder.

Rich in Features, High-value Product!
To enrich camera features, MT8735 equips a 13M camera ISP with advanced features, e.g. auto focus, electrical stabilization, auto sensor defect pixel correction, continuous video AF, face detection, face beautify, burst shot, panorama view, picture in picture, video in video and video face beautication.

Incredible Browser Experience!
The powerful CPU architecture with NEON multimedia processing engine brings PC-like browser experiences while keeping low standby power. GPU supporting OpenGL|ES 3.0 also provides you with excellent multimedia experiences.

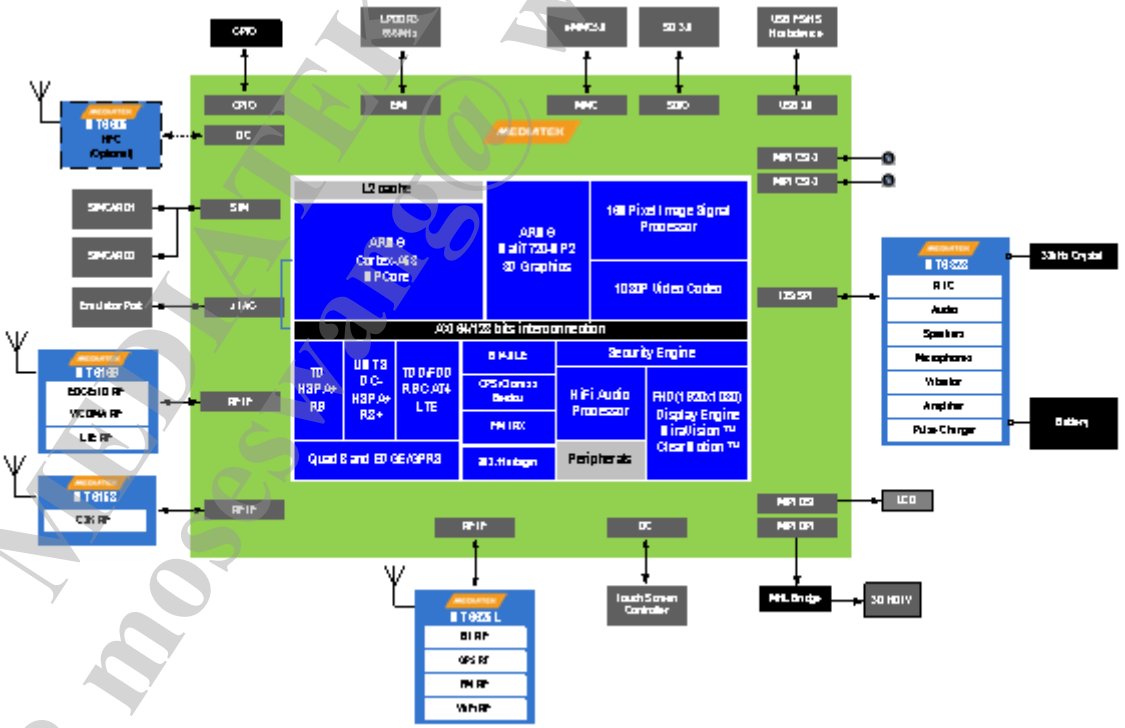


Figure 1-2. Block diagram of MT8735

2 Product Description

2.1 Pin Description

2.1.1 Ball Map View

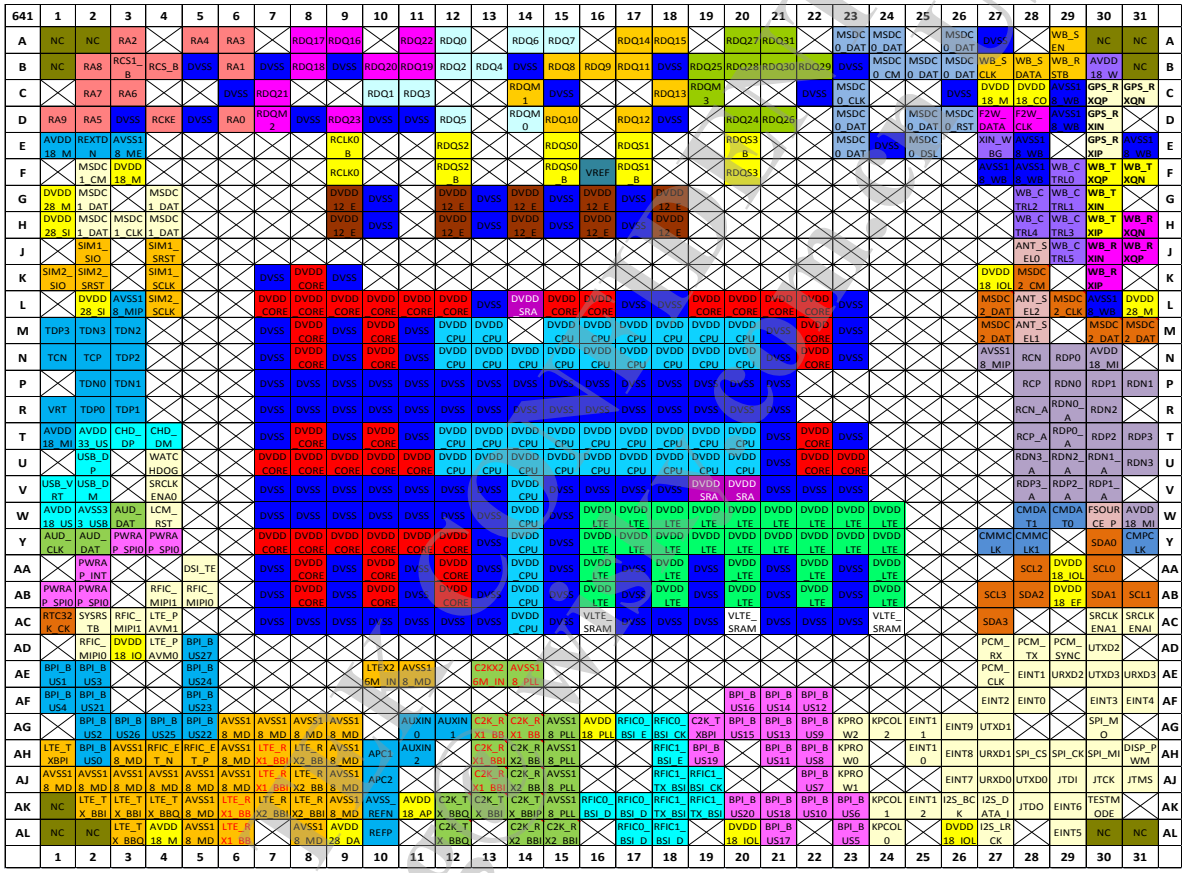


Figure 2-1. Ball map view for LPDDR3

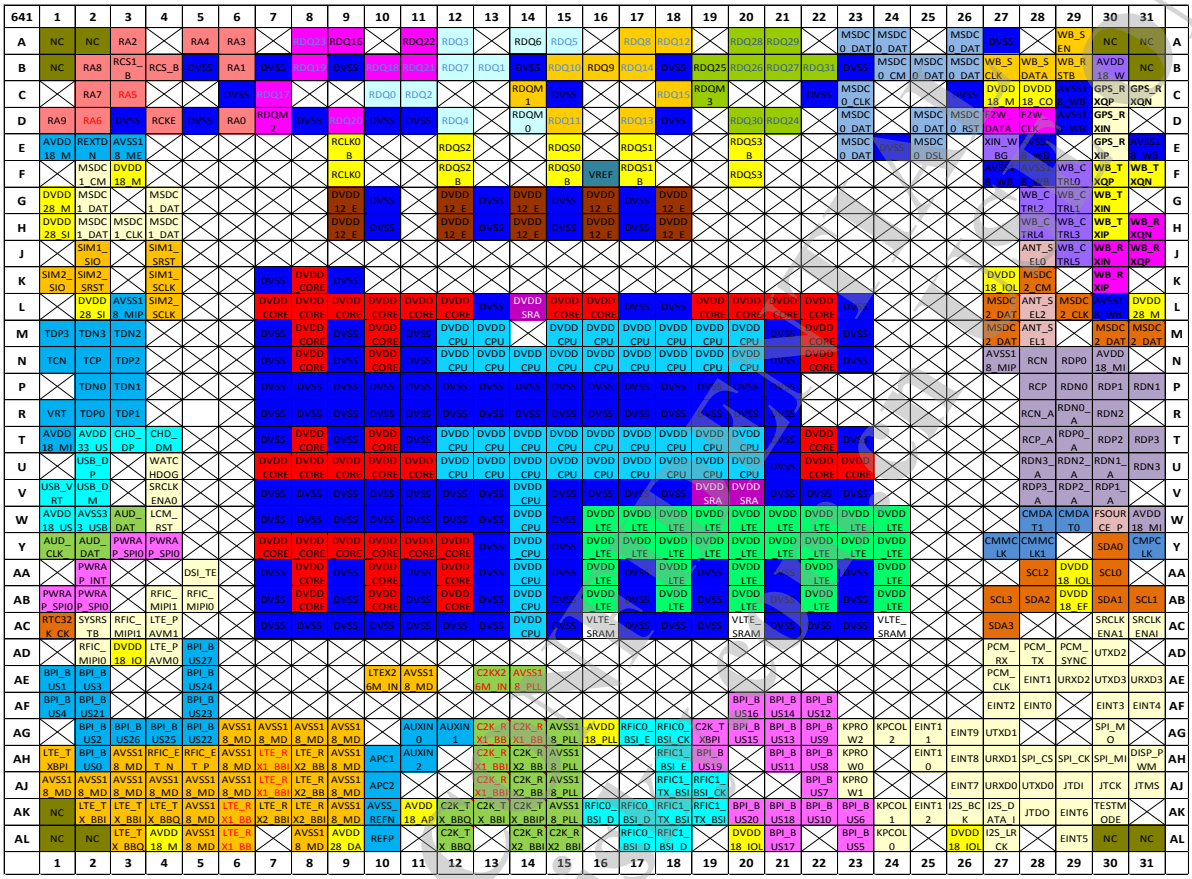


Figure 2-2. Ball map view for LPDDR2

2.1.2 Pin Coordinate

Table 2-1. Pin coordinate (using LPDDR3)

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A1	NC	M23	DVSS	AA28	SCL2
A2	NC	M27	MSDC2_DAT0	AA29	DVDD18_IOLB
A3	RA2	M28	ANT_SEL1	AA30	SCL0
A5	RA4	M30	MSDC2_DAT3	AB1	PWRAP_SPI0_MI
A6	RA3	M31	MSDC2_DAT2	AB2	PWRAP_SPI0_MO
A8	RDQ17	N1	TCN	AB4	RFIC_MIPI1_SDATA
A9	RDQ16	N2	TCP	AB5	RFIC_MIPI0_SDATA
A11	RDQ22	N3	TDP2	AB7	DVSS
A12	RDQ0	N7	DVSS	AB8	DVDD_CORE
A14	RDQ6	N8	DVDD_CORE	AB9	DVSS
A15	RDQ7	N9	DVSS	AB10	DVDD_CORE
A17	RDQ14	N10	DVDD_CORE	AB11	DVSS
A18	RDQ15	N11	DVSS	AB12	DVDD_CORE
A20	RDQ27	N12	DVDD_CPU	AB13	DVSS
A21	RDQ31	N13	DVDD_CPU	AB14	DVDD_CPU
A23	MSDC0_DAT4	N14	DVDD_CPU	AB15	DVSS

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
A24	MSDC0_DAT5	N15	DVDD_CPU	AB16	DVDD_LTE
A26	MSDC0_DAT0	N16	DVDD_CPU	AB17	DVSS
A27	DVSS	N17	DVDD_CPU	AB18	DVDD_LTE
A29	WB_SEN	N18	DVDD_CPU	AB19	DVSS
A30	NC	N19	DVDD_CPU	AB20	DVDD_LTE
A31	NC	N20	DVDD_CPU	AB21	DVSS
B1	NC	N21	DVSS	AB22	DVDD_LTE
B2	RA8	N22	DVDD_CORE	AB23	DVSS
B3	RCS1_B	N23	DVSS	AB24	DVDD_LTE
B4	RCS_B	N27	AVSS18_MIPIRX0	AB27	SCL3
B5	DVSS	N28	RCN	AB28	SDA2
B6	RA1	N29	RDP0	AB29	DVDD18_EFUSE
B7	DVSS	N30	AVDD18_MIPIRX0	AB30	SDA1
B8	RDQ18	P2	TDN0	AB31	SCL1
B9	DVSS	P3	TDN1	AC1	RTC32K_CK
B10	RDQ20	P7	DVSS	AC2	SYSRSTB
B11	RDQ19	P8	DVSS	AC3	RFIC_MIPI1_SCLK
B12	RDQ2	P9	DVSS	AC4	LTE_PAVM1
B13	RDQ4	P10	DVSS	AC7	DVSS
B14	DVSS	P11	DVSS	AC8	DVSS
B15	RDQ8	P12	DVSS	AC9	DVSS
B16	RDQ9	P13	DVSS	AC10	DVSS
B17	RDQ11	P14	DVSS	AC11	DVSS
B18	DVSS	P15	DVSS	AC12	DVSS
B19	RDQ25	P16	DVSS	AC13	DVSS
B20	RDQ28	P17	DVSS	AC14	DVDD_CPU
B21	RDQ30	P18	DVSS	AC15	DVSS
B22	RDQ29	P19	DVSS	AC16	VLTE_SRAM
B23	DVSS	P20	DVSS	AC17	DVSS
B24	MSDC0_CMD	P21	DVSS	AC18	DVSS
B25	MSDC0_DAT2	P28	RCP	AC19	DVSS
B26	MSDC0_DAT1	P29	RDN0	AC20	VLTE_SRAM
B27	WB_SCLK	P30	RDP1	AC21	DVSS
B28	WB_SDATA	P31	RDN1	AC22	DVSS
B29	WB_RSTB	R1	VRT	AC23	DVSS
B30	AVDD18_WBG	R2	TDP0	AC24	VLTE_SRAM
B31	NC	R3	TDP1	AC27	SDA3
C2	RA7	R7	DVSS	AC30	SRCLKENA1
C3	RA6	R8	DVSS	AC31	SRCLKENAI
C6	DVSS	R9	DVSS	AD2	RFIC_MIPI0_SCLK
C7	RDQ21	R10	DVSS	AD3	DVDD18_IORB
C10	RDQ1	R11	DVSS	AD4	LTE_PAVM0
C11	RDQ3	R12	DVSS	AD5	BPI_BUS27
C14	RDQM1	R13	DVSS	AD27	PCM_RX
C15	DVSS	R14	DVSS	AD28	PCM_TX
C18	RDQ13	R15	DVSS	AD29	PCM_SYNC
C19	RDQM3	R16	DVSS	AD30	UTXD2
C22	DVSS	R17	DVSS	AE1	BPI_BUS1
C23	MSDC0_CLK	R18	DVSS	AE2	BPI_BUS3
C26	DVSS	R19	DVSS	AE5	BPI_BUS24
C27	DVDD18_MC0	R20	DVSS	AE10	LTEX26M_IN
C28	DVDD18_CONN	R21	DVSS	AE11	AVSS18_MD

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
C29	AVSS18_WBG	R28	RCN_A	AE13	C2KX26M_IN
C30	GPS_RXQP	R29	RDN0_A	AE14	AVSS18_PLLGP
C31	GPS_RXQN	R30	RDN2	AE27	PCM_CLK
D1	RA9	T1	AVDD18_MIPITX	AE28	EINT1
D2	RA5	T2	AVDD33_USB	AE29	URXD2
D3	DVSS	T3	CHD_DP	AE30	UTXD3
D4	RCKE	T4	CHD_DM	AE31	URXD3
D5	DVSS	T7	DVSS	AF1	BPI_BUS4
D6	RA0	T8	DVDD_CORE	AF2	BPI_BUS21
D7	RDQM2	T9	DVSS	AF5	BPI_BUS23
D8	DVSS	T10	DVDD_CORE	AF20	BPI_BUS16
D9	RDQ23	T11	DVSS	AF21	BPI_BUS14
D10	DVSS	T12	DVDD_CPU	AF22	BPI_BUS12
D11	DVSS	T13	DVDD_CPU	AF27	EINT2
D12	RDQ5	T14	DVDD_CPU	AF28	EINT0
D14	RDQM0	T15	DVDD_CPU	AF30	EINT3
D15	RDQ10	T16	DVDD_CPU	AF31	EINT4
D17	RDQ12	T17	DVDD_CPU	AG2	BPI_BUS2
D18	DVSS	T18	DVDD_CPU	AG3	BPI_BUS26
D20	RDQ24	T19	DVDD_CPU	AG4	BPI_BUS25
D21	RDQ26	T20	DVDD_CPU	AG5	BPI_BUS22
D23	MSDC0_DAT6	T21	DVSS	AG6	AVSS18_MD
D25	MSDC0_DAT7	T22	DVDD_CORE	AG7	AVSS18_MD
D26	MSDC0_RSTB	T23	DVSS	AG8	AVSS18_MD
D27	F2W_DATA	T28	RCP_A	AG9	AVSS18_MD
D28	F2W_CLK	T29	RDP0_A	AG11	AUXIN0
D29	AVSS18_WBG	T30	RDP2	AG12	AUXIN1
D30	GPS_RXIN	T31	RDP3	AG13	C2K_RX1_BBQP
E1	AVDD18_MEMPLL	U2	USB_DP	AG14	C2K_RX1_BBQN
E2	REXTDN	U4	WATCHDOG	AG15	AVSS18_PLLGP
E3	AVSS18_MEMPLL	U7	DVDD_CORE	AG16	AVDD18_PLLGP
E9	RCLK0_B	U8	DVDD_CORE	AG17	RFIC0_BSI_EN
E12	RDQS2	U9	DVDD_CORE	AG18	RFIC0_BSI_CK
E15	RDQS0	U10	DVDD_CORE	AG19	C2K_TXBPI
E17	RDQS1	U11	DVDD_CORE	AG20	BPI_BUS15
E20	RDQS3_B	U12	DVDD_CPU	AG21	BPI_BUS13
E23	MSDC0_DAT3	U13	DVDD_CPU	AG22	BPI_BUS9
E24	DVSS	U14	DVDD_CPU	AG23	KPROW2
E25	MSDC0_DSL	U15	DVDD_CPU	AG24	KPCOL2
E27	XIN_WBG	U16	DVDD_CPU	AG25	EINT11
E28	AVSS18_WBG	U17	DVDD_CPU	AG26	EINT9
E30	GPS_RXIP	U18	DVDD_CPU	AG27	UTXD1
E31	AVSS18_WBG	U19	DVDD_CPU	AG30	SPI_MO
F2	MSDC1_CMD	U20	DVDD_CPU	AH1	LTE_TXBPI
F3	DVDD18_MC1	U21	DVSS	AH2	BPI_BUS0
F9	RCLK0	U22	DVDD_CORE	AH3	AVSS18_MD
F12	RDQS2_B	U23	DVDD_CORE	AH4	RFIC_ET_N
F15	RDQS0_B	U28	RDN3_A	AH5	RFIC_ET_P
F16	VREF	U29	RDN2_A	AH6	AVSS18_MD
F17	RDQS1_B	U30	RDN1_A	AH7	LTE_RX1_BBIP
F20	RDQS3	U31	RDN3	AH8	LTE_RX2_BBQN

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
F27	AVSS18_WBG	V1	USB_VRT	AH9	AVSS18_MD
F28	AVSS18_WBG	V2	USB_DM	AH10	APC1
F29	WB_CTRL0	V4	SRCLKENA0	AH11	AUXIN2
F30	WB_TXQP	V7	DVSS	AH13	C2K_RX1_BBIN
F31	WB_TXQN	V8	DVSS	AH14	C2K_RX2_BBQP
G1	DVDD28_MC1	V9	DVSS	AH15	AVSS18_PLLGP
G2	MSDC1_DAT3	V10	DVSS	AH18	RFIC1_BSI_EN
G4	MSDC1_DAT0	V11	DVSS	AH19	BPI_BUS19
G9	DVDD12_EMI	V12	DVSS	AH21	BPI_BUS11
G10	DVSS	V13	DVSS	AH22	BPI_BUS8
G12	DVDD12_EMI	V14	DVDD_CPU	AH23	KPROW0
G13	DVSS	V15	DVSS	AH25	EINT10
G14	DVDD12_EMI	V16	DVSS	AH26	EINT8
G15	DVSS	V17	DVSS	AH27	URXD1
G16	DVDD12_EMI	V18	DVSS	AH28	SPI_CS
G17	DVSS	V19	DVDD_SRAM	AH29	SPI_CK
G18	DVDD12_EMI	V20	DVDD_SRAM	AH30	SPI_MI
G28	WB_CTRL2	V21	DVSS	AH31	DISP_PWM
G29	WB_CTRL1	V22	DVSS	AJ1	AVSS18_MD
G30	WB_TXIN	V23	DVSS	AJ2	AVSS18_MD
H1	DVDD28_SIM1	V28	RDP3_A	AJ3	AVSS18_MD
H2	MSDC1_DAT2	V29	RDP2_A	AJ4	AVSS18_MD
H3	MSDC1_CLK	V30	RDP1_A	AJ5	AVSS18_MD
H4	MSDC1_DAT1	W1	AVDD18_USB	AJ6	AVSS18_MD
H9	DVDD12_EMI	W2	AVSS33_USB	AJ7	LTE_RX1_BBIN
H10	DVSS	W3	AUD_DAT_MISO	AJ8	LTE_RX2_BBQP
H12	DVDD12_EMI	W4	LCM_RST	AJ9	AVSS18_MD
H13	DVSS	W7	DVSS	AJ10	APC2
H14	DVDD12_EMI	W8	DVSS	AJ13	C2K_RX1_BBIP
H15	DVSS	W9	DVSS	AJ14	C2K_RX2_BBQN
H16	DVDD12_EMI	W10	DVSS	AJ15	AVSS18_PLLGP
H17	DVSS	W11	DVSS	AJ18	RFIC1_TX_BSI_D0
H18	DVDD12_EMI	W12	DVSS	AJ19	RFIC1_BSI_CK
H28	WB_CTRL4	W13	DVSS	AJ22	BPI_BUS7
H29	WB_CTRL3	W14	DVDD_CPU	AJ23	KPROW1
H30	WB_TXIP	W15	DVSS	AJ26	EINT7
H31	WB_RXQN	W16	DVDD_LTE	AJ27	URXD0
J2	SIM1_SIO	W17	DVDD_LTE	AJ28	UTXD0
J4	SIM1_SRST	W18	DVDD_LTE	AJ29	JTDI
J28	ANT_SEL0	W19	DVDD_LTE	AJ30	JTCK
J29	WB_CTRL5	W20	DVDD_LTE	AJ31	JTMS
J30	WB_RXIN	W21	DVDD_LTE	AK1	NC
J31	WB_RXQP	W22	DVDD_LTE	AK2	LTE_TX_BBIP
K1	SIM2_SIO	W23	DVDD_LTE	AK3	LTE_TX_BBIN
K2	SIM2_SRST	W24	DVDD_LTE	AK4	LTE_TX_BBQN
K4	SIM1_SCLK	W28	CMDAT1	AK5	AVSS18_MD
K7	DVSS	W29	CMDAT0	AK6	LTE_RX1_BBQP
K8	DVDD_CORE	W30	FSOURCE_P	AK7	LTE_RX2_BBIP
K9	DVSS	W31	AVDD18_MIPIRX1	AK8	LTE_RX2_BBIN
K27	DVDD18_IOLT	Y1	AUD_CLK_MOSI	AK9	AVSS18_MD
K28	MSDC2_CMD	Y2	AUD_DAT_MOSI	AK10	AVSS_REFN

Ball Loc.	Ball name	Ball Loc.	Ball name	Ball Loc.	Ball name
K30	WB_RXIP	Y3	PWRAP_SPI0_CK	AK11	AVDD18_AP
L2	DVDD28_SIM2	Y4	PWRAP_SPI0_CSN	AK12	C2K_TX_BBQN
L3	AVSS18_MIPITX	Y7	DVDD_CORE	AK13	C2K_TX_BBIN
L4	SIM2_SCLK	Y8	DVDD_CORE	AK14	C2K_TX_BBIP
L7	DVDD_CORE	Y9	DVDD_CORE	AK15	AVSS18_PLLGP
L8	DVDD_CORE	Y10	DVDD_CORE	AK16	RFIC0_BSI_D2
L9	DVDD_CORE	Y11	DVDD_CORE	AK17	RFIC0_BSI_D0
L10	DVDD_CORE	Y12	DVDD_CORE	AK18	RFIC1_TX_BSI_CK
L11	DVDD_CORE	Y13	DVSS	AK19	RFIC1_TX_BSI_EN
L12	DVDD_CORE	Y14	DVDD_CPU	AK20	BPI_BUS20
L13	DVSS	Y15	DVSS	AK21	BPI_BUS18
L14	DVDD_SRAM	Y16	DVDD_LTE	AK22	BPI_BUS10
L15	DVDD_CORE	Y17	DVDD_LTE	AK23	BPI_BUS6
L16	DVDD_CORE	Y18	DVDD_LTE	AK24	KPCOL1
L17	DVSS	Y19	DVDD_LTE	AK25	EINT12
L18	DVSS	Y20	DVDD_LTE	AK26	I2S_BCK
L19	DVDD_CORE	Y21	DVDD_LTE	AK27	I2S_DATA_IN
L20	DVDD_CORE	Y22	DVDD_LTE	AK28	JTDO
L21	DVDD_CORE	Y23	DVDD_LTE	AK29	EINT6
L22	DVDD_CORE	Y24	DVDD_LTE	AK30	TESTMODE
L23	DVSS	Y27	CMMCLK	AL1	NC
L27	MSDC2_DAT1	Y28	CMMCLK1	AL2	NC
L28	ANT_SEL2	Y30	SDA0	AL3	LTE_TX_BBQP
L29	MSDC2_CLK	Y31	CMPCLK	AL4	AVDD18_MD
L30	AVSS18_WBG	AA2	PWRAP_INT	AL5	AVSS18_MD
L31	DVDD28_MC2	AA5	DSI_TE	AL6	LTE_RX1_BBQN
M1	TDP3	AA7	DVSS	AL8	AVSS18_MD
M2	TDN3	AA8	DVDD_CORE	AL9	AVDD28_DAC
M3	TDN2	AA9	DVSS	AL10	REFP
M7	DVSS	AA10	DVDD_CORE	AL12	C2K_TX_BBQP
M8	DVDD_CORE	AA11	DVSS	AL14	C2K_RX2_BBIN
M9	DVSS	AA12	DVDD_CORE	AL15	C2K_RX2_BBIP
M10	DVDD_CORE	AA13	DVSS	AL17	RFIC0_BSI_D1
M11	DVSS	AA14	DVDD_CPU	AL18	RFIC1_BSI_D0
M12	DVDD_CPU	AA15	DVSS	AL20	DVDD18_IOLB
M13	DVDD_CPU	AA16	DVDD_LTE	AL21	BPI_BUS17
M15	DVDD_CPU	AA17	DVSS	AL23	BPI_BUS5
M16	DVDD_CPU	AA18	DVDD_LTE	AL24	KPCOL0
M17	DVDD_CPU	AA19	DVSS	AL26	DVDD18_IOLB
M18	DVDD_CPU	AA20	DVDD_LTE	AL27	I2S_LRCK
M19	DVDD_CPU	AA21	DVSS	AL29	EINT5
M20	DVDD_CPU	AA22	DVDD_LTE	AL30	NC
M21	DVSS	AA23	DVSS	AL31	NC
M22	DVDD_CORE	AA24	DVDD_LTE		

2.1.3 Detailed Pin Description

Table 2-2. Acronym for pin type

Abbreviation	Description

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 2-3. Detailed pin description (using LPDDR3)

Pin name	Type	Description	Power domain
SYSTEM			
SYSRSTB	DI	System reset input	DVDD18_IORB
WATCHDOG	DO	Watchdog reset output	DVDD18_IORB
TESTMODE	DIO	Test mode	DVDD18_IOLB
RTC32K_CK	DIO	32K clock input	DVDD18_IORB
SRCLKENAI	DIO	26MHz co-clock enable input	DVDD18_IOLB
SRCLKENA0	DIO	26MHz co-clock enable output	DVDD18_IORB
SRCLKENA1	DIO	26MHz co-clock enable output	DVDD18_IOLB
PMIC			
PWRAP_SPI0_MO	DIO	PMIC SPI control interface	DVDD18_IORB
PWRAP_SPI0_MI	DIO	PMIC SPI control interface	DVDD18_IORB
PWRAP_SPI0_CSN	DIO	PMIC SPI control interface	DVDD18_IORB
PWRAP_SPI0_CK	DIO	PMIC SPI control interface	DVDD18_IORB
PWRAP_INT	DIO	PMIC SPI control interface	DVDD18_IORB
AUD_CLK_MOSI	DIO	PMIC audio input interface	DVDD18_IORB
AUD_DAT_MOSI	DIO	PMIC audio input interface	DVDD18_IORB
AUD_DAT_MISO	DIO	PMIC audio input interface	DVDD18_IORB
SIM			
SIM1_SIO	DIO	SIM1 data, PMIC interface	DVDD18_MC1
SIM1_SRST	DIO	SIM1 reset, PMIC interface	DVDD18_MC1
SIM1_SCLK	DIO	SIM1 clock, PMIC interface	DVDD18_MC1
SIM2_SIO	DIO	SIM2 data, PMIC interface	DVDD18_MC1
SIM2_SRST	DIO	SIM2 reset, PMIC interface	DVDD18_MC1
SIM2_SCLK	DIO	SIM2 clock, PMIC interface	DVDD18_MC1
JTAG			
JTCK	DIO	JTCK	DVDD18_IOLB
JTDO	DIO	JTDO	DVDD18_IOLB
JTDI	DIO	JTDI	DVDD18_IOLB
JTMS	DIO	JTMS	DVDD18_IOLB
LCD			
DISP_PWM	DIO	Display PWM output	DVDD18_IOLB

Pin name	Type	Description	Power domain
DSI_TE	DIO	Parallel display interface tearing effect	DVDD18_IORB
LCM_RST	DIO	Parallel display interface reset signal	DVDD18_IORB
I2S			
I2S_DATA_IN	DIO	I2S data input pin	DVDD18_IOLB
I2S_BCK	DIO	I2S clock	DVDD18_IOLB
I2S_LRCK	DIO	I2S word select	DVDD18_IOLB
PCM/I2S merge interface			
PCM_TX	DIO	PCM audio interface	DVDD18_IOLB
PCM_CLK	DIO	PCM audio interface	DVDD18_IOLB
PCM_RX	DIO	PCM audio interface	DVDD18_IOLB
PCM_SYNC	DIO	PCM audio interface	DVDD18_IOLB
EINT			
EINT0	DIO	External interrupt 0	DVDD18_IOLB
EINT1	DIO	External interrupt 1	DVDD18_IOLB
EINT2	DIO	External interrupt 2	DVDD18_IOLB
EINT3	DIO	External interrupt 3	DVDD18_IOLB
EINT4	DIO	External interrupt 4	DVDD18_IOLB
EINT5	DIO	External interrupt 5	DVDD18_IOLB
EINT6	DIO	External interrupt 6	DVDD18_IOLB
EINT7	DIO	External interrupt 7	DVDD18_IOLB
EINT8	DIO	External interrupt 8	DVDD18_IOLB
EINT9	DIO	External interrupt 9	DVDD18_IOLB
EINT10	DIO	External interrupt 10	DVDD18_IOLB
EINT11	DIO	External interrupt 11	DVDD18_IOLB
EINT12	DIO	External interrupt 12	DVDD18_IOLB
UART			
URXD0	DIO	UART0 RX	DVDD18_IOLB
UTXD0	DIO	UART0 TX	DVDD18_IOLB
URXD1	DIO	UART1 RX	DVDD18_IOLB
UTXD1	DIO	UART1 TX	DVDD18_IOLB
URXD2	DIO	UART2 RX	DVDD18_IOLB
UTXD2	DIO	UART2 TX	DVDD18_IOLB
URXD3	DIO	UART3 RX	DVDD18_IOLB
UTXD3	DIO	UART3 TX	DVDD18_IOLB
SPI			
SPI_CS	DIO	SPI chip select	DVDD18_IOLB
SPI_MI	DIO	SPI data in	DVDD18_IOLB
SPI_MO	DIO	SPI data out	DVDD18_IOLB
SPI_CK	DIO	SPI clock	DVDD18_IOLB
BPI			
BPI_BUS0	DIO	BPI1 BUS0	DVDD18_IORB
BPI_BUS1	DIO	BPI1 BUS1	DVDD18_IORB

Pin name	Type	Description	Power domain
BPI_BUS2	DIO	BPI1 BUS2	DVDD18_IORB
BPI_BUS3	DIO	BPI1 BUS3	DVDD18_IORB
BPI_BUS4	DIO	BPI1 BUS4	DVDD18_IORB
BPI_BUS5	DIO	BPI1 BUS5	DVDD18_IOLB
BPI_BUS6	DIO	BPI1 BUS6	DVDD18_IOLB
BPI_BUS7	DIO	BPI1 BUS7	DVDD18_IOLB
BPI_BUS8	DIO	BPI1 BUS8	DVDD18_IOLB
BPI_BUS9	DIO	BPI1 BUS9	DVDD18_IOLB
BPI_BUS10	DIO	BPI1 BUS10	DVDD18_IOLB
BPI_BUS11	DIO	BPI1 BUS11	DVDD18_IOLB
BPI_BUS12	DIO	BPI1 BUS12	DVDD18_IOLB
BPI_BUS13	DIO	BPI1 BUS13	DVDD18_IOLB
BPI_BUS14	DIO	BPI1 BUS14	DVDD18_IOLB
BPI_BUS15	DIO	BPI1 BUS15	DVDD18_IOLB
BPI_BUS16	DIO	BPI1 BUS16	DVDD18_IOLB
BPI_BUS17	DIO	BPI1 BUS17	DVDD18_IOLB
BPI_BUS18	DIO	BPI1 BUS18	DVDD18_IOLB
BPI_BUS19	DIO	BPI1 BUS19	DVDD18_IOLB
BPI_BUS20	DIO	BPI1 BUS20	DVDD18_IOLB
BPI_BUS21	DIO	BPI1 BUS21	DVDD18_IORB
BPI_BUS22	DIO	BPI1 BUS22	DVDD18_IORB
BPI_BUS23	DIO	BPI1 BUS23	DVDD18_IORB
BPI_BUS24	DIO	BPI1 BUS24	DVDD18_IORB
BPI_BUS25	DIO	BPI1 BUS25	DVDD18_IORB
BPI_BUS26	DIO	BPI1 BUS26	DVDD18_IORB
BPI_BUS27	DIO	BPI1 BUS27	DVDD18_IORB
ANT_SEL0	DIO	Antenna select 0	DVDD18_IOLT
ANT_SEL1	DIO	Antenna select 1	DVDD18_IOLT
ANT_SEL2	DIO	Antenna select 2	DVDD18_IOLT
VM			
LTE_PAVM1	DIO	PA mode selection	DVDD18_IORB
LTE_PAVM0	DIO	PA mode selection	DVDD18_IORB
BSI			
RFIC1_BSI_EN	DIO	RFIC1 BSI enable	DVDD18_IOLB
RFIC1_BSI_CK	DIO	RFIC1 BSI clock	DVDD18_IOLB
RFIC1_BSI_D0	DIO	RFIC1 BSI Data0	DVDD18_IOLB
RFIC1_TX_BSI_EN	DIO	RFIC1 TX BSI enable	DVDD18_IOLB
RFIC1_TX_BSI_CK	DIO	RFIC1 TX BSI clock	DVDD18_IOLB
RFIC1_TX_BSI_D0	DIO	RFIC1 TX BSI Data0	DVDD18_IOLB
RFIC0_BSI_EN	DIO	RFIC0 BSI enable	DVDD18_IOLB
RFIC0_BSI_CK	DIO	RFIC0 BSI clock	DVDD18_IOLB
RFIC0_BSI_D2	DIO	RFIC0 BSI Data2	DVDD18_IOLB
RFIC0_BSI_D1	DIO	RFIC0 BSI Data1	DVDD18_IOLB

Pin name	Type	Description	Power domain
RFIC0_BSI_D0	DIO	RFIC0 BSI Data0	DVDD18_IOLB
RFIC_MIPI1_SCLK	DIO	RFIC MIPI1 SCLK	DVDD18_IORB
RFIC_MIPI1_SDATA	DIO	RFIC MIPI1 SDATA	DVDD18_IORB
RFIC_MIPI0_SCLK	DIO	RFIC MIPI0 SCLK	DVDD18_IORB
RFIC_MIPI0_SDATA	DIO	RFIC MIPI0 SDATA	DVDD18_IORB
C2K_TXBPI	DIO	C2K TXBPI	DVDD18_IOLB
LTE_TXBPI	DIO	LTE TXBPI	DVDD18_IORB
MSDC0			
MSDC0_DAT7	DIO	MSDC0 data7 pin	DVDD18_MC0
MSDC0_DAT6	DIO	MSDC0 data6 pin	DVDD18_MC0
MSDC0_DAT5	DIO	MSDC0 data5 pin	DVDD18_MC0
MSDC0_RSTB	DIO	MSDC0 reset output	DVDD18_MC0
MSDC0_DAT4	DIO	MSDC0 data4 pin	DVDD18_MC0
MSDC0_DAT2	DIO	MSDC0 data2 pin	DVDD18_MC0
MSDC0_DAT3	DIO	MSDC0 data3 pin	DVDD18_MC0
MSDC0_CMD	DIO	MSDC0 command pin	DVDD18_MC0
MSDC0_CLK	DIO	MSDC0 clock output	DVDD18_MC0
MSDC0_DAT1	DIO	MSDC0 data1 pin	DVDD18_MC0
MSDC0_DAT0	DIO	MSDC0 data0 pin	DVDD18_MC0
MSDC1			
MSDC1_CLK	DIO	MSDC1 clock output	DVDD28_MC1/DVDD18_MC1
MSDC1_CMD	DIO	MSDC1 command pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT0	DIO	MSDC1 data0 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT1	DIO	MSDC1 data1 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT2	DIO	MSDC1 data2 pin	DVDD28_MC1/DVDD18_MC1
MSDC1_DAT3	DIO	MSDC1 data3 pin	DVDD28_MC1/DVDD18_MC1
MSDC2			
MSDC2_CLK	DIO	MSDC2 clock output	DVDD28_MC2/DVDD18_IOLT
MSDC2_CMD	DIO	MSDC2 command pin	DVDD28_MC2/DVDD18_IOLT
MSDC2_DAT0	DIO	MSDC2 data0 pin	DVDD28_MC2/DVDD18_IOLT
MSDC2_DAT1	DIO	MSDC2 data1 pin	DVDD28_MC2/DVDD18_IOLT
MSDC2_DAT2	DIO	MSDC2 data2 pin	DVDD28_MC2/DVDD18_IOLT
MSDC2_DAT3	DIO	MSDC2 data3 pin	DVDD28_MC2/DVDD18_IOLT
WiFi/BT/GPS			
WB_SDATA	DIO	WiFi/BT SPI control data	DVDD18_CONN
WB_SCLK	DIO	WiFi/BT SPI control clock	DVDD18_CONN
WB_SEN	DIO	WiFi/BT SPI control enable	DVDD18_CONN
WB_RSTB	DIO	WiFi/BT SPI control reset	DVDD18_CONN
F2W_CLK	DIO	FM clock	DVDD18_CONN
F2W_DATA	DIO	FM data	DVDD18_CONN
WB_CTRL0	DIO	Data bus 0	DVDD18_IOLT

Pin name	Type	Description	Power domain
WB_CTRL1	DIO	Data bus 1	DVDD18_IOLT
WB_CTRL2	DIO	Data bus 2	DVDD18_IOLT
WB_CTRL3	DIO	Data bus 3	DVDD18_IOLT
WB_CTRL4	DIO	Data bus 4	DVDD18_IOLT
WB_CTRL5	DIO	Data bus 5	DVDD18_IOLT
EFUSE			
FSOURCE_P	DIO	E-FUSE blowing power control	FSOURCE_P
EMI			
RCLK0	DIO	DRAM clock 0 output	DVDD12_EMI
RCLK0_B	DIO	DRAM clock 0 output #	DVDD12_EMI
RCKE	DIO	DRAM command output CKE	DVDD12_EMI
RCS_B	DIO	DRAM chip select 0 #	DVDD12_EMI
RCS1_B	DIO	DRAM chip select 1 #	DVDD12_EMI
RA0	DIO	DRAM address output 0	DVDD12_EMI
RA1	DIO	DRAM address output 1	DVDD12_EMI
RA2	DIO	DRAM address output 2	DVDD12_EMI
RA3	DIO	DRAM address output 3	DVDD12_EMI
RA4	DIO	DRAM address output 4	DVDD12_EMI
RA5	DIO	DRAM address output 5	DVDD12_EMI
RA6	DIO	DRAM address output 6	DVDD12_EMI
RA7	DIO	DRAM address output 7	DVDD12_EMI
RA8	DIO	DRAM address output 8	DVDD12_EMI
RA9	DIO	DRAM address output 9	DVDD12_EMI
RDQM0	DIO	DRAM DQM 0	DVDD12_EMI
RDQM1	DIO	DRAM DQM 1	DVDD12_EMI
RDQM2	DIO	DRAM DQM 2	DVDD12_EMI
RDQM3	DIO	DRAM DQM 3	DVDD12_EMI
RDQS0	DIO	DRAM DQS 0	DVDD12_EMI
RDQS0_B	DIO	DRAM DQS 0 #	DVDD12_EMI
RDQS1	DIO	DRAM DQS 1	DVDD12_EMI
RDQS1_B	DIO	DRAM DQS 1 #	DVDD12_EMI
RDQS2	DIO	DRAM DQS 2	DVDD12_EMI
RDQS2_B	DIO	DRAM DQS 2 #	DVDD12_EMI
RDQS3	DIO	DRAM DQS 3	DVDD12_EMI
RDQS3_B	DIO	DRAM DQS 3 #	DVDD12_EMI
RDQ0	DIO	DRAM data pin 0	DVDD12_EMI
RDQ1	DIO	DRAM data pin 1	DVDD12_EMI
RDQ2	DIO	DRAM data pin 2	DVDD12_EMI
RDQ3	DIO	DRAM data pin 3	DVDD12_EMI
RDQ4	DIO	DRAM data pin 4	DVDD12_EMI
RDQ5	DIO	DRAM data pin 5	DVDD12_EMI
RDQ6	DIO	DRAM data pin 6	DVDD12_EMI
RDQ7	DIO	DRAM data pin 7	DVDD12_EMI

Pin name	Type	Description	Power domain
RDQ8	DIO	DRAM data pin 8	DVDD12_EMI
RDQ9	DIO	DRAM data pin 9	DVDD12_EMI
RDQ10	DIO	DRAM data pin 10	DVDD12_EMI
RDQ11	DIO	DRAM data pin 11	DVDD12_EMI
RDQ12	DIO	DRAM data pin 12	DVDD12_EMI
RDQ13	DIO	DRAM data pin 13	DVDD12_EMI
RDQ14	DIO	DRAM data pin 14	DVDD12_EMI
RDQ15	DIO	DRAM data pin 15	DVDD12_EMI
RDQ16	DIO	DRAM data pin 16	DVDD12_EMI
RDQ17	DIO	DRAM data pin 17	DVDD12_EMI
RDQ18	DIO	DRAM data pin 18	DVDD12_EMI
RDQ19	DIO	DRAM data pin 19	DVDD12_EMI
RDQ20	DIO	DRAM data pin 20	DVDD12_EMI
RDQ21	DIO	DRAM data pin 21	DVDD12_EMI
RDQ22	DIO	DRAM data pin 22	DVDD12_EMI
RDQ23	DIO	DRAM data pin 23	DVDD12_EMI
RDQ24	DIO	DRAM data pin 24	DVDD12_EMI
RDQ25	DIO	DRAM data pin 25	DVDD12_EMI
RDQ26	DIO	DRAM data pin 26	DVDD12_EMI
RDQ27	DIO	DRAM data pin 27	DVDD12_EMI
RDQ28	DIO	DRAM data pin 28	DVDD12_EMI
RDQ29	DIO	DRAM data pin 29	DVDD12_EMI
RDQ30	DIO	DRAM data pin 30	DVDD12_EMI
RDQ31	DIO	DRAM data pin 31	DVDD12_EMI
REXTDN	DIO	DRAM REXTDN pin	DVDD12_EMI
VREF	DIO		DVDD12_EMI
CAM			
CMPCLK	DIO	Pixel clock from sensor	DVDD18_IOLB
CMMCLK	DIO	Master clock to sensor	DVDD18_IOLB
CMMCLK1	DIO	Master clock1 to sensor	DVDD18_IOLB
CMDAT0	DIO	CAM sensor Data0	DVDD18_IOLB
CMDAT1	DIO	CAM sensor Data1	DVDD18_IOLB
I2C0			
SCL0	DIO	I2C0 clock	DVDD18_IOLB
SDA0	DIO	I2C0 data	DVDD18_IOLB
I2C1			
SCL1	DIO	I2C1 clock	DVDD18_IOLB
SDA1	DIO	I2C1 data	DVDD18_IOLB
I2C2			
SCL2	DIO	I2C2 clock	DVDD18_IOLB
SDA2	DIO	I2C2 data	DVDD18_IOLB
I2C3			
SCL3	DIO	I2C3 clock	DVDD18_IOLB

Pin name	Type	Description	Power domain
SDA3	DIO	I2C3 data	DVDD18_IOLB
ABB			
C2K_RX2_BBQP	AIO	C2K downlink QP for diversity path	AVDD18_MD
C2K_RX2_BBQN	AIO	C2K downlink QN for diversity path	AVDD18_MD
C2K_RX2_BBIN	AIO	C2K downlink IN for diversity path	AVDD18_MD
C2K_RX2_BBIP	AIO	C2K downlink IPP for diversity path	AVDD18_MD
C2K_RX1_BBQP	AIO	C2K downlink QP for main path	AVDD18_MD
C2K_RX1_BBQN	AIO	C2K downlink QN for main path	AVDD18_MD
C2K_RX1_BBIN	AIO	C2K downlink IN for main path	AVDD18_MD
C2K_RX1_BBIP	AIO	C2K downlink IPP for main path	AVDD18_MD
C2K_TX_BBQP	AIO	C2K uplink QP	AVDD18_MD
C2K_TX_BBQN	AIO	C2K uplink QN	AVDD18_MD
C2K_TX_BBIN	AIO	C2K uplink IN	AVDD18_MD
C2K_TX_BBIP	AIO	C2K uplink IP	AVDD18_MD
C2KX26M_IN	AIO	26MHz clock input for 2nd modem	AVDD18_MD
AUXIN0	AIO	AuxADC external input channel 0	AVDD18_AP
AUXIN1	AIO	AuxADC external input channel 1	AVDD18_AP
AUXIN2	AIO	AuxADC external input channel 2	AVDD18_AP
REFP	AIO	Positive reference port for internal circuit	AVDD18_AP
APC1	AIO	Automatic power control for MD1	AVDD28_DAC
APC2	AIO	Automatic power control for MD2	AVDD28_DAC
LTEX26M_IN	AIO	26MHz clock input for AP & 1st modem	AVDD18_MD
LTE_RX2_BBQP	AIO	LTE downlink QP for diversity path	AVDD18_MD
LTE_RX2_BBQN	AIO	LTE downlink QN for diversity path	AVDD18_MD
LTE_RX2_BBIN	AIO	LTE downlink IN for diversity path	AVDD18_MD
LTE_RX2_BBIP	AIO	LTE downlink IPP for diversity path	AVDD18_MD
LTE_RX1_BBQP	AIO	LTE downlink QP for main path	AVDD18_MD
LTE_RX1_BBQN	AIO	LTE downlink QN for main path	AVDD18_MD
LTE_RX1_BBIN	AIO	LTE downlink IN for main path	AVDD18_MD
LTE_RX1_BBIP	AIO	LTE downlink IP for main path	AVDD18_MD
LTE_TX_BBQP	AIO	LTE uplink QP	AVDD18_MD
LTE_TX_BBQN	AIO	LTE uplink QN	AVDD18_MD
LTE_TX_BBIN	AIO	LTE uplink IN	AVDD18_MD
LTE_TX_BBIP	AIO	LTE uplink IP	AVDD18_MD
RFIC_ET_N	AIO	Envelop Tracking DAC output N	AVDD18_MD
RFIC_ET_P	AIO	Envelop Tracking DAC output P	AVDD18_MD
WBG			
XIN_WBG	AIO	WIFI/BT clock source	AVDD18_WBG
GPS_RXQN	AIO	RXQN for GPS RX	AVDD18_WBG
GPS_RXQP	AIO	RXQP for GPS RX	AVDD18_WBG
GPS_RXIN	AIO	RXIN for GPS RX	AVDD18_WBG

Pin name	Type	Description	Power domain
GPS_RXIP	AIO	RXIP for GPS RX	AVDD18_WBG
WB_TXQN	AIO	TXQN for WIFI/BT TX	AVDD18_WBG
WB_TXQP	AIO	TXQP for WIFI/BT TX	AVDD18_WBG
WB_TXIN	AIO	TXIN for WIFI/BT TX	AVDD18_WBG
WB_TXIP	AIO	TXIP for WIFI/BT TX	AVDD18_WBG
WB_RXQN	AIO	RXQN for WIFI/BT RX	AVDD18_WBG
WB_RXQP	AIO	RXQP for WIFI/BT RX	AVDD18_WBG
WB_RXIN	AIO	RXIN for WIFI/BT RX	AVDD18_WBG
WB_RXIP	AIO	RXIP for WIFI/BT RX	AVDD18_WBG
MIPI			
TDN3	AIO	DSI0 lane3 N	DVDD18_MIPITX
TDP3	AIO	DSI0 lane3 P	DVDD18_MIPITX
TDN2	AIO	DSI0 lane2 N	DVDD18_MIPITX
TDP2	AIO	DSI0 lane2 P	DVDD18_MIPITX
TCN	AIO	DSI0 CK lane N	DVDD18_MIPITX
TCP	AIO	DSI0 CK lane P	DVDD18_MIPITX
TDN1	AIO	DSI0 lane1 N	DVDD18_MIPITX
TDP1	AIO	DSI0 lane1 P	DVDD18_MIPITX
TDN0	AIO	DSI0 lane0 N	DVDD18_MIPITX
TDP0	AIO	DSI0 lane0 P	DVDD18_MIPITX
VRT	AO	External resistor for DSI bias Connect 1.5K ohm 1% resistor to ground	DVDD18_MIPITX
RDN3	AIO	CSI0 lane3 N	DVDD18_MIPIRX0
RDP3	AIO	CSI0 lane3 P	DVDD18_MIPIRX0
RDN2	AIO	CSI0 lane2 N	DVDD18_MIPIRX0
RDP2	AIO	CSI0 lane2 P	DVDD18_MIPIRX0
RCN	AIO	CSI0 CK lane N	DVDD18_MIPIRX0
RCP	AIO	CSI0 CK lane P	DVDD18_MIPIRX0
RDN1	AIO	CSI0 lane1 N	DVDD18_MIPIRX0
RDP1	AIO	CSI0 lane1 P	DVDD18_MIPIRX0
RDN0	AIO	CSI0 lane0 N	DVDD18_MIPIRX0
RDP0	AIO	CSI0 lane0 P	DVDD18_MIPIRX0
RDN1_A	AIO	CSI1 lane1 N	DVDD18_MIPIRX1
RDP1_A	AIO	CSI1 lane1 P	DVDD18_MIPIRX1
RCN_A	AIO	CSI1 CK lane N	DVDD18_MIPIRX1
RCP_A	AIO	CSI1 CK lane P	DVDD18_MIPIRX1
RDN0_A	AIO	CSI1 lane0 N	DVDD18_MIPIRX1
RDP0_A	AIO	CSI1 lane0 P	DVDD18_MIPIRX1
RDN2_A	AIO	CSI1 lane 2 N	DVDD18_MIPIRX1
RDP2_A	AIO	CSI1 lane 2 P	DVDD18_MIPIRX1
RDN3_A	AIO	CSI1 lane 3 N	DVDD18_MIPIRX1
RDP3_A	AIO	CSI1 lane 3 P	DVDD18_MIPIRX1

Pin name	Type	Description	Power domain
USB			
USB_DP	AIO	USB porto D+ differential data line	AVDD33_USB
USB_DM	AIO	USB porto D- differential data line	AVDD33_USB
CHD_DP	AIO	BC1.1 Charger DP	AVDD33_USB
CHD_DM	AIO	BC1.1 Charger DM	AVDD33_USB
USB_VRT	AO	USB output for bias current; connect with 5.11K 1% Ohm to GND	AVDD18_USB
Keypad			
KPROW0	AIO	Keypad row 0	DVDD18_IOLB
KPROW1	AIO	Keypad row 1	DVDD18_IOLB
KPROW2	AIO	Keypad row 2	DVDD18_IOLB
KPCOL0	AIO	Keypad column 0	DVDD18_IOLB
KPCOL1	AIO	Keypad column 1	DVDD18_IOLB
KPCOL2	AIO	Keypad column 2	DVDD18_IOLB
Analog power			
DVDD18_PLLGP	P	Analog power input 1.8V for PLL	
AVDD18_AP	P	Analog power input 1.8V for AuxADC, TSENSE	
AVDD18_MD	P	Analog power input 1.8V for BBTX, BBRX, 2GBBTX	
AVDD18_MEMPLL	P	Analog power for MEMPLL	
AVDD18_USB	P	Analog power 1.8V for USB	
AVDD18_WBG	P	Analog power 1.8V for WiFi/BT/GPS	
DVDD18_MIPITX	P	Analog power for MIPI DSI	
DVDD18_MIPIRX0	P	Analog power for MIPI CSI	
DVDD18_MIPIRX1	P	Analog power for MIPI CSI	
AVDD28_DAC	P	Analog power input 2.8V for APC	
AVDD33_USB	P	Analog power 3.3V for USB port 1	
Digital power			
DVDD18_IOLT	P	Digital power input for IO	-
DVDD18_IOLB	P	Digital power input for IO	-
DVDD18_IORB	P	Digital power input for IO	-
DVDD18_CONN	P	Digital power input for IO	-
EVDD18_EFUSE	P	Digital power input for efuse IO	-
DVDD18_MC0	P	Digital power input for MSDC0 IO	-
DVDD18_MC1	P	Digital power input for MSDC1 IO	-
DVDD18_MC2	P	Digital power input for MSDC2 IO	-
DVDD28_MC1	P	Digital power input for 1.8/3.3V MSDC IO	-
DVDD28_MC2	P	Digital power input for 1.8/3.3V MSDC IO	-
DVDD12_EMI	P	Digital power input for 1.2V EMI	-
DVDD_TOP	P	Digital power input for core	-
DVDD_LTE	P	Digital power input for LTE	-

Pin name	Type	Description	Power domain
VLTE_SRAM	P	Digital power input for LTE SRAM	-
DVDD_CPU	P	Digital power input for processor	-
DVDD_SRAM	P	Digital power input for processor SRAM	-
Analog ground			
AVSS18_AP	G	analog ground	
AVSS18_MD	G	analog ground	
AVSS18_MEMPLL	G	analog ground	
AVSS18_WBG	G	analog ground	
AVSS_REFN	G	analog ground	
AVSS33_USB	G	analog ground	
DVSS18_MIPITX	G	analog ground	
DVSS18_MIPIRX0	G	analog ground	
DVSS18_MIPIRX1	G	analog ground	
AVSS33_USB	G	analog ground	
Digital ground			
DVSS	G	Digital ground	-

Table 2-4. Acronym for the table of state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
XO	Low or high output
PU	Pull-up
PD	Pull-dowm
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

Table 2-5. State of pins

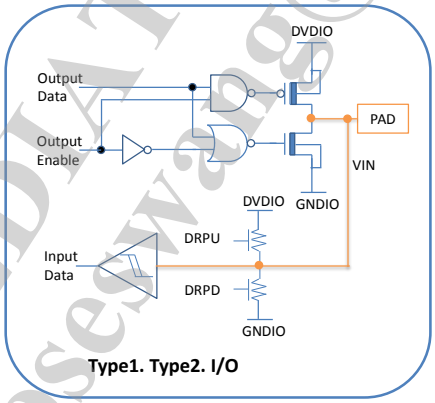
Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
eMMC Interface						
MSDC0_CLK	LO	1	-	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_CMD	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT0	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT1	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT2	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT3	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT4	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT5	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT6	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DAT7	I	1	PU	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_RSTB	HO	1	-	DIOH4,DIOL4	No Need	IO Type 4
MSDC0_DSL	I	1	PD	DIOH4,DIOL4	No Need	IO Type 4
SD Card Interface						
MSDC1_CLK	LO	1	-	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_CMD	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT0	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT1	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT2	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
MSDC1_DAT3	I	1	PU	DIOH6,DIOL6	No Need	IO Type 6
SIM Interface						
SIM1_SCLK	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM1_SRST	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM1_SIO	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SCLK	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SRST	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
SIM2_SIO	I	0	PD	DIOH7,DIOL7	No Need	IO Type 7
Audio Interface						
AUD_CLK_MOSI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
AUD_DAT_MISO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
AUD_DAT_MOSI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LCD Control						
DISP_PWM	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LCM_RST	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
DSI_TE	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CAM Interface						
CMPCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CMMCLK	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
CMMCLK1	I	0	PD	DIOH4,DIOL4	No Need	IO Type 4
CMPDAT0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
CMPDAT1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1

[1] The column "State" of "Reset" shows the pin state during reset (Input, High Output, Low Output, etc).
[2] The column "Aux" for "Reset" means the default aux. funtion number shown in Table "Pin Multiplexing, Capability and Settings".
[3] The column "PU/PD" for "Reset" means if there is internal pull-up or pull-down when the pin is input in the reset state.

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
PMIC SPI Interface						
PWRAP_SPI0_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_CSN	I	0	PU	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_MI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
PWRAP_SPI0_MO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2C Interface						
SCL0	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SCL1	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SCL2	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SCL3	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SDA0	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SDA1	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
SDA2	I	1	-	DIOH1,DIOL1	No Need	IO Type 1
SDA3	I	1	-	DIOH3,DIOL3	No Need	IO Type 3
RFIC Interface						
RFIC0_BSI_EN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC0_BSI_D2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_EN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_BSI_D0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_TX_BSI_EN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_TX_BSI_CK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC1_TX_BSI_D0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC_MIPI1_SCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC_MIPI1_SDATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC_MIPI0_SCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
RFIC_MIPI0_SDATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI Interface						
BPI_BUS0	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS1	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS2	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS3	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS4	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS5	I	0	PD	DIOH6,DIOL6	No Need	IO Type 6
BPI_BUS6	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS7	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS8	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS9	I	0	PD	DIOH5,DIOL5	No Need	IO Type 5
BPI_BUS10	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS11	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS12	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS13	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS14	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS15	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS16	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS17	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1

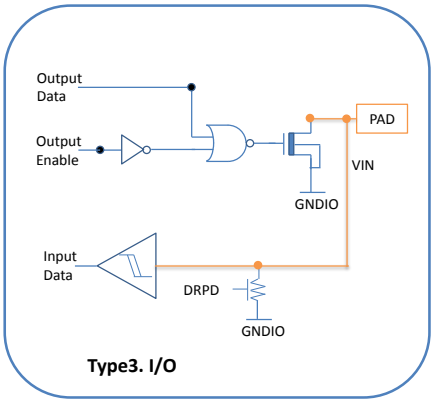
Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
BPI_BUS18	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS19	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS20	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS21	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS22	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS23	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS24	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS25	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS26	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
BPI_BUS27	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
LTE_TXBPI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
C2K_TXBPI	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
Connectivity RF Interface						
WB_CTRL0	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL3	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL4	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_CTRL5	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
F2W_DATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
F2W_CLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SCLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SDATA	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_SEN	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
WB_RSTB	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
Keypad						
KPCOL0	I	1	PU	DIOH1,DIOL1	No Need	IO Type 1
KPCOL1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
KPCOL2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
KPROW0	LO	1	PD	DIOH1,DIOL1	No Need	IO Type 1
KPROW1	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
KPROW2	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
DPI Interface						
DPI_D0	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D1	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D2	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D3	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D4	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D5	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D6	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D7	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D8	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D9	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D10	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_D11	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_DE	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_CK	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
DPI_HSYNC	I	0	PU	DIOH2,DIOL2	No Need	IO Type 2
DPI_VSYNC	I	0	PU	DIOH2,DIOL2	No Need	IO Type 2

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
I2S Interface						
I2S0_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S0_BCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S0_LRCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S0_DI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S1_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S1_BCK	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
I2S1_LRCK	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
I2S1_DO	I	0	PD	DIOH2,DIOL2	No Need	IO Type 2
I2S2_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S2_BCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S2_LRCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S2_DI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S3_MCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S3_BCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S3_LRCK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
I2S3_DO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI Interface						
SPI_CSB	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_CLK	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_MO	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
SPI_MI	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
System /Reset Clock Enable						
WATCHDOG	HO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENA0	HO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENA1	LO	1	-	DIOH1,DIOL1	No Need	IO Type 1
SRCLKENAI	I	1	PD	DIOH1,DIOL1	No Need	IO Type 1
IDDIG	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1
USB_DRVBUS	I	0	PD	DIOH1,DIOL1	No Need	IO Type 1



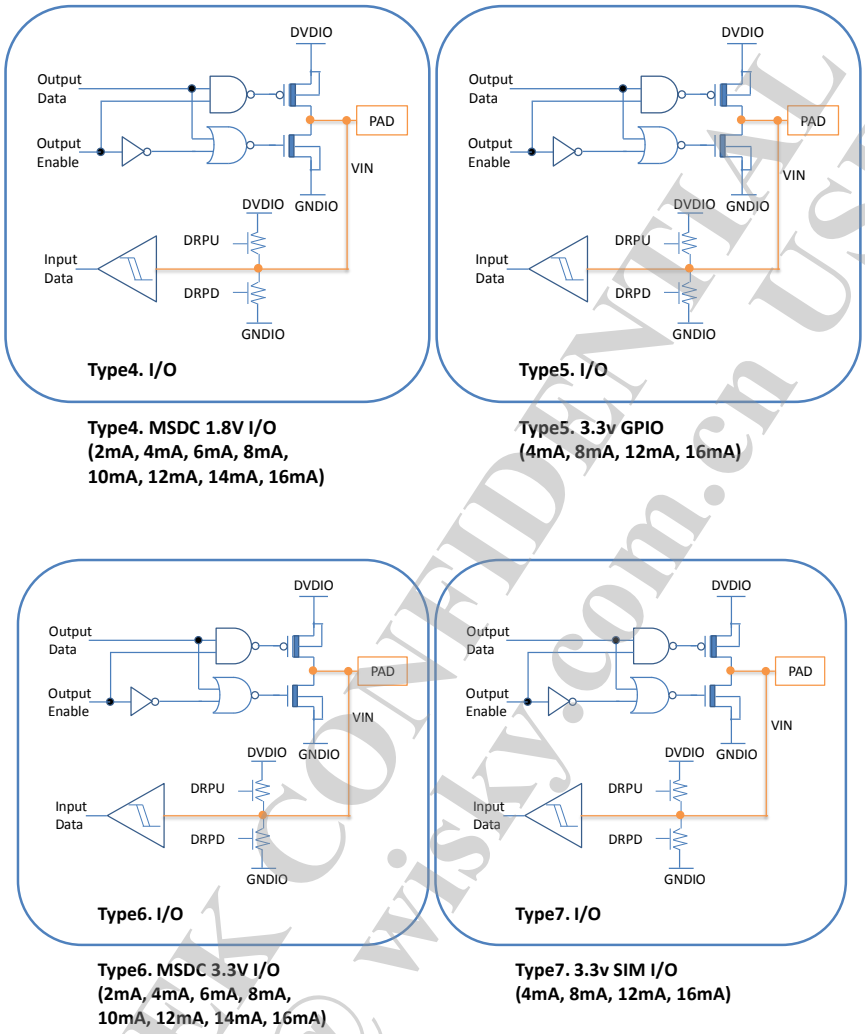
Type1. Type2. I/O

Type1. GPIO 28 type
(2mA, 4mA, 6mA, 8mA)
Type2. GPIO 4G type
(4mA, 8mA, 12mA, 16mA)



Type3. I/O

Type 3. Open-drain IO



Type4. MSDC 1.8V I/O (2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA)

Type5. 3.3v GPIO (4mA, 8mA, 12mA, 16mA)

Type6. MSDC 3.3V I/O (2mA, 4mA, 6mA, 8mA, 10mA, 12mA, 14mA, 16mA)

Type7. 3.3v SIM I/O (4mA, 8mA, 12mA, 16mA)

Figure 2-3. IO types in state of pins

2.1.4 Pin Multiplexing, Capability and Settings

Table 2-6. Acronym for pull-up and pull-down type

Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-dowm

Table 2-7. Pin multiplexing, capability and settings

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
MSDC0_CLK	0	GPIO174	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_CLK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_CMD	0	GPIO172	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_CMD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT0	0	GPIO175	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT1	0	GPIO176	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT2	0	GPIO177	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT3	0	GPIO178	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT4	0	GPIO179	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT4	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT5	0	GPIO180	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT5	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT6	0	GPIO181	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT6	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DAT7	0	GPIO182	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DAT7	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_RSTB	0	GPIO183	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_RSTB	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC0_DSL	0	GPIO173	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC0_DSL	I	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_CLK	0	GPIO167	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_CLK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_TCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	JTCK	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	CONN_MCU_AICE_TCKC	I	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_CMD	0	GPIO166	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_CMD	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_TMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	5	CONN_DSP_JMS	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	JTMS	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	CONN_MCU_AICE_TMSC	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT0	0	GPIO168	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_TDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	JTDI	I	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT1	0	GPIO169	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT1	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TDO	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_TDO	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TDO	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JDO	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	JTDO	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT2	0	GPIO170	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT2	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_MD32_JTAG_TRST	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_NTRST	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	4	TDD_TRSTN	I	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	CONN_DSP_JINTP	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	DM_JTINTP	O	CU, CD	2/4/6/8/10/12/14/16mA	0
MSDC1_DAT3	0	GPIO171	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	MSDC1_DAT3	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	3	C2K_RTCK	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	6	TDD_TXD	O	CU, CD	2/4/6/8/10/12/14/16mA	0
SIM1_SCLK	0	GPIO18	IO	CU, CD	4/8/12/16mA	0
	1	MD1_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	2	MD2_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	3	MD1_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
	4	MD2_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
SIM1_SRST	0	GPIO164	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM1_SRST	O	CU, CD	4/8/12/16mA	0
	2	MD_SIM2_SRST	O	CU, CD	4/8/12/16mA	0
	3	UIM1_RST	O	CU, CD	4/8/12/16mA	0
	4	UIM0_RST	O	CU, CD	4/8/12/16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
SIM1_SIO	0	GPIO165	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM1_SDAT	IO	CU, CD	4/8/12/16mA	0
	2	MD_SIM2_SDAT	IO	CU, CD	4/8/12/16mA	0
	3	UIM1_IO	IO	CU, CD	4/8/12/16mA	0
	4	UIM0_IO	IO	CU, CD	4/8/12/16mA	0
SIM2_SCLK	0	GPIO160	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM2_SCLK	O	CU, CD	4/8/12/16mA	0
	2	MD_SIM1_SCLK	O	CU, CD	4/8/12/16mA	0
	3	UIM0_CLK	O	CU, CD	4/8/12/16mA	0
	4	UIM1_CLK	O	CU, CD	4/8/12/16mA	0
SIM2_SRST	0	GPIO161	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM2_SRST	O	CU, CD	4/8/12/16mA	0
	2	MD_SIM1_SRST	O	CU, CD	4/8/12/16mA	0
	3	UIM0_RST	O	CU, CD	4/8/12/16mA	0
	4	UIM1_RST	O	CU, CD	4/8/12/16mA	0
SIM2_SIO	0	GPIO162	IO	CU, CD	4/8/12/16mA	0
	1	MD_SIM2_SDAT	IO	CU, CD	4/8/12/16mA	0
	2	MD_SIM1_SDAT	IO	CU, CD	4/8/12/16mA	0
	3	UIM0_IO	IO	CU, CD	4/8/12/16mA	0
	4	UIM1_IO	IO	CU, CD	4/8/12/16mA	0
AUD_CLK_MOSI	0	GPIO143	IO	CU, CD	2/4/6/8mA	0
	1	AUD_CLK_MOSI	O	CU, CD	2/4/6/8mA	0
AUD_DAT_MISO	0	GPIO144	IO	CU, CD	2/4/6/8mA	0
	1	AUD_DAT_MISO	I	CU, CD	2/4/6/8mA	0
	3	AUD_DAT_MOSI	O	CU, CD	2/4/6/8mA	0
AUD_DAT_MOSI	0	GPIO145	IO	CU, CD	2/4/6/8mA	0
	1	AUD_DAT_MOSI	O	CU, CD	2/4/6/8mA	0
	3	AUD_DAT_MISO	I	CU, CD	2/4/6/8mA	0
DISP_PWM	0	GPIO69	IO	CU, CD	2/4/6/8mA	0
	1	DISP_PWM	O	CU, CD	2/4/6/8mA	0
	2	PWM1	O	CU, CD	2/4/6/8mA	0
	3	LTE_MD32_JTAG_TRST	I	CU, CD	2/4/6/8mA	0
	4	TDD_TRSTN	I	CU, CD	2/4/6/8mA	0
	5	ANT_SEL7	O	CU, CD	2/4/6/8mA	0
	6	DM_JTINTP	O	CU, CD	2/4/6/8mA	0
LCM_RST	0	GPIO146	IO	CU, CD	2/4/6/8mA	0
	1	LCM_RST	O	CU, CD	2/4/6/8mA	0
DSI_TE	0	GPIO147	IO	CU, CD	2/4/6/8mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	1	DSI_TE	I	CU, CD	2/4/6/8mA	0
CMDAT0	0	GPIO42	IO	CU, CD	2/4/6/8mA	0
	1	CMDAT0	I	CU, CD	2/4/6/8mA	0
	2	CMCSD0	I	CU, CD	2/4/6/8mA	0
	3	CMMCLK1	O	CU, CD	2/4/6/8mA	0
	6	ANT_SEL5	O	CU, CD	2/4/6/8mA	0
	7	CLKM5	O	CU, CD	2/4/6/8mA	0
CMDAT1	0	GPIO43	IO	CU, CD	2/4/6/8mA	0
	1	CMDAT1	I	CU, CD	2/4/6/8mA	0
	2	CMCSD1	I	CU, CD	2/4/6/8mA	0
	3	CMFLASH	O	CU, CD	2/4/6/8mA	0
	4	MD_EINT0	I	CU, CD	2/4/6/8mA	0
	5	CMMCLK1	O	CU, CD	2/4/6/8mA	0
	6	CLKM4	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A10	IO	CU, CD	2/4/6/8mA	0
CMPCLK	0	GPIO44	IO	CU, CD	2/4/6/8mA	0
	1	CMPCLK	I	CU, CD	2/4/6/8mA	0
	2	CMCSK	I	CU, CD	2/4/6/8mA	0
	3	CMCSD2	I	CU, CD	2/4/6/8mA	0
	4	KCOL3	IO	CU, CD	2/4/6/8mA	0
	5	SRCLKENAI2	I	CU, CD	2/4/6/8mA	0
	6	PWM0	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A11	IO	CU, CD	2/4/6/8mA	0
CMMCLK	0	GPIO45	IO	CU, CD	2/4/6/8mA	0
	1	CMMCLK0	O	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A12	IO	CU, CD	2/4/6/8mA	0
CMMCLK1	0	GPIO46	IO	CU, CD	2/4/6/8mA	0
	1	CMMCLK1	O	CU, CD	2/4/6/8mA	0
	2	IDDIG	I	CU, CD	2/4/6/8mA	0
	3	LTE_MD32_JTAG_TRST	I	CU, CD	2/4/6/8mA	0
	4	TDD_TRSTN	I	CU, CD	2/4/6/8mA	0
	5	DM_JTINTP	O	CU, CD	2/4/6/8mA	0
	6	KCOL6	IO	CU, CD	2/4/6/8mA	0
	7	DBG_MON_A13	IO	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_CK	0	GPIO141	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPICK_I	O	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_CSN	0	GPIO142	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPICS_B_I	O	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_	0	GPIO138	IO	CU, CD	2/4/6/8mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
MI						
	1	PWRAP_SPIDO	IO	CU, CD	2/4/6/8mA	0
	2	PWRAP_SPIDI	IO	CU, CD	2/4/6/8mA	0
PWRAP_SPI0_MO	0	GPIO139	IO	CU, CD	2/4/6/8mA	0
	1	PWRAP_SPIDI	IO	CU, CD	2/4/6/8mA	0
	2	PWRAP_SPIDO	IO	CU, CD	2/4/6/8mA	0
WATCHDOG	0	GPIO149	IO	CU, CD	2/4/6/8mA	0
	1	WATCHDOG	O	CU, CD	2/4/6/8mA	0
SRCLKENA0	0	GPIO148	IO	CU, CD	2/4/6/8mA	0
	1	SRCLKENA0	O	CU, CD	2/4/6/8mA	0
SRCLKENA1	0	GPIO56	IO	CU, CD	2/4/6/8mA	0
	1	SRCLKENA1	O	CU, CD	2/4/6/8mA	0
SCL0	0	GPIO48	IO	CD		0
	1	SCL0_0	IO	CD		0
SCL1	0	GPIO50	IO	CD		0
	1	SCL1_0	IO	CD		0
SCL2	0	GPIO52	IO	CD		0
	1	SCL2_0	IO	CD		0
SCL3	0	GPIO54	IO	CD		0
	1	SCL3_0	IO	CD		0
	3	IDDIG	I	CD		0
SDA0	0	GPIO47	IO	CD		0
	1	SDA0_0	IO	CD		0
SDA1	0	GPIO49	IO	CD		0
	1	SDA1_0	IO	CD		0
SDA2	0	GPIO51	IO	CD		0
	1	SDA2_0	IO	CD		0
SDA3	0	GPIO53	IO	CD		0
	1	SDA3_0	IO	CD		0
	3	IDDIG	I	CD		0
RFIC0_BSI_EN	0	GPIO110	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_EN	O	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_EN	O	CU, CD	2/4/6/8mA	0
RFIC0_BSI_CK	0	GPIO111	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_CK	O	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_CLK	O	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D0	0	GPIO112	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D0	IO	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_D2	IO	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D1	0	GPIO113	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D1	IO	CU, CD	2/4/6/8mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	4	SPM_BSI_D1	IO	CU, CD	2/4/6/8mA	0
RFIC0_BSI_D2	0	GPIO114	IO	CU, CD	2/4/6/8mA	0
	1	RFIC0_BSI_D2	IO	CU, CD	2/4/6/8mA	0
	4	SPM_BSI_D0	IO	CU, CD	2/4/6/8mA	0
RFIC1_BSI_EN	0	GPIO104	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_EN	O	CU, CD	2/4/6/8mA	0
	5	C2K_RX_BSI_EN	O	CU, CD	2/4/6/8mA	0
RFIC1_BSI_CK	0	GPIO105	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_CK	O	CU, CD	2/4/6/8mA	0
	2	PCM1_SYNC	IO	CU, CD	2/4/6/8mA	0
	5	C2K_RX_BSI_CLK	O	CU, CD	2/4/6/8mA	0
RFIC1_BSI_D0	0	GPIO106	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D0	IO	CU, CD	2/4/6/8mA	0
	5	C2K_RX_BSI_DATA	IO	CU, CD	2/4/6/8mA	0
RFIC1_TX_BSI_EN	0	GPIO107	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D1	IO	CU, CD	2/4/6/8mA	0
	5	C2K_TX_BSI_EN	O	CU, CD	2/4/6/8mA	0
RFIC1_TX_BSI_CK	0	GPIO108	IO	CU, CD	2/4/6/8mA	0
	1	RFIC1_BSI_D2	IO	CU, CD	2/4/6/8mA	0
	5	C2K_TX_BSI_CLK	O	CU, CD	2/4/6/8mA	0
RFIC1_TX_BSI_D0	0	GPIO109	IO	CU, CD	2/4/6/8mA	0
	5	C2K_TX_BSI_DATA	IO	CU, CD	2/4/6/8mA	0
PAD_RFIC_MIPI1_SCLK	0	GPIO133	IO	CU, CD	2/4/6/8mA	0
	1	MIPI1_SCLK	O	CU, CD	2/4/6/8mA	0
PAD_RFIC_MIPI1_SDATA	0	GPIO134	IO	CU, CD	2/4/6/8mA	0
	1	MIPI1_SDATA	IO	CU, CD	2/4/6/8mA	0
PAD_RFIC_MIPI0_SCLK	0	GPIO135	IO	CU, CD	2/4/6/8mA	0
	1	MIPI0_SCLK	O	CU, CD	2/4/6/8mA	0
PAD_RFIC_MIPI0_SDATAB	0	GPIO136	IO	CU, CD	2/4/6/8mA	0
	1	MIPI0_SDATA	IO	CU, CD	2/4/6/8mA	0
BPI_BUS0	0	GPIO119	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS0	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B28	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS1	0	GPIO120	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS1	O	CU, CD	2/4/6/8/10/12/14/16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	7	DBG_MON_B29	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS2	0	GPIO121	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS2	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B30	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS3	0	GPIO122	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS3	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B31	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS4	0	GPIO123	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS4	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B32	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS5	0	GPIO87	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
	1	BPI_BUS5	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	2	LTE_C2K_BPI_BUS5	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	5	C2K_BPI_BUS5	O	CU, CD	2/4/6/8/10/12/14/16mA	0
	7	DBG_MON_B0	IO	CU, CD	2/4/6/8/10/12/14/16mA	0
BPI_BUS6	0	GPIO88	IO	CU, CD	4/8/12/16mA	0
	1	BPI_BUS6	O	CU, CD	4/8/12/16mA	0
	2	LTE_C2K_BPI_BUS6	O	CU, CD	4/8/12/16mA	0
	3	Reserved	-	CU, CD	4/8/12/16mA	0
	4	Reserved	-	CU, CD	4/8/12/16mA	0
	5	C2K_BPI_BUS6	O	CU, CD	4/8/12/16mA	0
	6	Reserved	-	CU, CD	4/8/12/16mA	0
	7	DBG_MON_B1	IO	CU, CD	4/8/12/16mA	0
BPI_BUS7	0	GPIO89	IO	CU, CD	4/8/12/16mA	0
	1	BPI_BUS7	O	CU, CD	4/8/12/16mA	0
	2	LTE_C2K_BPI_BUS7	O	CU, CD	4/8/12/16mA	0
	3	CLKM0	O	CU, CD	4/8/12/16mA	0
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS7	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B2	IO	CU, CD	4/8/12/16mA	-
BPI_BUS8	-	GPIO9-	IO	CU, CD	4/8/12/16mA	-
	1	BPI_BUS8	O	CU, CD	4/8/12/16mA	-
	2	LTE_C2K_BPI_BUS8	O	CU, CD	4/8/12/16mA	-
	3	CLKM1	O	CU, CD	4/8/12/16mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS8	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B3	IO	CU, CD	4/8/12/16mA	-
BPI_BUS9	-	GPIO91	IO	CU, CD	4/8/12/16mA	-
	1	BPI_BUS9	O	CU, CD	4/8/12/16mA	-

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	2	LTE_C2K_BPI_BUS9	O	CU, CD	2/4/6/8mA	-
	3	CLKM2	O	CU, CD	4/8/12/16mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS9	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B4	IO	CU, CD	4/8/12/16mA	-
BPI_BUS1-	-	GPIO92	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS1-	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS1-	O	CU, CD	2/4/6/8mA	-
	3	CLKM3	O	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS1-	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B5	IO	CU, CD	4/8/12/16mA	-
BPI_BUS11	-	GPIO93	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS11	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS11	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS11	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B6	IO	CU, CD	4/8/12/16mA	-
BPI_BUS12	-	GPIO94	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS12	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS12	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS12	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B7	IO	CU, CD	4/8/12/16mA	-
BPI_BUS13	-	GPIO95	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS13	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS13	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS13	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B8	IO	CU, CD	4/8/12/16mA	-

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
BPI_BUS14	-	GPIO96	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS14	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS14	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS14	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B9	IO	CU, CD	4/8/12/16mA	-
BPI_BUS15	-	GPIO97	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS15	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS15	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS15	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B1-	IO	CU, CD	4/8/12/16mA	-
BPI_BUS16	-	GPIO98	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS16	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS16	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS16	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B11	IO	CU, CD	4/8/12/16mA	-
BPI_BUS17	-	GPIO99	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS17	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS17	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS17	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B12	IO	CU, CD	4/8/12/16mA	-
BPI_BUS18	-	GPIO1--	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS18	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS18	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	5	C2K_BPI_BUS18	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B13	IO	CU, CD	4/8/12/16mA	-
BPI_BUS19	-	GPIO1-1	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS19	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS19	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS19	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B14	IO	CU, CD	4/8/12/16mA	-
BPI_BUS2-	-	GPIO1-2	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS2-	O	CU, CD	2/4/6/8mA	-
	2	LTE_C2K_BPI_BUS2-	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	C2K_BPI_BUS2-	O	CU, CD	4/8/12/16mA	-
	6	Reserved	-	CU, CD	4/8/12/16mA	-
	7	DBG_MON_B15	IO	CU, CD	4/8/12/16mA	-
BPI_BUS21	-	GPIO124	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS21	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	DPI_HSYNC1	O	CU, CD	4/8/12/16mA	-
	6	KCOL2	IO	CU, CD	4/8/12/16mA	-
	7	TDD_TXD	O	CU, CD	4/8/12/16mA	-
BPI_BUS22	-	GPIO125	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS22	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	DPI_VSYNC1	O	CU, CD	4/8/12/16mA	-
	6	KROW2	IO	CU, CD	4/8/12/16mA	-
	7	MD_URXD	I	CU, CD	4/8/12/16mA	-
BPI_BUS23	-	GPIO126	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS23	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	5	DPI_CK1	O	CU, CD	4/8/12/16mA	-
	6	I2S2_MCK	O	CU, CD	4/8/12/16mA	-
	7	MD_UTXD	O	CU, CD	4/8/12/16mA	-
BPI_BUS24	-	GPIO127	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS24	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	CONN_MCU_DBGI_N	I	CU, CD	2/4/6/8mA	-
	4	EXT_FRAME_SYNC	I	CU, CD	4/8/12/16mA	-
	5	DPI_DE1	O	CU, CD	4/8/12/16mA	-
	6	SRCLKENAI1	I	CU, CD	4/8/12/16mA	-
	7	URXD-	I	CU, CD	4/8/12/16mA	-
BPI_BUS25	-	GPIO128	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS25	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	GPS_FRAME_SYNC	O	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	I2S2_DI	I	CU, CD	4/8/12/16mA	-
	6	PTA_RXD	I	CU, CD	4/8/12/16mA	-
	7	UTXD-	O	CU, CD	4/8/12/16mA	-
BPI_BUS26	-	GPIO129	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS26	O	CU, CD	2/4/6/8mA	-
	2	DISP_PWM	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	I2S2_LRCK	O	CU, CD	4/8/12/16mA	-
	6	PTA_TXD	O	CU, CD	4/8/12/16mA	-
	7	LTE_URXD	I	CU, CD	4/8/12/16mA	-
BPI_BUS27	-	GPIO13-	IO	CU, CD	2/4/6/8mA	-
	1	BPI_BUS27	O	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	4/8/12/16mA	-
	5	I2S2_BCK	O	CU, CD	4/8/12/16mA	-
	6	IRTX_OUT	O	CU, CD	4/8/12/16mA	-
	7	LTE_UTXD	O	CU, CD	4/8/12/16mA	-
LTE_TXBPI	-	GPIO118	IO	CU, CD	2/4/6/8mA	-
	1	TXBPI	I	CU, CD	2/4/6/8mA	-
C2K_TXBPI	-	GPIO1-3	IO	CU, CD	2/4/6/8mA	-
	1	C2K_TXBPI	I	CU, CD	2/4/6/8mA	-
WB_CTRL-	-	GPIO13	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	1	WB_CTRL-	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_ARM_EINT-	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A-	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL1	-	GPIO14	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL1	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_ARM_EINT1	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A1	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL2	-	GPIO15	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL2	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_ARM_EINT2	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A2	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL3	-	GPIO16	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL3	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_ARM_EINT3	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A3	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL4	-	GPIO17	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL4	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	3	C2K_DM_EINT-	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	4	WATCHDOG	O	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A4	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
WB_CTRL5	-	GPIO18	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	1	WB_CTRL5	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	2	C2K_DM_EINT1	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
	7	DBG_MON_A5	IO	CU, CD	2/4/6/8/1-/12/14/16mA	-
F2W_DATA	-	GPIO184	IO	CU, CD	2/4/6/8mA	-
	1	F2W_DATA	I	CU, CD	2/4/6/8mA	-
	2	MRG_CLK	O	CU, CD	2/4/6/8mA	-
	3	C2K_DM_EINT2	IO	CU, CD	2/4/6/8mA	-
	4	PCM-_CLK	O	CU, CD	2/4/6/8mA	-
F2W_CLK	-	GPIO185	IO	CU, CD	2/4/6/8mA	-
	1	F2W_CK	I	CU, CD	2/4/6/8mA	-
	2	MRG_DI	I	CU, CD	2/4/6/8mA	-
	3	C2K_DM_EINT3	IO	CU, CD	2/4/6/8mA	-
	4	PCM-_DI	I	CU, CD	2/4/6/8mA	-
WB_SCLK	-	GPIO187	IO	CU, CD	2/4/6/8mA	-
	1	WB_SCLK	O	CU, CD	2/4/6/8mA	-
	2	MRG_DO	O	CU, CD	2/4/6/8mA	-
	4	PCM-_DO	O	CU, CD	2/4/6/8mA	-
WB_SDATA	-	GPIO188	IO	CU, CD	2/4/6/8mA	-
	1	WB_SDATA	IO	CU, CD	2/4/6/8mA	-
	2	MRG_SYNC	O	CU, CD	2/4/6/8mA	-

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	4	PCM-_SYNC	O	CU, CD	2/4/6/8mA	-
WB_SEN	-	GPIO189	IO	CU, CD	2/4/6/8mA	-
	1	WB_SEN	O	CU, CD	2/4/6/8mA	-
	4	UTXD3	O	CU, CD	2/4/6/8mA	-
	5	URXD3	I	CU, CD	2/4/6/8mA	-
WB_RSTB	-	GPIO186	IO	CU, CD	2/4/6/8mA	-
	1	WB_RSTB	O	CU, CD	2/4/6/8mA	-
	4	URXD3	I	CU, CD	2/4/6/8mA	-
	5	UTXD3	O	CU, CD	2/4/6/8mA	-
KPCOL-	-	GPIO84	IO	CU, CD	2/4/6/8mA	-
	1	KCOL-	IO	CU, CD	2/4/6/8mA	-
	2	URTS-	O	CU, CD	2/4/6/8mA	-
	3	CONN_MCU_DBGACK_N	O	CU, CD	2/4/6/8mA	-
	4	SCL2	IO	CU, CD	2/4/6/8mA	-
	5	C2K_TDO	IO	CU, CD	2/4/6/8mA	-
	6	AUXIF_CLK	O	CU, CD	2/4/6/8mA	-
	7	Reserved	-	CU, CD	2/4/6/8mA	-
KPCOL1	-	GPIO85	IO	CU, CD	2/4/6/8mA	-
	1	KCOL1	IO	CU, CD	2/4/6/8mA	-
	2	UCTS-	I	CU, CD	2/4/6/8mA	-
	3	UCTS1	I	CU, CD	2/4/6/8mA	-
	4	SDA2	IO	CU, CD	2/4/6/8mA	-
	5	C2K_TMS	I	CU, CD	2/4/6/8mA	-
	6	AUXIF_ST	O	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A31	IO	CU, CD	2/4/6/8mA	-
KPCOL2	-	GPIO86	IO	CU, CD	2/4/6/8mA	-
	1	KCOL2	IO	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	URTS1	O	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	2/4/6/8mA	-
	5	C2K_RTCK	O	CU, CD	2/4/6/8mA	-
	6	Reserved	-	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A32	IO	CU, CD	2/4/6/8mA	-
KPROW-	-	GPIO81	IO	CU, CD	2/4/6/8mA	-
	1	KROW-	IO	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	CONN_MCU_DBGI_N	I	CU, CD	2/4/6/8mA	-
	4	CORESONIC_SWCK	I	CU, CD	2/4/6/8mA	-
	5	C2K_TCK	I	CU, CD	2/4/6/8mA	-
	6	Reserved	-	CU, CD	2/4/6/8mA	-

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	7	C2K_DM_EINT1	IO	CU, CD	2/4/6/8mA	-
KPROW1	-	GPIO82	IO	CU, CD	2/4/6/8mA	-
	1	KROW1	IO	CU, CD	2/4/6/8mA	-
	2	Reserved	-	CU, CD	2/4/6/8mA	-
	3	CONN_MCU_TRST_B	I	CU, CD	2/4/6/8mA	-
	4	CORESONIC_SWD	IO	CU, CD	2/4/6/8mA	-
	5	C2K_NTRST	I	CU, CD	2/4/6/8mA	-
	6	USB_DRVVBUS	O	CU, CD	2/4/6/8mA	-
	7	C2K_DM_EINT2	IO	CU, CD	2/4/6/8mA	-
KPROW2	-	GPIO83	IO	CU, CD	2/4/6/8mA	-
	1	KROW2	IO	CU, CD	2/4/6/8mA	-
	2	USB_DRVVBUS	O	CU, CD	2/4/6/8mA	-
	3	Reserved	-	CU, CD	2/4/6/8mA	-
	4	Reserved	-	CU, CD	2/4/6/8mA	-
	5	C2K_TDI	I	CU, CD	2/4/6/8mA	-
	6	Reserved	-	CU, CD	2/4/6/8mA	-
	7	C2K_DM_EINT3	IO	CU, CD	2/4/6/8mA	-
SRCLKENAI	-	GPIO55	IO	CU, CD	2/4/6/8mA	-
	1	SRCLKENAI-	I	CU, CD	2/4/6/8mA	-
	2	PWM2	O	CU, CD	2/4/6/8mA	-
	3	CLKM5	O	CU, CD	2/4/6/8mA	-
	4	CORESONIC_SWD	IO	CU, CD	2/4/6/8mA	-
	5	ANT_SEL6	O	CU, CD	2/4/6/8mA	-
	6	KROW5	IO	CU, CD	2/4/6/8mA	-
	7	DISP_PWM	O	CU, CD	2/4/6/8mA	-
SPI_CSB	-	GPIO65	IO	CU, CD	2/4/6/8mA	-
	1	SPI_CSA	O	CU, CD	2/4/6/8mA	-
	2	EXT_FRAME_SYNC	I	CU, CD	2/4/6/8mA	-
	3	I2S3_MCK	O	CU, CD	2/4/6/8mA	-
	4	KROW2	IO	CU, CD	2/4/6/8mA	-
	5	GPS_FRAME_SYNC	O	CU, CD	2/4/6/8mA	-
	6	PTA_RXD	I	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A22	IO	CU, CD	2/4/6/8mA	-
SPI_CLK	-	GPIO66	IO	CU, CD	2/4/6/8mA	-
	1	SPI_CKA	O	CU, CD	2/4/6/8mA	-
	2	USB_DRVVBUS	O	CU, CD	2/4/6/8mA	-
	3	I2S3_BCK	O	CU, CD	2/4/6/8mA	-
	4	KCOL2	IO	CU, CD	2/4/6/8mA	-
	5	Reserved	-	CU, CD	2/4/6/8mA	-
	6	PTA_TXD	O	CU, CD	2/4/6/8mA	-

Name	Aux. function	Aux. name	Aux. type	PU/PD/CU/CD	Driving	SMT
	7	DBG_MON_A23	IO	CU, CD	2/4/6/8mA	-
SPI_MO	-	GPIO68	IO	CU, CD	2/4/6/8mA	-
	1	SPI_MOA	O	CU, CD	2/4/6/8mA	-
	2	SPI_MIA	I	CU, CD	2/4/6/8mA	-
	3	I2S3_LRCK	O	CU, CD	2/4/6/8mA	-
	4	PTA_TXD	O	CU, CD	2/4/6/8mA	-
	5	ANT_SEL4	O	CU, CD	2/4/6/8mA	-
	6	URTS1	O	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A25	IO	CU, CD	2/4/6/8mA	-
SPI_MI	-	GPIO67	IO	CU, CD	2/4/6/8mA	-
	1	SPI_MIA	I	CU, CD	2/4/6/8mA	-
	2	SPI_MOA	O	CU, CD	2/4/6/8mA	-
	3	I2S3_DO	O	CU, CD	2/4/6/8mA	-
	4	PTA_RXD	I	CU, CD	2/4/6/8mA	-
	5	IDDIG	I	CU, CD	2/4/6/8mA	-
	6	UCTS1	I	CU, CD	2/4/6/8mA	-
	7	DBG_MON_A24	IO	CU, CD	2/4/6/8mA	-

2.2 Electrical Characteristic

2.2.1 Absolute Maximum Ratings

Table 2-8. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
AVDD18_PLLGP AVDD18_MEMPLL	Analog power input 1.8V for PLL	1.7	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.9	V
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.94	V
DVDD18_MIPITX	Analog power for MIPI DSI	1.7	1.9	V
DVDD18_MIPIRX0 DVDD18_MIPIRX1	Analog power for MIPI CSI- & CSI1	1.7	1.9	V
AVDD33_USB_P	Analog power 3.3V for USB	3.135	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.7	1.9	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.7	1.9	V
DVDD18_IOLT1 DVDD18_IOLT2 DVDD18_IORB DVDD18_IOBR DVDD18_CONN	Digital power input for 1.8V IO	1.62	1.98	V
DVDD18_MC0	Digital power input for MSDC0	1.62	1.98	V
DVDD18_MC1	Digital power input for MSDC1	1.62	1.98	V
DVDD28_MSDC1	Digital power input for MSDC1	1.7	3.6	V
DVDD28_SIM1	Digital power input for SIM1	1.7	3.3	V
DVDD28_SIM2	Digital power input for SIM2	1.7	3.3	V
DVDD12_EMI	Digital power input for DRAM	1.14	1.3	V
DVDD_DVFS	Digital power input for DVFS	0.95	1.25	V
DVDD_LTE	Digital power input for LTE	0.95	1.15	V
DVDD_SRAM	Digital power input for SRAM	0.95	1.15	V
DVDD_TOP	Digital power input for TOP	0.95	1.25	V

Warning: *Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only.*

2.2.2 Recommended Operating Conditions

Table 2-9. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_PLLGP AVDD18_MEMPLL	Analog power input 1.8V for PLL	1.7	1.8	1.9	V
AVDD18_AP	Analog power input 1.8V for AuxADC, TSENSE	1.7	1.8	1.9	V

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
AVDD18_MD	Analog power input 1.8V for BBTX, BBRX	1.7	1.8	1.9	V
AVDD28_DAC	Analog power input 2.8V for APC	2.66	2.8	2.94	V
DVDD18_MIPITX1	Analog power for MIPI DSI	1.7	1.8	1.9	V
DVDD18_MIPIRX0 DVDD18_MIPIRX1	Analog power for MIPI CSI	1.7	1.8	1.89	V
AVDD33_USB	Analog power 3.3V for USB	3.135	3.3	3.465	V
AVDD18_USB	Analog power 1.8V for USB	1.71	1.8	1.89	V
AVDD18_WBG	Analog power 1.8V for connectivity ABB	1.71	1.8	1.89	V
DVDD18_IOLT1 DVDD18_IOLT2 DVDD18_IORB DVDD18_IOBR DVDD18_CONN	Digital power input for 1.8V IO	1.62	1.8	1.98	V
DVDD18_MC0	Digital power input for MSDC0	1.62	1.8	1.98	V
DVDD18_MC1	Digital power input for MSDC1	1.62	1.8	1.98	V
DVDD28_MC1	Digital power input for MSDC1	1.7	1.8	1.95	V
		2.7	3.3	3.6	
DVDD28_SIM1 DVDD28_SIM2	Digital power input for SIM1/SIM2	2.7	3.0	3.3	V
		1.7	1.8	1.9	
DVDD12_EMI	Digital power input for EMI (LPDDR2/3)	1.14	1.2	1.3	V
DVDD_DVFS	Digital power input for DVFS	0.95	1.15	1.25	V
DVDD_LTE	Digital power input for LTE	0.95	1.05	1.15	V
DVDD_SRAM	Digital power input for SRAM	0.95	1.05	1.15	V
DVDD_TOP	Digital power input for TOP	0.95	1.15	1.25	V

2.2.3 Storage Condition

1. Shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH).
2. After the bag is opened, devices subjected to infrared reflow, vapor-phase reflow or equivalent processing must be:
   - Mounted within 168 hours in factory condition of 30°C/60% RH, or
   - Stored at 20% RH
3. Devices require baking before being mounted, if they are placed
   - For 192 hours at 40°C +5°C/-0°C and < 5% RH in low temperature device containers, or
   - For 24 hours at 125°C +5°C/-0°C in high temperature device containers.

2.2.4 AC Electrical Characteristics and Timing Diagram

2.2.4.1 External Memory Interface for LPDDR3

The external memory interface, shown in Figure 2-4. Basic timing parameter for LPDDR3 commands, Figure 2-5 and Figure 2-6, is used to connect LPDDR3 device for MT8735. It includes pins CLK_T,

CLK_C, CKE[1:0], CS[1:0], DQS[3:0], DQS#[3:0], CA[9:0] and DQ[31:0]. Table 2-10 summarizes the symbol definition and the related timing specifications.

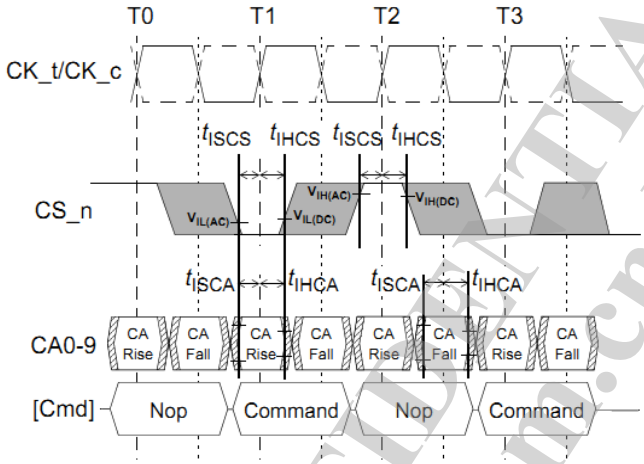


Figure 2-4. Basic timing parameter for LPDDR3 commands

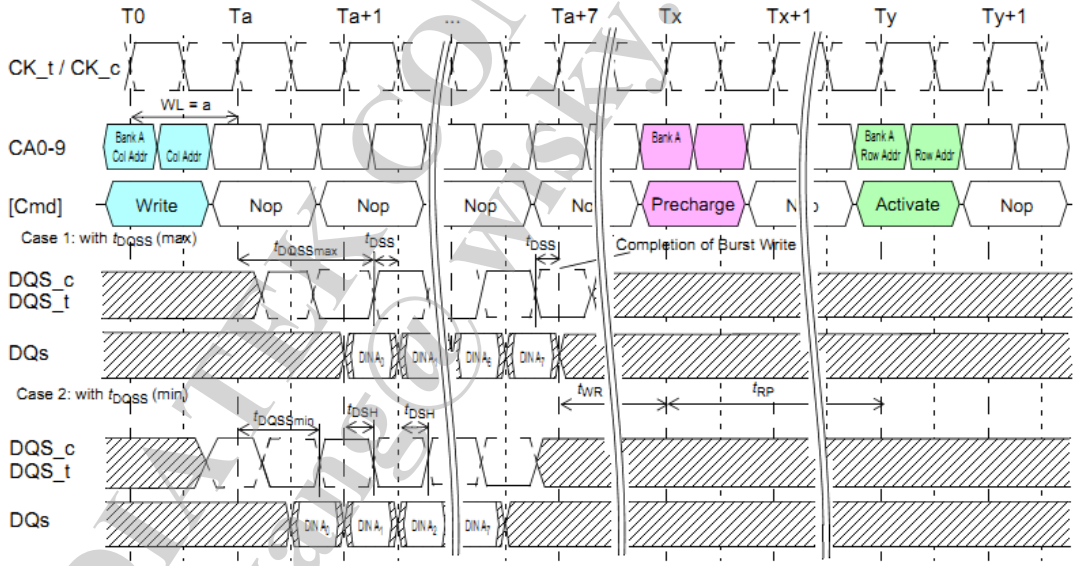


Figure 2-5. Basic timing parameter for LPDDR3 write

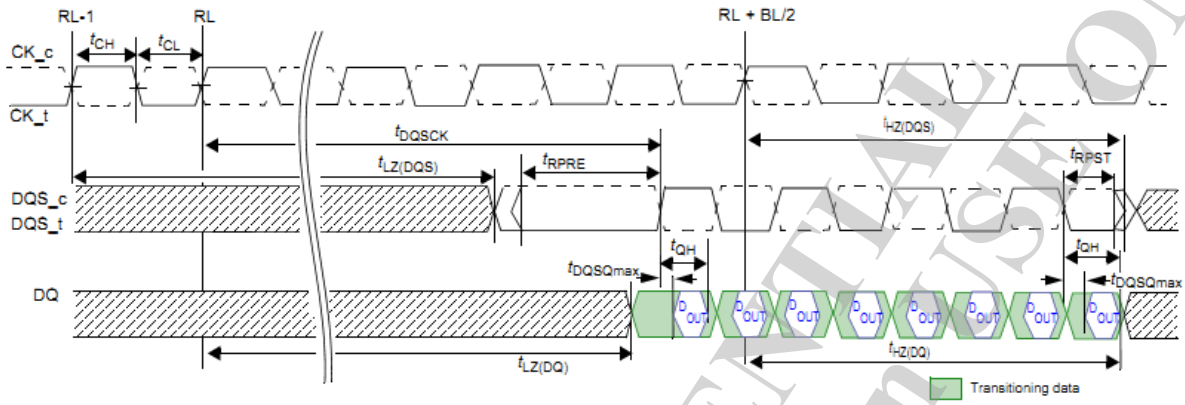


Figure 2-6. Basic LPDDR3 read timing parameter

Table 2-10. LPDDR3 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	1.071		100	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.13			ns
tDH	DQ & DM input hold time	0.13			ns
tDIPW	DQ and DM input pulse width	0.35			tCK
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tWPST	Write postamble	0.4			tCK
tWPRE	Write preamble	0.8			tCK
tISCA	Address & control input setup time	0.13			ns
tIHCA	Address & control input hold time	0.13			ns
tISCS	CS_ input setup time	0.23			ns
tIHCS	CS_ input hold time	0.23			ns
tIPWCA	Address and control input pulse width	0.35			tCK
tIPWCS	CS_ input pulse width	0.7			tCK
tCKE	CKE minimum pulse width (HIGH and LOW pulse width)	Max. (7.5ns, 3tCK)			ns
tISCKE	CKE input setup time	0.25			tCK
tIHCKE	CKE input hold time	0.25			tCK
tCPDED	Command path disable delay	2			tCK
tLZ(DQS)	DQS low-impedance time from CK/CK'	tDQSCK (MIN) - 0.3			ns
tHZ(DQS)	DQS high-impedance time from CK/CK'			tDQSCK (MAX) – 0.1	ns

Symbol	Description	Min.	Typ.	Max.	Unit
tLZ(DQ)	DQ low-impedance time from CK/CK'	tDQSCK (MIN) - 0.3			ns
tHZ(DQ)	DQ high-impedance time from CK/CK'			tDQSCK (MAX) + [1.4*tDQSQ (MAX)]	ns
tDQSQ	DQS-DQ skew			0.115	ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH - 0.05			tCK
tQSL	DQS output low pulse width	tCL - 0.05			tCK
tQH	DQ/DQS output hold time from DQS	Min. (tQSH, tQSL)			ns
tMRW	MODE register Write command period	Max. (10tCK, 15)			ns
tMRR	MODE register Read command period	4			tCK
tMRD	Mode register set command delay	Max. (10tCK, 14)			ns
tRPRE	Read preamble	0.9			tCK
tRPST	Read postamble	0.3			tCK
tRAS	ACTIVE to PRECHARGE command period	Max. (42ns, 3tCK)		70000	ns
tRC	ACTIVE to ACTIVE command period	tRAS + tRPab (with all-bank pre-charge) tRAS + tRPpb (with per-bank pre-charge)			ns
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			ns
tRCD	ACTIVE to READ or WRITE delay	Max. (18ns, 3tCK)			ns
tRPpb	Row PRECHARGE Time (single bank)	Max. (18ns, 3tCK)			ns
tRPab	Row PRECHARGE Time (all banks)	Max. (21ns, 3tCK)			ns
tRRD	ACTIVE bank A to ACTIVE bank B delay	Max. (10ns, 2tCK)			ns
tWR	WRITE recovery time	Max. (15ns, 4tCK)			ns
tWTR	Internal write to READ command time	Max. (7.5ns, 4tCK)			ns
tXSR	SELF REFRESH exit to next valid command	Max. (tRFCab + 10ns, 2tCK)			ns
tXP	EXIT power down to next valid command delay	Max. (7.5ns, 3tCK)			ns
tREFW	Refresh period			32	ms

Symbol	Description	Min.	Typ.	Max.	Unit
tRFCab	Refresh cycle time	130			ns
tRFCpb	Per bank refresh cycle time	60			ns
tRTP	Internal READ to PRECHARGE command delay	Max. (7.5ns, 4tCK)			ns
tCCD	CAS-to-CAS delay	4			tCK

2.2.4.2 External Memory Interface for LPDDR2

The external memory interface, shown in Figure 2-4. Basic timing parameter for LPDDR3 commands, Figure 2-59 and Figure 2-610, is used to connect LPDDR2 device for MT8735. It includes pins ED_CLK, ED_CLK_B, ECKE, ECS#, EBA[2:0], EDQS[3:0], EDQS#[3:0], EA[9:0] and ED[31:0]. Table 2-10 summarizes the symbol definition and the related timing specifications.

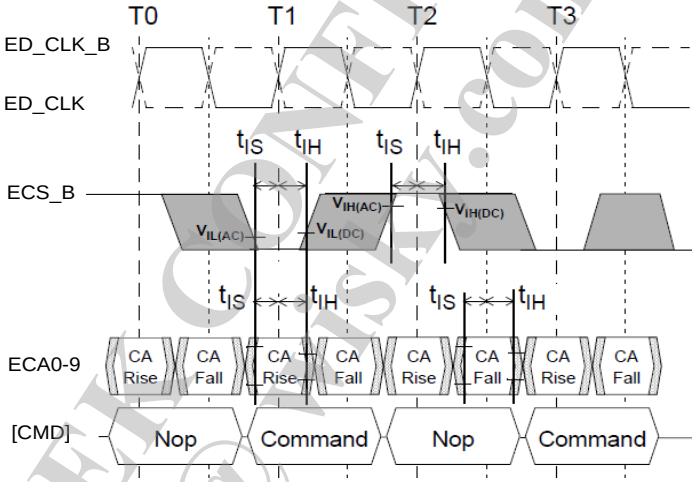


Figure 2-7. Basic timing parameter for LPDDR2 commands

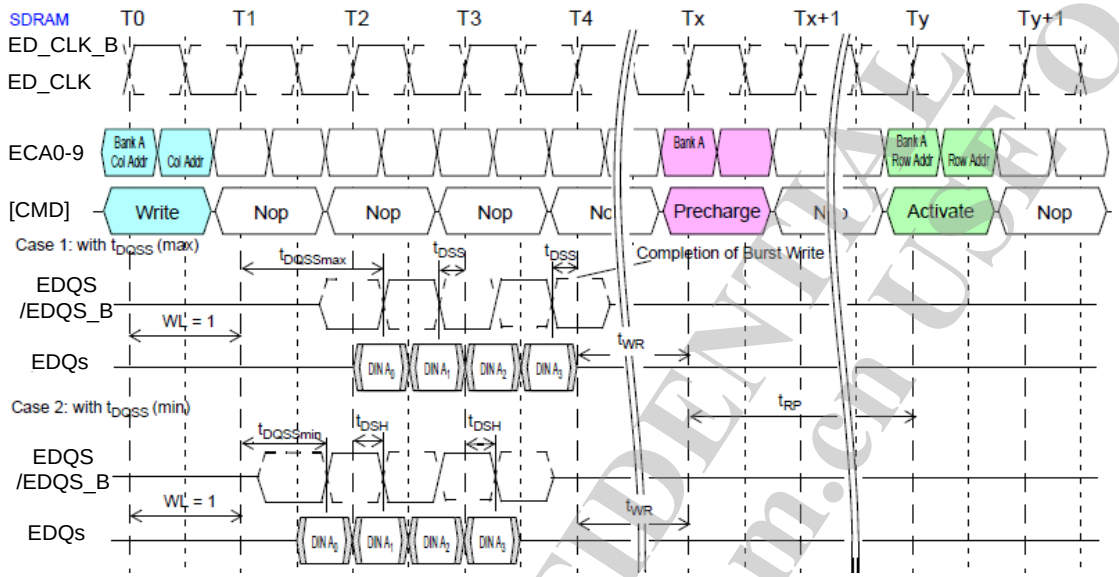


Figure 2-8. Basic timing parameter for LPDDR2 write

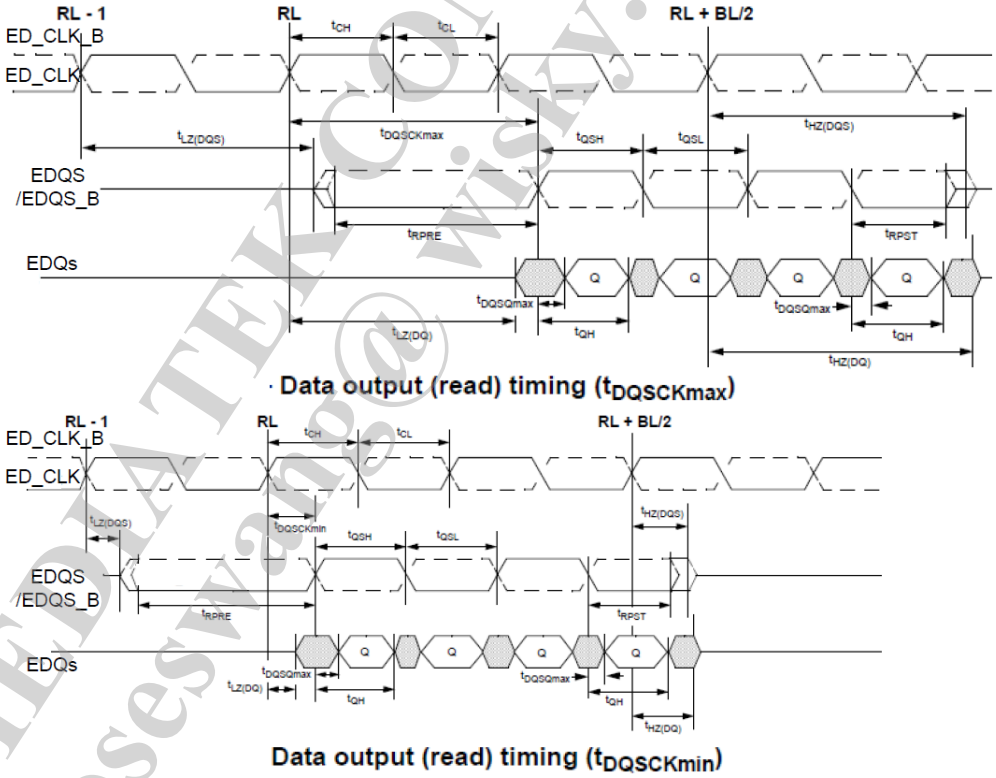


Figure 2-9. Basic timing parameter for LPDDR2 read

Table 2-11. LPDDR2 AC timing parameter table of external memory interface

Symbol	Description	Min.	Typ.	Max.	Unit
tCK	Clock cycle time	3.75		8	ns
tDQSCK	DQS output access time from CK/CK'	2.5		5.5	ns
tCH	Clock high level width	0.45		0.55	tCK
tCL	Clock low level width	0.45		0.55	tCK
tHP	Clock half period	0.45		0.55	tCK
tDS	DQ & DM input setup time	0.43			ns
tDH	DQ & DM input hold time	0.43			ns
tDQSS	Write command to 1st DQS latching transition	0.75		1.25	tCK
tDSS	DQS falling edge to CK setup time	0.2			tCK
tDSH	DQS falling edge hold time from CK	0.2			tCK
tIS	Address & control input setup time	0.46			ns
tIH	Address & control input hold time	0.46			ns
tLZ(DQS)	DQS low-impedance time from CK/CK'	tDQSCK (Min.) – 300			ns
tHZ(DQS)	DQS high-impedance time from CK/CK'	tDQSCK (Max.) – 100			ns
tLZ(DQ)	DQ low-impedance time from CK/CK'	tDQSCK (Min.) – [1.4*tQHS (Max.)]			ns
tHZ(DQ)	DQ high-impedance time from CK/CK'	tDQSCK (Max.) + [1.4*tDQSQ (Max.)]			ns
tDQSQ	DQS-DQ skew	0.34			ns
tQHP	Data half period	Min. (tQSH, tQSL)			tCK
tQHS	Data hold skew factor	0.4			ns
tQH	DQ/DQS output hold time from DQS	tQHP – tQHS			ns
tDQSH	DQS input high-level width	0.4			tCK
tDQSL	DQS input low-level width	0.4			tCK
tQSH	DQS output high pulse width	tCH – 0.05			tCK
tQSL	DQS output low pulse width	tCL – 0.05			tCK
tMRW	MODE register Write command period	5			tCK
tMRR	MODE register Read command period	2			tCK
tRPRE	Read preamble	0.9		1.1	tCK
tRPST	Read postamble	tCL – 0.05			tCK
tRAS	ACTIVE to PRECHARGE command period	3			tCK
tRC	ACTIVE to ACTIVE command period	6			tCK
tRFC	AUTO REFRESH to ACTIVE/AUTO REFRESH command period	56			tCK
tRCD	ACTIVE to READ or WRITE delay	3			tCK
tRP	PRECHARGE command period	3			tCK
tRRD	ACTIVE bank A to ACTIVE bank B delay	2			tCK
tWR	WRITE recovery time	3			tCK
tWTR	Internal write to READ command time	2			tCK
tXSR	SELF REFRESH exit to the next valid command	40			tCK

Symbol	Description	Min.	Typ.	Max.	Unit
tXP	EXIT power-down to the next valid command delay	2			tCK
tCKE	CKE min. pulse width (high & low pulse width)	2			tCK

2.3 System Configuration

2.3.1 Mode Selection

Table 2-12. Mode selection

Pin name	Description
KCOL0	0: Force USB download mode in bootrom 1: NA (default)

2.3.2 Constant Tie Pins

Table 2-13. Constant tied pins

Pin name	Description
TESTMODE	Test mode (tied to GND)

2.4 Power-on Sequence

The power-on/off sequence with XTAL is shown in the following figure:

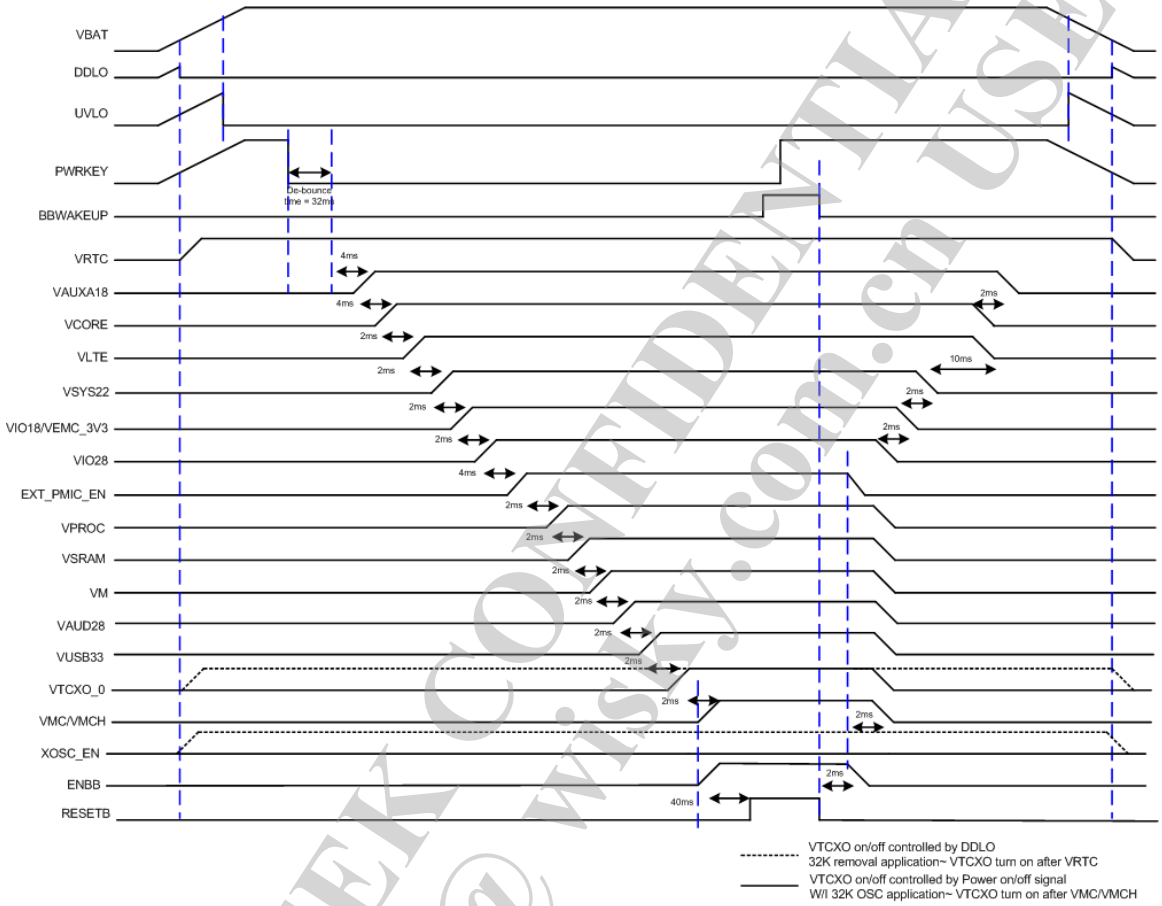


Figure 2-10. Power on/off Sequence by pressing PWRKEY

2.5 Analog Baseband

2.5.1 Introduction

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. In the write or read of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS/WCDMA/LTE/C2K base-band signal processing:

- Base-band Rx: For I/Q channels base-band A/D conversion
- Base-band Tx: For I/Q channels base-band D/A conversion and smoothing filtering
- ETDAC: A DAC output to control buck-converter for envelop tracking technique.
- RF control: Two DACs for automatic power control (APC) is included.The outputs are provided to external RF power amplifiers respectively.
- Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring.
- Clock generation: One clock-squarer for shaping the input sinwave clock and 20 PLLs providing clock signals to base-band TRx, DSP, MCU, USB, MSDC units.

2.5.2 Features

The analog blocks include the following analog functions for complete GSM/GPRS/WCDMA/LTE/C2K base-band signal processing:

- LTE_BBRX
- C2K_BBRX
- LTE_BBTX
- C2K_BBTX
- ETDAC
- APC-DAC
- AUXADC
- Phase locked loop
- Temperature sensor

2.5.3 Block Diagram

2.5.3.1 LTE_BBRX

2.5.3.1.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 4 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

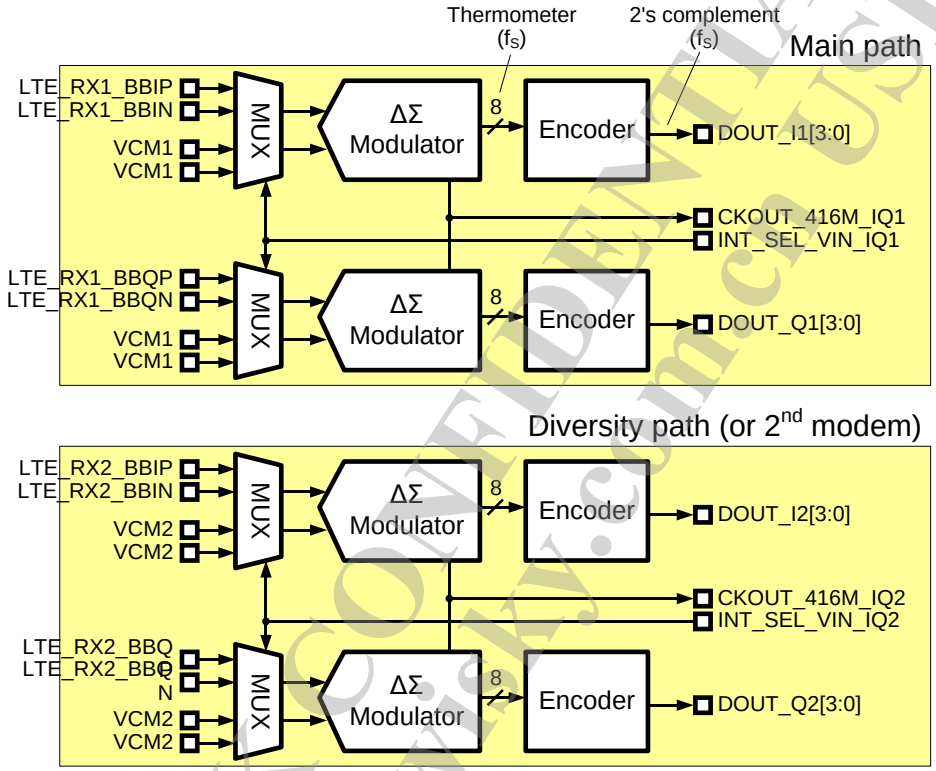


Figure 2-11. Block diagram of LTE_BBRX-ADC

2.5.3.1.2 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-14. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.7	0.75	V
FC	Input clock frequency – Clock rate (LTE HB mode) – Clock rate (LTE LB mode) – Clock rate (DC mode) – Clock rate (SC mode & GSM mode)		 416 208 416 208		MHz
	Input clock duty cycle	49.5	50	50.5	%

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input clock period jitter, DC mode			0.14	% (rms)
	Input clock period jitter, SC mode & GSM mode			0.61	% (rms)
RIN	Differential input resistance – LTE HB mode – LTE LB mode – DC mode – SC mode & GSM mode	 2.8 5.6 5.6 11.2	 4 8 8 16	 5.2 10.4 10.4 20.8	kΩ
FS	Output sampling rate		416/208		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – LTE HB mode, 2.4Vpp (10.2MHz) sinewave, 1kHz ~ 9MHz band – LTE LB mode, 2.4Vpp (5.2MHz) sinewave, 1kHz ~ 4.5MHz band – DC mode, 2.4Vpp (5.2MHz) sinewave, 400kHz ~ 4.6MHz band – SC mode, 2.4Vpp (2.7MHz) sinewave, 1kHz ~ 2.1MHz band – GSM mode: 2.4Vpp(570kHz) sinewave, 70kHz ~ 270kHz band	 70 70 72 72 83	 73 73 75 75 86		 dB dB dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	–20		80	°C
	Current consumption (per channel, 1 ADC) – Power-up – Power-down			 4.5 1	 mA uA

2.5.3.2 C2K_BBRX

2.5.3.2.1 Block Descriptions

The receiver (Rx) performs baseband I/Q channels downlink analog-to-digital conversion:

1. Analog input multiplexer: For each channel, a 2-input multiplexer is included.
2. A/D converter: 4 high performance sigma-delta ADCs perform I/Q digitization for further digital signal processing.

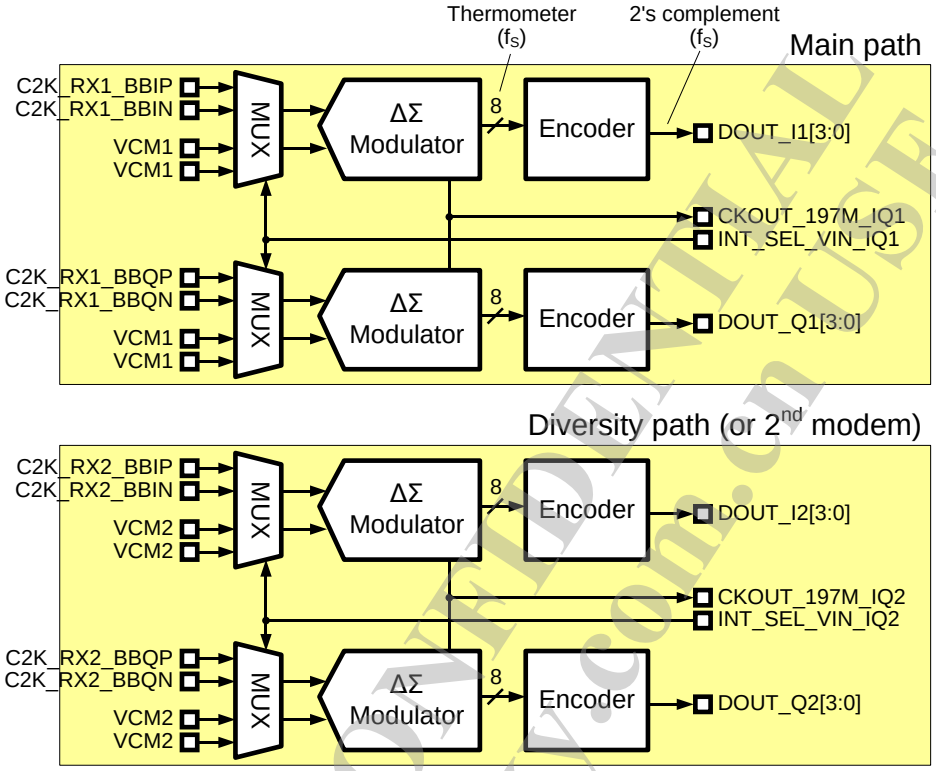


Figure 2-12. Block diagram of C2K_BBRX-ADC

2.5.3.3 Functional Specifications

See the table below for the functional specifications of the base-band downlink receiver.

Table 2-15. Baseband downlink specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Differential analog input voltage (peak-to-peak)			2.4	V
ICM	Common mode input current magnitude			1	uA
VCM	Common mode input voltage	0.65	0.70	0.75	V
FC	Clock rate		196.608		MHz
	Input clock duty cycle	49.5	50	50.5	%
	Input clock period jitter			0.61	% (rms)
RIN	Differential input resistance	11.2	16	20.8	kΩ
FS	Output sampling rate		196.608		MSPS
VOS	Differential input referred offset			10	mV
SIN	Signal to in-band noise – 2.4Vpp (1.6MHz) sinewave, 1kKHz ~ 640kHz band	79	82		dB
DVDD18	Digital power supply	1.7	1.8	1.9	V
AVDD18	Analog power supply	1.7	1.8	1.9	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	–20		80	°C
	Current consumption (per channel, 1 ADC) – Power-up – Power-down			 2 1	 mA uA

2.5.3.4 LTE_BBTX

2.5.3.4.1 Block Descriptions

BBTX includes two channel DACs with the 1st order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current and the active RC filter performs current to voltage buffer.

The bitwidth of DACs is 11-bit which is encoded into 7 bits of thermometer code and 8 binary code by digital hard macro inside BBTX layout. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. The MD-PLL delivers 832MHz differential clock to BBTX. A clock divider translates the 832MHz to 416MHz for DACs and AFIFO inside mixedsys.

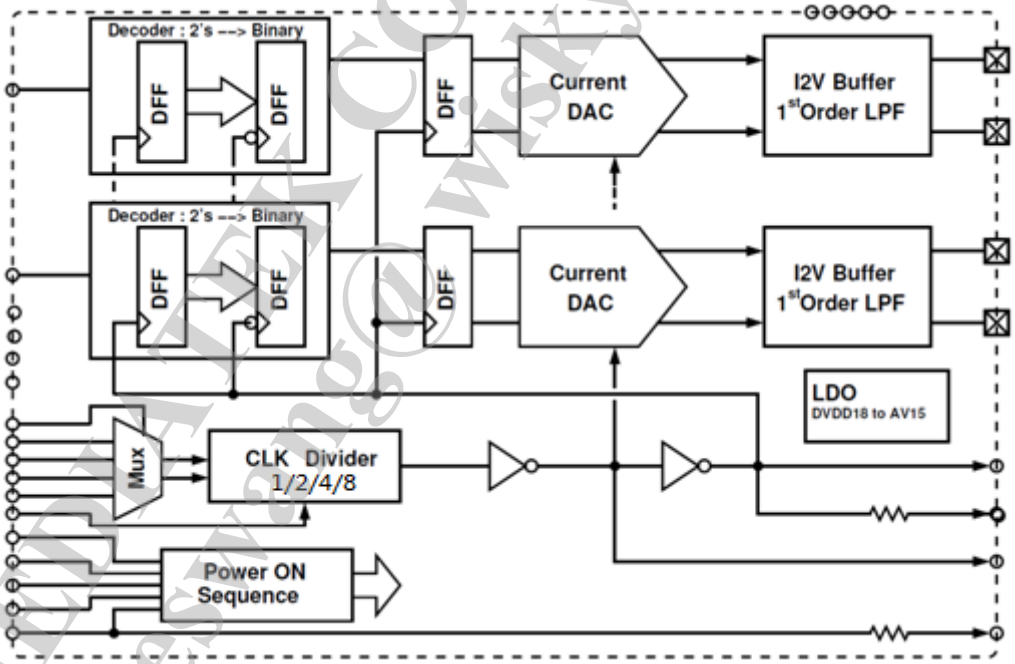


Figure 2-13. Block diagram of LTE_BBTX

2.5.3.4.2 Functional Specifications

Table 2-16. LTE_BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF leakage current @ supply, Irms @416*2 = 832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		11.0		bit
F_s	Sampling clock		416		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os}	3-sigma output differential DC offset			20	mV
F_{3dB}	3dB corner freq.		20/40		MHz
N_{OOB}	Output noise level @25MHz		40		nVrms/sqrt(Hz)
Dinb	Inband Droop		0.1		dB
DNL			1		LSB
INL			2		LSB
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-58	-55	dBc
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 6.5 10		 mA uA

2.5.3.5 C2K_BBTX

2.5.3.5.1 Block Descriptions

BBTX includes two channels of DACs with the first order low pass filter. The DACs are PMOS current-steering topology with NMOS constant sinking current, and the active RC filter performs current to the voltage buffer.

The bitwidth of DACs is 10-bit which is encoded into 7 bits of thermometer code and 7 binary code by mixedsys hardware. The encoded bits are timing synchronized by D-type flip-flop which is toggled by the analog local clock. MD-PLL2 deliver 393.216MHz differential clock to BBTX. A clock divider buffered the 393.216MHz to AFIFO inside the mixedsys.

The IO power, DVDD18_MD, is regulated to a voltage around 1.55V to supply analog component, and the required bias currents are generated by BBRX.

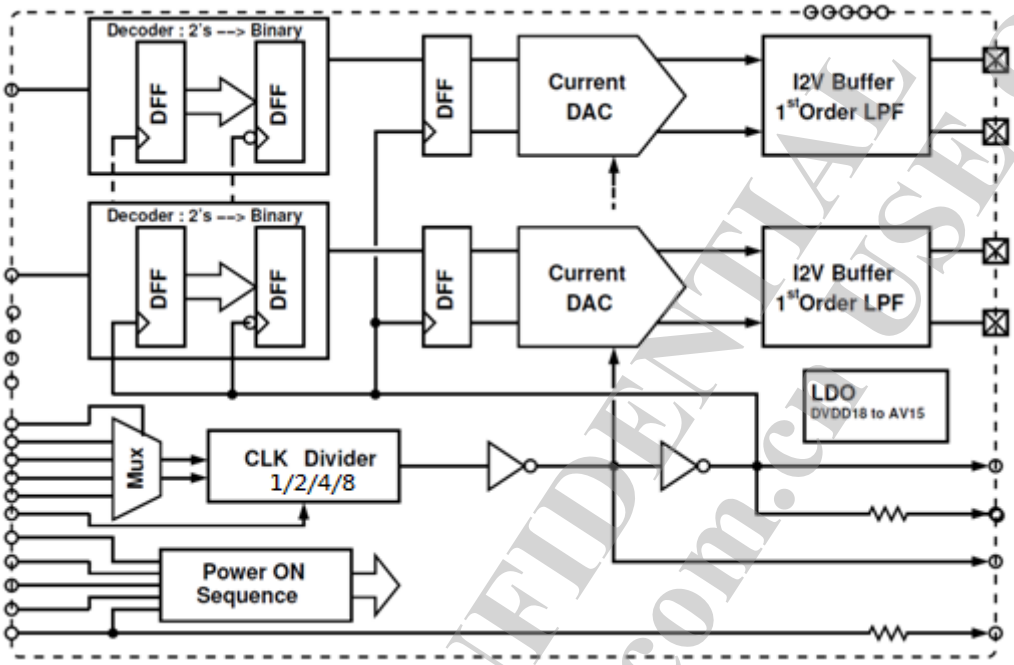


Figure 2-14. Block diagram of C2K_BBTX

2.5.3.5.2 Functional Specifications

Table 2-17. C2K_BBTX specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit.
V_{ocm}	DC output common mode voltage	0.615	0.65	0.685	V
I_K	HF Leakage current @ supply, Irms @416*2=832MHz			3.5	uA
V_{fs}	DAC output swing		2100		mV
N	DAC resolution		10.0		bit
F_s	Sampling clock		393.216		MHz
I_{mis}	1-sgma DAC unit cell mismatch			1	%
G_{mis}	3-sigma I/Q gain mismatch	-0.2		0.2	dB
V_{os_T}	3-sigma output differential DC offset over temp.			4	mV
V_{os}	3-sigma output differential DC offset			10	mV
F_{3dB}	3dB corner freq.	20	25	30	MHz
S_{LPF}	LPF selectivity @832MHz	28			dB
N_{OOB}	Output noise level @45MHz		15.1	30.1.	nVrms/sqrt(Hz)
CN	Signal to noise ratio@45MHz		-146	-140	dBc/Hz
IM3	In-band two-tone test swing V1=V2=290/sqrt(2) mV		-60	-56	dBc
T	Operating temperature	-20		80	°C

Symbol	Parameter	Min.	Typ.	Max.	Unit.
	Current consumption				
	Power-up		6.5		mA
	Power-down		10		uA

2.5.3.6 ETDAC

2.5.3.6.1 Block Descriptions

The ETDAC (Envelope Tracking DAC) provides analog envelope signal to external ET modulator. It includes:

1. 11-bit D/A converter: Converts digital modulated signals to analog domain. The input to the DAC is sampled at 416MHz rate with the 11-bit resolution.
2. Smoothing filter: The low-pass filter performs smoothing function for DAC output signals with a 20/40MHz 1st-order Butterworth frequency response.

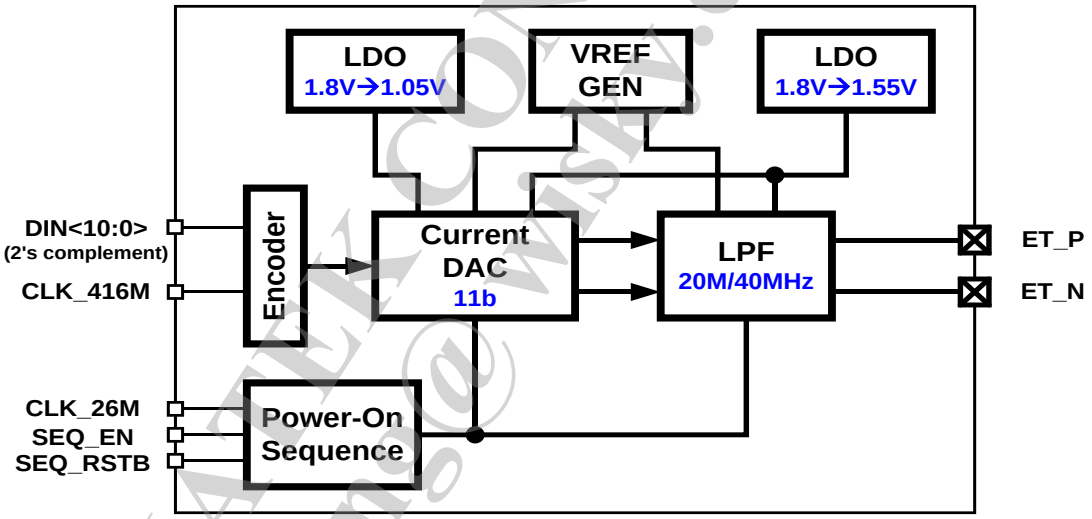


Figure 2-15. Block diagram of ETDAC

2.5.3.6.2 Functional Specfications

Table 2-18. ETDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		11		Bit
FS	Sampling rate		416		MSPS
IM3	3rd order Intermodulation distortion		-60	-50	dB
	Output swing (full swing)		2		Vppd
VOCM	Output CM voltage	0.6		0.85	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output capacitance (single-ended)			10	PF
	Output resistance (differential)		100		KΩ
DNL	Differential nonlinearity	-1		+1	LSB
INL	Integral nonlinearity	-2		+2	LSB
FCUT	Filter -3dB cutoff frequency (calibrated)		20/40		MHz
DVDD	Digital power supply	0.95	1.05	1.15	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption – Power-up – Power-down		 4.5 10		 mA uA

2.5.3.7 APC-DAC

2.5.3.7.1 Block Descriptions

See the figure below. APC-DAC is designed to produce a single-ended output signal at APC pin. Two APC-DACs provide two separate output signals (APC1 and APC2).

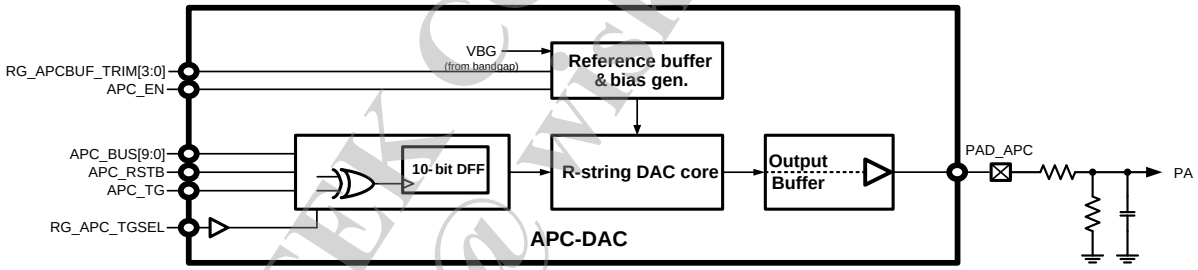


Figure 2-16. Block diagram of APC-DAC (same architecture for two APC-DACs)

2.5.3.7.2 Functional Specifications

See the table below for the functional specifications of the APC-DAC (apply to both APC-DACs).

Table 2-19. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
Fs	Clock rate	1.0833		2.1666	MS/s
SNDR	Signal-to-noise-and-distortion ratio (10kHz sine wave with 1.0V swing)		50		dB
Ts	Settling time (99% full-swing settling)			5	us
$V_{O,max}$	Maximum output			AVDD –	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
				0.2	
C_L	Output loading capacitance		220	2200	pF
DNL	Differential nonlinearity (code 30 ~ 970)		±1.0		LSB
INL	Integral nonlinearity (code 30 ~ 970)		±2.0		LSB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	–20		85	°C
I_{ON}	Current consumption (power-on state)		450		uA
I_{OFF}	Current consumption (power-down state)			20	uA

2.5.3.8 AUXADC

2.5.3.8.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the auxiliary input channels. There are 16 input channels of AUXADC. Some are for internal voltage measurement and some for external voltage measurement. Environmental messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

See Table 2-20 for brief descriptions of AUXADC input channels.

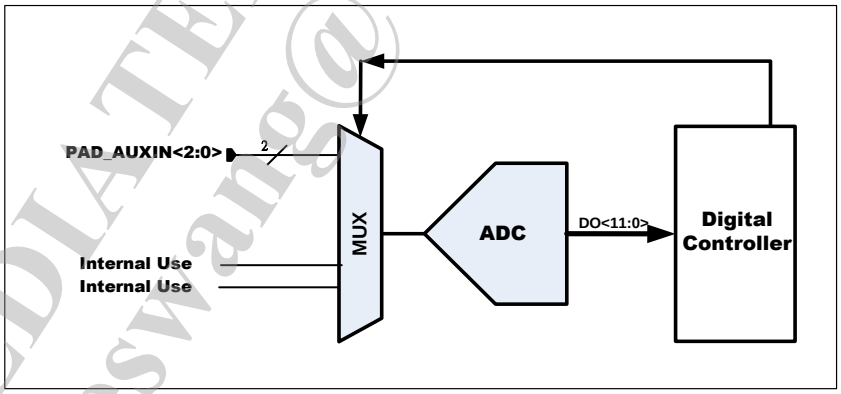


Figure 2-17. Block diagram of AUXADC

Table 2-20. Definitions of AUXADC channels

AUXADC channel ID	Description
Channel 0	External use (AUX_IN0)

AUXADC channel ID	Description
Channel 1	External use (AUX_IN1)
Channel 2	NA
Channel 3	NA
Channel 4	NA
Channel 5	NA
Channel 6	NA
Channel 7	NA
Channel 8	NA
Channel 9	NA
Channel 10	Internal use
Channel 11	Internal use
Channel 12	External use (AUX_IN2)
Channel 13	NA
Channel 14	NA
Channel 15	NA

2.5.3.8.2 Functional Specifications

See the table below for the functional specifications of auxiliary ADC.

Table 2-21. AUXADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		12		Bit
FC	Clock rate		3.25		MHz
FS	Sampling rate @ N-Bit		3.25/(N+8)		MSPS
	Input swing	0.05		1.45	V
CIN	Input capacitance Unselected channel Selected channel		 50 4		 fF pF
RIN	Input resistance Unselected channel	 20			 MΩ
	Clock latency		N+8		1/FC
DNL	Differential nonlinearity		+1.0/-1.0		LSB
INL	Integral nonlinearity		+2.0/-2.0		LSB
SINAD	Signal to noise and distortion ratio (1kHz full swing input & 1.0833MHz clock rate)	56	64		dB
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption - Power-up - Power-down		 600 1		 uA uA

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Accuracy- before trim			+-75	mV
	Accuracy- after trim			+-10	mV

2.5.3.9 Clock Squarer

2.5.3.9.1 Block Descriptions

For most VCXO, the output clock waveform is sinusoidal with too small amplitude (about several hundred mV) to make digital circuits function well. The clock squarer is designed to convert such a small signal to a rail-to-rail clock signal with excellent duty-cycle.

2.5.3.9.2 Functional Specifications

See the table below for the functional specifications of clock squarer.

Table 2-22. Clock squarer specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	13	26		MHz
Fout	Output clock frequency	13	26		MHz
Vin	Input signal amplitude	350	500	1,000	mVpp
DcycIN	Input signal duty cycle		50		%
DcycOUT	Output signal duty cycle	DcycIN-5		DcycIN+5	%
TR	Rise time on pin CLKSQOUT			5	ns/pF
TF	Fall time on pin CLKSQOUT			5	ns/pF
DVDD	Digital power supply	0.81	1.0	1.1	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		500		uA

2.5.3.10 Phase Locked Loop

2.5.3.10.1 Block Descriptions

There are total 17 PLLs in PLL macro separated into 2 groups, providing several clocks for CPU, BUS, modem, analog modem, MSDC and image-sensor.

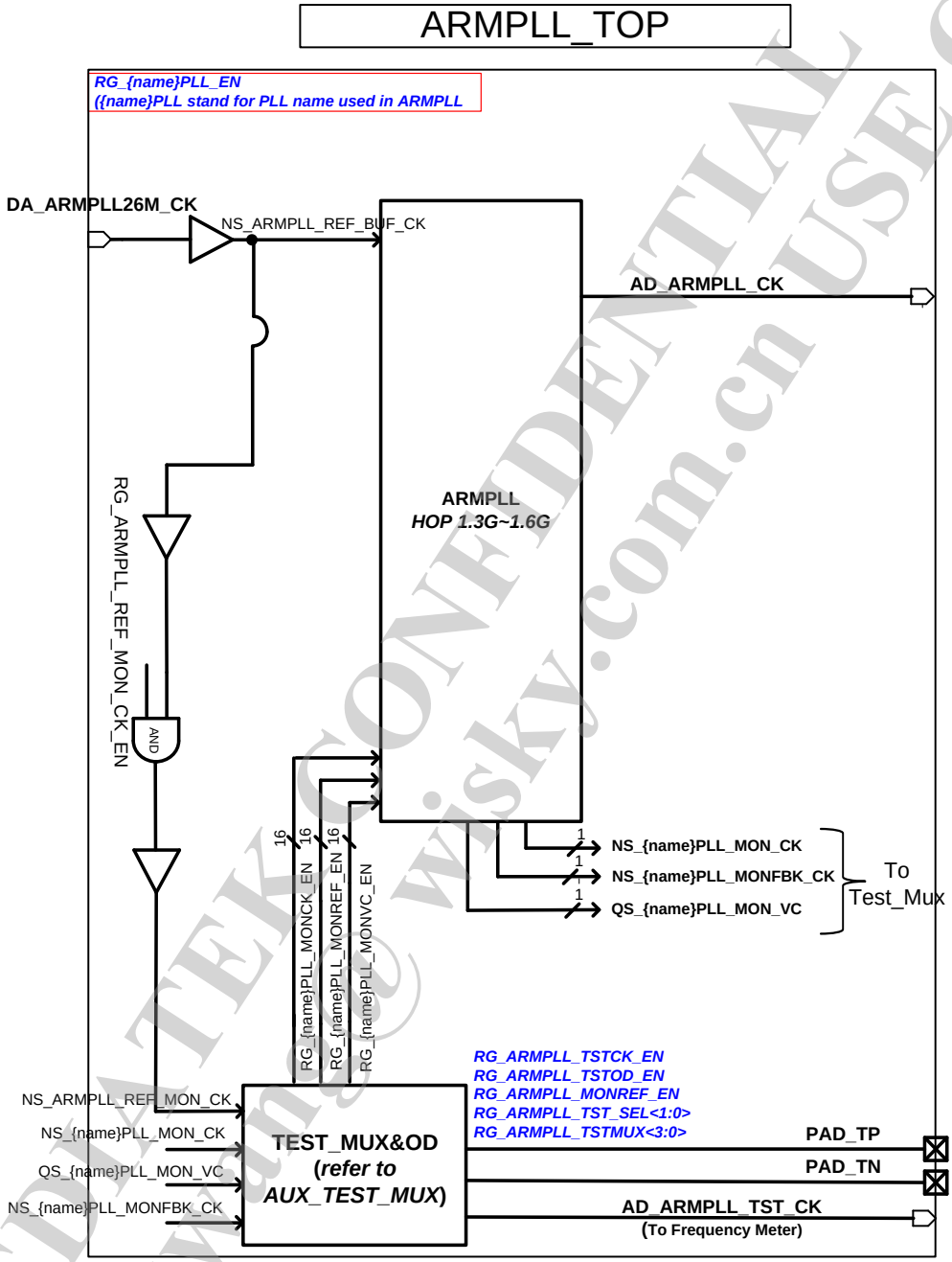


Figure 2-18. Block diagram of ARMPLL

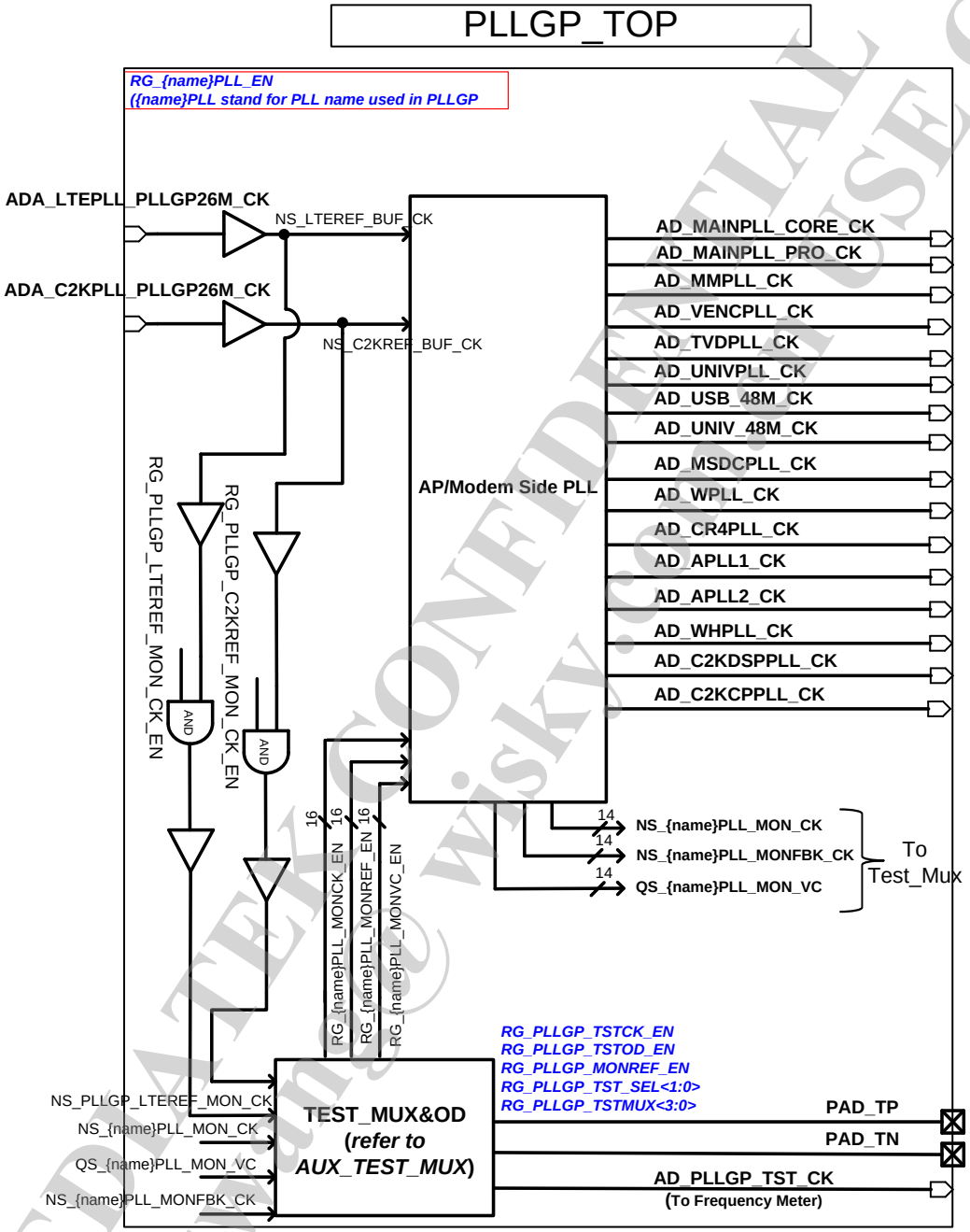


Figure 2-19. Block diagram of PLLGP

2.5.3.10.2 Functional Specifications

See the table below for the functional specifications of PLL.

Table 2-23. ARMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1300		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			1	uA

Table 2-24. MAINPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1092		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		1		mA
	Power-down current consumption			1	uA

Table 2-25. MMPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		450		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-26. UNIVPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency	N/A	1248	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-27. MSDCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		800		MHz
	Settling time		20		us
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-28. WPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	491.52	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (rms period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-29. WHPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency	N/A	500.5	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (rms period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-30. C2KCPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency	N/A	780	N/A	MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-31. C2KDSPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		340		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-32. CR4PLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		1196		MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		30		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-33. VENCPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		295.75		MHz
	Settling time		20		us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-34. TVDPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		148.5		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-35. LTEDSPPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		320		MHz
	Settling time		20		Us

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

Table 2-36. APLL1 specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency		26		MHz
Fout	Output clock frequency		98.304		MHz
	Settling time		20		Us
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)		60		Ps
DVDD	Digital power supply	0.945	1.05	1.155	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-20		80	°C
	Current consumption		0.8		mA
	Power-down current consumption			1	uA

2.5.3.11 Temperature Sensor

2.5.3.11.1 Block Descriptions

In order to monitor the temperature of CPUs, several temperature sensors are provided. The temperature sensor is made of substrate BJT in the CMOS process. The voltage output of temperature sensor is measured by AUXADC.

2.5.3.11.2 Functional Specifications

See the table below for the functional specifications of temperature sensor.

Table 2-37. Temperature sensor specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Resolution		0.15		°C
	Temperature range	0		85	°C
	Accuracy	-5		5	°C
	Active current		60		uA

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Quiescent current		12		uA

2.6 Package Information

2.6.1 Package Outlines

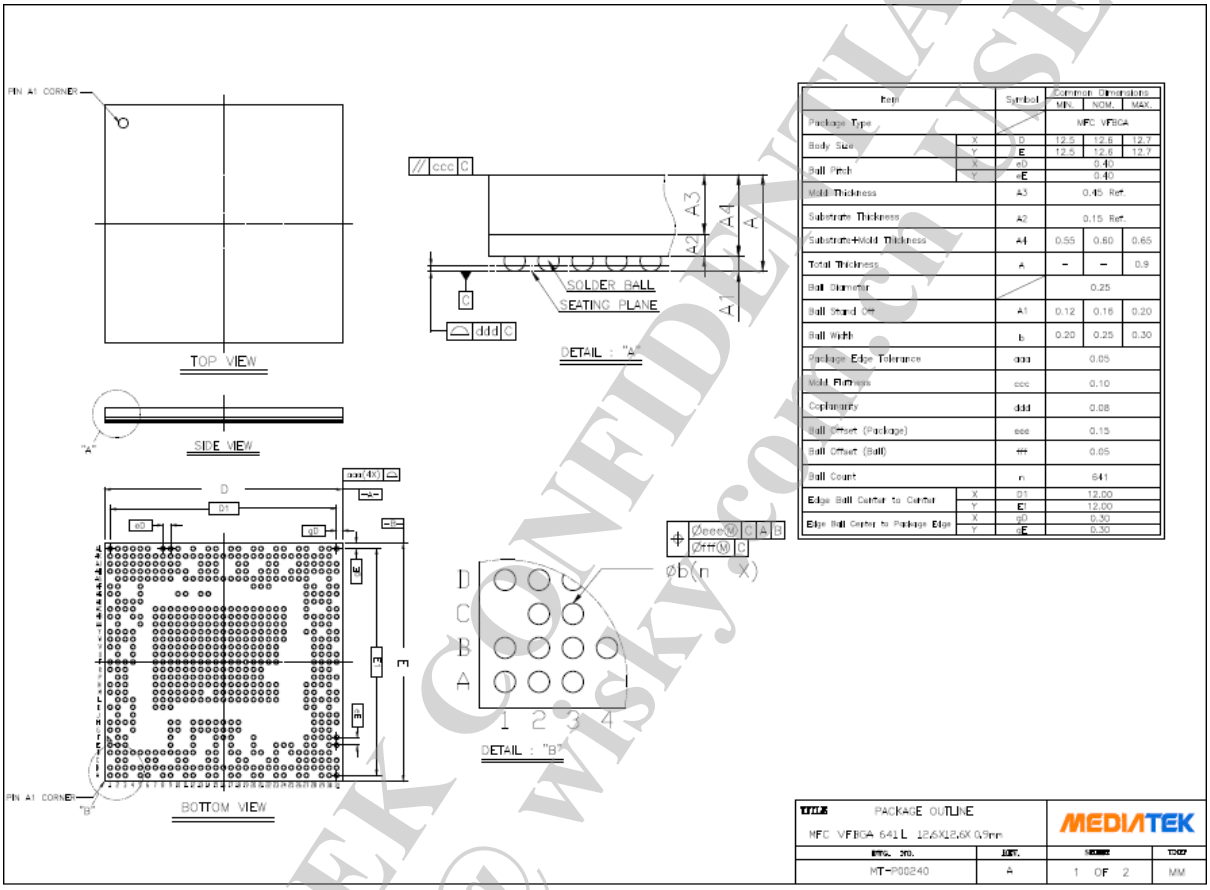


Figure 2-20. Outlines and dimensions of VFBGA 12.6mm*12.6mm, 641 balls, 0.4mm pitch package

2.6.2 Thermal Operating Specifications

Table 2-38. Thermal operating specifications

Symbol	Description	Value	Unit	Note
	Max. operating junction temperature	125	°C	
	Package thermal resistances in nature convection	25.46	°C/Watt	

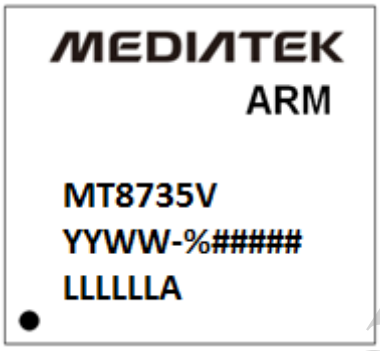
2.6.3 Lead-free Packaging

The chip is provided in a lead-free package and meets RoHS requirements.

2.7 Ordering Information

Order#	Marking	Temp.range	Package
MT8735V/C	MT8735V	-20C~80C	VFBGA
MT8735V/W	MT8735V	-20C~80C	VFBGA
MT8735V/T	MT8735V	-20C~80C	VFBGA

2.7.1 Top Marking Definition



- YYWW: Date code
- %: Functional code
- #####: Subcontractor code
- LLLLLLL: Die lot No.

Figure 2-21. Top mark of MT8735