## GENERAL DESCRIPTION

The MC3430 is a low-noise, integrated digital output 3-axis accelerometer with a feature set optimized for cell phones and consumer product motion sensing. Applications include user interface control, gaming motion input, electronic compass tilt compensation for cell phones, game controllers, remote controls and portable media products.

Accurate event detection is enabled with a low noise architecture that minimizes false triggering found in competing devices. Low noise and low power are inherent in the monolithic fabrication approach, where the MEMS accelerometer is integrated in a single-chip with the electronics integrated circuit.

The sample rate of the MC3430 can be programmed from 1 to 128 samples / second. Even greater power savings can be achieved by taking advantage of event detection while the device is in a low power mode. Specific orientation and gesture conditions can trigger an interrupt to a remote MCU, allowing the processor to remain in a standby state until an event occurs. Alternatively, the device supports the reading of sample and event status via polling.

## FEATURES

Range, Sampling & Power

- ± 1.5g range
- 6,7, or 8-bit resolution
- 1 to 128 samples/sec
- Low power operation
  - 5 µA at 1 sample/sec
  - 30 µA at 128 sample/sec
  - Auto-wake/sniff modes

Event Detection

- Low-noise architecture minimizes false triggering
- Tap, Shake, Drop
- Portrait or landscape orientation with programmable hysteresis
- Tilt detection in six orientations

Simple System Integration

- I2C interface, up to 400 kHz
- 2 × 2 × 0.92 mm 12-pin package
- Pin-compatible to Bosch BMA2xx
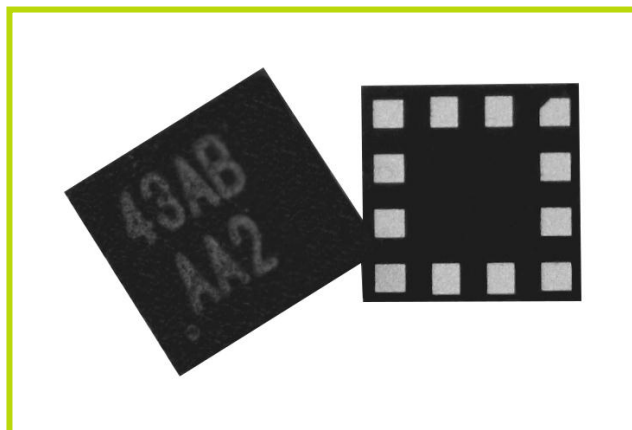- Single-chip 3D silicon MEMS

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# 1 ORDER INFORMATION

| Part Number | Resolution | Order Number | Package | Shipping |
|:---:|:---:|:---:|:---:|:---:|
| MC3430 | 8-bit | MC3430-I5 | VLGA-12 | Tape & Reel, 5Ku |

**Table 1. Order Information**

# 2 FUNCTIONAL BLOCK DIAGRAM
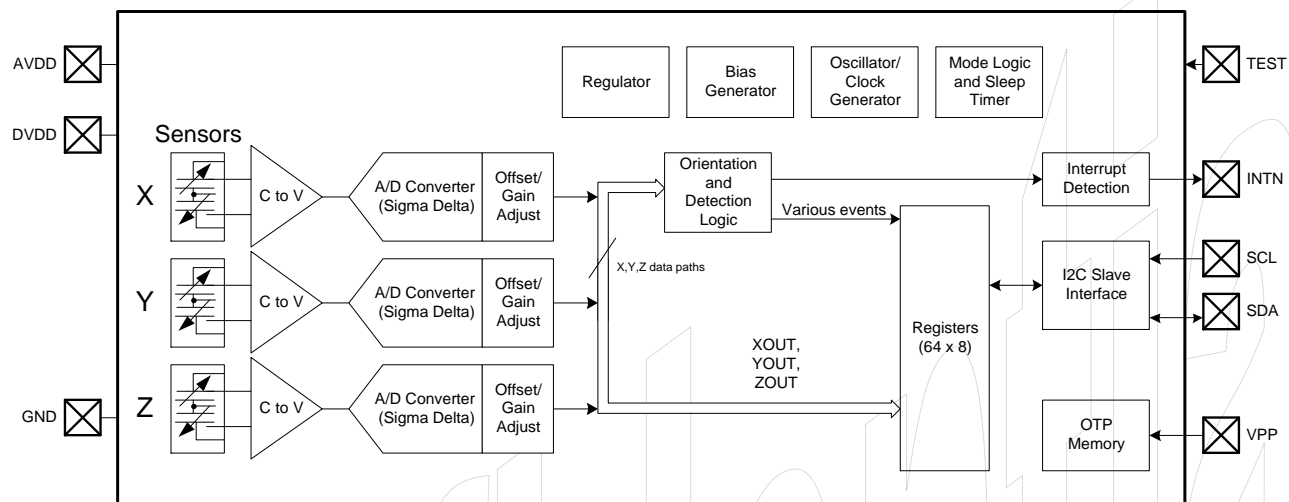


**Figure 1. Block Diagram**

# 3 PACKAGING AND PIN DESCRIPTION

## 3.1 PACKAGE OUTLINE
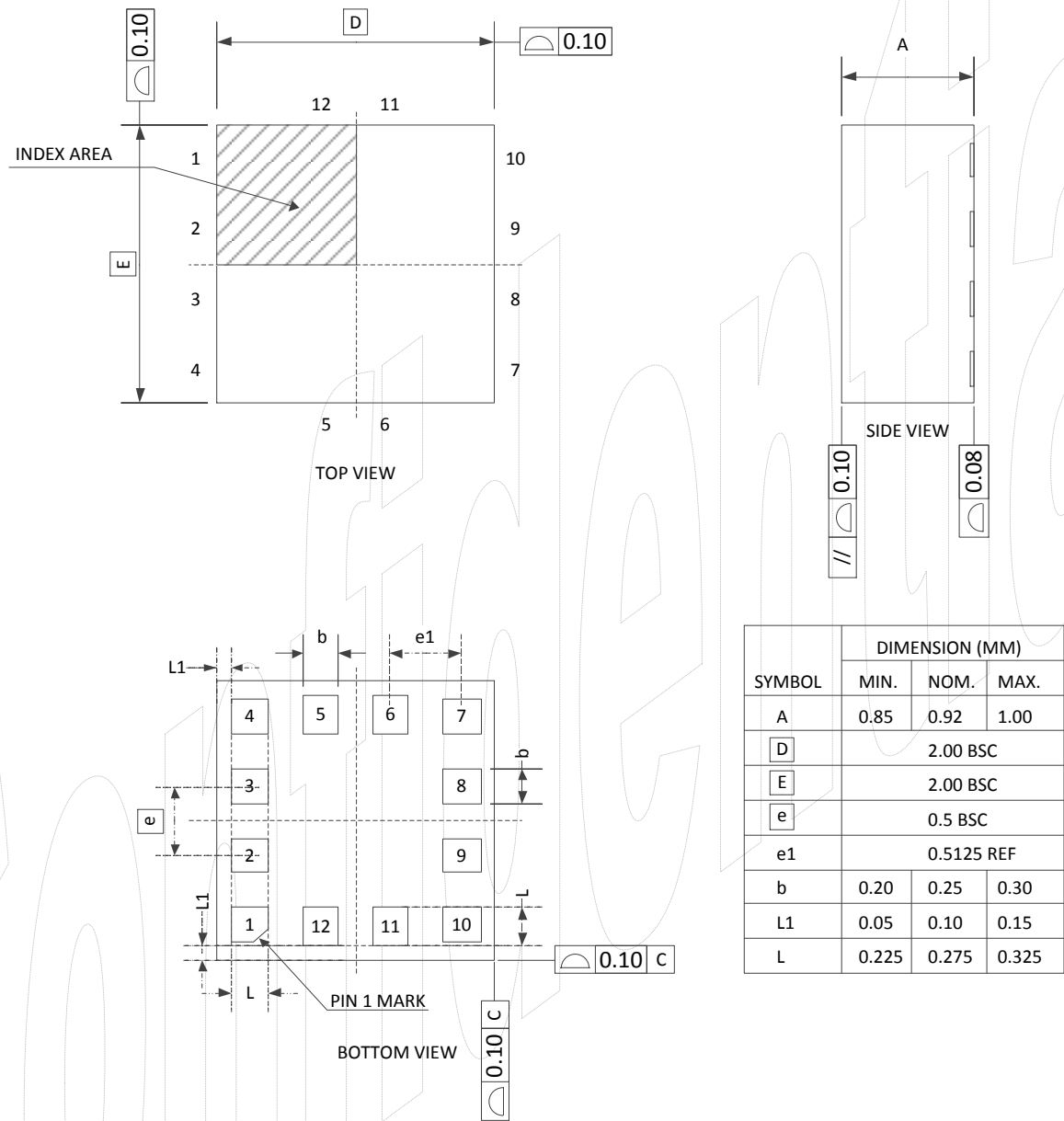


**Figure 2. Package Outline and Mechanical Dimensions**

| SYMBOL | DIMENSION (MM) | | |
|--------|------|------|------|
|        | MIN. | NOM. | MAX. |
| A      | 0.85 | 0.92 | 1.00 |
| D      | 2.00 BSC | | |
| E      | 2.00 BSC | | |
| e      | 0.5 BSC | | |
| e1     | 0.5125 REF | | |
| b      | 0.20 | 0.25 | 0.30 |
| L1     | 0.05 | 0.10 | 0.15 |
| L      | 0.225 | 0.275 | 0.325 |

NOTE: Additional packaging information and device orientation can be found in Section 11.3 TILT: Status Register.

## 3.2  PIN DESCRIPTION

| Pin | Name | Function |
|:---:|:---:|:---:|
| 1 | NC | No connect |
| 2 | SDA [1] | I2C serial data input/output |
| 3 | DVDD | I/O power supply |
| 4 | NC | No connect |
| 5 | INTN [2] | Interrupt active LOW [3] |
| 6 | VPP | Connect to GND |
| 7 | AVDD | Analog power supply |
| 8 | NC | No Connect |
| 9 | GND | Ground |
| 10 | TEST | Optional probe pin |
| 11 | NC | No connect |
| 12 | SCL [1] | I2C serial clock input |

**Table 2. Pin Description**

Notes:

1) This pin requires a pull-up resistor, typically 4.7kΩ to DVDD. Refer to I2C Specification for Fast-Mode devices. Higher resistance values can be used (typically done to reduce current leakage) but such applications are outside the scope of this datasheet.
2) This pin can be configured by software to operate either as an open-drain output or push-pull output (MODE: Register). If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to DVDD.
3) INTN pin polarity is programmable in the MODE: Register.

## 3.3 TYPICAL APPLICATION CIRCUIT
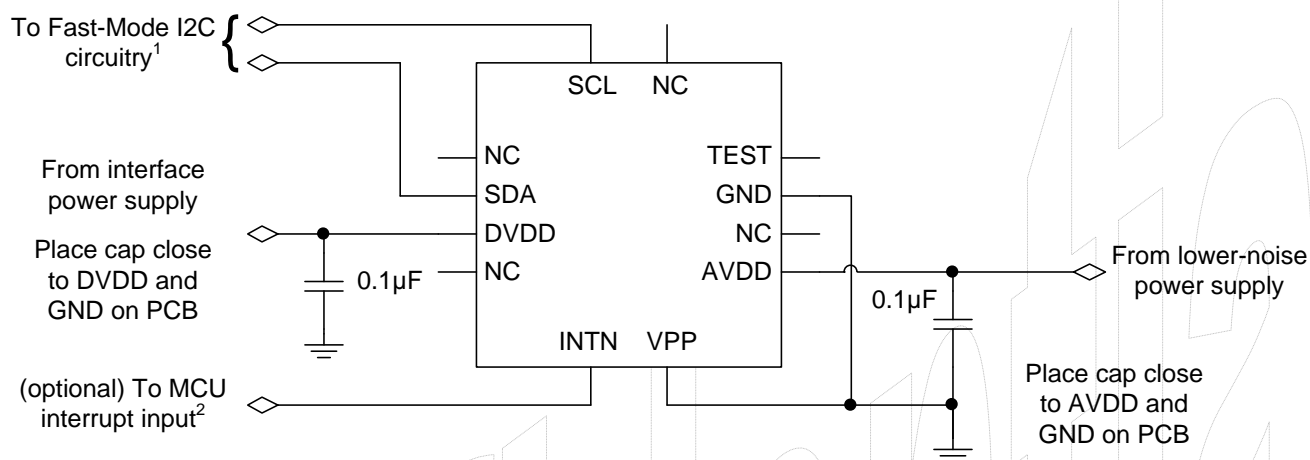


NOTE[1]: Attach typical 4.7kΩ pullup resistors to DVDD, per I2C specification. When
DVDD is powered down, SDA and SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

**Figure 3. Typical Application Circuit**

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be kept away from the sensor. Therefore, for some applications a lower-noise power supply might be desirable to power the AVDD pin.

## 3.4  TAPE AND REEL

Devices are shipped in reels, in standard cardboard box packaging. See Figure 4. MC3430 Tape Dimensions and Figure 5. MC3430 Reel Dimensions.
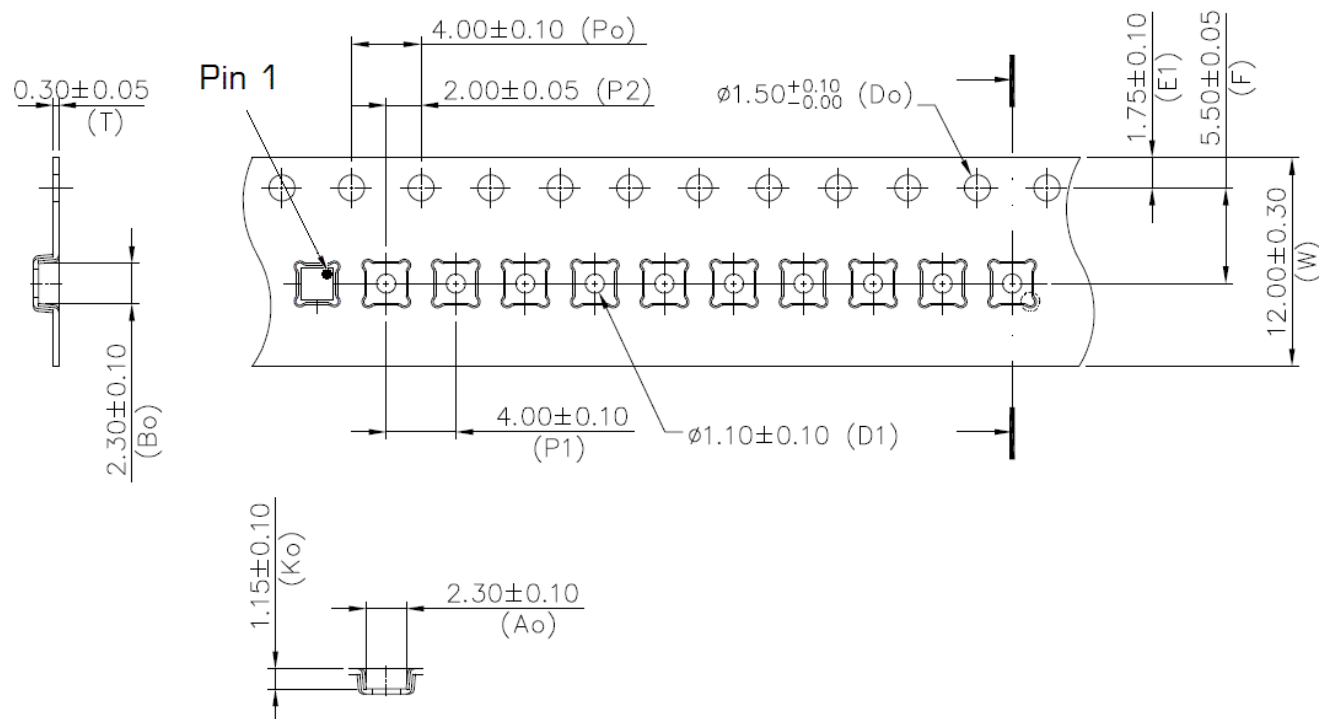


- Dimensions in mm.
- 10 sprocket hole pitch cumulative tolerance ±0.2
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

**Figure 4. MC3430 Tape Dimensions**
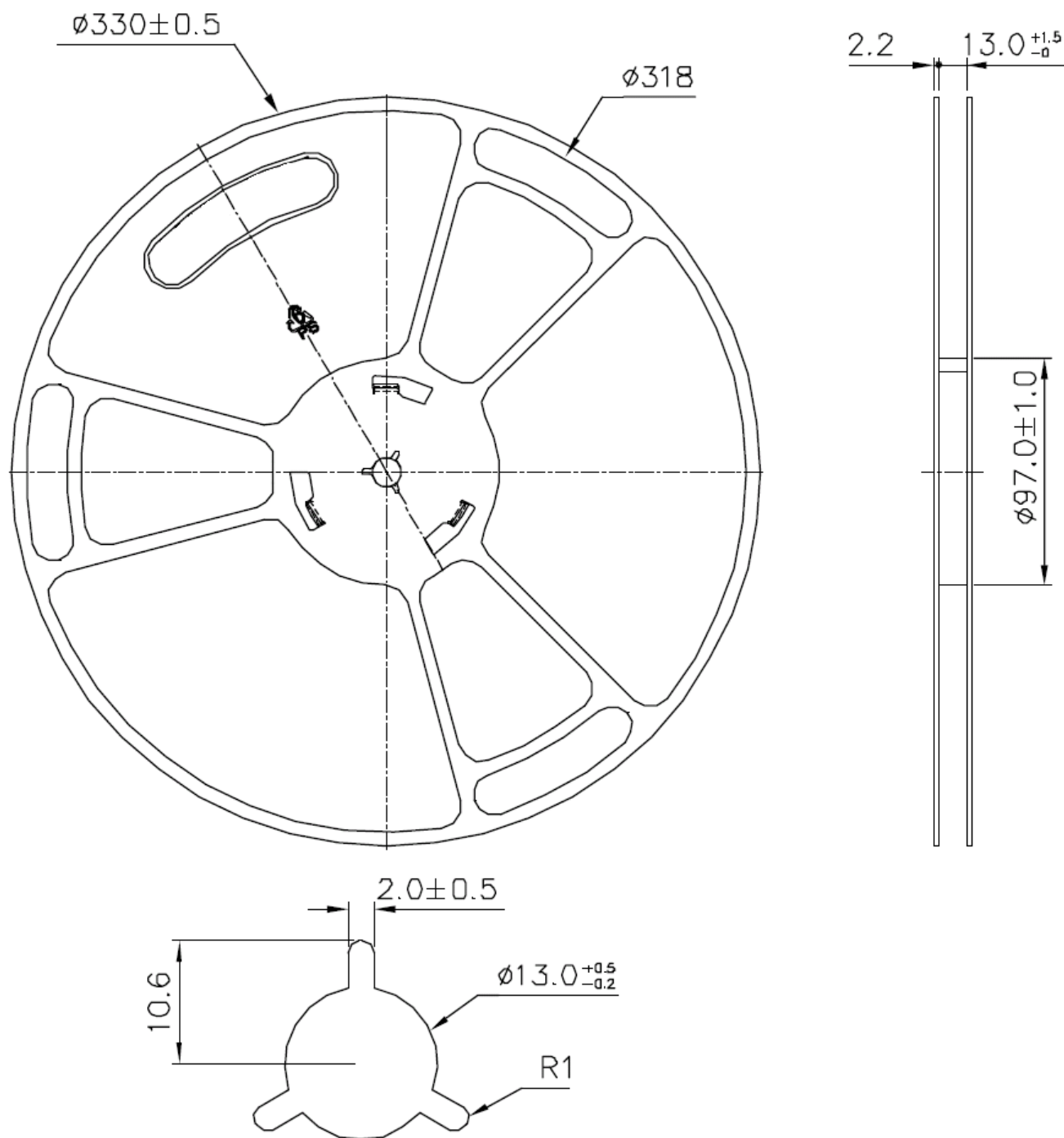
- Dimensions in mm.

**Figure 5. MC3430 Reel Dimensions**

# 4 SPECIFICATIONS

## 4.1 ABSOLUTE MAXIMUM RATINGS

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

| Rating | Symbol | Minimum / Maximum Value | Unit |
|---|---|---|---|
| Supply Voltages | Pins DVDD and AVDD | -0.3 / +3.6 | V |
| Acceleration, any axis, 100 µs | $g_{MAX}$ | 10000 | g |
| Ambient operating temperature | $T_{OP}$ | -40 / +85 | $^0$C |
| Storage temperature | $T_{STG}$ | -40 / +125 | $^0$C |
| ESD human body model | HBM | ± 2000 | V |
| Latch-up current at $T_{op}$ = 25 $^0$C | $I_{LU}$ | 100 | mA |
| Input voltage to non-power pin | Pins INTN, SCL and SDA | -0.3 / (DVDD + 0.3) or 3.6 whichever is lower | V |

**Table 3. Absolute Maximum Ratings**

## 4.2  SENSOR CHARACTERISTICS

DVDD, AVDD = 2.8V, $T_{op}$ = 25 $^0$C unless otherwise noted

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Acceleration range | | | ±1.5 | | g |
| Sensitivity | | | 85 | | LSB/g |
| Sensitivity Temperature Coefficient [1] | -40 ≤ $T_{op}$ ≤ +85 $^0$C | | ± 0.02 | | %/$^0$C |
| Zero-g Offset | | | ± 100 | | mg |
| Zero-g Offset Temperature Coefficient [1] | -40 ≤ $T_{op}$ ≤ +85 $^0$C | | ± 1 | | mg/$^0$C |
| Noise Density [1] | | | 200 | | µg/√Hz |
| Nonlinearity [1] | | | 1 | | % FS |
| Cross-axis Sensitivity [1] | Between any two axes | | 1 | | % |

**Table 4. Sensor Characteristics**

---

[1] Values are based on device characterization, not tested in production.

## 4.3  ELECTRICAL AND TIMING CHARACTERISTICS

### 4.3.1  ELECTRICAL POWER AND INTERNAL CHARACTERISTICS

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage [2] | | AVDD | 2.0 | | 3.6 | V |
| I/O voltage [2] | | DVDD | 1.7 | | 3.6 | V |
| Sample Rate Tolerance [3] | | Tclock | -5 | | 5 | % |

Test condition: AVDD = DVDD = 2.8V, $T_{op}$ = 25 $^0$C unless otherwise noted

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Standby current | AVDD=2.0V | $I_{dd0}$ | | 1.6 | | µA |
| | AVDD=2.8V | | | 1.8 | | |
| | AVDD=3.6V | | | 2.0 | | |
| WAKE state supply current | 1 sample/s | $I_{dd1}$ | | 5 | | µA |
| | 128 samples / s | $I_{dd128}$ | | 30 | | |
| Pad Leakage | Per I/O pad | $I_{pad}$ | -1 | 0.01 | 1 | µA |

**Table 5. Electrical Characteristics**

---

[2] Min and Max limits are hard limits without additional tolerance.

[3] Values are based on device characterization, not tested in production.

## 4.3.2 I2C ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| LOW level input voltage | VIL | -0.5 | 0.3*DVDD | V |
| HIGH level input voltage | VIH | 0.7*DVDD | - | V |
| Hysteresis of Schmitt trigger inputs | Vhys | 0.05*DVDD | - | V |
| Output voltage, pin INTN, Iol ≤ 2 mA | Vol | 0 | 0.4 | V |
| | Voh | 0 | 0.9*DVDD | V |
| Output voltage, pin SDA (open drain), Iol ≤ 1 mA | Vols | - | 0.1*DVDD | V |
| Input current, pins SDA and SCL (input voltage between 0.1*DVDD and 0.9*DVDD max) | Ii | -10 | 10 | µA |
| Capacitance, pins SDA and SCL[4] | Ci | - | 10 | pF |

**Table 6. I2C Electrical and Timing Characteristics**


NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCL should exist. Also, care must be taken to not violate the I2C specification for capacitive loading.
- When DVDD is not powered and set to 0V, INTN, SDA and SCL will be held to DVDD plus the forward voltage of the internal static protection diodes, typically about 0.6V.
- When DVDD is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.

---

[4] Values are based on device characterization, not tested in production.

### 4.3.3 I2C TIMING CHARACTERISTICS
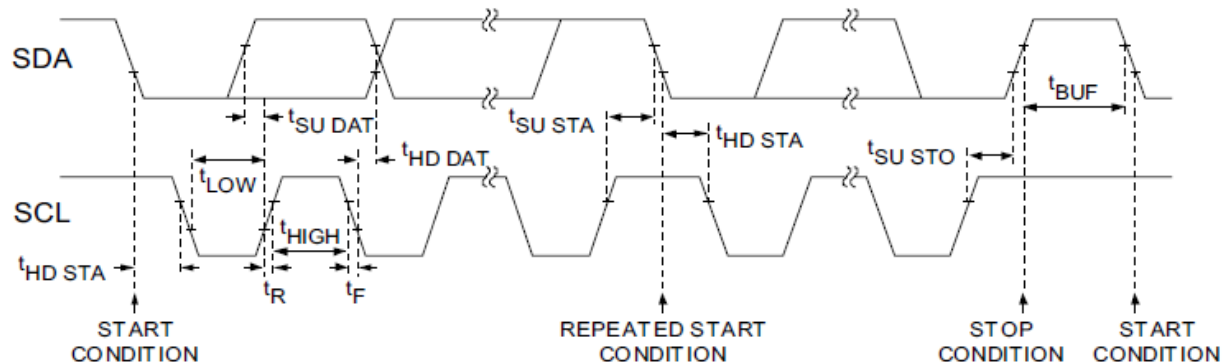


**Figure 6. I2C Interface Timing**

| Parameter | Description | Standard Mode | | Fast Mode | | Units |
|---|---|---|---|---|---|---|
| | | **Min** | **Max** | **Min** | **Max** | **Units** |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{HD; STA}$ | Hold time (repeated) START condition | 4.0 | - | 0.6 | - | μs |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | - | 1.3 | - | μs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | - | 0.6 | - | μs |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | 4.7 | - | 0.6 | - | μs |
| $t_{HD;DAT}$ | Data hold time | 5.0 | - | - | - | μs |
| $t_{SU;DAT}$ | Data set-up time | 250 | - | 100 | - | ns |
| $t_{SU;STO}$ | Set-up time for STOP condition | 4.0 | - | 0.6 | - | μs |
| $t_{BUF}$ | Bus free time between a STOP and START | 4.7 | - | 1.3 | - | μs |

**Table 7. I2C Timing Characteristics**

NOTE: Values are based on I2C Specification requirements, not tested in production.

See also Section 10.3 I2C Message Format.

# 5 GENERAL OPERATION

The sampling rate range for the MC3430 can be set from 1 to 128 samples per second. The resulting sensor readings appear as signed 8-bit values. If 6-bit or 7-bit values are desired by a customer application, software should truncate LSBs from the 8-bit bit-field appropriately.

## 5.1 SENSOR SAMPLING

In the WAKE state, acceleration data for X, Y, and Z axes is sampled at a rate between 1 and 128 samples/second. See Section 11.8 SAMPR: Sample Rate Register.

When the sample rate is set to 128 samples/second, the event detection logic runs at 256 Hz. At other sample rates the event detection logic runs at the sample rate.

The detectable acceleration range is from -1.5g to +1.5g.

In the lower power SNIFF state, acceleration data for X, Y, and Z axes is sampled at a reduced rate between 1 and 32 samples/second. See Section 11.8 SAMPR: Sample Rate Register.

Typically, a rate of about 20 to 50 samples per second is required to detect shake events in user-interface types of applications. Detecting tap events in these applications is best done at the rate of 64 to 128 samples per second. An event may be detected at any sampling rate, no matter how slow, however the trade-off is that at slower rates the events must be stronger to be detected.

The measurement data is stored in the XOUT, YOUT, and ZOUT registers in 2's complement format. Each sample is used to update the SHAKED, TAPD, DROPD, and BAFR and POLA orientation status bits in the TILT: Status Register. See Section 11.2 XOUT, YOUT & ZOUT: X, Y & Z-Axis Accelerometer Registers.

| Resolution | Acceleration Range | Value per bit (mg/LSB) | Full Scale Negative Reading | Full Scale Positive Reading | Comments |
|---|---|---|---|---|---|
| 8-bit | ± 1.5g | ~11.7 | 0x80 (-128) | 0x7F (+127) | Signed 2's complement number, results in XOUT, YOUT, ZOUT. The MSB is the sign bit. (Integer interpretation also shown) |

**Table 8. Summary of Resolution, Range, and Scaling**

## 5.2  OFFSET AND GAIN CALIBRATION

Digital offset and gain calibration can be performed on the sensor, if necessary, in order to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values. The register controls are described in Sections 11.14 through 11.19.

# 6 OPERATIONAL STATES

The device has three states of operation: STANDBY (the default state after power-up), SNIFF, and WAKE, to provide a balance between power consumption and motion event detection.

The STANDBY state offers the lowest power consumption. In this state, the I2C interface is active and all register reads and writes are allowed. There is no event detection, sampling, or acceleration measurement in the STANDBY state. Internal clocking is halted. Complete access to the register set is allowed in this state, but interrupts cannot be serviced. The device defaults to the STANDBY state following power-up. The time to change states from STANDBY to another state is less than 10uSec and does not depend upon the sample rate.

**Registers can be written (and therefore thresholds and other settings changed) only when the device is in STANDBY state.**

The SNIFF state offers low power consumption, event detection, and an auto-wake feature at a reduced sampling rate. The SNIFF state samples the accelerometer values at a slower rate than the WAKE state, typically done to save power.

The WAKE state offers the highest sampling rate and therefore the most precise motion event detection. The WAKE state also features an auto-sniff option that changes the device back to the lower-power SNIFF state if there is no motion activity for a timeout period. The sampling rate can vary from 1 sample/second to up to 128 samples/second, as described in Table 12. WAKE State Sample Rates.

The I2C interface allows write access to all registers only in the STANDBY state. In SNIFF and WAKE states, the only I2C register write access permitted is to the MODE: Register. Full read access is allowed in all states.

| State | I2C Bus | Description |
|-------|---------|-------------|
| STANDBY | Device responds to I2C bus (R/W) | Device is powered; Registers can be accessed via I2C. Auto-wake is not enabled, so there is no event sniffing. Lowest power state. No interrupt generation, internal clocking disabled. Default power-on state. |
| SNIFF | Device responds to I2C bus (Read) | Low power state, auto-wake is enabled. The device sniffs or checks for motion events at the sample rate specified by the bit-field SNIFFR. All registers except the MODE: Register are read-only. |
| WAKE | Device responds to I2C bus (Read) | WAKE state has the most choices for sample rate, allows for the continuous sampling and reading of sense data, and can make use of the sleep counter to detect periods of inactivity. During Low-Res sampling, the wake state sample rate is determined by the WAKER bit-field in the SAMPR: Sample Rate Register. All registers except the MODE: Register are read-only. |

**Table 9. Operational States**

# 7 OPERATIONAL STATE FLOW

Figure 7. Operational State Flow shows the operational state flow for the device. When set to fully automatic mode (via the MODE: Register), the device will automatically transition between SNIFF and WAKE states as motion events or periods of inactivity are detected. Settings in the MODE: Register can be used to force the device into any of the three states. The device defaults to STANDBY following power-on.
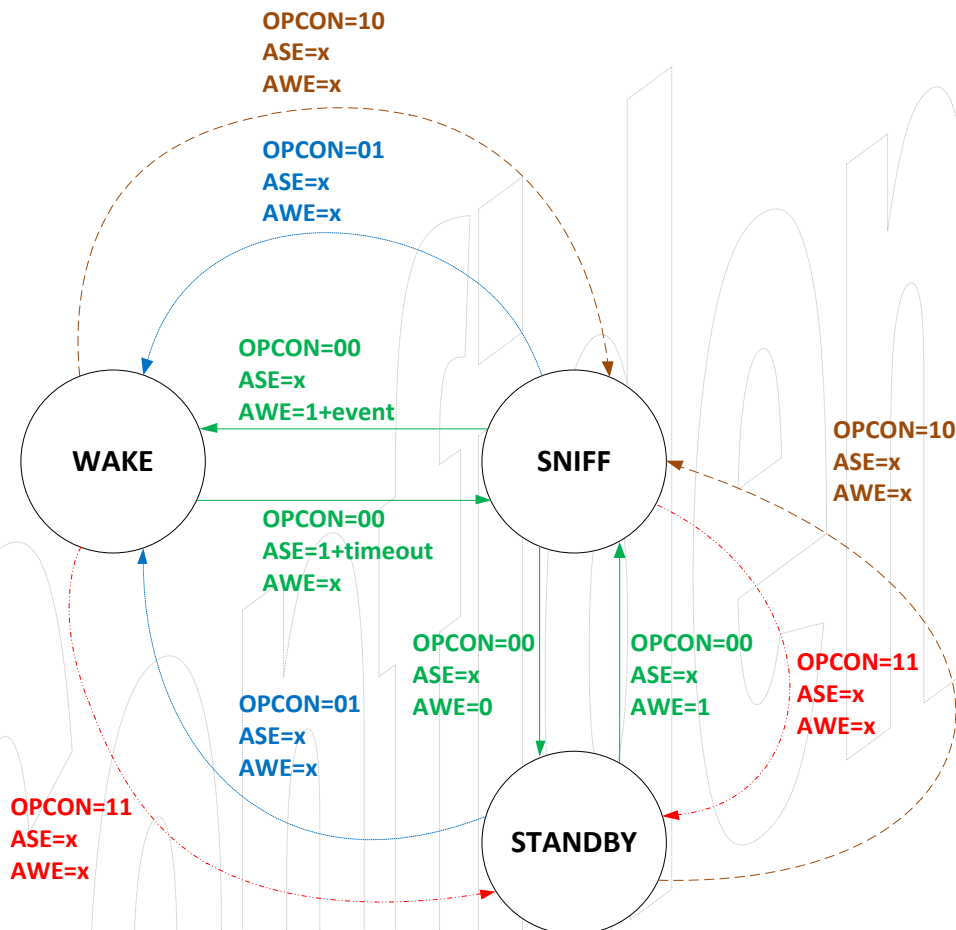


**Figure 7. Operational State Flow**

Additionally, the operational state may be forced to a specific state by writing into the OPCON bits, as shown below. The operational state will stay in the mode specified until changed:

| Action | Setting | Effect |
|---|---|---|
| Force Wake State | OPCON[1:0] = 01 | • Switch to WAKE state and stay there<br>• Switch to WAKER sampling rate |
| Force Sniff State | OPCON[1:0] = 10 | • Switch to SNIFF state and stay there<br>• Switch to SNIFFR sample rate<br>• Ignore sleep counter timeout<br>• Ignore AWE |
| Force Standby State | OPCON[1:0] = 11 | • Switch to STANDBY state and stay there<br>• Disable sensor and event sampling<br>• Ignore AWE |
| Set to auto-wake / sniff | OPCON[1:0] = 00 | • See Table 11 below |

**Table 10. Forcing Operational States**

The truth table for the Operational State Flow is shown in Table 11. Auto-Wake / Sniff Operational State Flow Truth Table.

| ASE | AWE | EVENT | SNIFF TIMEOUT | Current State | Next State | Comments |
|---|---|---|---|---|---|---|
| x | 1 | x | x | STANDBY | SNIFF | Use AWE to move from STANDBY to SNIFF |
| x | 0 | x | x | SNIFF | STANDBY | |
| x | 1 | 1 | x | SNIFF | WAKE | Use AWE and EVENT to move from SNIFF to WAKE |
| 1 | x | x | 1 | WAKE | SNIFF | Use ASE and SNIFF TIMEOUT to move from WAKE to SNIFF |

**Table 11. Auto-Wake / Sniff Operational State Flow Truth Table**

## 7.1  SAMPLING RATES

The MC3430 features two sample rate selections, one for the WAKE state and one for the SNIFF state. The SAMPR: Sample Rate Register contains the controls for the WAKE state sample rate, set by the WAKER bit-field and the SNIFF state sample rate, set by the SNIFFR bit-field. The WAKE state sample rate can be set between 1 and 128 samples/second, as shown in Table 12. The SNIFF state sample rate can be set between 1 and 32 samples/second as shown in Table 13.

Sample measurements appear, one set per sample period, in the XOUT, YOUT, and ZOUT registers.

| WAKER [2:0] | WAKE State Samples/ Second | Description |
|---|---|---|
| 000 | 128 | |
| 001 | 64 | |
| 010 | 32 | Wake State Sample Rate |
| 011 | 16 | |
| 100 | 8 | The wake state sample rate is determined by the WAKER bit-field in the SAMPR: Sample Rate Register. |
| 101 | 4 | |
| 110 | 2 | |
| 111 | 1 | |

**Table 12. WAKE State Sample Rates**

| SNIFFR [1:0] | SNIFF State Samples/ Second | Description |
|---|---|---|
| 00 | 32 | Sniff State Sample Rate |
| 01 | 16 | The SNIFF state sample rate is determined by the SNIFFR bit-field in the SAMPR: Sample Rate Register. |
| 10 | 8 | |
| 11 | 1 | |

**Table 13. SNIFF State Sample Rates**

# 8  INTERRUPTS

The sensor device utilizes output pin INTN to signal to an external microprocessor that an event has been sensed. The microprocessor would contain an interrupt service routine which would perform certain tasks after receiving this interrupt and reading the associated status bits, perhaps after the product was put into a certain orientation or had been tapped. The microprocessor would set up the registers in the sensor so that when a specific event is detected, the microprocessor would receive the interrupt and the interrupt service routine would be executed.

For products that will instead use polling, the method of reading sensor data would be slightly different. Instead of receiving an interrupt when an event occurs, the microprocessor must periodically poll the sensor and read status data while the INTN pin is not used. For most applications this is likely best done at the sensor sampling rate or faster. Note that at least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

**In this case, the event detection bits (TAPD, SHAKED, DROPD) and associated interrupt enable bits in the <u>TILT: Status Register</u> must still be set up as if interrupts would occur in order for the status registers to be updated with proper data.**

Although the INTN is not connected, the registers in the sensor will still contain valid status and so can be used by software to know the orientation of the product or if an event has occurred.

## 8.1  ENABLING AND CLEARING INTERRUPTS

The <u>INTEN: Interrupt Enable Register</u> determines which events generate interrupts. When an event is detected, it is masked with an interrupt enable bit in this register and the corresponding status bit is set in the <u>TILT: Status Register</u>. Multiple interrupt events might be reported at the same time in the <u>TILT: Status Register</u>, so software must interpret and prioritize the results.

**The pin INTN is cleared during the next I2C bus cycle after the device ID has been recognized by the device.**

When an interrupt is triggered, the first I2C read access to the device clears INTN pin. The condition (TAPD, SHAKED, DROPD) that generated the interrupt will remain held in the <u>TILT: Status Register</u> until it is read. Note that the orientation bit-fields POLA and BAFR are continuously updated (every sample) in the <u>TILT: Status Register</u> and are not held. Note that multiple interrupts may be active at the same time, and so a software routine reading the <u>TILT: Status Register</u> should account for this.

Any of the following interrupts can be enabled or disabled in the <u>INTEN: Interrupt Enable Register</u> and <u>DROP: Drop Event Control Register</u>.

– Front/Back Interrupt

– Up/Down/Left/Right (portrait / landscape) Interrupt

– Tap Detection Interrupt

– GINT (real-time motion tracking, generate interrupt each sample period)

– Shake on X-axis, Shake on Y-axis, and Shake on Z-axis

– Drop event detection

The <u>INTEN: Interrupt Enable Register</u> contains many of the interrupt enable bits. The drop interrupt enable bit DINT is located in the <u>DROP: Drop Event Control Register</u>.

## 8.2  INTERRUPT SUPPORT

The following table shows the relationship between motion events, interrupt enable bits, and the states the device may be in for determining when the device will generate an interrupt. No measurements or interrupts are generated in the STANDBY state.

| Motion Event | Interrupt Enable Bits | Wake | Sniff | Standby |
|---|---|---|---|---|
| Portrait/Landscape or Front/Back orientation change | FBINT = 1 PLINT = 1 | Yes | Yes | No |
| Shake | SHINTX = 1 SHINTY = 1 SHINTZ = 1 | Yes | Yes | No |
| Tap | TINT = 1 | Yes | No | No |
| | | Yes | Yes | No |
| Drop | DINT = 1 | Yes | Yes | No |
| Auto-Sniff (no activity detected) | ASINT = 1 | Yes when ASE=1 | No | No |
| Sample Update | GINT = 1 | Yes | No | No |

**Table 14. Interrupt Support**

## 8.3  GINT INTERRUPT

When enabled, the GINT interrupt triggers each time a sample acquisition is completed. The next I2C read operation rearms the interrupt for the next sample period but the condition (e.g. TAPD, SHAKED, DROPD) that generated the interrupt will remain held in the TILT: Status Register until it is read. The GINT interrupt frequency is determined by the WAKE state sample rate, 1 to 128 samples/seconds.

## 8.4  EVENT DETECTION

The detection logic monitors and compares sensor outputs against the comparisons selected by the application software. Each type of event can be masked by a separate bit in the <u>INTEN: Interrupt Enable Register</u>. The following table shows how the detection events are evaluated.

| Event | X Axis | Y Axis | Z Axis |
|---|---|---|---|
| Up | $\|Z\| <$ (UD_Z_TH) and $\|X\| >$ (UD_X_TH) and $X < 0$ [1] | | |
| Down | $\|Z\| <$ (UD_Z_TH) and $\|X\| >$ (UD_X_TH) and $X > 0$ [1] | | |
| Right | | $\|Z\| <$ (RL_Z_TH) and $\|Y\| >$ (RL_Y_TH) and $Y < 0$ [2] | |
| Left | | $\|Z\| <$ (RL_Z_TH) and $\|Y\| >$ (RL_Y_TH) and $Y > 0$ [2] | |
| Front | | | $Z >$ FB_Z_TH [3] |
| Back | | | $Z < -1 *$ FB_Z_TH [3] |
| SHAKED [4] | $\|X\| > 1.3g \pm$ SHAKE_TH | $\|Y\| > 1.3g \pm$ SHAKE_TH | $\|Z\| > 1.3g \pm$ SHAKE_TH |
| DROPD [5] | $\|X\| < 0.5g \pm$ DROP_TH | $\|Y\| < 0.5g \pm$ DROP_TH | $\|Z\| < 0.5g \pm$ DROP_TH |
| TAPD [6] | $\|X\| >$ TAP_TH | $\|Y\| >$ TAP_TH | $\|Z\| >$ TAP_TH |

**Table 15. Detection Logic Event Evaluation**

[1] Up/Down Z threshold is programmable from 0.425g to 1.172g, up/down X threshold is programmable from $\|X\|$ to $\|X\| + 0.747g$.

[2] Right/left Z threshold is programmable from 0.425g to 1.172g, right/left Y threshold is programmable from $\|Y\|$ to $\|Y\| + 0.747g$.

[3] Front/back Z threshold is programmable from 0.174g to 0.547g.

[4] SHAKED event is triggered when any axis > SHAKE_TH, programmable from 0.925g to 1.1672g.

[5] DROPD event is triggered when condition (a) $\|X\| + \|Y\| + \|Z\| < 0.5g +$ DROP_TH or condition (b) $\|X\| < 0.5g \pm$ DROP_TH and $\|Y\| < 0.5g \pm$ DROP_TH and $\|Z\| < 0.5g \pm$ DROP_TH, this is user selectable. The range is from 0.125g to 0.872g.

[6] TAPD event is triggered by $\|X\| >$ TAP_TH or $\|Y\| >$ TAP_TH g or $\|Z\| >$ TAP_TH, where TAP_TH is programmable and any combination of X, Y, and Z may be selected.

# 9 ORIENTATION DETECTION

The MC3430 allows an application to determine the orientation of the device. The current orientation of the device is reported as Left, Right, Up, Down, Front, and Back for each sampling period. This information generates the Portrait/Landscape status bits in the TILT: Status Register.

## 9.1 ORIENTATION EVENT FILTER

Application software can change the sensitivity of the POLA orientation detection by using the debounce filter settings FILT bit-field in the SAMPR: Sample Rate Register.

If FILT = 0, then new values for Left, Right, Up and Down are updated in the TILT: Status Register after each sampling period.  If the FILT bit-field is set to another value, the device will update these values in the TILT: Status Register only after the orientation readings for Left, Right, Up and Down are the same for that number of consecutive sampling periods. The FILT bit-field has no effect on the reporting of Back / Front orientation status.

The debounce filter is reset after a mismatched reading or the orientation condition is met and the TILT: Status Register updated.

## 9.2 ORIENTATION HYSTERESIS

Hysteresis can be added to portrait/landscape and front/back detection by modifying the default threshold offset values. See the specific sections below for more information.

## 9.3 PORTRAIT/LANDSCAPE EVENTS

Portrait/landscape detection is a combination of left, right, up, and down events, also partially dependent upon Z sensor readings.

The default comparison angle for portrait/landscape is 45 degrees when evaluating differences between LEFT, RIGHT, UP, and DOWN, as long as the magnitude of Z is < 0.8g (default). See Figure 8.

By increasing the threshold values written to the UD_X_TH: Up/Down X Axis Threshold and RL_Y_TH: Right/Left Y Axis Threshold, hysteresis can be introduced to the angle of evaluation. These registers add a small offset to the default X and Y values and introduce additional margin in the portrait/landscape detection logic.

For most applications, the same value should be written to both registers.

When the device orientation is in the hysteresis region, the device will report orientation as "unknown". When this reading is reported, in order to implement a hysteresis effect for orientation, high-level software should use the last known portrait/landscape information.

In the example shown in Figure 9 the evaluation angle has been decreased to 40 degrees in each threshold, such that there is a 10 degree "deadband" or hysteresis-area between LEFT/RIGHT and DOWN/UP areas. The circle represents the acceleration in the Z axis, which has a default of 0.8g, or about a 33 degree tilt relative to the Z axis.
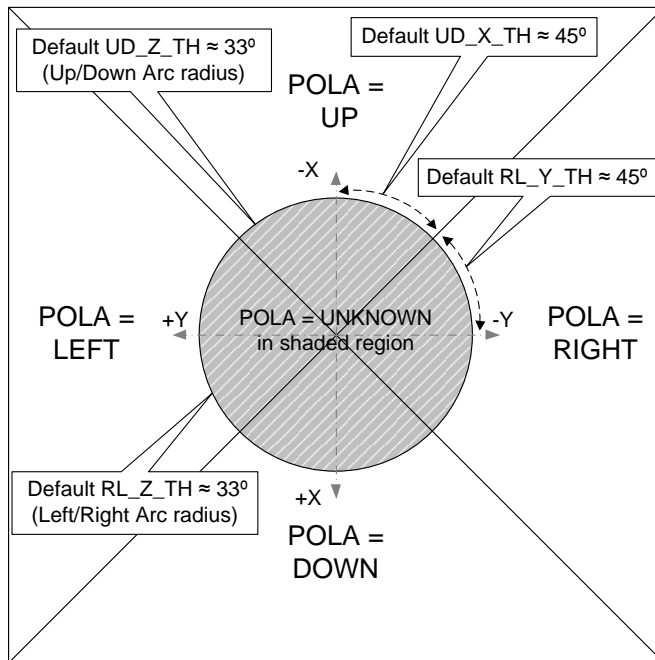


**Figure 8. Default Orientation Settings**
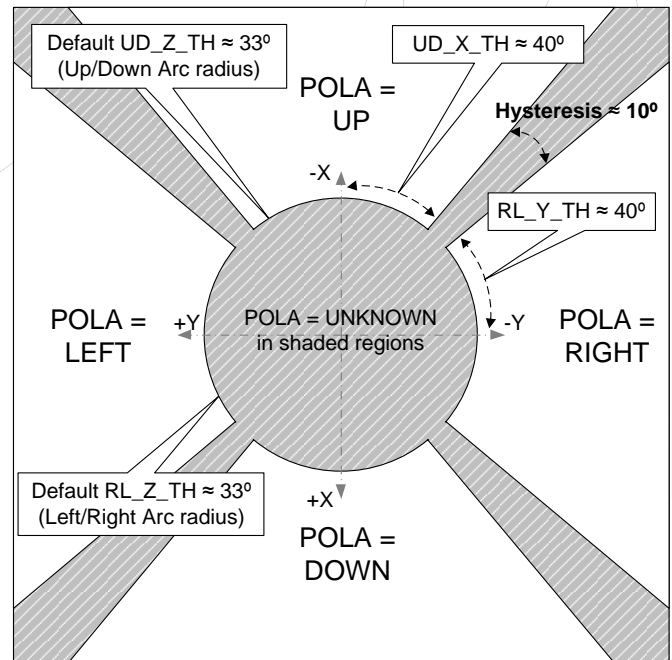


**Figure 9. Example Simple Orientation Hysteresis = 10 degrees**

The Z threshold for each direction can also be adjusted, as shown in Figure 10. This has the effect of altering the angle relative to the Z axis which causes the orientation state to change.

Figure 11 shows an example of setting the UD_Z_TH and RL_Z_TH registers to different values, as well as setting the UD_X_TH and RL_Y_TH registers to different values. However for most applications the same value should be written to both registers in both cases.
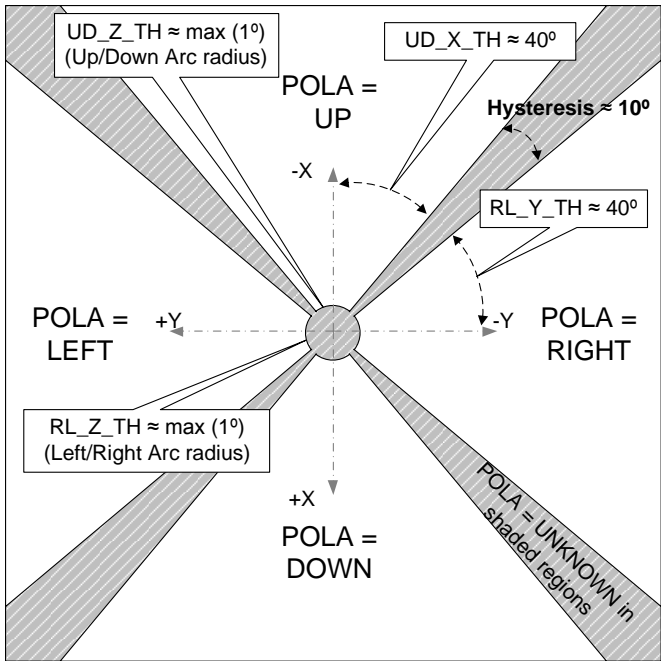
**Figure 10. Effect of Changing UD_Z_TH Threshold with Hysteresis = 10 degrees**
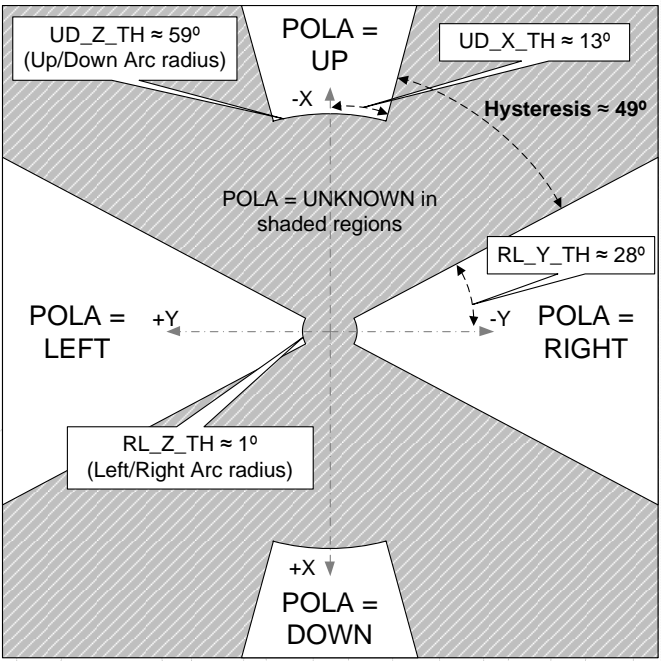
**Figure 11. Example of Complex Thresholds for Up/Down X, Right/Left Y, Up/Down Z & Right/Left Z**

Table 16 summarizes the portrait/landscape event evaluation criteria. Some example threshold values and the corresponding trip angle and amount of hysteresis are shown in Table 17.

| Event | X Axis | Y Axis | Z Axis |
|-------|--------|--------|--------|
| Up | \|Z\| < (UD_Z_TH) and <br> \|X\| > (UD_X_TH) and <br> X < 0 | | |
| Down | \|Z\| < (UD_Z_TH) and <br> \|X\| > (UD_X_TH) and <br> X > 0 | | |
| Right | | \|Z\| < (RL_Z_TH) and <br> \|Y\| > (RL_Y_TH) and <br> Y < 0 | |
| Left | | \|Z\| < (RL_Z_TH) and <br> \|Y\| > (RL_Y_TH) and <br> Y > 0 | |

**Table 16. Portrait/Landscape Event Evaluation Criteria**

| Registers UD_X_TH or RL_Y_TH Threshold Value | Trip Angle (approx. degrees) | Resulting Hysteresis (approx. degrees) | Corresponding g Value (approximate) |
|---|---|---|---|
| 0x00 | 45 | 0 | 0.72 |
| 0x10 | 43 | 4 | 0.68 |
| 0x20 | 41 | 8 | 0.66 |
| 0x30 | 39 | 12 | 0.63 |
| 0x40 | 37 | 16 | 0.61 |
| 0x50 | 36 | 20 | 0.58 |
| 0x60 | 34 | 24 | 0.55 |
| … | … | … | … |
| 0xFF | 15 | 64 | 0.26 |

**Table 17. Some Approximate X and Y-axis Portrait/Landscape Evaluation Angles and Values**

| Registers UD_Z_TH or RL_Z_TH Threshold Value | Trip Angle (approx. degrees) | Corresponding g Value (approximate) |
|---|---|---|
| 0x80 | 67 | 0.43 |
| 0x90 | 64 | 0.47 |
| … | … | … |
| 0xE0 | 48 | 0.71 |
| 0xF0 | 45 | 0.75 |
| 0x00 | 40 | 0.80 |
| 0x10 | 36 | 0.85 |
| 0x20 | 32 | 0.89 |
| … | … | … |
| 0x70 | 9 | 1.13 |
| 0x7F | 3 | Max (~1.17)* |

**Table 18. Some Approximate Z-axis Portrait/Landscape Evaluation Angles and Values**

NOTE*: Max values > 1.0g are possible, to cover offset variations.

Table 19 shows the orientation event conditions for the portrait/landscape detection hardware. The FILT bit-field in the SAMPR: Sample Rate Register can be used for the debouncing of portrait/landscape updates, as described above.

| POLA[2:0] | Left | Right | Down | Up | Description/Comments |
|---|---|---|---|---|---|
| 000 | 0 | 0 | 0 | 0 | Unknown |
| 001 | 1 | 0 | 0 | 0 | Left/landscape |
| 010 | 0 | 1 | 0 | 0 | Right/landscape |
| 101 | 0 | 0 | 1 | 0 | Down/portrait |
| 110 | 0 | 0 | 0 | 1 | Up/portrait |

**Table 19. Portrait/Landscape TILT: Status Register Assignments**

## 9.4  FRONT/BACK EVENTS

The front/back detection compares ZOUT with a low g value, ranging from 0.174g to 0.547g, with the offset from 0.174g specified by the FB_Z_TH: Front/Back Z Axis Threshold Register. This equates to a range of approximately 55 degrees.

The BAFR bit-field is updated in the TILT: Status Register according to the front/back orientation sensed by the device. Additional hysteresis can be added to front/back detection by increasing the front/back Z axis threshold value located in the FB_Z_TH: Front/Back Z Axis Threshold Register.

When the front/back orientation of the device is in the deadband region, BAFR bit-field will report the orientation as "unknown". The default settings (0x00) equate to a range of approximately 25 degrees where the sensor will report BAFR = FRONT (or BACK). The maximum settings (0xFF) equate to about a 80 degree range. See Figure 12 and Figure 13.
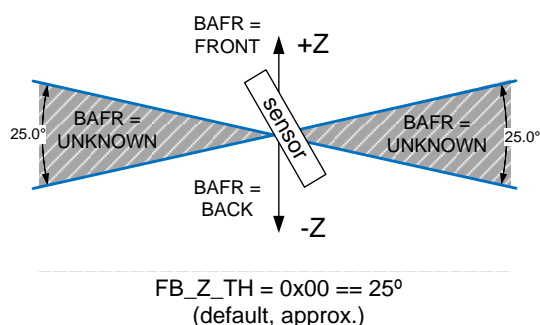


**Figure 12. Default Setting of FB_Z_TH for BAFR Readings**
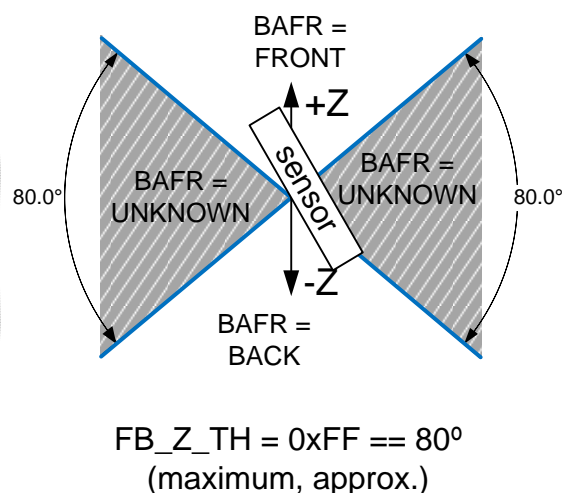


**Figure 13. Maximum setting of FB_Z_TH for BAFR Readings**

The bit settings for the BAFR bit-field are shown in Table 20. Table 21 shows the front/back orientation evaluation criteria. Some example threshold values and the corresponding trip angles are shown in Table 22. All values are approximate and not tested in production.

| BAFR[1:0] | Status |
|-----------|--------|
| 00 | Unknown condition of front or back |
| 01 | Front: Device is in orientation e. in Figure 20 |
| 10 | Back: Device is in orientation f. in Figure 20 |
| 11 | Reserved |

**Table 20. BAFR Bit Assignments in the <u>TILT: Status Register</u>**

| Event | X Axis | Y Axis | Z Axis |
|-------|--------|--------|--------|
| Front | | | Z > FB_Z_TH |
| Back | | | Z < -1 * FB_Z_TH |

**Table 21. Front/Back Event Evaluation**

| Threshold Value | FB_Z_TH Trip Angle (approx. degrees) |
|-----------------|--------------------------------------|
| 0x00 | 25 |
| 0x10 | 28 |
| 0x20 | 32 |
| 0x30 | 35 |
| 0x40 | 39 |
| 0x50 | 42 |
| 0x60 | 46 |
| 0x70 | 49 |
| … | … |
| 0xFF | 80 |

**Table 22. Approximate Front/Back Evaluation Angles and Values**

## 9.5  SHAKE DETECTION

The threshold for detecting a shake event can be set to a range of values around a 1.3g baseline. The shake threshold can range from 0.925g to 1.672g. The value is a signed, 2's complement number. Resolution is approximately 2.9mg/bit.

A shake event will be triggered when high-g values are sensed for a sufficient number of samples.

SHDB: Shake Debounce Register can be set to count from 1 to 63 events before setting the SHAKED bit in the TILT: Status Register. Higher values yield longer evaluation periods. See Figure 14 and Figure 15.

Shake detection can be any combination of axes. To enable detection even when not using interrupts, set the corresponding SHINTX, SHINTY, or SHINTZ bit-fields in the INTEN: Interrupt Enable Register.

| Event | X Axis | | Y Axis | | Z Axis |
|-------|--------|-----|--------|-----|--------|
| Shake | \|X\| > +1.3g ± Threshold | or | \|Y\| > +1.3g ± Threshold | or | \|Z\| > +1.3g ± Threshold |

**Table 23. SHAKE Event Evaluation (Baseline + Offset)**
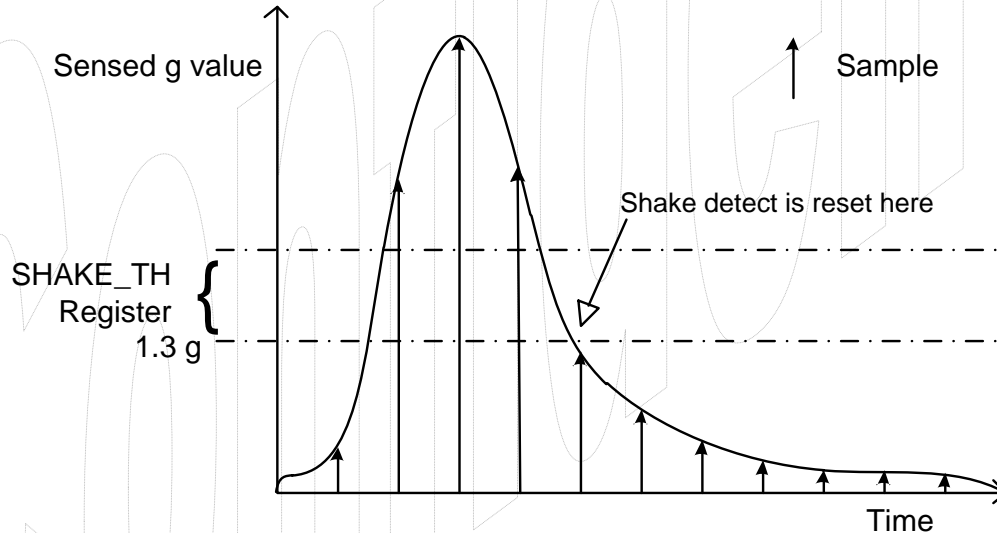


Shake Debounce Register == 4 but the sensed g value is above 1.3g + SHAKE_TH for only 3 samples. Shake event is not detected.

**Figure 14. Example Use of Shake Detection Hardware – Shake Not Detected**
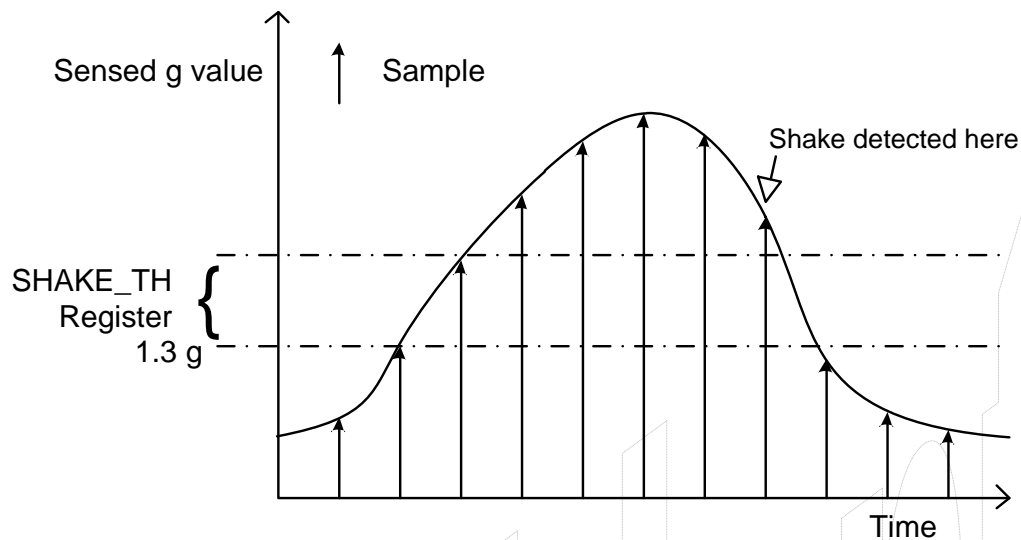
Shake Debounce Register == 4 and the sensed g value is above 1.3g + SHAKE_TH for 5 samples. Shake event is detected.

**Figure 15. Example Use of Shake Detection Hardware – Shake Detected.**

## 9.6  DROP DETECTION

Drop detection is defined as a low-g acceleration applied to all axes. Two modes of drop detection are supported:

> Mode A: Drop detection is a summation of all 3 axes:
>
>> Drop is detected when:
>>
>>> Sum( mag(X) + mag(Y) + mag(Z) ) < 0.5g ± DROP_TH Threshold
>>
>> else Drop not detected;

> Mode B: Drop detection is the logical AND of three comparisons:
>
>> Drop is detected when:
>>
>>> mag(X) < 0.5g ± DROP_TH Threshold and
>>>
>>> mag(Y) < 0.5g ± DROP_TH Threshold and
>>>
>>> mag(Z) < 0.5g ± DROP_TH Threshold
>>
>> else Drop not detected.

The typical drop threshold value is on the order of < 0.5g for all axes. The drop detection range is from 0.125g to 0.872g. The drop debounce value (bit-field DDB in the <u>DROP: Drop Event Control Register</u>) can filter from 1 to 8 consecutive events before setting the drop interrupt.

| Event | X Axis | | Y Axis | | Z Axis |
|---|---|---|---|---|---|
| Drop Mode A | Sum (\|X\| | + | \|Y\| | + | \|Z\|) < 0.5g ± DROP_TH |
| Drop Mode B | \|X\| < 0.5g ± DROP_TH | and | \|Y\| < 0.5g ± DROP_TH | and | \|Z\| < 0.5g ± DROP_TH |

**Table 24. Drop Event Evaluation**

## 9.7  TAP DETECTION

On-chip tap detection hardware allows the device to detect user events such as on-screen button presses. Tap detection can be enabled or disabled on each axis via the TAPEN: Tap Detection Enable Register.

To detect fast, impulse events like a tap, the TAPP: Tap Pulse Register should be written with a tap pulse parameter that sets the maximum number of sample periods that a TAPD event may exceed the threshold before it is ignored by the detection logic. Sensed values that are above the threshold for long periods of time typically do not correspond to tap events.

For example, setting the pulse value to 5 requires that the tap impulse exceed the threshold for at least 1 sample period and up to 5 sample periods. The tap detection hardware is rearmed after the sensed value is below the threshold. See the example in Figure 16 and Figure 17.
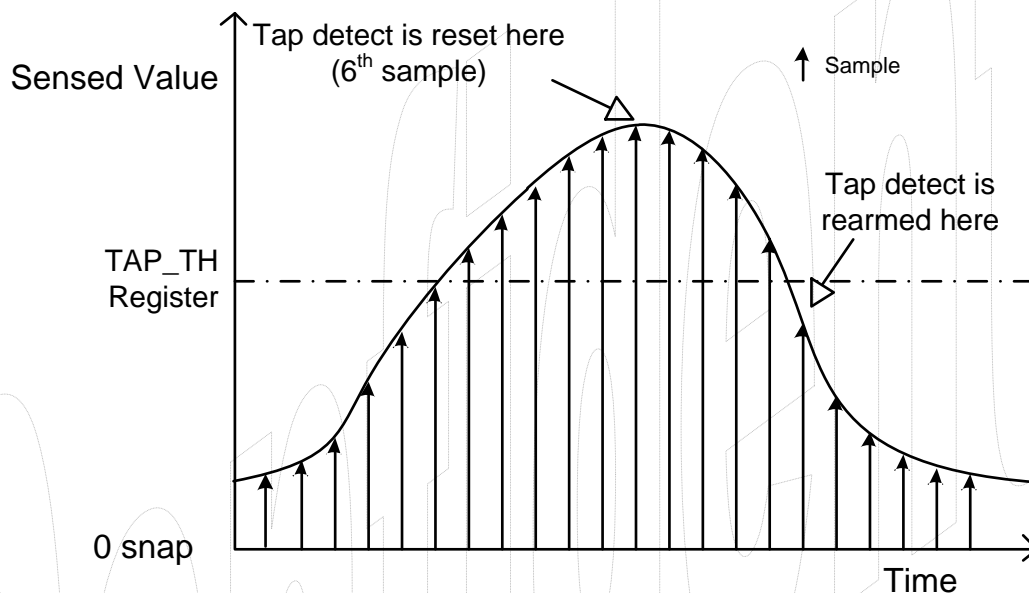


Tap Pulse Register == 5 but the sensed value is above the threshold for 10 samples. No tap is detected.

**Figure 16. Example Use of Tap Detection Hardware – No Tap Detected**
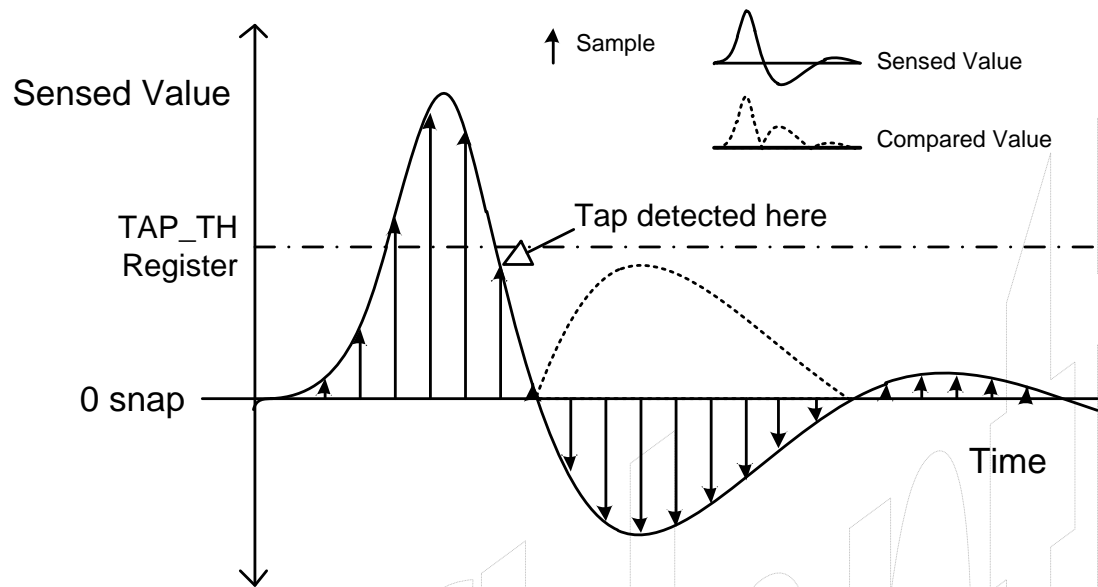
Tap Pulse Register == 5 and the sensed value is above the threshold for 3 samples. Tap is detected.

**Figure 17. Example Use of Tap Detection Hardware – Tap Detected**

The threshold value, set by writing the TAP_TH: Tap Threshold Register, is an 8-bit unsigned number that species the threshold detection level for all tap events. This value is not an offset, but a magnitude which determines the minimum level for a valid tap event.

| Event | X Axis | Y Axis | Z Axis |
|-------|--------|--------|--------|
| Tap | \|X\| > TAP_TH | \|Y\| > TAP_TH | \|Z\| > TAP_TH |

**Table 25. Default Tap Event Evaluation**

## 9.8  CONTINUOUS SAMPLING

The device has the ability to read all sampled readings in a continuous sampling fashion. While sampling, the device updates the XOUT, YOUT, and ZOUT registers at a maximum rate of 128 samples / second, selectable by the SAMPR: Sample Rate Register.

An optional interrupt can be generated each time the sample registers have been updated (GINT interrupt bit in the INTEN: Interrupt Enable Register). See Sections 8.3 and 11.13 for GINT operation and options.

# 10   I2C INTERFACE

## 10.1 PHYSICAL INTERFACE

The I2C slave interface operates at a maximum speed of 400 kHz. The SDA (data) is an open-drain, bi-directional pin and the SCL (clock) is an input pin.

**The device always operates as an I2C slave.**

An I2C master initiates all communication and data transfers and generates the SCL clock that synchronizes the data transfer. The I2C device address is 0x4c (8-bit address 0x98).

The I2C interface remains active as long as power is applied to the DVDD and AVDD pins. In STANDBY state the device responds to I2C read and write cycles, but interrupts cannot be serviced or cleared. All registers can be written in the STANDBY state, but in SNIFF and WAKE only the MODE: Register can be modified.

Internally, the registers which are used to store samples are clocked by the sample clock gated by I2C activity. Therefore, in order to allow the device to collect and present samples in the sample registers at least one I2C STOP condition must be present between samples.

Refer to the I2C specification for a detailed discussion of the protocol.  Per I2C requirements, SDA is an open drain, bi-directional pin. SCL and SDA each require an external pull-up resistor, typically 4.7kΩ. Refer also to Figure 3. Typical Application Circuit.

## 10.2 TIMING

See Section 4.3.3 I2C Timing Characteristics for I2C timing requirements.

## 10.3 I2C MESSAGE FORMAT

The device uses the following general format for writing to the internal registers. The I2C master generates a START condition, and then supplies the device ID, 0x4C or 1001100. The 8th bit is the R/W# flag (write cycle = 0). The device pulls SDA low during the 9th clock cycle indicating a positive ACK. This means, from an 8-bit point of view of an external I2C master, writes should be written to address 0x98 and reads will occur by reading address 0x99.

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.
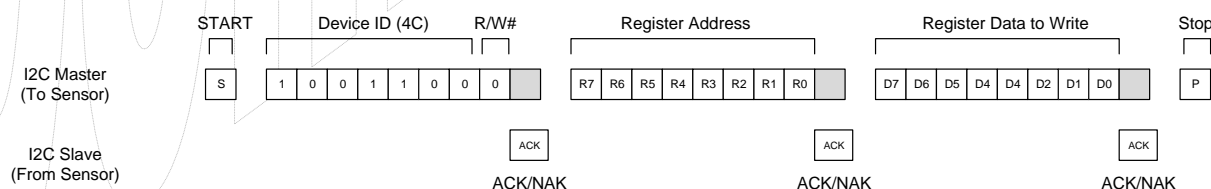


**Figure 18. I2C Message Format, Write Cycle, Single Register Write**

In a read cycle, the I2C master writes the device ID (R/W#=0) and register address to be read. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to '1'. The device shifts out the contents of the register address.
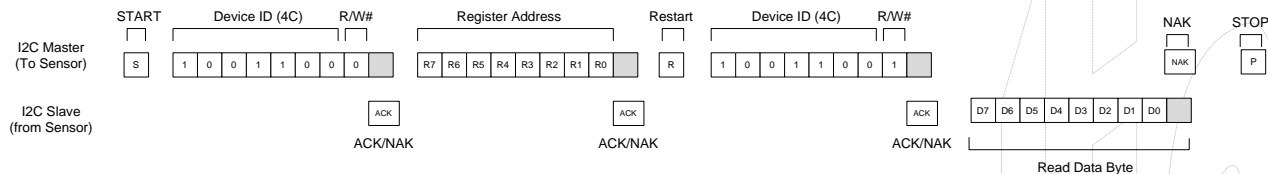


**Figure 19. I2C Message Format, Read Cycle, Single Register Read**

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

**If an I2C burst read operation reads past register address 0x12 the internal address pointer "wraps" to address 0x03 and the contents of the TILT: Status Register are returned.**

# 11   REGISTER INTERFACE

The device has a simple register interface which allows a MCU or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, Bit 0 is the least significant bit (LSB) of a byte register.

Acceleration data is contained in the single-byte per axis <u>XOUT, YOUT & ZOUT: X, Y & Z-Axis Accelerometer Registers</u>.

## 11.1 REGISTER SUMMARY

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W[5] |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|--------|
| 0x00 | XOUT | XOUT Accelerometer Register | XOUT[7] | XOUT[6] | XOUT[5] | XOUT[4] | XOUT[3] | XOUT[2] | XOUT[1] | XOUT[0] | 0x00 | R |
| 0x01 | YOUT | YOUT Accelerometer Register | YOUT[7] | YOUT[6] | YOUT[5] | YOUT[4] | YOUT[3] | YOUT[2] | YOUT[1] | YOUT[0] | 0x00 | R |
| 0x02 | ZOUT | ZOUT Accelerometer Register | ZOUT[7] | ZOUT[6] | ZOUT[5] | ZOUT[4] | ZOUT[3] | ZOUT[2] | ZOUT[1] | ZOUT[0] | 0x00 | R |
| 0x03 | TILT | Tilt Status Register | SHAKED | DROPD | TAPD | POLA[2] | POLA[1] | POLA[0] | BAFR[1] | BAFR[0] | 0x00 | R |
| 0x04 | OPSTAT | Operational State Status Register | OTPA | 0 | Resv[7] | 0 | 0 | 0 | OPSTAT[1] | OPSTAT[0] | 0x03 | R |
| 0x05 | SC | Sleep Counter Register | SC[7] | SC[6] | SC[5] | SC[4] | SC[3] | SC[2] | SC[1] | SC[0] | 0x00 | W |
| 0x06 | INTEN | Interrupt Enable Register | SHINTX | SHINTY | SHINTZ | GINT | ASINT | TINT | PLINT | FBINT | 0x00 | W |
| 0x07 | MODE | Mode Register | IAH | IPP | SCPS | ASE | AWE | 0[6] | OPCON[1] | OPCON[0] | 0x03 | W |
| 0x08 | SAMPR | Sample Rate Register | FILT[2] | FILT[1] | FILT[0] | SNIFFR[1] | SNIFFR[0] | WAKER[2] | WAKER[1] | WAKER[0] | 0x00 | W |
| 0x09 | TAPEN | Tap Detection Enable Register | ZDA | YDA | XDA | Resv[7] | Resv[7] | Resv[7] | Resv[7] | Resv[7] | 0x00 | W |
| 0x0A | TAPP | Tap Pulse Register | Resv[7] | Resv[7] | Resv[7] | Resv[7] | TAPP[3] | TAPP[2] | TAPP[1] | TAPP[0] | 0x00 | W |
| 0x0B | DROP | Drop Event Control Register | DROP_MODE | DINT | Resv[7] | Resv[7] | Resv[7] | DROP_DB[2] | DROP_DB[1] | DROP_DB[0] | 0x00 | W |
| 0x0C | SHDB | Shake Debounce Register | Resv[7] | Resv[7] | SHDB[5] | SHDB[4] | SHDB[3] | SHDB[2] | SHDB[1] | SHDB[0] | 0x00 | W |
| 0x0D-0x17 | | | RESERVED[8] | | | | | | | | | |
| 0x18 | CHIPID | Chip ID Register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0x02 | R |
| 0x19-0x20 | | | RESERVED[8] | | | | | | | | | |
| 0x21 | XOFFL | X-Offset LSB Register | XOFF[7] | XOFF[6] | XOFF[5] | XOFF[4] | XOFF[3] | XOFF[2] | XOFF[1] | XOFF[0] | Per chip | W |
| 0x22 | XOFFH | X-Offset MSB Register | XGAIN[8] | Resv[7] | XOFF[13] | XOFF[12] | XOFF[11] | XOFF[10] | XOFF[9] | XOFF[8] | Per chip | W |
| 0x23 | YOFFL | Y-Offset LSB Register | YOFF[7] | YOFF[6] | YOFF[5] | YOFF[4] | YOFF[3] | YOFF[2] | YOFF[1] | YOFF[0] | Per chip | W |

---

[5] 'R' registers are read-only, via external I2C access. 'W' registers are read-write, via external I2C access.
[6] Software must always write a zero '0' to this bit.
[7] Bits designated as 'Resv' are reserved for future use.
[8] Registers designated as 'RESERVED' should not be accessed by software.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W[5] |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|--------|
| 0x24 | YOFFH | Y-Offset MSB Register | YGAIN[8] | Resv[7] | YOFF[13] | YOFF[12] | YOFF[11] | YOFF[10] | YOFF[9] | YOFF[8] | Per chip | W |
| 0x25 | ZOFFL | Z-Offset LSB Register | ZOFF[7] | ZOFF[6] | ZOFF[5] | ZOFF[4] | ZOFF[3] | ZOFF[2] | ZOFF[1] | ZOFF[0] | Per chip | W |
| 0x26 | ZOFFH | Z-Offset MSB Register | ZGAIN[8] | Resv[7] | ZOFF[13] | ZOFF[12] | ZOFF[11] | ZOFF[10] | ZOFF[9] | ZOFF[8] | Per chip | W |
| 0x27 | XGAIN | X Gain Register | XGAIN[7] | XGAIN[6] | XGAIN[5] | XGAIN[4] | XGAIN[3] | XGAIN[2] | XGAIN[1] | XGAIN[0] | Per chip | W |
| 0x28 | YGAIN | Y Gain Register | YGAIN[7] | YGAIN[6] | YGAIN[5] | YGAIN[4] | YGAIN[3] | YGAIN[2] | YGAIN[1] | YGAIN[0] | Per chip | W |
| 0x29 | ZGAIN | Z Gain Register | ZGAIN[7] | ZGAIN[6] | ZGAIN[5] | ZGAIN[4] | ZGAIN[3] | ZGAIN[2] | ZGAIN[1] | ZGAIN[0] | Per chip | W |
| 0x2A | | RESERVED[8] | | | | | | | | | | |
| 0x2B | SHAKE_TH | Shake Threshold Register | SHAKE_TH[7] | SHAKE_TH[6] | SHAKE_TH[5] | SHAKE_TH[4] | SHAKE_TH[3] | SHAKE_TH[2] | SHAKE_TH[1] | SHAKE_TH[0] | 0x00 | W |
| 0x2C | UD_Z_TH | Up/Down Z Threshold Register | UD_Z_TH[7] | UD_Z_TH[6] | UD_Z_TH[5] | UD_Z_TH[4] | UD_Z_TH[3] | UD_Z_TH[2] | UD_Z_TH[1] | UD_Z_TH[0] | 0x00 | W |
| 0x2D | UD_X_TH | Up/Down X Threshold Register | UD_X_TH[7] | UD_X_TH[6] | UD_X_TH[5] | UD_X_TH[4] | UD_X_TH[3] | UD_X_TH[2] | UD_X_TH[1] | UD_X_TH[0] | 0x00 | W |
| 0x2E | RL_Z_TH | Right/Left Z Threshold Register | RL_Z_TH[7] | RL_Z_TH[6] | RL_Z_TH[5] | RL_Z_TH[4] | RL_Z_TH[3] | RL_Z_TH[2] | RL_Z_TH[1] | RL_Z_TH[0] | 0x00 | W |
| 0x2F | RL_Y_TH | Right/Left Y Threshold Register | RL_Y_TH[7] | RL_Y_TH[6] | RL_Y_TH[5] | RL_Y_TH[4] | RL_Y_TH[3] | RL_Y_TH[2] | RL_Y_TH[1] | RL_Y_TH[0] | 0x00 | W |
| 0x30 | FB_Z_TH | Front/Back Z Threshold Register | FB_Z_TH[7] | FB_Z_TH[6] | FB_Z_TH[5] | FB_Z_TH[4] | FB_Z_TH[3] | FB_Z_TH[2] | FB_Z_TH[1] | FB_Z_TH[0] | 0x00 | W |
| 0x31 | DROP_TH | Drop Threshold Register | DROP_TH[7] | DROP_TH[6] | DROP_TH[5] | DROP_TH[4] | DROP_TH[3] | DROP_TH[2] | DROP_TH[1] | DROP_TH[0] | 0x00 | W |
| 0x32 | TAP_TH | Tap Threshold Register | TAP_TH[7] | TAP_TH[6] | TAP_TH[5] | TAP_TH[4] | TAP_TH[3] | TAP_TH[2] | TAP_TH[1] | TAP_TH[0] | 0x00 | W |
| 0x33 to 0x3A | | RESERVED[8] | | | | | | | | | | |
| 0x3B | PCODE | Product Code | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0x39 | R |
| 0x3C to 0x3F | | RESERVED[8] | | | | | | | | | | |

**Table 26. Register Summary[9]**

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[9] No registers are updated with new event status or samples while a I2C cycle is in process.

## 11.2 XOUT, YOUT & ZOUT: X, Y & Z-AXIS ACCELEROMETER REGISTERS

Accelerometer measurements are stored in the XOUT, YOUT, and ZOUT registers. The measurements are in signed 2's complement format. The range is always ± 1.5g. XOUT[7] is the sign bit. If 6-bit or 7-bit values are desired by a customer application, software should truncate the 8-bit bit-field appropriately.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x00 | XOUT | XOUT Accelerometer Register | XOUT [7] | XOUT [6] | XOUT [5] | XOUT [4] | XOUT [3] | XOUT [2] | XOUT [1] | XOUT [0] | 0x00 | R |
| 0x01 | YOUT | YOUT Accelerometer Register | YOUT [7] | YOUT [6] | YOUT [5] | YOUT [4] | YOUT [3] | YOUT [2] | YOUT [1] | YOUT [0] | 0x00 | R |
| 0x02 | ZOUT | ZOUT Accelerometer Register | ZOUT [7] | ZOUT [6] | ZOUT [5] | ZOUT [4] | ZOUT [3] | ZOUT [2] | ZOUT [1] | ZOUT [0] | 0x00 | R |

**Table 27. Accelerometer Value Registers**

## 11.3 TILT: STATUS REGISTER

This register contains bits which are set when a motion event is detected. Each event has a corresponding interrupt enable which can mask any combination of events. The event detection bits (SHAKED, DROPD, TAPD) remain held until the register is read by the I2C interface. Note that the orientation bit-fields POLA and BAFR are continuously updated (every sample) in the TILT: Status Register and are not held. Note that multiple interrupts may be active at the same time, and so a software routine reading the TILT: Status Register should account for this. Refer to Figure 20. Package Orientation and Figure 21. Package Axis Reference.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x03 | TILT | Tilt Status Register | SHAKED | DROPD | TAPD | POLA [2] | POLA [1] | POLA [0] | BAFR [1] | BAFR [0] | 0x00 | R |

| BAFR[1:0] | Back or Front<br>00: Unknown condition of front or back<br>01: Front – Device is in orientation e in Figure 20. Package Orientation.<br>10: Back – Device is in orientation f in Figure 20. Package Orientation.<br>11: Reserved |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POLA[2:0] | Portrait or Landscape<br>000: Unknown condition of up, down, left or right<br>001: Left – Device is in orientation b in Figure 20. Package Orientation.<br>010: Right – Device is in orientation c in Figure 20. Package Orientation.<br>011: Reserved<br>100: Reserved<br>101: Down – Device is in orientation d in Figure 20. Package Orientation.<br>110: Up – Device is in orientation a in Figure 20. Package Orientation.<br>111: Reserved |
| TAPD | 0: Tap event not detected<br>1: Tap event detected |
| DROPD | 0: Drop event not detected<br>1: Drop event detected |
| SHAKED | 0: Shake event not detected<br>1: Shake event detected |

**Table 28. TILT Status Register Settings**

Top View

Direction of
Earth gravity
acceleration

**a.**

XOUT = +1g
YOUT = 0g
ZOUT = 0g
**TILT = UP**

**b.**

XOUT = 0g
YOUT = -1g
ZOUT = 0g
**TILT = LEFT**

**d.**

XOUT = -1g
YOUT = 0g
ZOUT = 0g
**TILT = DOWN**

Pin 1

**c.**

XOUT = 0g
YOUT = +1g
ZOUT = 0g
**TILT = RIGHT**

Top

Side View

**e.**

XOUT = 0g
YOUT = 0g
ZOUT = +1g
**TILT = FRONT**

**f.**

XOUT = 0g
YOUT = 0g
ZOUT = -1g
**TILT = BACK**

**Figure 20. Package Orientation**

**+Z**

**+Y**

**+X**

**-X**

**-Y**

**-Z**
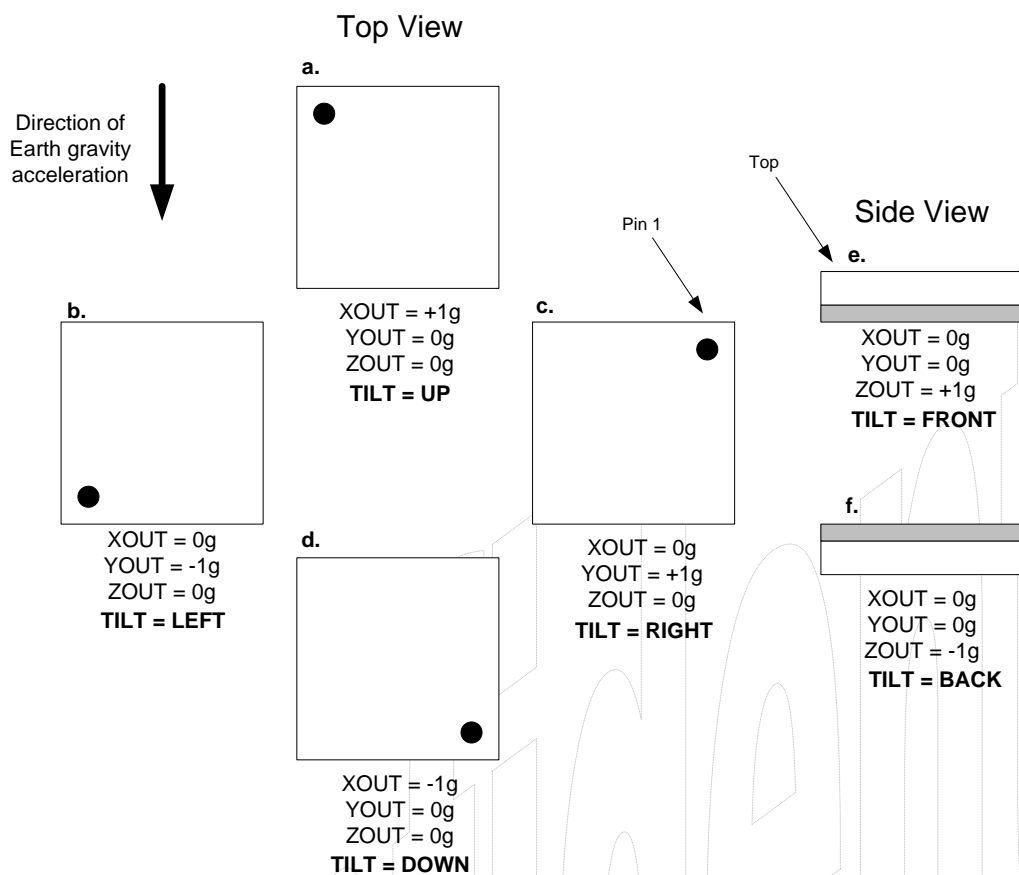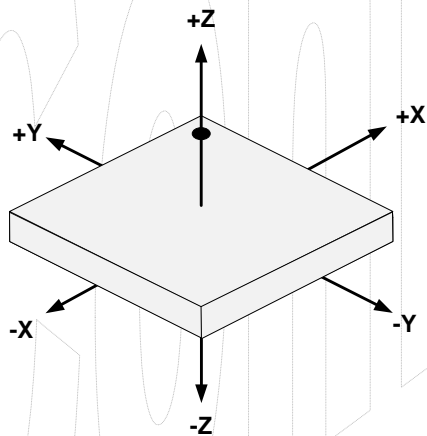
**Figure 21. Package Axis Reference**

## 11.4 OPSTAT: OPERATIONAL STATE STATUS REGISTER

The Operational State status register reports which operational state the device is in, either SNIFF, WAKE or STANDBY as shown in Table 29. Operational State Status Register

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x04 | OPSTAT | Operational State Status Register | OTPA | 0 | Resv | 0 | 0 | 0 | OPSTAT [1] | OPSTAT [0] | 0x03 | R |

| | |
|---|---|
| OPSTAT[1:0] | Sampling State Register Status, Wait State Register Status<br>00: Device is in auto-wake/auto-sniff mode<br>01: Device is in WAKE state, sample rate defined by WAKER[2:0] is active<br>10: Device is in SNIFF state, sample rate defined by SNIFFR[1:0] is active<br>11: Device is in STANDBY state, no sampling |
| Resv | Reserved |
| OTPA | One-time Programming (OTP) activity status<br>0: Internal memory is idle and the device is ready for use<br>1: Internal memory is active and the device is not yet ready for use |

**Table 29. Operational State Status Register**

## 11.5 SC: SLEEP COUNTER REGISTER

If the device is in WAKE state, the sleep counter counts down during periods of inactivity. Inactivity is defined as no detectable motion events as masked by the interrupt enable register. If there are no interrupts during the WAKE state, the sleep counter will timeout.

The sleep counter has two ranges of timeout values. If set, the SCPS prescaler bit in the MODE: Register enables an extended set of timeout values.

If auto-sniff mode (ASE=1) is enabled, the sleep counter decrements if there is no detectable motion during the timeout period. If the sleep counter reaches 0, the device transitions to the SNIFF state. If the auto-wake feature (AWE=1) is enabled, the device remains in the SNIFF state and begins sampling at the reduced sample rate. If AWE=0, the device transitions to the STANDBY state.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x05 | SC | Sleep Counter Register | SC[7] | SC[6] | SC[5] | SC[4] | SC[3] | SC[2] | SC[1] | SC[0] | 0x00 | W |

**Table 30. Sleep Counter Register Settings**

The sleep counter is decremented by the current sampling rate. Table 31 shows the relationship between the current sampling rate and the sleep counter timeout value. All values are approximate.

| WAKER Setting | SCPS = 0 | | SCPS = 1 | |
|---------------|----------|----------|----------|----------|
| | Min (mSec) | Max (sec) | Min (sec) | Max (sec) |
| 1 | 1000 | 256 | 16 | 4096 |
| 2 | 500 | 128 | 8 | 2048 |
| 4 | 250 | 64 | 4 | 1024 |
| 8 | 125 | 32 | 2 | 512 |
| 16 | 62.5 | 16 | 1 | 256 |
| 32 | 31.3 | 8 | 0.5 | 128 |
| 64 | 15.6 | 4 | 0.3 | 64 |
| 128 | 7.8 | 2 | 0.1 | 32 |

**Table 31. Sleep Counter Timeout Settings**

## 11.6 INTEN: INTERRUPT ENABLE REGISTER

The interrupt enable register enables or disables interrupts on various motion or auto-sniff events. If the corresponding interrupt enable bit is set, a matching event will generate an interrupt transition on the external interrupt pin, INTN. To enable the drop interrupt, set the DINT control bit in the DROP: Drop Event Control Register.

When an interrupt is triggered, the first I2C access to the device will clear the external interrupt pin, but the condition (TAPD, SHAKED, DROPD) that generated the interrupt will remain held in the TILT: Status Register until it is read. Note that the orientation bit-fields POLA and BAFR are continuously updated (every sample) in the TILT: Status Register and are not held.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x06 | INTEN | Interrupt Enable Register | SHINTX | SHINTY | SHINTZ | GINT | ASINT | TINT | PLINT | FBINT | 0x00 | W |

| | | |
|---|---|---|
| FBINT | Front / Back Interrupt<br>0: Disable interrupt on front/back position change<br>1: Enable interrupt on front/back position change | |
| PLINT | Portrait / Landscape Interrupt<br>0: Disable interrupt on up/down/left/right position change<br>1: Enable interrupt on up/down/left/right position change | |
| TINT | Tap Interrupt<br>0: Disable interrupt on tap detection<br>1: Enable interrupt on tap detection | |
| ASINT | Auto-Sniff Interrupt<br>0: Disable interrupt on exiting auto-sniff mode<br>1: Enable interrupt on exiting auto-sniff mode | |
| GINT | Generate Interrupt<br>0: Disable automatic interrupt after each measurement<br>1: Enable automatic interrupt after each measurement is updated in XOUT, YOUT, or ZOUT. The interrupt occurs for each measurement, not value change. See Section 8.3. | |
| SHINTX | Shake Interrupt, X-axis<br>0: Disable X-axis interrupt, SHAKED is not set in TILT: Status Register upon event<br>1 : Enable X-axis interrupt, SHAKED is set in TILT: Status Register upon event | |
| SHINTY | Shake Interrupt, Y-axis<br>0: Disable Y-axis interrupt, SHAKED bit is not set in TILT: Status Register upon event<br>1 : Enable Y-axis interrupt, SHAKED bit is set in TILT: Status Register upon event | |
| SHINTZ | Shake Interrupt, Z-axis<br>0: Disable Z-axis interrupt, SHAKED bit is not set in TILT: Status Register upon event<br>1 : Enable Z-axis interrupt, SHAKED bit is set in TILT: Status Register upon event | |

**Table 32. Interrupt Enable Register Settings**

## 11.7 MODE: REGISTER

The MODE register controls the active operating state of the device. This register can be written from any operational state (STANDBY, SNIFF, WAKE). Setting the OPCON bits to 00 allows the device to operate in auto-wake/sniff mode and automatically transition between WAKE and SNIFF when auto-wake (AWE) and auto-sniff (ASE) are enabled.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x07 | MODE | Mode Register | IAH | IPP | SCPS | ASE | AWE | 0* | OPCON [1] | OPCON [0] | 0x03 | W |

**NOTE\*: Software must always write a zero '0' to Bit 2.**

| | | |
|---|---|---|
| OPCON [1:0] | 00: Operate using the automatic auto-wake/auto-sniff settings. The device automatically transitions between WAKE and SNIFF states based upon events or timeouts. | Set Device Operational State. WAKE, SNIFF or STANDBY |
| | 01: Move to WAKE state and remain there | |
| | 10: Move to SNIFF state and remain there | |
| | 11: Move to STANDBY state and remain there (STANDBY is the default POR state) | |
| AWE | 0: Disable auto-wake | **Auto Wake Enable**. The device uses the samples per second specified by the SNIFFR bit-field. When the device exits the SNIFF state and moves to the WAKE state (AWE=1) an interrupt can occur and the device will switch to the samples per second specified by WAKER bit-field. The AWE bit also determines if the device transitions from the STANDBY state to the SNIFF state |
| | 1: Enable auto-wake | |
| ASE | 0: Disable auto-sniff | **Auto Sniff Enable.** The device uses the sample rate specified in the WAKER bit-field. When the device exits the WAKE state through a sleep counter timeout, it will switch to the sample rate specified by the SNIFFR bit-field if AWE = 1. If AWE = 0, the device transitions from the SNIFF state to STANDBY. If ASE=0, device will remain in the WAKE state and not transition to SNIFF or STANDBY |
| | 1: Enable auto-sniff | |
| SCPS | 0: Sleep counter prescaler is divide-by-1 | Sleep Counter Prescaler This bit is the sleep counter prescaler enable. If the bit is '1', the sleep counter timeout is 16 times larger. |
| | 1: Sleep counter prescaler is divide-by-16 (enable long range sleep counts) | |
| IPP | 0: Interrupt pin INTN is open drain (default) and requires an external pull-up to AVDD. | Interrupt Push Pull |
| | 1: Interrupt pin INTN is push-pull. No external pull-up resistor should be installed. | |
| IAH | 0: Interrupt pin INTN is active low | Interrupt Active High |
| | 1: Interrupt pin INTN is active high | |

**Table 33. Mode Register Functionality**

## 11.8 SAMPR: SAMPLE RATE REGISTER

This register sets the sample rate during the WAKE and SNIFF states. The WAKE state sample rate is set in bit-field WAKER and the SNIFF state rate is set in bit-field SNIFFR. Measurements are updated to the XOUT, YOUT, and ZOUT registers at the specified sample rate. For tap detection, it is recommended to set the WAKER register to the maximum 128 samples/second.

The contents of XOUT, YOUT, and ZOUT are updated continuously with new sample data regardless of whether or not their values have been read out over the I2C interface.

If the auto-wake feature (AWE=1 in the MODE: Register) is enabled, the device will continue to look for motion events while in the SNIFF state, but at a reduced sample rate. The following table shows the possible reduced sample rate values. Note that the auto-wake bit must be enabled for the reduced sample rate to take affect while the device is dozing.

The FILT bit-field provides an event filter can be used to identify when anywhere from 2 to 8 samples match the orientation before detection is valid for portrait / landscape orientation changes.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x08 | SAMPR | Sample Rate Register | FILT [2] | FILT [1] | FILT [0] | SNIFFR [1] | SNIFFR [0] | WAKER [2] | WAKER [1] | WAKER [0] | 0x00 | W |

| WAKER [2:0] | WAKE Sample Rate (Samples/Second) |
|-------------|-----------------------------------|
| 000 | 128 |
| 001 | 64 |
| 010 | 32 |
| 011 | 16 |
| 100 | 8 |
| 101 | 4 |
| 110 | 2 |
| 111 | 1 |

| SNIFFR [1:0] | SNIFF Sample Rate (Samples/Second) |
|--------------|------------------------------------|
| 00 | 32 |
| 01 | 16 |
| 10 | 8 |
| 11 | 1 |

**Table 34. Wake/Sniff Sample Rate Settings**

The FILT bit-field allows for the debouncing of portrait/landscape events as reported in the TILT: Status Register. The POLA bit-field in the TILT: Status Register must match for the specified number of sample periods in the FILT bit-field before the POLA bit-field in the TILT: Status Register is updated, noting that a change in orientation was detected.

| FILT[2:0] | Tilt Debounce Matching Samples (n) | Description |
|---|---|---|
| 000 | n/a | Tilt debounce filtering is disabled. The device updates portrait/landscape status at every sample, at the rate set by bit-fields WAKER or SNIFFR. |
| 001 | 2 | Event Filter<br>'n' measurement samples at the rate set by WAKER or SNIFFR must match before the device updates the portrait/landscape status in the TILT: Status Register. |
| 010 | 3 | |
| 011 | 4 | |
| 100 | 5 | |
| 101 | 6 | |
| 110 | 7 | |
| 111 | 8 | |

**Table 35. Tilt Debounce Filter Settings**

## 11.9 TAPEN: TAP DETECTION ENABLE REGISTER

This register allows individual tap/pulse detection on each axis. Setting XDA, YDA, or ZDA adds the corresponding axis to tap event detection. See also Section 9.7 Tap Detection.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x09 | TAPEN | Tap Detection Enable Register | ZDA | YDA | XDA | Resv | Resv | Resv | Resv | Resv | 0x00 | W |

| | | |
|---|---|---|
| XDA | 0: Disable Tap  detection on X-axis<br>1: Enable Tap detection on X-axis | |
| YDA | 0: Disable Tap detection on Y-axis<br>1: Enable Tap detection on Y-axis | |
| ZDA | 0: Disable Tap detection on Z-axis<br>1: Enable Tap detection on Z-axis | |

**Table 36. TAPEN Register Settings**

## 11.10 TAPP: TAP PULSE REGISTER

This value sets the number of samples for which a tap pulse must exceed the TAP_TH threshold before it is rejected as not a tap event. If the values detected by the sensor exceed the TAP_TH threshold for longer than the reject count, no tap event is detected and the interrupt is not set. See also Section 9.7 Tap Detection.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x0A | TAPP | TAP Pulse Register | Resv | Resv | Resv | Resv | TAPP [3] | TAPP [2] | TAPP [1] | TAPP [0] | 0x00 | W |

| TAPP [3:0] | Tap Detection Sample Periods (n) | Description |
|------------|----------------------------------|-------------|
| 0x0 | 1 | This tap detection filtering requires the sensed values to exceed the TAP_TH threshold level for at least 1 sample and less than n sample periods. When they have, the sensor will set TAPD bit in the TILT: Status Register. In addition, if the TINT tap interrupt is enabled in the INTEN: Interrupt Enable Register then an interrupt will be generated by the device. |
| 0x1 | 2 | |
| 0x2 | 3 | |
| 0x3 | 4 | |
| … | 5 ≤ n ≤ 15 | |
| 0xF | 16 | |

**Table 37. TAPP Tap Pulse Register Settings**

## 11.11 DROP: DROP EVENT CONTROL REGISTER

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x0B | DROP | Drop Event Control Register | DROP_ MODE | DINT | Resv | Resv | Resv | DROP_ DB[2] | DROP_ DB[1] | DROP_ DB[0] | 0x00 | W |

| | | |
|---|---|---|
| DROP_DB[2:0] | Drop Debounce<br>000: 1 drop event<br>001: 2 adjacent drop events<br>010: 3 adjacent drop events<br> … : 4 ≤ n ≤ 7 adjacent drop events<br>111: 8 adjacent drop events | Drop event debounce value, the number of drop events detected must reach this count for the final event to be valid. |
| DINT | Drop Interrupt<br>0: Disable drop event interrupt<br>1: Enable drop event interrupt | The DROPD bit in the TILT: Status Register will be set upon event occurrence regardless of this bit setting. |
| DROP_MODE | Drop Mode<br>0: Mode A: Drop detection is a summation of all 3 axes:<br>    Drop is detected when:<br>       Sum( mag(X) + mag(Y) +  mag(Z) ) < 0.5g ± DROP_TH Threshold<br>     else Drop not detected;<br><br>1: Mode B: Drop detection is the logical AND of three comparisons:<br>    Drop is detected when:<br>       mag(X) < 0.5g ± DROP_TH Threshold and<br>       mag(Y) < 0.5g ± DROP_TH Threshold and<br>       mag(Z) < 0.5g ± DROP_TH Threshold<br>    else Drop not detected. | |

**Table 38. Drop Event Control Register Settings**

## 11.12 SHDB: SHAKE DEBOUNCE REGISTER

The shake debounce register allows a 1 to 63 event count to be required before a valid shake event is detected or an interrupt is generated. The debounce value applies to all 3-axes.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x0C | SHDB | Shake Debounce Register | Resv | Resv | SHDB [5] | SHDB [4] | SHDB [3] | SHDB [2] | SHDB [1] | SHDB [0] | 0x00 | W |

| SHDB[5:0] | Adjacent Shake Events (n) | Description |
|-----------|---------------------------|-------------|
| 0x01 | 1 | Shake detection debounce filtering requires n adjacent shake detection events in order to trigger a shake event and set the SHAKED bit in the <u>TILT: Status Register</u>. In addition, if the SHINTX, SHINTY or SHINTZ bits are set in the <u>INTEN: Interrupt Enable Register</u> and that event occurs, then an interrupt will be generated by the device. |
| 0x02 | 2 | |
| 0x03 | 3 | |
| …. | 4 ≤ n ≤ 62 | |
| 0x3F | 63 | |

**Table 39. SH_DB Shake Debounce Register Settings**

## 11.13 CHIPID: CHIP IDENTIFICATION REGISTER

This register returns 0x02.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x18 | CHIPID | Chip ID Register | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0x02 | R |

## 11.14 X-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 14-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x21 | XOFFL | X-Offset LSB Register | XOFF[7] | XOFF[6] | XOFF[5] | XOFF[4] | XOFF[3] | XOFF[2] | XOFF[1] | XOFF[0] | Per chip | W |
| 0x22 | XOFFH | X-Offset MSB Register | XGAIN[8] | Resv | XOFF[13] | XOFF[12] | XOFF[11] | XOFF[10] | XOFF[9] | XOFF[8] | Per chip | W |

## 11.15 Y-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 14-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x23 | YOFFL | Y-Offset LSB Register | YOFF[7] | YOFF[6] | YOFF[5] | YOFF[4] | YOFF[3] | YOFF[2] | YOFF[1] | YOFF[0] | Per chip | W |
| 0x24 | YOFFH | Y-Offset MSB Register | YGAIN[8] | Resv | YOFF[13] | YOFF[12] | YOFF[11] | YOFF[10] | YOFF[9] | YOFF[8] | Per chip | W |

## 11.16 Z-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 14-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x25 | ZOFFL | Z-Offset LSB Register | ZOFF[7] | ZOFF[6] | ZOFF[5] | ZOFF[4] | ZOFF[3] | ZOFF[2] | ZOFF[1] | ZOFF[0] | Per chip | W |
| 0x26 | ZOFFH | Z-Offset MSB Register | ZGAIN[8] | Resv | ZOFF[13] | ZOFF[12] | ZOFF[11] | ZOFF[10] | ZOFF[9] | ZOFF[8] | Per chip | W |

## 11.17 X-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x22 | XOFFH | X-Offset MSB Register | **XGAIN[8]** | Resv | XOFF[13] | XOFF[12] | XOFF[11] | XOFF[10] | XOFF[9] | XOFF[8] | Per chip | W |
| 0x27 | XGAIN | X Gain Register | **XGAIN[7]** | **XGAIN[6]** | **XGAIN[5]** | **XGAIN[4]** | **XGAIN[3]** | **XGAIN[2]** | **XGAIN[1]** | **XGAIN[0]** | Per chip | W |

## 11.18 Y-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x24 | YOFFH | Y-Offset MSB Register | **YGAIN[8]** | Resv | YOFF[13] | YOFF[12] | YOFF[11] | YOFF[10] | YOFF[9] | YOFF[8] | Per chip | W |
| 0x28 | YGAIN | Y Gain Register | **YGAIN[7]** | **YGAIN[6]** | **YGAIN[5]** | **YGAIN[4]** | **YGAIN[3]** | **YGAIN[2]** | **YGAIN[1]** | **YGAIN[0]** | Per chip | W |

## 11.19 Z-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

**NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.**

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x26 | ZOFFH | Z-Offset MSB Register | ZGAIN[8] | Resv | ZOFF[13] | ZOFF[12] | ZOFF[11] | ZOFF[10] | ZOFF[9] | ZOFF[8] | Per chip | W |
| 0x29 | ZGAIN | Z Gain Register | ZGAIN[7] | ZGAIN[6] | ZGAIN[5] | ZGAIN[4] | ZGAIN[3] | ZGAIN[2] | ZGAIN[1] | ZGAIN[0] | Per chip | W |

## 11.20 SHAKE_TH: SHAKE THRESHOLD REGISTER

SHAKE_TH has a baseline value of 1.3g plus a threshold, SHAKE_TH. The shake threshold can range from 0.925g to 1.672g. The value is an 8-bit signed 2's complement number. The resolution is approximately 2.9mg/bit. See also Section 9.5 Shake Detection.

Shake Event =    ( mag(X) > 1.3g + SHAKE_TH ) or

( mag(Y) > 1.3g + SHAKE_TH ) or

( mag(Z) > 1.3g + SHAKE_TH )

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x2B | SHAKE_TH | Shake Threshold Register | Signed 2's complement value | | | | | | | | 0x00 | W |

| SHAKE_TH[7:0] | Description (~2.9mg/LSB) |
|---------------|--------------------------|
| 0x80 | Shake threshold is 0.925g |
| 0x00 | Shake threshold is 1.3g |
| 0x7F | Shake threshold is 1.672g |

**Table 40. SHAKE_TH Threshold Register Settings**

## 11.21 UD_Z_TH: UP/DOWN Z AXIS THRESHOLD REGISTER

The threshold value, UD_Z_TH[7:0] is an 8-bit signed 2's complement number that can range from 0.425g to 1.172g, for determination of the POLA orientation bits. The resolution is approximately 2.9mg/bit. See also Section 9.3 Portrait/Landscape.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x2C | UD_Z_TH | Up/Down Z Axis Threshold Register | | | | Signed 2's complement value | | | | | 0x00 | W |

| UD_Z_TH[7:0] | Description (~2.9mg/LSB) |
|--------------|--------------------------|
| 0x80 | Up/down Z axis threshold is 0.425g |
| 0x00 | Up/down Z axis threshold is 0.8g |
| 0x7F | Up/down Z axis threshold is 1.172g |

**Table 41. Up/Down Z-axis Threshold Register Settings**

## 11.22 UD_X_TH: UP/DOWN X AXIS THRESHOLD REGISTER

This 8-bit unsigned value is an offset that is added to the magnitude of the X-axis accelerometer measurement. The range of the offset is 0g to 0.747g; the resolution is approximately 2.9mg/bit. See also Section 9.3 Portrait/Landscape.

Increasing this value in conjunction with the RL_Y_TH: Right/Left Y Axis Threshold Register widens the deadband in portrait /landscape detection.

For most applications, the same value should be written to both registers.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x2D | UD_X_TH | Up/Down X Axis Threshold Register | | | | Unsigned value | | | | | 0x00 | W |

| UD_X_TH[7:0] | Description (~2.9mg/LSB) |
|--------------|--------------------------|
| 0x00 | Up/down X threshold offset is 0g |
| 0xFF | Up/down X threshold offset is +0.747g |

**Table 42. Up/Down X-axis Threshold Register Settings**

## 11.23 RL_Z_TH: RIGHT/LEFT Z AXIS THRESHOLD REGISTER

The threshold value, RL_Z_TH[7:0] is an 8-bit signed 2's complement number that can range from 0.425g to 1.172g, for determination of the POLA orientation bits. The resolution is approximately 2.9mg/bit. See also Section 9.3 Portrait/Landscape.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x2E | RL_Z_TH | Right/Left Z Axis Threshold Register | | | | Signed 2's complement value | | | | | 0x00 | W |

| RL_Z_TH[7:0] | Description (~2.9mg/LSB) |
|--------------|--------------------------|
| 0x80 | Right/left Z axis threshold is 0.425g |
| 0x00 | Right/left Z axis threshold is 0.8g |
| 0x7F | Right/left Z axis threshold is 1.172g |

**Table 43. Right/Left Z-axis Threshold Register Settings**

## 11.24 RL_Y_TH: RIGHT/LEFT Y AXIS THRESHOLD REGISTER

This 8-bit unsigned value is an offset this is added to the magnitude of the Y-axis accelerometer measurement. The range of the offset is 0g to 0.747g; the resolution is approximately 2.9mg/bit. See also Section 9.3 Portrait/Landscape.

Increasing this value in conjunction with the UD_X_TH: Up/Down X Axis Threshold Register widens the dead-band in portrait /landscape detection.

For most applications, the same value should be written to both registers.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x2F | RL_Y_TH | Right/Left Y Axis Threshold Register | | | | Unsigned value | | | | | 0x00 | W |

| RL_Y_TH[7:0] | Description (~2.9mg/LSB) |
|--------------|--------------------------|
| 0x00 | Right/left Y-axis threshold offset is 0g |
| 0xFF | Right/left Y-axis threshold offset is +0.747g |

**Table 44. Right/Left Y-axis Threshold Register Settings**

## 11.25 FB_Z_TH: FRONT/BACK Z AXIS THRESHOLD REGISTER

The threshold value, FB_Z_TH[7:0] is an 8-bit unsigned number that adds up to + 0.373g to the baseline detection level of 0.174g, in increments of approximately 1.46mg/LSB. Increasing the threshold value increases the hysteresis of the front/back detection level. See also Section 9.4 Front/Back.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x30 | FB_Z_TH | Front/Back Z Axis Threshold Register | | | | Unsigned value | | | | | 0x00 | W |

| FB_Z_TH[7:0] | Description (~1.46mg/LSB) |
|--------------|---------------------------|
| 0x00 | Front/back Z threshold is 0.174g |
| 0xFF | Front/back Z threshold is 0.547g |

**Table 45. Front/Back Z-axis Threshold Register Settings**

## 11.26 DROP_TH: DROP THRESHOLD REGISTER

The threshold value, DROP_TH[7:0] is an 8-bit signed 2's complement number that adjusts the drop-detection baseline detection level of 0.5g. See also Section 9.6 Drop Detection.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x31 | DROP_TH | Drop Threshold Register | | | | Signed 2's complement value | | | | | 0x00 | W |

| DROP_TH[7:0] | Description (~2.9mg/LSB) |
|--------------|--------------------------|
| 0x80 | Drop threshold is 0.125g |
| 0x00 | Drop threshold is 0.5g |
| 0x7F | Drop threshold is 0.872g |

**Table 46. Drop Threshold Register Settings**

## 11.27 TAP_TH: TAP THRESHOLD REGISTER

The threshold value, TAP_TH[7:0] is an 8-bit unsigned number that species the threshold detection level for all tap events. This value is not an offset, but a magnitude which determines the minimum level for a valid tap event. The detector is implemented as a $2^{nd}$-order high pass filter. As such, the units are the $2^{nd}$ derivative of acceleration, also known as 'snap'. The full range is 0 to 12 snap. The resolution is ~47 milliSnap/bit. See also Section 9.7 Tap Detection.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x32 | TAP_TH | Tap Threshold Register | | | | Unsigned value | | | | | 0x00 | W |

| TAP_TH[7:0] | Description (~47 mSnap/LSB) |
|-------------|------------------------------|
| 0x00 | Tap threshold is 0 snap |
| 0x80 | Tap threshold is 6 snap |
| 0xFF | Tap threshold is 12 snap |

**Table 47. TAP_TH Tap Threshold Register Settings**

## 11.28 PCODE: PRODUCT CODE

This register returns a value specific to the part number of this mCube device, noted below.

| Addr | Name | Description | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | POR Value | R/W |
|------|------|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----------|-----|
| 0x3B | PCODE | Product Code Register | | | | | 0x39 | | | | 0x39 | R |

# 12   EXAMPLE MC3430 CONFIGURATION

This section shows some example configurations, for demonstration purposes. The sequences are described as register read and write cycles; the I2C device ID and protocol are implied.

## 12.1 EXAMPLE: TAP DEMO

| Sequence | Register | Data to Write | Comments |
|---|---|---|---|
| 1 | 0x07 | 0x43 | Go to STANDBY state, configure INTN pin, active low (IAH = 0), active drive (IPP = 1) |
| 2 | 0x05 | 0x00 | Sleep Counter is 0 |
| 3 | 0x08 | 0x00 | Sample rate is continuous, 128 samples/sec |
| 4 | 0x09 | 0x80 | Enable Tap detection on Z-axis |
| 5 | 0x0B | 0x00 | Set drop mode A, no debounce, no drop interrupt |
| 6 | 0x31 | 0x80 | Set a very low drop threshold (to avoid frequent drop detection) |
| 7 | 0x0A | 0x03 | Tap detected for pulses > Tap threshold and for 4 or fewer sample periods |
| 8 | 0x32 | 0x5C | Tap threshold set to ~4.3 snap |
| 9 | 0x06 | 0x04 | Enable Tap interrupt, disable others |
| 10 | 0x07 | 0x41 | Go to WAKE state, enable sampling, configure INTN pin, active low (IAH = 0), active drive (IPP = 1) |

**Table 48. Tap Demo Register Sequence**

To observe the demo:

–   Write the registers as shown above.

–   Tap the device in the Z-direction

–   Observe the interrupt trigger

–   Read TILT: Status Register to reset the Tap interrupt

–   Tap the device in the X and Y directions

–   Observer no interrupt triggers

## 12.2 EXAMPLE: GINT INTERRUPT WITH AUTO-WAKE AND AUTO-SNIFF ENABLED

| Sequence | Register | Data to Write | Comments |
|----------|----------|---------------|----------|
| 1 | 0x07 | 0x43 | Go to STANDBY state<br>Disable auto-wake / auto-sniff<br>Configure INTN pin, active low (IAH = 0), active drive (IPP = 1)<br>Set Sleep Counter prescaler to divide by 1 (SCPS = 0) |
| 2 | 0x08 | 0x12 | Set:<br>Sniff state sample rate to 8 samples/second<br>Wake state sample rate to 32 samples/second |
| 3 | 0x06 | 0x11 | Enable GINT and FBINT interrupt bits (continuous sample interrupt and FRONT/BACK interrupt) |
| 4 | 0x05 | 0xFF | Set the SC sleep counter timeout:<br>Set to 8 seconds, because SCPS = 0 and SC = 0xFF, which is the maximum, from Table 31. |
| 5 | 0x07 | 0x41 | Go to Wake state |
| 6 | 0x07 | 0x58 | Allow state to change via auto-wake/sniff (AWE = 1, ASE = 1) and maintain other settings |

**Table 49. GINT Interrupt Register Sequence**

To run the demo:

–  Read X, Y, Z registers (0x00, 0x01, 0x02) on every INT pin assertion. A fast ISR (interrupt service routine) is recommended, faster than 32 reads / second.

–  Lay the board flat on a surface. Observe the switch to slower sample rate (8Hz) after approximately 8 seconds of inactivity by observing the INT signal on an oscilloscope.

–  Flip the device over (z axis) and observe an immediate exit from sniff state to wake state. This may be observed by viewing GINT on scope or reading the OPSTAT: Operational State Status Register in real time.

# 13   INDEX OF TABLES

# 14   REVISION HISTORY

| Date | Revision | Description |
| --- | --- | --- |
| 2012-03 | APS-048-0011v1.0 | First release. |
| 2012-10 | APS-048-0011v1.1 | Changed device orientation pictures. Change PCODE. Updated current specs. Clarified text in tables, gain registers and footnotes. |
| 2013-03 | APS-048-0011v1.2 | Add Tape and Reel info. |
|  |  |  |

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