GENERAL DESCRIPTION

The MC3433 is a low-noise, integrated digital output 3-axis accelerometer with a feature set optimized for cell phones and consumer product motion sensing. Applications include user interface control, gaming motion input, electronic compass tilt compensation for cell phones, game controllers, remote controls and portable media products.

Low noise and low power are inherent in the monolithic fabrication approach, where the MEMS accelerometer is integrated in a single-chip with the electronics integrated circuit.

In the MC3433 the internal sample rate can be set from 0.1 to 128 samples / second. The device supports the reading of sample and event status via polling or interrupts.

FEATURES

Range, Sampling & Power

- ± 2g range
- 6,7, or 8-bit resolution
- 0.1 to 128 samples/sec
- 200 µA typical active current

Simple System Integration

- I2C interface, up to 400 kHz
- 2 × 2 × 0.92 mm 12-pin package
  - Pin-compatible to Bosch BMA2xx
- Single-chip 3D silicon MEMS

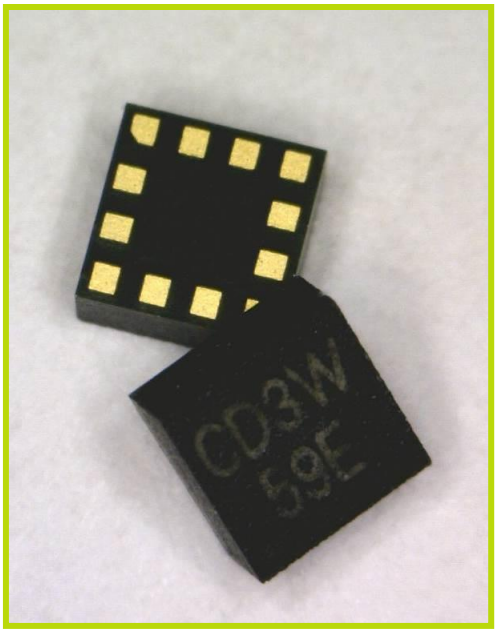


TABLE OF CONTENTS

1 ORDER INFORMATION

Part Number	Resolution	Order Number	Package	Shipping
MC3433	8-bit	MC3433-I5	VLGA-12	Tape & Reel, 5Ku

Table 1. Order Information

2 FUNCTIONAL BLOCK DIAGRAM

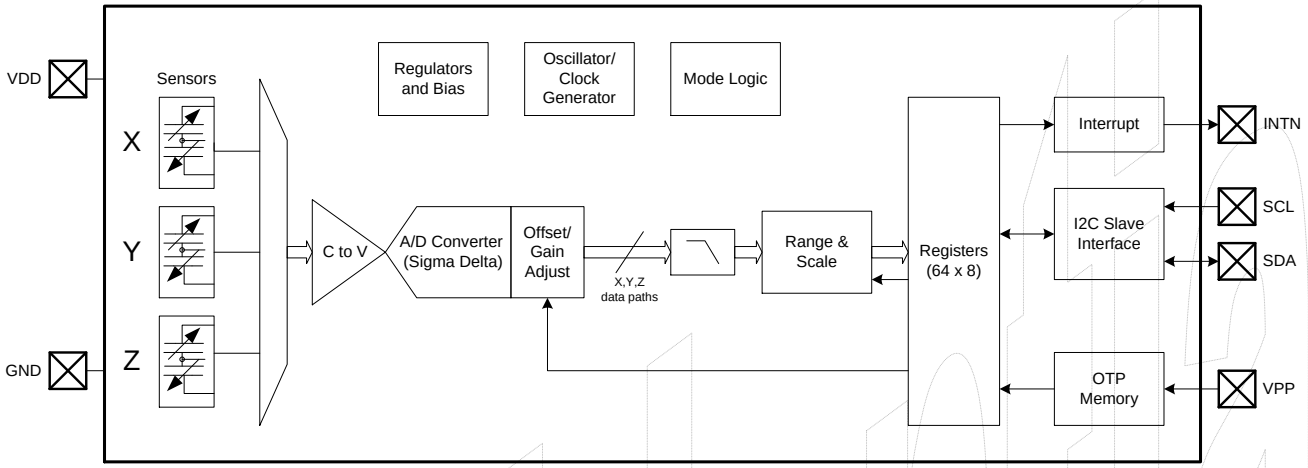
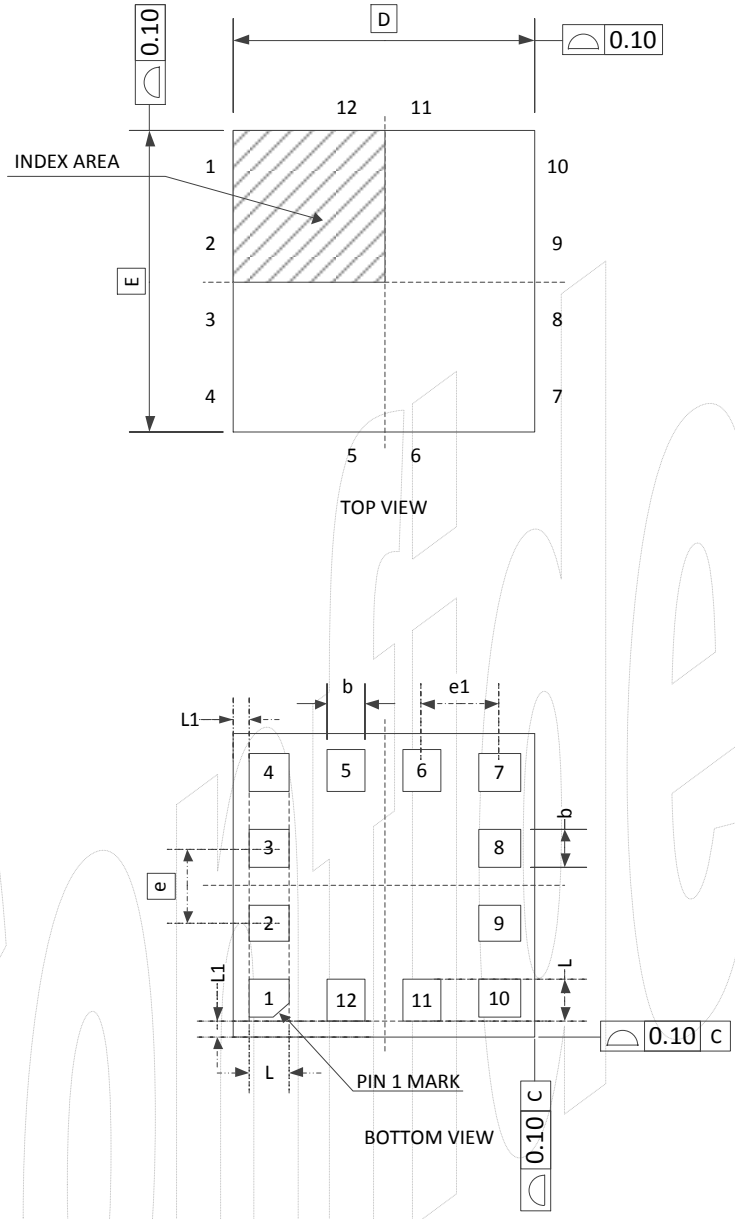


Figure 1. Block Diagram

3 PACKAGING AND PIN DESCRIPTION

3.1 PACKAGE OUTLINE



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.85	0.92	1.00
D		2.00 BSC	
E		2.00 BSC	
e		0.5 BSC	
e1		0.5125 REF	
b	0.20	0.25	0.30
L1	0.05	0.10	0.15
L	0.225	0.275	0.325

Figure 2. Package Outline and Mechanical Dimensions

3.2 PACKAGE ORIENTATION

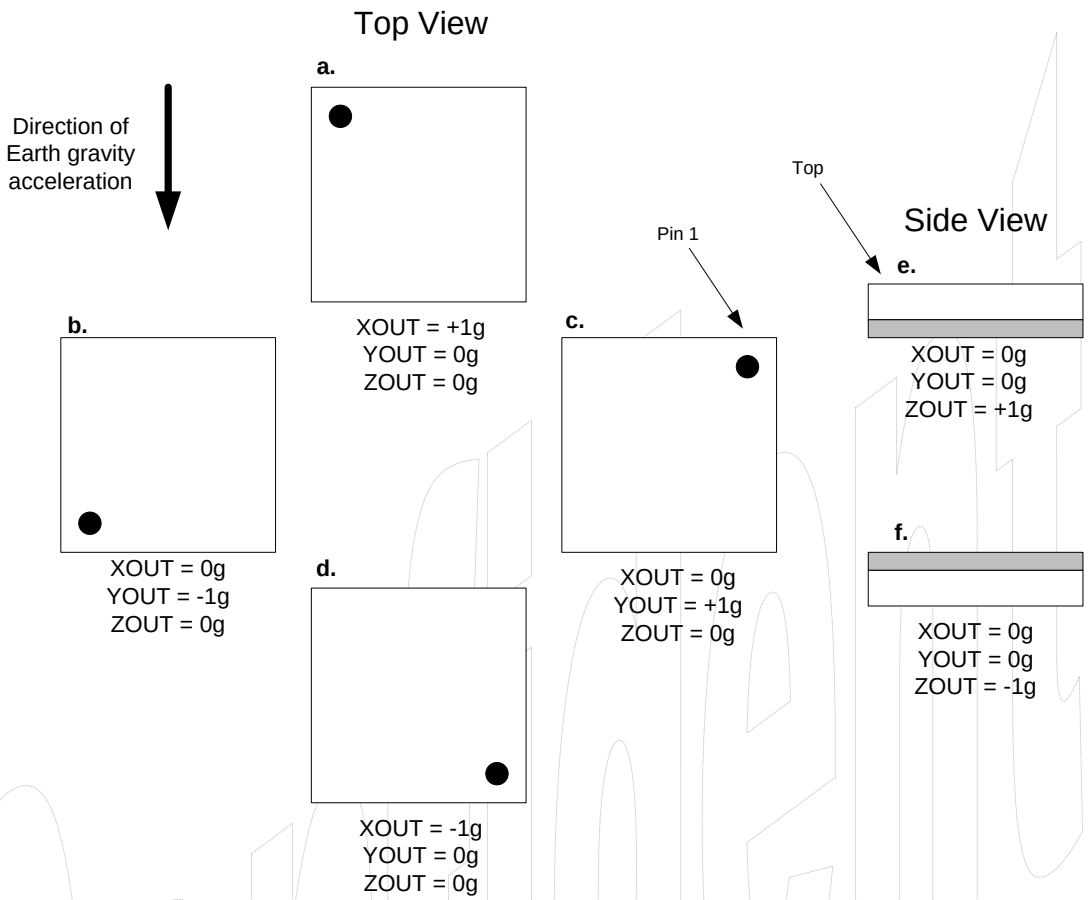


Figure 3. Package Orientation

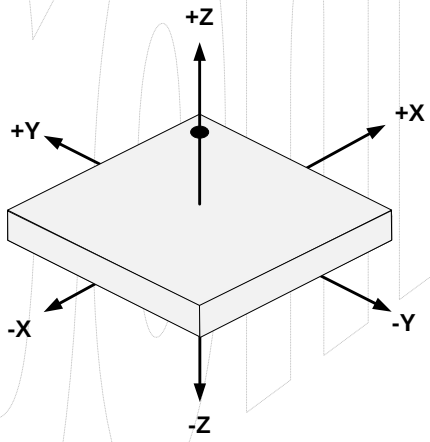


Figure 4. Package Axis Reference

3.3 PIN DESCRIPTION

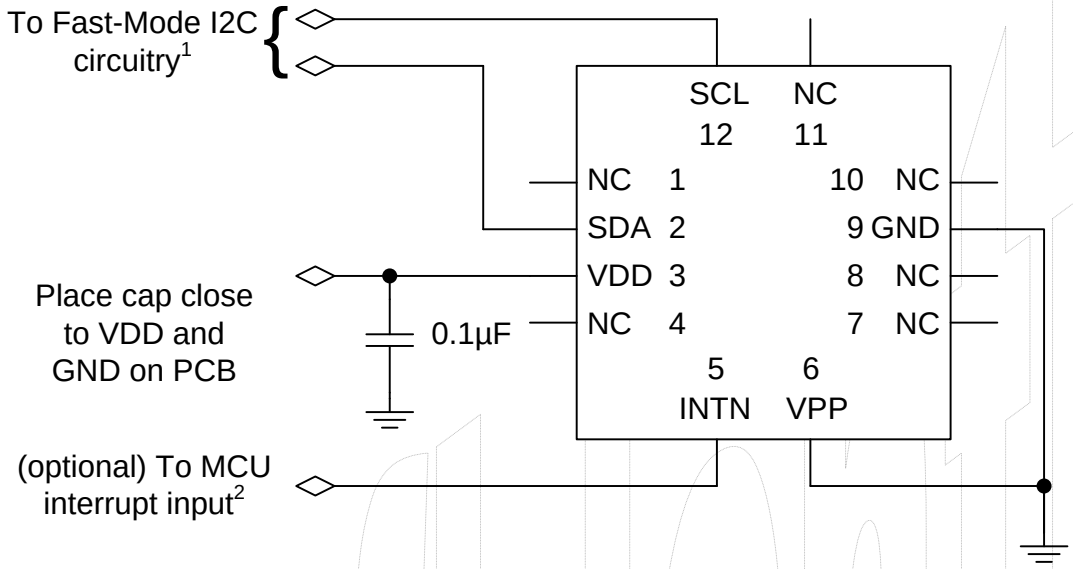
Pin	Name	Function
1	NC	No connect
2	SDA [1]	I2C serial data input/output
3	VDD	Power supply
4	NC	No connect
5	INTN [2]	Interrupt active LOW [3]
6	VPP	Connect to GND
7	NC	No Connect
8	NC	No Connect
9	GND	Ground
10	NC	No Connect
11	NC	No connect
12	SCL [1]	I2C serial clock input

Table 2. Pin Description

Notes:

1) This pin requires a pull-up resistor, typically 4.7kΩ to VDD. Refer to I2C Specification for Fast-Mode devices. Higher resistance values can be used (typically done to reduce current leakage) but such applications are outside the scope of this datasheet.
2) This pin can be configured by software to operate either as an open-drain output or push-pull output (MODE Register). If set to open-drain, then it requires a pull-up resistor, typically 4.7kΩ to VDD.
3) INTN pin polarity is programmable in the MODE Register.

3.4 TYPICAL APPLICATION CIRCUIT



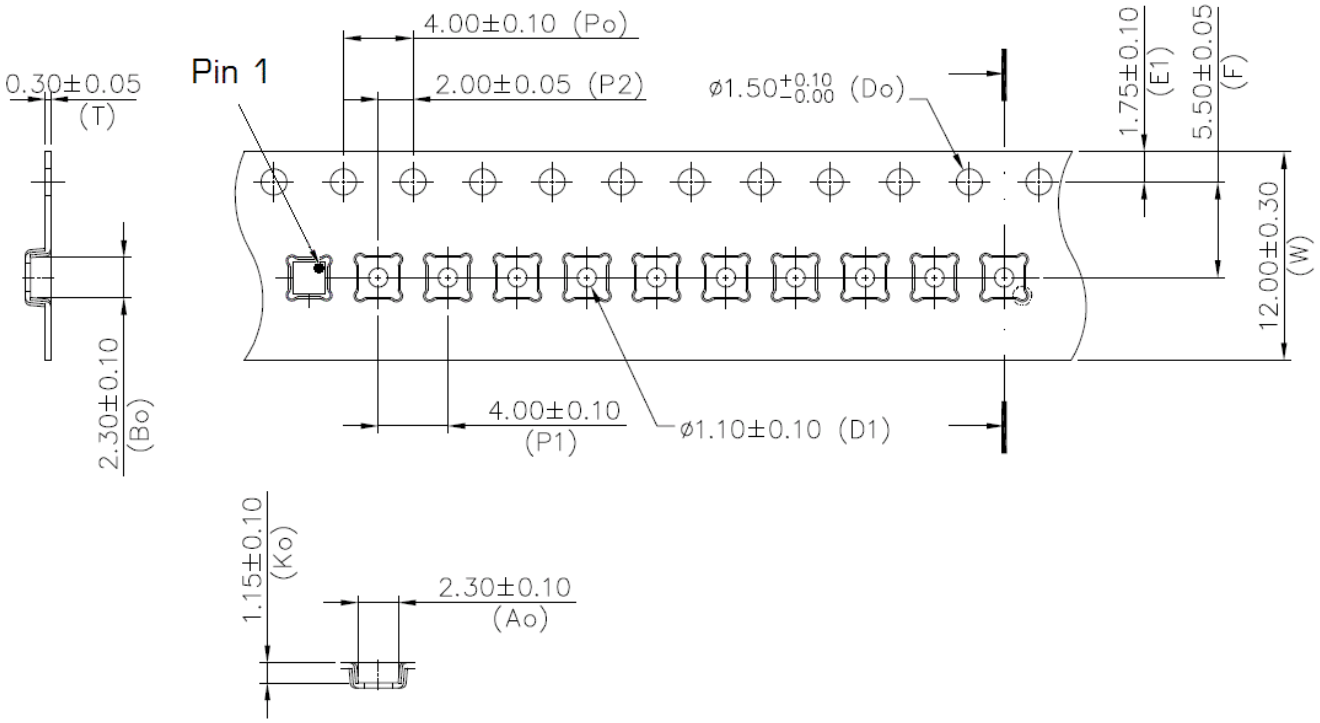
NOTE[1]: Attach typical 4.7kΩ pullup resistors to DVDD, per I2C specification. When DVDD is powered down, SDA and SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 5. Typical Application Circuit

In typical applications, the interface power supply may contain significant noise from external sources and other circuits which should be kept away from the sensor. Therefore, for some applications a lower-noise power supply might be desirable to power the VDD pin.

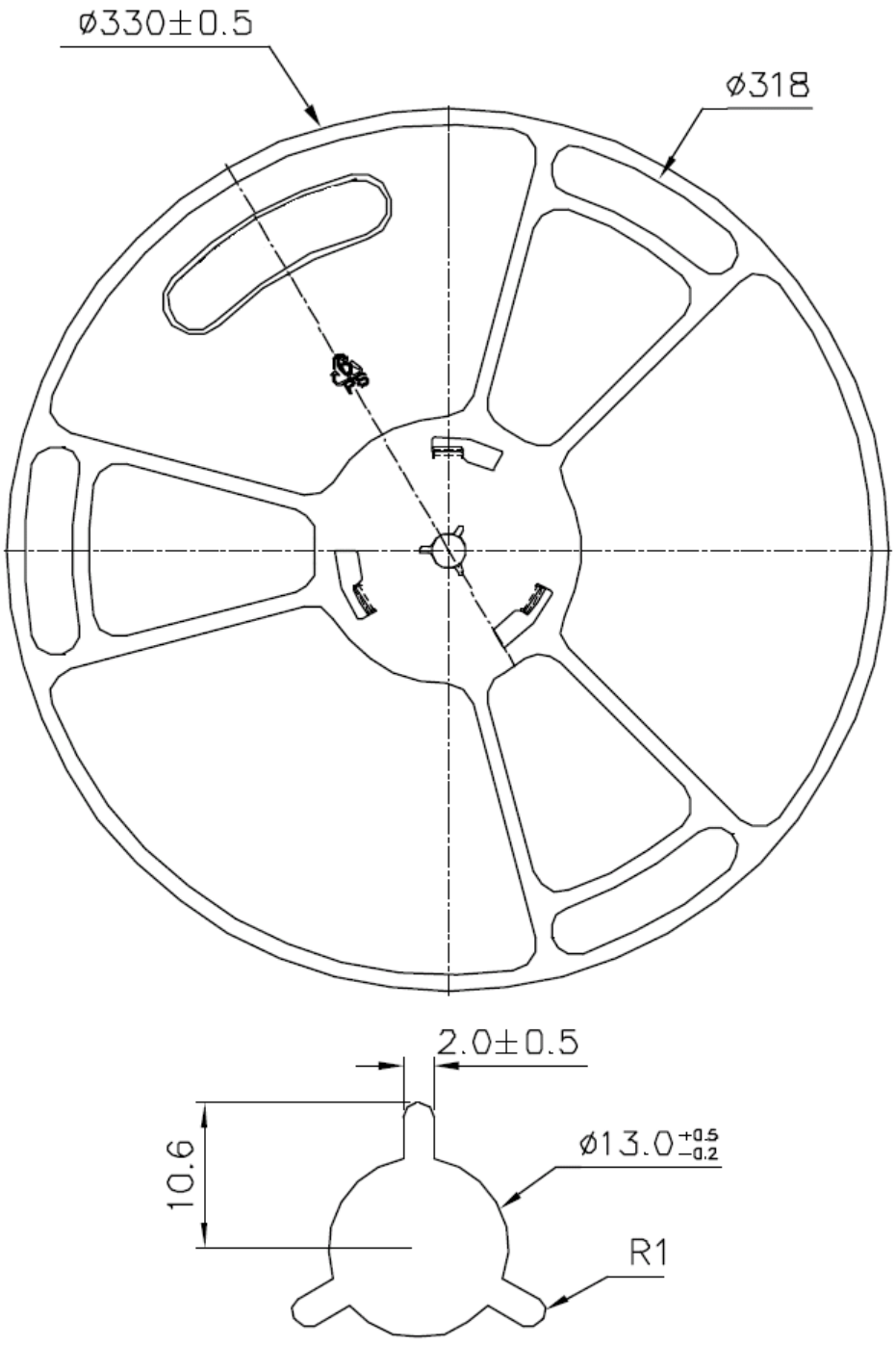
3.5 TAPE AND REEL

Devices are shipped in reels, in standard cardboard box packaging. See Figure 6. MC3433 Tape Dimensions and Figure 7. MC3433 Reel Dimensions.



- Dimensions in mm.
- 10 sprocket hole pitch cumulative tolerance ±0.2
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 6. MC3433 Tape Dimensions



- Dimensions in mm.

Figure 7. MC3433 Reel Dimensions

4 SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS

Parameters exceeding the Absolute Maximum Ratings may permanently damage the device.

Rating	Symbol	Minimum / Maximum Value	Unit
Supply Voltages	Pin VDD	-0.3 / +3.6	V
Acceleration, any axis, 100 µs	g_{MAX}	10000	g
Ambient operating temperature	T_{OP}	-40 / +85	^{0}C
Storage temperature	T_{STG}	-40 / +125	^{0}C
ESD human body model	HBM	± 2000	V
Latch-up current at T_{op} = 25 ^{0}C	I_{LU}	200	mA
Input voltage to non-power pin	Pins INTN, SCL and SDA	-0.3 / (VDD + 0.3) or 3.6 whichever is lower	V

Table 3. Absolute Maximum Ratings

4.2 SENSOR CHARACTERISTICS

VDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
Acceleration range			±2.0		g
Sensitivity			64		LSB/g
Sensitivity Temperature Coefficient [1]	-10 ≤ T_{op} ≤ +55 ^{0}C		± 0.025		%/^{0}C
Zero-g Offset			± 80		mg
Zero-g Offset Temperature Coefficient [1]	-10 ≤ T_{op} ≤ +55 ^{0}C		± 1		mg/^{0}C
Noise Density [1]			800		µg/√Hz
Nonlinearity [1]			2		% FS
Cross-axis Sensitivity [1]	Between any two axes		2		%

Table 4. Sensor Characteristics

[1] Values are based on device characterization, not tested in production.

4.3 ELECTRICAL AND TIMING CHARACTERISTICS

4.3.1 ELECTRICAL POWER AND INTERNAL CHARACTERISTICS

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Supply voltage [2]		VDD	1.8		3.6	V
Sample Rate Tolerance [3]		Tclock	-10		10	%

Test condition: VDD = 2.8V, T_{op} = 25 ^{0}C unless otherwise noted

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Standby current		I_{ddsb}		4		µA
WAKE state supply current		I_{ddw}		200		µA
Pad Leakage	Per I/O pad	I_{pad}	-1	0.01	1	µA

Table 5. Electrical Characteristics

[2] Min and Max limits are hard limits without additional tolerance.

[3] Values are based on device characterization, not tested in production.

4.3.2 I2C ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
LOW level input voltage	VIL	-0.5	0.3*VDD	V
HIGH level input voltage	VIH	0.7*VDD	-	V
Hysteresis of Schmitt trigger inputs	Vhys	0.05*VDD	-	V
Output voltage, pin INTN, Iol ≤ 2 mA	Vol Voh	0 0	0.4 0.9*VDD	V V
Output voltage, pin SDA (open drain), Iol ≤ 1 mA	Vols	-	0.1*VDD	V
Input current, pins SDA and SCL (input voltage between 0.1*VDD and 0.9*VDD max)	Ii	-10	10	µA
Capacitance, pins SDA and SCL [4]	Ci	-	10	pF

Table 6. I2C Electrical and Timing Characteristics

NOTES:

- If multiple slaves are connected to the I2C signals in addition to this device, only 1 pull-up resistor on each of SDA and SCL should exist. Also, care must be taken to not violate the I2C specification for capacitive loading.
- When VDD is not powered and set to 0V, INTN, SDA and SCL will be held to VDD plus the forward voltage of the internal static protection diodes, typically about 0.6V.
- When VDD is disconnected from power or ground (e.g. Hi-Z), the device may become inadvertently powered up through the ESD diodes present on other powered signals.

[4] Values are based on device characterization, not tested in production.

4.3.3 I2C TIMING CHARACTERISTICS

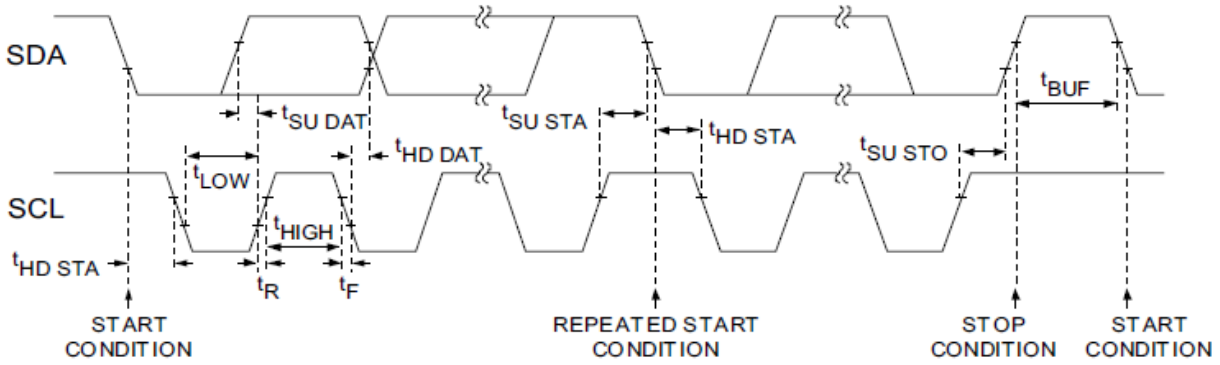


Figure 8. I2C Interface Timing

Parameter	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	4.0	-	0.26	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time	5.0	-	-	-	µs
$t_{SU;DAT}$	Data set-up time	250	-	100	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START	4.7	-	1.3	-	µs

Table 7. I2C Timing Characteristics

NOTE: Values are based on I2C Specification requirements, not tested in production.

See also Section 10.3 I2C Message Format.

5 GENERAL OPERATION

The device supports the reading of samples and device status upon interrupt or via polling.

5.1 SENSOR SAMPLING

In the WAKE state, acceleration data for X, Y, and Z axes is sampled at a rate between 0.125 and 128 samples/second. See Section11.7 SRFR Sample Rate Register.

The detectable acceleration range is from -2g to +2g.

Resolution	Acceleration Range	Value per bit (mg/LSB)	Full Scale Negative Reading	Full Scale Positive Reading	Comments
8-bit	± 2g	~15.6	0x80 (-128)	0x7F (+127)	Signed 2's complement number, results in XOUT, YOUT, ZOUT. The MSB is the sign bit. (Integer interpretation also shown)

Table 8. Summary of Resolution, Range, and Scaling

Based upon the intended application, filtering of the data samples may be desired. When enabled, the LPF is a first order IIR filter and has a fixed cutoff frequency of approximately 0.25 of the ODR sampling rate chosen in Section 11.7 SRFR Sample Rate Register. The ACQ_INT interrupt (interrupt on sample) will continue to trigger at the sample rate, not the filtered rate.

5.2 OFFSET AND GAIN CALIBRATION

Digital offset and gain calibration can be performed on the sensor, if necessary, in order to reduce the effects of post-assembly influences and stresses which may cause the sensor readings to be offset from their factory values.

6 OPERATIONAL STATES

The device has two states of operation: STANDBY (the default state after power-up), and WAKE.

The STANDBY state offers the lowest power consumption. In this state, the I2C interface is active and all register reads and writes are allowed. There is no event detection, sampling, or acceleration measurement in the STANDBY state. Internal clocking is halted. Complete access to the register set is allowed in this state, but interrupts cannot be serviced. The device defaults to the STANDBY state following power-up. The time to change states from STANDBY to WAKE is less than 10uSec.

Registers can be written (and therefore resolution, range. thresholds and other settings changed) only when the device is in STANDBY state.

The I2C interface allows write access to all registers only in the STANDBY state. In WAKE state, the only I2C register write access permitted is to the MODE Register. Full read access is allowed in all states.

State	I2C Bus	Description
STANDBY	Device responds to I2C bus (R/W)	Device is powered; Registers can be accessed via I2C. Lowest power state. No interrupt generation, internal clocking disabled. Default power-on state.
WAKE	Device responds to I2C bus (Read)	Continuous sampling and reading of sense data. All registers except the MODE Register are read-only.

Table 9. Operational States

7 OPERATIONAL STATE FLOW

Figure 9. Operational State Flow shows the operational state flow for the device. The device defaults to STANDBY following power-on.

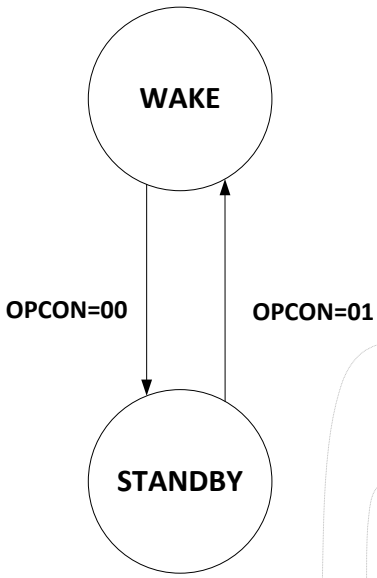


Figure 9. Operational State Flow

The operational state may be forced to a specific state by writing into the OPCON bits, as shown below. Two bits are specified in order to promote software compatibility with other mCube devices. The operational state will stay in the mode specified until changed:

Action	Setting	Effect
Force Wake State	OPCON[1:0] = 01	• Switch to WAKE state and stay there • Continuous sampling
Force Standby State	OPCON[1:0] = 00	• Switch to STANDBY state and stay there • Disable sensor and event sampling

Table 10. Forcing Operational States

8 INTERRUPTS

The sensor device utilizes output pin INTN to signal to an external microprocessor that an event has been sensed. The microprocessor would contain an interrupt service routine which would perform certain tasks after receiving this interrupt and reading the associated status bits, perhaps after a sample was made ready. If interrupts are to be used, the microprocessor must set up the registers in the sensor so that when a specific event is detected, the microprocessor would receive the interrupt and the interrupt service routine would be executed. If polling is used there is no need for the interrupt registers to be set up.

For products that will instead use polling, the method of reading sensor data would be slightly different. Instead of receiving an interrupt when an event occurs, the microprocessor must periodically poll the sensor and read status data (the INTN pin is not used). For most applications, this is likely best done at the sensor sampling rate or faster.

Note that at least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

8.1 ENABLING AND CLEARING INTERRUPTS

The SR Status Register contains the flag bits for the sample acquisition interrupt ACQ_INT. The INTEN Interrupt Enable Register determines if a flag event generate interrupts.

The flags (and interrupts) are cleared and rearmed each time the SR Status Register is read.

When an event is detected, it is masked with a flag bit in the INTEN Interrupt Enable Register, and then the corresponding status bit is set in the SR Status Register.

The polarity and driving mode of the external interrupt signal may be chosen by setting the IPP and IAH bits in the MODE Register.

8.2 ACQ_INT INTERRUPT

The ACQ_INT flag bit in the SR Status Register is always active. This bit is cleared when it is read. When a sample has been produced, an interrupt will be generated only if the ACQ_INT_EN bit in the INTEN Interrupt Enable Register is active. Note that the frequency of this ACQ_INT bit being set active is always the same as the sample rate, regardless of the LPF setting.

9 SAMPLING

9.1 CONTINUOUS SAMPLING

The device has the ability to read all sampled readings in a continuous sampling fashion. The device always updates the XOUT, YOUT, and ZOUT registers at the chosen ODR.

An optional interrupt can be generated each time the sample registers have been updated (ACQ_INT interrupt bit in the INTEN Interrupt Enable Register). See Sections 8.2 and SR Status Register for ACQ_INT operation and options.

10 I2C INTERFACE

10.1 PHYSICAL INTERFACE

The I2C slave interface operates at a maximum speed of 400 kHz. The SDA (data) is an open-drain, bi-directional pin and the SCL (clock) is an input pin.

The device always operates as an I2C slave.

An I2C master initiates all communication and data transfers and generates the SCL clock that synchronizes the data transfer. The I2C device address depends upon the state of the VPP pin during power-up as shown in the table below.

An optional I2C watchdog timer reset can be enabled to prevent bus stall conditions. When enabled, the sensor I2C circuitry will reset itself if the master takes too long to issue clocks to the sensor during a read cycle (i.e. if there is a gap in SCL clocks of more than about 200mSec). A status bit can be read to observe if this condition has occurred.

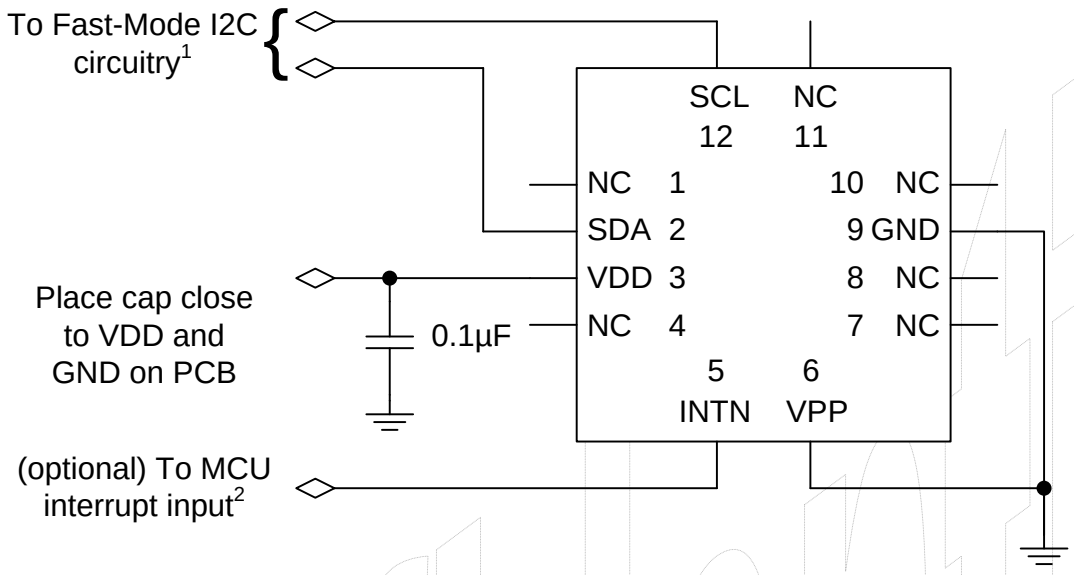
7-bit Device ID	8-bit Address – Write	8-bit Address – Read	VPP level upon power-up
0x4C (0b1001100)	0x98	0x99	GND
0x6C (0b1101100)	0xD8	0xD9	VDD

Table 11 - I2C Address Selection

The I2C interface remains active as long as power is applied to the VDD pin. In STANDBY state the device responds to I2C read and write cycles, but interrupts cannot be serviced or cleared. All registers can be written in the STANDBY state, but in WAKE only the MODE Register can be modified.

Internally, the registers which are used to store samples are clocked by the sample clock gated by I2C activity. Therefore, in order to allow the device to collect and present samples in the sample registers at least one I2C STOP condition must be present between samples.

Refer to the I2C specification for a detailed discussion of the protocol. Per I2C requirements, SDA is an open drain, bi-directional pin. SCL and SDA each require an external pull-up resistor, typically 4.7kΩ.



NOTE[1]: Attach typical 4.7kΩ pullup resistors to DVDD, per I2C specification. When DVDD is powered down, SDA and SCL will be driven low by internal ESD diodes.
NOTE[2]: Attach typical 4.7kΩ pullup resistor if INTN is defined as open-drain.

Figure 10. Typical Application Circuit

10.2 TIMING

See Section 4.3.3 I2C Timing Characteristics for I2C timing requirements.

10.3 I2C MESSAGE FORMAT

Note that at least one I2C STOP condition must be present between samples in order for the sensor to update the sample data registers.

The device uses the following general format for writing to the internal registers. The I2C master generates a START condition, and then supplies the 7-bit device ID. The 8th bit is the R/W# flag (write cycle = 0). The device pulls SDA low during the 9th clock cycle indicating a positive ACK.

The second byte is the 8-bit register address of the device to access, and the last byte is the data to write.

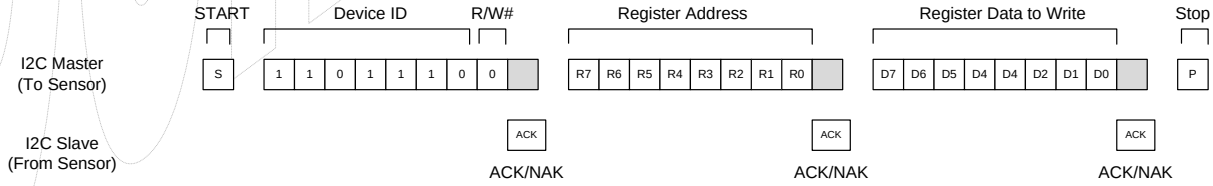


Figure 11. I2C Message Format, Write Cycle, Single Register Write

In a read cycle, the I2C master writes the device ID (R/W#=0) and register address to be read. The master issues a RESTART condition and then writes the device ID with the R/W# flag set to '1'. The device shifts out the contents of the register address.

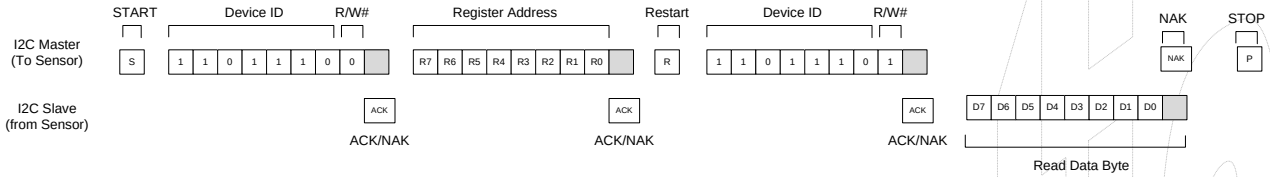


Figure 12. I2C Message Format, Read Cycle, Single Register Read

The I2C master may write or read consecutive register addresses by writing or reading additional bytes after the first access. The device will internally increment the register address.

If an I2C burst read operation reads past register address 0x12 the internal address pointer "wraps" to address 0x03 and the contents of the XOUT, YOUT & ZOUT X, Y & Z-Axis Accelerometer Registers are returned. This allows application software to burst read the contents of the six extended registers and the relevant device state registers in a single I2C cycle.

10.4 WATCHDOG TIMER

When enabled (see MODE Register), the I2C watchdog timer prevents bus stall conditions in cases where the master does not provide enough clocks to the slave to complete a read cycle.

During a read cycle, the slave that is actively driving the bus (SDA pin) will not release the bus until 9 SCL clock edges are detected. While the SDA pin is held low by a slave open-drain output, any other I2C devices attached to the sample bus will be unable to communicate. If the slave does not see 9 SCL clocks from the master within the timeout period, the slave will assume a system problem has occurred and so the I2C circuitry will be reset, the SDA pin released and the sensor made ready for additional I2C commands.

No other changes to registers are made.

When enabled, the I2C watchdog timer does not resolve why the master did not provide enough clocks to complete a read cycle, but it does prevent a slave from holding the bus indefinitely.

When enabled, the timeout period is about 200mSec.

When an I2C watchdog timer event is triggered, the I2C_WDT bit in register will be set active by the Watchdog timer hardware. External software can detect this status by noticing this bit is active. The act of reading register 0x04 will clears the status.

11 REGISTER INTERFACE

The device has a simple register interface which allows a MCU or I2C master to configure and monitor all aspects of the device. This section lists an overview of user programmable registers. By convention, Bit 0 is the least significant bit (LSB) of a byte register.

11.1 REGISTER SUMMARY

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W[5]
0x00	XOUT	XOUT Accelerometer Register	XOUT[7]	XOUT[6]	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]	0x00	W
0x01	YOUT	YOUT Accelerometer Register	YOUT[7]	YOUT[6]	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]	0x00	W
0x02	ZOUT	ZOUT Accelerometer Register	ZOUT[7]	ZOUT[6]	ZOUT[5]	ZOUT[4]	ZOUT[3]	ZOUT[2]	ZOUT[1]	ZOUT[0]	0x00	W
0x03	SR	Status Register	ACQ_INT	Resv	Resv	Resv	Resv	Resv	Resv	Resv	0x00	R
0x04	OPSTAT	Operational State Status Register	OTPA	Resv	Resv	I2C_WDT	Resv	Resv	OPSTAT [1]	OPSTAT [0]	0x03	R
0x05		RESERVED										
0x06	INTEN	Interrupt Enable Register	ACQ_INT_EN	Resv	Resv	Resv	Resv	Resv	Resv	Resv	0x00	W
0x07	MODE	Mode Register	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0[6]	OPCON [1]	OPCON [0]	0x03	W
0x08	SRFR	Sample Rate Register	Resv	Resv	Resv	Resv	RATE[3]	RATE[2]	RATE[2]	RATE[0]	0x00	W
0x09-0x1F		RESERVED										
0x20	OUTCFG	Output Configuration Register	LPF_EN	Resv	Resv	Resv	Resv	Resv	RES[1]	RES[0]	0x00	W
0x21	XOFFL	X-Offset LSB Register	XOFF[7]	XOFF[6]	XOFF[5]	XOFF[4]	XOFF[3]	XOFF[2]	XOFF[1]	XOFF[0]	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x23	YOFFL	Y-Offset LSB Register	YOFF[7]	YOFF[6]	YOFF[5]	YOFF[4]	YOFF[3]	YOFF[2]	YOFF[1]	YOFF[0]	Per chip	W
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x25	ZOFFL	Z-Offset LSB Register	ZOFF[7]	ZOFF[6]	ZOFF[5]	ZOFF[4]	ZOFF[3]	ZOFF[2]	ZOFF[1]	ZOFF[0]	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x27	XGAIN	X Gain Register	XGAIN[7]	XGAIN[6]	XGAIN[5]	XGAIN[4]	XGAIN[3]	XGAIN[2]	XGAIN[1]	XGAIN[0]	Per chip	W
0x28	YGAIN	Y Gain Register	YGAIN[7]	YGAIN[6]	YGAIN[5]	YGAIN[4]	YGAIN[3]	YGAIN[2]	YGAIN[1]	YGAIN[0]	Per chip	W
0x29	ZGAIN	Z Gain Register	ZGAIN[7]	ZGAIN[6]	ZGAIN[5]	ZGAIN[4]	ZGAIN[3]	ZGAIN[2]	ZGAIN[1]	ZGAIN[0]	Per chip	W
0x2A-0x3A		RESERVED										
0x3B	PCODE	Product Code	0	1	1	0	*[7]	*[7]	*[7]	0	NOTE	R
0x3C to 0x3F		RESERVED										

Table 12. Register Summary[8]

[5] 'R' registers are read-only, via external I2C access. 'W' registers are read-write, via external I2C access.
[6] Software must always write a zero '0' to this bit.
[7] Bits denoted with '*' might be any value, set by the factory. Software should ignore these bits.

11.2 XOUT, YOUT & ZOUT X, Y & Z-AXIS ACCELEROMETER REGISTERS

Accelerometer measurements are stored in the XOUT, YOUT, and ZOUT registers. The measurements are in signed 2's complement format. The range is always ± 2g. XOUT[7], YOUT[7] and ZOUT[7] are the sign bits for their registers.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x00	XOUT	XOUT Accelerometer Register	XOUT [7]	XOUT [6]	XOUT [5]	XOUT [4]	XOUT [3]	XOUT [2]	XOUT [1]	XOUT [0]	0x00	R
0x01	YOUT	YOUT Accelerometer Register	YOUT [7]	YOUT [6]	YOUT [5]	YOUT [4]	YOUT [3]	YOUT [2]	YOUT [1]	YOUT [0]	0x00	R
0x02	ZOUT	ZOUT Accelerometer Register	ZOUT [7]	ZOUT [6]	ZOUT [5]	ZOUT [4]	ZOUT [3]	ZOUT [2]	ZOUT [1]	ZOUT [0]	0x00	R

Table 13. Accelerometer Value Registers

[8] No registers are updated with new event status or samples while a I2C cycle is in process.

11.3 SR STATUS REGISTER

This register contains the flag/event bit for sample acquisition.

The flag (and interrupt) is cleared and rearmed each time this register is read.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x03	SR	Status Register	ACQ_INT	Resv	Resv	Resv	Resv	Resv	Resv	Resv	0x00	R

ACQ_INT	0: No sample has been generated by the sensor since last read. 1: Sample has been acquired, flag bit is set in polling mode or interrupt mode. This bit cannot be disabled and is always set be hardware when a sample is ready. The host must poll at the sample rate or faster to see this bit transition.

Table 14. SR Status Register Settings

11.4 OPSTAT DEVICE STATUS REGISTER

The device status register reports various conditions of the sensor circuitry.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x04	OPSTAT	Operational State Status Register	OTPA	Resv	Resv	I2C_WDT	Resv	Resv	OPSTAT [1]	OPSTAT [0]	0x03	R

OPSTAT[1:0]	Sampling State Register Status, Wait State Register Status 00: Device is in STANDBY state, no sampling 01: Device is in WAKE state, sampling at set sample rate 10: Reserved 11: Reserved
I2C_WDT	I2C watchdog timeout event has been detected by hardware, I2C slave state machine reset to idle. This flag is cleared by reading this register.
OTPA	One-time Programming (OTP) activity status 0: Internal memory is idle and the device is ready for use 1: Internal memory is active and the device is not yet ready for use

Table 15. OPSTAT Device Status Register

11.5 INTEN INTERRUPT ENABLE REGISTER

The interrupt enable register allows the flag bits for sample events to also trigger a transition of the external INTN pin. This is the only effect these bits have as the flag bits will be set/cleared in the SR Status Register regardless of which interrupts are enabled in this register.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x06	INTEN	Interrupt Enable Register	ACQ_INT_EN	Resv	Resv	Resv	Resv	Resv	Resv	Resv	0x00	W

ACQ_INT_EN	Generate Interrupt 0: Disable automatic interrupt on INTN pad after each sample (default). 1: Enable automatic interrupt on INTN pad after each sample.

Table 16. INTEN Interrupt Enable Register Settings

11.6 MODE REGISTER

The MODE register controls the active operating state of the device. This register can be written from either operational state (STANDBY or WAKE).

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x07	MODE	Mode Register	IAH	IPP	I2C_WDT_POS	I2C_WDT_NEG	Resv	0*	OPCON [1]	OPCON [0]	0x03	W

NOTE*: Software must always write a zero '0' to Bit 2.

OPCON [1:0]	00: STANDBY state (default)	Set Device Operational State. WAKE or STANDBY
	01: WAKE state	
	10: Reserved	
	11: Reserved	
I2C_WDT_NEG	0: I2C watchdog timer for negative SCL stalls disabled (default) 1: I2C watchdog timer for negative SCL stalls enabled	WDT for negative SCL stalls
I2C_WDT_POS	0: I2C watchdog timer for positive SCL stalls disabled (default) 1: I2C watchdog timer for positive SCL stalls enabled	WDT for positive SCL stalls
IPP	0: Interrupt pin INTN is open drain (default) and requires an external pull-up to VDD.	Interrupt Push Pull
	1: Interrupt pin INTN is push-pull. No external pull-up resistor should be installed.	
IAH	0: Interrupt pin INTN is active low (default)	Interrupt Active High
	1: Interrupt pin INTN is active high	

Table 17. MODE Register Functionality

11.7 SRFR SAMPLE RATE REGISTER

This register sets the sampling output data rate (ODR) for sensor. The lower 4 bits control the rate, as shown in the table below.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x08	SRFR	Sample Rate Register	Resv	Resv	Resv	Resv	RATE[3]	RATE[2]	RATE[1]	RATE[0]	0x00	W

RATE[3:0]	0000: 16 Hz (default) 0001: 8 Hz 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 0.5 Hz 0110: 0.25 Hz 0111: 0.125 Hz 1000: 32 Hz 1001: 64 Hz 1010: 128 Hz 1011: Reserved 1100: Reserved 1101: Reserved 1110: Reserved 1111: Reserved

Table 18. SRFR Register Functionality

11.8 OUTCFG OUTPUT CONFIGURATION REGISTER

This register can be used to set the resolution of the accelerometer measurements, and enabling the low pass filter.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x20	OUTCFG	Output Configuration Register	LPF_EN	Resv	Resv	Resv	Resv	Resv	RES[1]	RES[0]	0x00	W

RES[1:0]	Accelerometer g Resolution 00: Select 6-bit resolution 01: Select 7-bit resolution 10: Select 8-bit resolution 11: Reserved
LPF_EN	Low Pass Filter Enable 0: Disable low pass filter 1: Enable low pass filter The pass band is approximately 0.25 of the sampling frequency. The LPF is a first order IIR filter and has a fixed cutoff frequency of Fc = 0.25Fs. The GINT interrupt (interrupt on sample) will continue to trigger at the sample rate, not the filtered rate.

Table 19. OUTCFG Resolution Register Settings

11.9 X-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x21	XOFFL	X-Offset LSB Register	**XOFF[7]**	**XOFF[6]**	**XOFF[5]**	**XOFF[4]**	**XOFF[3]**	**XOFF[2]**	**XOFF[1]**	**XOFF[0]**	Per chip	W
0x22	XOFFH	X-Offset MSB Register	XGAIN[8]	**XOFF[14]**	**XOFF[13]**	**XOFF[12]**	**XOFF[11]**	**XOFF[10]**	**XOFF[9]**	**XOFF[8]**	Per chip	W

11.10 Y-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x23	YOFFL	Y-Offset LSB Register	**YOFF[7]**	**YOFF[6]**	**YOFF[5]**	**YOFF[4]**	**YOFF[3]**	**YOFF[2]**	**YOFF[1]**	**YOFF[0]**	Per chip	W
0x24	YOFFH	Y-Offset MSB Register	YGAIN[8]	**YOFF[14]**	**YOFF[13]**	**YOFF[12]**	**YOFF[11]**	**YOFF[10]**	**YOFF[9]**	**YOFF[8]**	Per chip	W

11.11 Z-AXIS OFFSET REGISTERS

This register contains a signed 2's complement 15-bit value applied as an offset adjustment to the output of the sensor values, prior to being sent to the OUT registers. The Power-On-Reset value for each chip is unique and is set as part of factory calibration. If necessary, this value can be overwritten by software.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x25	ZOFFL	Z-Offset LSB Register	**ZOFF[7]**	**ZOFF[6]**	**ZOFF[5]**	**ZOFF[4]**	**ZOFF[3]**	**ZOFF[2]**	**ZOFF[1]**	**ZOFF[0]**	Per chip	W
0x26	ZOFFH	Z-Offset MSB Register	ZGAIN[8]	**ZOFF[14]**	**ZOFF[13]**	**ZOFF[12]**	**ZOFF[11]**	**ZOFF[10]**	**ZOFF[9]**	**ZOFF[8]**	Per chip	W

11.12 X-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x22	XOFFH	X-Offset MSB Register	**XGAIN[8]**	XOFF[14]	XOFF[13]	XOFF[12]	XOFF[11]	XOFF[10]	XOFF[9]	XOFF[8]	Per chip	W
0x27	XGAIN	X Gain Register	**XGAIN[7]**	**XGAIN[6]**	**XGAIN[5]**	**XGAIN[4]**	**XGAIN[3]**	**XGAIN[2]**	**XGAIN[1]**	**XGAIN[0]**	Per chip	W

11.13 Y-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x24	YOFFH	Y-Offset MSB Register	**YGAIN[8]**	YOFF[14]	YOFF[13]	YOFF[12]	YOFF[11]	YOFF[10]	YOFF[9]	YOFF[8]	Per chip	W
0x28	YGAIN	Y Gain Register	**YGAIN[7]**	**YGAIN[6]**	**YGAIN[5]**	**YGAIN[4]**	**YGAIN[3]**	**YGAIN[2]**	**YGAIN[1]**	**YGAIN[0]**	Per chip	W

11.14 Z-AXIS GAIN REGISTERS

The gain value is an unsigned 9-bit number.

NOTE: When modifying these registers with new gain or offset values, software should perform a read-modify-write type of access to ensure that unrelated bits do not get changed inadvertently.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x26	ZOFFH	Z-Offset MSB Register	**ZGAIN[8]**	ZOFF[14]	ZOFF[13]	ZOFF[12]	ZOFF[11]	ZOFF[10]	ZOFF[9]	ZOFF[8]	Per chip	W
0x29	ZGAIN	Z Gain Register	**ZGAIN[7]**	**ZGAIN[6]**	**ZGAIN[5]**	**ZGAIN[4]**	**ZGAIN[3]**	**ZGAIN[2]**	**ZGAIN[1]**	**ZGAIN[0]**	Per chip	W

11.15 PCODE PRODUCT CODE

This register returns a value specific to the part number of this mCube device, noted below.

Addr	Name	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value	R/W
0x3B	PCODE	Product Code Register	0	1	1	0	*	*	*	0	Note	R

Note: Bits denoted with '*' might be any value, set by the factory. Software should ignore these bits.

12 INDEX OF TABLES

13 REVISION HISTORY

Date	Revision	Description
2013-12	APS-048-0025v1.0	First release.

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