MSG2156A
Capacitive Touch Panel Controller

Preliminary Data Sheet Version 0.2

MStar Confidential

for 深圳市海派通讯

科技有限公司

Internal Use Only

REVISION HISTORY

Revision No.	Description	Date
0.1	Ÿ Initial release	12/10/2012
0.2	Ÿ Updated Mechanical Dimensions (D2/E2)	01/04/2013

Doc.No.: 2013070444

FEATURES

n Capacitive Touch Screen Controller

- Ÿ Supports up to 46 sensors
- Ÿ Supports screen size up to 7"
- Ÿ X, Y resolution up to 2048 pixels x 2048 pixels
- Ÿ Programmable reporting rate: max 5ms/report
- Ÿ Accurate single-touch coordinate report and two-touch gesture
- Ÿ Automatic background capacitance tracking
- Ÿ 14-bit ADC

n Hardware

- Ÿ 32-bit MCU
- Ÿ SRAM embedded
- Ÿ I2C slave interface, up to 400Kb/s
- Ÿ Built-in oscillator

n Operation Voltage

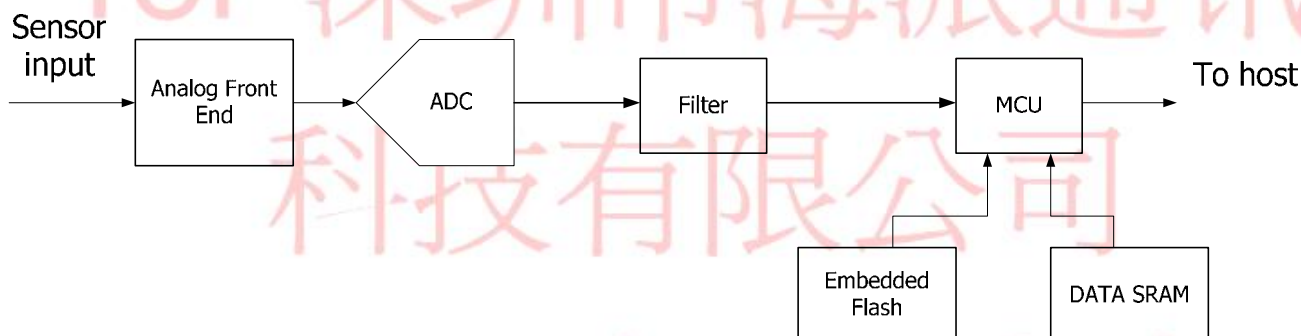- Ÿ 2.8V ~ 3.3V

n Misc.

- Ÿ UQFN-56 package

GENERAL DESCRIPTION

The MSG2156A is a capacitive touch screen controller. The internal ADC & DSP circuitry implement high-accuracy self-capacitance measurement. A 32-bit MCU with embedded flash provides programmability to suffice different requirements of various touch screen designs.

BLOCK DIAGRAM

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PIN DIAGRAM (MSG2156A)
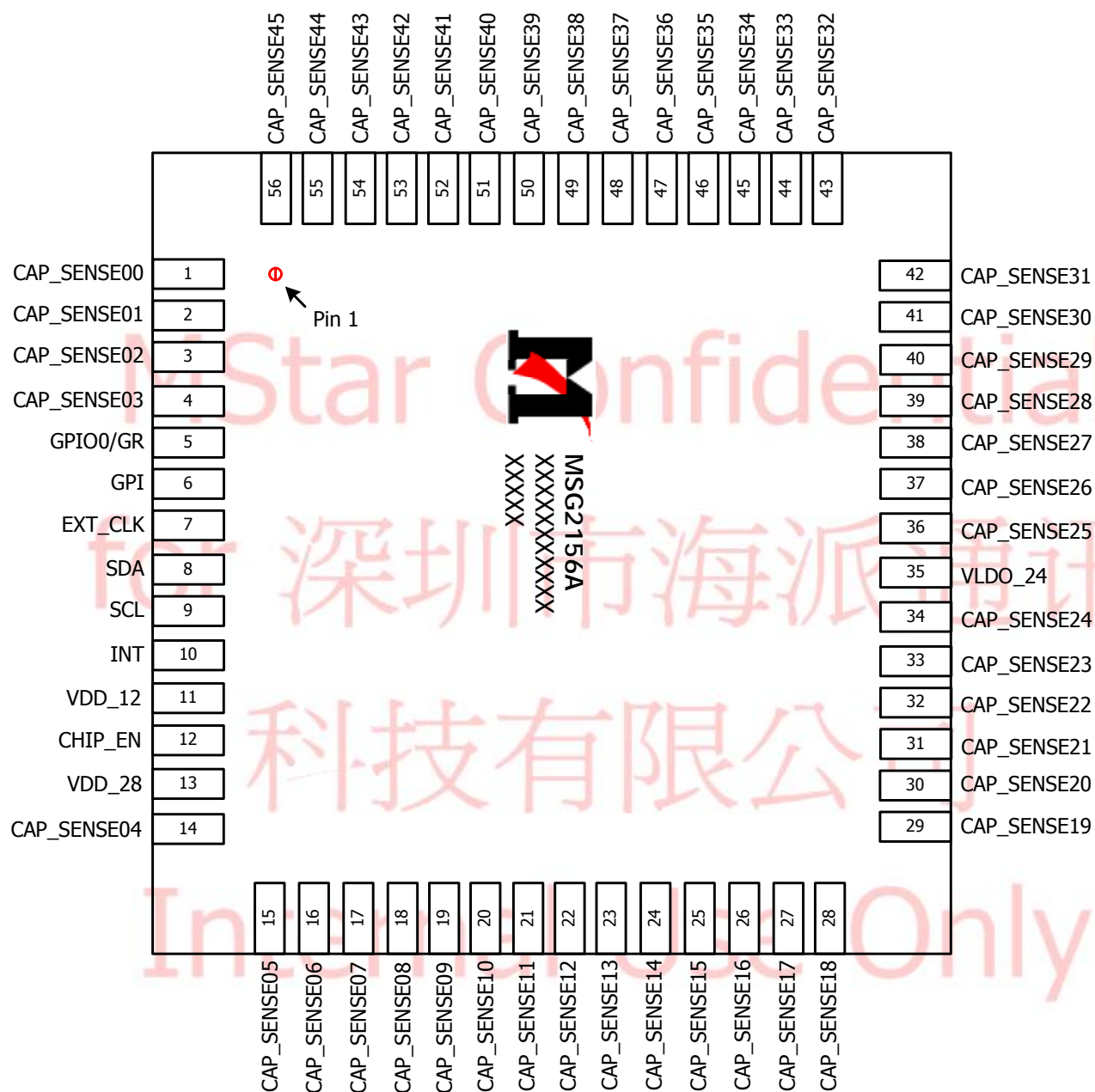
PIN DESCRIPTION

Capacitive Touch Sensor Interface

Pin Name	Pin Type	Function	Pin
CAP_SENSE00	Analog Input	Capacitive touch sensor input	1
CAP_SENSE01	Analog Input	Capacitive touch sensor input	2
CAP_SENSE02	Analog Input	Capacitive touch sensor input	3
CAP_SENSE03	Analog Input	Capacitive touch sensor input	4
CAP_SENSE04	Analog Input	Capacitive touch sensor input	14
CAP_SENSE05	Analog Input	Capacitive touch sensor input	15
CAP_SENSE06	Analog Input	Capacitive touch sensor input	16
CAP_SENSE07	Analog Input	Capacitive touch sensor input	17
CAP_SENSE08	Analog Input	Capacitive touch sensor input	18
CAP_SENSE09	Analog Input	Capacitive touch sensor input	19
CAP_SENSE10	Analog Input	Capacitive touch sensor input	20
CAP_SENSE11	Analog Input	Capacitive touch sensor input	21
CAP_SENSE12	Analog Input	Capacitive touch sensor input	22
CAP_SENSE13	Analog Input	Capacitive touch sensor input	23
CAP_SENSE14	Analog Input	Capacitive touch sensor input	24
CAP_SENSE15	Analog Input	Capacitive touch sensor input	25
CAP_SENSE16	Analog Input	Capacitive touch sensor input	26
CAP_SENSE17	Analog Input	Capacitive touch sensor input	27
CAP_SENSE18	Analog Input	Capacitive touch sensor input	28
CAP_SENSE19	Analog Input	Capacitive touch sensor input	29
CAP_SENSE20	Analog Input	Capacitive touch sensor input	30
CAP_SENSE21	Analog Input	Capacitive touch sensor input	31
CAP_SENSE22	Analog Input	Capacitive touch sensor input	32
CAP_SENSE23	Analog Input	Capacitive touch sensor input	33
CAP_SENSE24	Analog Input	Capacitive touch sensor input	34
CAP_SENSE25	Analog Input	Capacitive touch sensor input	36
CAP_SENSE26	Analog Input	Capacitive touch sensor input	37
CAP_SENSE27	Analog Input	Capacitive touch sensor input	38
CAP_SENSE28	Analog Input	Capacitive touch sensor input	39
CAP_SENSE29	Analog Input	Capacitive touch sensor input	40
CAP_SENSE30	Analog Input	Capacitive touch sensor input	41
CAP_SENSE31	Analog Input	Capacitive touch sensor input	42
CAP_SENSE32	Analog Input	Capacitive touch sensor input	43

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Pin Name	Pin Type	Function	Pin
CAP_SENSE33	Analog Input	Capacitive touch sensor input	44
CAP_SENSE34	Analog Input	Capacitive touch sensor input	45
CAP_SENSE35	Analog Input	Capacitive touch sensor input	46
CAP_SENSE36	Analog Input	Capacitive touch sensor input	47
CAP_SENSE37	Analog Input	Capacitive touch sensor input	48
CAP_SENSE38	Analog Input	Capacitive touch sensor input	49
CAP_SENSE39	Analog Input	Capacitive touch sensor input	50
CAP_SENSE40	Analog Input	Capacitive touch sensor input	51
CAP_SENSE41	Analog Input	Capacitive touch sensor input	52
CAP_SENSE42	Analog Input	Capacitive touch sensor input	53
CAP_SENSE43	Analog Input	Capacitive touch sensor input	54
CAP_SENSE44	Analog Input	Capacitive touch sensor input	55
CAP_SENSE45	Analog Input	Capacitive touch sensor input	56

Host Interface

Pin Name	Pin Type	Function	Pin
CHIP_EN	Input w/ 5V-tolerant	Chip Enable	12
EXT_CLK	Input w/ 5V-tolerant	External Sync Clock Input	7
SDA	I/O w/ 5V-tolerant	I^{2}C Serial Data Input/Output	8
SCL	I/O w/ 5V-tolerant	I^{2}C Serial Clock Input/Output	9
INT	I/O w/ 5V-tolerant	Interrupt signal; active low	10

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPI	Input w/ 5V-tolerant	General Purpose Input; 4mA driving strength	6
GPIO0/ GR	I/O w/ 5V-tolerant/ analog output	General Purpose Input/Output; 4mA driving strength/ Guard ring driver output	5

Power Pins

Pin Name	Pin Type	Function	Pin
VDD_28	2.8V Power	2.8V~3.3V power supply; connect 1uF capacitor to Ground	13
VLDO_24	2.4V Power	Internally generated reference voltage; connect 1uF capacitor to Ground	35
VDD_12	1.2V Power	Internally generated digital power supply; connect 1uF capacitor to Ground	11

Note: E-pad should be connected to system GND net.

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ELECTRICAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Input Voltage 1, High (V_{IH1})[1]	1			V
Input Voltage 2, High (V_{IH2})[2]	2.1			V
Input Voltage, Low (V_{IL})			0.5	V
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH1})[3]		See Note3		V
Output Voltage, High (V_{OH2})[4]	V_{VDD} - 0.1			
Output Voltage, Low (V_{OL})			0.1	V

Specifications are subjected to change without notice.

Notes:

1. V_{IH1} includes pins EXT_CLK, CHIP_EN, SDA, SCL, INT.
2. V_{IH2} refers to other digital pins.
3. V_{OH1} is for INT output voltage level which is programmable by registers. Typical values are 1.2V/1.5V/1.8V/V_{VDD}.
4. V_{OH2} refers to other digital pins.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{VDD}	2.8	-	3.3	V
Ambient Operating Temperature	T_A	-20		85	°C
Junction Temperature	T_J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{VDD}			3.6	V
Analog Input Voltage	V_{INANA}			V_{VDD}	V
Digital Input Voltage	V_{INDIG}			5	V
Storage Temperature	T_{STG}	-40		85	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MSG2156A	-20°C to +85°C	UQFN	56

MARKING INFORMATION

MSG2156A

Part Number

Lot Number
Operation Code A

Operation Code B
Date Code (YYWW)
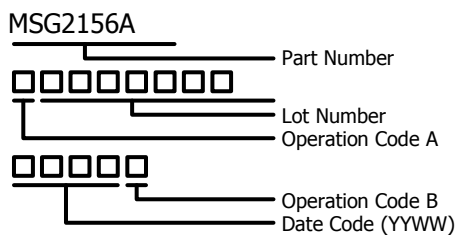
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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection.   MSG2156A comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges.   The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

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MECHANICAL DIMENSIONS
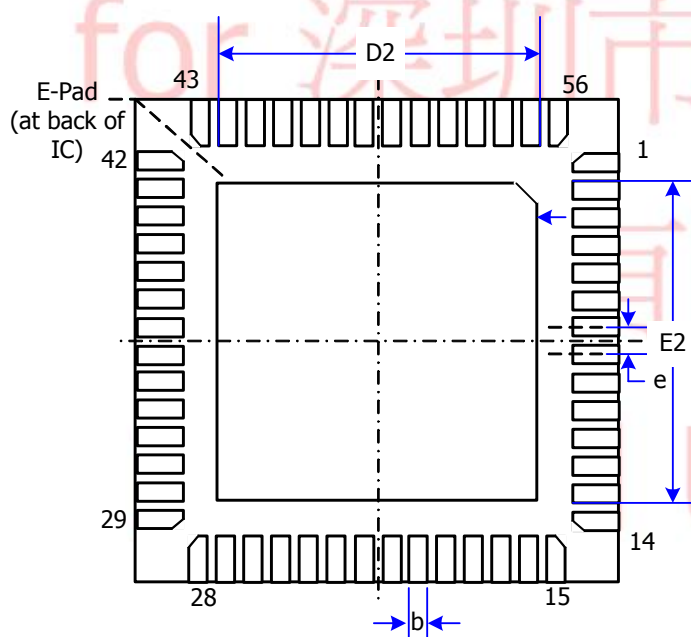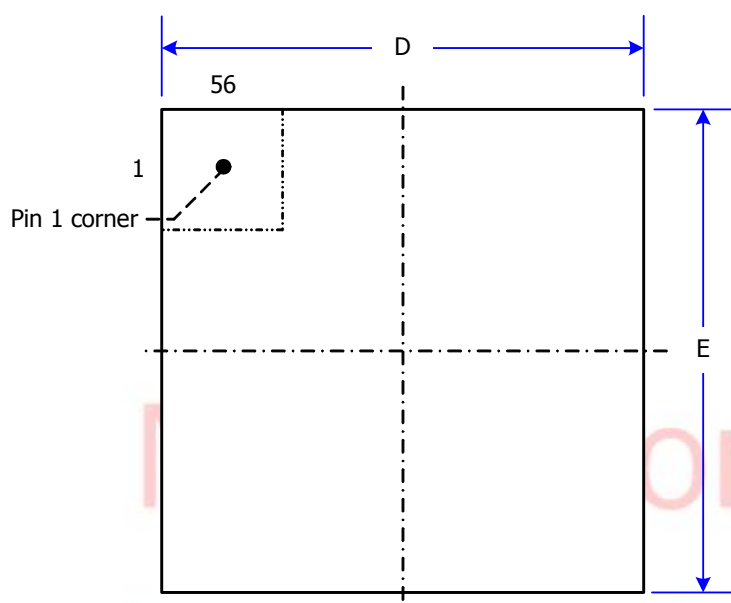
Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.55	0.6	0.65	0.022	0.024	0.026
D	6.9	7	7.1	0.272	0.276	0.280
E	6.9	7	7.1	0.272	0.276	0.280
D2	3.35	-	5.8	0.132	-	0.228
E2	3.35	-	5.8	0.132	-	0.228
b	0.15	0.2	0.25	0.006	0.008	0.010
e	0.35	0.4	0.45	0.014	0.016	0.018

Note: E-pad have to connect to system GND net.

REGISTER DESCRIPTION

ANA1 Register (Bank = 11)

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Index	**Mnemonic**	**Bit**	**Description**	
1180h	REG1180	15:0	Default : 0x00FF	Access : R/W
	TGEN_SOFT_RST[15:0]	15:0	Analog timing gen software reset, 1: reset, 0: normal operation.	
1181h	REG1181	15:0	Default : 0x0000	Access : R/W
	-	15:13	Reserved.	
	AFE_RMODE_EN	12	Afe r-mode enable, 1:enable, 0:disable.	
	TST_PWR_EN	11	Some sensor PADs power switch to PVDD for test mode, 1:enable, 0:disable.	
	SHIELDING_EN	10	Enable shielding path to sensor00 (directly to PAD).	
	DRV_VSUB_EXT_EN	9	Driver external Csub mode enable control.	
	HI_SLEW_EN	8	Driver high slew rate mode enable.	
	CAL_EN	7	Driver calibration mode enable.	
	DRV_CP_EN	6	Driver current comparator enable.	
	DRV_PRE_EN	5	Driver, pre_driver enable.	
	CTH_BIAS_EN	4	C_touch_atop bias gen enable.	
	REFBUF_EN	3	ADC 1.2V buffer enable.	
	LDO_EN	2	Ref_top LN_LDO24 enable.	
	IGEN_EN	1	Ref_top igen enable.	
	BG_EN	0	Bandgap reference enable.	
1182h	REG1182	15:0	Default : 0x0000	Access : R/W
	-	15	Reserved.	
	AFE_CS_SENSOR[4:0]	14:10	Afe compensation cap 5bits selection for sensor mode.	
	AFE_CS_BUTTON[4:0]	9:5	Afe compensation cap 5bits selection for button mode.	
	AFE_CFB_SENSOR[1:0]	4:3	Afe cfb 2bit selection for sensor mode.	
	AFE_CFB_BUTTON[1:0]	2:1	Afe cfb 2bit selection for button mode.	
	AFE_CAL_CAP_ON	0	Afe calibrationcap on/off control, 1:on, 0:off.	
1183h	REG1183	15:0	Default : 0x0000	Access : R/W
	-	15	Reserved.	
	DRV_CURR_LVL[2:0]	14:12	Driver current comparator current threshold 3bits selection.	

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ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	DRV_CS_SEL[2:0]	11:9	Driver compensation 3bit selection.	
	-	8:0	Reserved.	
1184h	**REG1184**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DRV_MUX_SYNC[15:0]	15:0	Driver mux selection for sync mode, set to sensors used in sync mode.	
1185h	**REG1185**	**15:0**	**Default : 0x0000**	**Access : R/W**
	DRV_MUX_SYNC[31:16]	15:0	See description of '1184h'.	
1186h	**REG1186**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15	Reserved.	
	DRV_MUX_SYNC[46:32]	14:0	See description of '1184h'.	
1187h	**REG1187**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:12	Reserved.	
	DRV_SW_MODE	11	1: Noise sensing mode. 0: Normal mode.	
	DRV_SLEW_LIM_PRE_SW2[2:0]	10:8	Driver SW2 slew rate 3bits selection.	
	-	7:6	Reserved.	
	DRV_SLEW_LIM_PRE_SW1[2:0]	5:3	Driver SW1 slew rate 3bits selection.	
	DRV_REF_SEL[2:0]	2:0	Driver reference voltage 3bits selection.	
1188h	**REG1188**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:11	Reserved.	
	AFE_RC_SEL[1:0]	10:9	Afe 300KHz low pass filter R-C selection.	
	SYNC_PL	8	Driver pull-low selection bit in sync mode (0V?1.2V?). 0: 1.2V. 1: Pull-low (ground).	
	LPC_SEL[3:0]	7:4	Driver BPF low-pass filter corner 4bits selection.	
	GAIN_SEL[3:0]	3:0	Driver BPF gain 4bits selection.	
1189h	**REG1189**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:8	Reserved.	
	CT_TST[7:0]	7:0	Reserved.	
118Ah	**REG118A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:7	Reserved.	
	ADC_GAINCOR_E	6	Odd/even gain cor. Enable.	

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	ADC_CAL_SEL[2:0]	5:3	Adc calibration selection. [2:1]: off/gain/lin; [0]: Odd/even.	
	ADC_CAL	2	Adc calibration enable.	
	ADC_SMP_PH_SEL[1:0]	1:0	Adc sampling phase selection.	
1190h	REG1190	15:0	Default : 0x0000	Access : R/W
	DET_DEG_TH[7:0]	15:8	Det_out_p/det_out_n deg threshold @ 24MHz.	
	VCOM_DEG_TH[7:0]	7:0	Vcom sync deg threshold @ 24MHz.	
1191h	REG1191	15:0	Default : 0x0000	Access : R/W
	AVCOM_L_LVL_WAIT_CYC[7:0]	15:8	Low level wait cycles to mask out possible spike noise, step 1T, for debouncing.	
	AVCOM_H_LVL_WAIT_CYC[7:0]	7:0	High level wait cycles to mask out possible spike noise, step 1T, for debouncing.	
1192h	REG1192	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	
	VCOM_FDET_TOUT[4:0]	9:5	1ms~31ms, roughly 1ms per step, stop freq training if timeout, if set to 0=> no timeout.	
	VCOM_FDET_DUR_NUM[2:0]	4:2	High and low duration counts for freq. Training, 2^N, (2, 4, 8, 16, 32, 64, 128), must be consecutive passed.	
	VCOM_FDET_MODE	1	0: Normal; 1: successive.	
	VCOM_FDET_TRIG	0	Vcom sync freq. Detection trigger.	
1193h	REG1193	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	EXP_VCOM_H_DUR[11:0]	11:0	High duration spec. Center for freq. Training.	
1194h	REG1194	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	EXP_VCOM_L_DUR[11:0]	11:0	Low duration spec. Center for freq. Training.	
1195h	REG1195	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	

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ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	EXP_VCOM_H_TH[9:0]	9:0	The threshold for freq_training high duration, the high duration spec. Would be high_duration +/- th.	
1196h	REG1196	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	
	EXP_VCOM_L_TH[9:0]	9:0	The threshold for freq_training low duration, the low duration spec. Would be low_duration +/- th.	
1197h	REG1197	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	
	DET_MASK[1:0]	9:8	Det_out_p/det_out_p mask. [0]: Det_out_p. [1]: Det_out_n.	
	-	7:4	Reserved.	
	VCOM_DEB_DIS[3:0]	3:0	Vcom_sync deg/deb disable. [0]: Ana vcom deg dis. [1]: Ana vcom deb dis. [2]: Ext vcom deg dis. [3]: Det_out_p/det_out_n deg dis.	
119Ah	REG119A	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	VCOM_GEN_EDGE_SEL[1:0]	11:10	0: Non; 1: rising; 2: falling; 3: rising + falling.	
	VCOM_GEN_SYNC_MODE[1:0]	9:8	0: Freerun counter; 1: analog vcom; 2: ext_vcom; 3: analog + emulated.	
	VCOM_SYNC_SETTLE_EDGE_NUM[5:0]	7:2	Consecutive passed high and low duration counts required for vcom_sync signal (BPF) settling, 1~64 (max. 32 periods).	
	VCOM_GEN_HW_TRIG_DIS	1	Hw sync disable.	
	VCOM_GEN_SW_TRIG	0	Software_resync.	
119Bh	REG119B	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	VCOM_SYNC_SETTLE_TOUT[9:0]	9:0	10.067us~10.9ms, 10.067us per step (256T). Vcom_sync_timeout << vcom blanking time in phase training. Vcom_sync_timeout >> vcom blanking time in normal operation. Start to generate emulated vcom if timeout occurs.	
119Ch	REG119C	15:0	Default : 0x0000	Access : R/W
	EMU_VCOM_PER[15:0]	15:0	Emulated vcom period, fill by software, with 13+6 bits.	
119Dh	REG119D	15:0	Default : 0x0000	Access : R/W
	-	15:3	Reserved.	
	EMU_VCOM_PER[18:16]	2:0	See description of '119Ch'.	
119Eh	REG119E	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	EMU_VCOM_H_DUR[11:0]	11:0	Emulated vcom high duration, fill by software.	
119Fh	REG119F	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	EMU_VCOM_L_DUR[11:0]	11:0	Emulated vcom low duration, fill by software.	
11A0h	REG11A0	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	
	VCOM_SYNC_H_TH[9:0]	9:0	The threshold for vcom_sync high duration, the high duration spec. Would be emulated_vcom_high_duration +/- th.	
11A1h	REG11A1	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	HPF_BYPASS_DUR[3:0]	13:10	To analog.	
	VCOM_SYNC_L_TH[9:0]	9:0	The threshold for vcom_sync low duration, the low duration spec. Would be emulated_vcom_low_duration +/- th.	
11A3h	REG11A3	15:0	Default : 0x0000	Access : R/W
	-	15:7	Reserved.	
	GAIN_PEAK_DET_RST_DUR[2:0]	6:4	Rst length settings, 1ms per step.	
	GAIN_SWITCH_DUR[2:0]	3:1	1~8ms settling settings for each gain.	
	GAIN_TRAIN_TRIG	0	Gain training process trigger.	
11A5h	REG11A5	15:0	Default : 0x0000	Access : R/W

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	-	15:2	Reserved.	
	ATGEN_SF_NUM	1	Mode selection for subframe number 0:<=4 or 1:>4.	
	ATGEN_MODE	0	0: Normal; 1: ac noise sensing.	
11A6h	REG11A6	15:0	Default : 0x0000	Access : R/W
	-	15:1	Reserved.	
	AFE_MUXSEL_MAP_AC_TRIG	0	Ac noise sensing settings loading trigger.	
11A7h	REG11A7	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE1SUB0_AFE1SUB0[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE0SUB0_AFE0SUB0[5:0]	5:0	AFE mux sel settings.	
11A8h	REG11A8	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE3SUB0_AFE3SUB0[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE2SUB0_AFE2SUB0[5:0]	5:0		
11A9h	REG11A9	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE5SUB0_AFE1SUB1[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE4SUB0_AFE0SUB1[5:0]	5:0		
11AAh	REG11AA	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE7SUB0_AFE3SUB1[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE6SUB0_AFE2SUB1[5:0]	5:0		
11ABh	REG11AB	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE9SUB0_AFE1SUB2[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE8SUB0_AFE0SUB2[5:0]	5:0		
11ACh	REG11AC	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE11SUB0_AFE3SUB2[5:0]	13:8		

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	-	7:6	Reserved.	
	MUXSEL_AFE10SUB0_AFE2SUB2[5:0]	5:0		
11ADh	REG11AD	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE1SUB1_AFE1SUB3[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE0SUB1_AFE0SUB3[5:0]	5:0		
11AEh	REG11AE	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE3SUB1_AFE3SUB3[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE2SUB1_AFE2SUB3[5:0]	5:0		
11AFh	REG11AF	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE5SUB1_AFE1SUB4[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE4SUB1_AFE0SUB4[5:0]	5:0		
11B0h	REG11B0	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE7SUB1_AFE3SUB4[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE6SUB1_AFE2SUB4[5:0]	5:0		
11B1h	REG11B1	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE9SUB1_AFE1SUB5[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE8SUB1_AFE0SUB5[5:0]	5:0		
11B2h	REG11B2	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE11SUB1_AFE3SUB5[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE10SUB1_AFE2SUB5[5:0]	5:0		
11B3h	REG11B3	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	MUXSEL_AFE1SUB2_AFE1SUB6[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE0SUB2_AFE0SUB6[5:0]	5:0		
11B4h	REG11B4	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE3SUB2_AFE3SUB6[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE2SUB2_AFE2SUB6[5:0]	5:0		
11B5h	REG11B5	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE5SUB2_AFE1SUB7[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE4SUB2_AFE0SUB7[5:0]	5:0		
11B6h	REG11B6	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE7SUB2_AFE3SUB7[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE6SUB2_AFE2SUB7[5:0]	5:0		
11B7h	REG11B7	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE9SUB2_AFE1SUB8[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE8SUB2_AFE0SUB8[5:0]	5:0		
11B8h	REG11B8	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE11SUB2_AFE3SUB8[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE10SUB2_AFE2SUB8[5:0]	5:0		
11B9h	REG11B9	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	MUXSEL_AFE1SUB3_AFE1SUB9[5:0]	13:8		
	-	7:6	Reserved.	
	MUXSEL_AFE0SUB3_AFE0SUB9[5:0]	5:0		
11BAh	REG11BA	15:0	Default : 0x0000	Access : R/W

Index	Mnemonic	Bit	Description	
ANA1 Register (Bank = 11)				
Index	**Mnemonic**	**Bit**	**Description**	
-		15:14	Reserved.	
	MUXSEL_AFE3SUB3_AFE3SUB9[5:0]	13:8		
-		7:6	Reserved.	
	MUXSEL_AFE2SUB3_AFE2SUB9[5:0]	5:0		
11BBh	**REG11BB**	**15:0**	**Default : 0x0000**	**Access : R/W**
-		15:14	Reserved.	
	MUXSEL_AFE5SUB3_AFE1SUB10[5:0]	13:8		
-		7:6	Reserved.	
	MUXSEL_AFE4SUB3_AFE0SUB10[5:0]	5:0		
11BCh	**REG11BC**	**15:0**	**Default : 0x0000**	**Access : R/W**
-		15:14	Reserved.	
	MUXSEL_AFE7SUB3_AFE3SUB10[5:0]	13:8		
-		7:6	Reserved.	
	MUXSEL_AFE6SUB3_AFE2SUB10[5:0]	5:0		
11BDh	**REG11BD**	**15:0**	**Default : 0x0000**	**Access : R/W**
-		15:14	Reserved.	
	MUXSEL_AFE9SUB3[5:0]	13:8		
-		7:6	Reserved.	
	MUXSEL_AFE8SUB3[5:0]	5:0		
11BEh	**REG11BE**	**15:0**	**Default : 0x0000**	**Access : R/W**
-		15:14	Reserved.	
	MUXSEL_AFE11SUB3[5:0]	13:8		
-		7:6	Reserved.	
	MUXSEL_AFE10SUB3[5:0]	5:0		
11BFh	**REG11BF**	**15:0**	**Default : 0x0000**	**Access : R/W**
	AFE_SENSE_MUXSEL[15:0]	15:0	Sensor used for AC noise sensing, enabled sensors must less than 12.	
11C0h	**REG11C0**	**15:0**	**Default : 0x0000**	**Access : R/W**
	AFE_SENSE_MUXSEL[31:16]	15:0	See description of '11BFh'.	
11C1h	**REG11C1**	**15:0**	**Default : 0x0000**	**Access : R/W**
-		15:14	Reserved.	
	AFE_SENSE_MUXSEL[45:32]	13:0	See description of '11BFh'.	
11C2h	**REG11C2**	**15:0**	**Default : 0x0000**	**Access : R/W**
-		15:14	Reserved.	

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	CSUBSEL_AFE1SUB0_AFE1SUB0_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE0SUB0_AFE0SUB0_P0[5:0]	5:0	Subtraction cap selection for each AFE, each subframe, PRS=0.	
11C3h	REG11C3	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE3SUB0_AFE3SUB0_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE2SUB0_AFE2SUB0_P0[5:0]	5:0		
11C4h	REG11C4	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE5SUB0_AFE1SUB1_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE4SUB0_AFE0SUB1_P0[5:0]	5:0		
11C5h	REG11C5	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE7SUB0_AFE3SUB1_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE6SUB0_AFE2SUB1_P0[5:0]	5:0		
11C6h	REG11C6	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE9SUB0_AFE1SUB2_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE8SUB0_AFE0SUB2_P0[5:0]	5:0		
11C7h	REG11C7	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE11SUB0_AFE3SUB2_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE10SUB0_AFE2SUB2_P0[5:0]	5:0		
11C8h	REG11C8	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE1SUB1_AFE1SUB3_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE0SUB1_AFE0SUB3_P0[5:0]	5:0		

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
11C9h	REG11C9	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE3SUB1_AFE3SUB3_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE2SUB1_AFE2SUB3_P0[5:0]	5:0		
11CAh	REG11CA	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE5SUB1_AFE1SUB4_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE4SUB1_AFE0SUB4_P0[5:0]	5:0		
11CBh	REG11CB	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE7SUB1_AFE3SUB4_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE6SUB1_AFE2SUB4_P0[5:0]	5:0		
11CCh	REG11CC	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE9SUB1_AFE1SUB5_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE8SUB1_AFE0SUB5_P0[5:0]	5:0		
11CDh	REG11CD	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE11SUB1_AFE3SUB5_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE10SUB1_AFE2SUB5_P0[5:0]	5:0		
11CEh	REG11CE	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE1SUB2_AFE1SUB6_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE0SUB2_AFE0SUB6_P0[5:0]	5:0		
11CFh	REG11CF	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE3SUB2_AFE3SUB6_P0[5:0]	13:8		
	-	7:6	Reserved.	

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description		
	CSUBSEL_AFE2SUB2_AFE2SUB6_P0[5:0]	5:0			
11D0h	REG11D0	15:0	Default : 0x0000		Access : R/W
	-	15:14	Reserved.		
	CSUBSEL_AFE5SUB2_AFE1SUB7_P0[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE4SUB2_AFE0SUB7_P0[5:0]	5:0			
11D1h	REG11D1	15:0	Default : 0x0000		Access : R/W
	-	15:14	Reserved.		
	CSUBSEL_AFE7SUB2_AFE3SUB7_P0[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE6SUB2_AFE2SUB7_P0[5:0]	5:0			
11D2h	REG11D2	15:0	Default : 0x0000		Access : R/W
	-	15:14	Reserved.		
	CSUBSEL_AFE9SUB2_AFE1SUB8_P0[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE8SUB2_AFE0SUB8_P0[5:0]	5:0			
11D3h	REG11D3	15:0	Default : 0x0000		Access : R/W
	-	15:14	Reserved.		
	CSUBSEL_AFE11SUB2_AFE3SUB8_P0[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE10SUB2_AFE2SUB8_P0[5:0]	5:0			
11D4h	REG11D4	15:0	Default : 0x0000		Access : R/W
	-	15:14	Reserved.		
	CSUBSEL_AFE1SUB3_AFE1SUB9_P0[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE0SUB3_AFE0SUB9_P0[5:0]	5:0			
11D5h	REG11D5	15:0	Default : 0x0000		Access : R/W
	-	15:14	Reserved.		
	CSUBSEL_AFE3SUB3_AFE3SUB9_P0[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE2SUB3_AFE2SUB9_P0[5:0]	5:0			
11D6h	REG11D6	15:0	Default : 0x0000		Access : R/W
	-	15:14	Reserved.		
	CSUBSEL_AFE5SUB3_AFE1SUB10_P0[5:0]	13:8			

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ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	-	7:6	Reserved.	
	CSUBSEL_AFE4SUB3_AFE0SUB10_P0[5:0]	5:0		
11D7h	**REG11D7**	**15:0**	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE7SUB3_AFE3SUB10_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE6SUB3_AFE2SUB10_P0[5:0]	5:0		
11D8h	**REG11D8**	**15:0**	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE9SUB3_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE8SUB3_P0[5:0]	5:0		
11D9h	**REG11D9**	**15:0**	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE11SUB3_P0[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE10SUB3_P0[5:0]	5:0		
11DAh	**REG11DA**	**15:0**	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE1SUB0_AFE1SUB0_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE0SUB0_AFE0SUB0_P1[5:0]	5:0	Subtraction cap selection for each AFE, each subframe, PRS=1.	
11DBh	**REG11DB**	**15:0**	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE3SUB0_AFE3SUB0_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE2SUB0_AFE2SUB0_P1[5:0]	5:0		
11DCh	**REG11DC**	**15:0**	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE5SUB0_AFE1SUB1_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE4SUB0_AFE0SUB1_P1[5:0]	5:0		
11DDh	**REG11DD**	**15:0**	Default : 0x0000	Access : R/W

Index	Mnemonic	Bit	Description	
ANA1 Register (Bank = 11)				
Index	**Mnemonic**	**Bit**	**Description**	
	-	15:14	Reserved.	
	CSUBSEL_AFE7SUB0_AFE3SUB1_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE6SUB0_AFE2SUB1_P1[5:0]	5:0		
11DEh	REG11DE	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE9SUB0_AFE1SUB2_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE8SUB0_AFE0SUB2_P1[5:0]	5:0		
11DFh	REG11DF	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE11SUB0_AFE3SUB2_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE10SUB0_AFE2SUB2_P1[5:0]	5:0		
11E0h	REG11E0	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE1SUB1_AFE1SUB3_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE0SUB1_AFE0SUB3_P1[5:0]	5:0		
11E1h	REG11E1	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE3SUB1_AFE3SUB3_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE2SUB1_AFE2SUB3_P1[5:0]	5:0		
11E2h	REG11E2	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE5SUB1_AFE1SUB4_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE4SUB1_AFE0SUB4_P1[5:0]	5:0		
11E3h	REG11E3	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE7SUB1_AFE3SUB4_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE6SUB1_AFE2SUB4_P1[5:0]	5:0		

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
11E4h	REG11E4	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE9SUB1_AFE1SUB5_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE8SUB1_AFE0SUB5_P1[5:0]	5:0		
11E5h	REG11E5	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE11SUB1_AFE3SUB5_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE10SUB1_AFE2SUB5_P1[5:0]	5:0		
11E6h	REG11E6	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE1SUB2_AFE1SUB6_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE0SUB2_AFE0SUB6_P1[5:0]	5:0		
11E7h	REG11E7	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE3SUB2_AFE3SUB6_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE2SUB2_AFE2SUB6_P1[5:0]	5:0		
11E8h	REG11E8	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE5SUB2_AFE1SUB7_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE4SUB2_AFE0SUB7_P1[5:0]	5:0		
11E9h	REG11E9	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE7SUB2_AFE3SUB7_P1[5:0]	13:8		
	-	7:6	Reserved.	
	CSUBSEL_AFE6SUB2_AFE2SUB7_P1[5:0]	5:0		
11EAh	REG11EA	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CSUBSEL_AFE9SUB2_AFE1SUB8_P1[5:0]	13:8		
	-	7:6	Reserved.	

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Index	Mnemonic	Bit	Description		
	CSUBSEL_AFE8SUB2_AFE0SUB8_P1[5:0]	5:0			
11EBh	REG11EB	15:0	Default : 0x0000	Access : R/W	
	-	15:14	Reserved.		
	CSUBSEL_AFE11SUB2_AFE3SUB8_P1[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE10SUB2_AFE2SUB8_P1[5:0]	5:0			
11ECh	REG11EC	15:0	Default : 0x0000	Access : R/W	
	-	15:14	Reserved.		
	CSUBSEL_AFE1SUB3_AFE1SUB9_P1[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE0SUB3_AFE0SUB9_P1[5:0]	5:0			
11EDh	REG11ED	15:0	Default : 0x0000	Access : R/W	
	-	15:14	Reserved.		
	CSUBSEL_AFE3SUB3_AFE3SUB9_P1[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE2SUB3_AFE2SUB9_P1[5:0]	5:0			
11EEh	REG11EE	15:0	Default : 0x0000	Access : R/W	
	-	15:14	Reserved.		
	CSUBSEL_AFE5SUB3_AFE1SUB10_P1[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE4SUB3_AFE0SUB10_P1[5:0]	5:0			
11EFh	REG11EF	15:0	Default : 0x0000	Access : R/W	
	-	15:14	Reserved.		
	CSUBSEL_AFE7SUB3_AFE3SUB10_P1[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE6SUB3_AFE2SUB10_P1[5:0]	5:0			
11F0h	REG11F0	15:0	Default : 0x0000	Access : R/W	
	-	15:14	Reserved.		
	CSUBSEL_AFE9SUB3_P1[5:0]	13:8			
	-	7:6	Reserved.		
	CSUBSEL_AFE8SUB3_P1[5:0]	5:0			
11F1h	REG11F1	15:0	Default : 0x0000	Access : R/W	
	-	15:14	Reserved.		
	CSUBSEL_AFE11SUB3_P1[5:0]	13:8			

ANA1 Register (Bank = 11)

Index	Mnemonic	Bit	Description	
	-	7:6	Reserved.	
	CSUBSEL_AFE10SUB3_P1[5:0]	5:0		
11F6h	REG11F6	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	AFE_VCOM_DET_CSUBSEL[5:0]	13:8	Csubsel settings for Vcom detection mode.	
	-	7:6	Reserved.	
	AFE_SENSE_CSUBSEL[5:0]	5:0	Csubsel settings for AC noise sensing mode.	
11F7h	REG11F7	15:0	Default : 0x0000	Access : R/W
	SENSOR_EN[15:0]	15:0	Enabled sensors, to define active and idle sensors.	
11F8h	REG11F8	15:0	Default : 0x0000	Access : R/W
	SENSOR_EN[31:16]	15:0	See description of '11F7h'.	
11F9h	REG11F9	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	SENSOR_EN[45:32]	13:0	See description of '11F7h'.	
11FAh	REG11FA	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	AFE_KEYSEL_SUB0[11:0]	11:0	Key or sensor selection.	
11FBh	REG11FB	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	AFE_KEYSEL_SUB1[11:0]	11:0		
11FCh	REG11FC	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	AFE_KEYSEL_SUB2[11:0]	11:0		
11FDh	REG11FD	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	AFE_KEYSEL_SUB3[11:0]	11:0		

ANA2 Register (Bank = 12)

Index	Mnemonic	Bit	Description	
1280h	REG1280	15:0	Default : 0x0000	Access : R/W
	PRS_COEFF[15:0]	15:0		
1281h	REG1281	15:0	Default : 0x0000	Access : R/W

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ANA2 Register (Bank = 12)

Index	Mnemonic	Bit	Description	
	-	15:8	Reserved.	
	PRS_COEFF[23:16]	7:0	See description of '1280h'.	
1282h	**REG1282**	**15:0**	**Default : 0x0000**	**Access : R/W**
	PRS_SEED[15:0]	15:0		
1283h	**REG1283**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:8	Reserved.	
	PRS_SEED[23:16]	7:0	See description of '1282h'.	
1284h	**REG1284**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:4	Reserved.	
	PRS_SHIFT_SEL[2:0]	3:1	(atgen_PRS_SHIFT_SEL == 3'h0) ? (dig_prs_en) : (atgen_PRS_SHIFT_SEL == 3'h1) ? (~dig_prs_en) : (atgen_PRS_SHIFT_SEL == 3'h2) ? (chop ^ (dig_prs_en)) : (atgen_PRS_SHIFT_SEL == 3'h3) ? (chop ^ (~dig_prs_en)) : (atgen_PRS_SHIFT_SEL == 3'h4) ? (sh_reg[0] ^ (dig_prs_en)) : (atgen_PRS_SHIFT_SEL == 3'h5) ? (sh_reg[0] ^ (~dig_prs_en)) : (atgen_PRS_SHIFT_SEL == 3'h6) ? 1'b0 : 1'b1;	
	PRS_SEED_LOAD	0		
1285h	**REG1285**	**15:0**	**Default : 0x0000**	**Access : R/W**
	CH_EN_SUB3[3:0]	15:12	Enabled channel numbers for subframe 3 (subframe <=4).	
	CH_EN_SUB2[3:0]	11:8	Enabled channel numbers for subframe 2 (subframe <=4).	
	CH_EN_SUB1[3:0]	7:4	Enabled channel numbers for subframe 1 (subframe <=4).	
	CH_EN_SUB0[3:0]	3:0	Enabled channel numbers for subframe 0 (subframe <=4). Enabled channel numbers for all subframes (subframe = 5~11).	
128Ah	**REG128A**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:8	Reserved.	
	STGEN_SCAN_RATE_SEL[4:0]	7:3	Scan rate timer period (4ms~35ms).	
	STGEN_SYNC_MODE[1:0]	2:1	System timing gen mode. 2'b00: one-shot mode. 2'b01: free-run mode.	
	STGEN_SW_TRIG	0	System timing gen software one-shot trigger.	
128Bh	**REG128B**	**15:0**	**Default : 0x0000**	**Access : R/W**
	-	15:5	Reserved.	
	SF_NUM[3:0]	4:1	Subframe numbers, 0:1subframe, 1:2subframe.	

ANA2 Register (Bank = 12)

Index	Mnemonic	Bit	Description	
	ATGEN_SYNC_MODE	0	0: Freerun; 1: vcom_sync.	
128Ch	REG128C	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	SMP_N2[8:0]	13:5	N2, edge numbers per re-sync, 0:1.	
	SMP_N1[4:0]	4:0	N1, samples per edge triggered, 0:1.	
128Dh	REG128D	15:0	Default : 0x0000	Access : R/W
	-	15:9	Reserved.	
	SMP_NUM0[8:0]	8:0	Sample number for subframe 0. (if subrame>4, all sample numbers will follow SMP_NUM0).	
128Eh	REG128E	15:0	Default : 0x0000	Access : R/W
	-	15:9	Reserved.	
	SMP_NUM1[8:0]	8:0	Sample number for subframe 1.	
128Fh	REG128F	15:0	Default : 0x0000	Access : R/W
	-	15:9	Reserved.	
	SMP_NUM2[8:0]	8:0	Sample number for subframe 2.	
1290h	REG1290	15:0	Default : 0x0000	Access : R/W
	-	15:9	Reserved.	
	SMP_NUM3[8:0]	8:0	Sample number for subframe 3.	
1291h	REG1291	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	SYNC_DET_TOUT[11:0]	11:0	Sync. Detection timeout, step 4T, 0: no timeout.	
1292h	REG1292	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	CHARGE_RST_DUR[7:0]	13:6	Charge(SW1) duration, step 8T, 0: 8T.	
	PRE_IDLE_DUR[5:0]	5:0	Pre idle duration, step 4T, 0: no pre_idle.	
1293h	REG1293	15:0	Default : 0x0000	Access : R/W
	SW2R_2_SW3R_DLY[3:0]	15:12	SW2 rising to SW3 rising, step 8T, 0:0.	
	SW1F_2_SW2R_DLY[3:0]	11:8	SW1 falling to SW2 rising, step 8T, 0:8T.	
	SW1R_2_SW5R_DLY[7:0]	7:0	SW1 rising to SW5 rising, step 8T, 0:8T.	
1294h	REG1294	15:0	Default : 0x0000	Access : R/W
	-	15:12	Reserved.	
	SW3F_2_SW2F_DLY[3:0]	11:8	SW3 falling to SW2 falling, step 8T, 0:0.	
	RST_DUR[7:0]	7:0	Reset duration, step 8T, 0: 8T.	

ANA2 Register (Bank = 12)

Index	Mnemonic	Bit	Description	
1295h	REG1295	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	
	SW2F_2_SW4R_DLY[1:0]	9:8	SW2 falling to SW4 rising non-overlapping, step 4T, 0:4T.	
	DUMP_DUR[7:0]	7:0	SW2 duration, step 8T, 0:8T.	
1296h	REG1296	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	
	POST_IDLE0_DUR[9:0]	9:0	Post idle time 0, step 1T, 0: no post idle.	
1297h	REG1297	15:0	Default : 0x0000	Access : R/W
	-	15:10	Reserved.	
	POST_IDLE1_DUR[9:0]	9:0	Post idle time 1, step 1T, 0: no post idle.	
1298h	REG1298	15:0	Default : 0x0000	Access : R/W
	SW4R_2_SMPR_DLY[3:0]	15:12	SW4 rising to sample start delay, step 8T, 0:8T.	
	-	11:10	Reserved.	
	POST_IDLE2_DUR[9:0]	9:0	Post idle time 2, step 1T, 0; no post idle.	
1299h	REG1299	15:0	Default : 0x0000	Access : R/W
	ADC_LAT_DLY[3:0]	15:12	Adc analog + digital pipe delay.	
	ADC_CONV_DUR[3:0]	11:8	Adc conversion duration due to pipe delay after 12 samples input is done, step 4T, 0:4T.	
	ADCPDF_2_SMPR_DLY[3:0]	7:4	Adc power down release before sample start, step 4T, should be fixed to 40T, 0:0, , may have 0~4T variation.	
	SMPR_2_SW4F_DLY[3:0]	3:0	Sample start to SW4 falling delay, step 4T, should be fixed delay for 12 sampling input, 0:4T.	
129Ah	REG129A	15:0	Default : 0x0000	Access : R/W
	-	15:13	Reserved.	
	PH_DLY_STEP[4:0]	12:8	Phase delay step for phase training, step 8T.	
	SF_IDLE_DUR[7:0]	7:0	Idle duration between subframes, step 8T, 0:0.	
129Bh	REG129B	15:0	Default : 0x0000	Access : R/W
	-	15:13	Reserved.	
	PH_DLY_R_BASE[12:0]	12:0	Phase delay sweep initial value for rising edge, step 1T.	
129Ch	REG129C	15:0	Default : 0x0000	Access : R/W
	-	15:13	Reserved.	
	PH_DLY_F_BASE[12:0]	12:0	Phase delay sweep initial value for falling edge, step 1T.	
129Dh	REG129D	15:0	Default : 0x0000	Access : R/W

ANA2 Register (Bank = 12)

Index	Mnemonic	Bit	Description	
	DET_AF_RSTF[3:0]	15:12	Analog dropping window after reset(SW1) falling, step 8T, 0:8T.	
	DET_BF_RSTF[3:0]	11:8	Analog dropping window before reset(SW1) falling, step 8T, 0:8T.	
	DET_AF_SW3F[3:0]	7:4	Analog dropping window after SW3 falling, step 8T, 0:8T.	
	DET_BF_SW3F[3:0]	3:0	Analog dropping window before SW3 falling, step 8T, 0:8T.	
129Eh	REG129E	15:0	Default : 0x0000	Access : R/W
	-	15:13	Reserved.	
	ADC_DESP_CODE[12:0]	12:0	ADC de-spreading code (center value).	
12B0h	REG12B0	15:0	Default : 0x0000	Access : RO
	-	15:2	Reserved.	
	VCOM_FDET_TOUT_FLAG	1	Vcom freq. Detection timeout flag.	
	VCOM_FDET_DONE	0	Vcom freq. Detection done flag.	
12B1h	REG12B1	15:0	Default : 0x0000	Access : RO
	VCOM_FDET_H_DUR[15:0]	15:0	Vcom freq. Detection high duration results.	
12B2h	REG12B2	15:0	Default : 0x0000	Access : RO
	-	15:2	Reserved.	
	VCOM_FDET_H_DUR[17:16]	1:0	See description of '12B1h'.	
12B3h	REG12B3	15:0	Default : 0x0000	Access : RO
	VCOM_FDET_L_DUR[15:0]	15:0	Vcom freq. Detection low duration results.	
12B4h	REG12B4	15:0	Default : 0x0000	Access : RO
	-	15:2	Reserved.	
	VCOM_FDET_L_DUR[17:16]	1:0	See description of '12B3h'.	
12B6h	REG12B6	15:0	Default : 0x0000	Access : RO
	VCOM_SYNC_H_AVG16[15:0]	15:0	Vcom high duration monitoring.	
12B7h	REG12B7	15:0	Default : 0x0000	Access : RO
	VCOM_SYNC_L_AVG16[15:0]	15:0	Vcom low duration monitoring.	
12B8h	REG12B8	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	VCOM_AMP_AVG16[12:0]	12:0	Vcom amplitude monitoring.	
12C0h	REG12C0	15:0	Default : 0x0000	Access : RO

ANA2 Register (Bank = 12)

Index	Mnemonic	Bit	Description	
	-	15:9	Reserved.	
	ADC_CAL_DONE	8		
	ADC_CALOUT[7:0]	7:0		
12C6h	REG12C6	15:0	Default : 0x0000	Access : RO
	-	15:1	Reserved.	
	GAIN_TRAIN_DONE	0	Vcom gain training done flag.	
12C7h	REG12C7	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G0[12:0]	12:0	Vcom gain training results.	
12C8h	REG12C8	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G1[12:0]	12:0	Vcom gain training results.	
12C9h	REG12C9	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G2[12:0]	12:0	Vcom gain training results.	
12CAh	REG12CA	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G3[12:0]	12:0	Vcom gain training results.	
12CBh	REG12CB	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G4[12:0]	12:0	Vcom gain training results.	
12CCh	REG12CC	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G5[12:0]	12:0	Vcom gain training results.	
12CDh	REG12CD	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G6[12:0]	12:0	Vcom gain training results.	
12CEh	REG12CE	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G7[12:0]	12:0	Vcom gain training results.	
12CFh	REG12CF	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_G8[12:0]	12:0	Vcom gain training results.	
12D0h	REG12D0	15:0	Default : 0x0000	Access : RO

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ANA2 Register (Bank = 12)

Index	Mnemonic	Bit	Description	
	-	15:13	Reserved.	
	ADC_DATA_G9[12:0]	12:0	Vcom gain training results.	
12D1h	REG12D1	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_GA[12:0]	12:0	Vcom gain training results.	
12D2h	REG12D2	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_GB[12:0]	12:0	Vcom gain training results.	
12D3h	REG12D3	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_GC[12:0]	12:0	Vcom gain training results.	
12D4h	REG12D4	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_GD[12:0]	12:0	Vcom gain training results.	
12D5h	REG12D5	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_GE[12:0]	12:0	Vcom gain training results.	
12D6h	REG12D6	15:0	Default : 0x0000	Access : RO
	-	15:13	Reserved.	
	ADC_DATA_GF[12:0]	12:0	Vcom gain training results.	
12E0h	REG12E0	15:0	Default : 0x0000	Access : R/W
	STGEN_TST_S_SEL[3:0]	15:12	Stgen status selection.	
	STGEN_TST_B_SEL[3:0]	11:8	Stgen testbus selection.	
	TGEN_TST_S_SEL[3:0]	7:4	Tgen status selection.	
	TGEN_TST_B_SEL[3:0]	3:0	Tgen testbus selection.	
12E1h	REG12E1	15:0	Default : 0x0000	Access : R/W
	FDET_TST_S_SEL[3:0]	15:12	Fdet status selection.	
	FDET_TST_B_SEL[3:0]	11:8	Fdet testbus selection.	
	GTRAIN_TST_S_SEL[3:0]	7:4	Gtrain status selection.	
	GTRAIN_TST_B_SEL[3:0]	3:0	Gtrain testbus selection.	
12E2h	REG12E2	15:0	Default : 0x0000	Access : R/W
	ATFSM_TST_S_SEL[3:0]	15:12	Atfsm status selection.	
	ATFSM_TST_B_SEL[3:0]	11:8	Atfsm testbus selection.	
	VGEN_TST_S_SEL[3:0]	7:4	Vgen status selection.	

ANA2 Register (Bank = 12)

Index	Mnemonic	Bit	Description	
	VGEN_TST_B_SEL[3:0]	3:0	Vgen testbus selection.	
12E3h	REG12E3	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	ATANA_TST_B1_SEL[5:0]	13:8	Atana testbus1 selection.	
	-	7:6	Reserved.	
	ATANA_TST_B0_SEL[5:0]	5:0	Atana testbus0 selection.	
12E4h	REG12E4	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	ATANA_TST_B3_SEL[5:0]	13:8	Atana testbus3 selection.	
	-	7:6	Reserved.	
	ATANA_TST_B2_SEL[5:0]	5:0	Atana testbus2 selection.	
12E5h	REG12E5	15:0	Default : 0x0000	Access : R/W
	-	15:14	Reserved.	
	ATGEN_DPAT_EN	13	Atgen internal desp pattern enable.	
	ATGEN_DPAT_INI[12:0]	12:0	Atgen internal desp pattern initial value.	
12EAh	REG12EA	15:0	Default : 0x0000	Access : RO
	TGEN_TST_S[15:0]	15:0	Tgen status.	
12F0h	REG12F0	15:0	Default : 0x0000	Access : R/W
	ANA2_RESERVED0[15:0]	15:0	Reserved.	
12F1h	REG12F1	15:0	Default : 0x0000	Access : R/W
	ANA2_RESERVED1[15:0]	15:0	Reserved.	
12F2h	REG12F2	15:0	Default : 0x0000	Access : R/W
	ANA2_RESERVED2[15:0]	15:0	Reserved.	
12F3h	REG12F3	15:0	Default : 0x0000	Access : R/W
	ANA2_RESERVED3[15:0]	15:0	Reserved.	
12F4h	REG12F4	15:0	Default : 0x0000	Access : R/W
	ANA2_RESERVED4[15:0]	15:0	Reserved.	
12F5h	REG12F5	15:0	Default : 0x0000	Access : R/W
	ANA2_RESERVED5[15:0]	15:0	Reserved.	
12F6h	REG12F6	15:0	Default : 0x0000	Access : R/W
	ANA2_RESERVED6[15:0]	15:0	Reserved.	
12F7h	REG12F7	15:0	Default : 0x0000	Access : R/W
	ANA2_RESERVED7[15:0]	15:0	Reserved.	

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FILTER Register (Bank = 13)

FILTER Register (Bank = 13)				
Index	**Mnemonic**	**Bit**	**Description**	
1380h~ 139Eh	- _	- -	Default :- Reserved.	Access :-
139Fh	REG139F	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS15[15:0]	15:0	0x3E. Fir_check_sum.	
13A0h	REG13A0	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS16[15:0]	15:0	0x40.	
13A1h	REG13A1	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS17[15:0]	15:0	0x42.	
13A2h	REG13A2	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS18[15:0]	15:0	0x44.	
13A3h	REG13A3	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS19[15:0]	15:0	0x46.	
13A4h	REG13A4	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS20[15:0]	15:0	0x48.	
13A5h	REG13A5	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS21[15:0]	15:0	0x4A.	
13A6h	REG13A6	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS22[15:0]	15:0	0x4C.	
13A7h	REG13A7	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS23[15:0]	15:0	0x4E.	
13A8h	REG13A8	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS24[15:0]	15:0	0x50.	
13A9h	REG13A9	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS25[15:0]	15:0	0x52.	
13AAh	REG13AA	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS26[15:0]	15:0	0x54.	
13ABh	REG13AB	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS27[15:0]	15:0	0x56.	
13ACh	REG13AC	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS28[15:0]	15:0	0x58.	
13ADh	REG13AD	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS29[15:0]	15:0	0x5A.	

FILTER Register (Bank = 13)

Index	Mnemonic	Bit	Description	
13AEh	REG13AE	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS30[15:0]	15:0	0x5C.	
13AFh	REG13AF	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS31[15:0]	15:0	0x5E.	
13B0h	REG13B0	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS32[15:0]	15:0	0x60.	
13B1h	REG13B1	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS33[15:0]	15:0	0x62.	
13B2h	REG13B2	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS34[15:0]	15:0	0x64.	
13B3h	REG13B3	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS35[15:0]	15:0	0x66.	
13B4h	REG13B4	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS36[15:0]	15:0	0x68.	
13B5h	REG13B5	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS37[15:0]	15:0	0x6A.	
13B6h	REG13B6	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS38[15:0]	15:0	0x6C.	
13B7h	REG13B7	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS39[15:0]	15:0	0x6E.	
13B8h	REG13B8	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS40[15:0]	15:0	0x70.	
13B9h	REG13B9	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS41[15:0]	15:0	0x72.	
13BAh	REG13BA	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS42[15:0]	15:0	0x74.	
13BBh	REG13BB	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS43[15:0]	15:0	0x76.	
13BCh	REG13BC	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS44[15:0]	15:0	0x78.	
13BDh	REG13BD	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS45[15:0]	15:0	0x7A.	
13BEh	REG13BE	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS46[15:0]	15:0	0x7C.	

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FILTER Register (Bank = 13)

Index	Mnemonic	Bit	Description	
13BFh	REG13BF	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS47[15:0]	15:0	0x7E.	
13C0h	REG13C0	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS48[15:0]	15:0	0x80.	
13C1h	REG13C1	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS49[15:0]	15:0	0x82.	
13C2h	REG13C2	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS50[15:0]	15:0	0x84.	
13C3h	REG13C3	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS51[15:0]	15:0	0x86.	
13C4h	REG13C4	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS52[15:0]	15:0	0x88.	
13C5h	REG13C5	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS53[15:0]	15:0	0x8A.	
13C6h	REG13C6	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS54[15:0]	15:0	0x8C.	
13C7h	REG13C7	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS55[15:0]	15:0	0x8E.	
13C8h	REG13C8	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS56[15:0]	15:0	0x90.	
13C9h	REG13C9	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS57[15:0]	15:0	0x92.	
13CAh	REG13CA	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS58[15:0]	15:0	0x94.	
13CBh	REG13CB	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS59[15:0]	15:0	0x96.	
13CCh	REG13CC	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS60[15:0]	15:0	0x98.	
13CDh	REG13CD	15:0	Default : 0x0000	Access : RO
	FILTER_STATUS61[15:0]	15:0	0x9A.	

PM_ANA_CAL Register (Bank = 14)

PM_ANA_CAL Register (Bank = 14)					
Index	**Mnemonic**	**Bit**	**Description**		
1480h	REG1480	15:0	Default : 0x0000		Access : R/W
	PM_ANA_CAL_LOG[15:0]	15:0	Analog calibration log.		
1481h	REG1481	15:0	Default : 0x0000		Access : R/W
	PM_ANA_CAL_LOG[31:16]	15:0	See description of '1480h'.		
14B0h	REG14B0	15:0	Default : 0x0004		Access : R/W
	-	15	Reserved.		
	PM_IIC_ID[6:0]	14:8	Pm no clock iic id.		
	-	7:3	Reserved.		
	PM_IIC_SOFT_RST	2	Pm no clock iic software reset.		
	-	1:0	Reserved.		
14B1h	REG14B1	15:0	Default : 0x0000		Access : R/W
	-	15:1	Reserved.		
	PM_IIC_WAKEUP_CLR	0	Pm no clock iic wake up clear.		

CHIPTOP Register (Bank = 1E)

CHIPTOP Register (Bank = 1E)					
Index	**Mnemonic**	**Bit**	**Description**		
1E80h ~1E81h	-	15:0	Default : -		Access : -
	-	-	Reserved.		
1E91h	REG1E91	15:0	Default : 0x0000		Access : R/W
	CKG_SPI_CLK[3:0]	15:12	Spi clock setting; [0]: Spi clock gated. [1]: Spi clock invert. [3:2]: spi clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.		

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Index	Mnemonic	Bit	Description
	CKG_UART_CLK[3:0]	11:8	Uart clock setting; [0]: Uart clock gated. [1]: Uart clock invert. [3:2]: uart clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.
	-	7:6	Reserved.
	CKG_FRO_DIV4_CLK[1:0]	5:4	Fro_div4 clock setting; [0]: Fro_div4 clock gated. [1]: Fro_div4 clock invert.
	CKG_MCU_CLK[3:0]	3:0	Mcu clock setting; [0]: Mcu clock gated. [1]: Mcu clock invert. [3:2]: mcu clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.
1E92h	REG1E92	15:0	Default : 0x0511 Access : R/W
	CKG_DB_CLK[3:0]	15:12	Db bus clock setting; [0]: Db bus clock gated. [1]: Db bus clock invert. [3:2]: db bus clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.
	CKG_DELTA_C_CLK[1:0]	11:10	Delta_c clock setting; [0]: Delta_c clock gated. [1]: Delta_c clock invert.
	CKG_CHIP_TGEN_CLK[1:0]	9:8	Cthcap frame clock setting; [0]: Analog timing gen clock gated. [1]: Analog timing gen clock invert.

Index	Mnemonic	Bit	Description	
	CHIPTOP Register (Bank = 1E)			
Index	**Mnemonic**	**Bit**	**Description**	
	CKG_CTS_FILTER_CLK[3:0]	7:4	Cts_filter clock setting; [0]: Cts_filter clock gated. [1]: Cts_filter clock invert. [3:2]: cts_filter clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.	
	CKG_ANA_TGEN_CLK[3:0]	3:0	Cthcap frame clock setting; [0]: Analog timing gen clock gated. [1]: Analog timing gen clock invert. [3:2]: analog timing gen clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.	
1E93h	**REG1E93**	**15:0**	**Default : 0x0410**	**Access : R/W**
	CKG_SSPI_CLK[3:0]	15:12	Sspi clock setting; [0]: Sspi clock gated. [1]: Sspi clock invert. [3:2]: sspi clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.	
	CKG_DW_IIC_CLK[3:0]	11:8	DW_IIC clock setting; [0]: Dw_iic clock gated. [1]: Dw_iic clock invert. [3:2]: dw_iic clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.	

CHIPTOP Register (Bank = 1E)

Index	Mnemonic	Bit	Description	
	CKG_DATA_FILTER_CLK[3:0]	7:4	Data_filter clock setting; [0]: Data_filter clock gated. [1]: Data_filter clock invert. [3:2]: data_filter clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.	
	CKG_EFUSE_CLK[3:0]	3:0	Efuse clock setting; [0]: Efuse clock gated. [1]: Efuse clock invert. [3:2]: efuse clock select. 2'b00: osc clock. 2'b01: osc clock / 2. 2'b10: osc clock / 4. 2'b11: osc clock / 8.	
1EB0h	REG1EB0	15:0	Default : 0x0000	Access : RO
	GPIO_IN[15:0]	15:0	PAD_GPIO_IN[15:0].	
1EB1h	REG1EB1	15:0	Default : 0x0000	Access : R/W
	GPIO_OUT[15:0]	15:0	PAD_GPIO_OUT[15:0].	
1EB2h	REG1EB2	15:0	Default : 0xFFFF	Access : R/W
	GPIO_OEN[15:0]	15:0	PAD_GPIO_OEN[15:0].	
1EFEh ~1EFFh	- _	15:0 -	Default : - Reserved.	Access : -

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
08/27/2012		Created first version.