Thuraya Satellite Telecommunications Company

THURAYA Second-Generation User Terminal

SM-2500 Technical Information Manual

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1 Introduction

1.1 Scope

The purpose of this document is to explain the hardware technical information and specifications of SM-2500, Thuraya satellite module. This document will be helpful to third party designers.

The AT command set for the SM-2500, is fully described in the document Thuraya Second Generation User Terminal AT Command Set.

1.2 Related documents

Table 1 Related documents

Document Number	Remark
	Thuraya Second Generation User Terminal AT Command Set
ETSI TS 101 376-5-5	GMR-1 05.05, and GMPRS-1 05.05 -Radio Transmission and Reception.

1.3 Terms and abbreviations

Table 2 Terms and abbreviatioins

Abbreviation	Description
SAT	Satellite.
GPS	Global Positioning System
PA	Power Amplifier
GMR	GEO Mobile Radio
RF	Radio Frequency
UART	Universal Asynchronous Receive and Transmitt
RTC	Real Time Clock

1.4 Overview

The Thuraya SM-2500 is a stand alone device which is able to access satellite mobile services via the GMR-1 and GRPRS-1 air interface, without additional components apart from the following: SAT antenna, GPS antenna, keypad, LCD, GSM Module, Bluetooth Module and battery / power supply.

The following Figure1 and Figure 2 shows the outline of SM-2500 and external interfaces that sat antenna RF connector, GPS antenna connector and 100 pins of board to board connector.

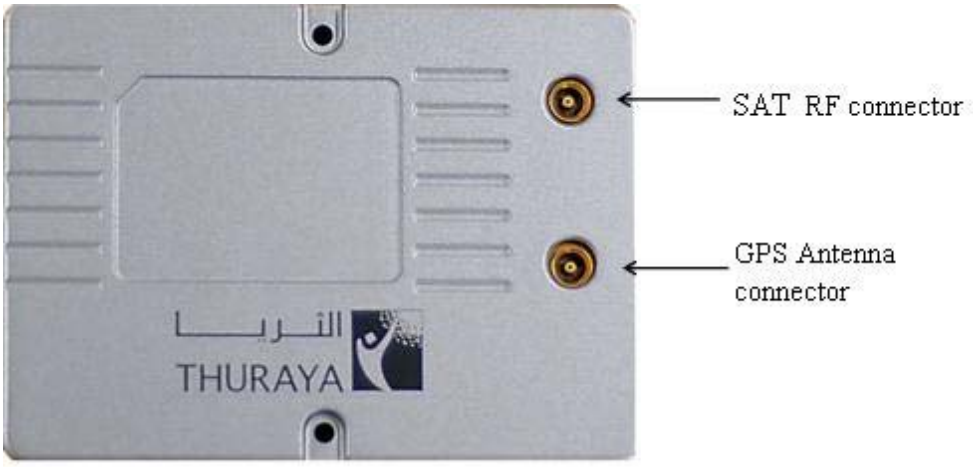


Figure 1 Top side

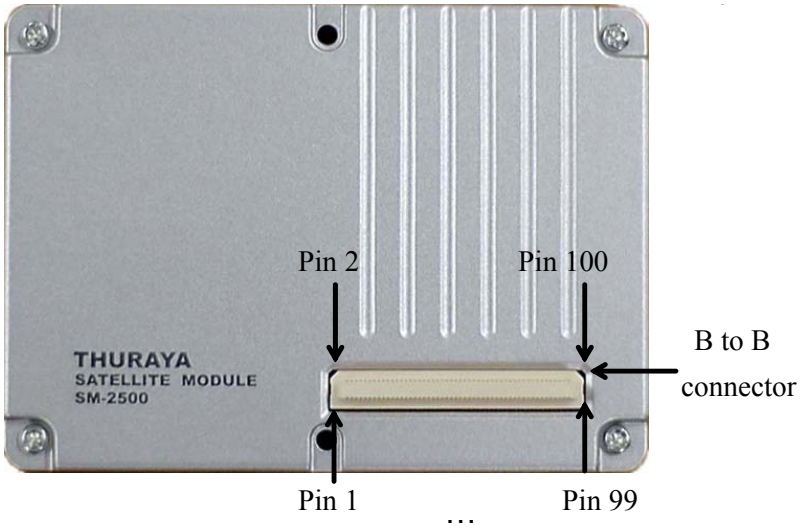


Figure 2 Bottom side

2 Pin description

SAT module has 100-pins B-to-B connector for interface with external device. Each pin, its designated function and interface is shown in Table 3 .

Table 3 Pin functional and electrical description

PIN NAME	I/O	DESCRIPTION	ELECTRICAL SPEC.
VPWR	I	6 pin-allotted VPWR at board-to-board of SAT Module use as power and allowed input Voltage is +3.2~4.5V. Supply max current: 300 ㎃ (at 3.7, VEXT not used)	$V_I$max = +4.5V $V_I$min = +3.2V $V_I$typ = +3.7V
5V_TX	I	Pin-allotted 5V_TX at board-to-board of SAT Module use as input power of RF power amplifier and allowed input Voltage is +4.8V~5.3V. This power supply has to be low ripple noise (max 50 ㎷: 1 ㎒~100 ㎒) and enable to supply 1.5A (at 5V) of peak voltage well when TX transmit burst.	$V_I$max = +5.3 V $V_I$min = +4.8V $V_I$typ = +5.0V
VEXT	O	Power to supply external 3V. Do not exceed the Load current of 200 ㎃.	$V_O$max = +3.1V $V_O$min = +2.9V $V_O$typ = +3.0V I_{OL}max = 200 ㎃
LCD_D[0:7]	I/O	8bit bi-directional data bus for LCD data	V_{OH}min = 2.4V V_{OL}max = 0.6V I_{OL} = 4 ㎃ V_{IH}min = 2.1V V_{IL}max = 0.9V I_{IL} = 1 ㎂
/LCD_CS	O	LCD chip select output pin. Data/Iinstruction is enabled only when LCD_CS is low level.	
/LCD_RD	O	Servers as a read strobe signal and read data at the low level.	
/LCD_WR	O	Servers as a write strobe signal and write data at the low level.	
LCD_RS	O	Data/Instruction select output pin H:LCD_D[0:7] are display data L: LCD_D[0:7] are instruction data	
LCD_EN	O	External LCD part power enable output pin. Active high	V_{OH}min = 2.5V V_{OL}max = 0.8V I_{OL} = 8 ㎃
/LCD_RESET	O	LCD reset output pin. When /LCD_RESET is low level, initialization is executed.	
LCD_BL_EN	O	White LED to backlight of LCD module enable pin. Active high	
LCD_DIM	O	White LCD to backlight of LCD module dimming control	V_{OH}min = 2.4V

		pin.	V_{OL}max = 0.6V I_{OL} = 4 mA
KBR[00:04]	I	Row line input pin of keypad matrix.	V_{IH}min = 2.1V V_{IL}max = 0.9V I_{IL} = 1 µA
KBC[00:04]	O	Column line input pin of keypad matrix.	V_{OH}min = 2.4V V_{OL}max = 0.6V I_{OL} = 4 mA
KEYPAD_BL_EN	O	Keypad backlight enable output pin. Active high	V_{OH}min = 2.5V V_{OL}max = 0.8V I_{OL} = 8 mA
UART1_TXD	O	UART1 serial data output	See table 5 and table 6
UART1_RXD	I	UART1 serial data input.	
UART1_CTS	I	UART1 clear to send input.	
UART1_RTS	O	UART1 request to send output.	
UART1_DTR	O	UART1 data transmit ready output.	
UART1_DSR	I	UART1 data set ready input.	
UART1_DCD	O	UART1 data carrier detect output	
UART1_RI	O	UART1 ring indicator output.	
UART2_TXD	O	UART2 serial data output.	
UART2_RXD	I	UART2 serial data input.	
UART2_RTS	O	UART2 request to send output.	
UART2_CTS	I	UART2 clear to send input.	
I2C_SCL	O	I2C serial clock output.	V_{IH}min = 2.1V V_{IL}max = 0.9V V_{OL}max = 0.4V I_{OL} = 3 mA
I2C_SDA	I/O	I2C serial bi-directional data.	
/I2C_INT	I	External I2C device detect and interrupt input.	V_{IH}min = 2.1V V_{IL}max = 0.9V I_{IL} = 20 µA
USB_VBUS	I	USB device detection input.	V_{IH}min = 3.0V V_{IL}max = 0.5V

			I_{IL} = 10 µA
USB_DP	I/O	USB data plus	V_{IH}min = 2.1V V_{IL}max = 0.75V V_{OH}min = 2.0V V_{OL}max = 0.8V I_{OL} = 18.3 mA
USB_DM	I/O	USB data minus	
SAT_ON	I	Input pin to power SAT module on	V_{IH}min = 2.5V V_{IL}max = 0.5V I_{IL} = 10 µA
SAT_OFF	I	Input pin that to power off the SAT module.	V_{IH}min = 2.1V V_{IL}max = 0.75V I_{IL} = 2 mA
/SAT_RESET	I	Input pin to initialize SAT module. When boot up of SAT module, reset signal is generated by internal circuit to fit the processor reset timing, so it doesn't need to generate at external circuit. This pin has an internal pull-up 20 kΩ resistor.	V_{IH}min = 2.1V V_{IL}max = 0.75V Id = 20 mA
SAT_STATUS	O	Output pin to inform a condition of SAT module to HOST.	V_{OH}min = 2.5V V_{OL}max = 0.8V I_{OL} = 8 mA
SAT_WAKEUP	I	Input pin to wake SAT module up of sleep condition.	V_{IH}min = 2.1V V_{IL}max = 0.9V I_{IL} = 20 µA
HOST_STATUS	I	Input pin to recognize condition of HOST at SAT module.	V_{IH}min = 2.1V V_{IL}max = 0.9V I_{IL} = 20 µA
HOST_WAKEUP	O	Output pin to wake SAT module up before sending data to HOST when HOST device is in sleep condition.	V_{OH}min = 2.4V V_{OL}max = 0.6V I_{OL} = 4 mA
GPIO1	I/O	General purpose I/O 1. User can control at command of user's own accord.	V_{IH}min = 2.0V V_{IL}max = 0.8V I_{IL} = - 1 µA
GPIO2	I/O	General purpose I/O 2.	

		User can control at command of user's own accord.	I_{IH} = 1 µA V_{OH}min = 2.5V V_{OL}max = 0.8V I_{OL} = 8 mA
SIM_VDD	O	Supply voltage for SIM card.	1.8V SIM: Vmin = +1.71V Vmax = +1.89V Vtyp = +1.8V **3.0V SIM**: Vmin = +2.8V Vmax = +3.2V Vtyp = +3.0V Id_{typ} = 50 mA(max:150 mA)
SIM_DATA	I/O	SIM card serial data.	**1.8V SIM**: V_{IH}min = 0.7*SIM_VDD V_{IL}max = 0.4V V_{OH}min = 0.8*SIM_VDD V_{OL}min = 0.4V **3.0V SIM**: V_{IH}min = 0.7*SIM_VDD V_{IL}max = 0.2*SIM_VDD V_{OH}min = 0.8*SIM_VDD V_{OL}min = 0.4V
SIM_RST	O	SIM card reset.	1.8V SIM: V_{OH}min = 0.9*SIM_VDD V_{OL}max = 0.2*SIM_VDD 3.0V SIM: V_{OH}min = 0.9*SIM_VDD V_{OL}max = 0.4V
SIM_CLK	O	SIM card serial clock.	
VRTC	I	Backup power pin to supply power to interior RTC block when power is not supplied to module. This pin is used as voltage supply to fill up exterior battery	V_{IN}max = +5.5V V_{IN}min = +2.0V

		when power is supplied to module.	V_{IN}typ = +3V Idd = 15 µA (max)
DAI_DIN	I	Input data for digital audio interface.	
DAI_DOUT	O	Output data for digital audio interface.	
DAI_CLK	O	Clock for digital audio interface.	
DAI_SYNC	O	Frame sync for digital audio interface.	
CODEC_SEL	I	Selects the internal or external PCM CODEC. H: external, L: internal	V_{IH}min = 2.0V V_{IL}max = 0.8V I_{IL} = - 1 µA I_{IH} = 1 µA
SPK+	O	Positive speaker output.	See Section 8.4
SPK-	O	Negative speaker output.	
MIC+	I	Positive mic input.	
MIC-	I	Negative mic input.	
BUZZER	O	External buzzer control output.	V_{OH}min = 2.4V V_{OL}max = 0.6V I_{OL} = 4 mA
GND		Gound	

3 Power supply

The power requirements of SAT module is composed as dual voltage source of VPWR (3.2V~4.5V) and 5V_TX (4.8V~5.3V).
The 5V_TX supply the internal Transmit Power amplifier, it has been separated from the other supplies to reduce the effects of voltage ripple on the module components.
The ripple noise level of the power supply has to be limited to 50mV RMS in the 1㎒ ~ 100㎒ frequency range.
The requirements of the two power supplies are described in follow sections

3.1 VPWR

VPWR is main power source supplied at entire circuit except PA power in SAT module.

The suppled voltage range at VPWR is from 3.2V to 4.5V.
The internal ASIC in the module will detect voltage level of these pins.
If these pins are below 3.2V, module is power off, so when you design the power supply applications, it must be considered that the power source be able to provide sufficient current (350㎃).

User can read to the voltage level of these pins as using AT command.(State AT-Command)

The design considerations should incorporate the following:

- Power supply lines must be able to carry the rated 350㎃(@3.7V) current
- kept short as possible to reduce lines impedance.
- Bypass capacitors must be added to the power supply lines minimum of 33μF MLCC (Multi-layer ceramic chip) or tantalum capacitor of low ESR for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes and small value ceramic capacitor in parallel as close as posible to the B-to-B connector.

3.2 5V_TX

5V_TX is main power source for internal PA (power amplifier) in SAT module.

In some case, the ripple in a transmit burst may cause voltage drops when current consumption rises to typical peaks of 1.5A (5V), so the power supply must be able to provide sufficient current up to 1.5A.
These pins shouldn't be drops below 4.8V.
If voltage of these pins is below 4.8V, module will not process the call.
The best way to reducing voltage drops is using the low impedance power source including power supply lines and ESR value of the bypass capacitors.

We recommend that design implements the use linear regulators what has low ripple noise and good transient response as source power.

.

5V_TX input capacitor depends on the impedance of the source supply and input power ripple. To satisfy this high RMS current demand, two 150 µF (10V) are required.

In parallel with these bulk capacitors, two 47 µF (10V), low ESR (X5R) ceramic capacitors are added for HF noise reduction.

Power consumption timing diagrams is in figure 3 at talk time.

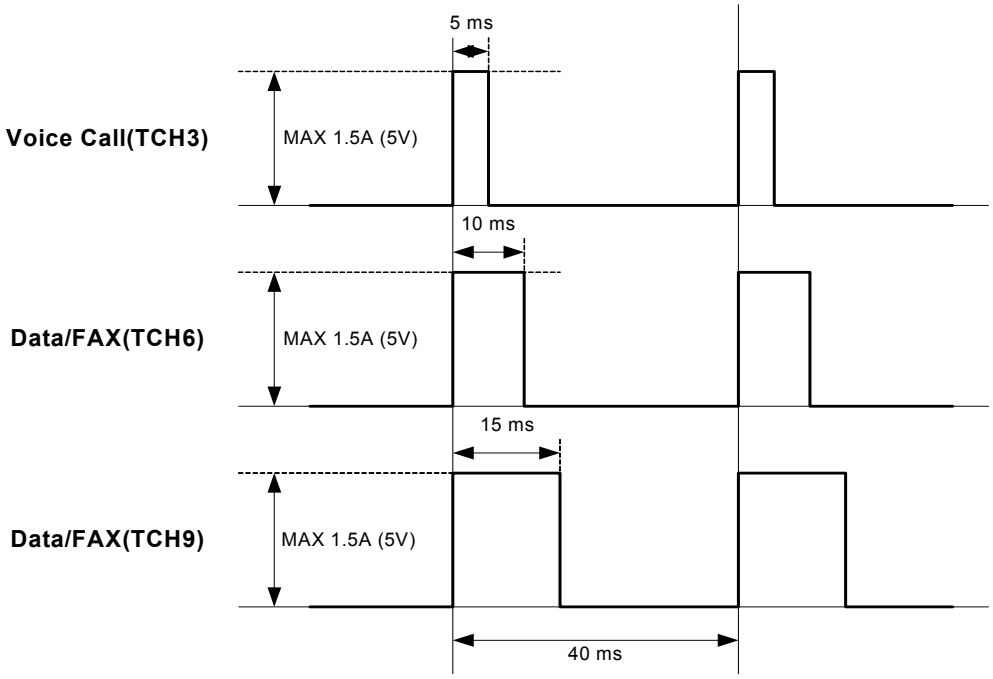


Figure 3 5V_TX timing diagrams on each talk mode

3.3 Power supply design solutions

The designer should select power supply taking into consideration the following items :
1. Ripple noise should be minimal.
2. Transient response should be very good.
3. Output current should be able to support enough current to each PIN
4. Whether Volatge and Current accuracy is guaranteed

3.3.1 Power supply design examples

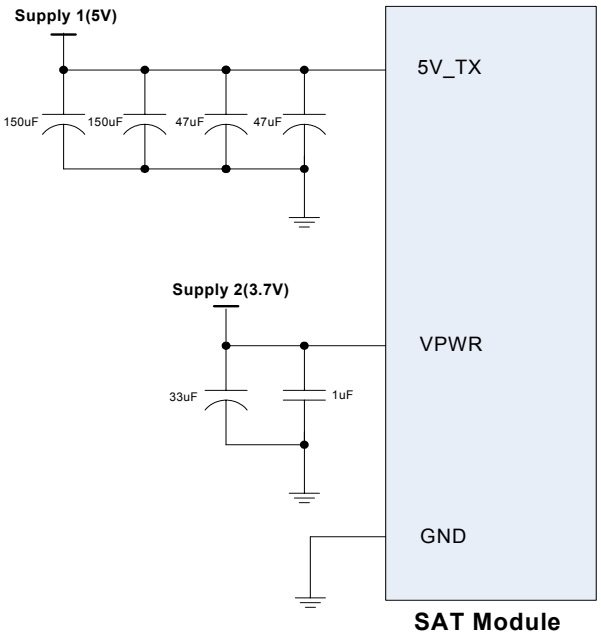


Figure 4 Dual power souce reference circuit

The example in Figure 4 is applicable to the power which has double voltage such as 5V and 3.7V.

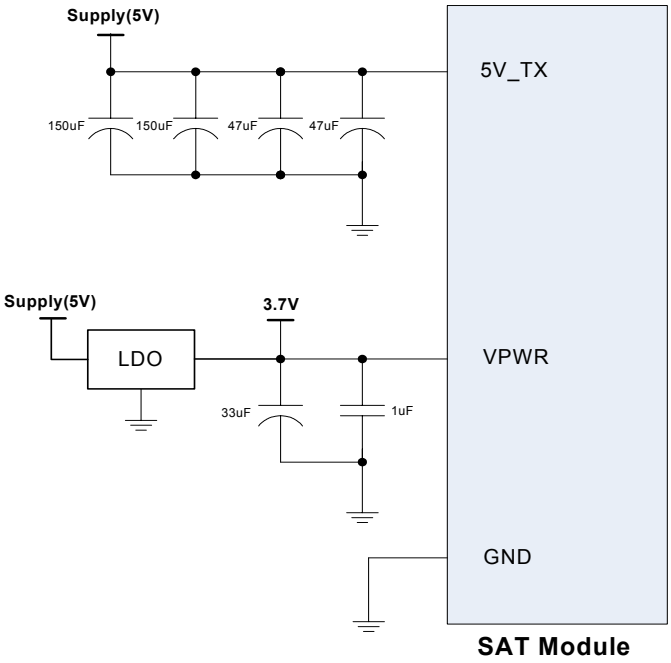


Figure 5 Single 5v power source reference circuit

The example Figure 5 is applicable to single power which has voltage of 5V.
Connect main power and 5V_TX directly, and connect VPWR after putting voltage down as 3.7V by using LDO.
Attention to that the LDO should be selected that enable to supply current of 350mA at VPWR well.

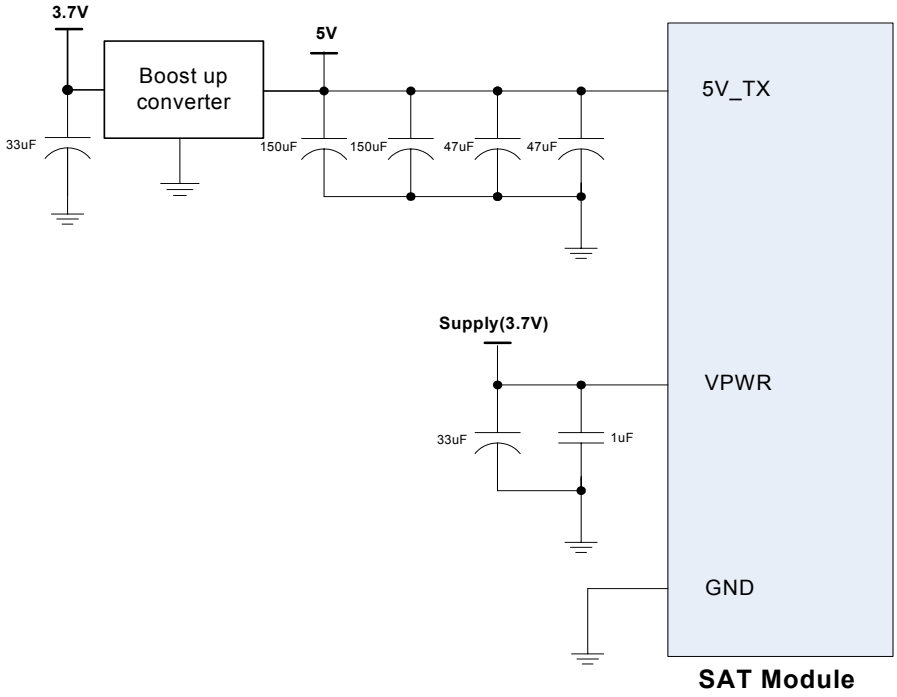


Figure 6 3.7v single power source reference circuit

The example in Figure 6 is for a general 3.7V 1-Cell Li-Ion battery. Main source power is directly connected wich VPWR and boost-up converter is used to allow the voltage which is proper to 5V_TX. The design should be able to supply enough current to the entire system, and boost-up converter should be able to supply enough current to 5V_TX.

4 Control signals

There are 7-pins for control SAT module. It is pins for SAT_ON, SAT_OFF, /SAT_RESET, SAT_WAKEUP, HOST_WAKEUP, SAT_STATUS, and HOST_STATUS.

The status of SAT mudule and HOST is shown in Figure 7 according to each of the control signals timing.

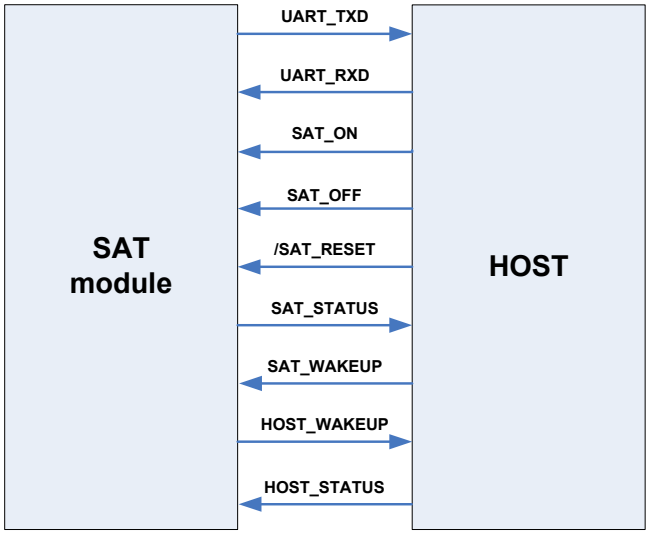


Figure 7 Connection diagram of control signals

Functions of each control signal are described in the following sections.

4.1 SAT_STATUS

This signal is used to inform the current condition of SAT Module to HOST.

If this signal is low level, SAT module is status of IDLE(wakeup), and if this signal is high level, SAT module is status of SLEEP as shown in Figure 8.
The designer can prevent to loss of data, because the HOST knows status of module whether in sleep status or not, before the data is transmitted from HOST to SAT module.

This signal shoulod remain floating if this function is not going to be used.

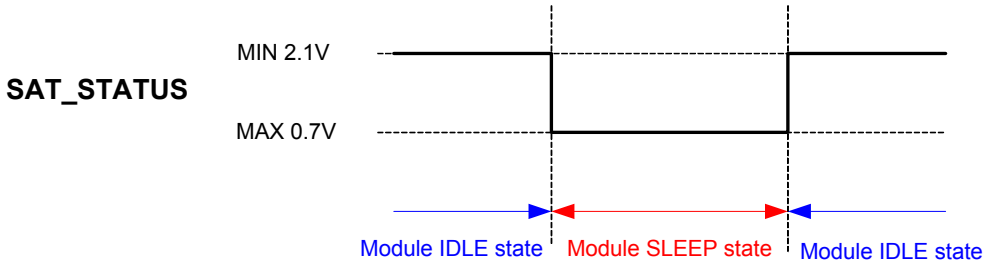


Figure 8 SAT_STATUS timing diagram

4.2 SAT_WAKEUP

This signal is used for waking up SAT Module before data transmission to prevent loss of data delivered from HOST when SAT Module is in SLEEP condition.

If you make this signal as rising high when SAT module is status of SLEEP, it is awakened from SLEEP condition.

Detail timing diagram is shown in Figure 9.

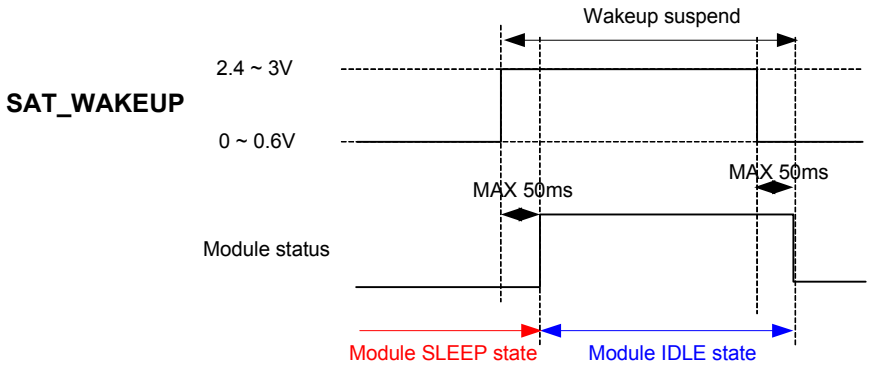


Figure 9 SAT_WAKEUP timing diagram

4.3 HOST_STATUS

This signal is used for informing current status of HOST to SAT Module.

When this signal is at a logic high level the host is available to receive commands, when the signal is low the HOST is in Sleep mode

If HOST is always staus of IDLE, you must make this signal at a logic high state by pulling it to a logic high state.

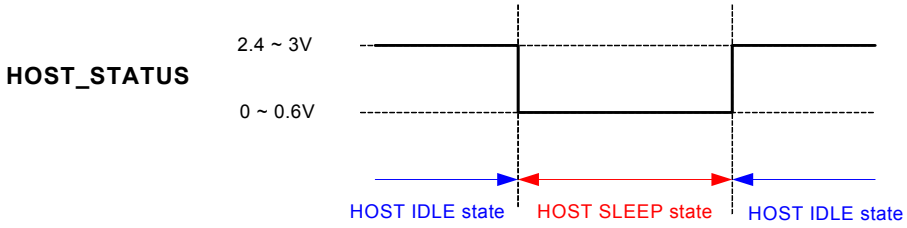


Figure 10 HOST_STATUS timing diagram

4.4 HOST_WAKEUP

This signal is used for waking up HOST before data transmission to prevent loss of data delivered from SAT Module when HOST is in SLEEP condition.

This signal should remain floating if this function is not going to be used.

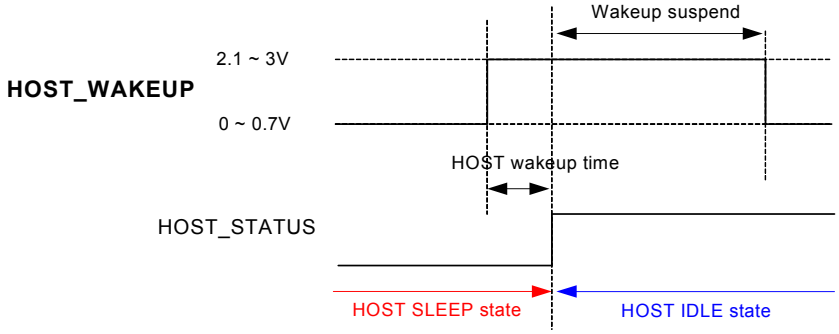


Figure 11 HOST_WAKEUP timing diagram

4.5 System Reset

SAT module provides two methods for the system reset. One is software reset by using AT command, and another is hardware reset by /SAT_RESET pin.

When user should reset module, it can be executed by using AT command at host generally. But if there is no reaction at UART port because of misoperation of module, reset is achieved by implementing the following hardware sequence.

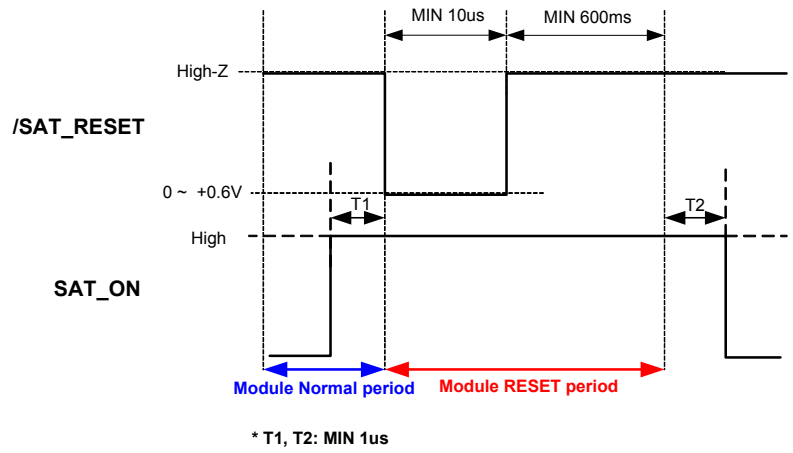


Figure 12 System reset timing diagram by using /SAT_RESET pin

Figure 12 tells the time which executing system reset by using /SAT_RESET PIN.

MODULE became RESET if /SAT_RESET SIGNAL is maintained as LOW LEVEL during 10us. But SAT_ON PN should be maintained as High during module reset period because when /SAT_RESET SIGNAL falls by LOW LEVEL, SAT MODULE become shut down. T1 and T2 should be maintained the timing by more than 1us, which is the GUARD time of start and end of each RESET PERIOD.

4.5.1 Feature of /SAT_RESET pin

/SAT_RESET PIN is connected by input pin of manual reset of internal reset block. This procedure prolongs maintaining time of /RESET by low level during booting status because of the internal RC combination which extends the pulse (20 kΩ and10 µF)

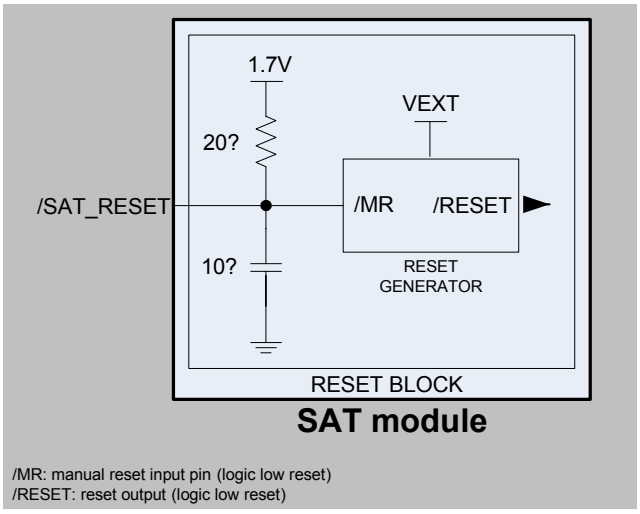


Figure 13 Internal Reset Circuitry

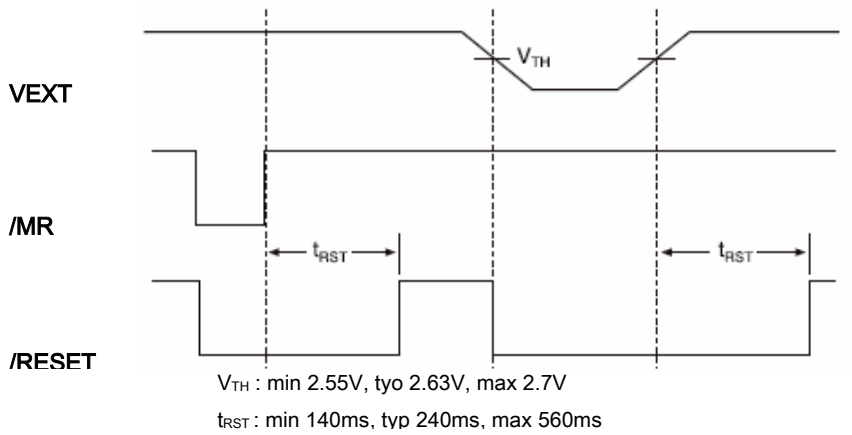


Figure 14 Timing diagram of Internal RESET Circuitry

When boot up of SAT module, reset signal is generated by internal circuit to fit the processor reset timing as Figure 15,

This signal should remain floating if this function is not going to be used.

The following function can be executed by using /SAT_RESET pin.

1. Emergency off : this function can be used as emergency off when SAT module operates abnormally. To turn SAT module off, /SAT_RESET hold as low level over 10 μs without SAT_ON signal hold as high level. But the datas of internal memory can be deleted without any saving process because this function makes the entire power off. Accordingly, this function should be executed when serious problem has occurred such as module does not power off by SAT_OFF signal or no answer is found at UART port because internal software operates abnormally only.

2. Hardware reset: This function has explained at Section 4.5.2

4.5.2 Waveform of /SAT_RESET pin

The following figures are actual measured waveforms when executing functions explained in the previous sections

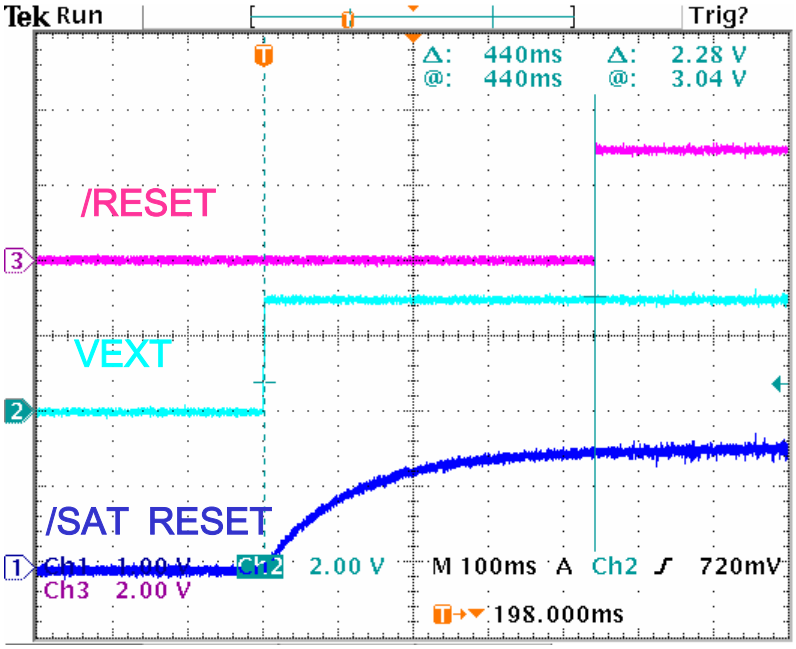


Figure 15 /SAT_RESET pin waveform at boot up time

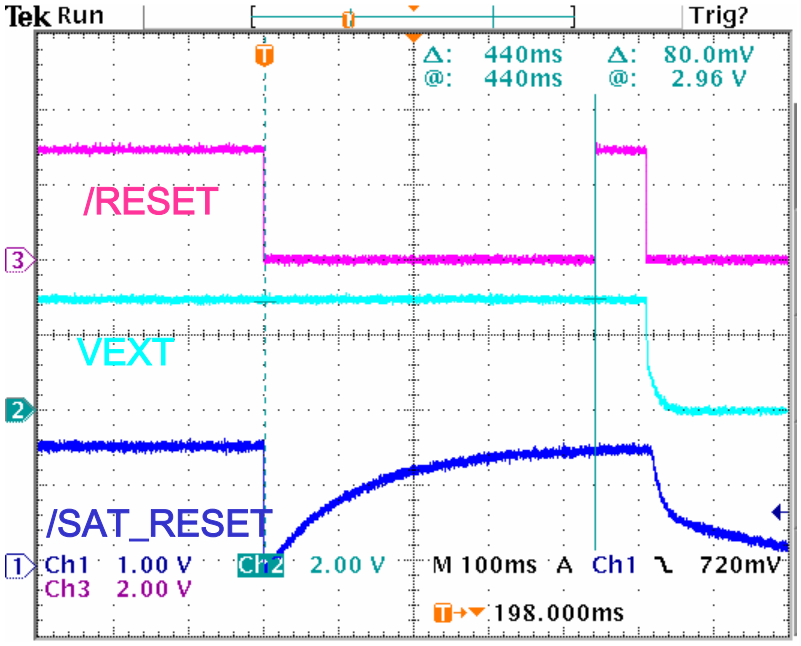


Figure 16 /SAT_RESET pin waveform at emergency off time

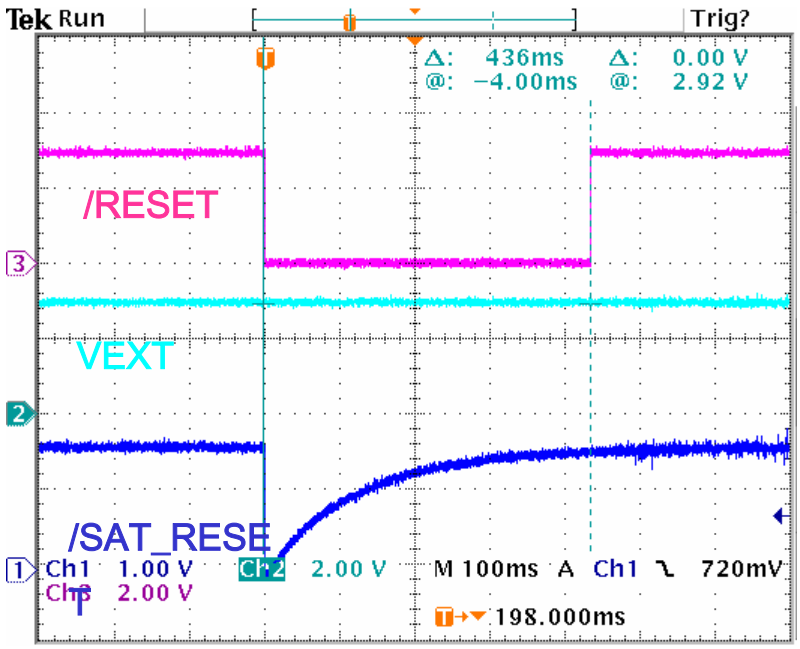
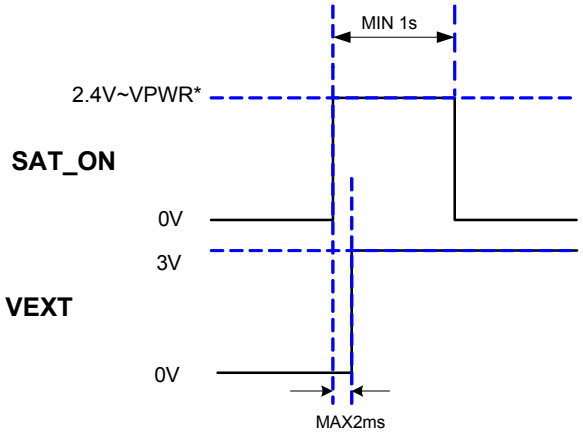


Figure 17 /SAT_RESET pin waveform at hardware reset time

4.6 Turn on

To turn on SAT module, hold SAT_ON signal high during for minimum 1 second and put it low after inserting the power at VPWR, 5V_TX.



Note) VPWR*: Input voltage of VPWR pins

Figure 18 Turn on timing diagram

4.7 Turn off

Ways to turn SAT module off.

1. Way to use SAT_OFF signal: Module turns off when SAT module works while SAT_OFF signal holds high. If SAT_ON remains at high, module is not off.

2. Automatically turn off when over-voltage or under-voltage at VPWR is present.

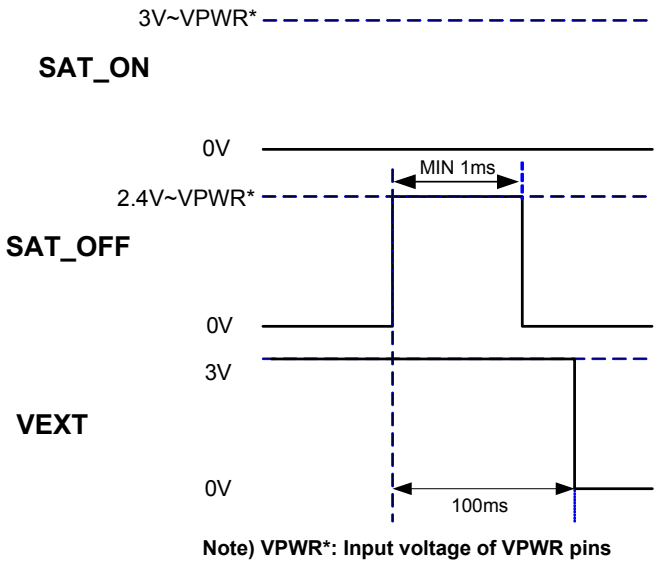


Figure 19 Turn off timing diagram

5 RTC backup battery interface

RTC (Real Time Clock) power of SAT module is supplied by VRTC signal of board-to-board connector. VRTC is used power souce of internal RTC block and GPS chipset.

External backup battery should be connected at VRTC signal because there's no supply of internal power in VRTC signal. When RTC backup battery is not used, it should be connected with VPWR or VEXT. Failure to do so will prevent the Module from working.

Electrical character of VRTC signal is as below.
Vmax = +5.5V
Vmin = +2.0V
Vnorm = +3V
Idd = 15 µA (max)
The following are various examples of external backup battery interface.

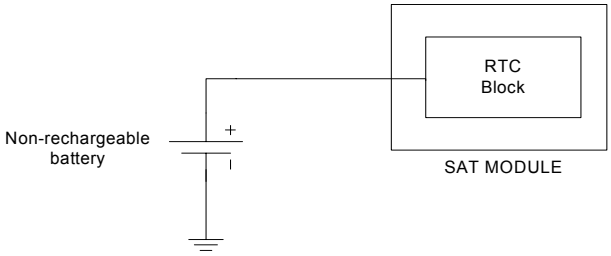


Figure 20 Supply from non-rechargeable battery

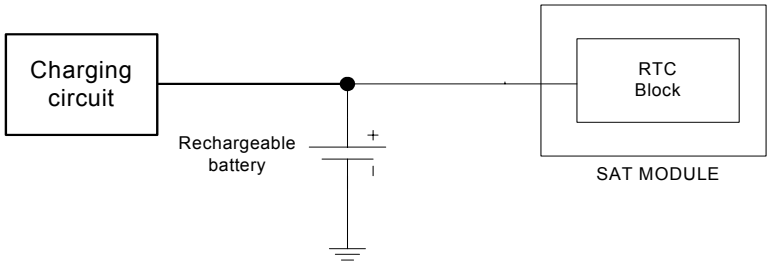


Figure 21 Supply from rechargeable battery

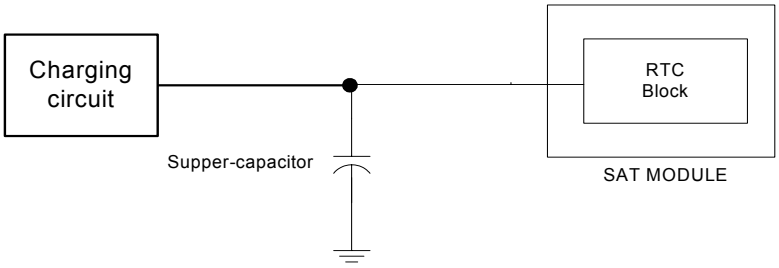


Figure 22 Supply from super-capacitor

If you use super-capacitor or rechargeable battery, external battery charging circuit should be included because there is not battery charging circuit at inside of module. R and LDO should be used suitable value to specifications of rechargeable or super-capacitor in Figure 22.

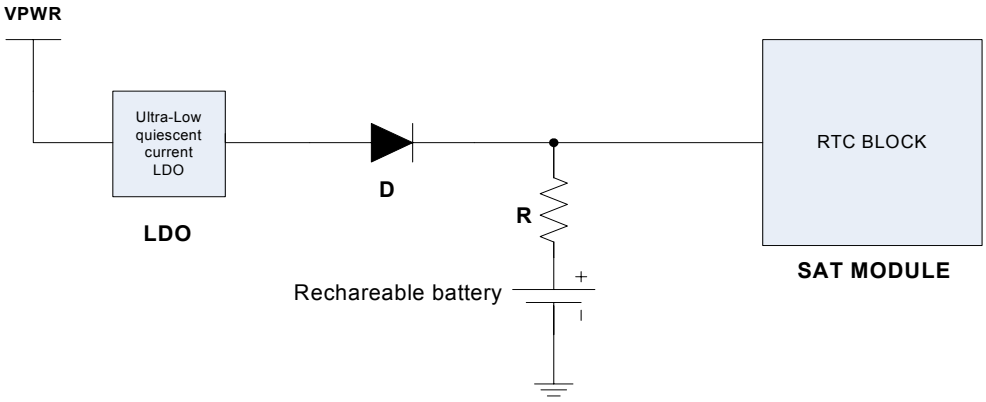


Figure 23 External rechargeable battery charging circuit example

6 UART interface

SAT module offers two UART ports. One provides 8-full-signals communications and the other one provides only 4 signals.

Driving current of each signal and voltage level of UART port are as follows.

Table 4 Max driving current of each UART pins

UART1	TXD	2	mA
	RXD	20	µA
	CTS	20	µA
	RTS	2	mA
	DSR	20	µA
	DTR	4	mA
	DCD	8	mA
	RI	8	mA
UART2	TXD	8	mA
	RXD	20	µA
	CTS	20	µA
	RTS	8	mA

Table 5 Logic level of UART port

	min	max	
Logic high input	2.1	3.3	V
Logic low input	0	0.9	V
Logic high output	2.4	3	V
Logic low output	0	0.6	V

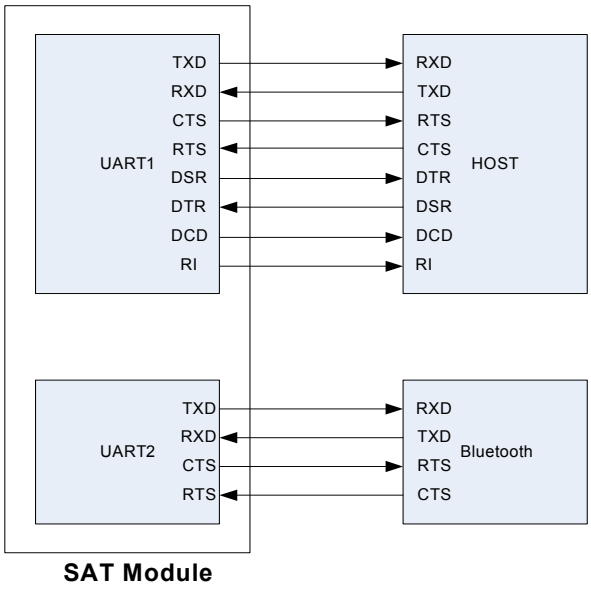


Figure 24 UART connection block diagram

6.1 UART1

8-signal full port interface:
This is used as a port to control SAT module by using AT command and to transmit DATA/FAX.
Transferred baud rate that supported is as follows.

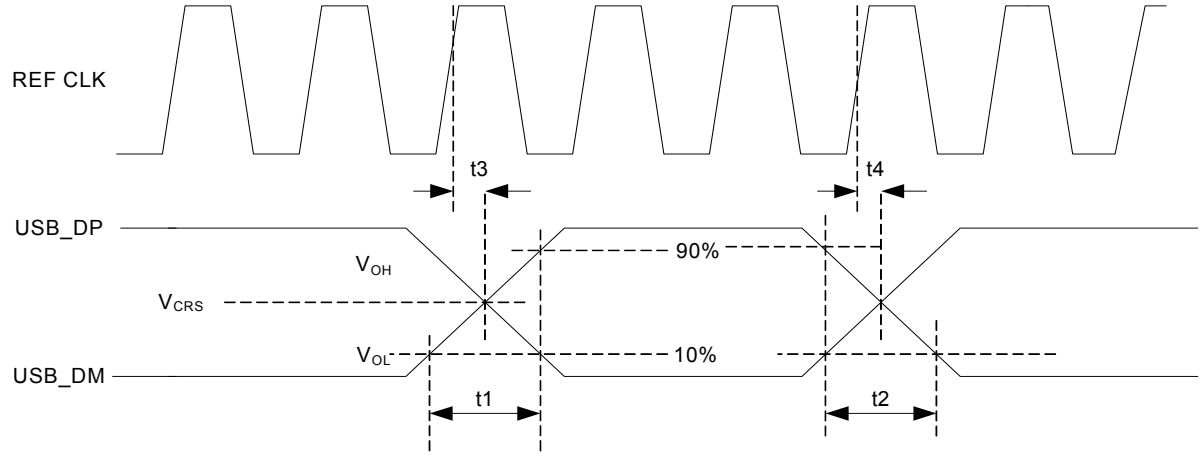
4800 bps, 9600 bps, 38400 bps, 57600 bps, 115200 bps
Default: 115200bps

6.2 UART2

4-signal port interface:
This is used for communicating to interface with Bluetooth and to debug SAT module.
Transferred baud rate is fixed at 11.52 kbps

7 USB interface

SAT module supports Revision 1.1 of Universal Serial Bus Specification.



C_L= 70pF
t_{RFM} = (t1/t2) X 100
t_{jr} = t4-t3

Parameter	MIN	MAX	UNIT
t1 (Rise time)	4	20	ns
t2 (Fall time)	4	20	ns
t_{RFM} (Rise/Fall time matching)	90	111.11	%
V_{CRS} (Output signal cross-over voltage)	1.3	2.0	V
t_{jr} (Differential propagation jitter)	-2	2	ns

Figure 25 USB interface timing

8 AUDIO interface

8.1 CODEC selection

SAT module offers analog audio interface and digital audio interface.

Using or not of digital audio interface is decided by voltage level of CODEC_SEL signal.
If CODEC_SEL signal is 'high' level, then internal PCM CODEC is disabled and you can use external PCM CODEC. If CODEC_SEL signal is 'low' level, then internal PCM CODEC is used.
If the CODEC_SEL signal is left floating, Satellite module is using internal PCM CODEC.

When SAT module use internal PCM CODEC, the signals, DAI_DIN, DAI_DOUT, DAI_CLK, and DAI_SYNC signals must be floating.

8.2 Digital Audio Interface

SAT module supply DAI for various audio applications.

The digital audio interface consist of data input (DAI_DIN), data output (DAI_DOUT), clock output (DAI_CLK), and frame sync. (DAI_SYNC).

DAI_CLK : generated as 2.048MHz clock from SAT module.
DAI_SYNC : generated as 8kHz clock from SAT module.
DAI_DIN : received to 16-bits data from MSB bit to LSB bit at rising edge of clock.
DAI_DOUT: transmitted 16-bits data from MSB bit to LSB bit at rising edge of clock.

We recommend PCM CODEC IC (TLV320AIC1110) of TI co. (http://www.ti.com/)

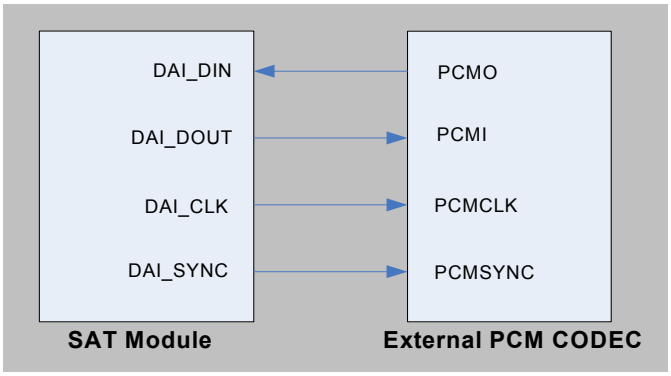
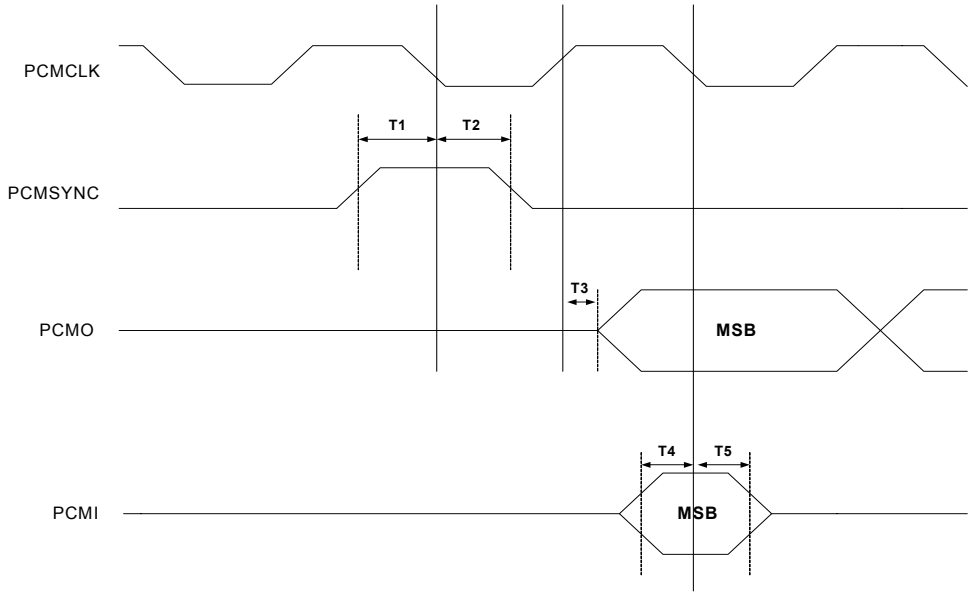


Figure 26 External PCM CODEC interface block diagram



T1	PCMSYNC setup time	Min 20 ns
T2	PCMSYNC hold time	Min 20 ns
T3	Transmit data delay time	Max 35 ns
T4	Receive data setup time	Min 20 ns
T5	Receive data hold time	Min 20 ns

Figure 27 PCM timing diagram

8.3 Analog Audio Interface

The analog audio interface consists of differential microphone inputs (SAT_MIC+, SAT_MIC-) and differential earphone outputs (SAT_SPK+, SAT_SPK-).
External audio circuitry should be included ESD, RF by pass capacitors and MIC Bias, if it is connected to microphone or speaker directly.

Mic Bias voltage is shown in the diagram but not stated here.

It is recommended to use a microphone with a sensitivity of at least -44±dB/Pa at 2V and 2kΩ(0dB=1V/Pa, 1kHz). It should be equipped with an internal EMI capacitor for 1600 MHz bands. This should say that small value surface mount capacitors should be used to decouple the transmit RF. Even a high-quality microphone should be placed at least 10 cm away from the antenna. Other audio problems may be due to insufficient filtering of power supply and different GND levels between PCBs. Some detail about grounding requirements and schemes is required along with detail of power supply filtering requirements.

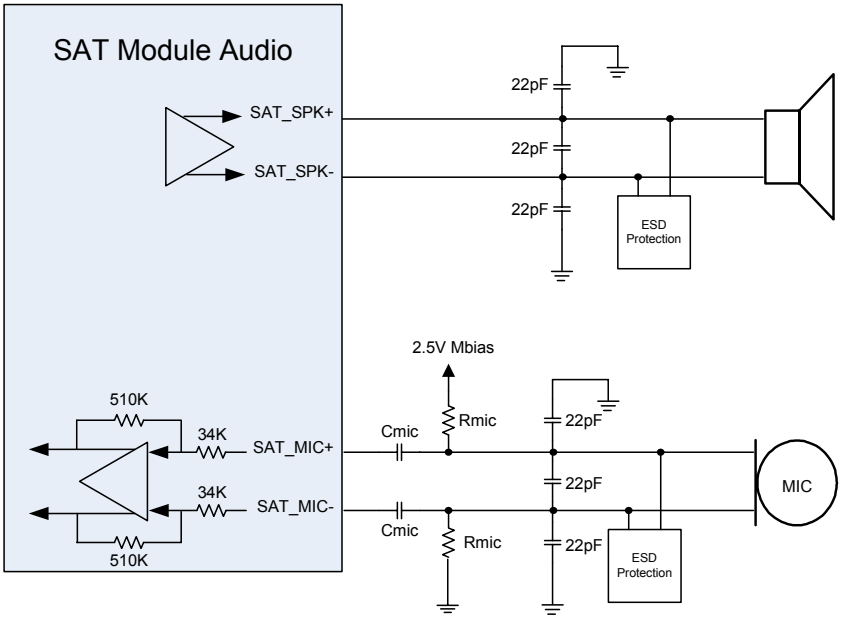


Figure 28 Analog audio interface

8.4 Principles of MIC & SPK

SAT module has no internal mic bias, therefore you should compose a balanced microphone feed. to the module's audio input (SAT_MIC+/-) as shown in Figure 28 The microphone signal is very sensitive to any disturbances from the power supply, poor ground or induced RF. A balanced microphone feed gives high common mode rejection and helps reduce RF induced standing voltages.

Table 6 MIC interface specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage at MIC		-5		5	mV
Input bias current at MIC		-300		300	nA
Input capacitance at MIC		5			pF
MIC input referred noise	MIC amp 1 gain = 23.5 dB MIC amp 2 gain = 0 dB		3	4.7	µVrms
Output source current of MBIAS		1 1.2			mA
MIC bias supply voltage		2.3	2.5	2.65	V
MICMUTE		-80			dB

Input impedance	Fully differential	35	60	100	kΩ

Table 7 SPEAKER interface specification

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SPK AMP output power	VDD=3V, fully differential, 8Ω load, 3dB0 output, volume control=-3dB, RXPGA=-4dB level	161	200		mW
	VDD=3V, fully differential, 16Ω load, 3dB0 output, volume control=-3dB, RXPGA=-2dB level	128	160		mW
	VDD=3V, fully differential, 32Ω load, 3dB0 output, volume control=-3dB, RXPGA=-1dB level	81	100		
Output offset voltage at SPK		10	12.5		mV
Maximum output current for SPK		141	178		mA
		90	112		
		50	63		
SPK MUTE		-80			dB

9 SIM card interface

SAT module requires a SIM card to operate in SAT mode (except for emergency call).

Support to the standard plug-in SIM card as defined in ETSI standard GSM 11.11, as modified by GSM 11.12. Both 1.8V/3.0V and 3.0V only SIM cards are supported.

Table 8 SIM card interface pins function description

SIM_VDD	SIM card power supply. 1.8V(MAX:±10%)/3V(MAX:±10%) SIM card auto detect, provided by SAT module.
SIM_CLK	SIM card clock, provided by SAT module.
SIM_RST	SIM card reset, provided by SAT module.
SIM_DATA	SIM card data line, input and output.

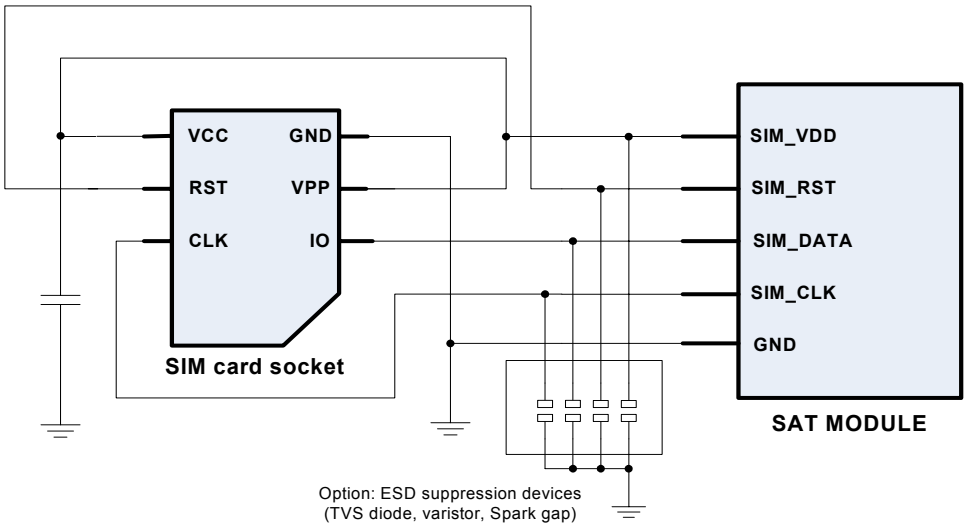


Figure 29 SIM interface reference circuit

It is recommended that use external ESD protection device (varistor or TVS diode) for protection of SIM card, and the total cable length between the board-to-board connector signals on module and the signals of the SIM card holder route as short as possible to satisfy the requirements of EMC compliance.

To avoid possible cross-talk from the SIM_CLK signal to the SIM_DATA signal be careful that both lines are not placed closely next to each other. A useful approach is using the GND line to shield the SIM_DATA line from the SIM_CLK line.

If you will use ESD suppression device, it should be placed in close to SIM card. It is recommended that NZQA6V8AXV5T1 (ON semiconductor: http://www.onsemi.com) as ESD suppresstion device

10 LCD interface

SAT module provides 14-signals interface with a LCD.

Specific characteristics are as below.

1. Supports 128*128 dot, 65k color LCD.

2. Using 8080-series 8bits parallel bus interface.

2. Supply LCD_ EN for control main power of LCD.

4. Support LCD driver IC: S6B33B6 (SEC: http://www.samsung.com/)

Table 9 LCD interface pins function description

PIN NAME	FUNCTION DESCRIPTION
LCD_D0	LCD data bit 0
LCD_D1	LCD data bit 1
LCD_D2	LCD data bit 2
LCD_D3	LCD data bit 3
LCD_D4	LCD data bit 4
LCD_D5	LCD data bit 5
LCD_D6	LCD data bit 6
LCD_D7	LCD data bit 7
LCD_CS	LCD chip select (Active LOW)
LCD_RS	Data/Instruction select (H:data, L:instruction)
LCD_WR	LCD data write enable (Active LOW)
LCD_RD	LCD data read enable (Active LOW)
LCD_EN	LCD power enable (Active HIGH)
LCD_ RESET	LCD reset (Active LOW reset)

11 Backlight interface

3-signals are used to control backlight of keypad and LCD in SAT module.

Table 10 Backlight interface pins function description

LCD_BL_EN	LCD backlight enable (Active HIGH)
LCD_BL_DIM	LCD backlight dimming control (PWL signal output)
KEYPAD_BL_EN	KEYPAD backlight enable (Active HIGH)

11.1 Keypad backlight interface

KEYPAD_BL_EN signal is used for ON/OFF of external keypad's backlight.
When the key is pressed, backlight is placed at ON and then OFF several moments later.

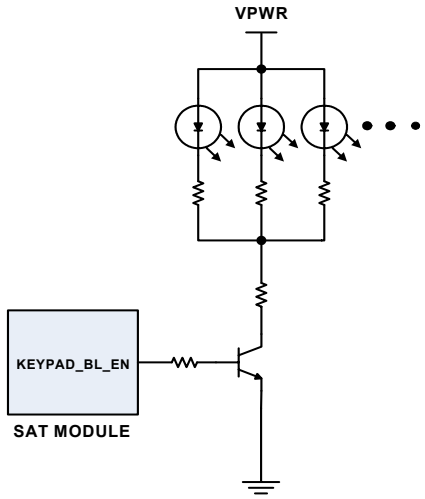


Figure 30 Keypad backlight interface reference circuit

11.2 LCD backlight interface

LCD backlight interface is used for backlight ON/OFF and bright control when external LCD is used.

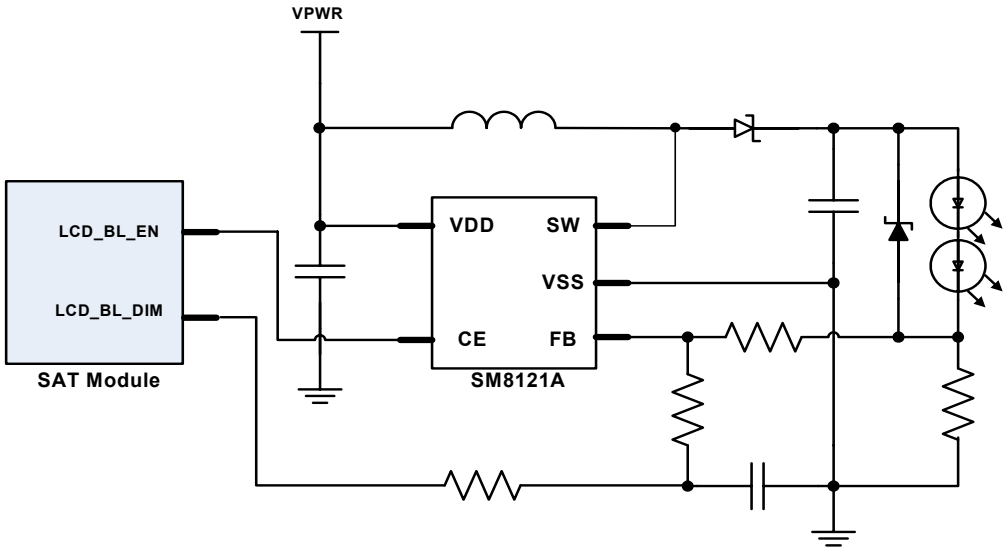


Figure 31 LCD backlight interface reference circuit

This reference circuit includes 2 White LED as a series for LCD backlight, the constant current type of white LED driver IC of NPC Co. is used to maintain regular brightness. For detail specifications of White LED driver IC, refer to web site: http://www.npc.co.jp/

12 Keypad interface

SAT module provides keypad interface of 5*5 matrix scan method.
All of functions of module can be controlled by keypad.
Method of keypad interface and functions of each key are as below.

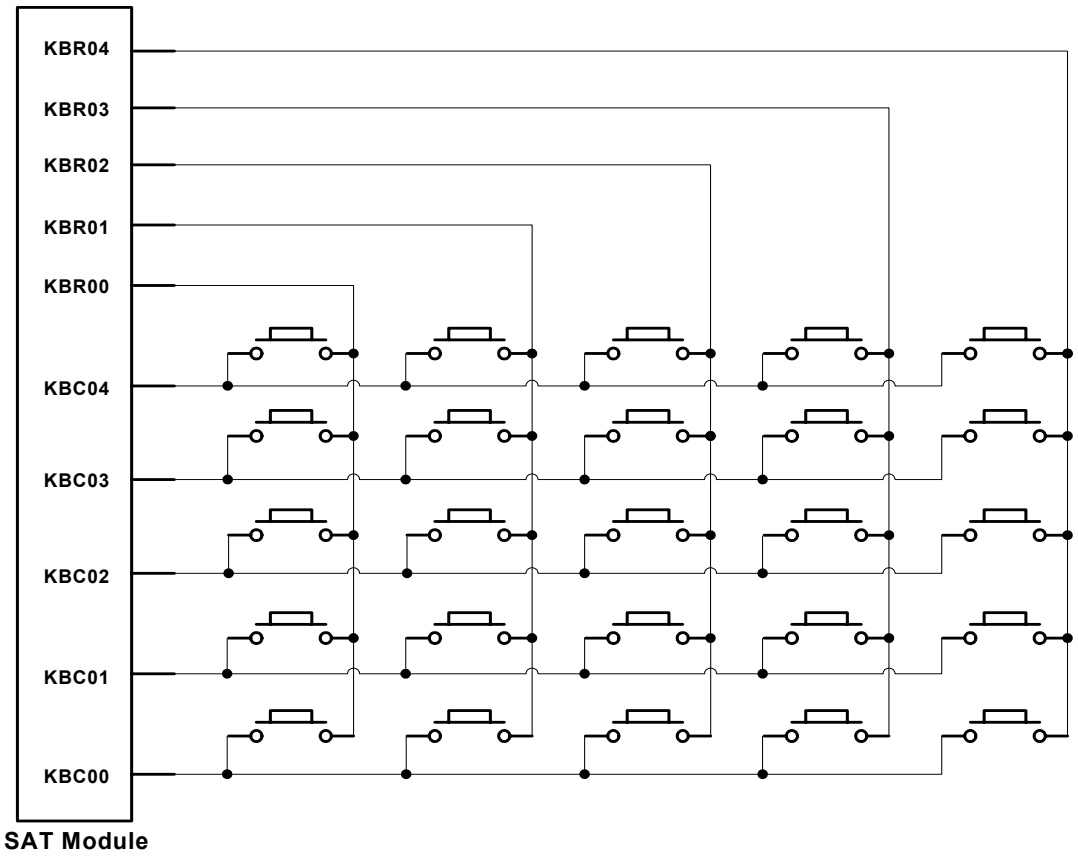


Figure 32 Keypad interface reference circuit

Table 11 KEYPAD functional mapping table

	KBR00	KBR01	KBR02	KBR03	KBR04
KBC00	RESERVE	*	0	#	RIGHT
KBC01	RESERVE	7	8	9	LEFT
KBC02	RESERVE	4	5	6	CENTER
KBC03	RESERVE	1	2	3	DOWN
KBC04	MENU	SELECT	SEND	END	UP

13 Buzzer interface

BUZZER of No. 84 pin of board-to-board connector is used as inform about calling-receipt by operating external buzzer, a sample circuit is shown in Figure 33

V_{OH}min = +2.75V
V_{OL}max = +0.25V
IL = +3.2 mA

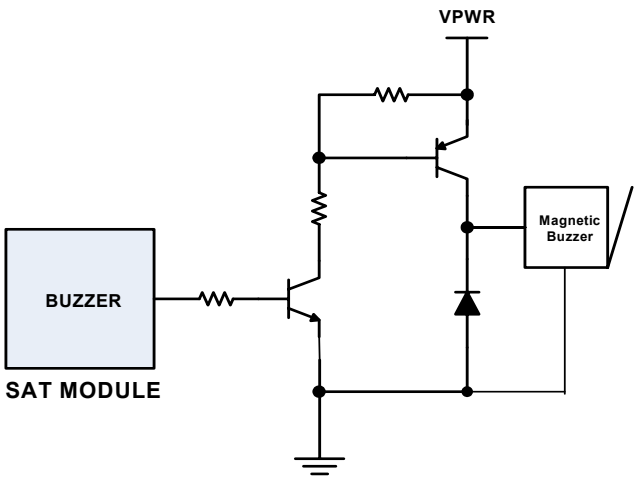


Figure 33 Buzzer interface refence circuit

14 I2C device interface

The I2C bus is compliant to Philips I2C-bus specification version 2.1 and support standard mode (up to 100kbps) and fast mode (up to 400kbps).

12C port of SAT module is used for controlling power class that suits for application purpose that module is used. Please see the manufacturers web site for further details (http://www.semiconductors.philips.com)
For Classes 1~8: PCF8574 and for Classes 9~16: PCF8574A

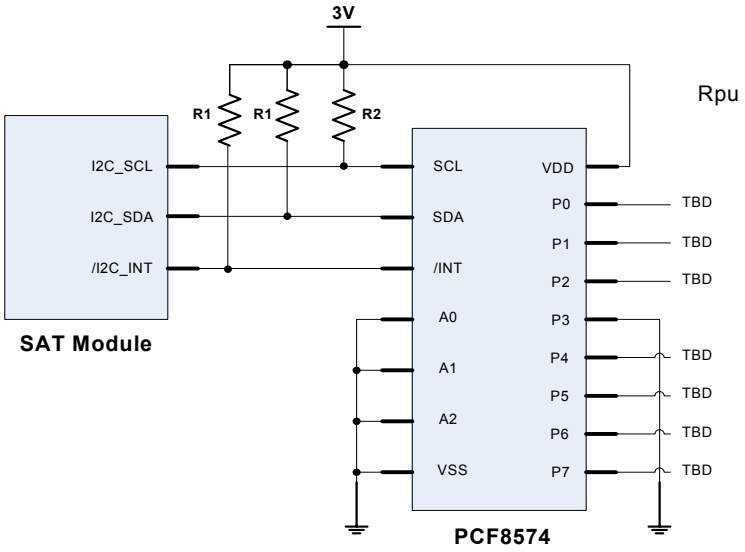


Figure 34 I2C device interface reference circuit (EX. power class 1)

** NOTE*

It is recommended to use that R1 is 470Ω and R2 is 100 kΩ when PCF8574 or PCF8574A is connected with I2C interface lines.

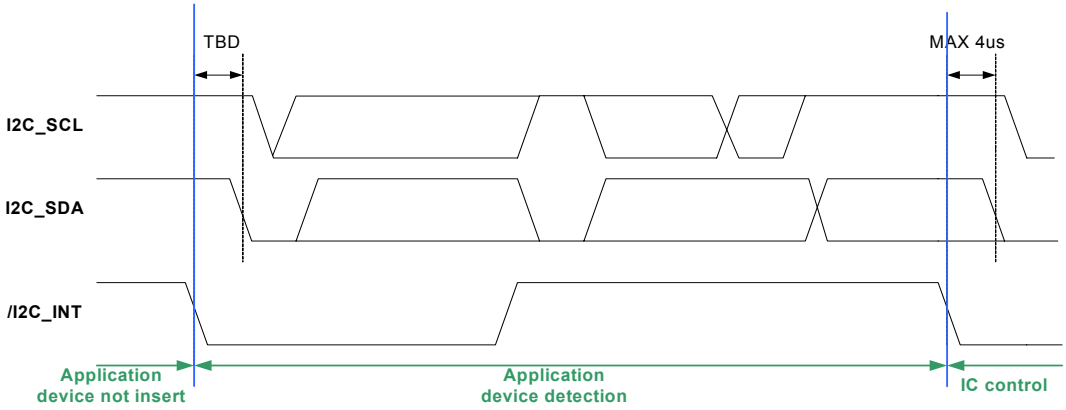


Figure 35 I2C device interface timing diagram (power class 1)

There are 3 types of modes of timing.

1. Application device not detect: This is the situation of not connecting the IC with 12C port and all of the 12C_SCL, 12C_SDA and /12C_INT is at the high level condition. If connection is done but the power at IC (PCF8574) is not permitted, be sure to permit the power on IC at connection condition because SAT module is not booting.

2. Application device detection: When /12C_INT is placed at initially at low logic level, the SAT module recognizes external device, it then understands kind of external device by scanning 16 addresses and provides setting of power class.
To maintain low level of /INT when IC (PCF8574, PCF8574A) is booted, IO has to stay at low level. For more information, refer to the IC datasheet.

3. /12C_INT uses as different interrupting signal at input change that appointed as IO port among the IO port of IC (PCF8574, PCF8574A)

12C device addresses that assigned to each power class are as follow.

Table 12 Device address table assigned by power class

Power Class	Minimum EIRP(dbw)	Maximum EIRP(dbw)	G/T	Application	I2C device addresses
1	5	7	-24	UT, Handheld, Data terminal C, Data Cable	0100 000X
2	5	7	-24	Vehicular, No adjustable antenna	0100 001X
3	7	11	-22	Vehicular, Adjustable Antenna	0100 011X
4	7	11	-22	Vehicular, Adjustable Antenna	0100 101X
5	7	11	-22	Maritime Antenna	0100 110X
6	5	9	-18	Fixed	0100 010X
7	5	9	-18	PCO	0100 111X
8	9.1	14.9	-16.2	Data terminal A & B	Not used
9	5	7	-24	External Encrypter	0111 000X
10	Reserved	Reserved	Reserved	Reserved	0111 001X
11	Reserved	Reserved	Reserved	Reserved	0111 010X
12	Reserved	Reserved	Reserved	Reserved	0111 011X
13	Reserved	Reserved	Reserved	Reserved	0111 100X
14	Reserved	Reserved	Reserved	Reserved	0111 101X
15	Reserved	Reserved	Reserved	Reserved	0111 110X
16	Reserved	Reserved	Reserved	Reserved	0111 111X

15 B-to-B Connector Pin Assignment

The Board to board connector is a Panasonic (NAIS) Part No AXK6S00645P. For details of appropriate matching parts please refer to Table 15.
Each pin assigned as shown in Table 13 B-to-B connector pin assignment.

Table 13 B-to-B connector pin assignment

Num	Pin Name	Description	Num	Pin Name	Description
1	LCD_ D0	LCD DATA 0	2	KBR00	KEYPAD Row 0
3	LCD_ D1	LCD DATA 1	4	KBR01	KEYPAD Row 1
5	LCD_ D2	LCD DATA 2	6	KBR02	KEYPAD Row 2
7	LCD_ D3	LCD DATA 3	8	KBR03	KEYPAD Row 3
9	LCD_D4	LCD DATA 4	10	KBR04	KEYPAD Row 4
11	LCD_D5	LCD DATA 5	12	KBC00	KEYPAD Col 0
13	LCD_D6	LCD DATA 6	14	KBC01	KEYPAD Col 1
15	LCD_D7	LCD DATA 7	16	KBC02	KEYPAD Col 2
17	/LCD_CS	LCD Chip Select	18	KBC03	KEYPAD Col 3
19	/LCD_RD	LCD Read	20	KBC04	KEYPAD Col 4
21	/LCD_WR	LCD Write	22	UART1_TXD	UART_TX
23	LCD_RS	LCD Data/Instruction Select	24	UART1_RXD	UART RX
25	LCD_EN	LCD Enable	26	UART1_CTS	UART CTS
27	/LCD_RESET	LCD RESET	28	UART1_RTS	UART RTS
29	LCD_BL_EN	LCD Backlight Enable	30	UART1_DTR	UART DTR
31	LCD_DIM	LCD Backlight Dimming Control	32	UART1_DSR	UART DSR
33	KEYPAD_BL_EN	KEYPAD Backlight Enable	34	UART1_DCD	UART DCD
35	GND	Ground	36	UART1_RI	UART RI
37	I2C_SCL	Serial Clock	38	UART2_TXD	UART TX
39	I2C_SDA	Serial Data	40	UART2_RXD	UART RX
41	/I2C_INT	Accessory Detection and Interrupt	42	UART2_CTS	UART CTS
43	DAI_DIN	Ground	44	UART2_RTS	UART RTS
45	DAI_DOUT	Do not connect any signal	46	GPIO1	GPIO
47	DAI_CLK	Do not connect any signal	48	GPIO2	GPIO

49	DAI_SYNC	Ground	50	GND	Ground
51	/SAT_RESET	SAT Module Reset	52	USB_DP	USB D+
53	HOST_WAKEUP	Host Wakeup	54	USB_DM	USB D-
55	HOST_STATUS	Host Status	56	USB_VBUS	USB Power
57	SAT_ON	SAT Module ON	58	SIM_DATA	SIM DATA
59	SAT_OFF	SAT Module OFF	60	SIM_CLK	SIM CLOCK
61	SAT_STATUS	SAT Module Status	62	SIM_RST	SIM RESET
63	SAT_WAKEUP	SAT Module Wakeup	64	SIM_VDD	SIM POWER
65	VRTC	RTC Backup Battery	66	VEXT	3V Ourput Power
67	GND	Ground	68	GND	Ground
69	GND	Ground	70	GND	Ground
71	CODEC_SEL	Main 5V Power	72	SAT_SPK-	Speaker Out -
73	VPWR	Main 5V Power	74	SAT_SPK+	Speaker Out +
75	VPWR	Main 5V Power	76	GND	Ground
77	VPWR	Main 5V Power	78	SAT_MIC-	Mic In -
79	VPWR	Main 5V Power	80	SAT_MIC+	Mic In+
81	VPWR	Main 5V Power	82	GND	Ground
83	GND	Ground	84	BUZZER	BUZZER Control
85	GND	Ground	86	GND	Ground
87	GND	Ground	88	GND	Ground
89	GND	Ground	90	GND	Ground
91	GND	Ground	92	GND	Ground
93	5V_TX	RF TX 5V Power	94	5V_TX	RF TX 5V Power
95	5V_TX	RF TX 5V Power	96	5V_TX	RF TX 5V Power
97	5V_TX	RF TX 5V Power	98	5V_TX	RF TX 5V Power
99	5V_TX	RF TX 5V Power	100	5V_TX	RF TX 5V Power

16 Antenna Interface

There are two antenna interfaces on the SM-2500, SAT module.

The one is for Thuraya satellite network(SAT) , another is for Global Positioning system(GPS). The two connectors, Radiall R-MCX(R299-142-821), are the same electrical and mechanical characteristics. Counter part plugs can be also found out www.radiall.com, Thuraya recommends the following Radiall Part R300-113-100W.

There is no DC output from antenna connector port. In the case of using external active antenna, an appropriate bias network should be composed at the outside of the SM-2500.

Figure 1 shows the connector port of satellite antenna and GPS antenna port.

For SAT and GPS antenna specifications requirements, Please refere to the GMR-1 05.05 ETSI specifications.

All of the external RF requirements are driven by the GMR-1.

Table 14 RF parameters.

RX frequency band	1525.0 to 1559.0MHz
TX frequency band	1626.5 to 1660.5MHz
G/T limit	-24dB/K
Min. nonbacked off RF PA output	2W
Power control step size	0.4 dB
RSSI range	-125 to -105 dBm
Receiver Noise Figure	< 1.8dB

17 Mechanical interface

The Figure 37 shows the mechanical interfaces of SM-2500 Recommended board to board female connector are also shown in Table 15. It's the recommended base in Figure 38.

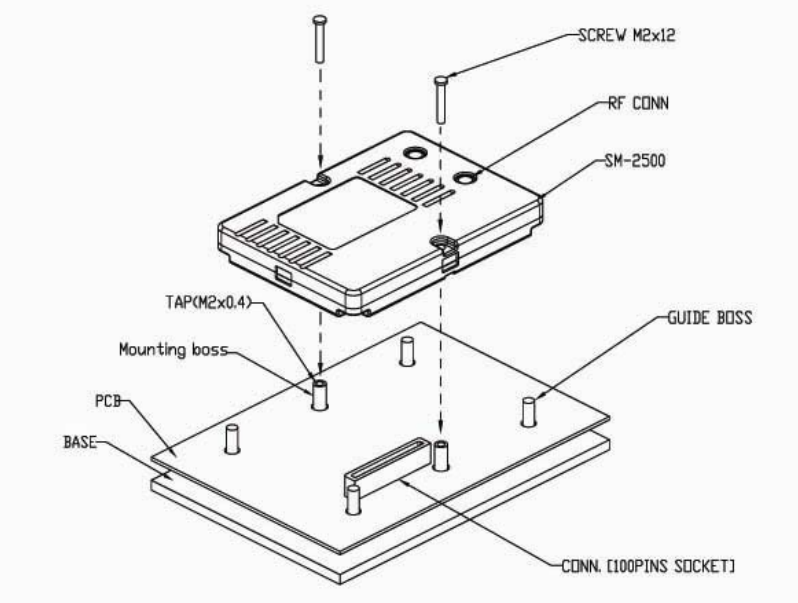


Figure 36 Mechanical interface

Mated Height (mm)	Part No Socket	A Socket Height (mm)	B PCB to SM-2500 (mm)	C Guide Boss Height (mm)	D Mounting Boss Height (mm)
6.0	AXK5S00037	3.05	2.9	3.8	3.8
6.5	AXK5S00237	3.55	3.4	4.3	4.3
9.0	AXK5S00337	6.05	5.9	6.8	6.8

Table 15 Recommended Board to Board Female connector

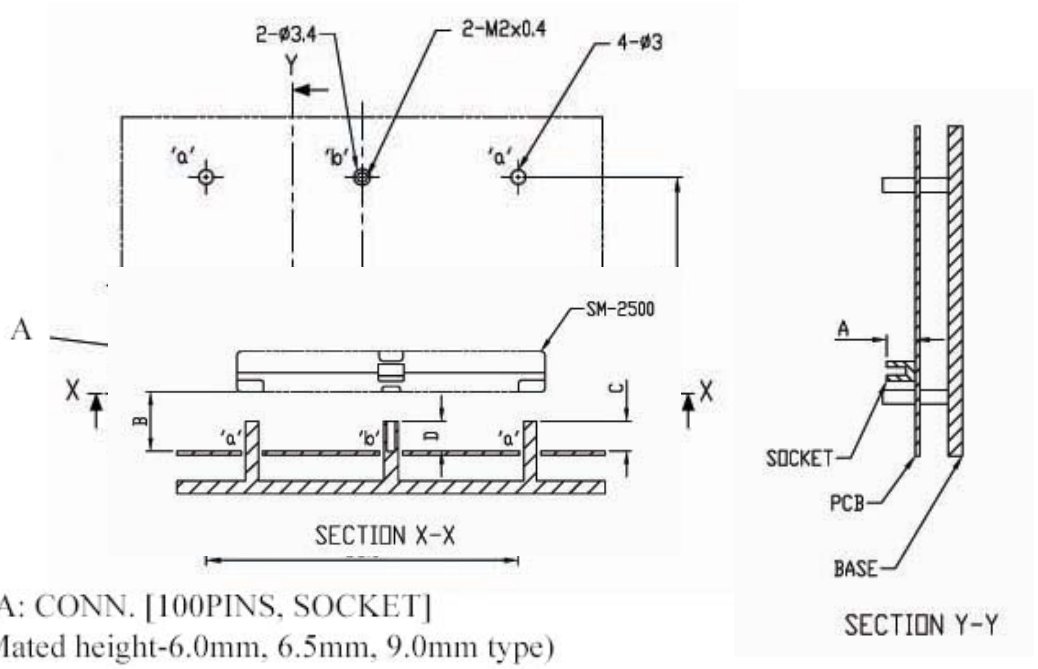


Figure 37 Recommended Base

18 Thermal DISSIPATION

18.1 Installation method of Heat Sink

The proper method of heat dissipation to avoid overheating is necessary when SM-2500 is used in the closed space. A installation of HEAT SINK is recommended between PCB and SM-2500 as shown in the following figure.

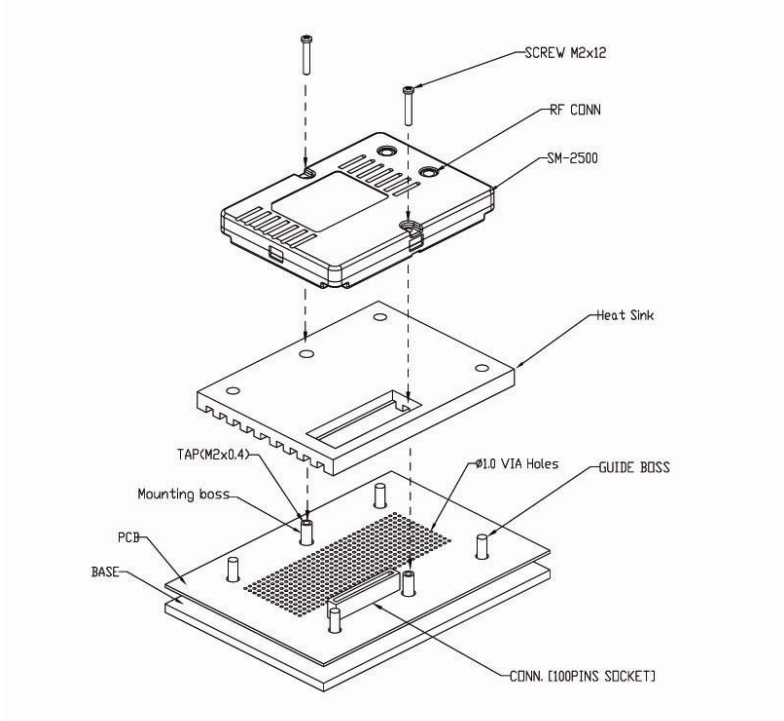


Figure 38 Installation method of Heat Sink

18.2 Guide of HEAT SINK and PCB design

The thickness of HEAT SINK should be changed depending on MATED HEIGHT as shown in the Figure 40 Example of HEAT SINK Design.

The housing or case including SM-2500 and Heat Sink should be the material having good thermal conductivity such as Aluminum and keep a good thermal contact between SM-2500 and Heat Sink, and between the Heat Sink and outside housing.

The parts should not be located on the urface of the PCB including B2B connector contacting with Heat sink for SM-2500 and VIA hole during PCB design should be created on PCB as many as possible good heat dissipation regarding the PCB area shown in the following figure.

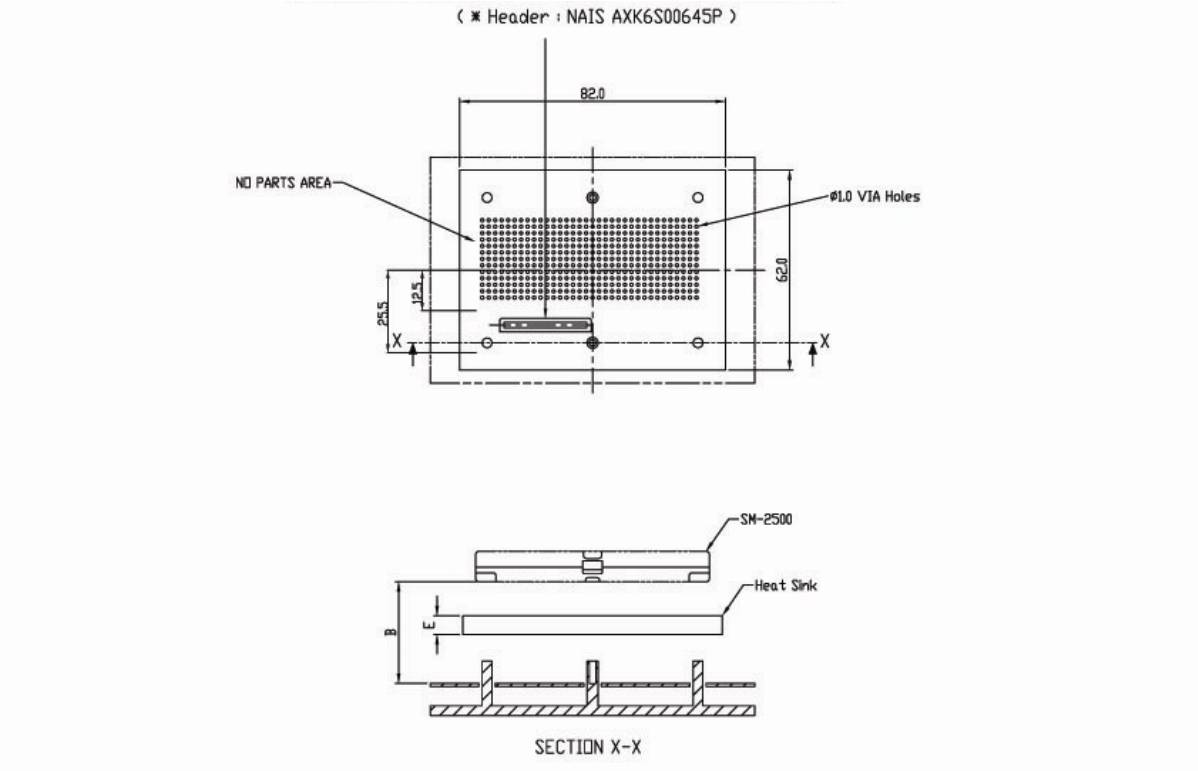


Figure 39 Guide of HEAT SINK and PCB design

18.3 Example of HEAT SINK Design

The material like Aluminum which has good thermal conductivity should be used. The following figure is the example and size of heat sink for SM-2500.

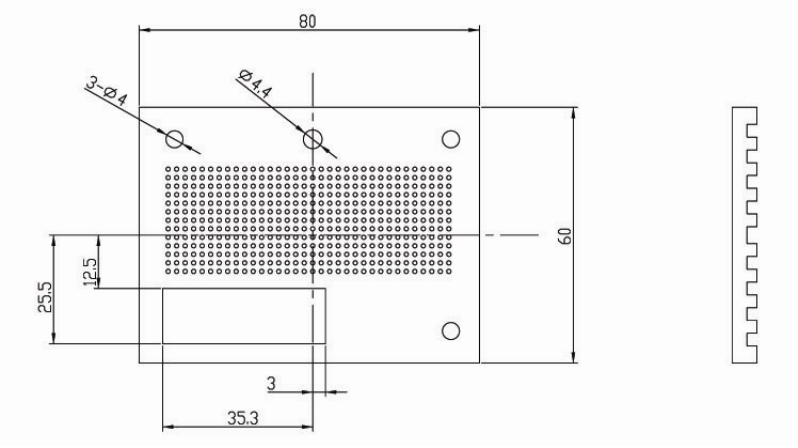


Figure 40 Example of HEAT SINK Design

