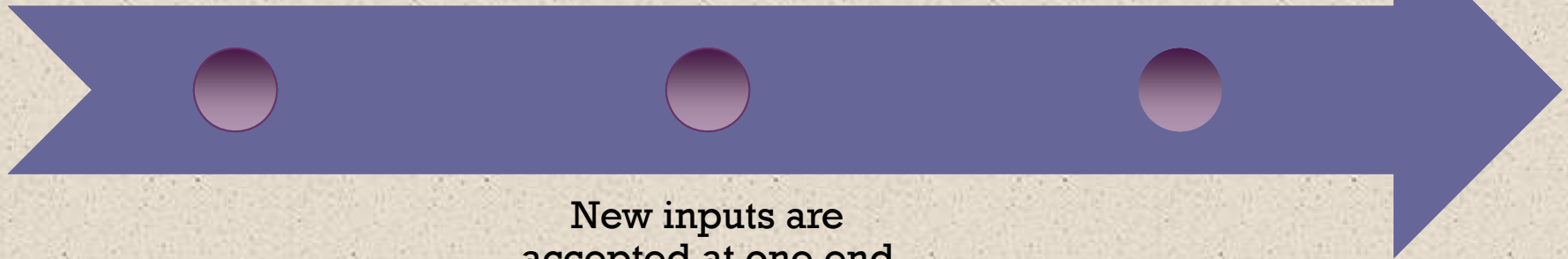


Pipelining Strategy

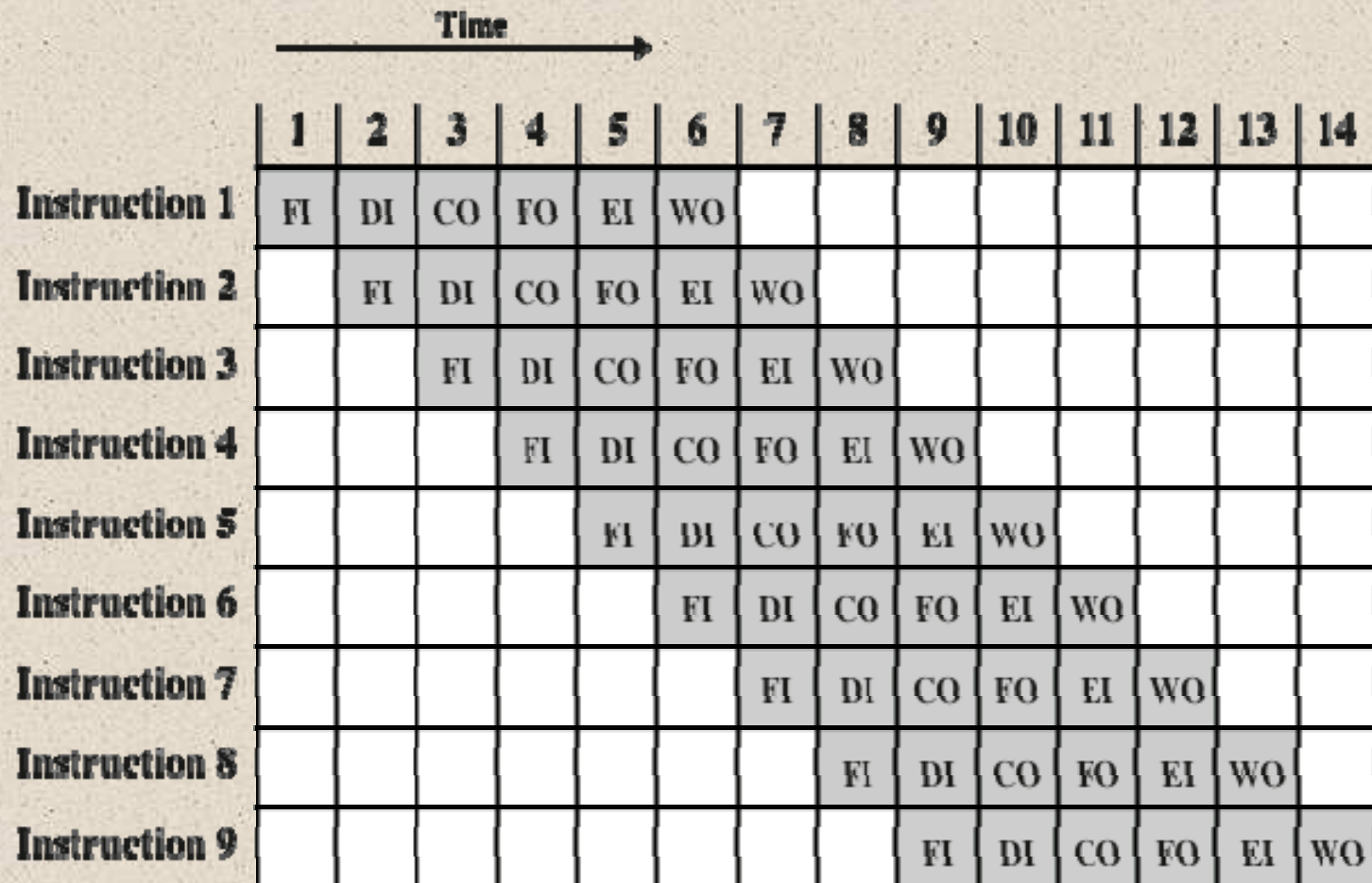
Similar to the use of
an assembly line in a
manufacturing plant

To apply this concept
to instruction
execution we must
recognize that an
instruction has a
number of stages



New inputs are
accepted at one end
before previously
accepted inputs
appear as outputs at
the other end

Timing Diagram for Instruction Pipeline Operation



A timing diagram for an instruction pipeline. It features a grid with 9 rows representing instructions and 14 columns representing time steps. The columns are labeled 1 through 14 at the top. Above the grid, a horizontal arrow points to the right and is labeled 'Time'. Each row is labeled on the left from 'Instruction 1' to 'Instruction 9'. The cells in the grid contain the stages of the pipeline: FI (Fetch Instruction), DI (Decode Instruction), CO (Calculate Operands), FO (Fetch Operands), EI (Execute Instruction), and WO (Write Back). The stages are staggered by one time step for each successive instruction, starting from time step 1 for Instruction 1. For example, Instruction 1 has stages from time step 1 to 6, while Instruction 9 has stages from time step 9 to 14.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Instruction 1	FI	DI	CO	FO	EI	WO								
Instruction 2		FI	DI	CO	FO	EI	WO							
Instruction 3			FI	DI	CO	FO	EI	WO						
Instruction 4				FI	DI	CO	FO	EI	WO					
Instruction 5					FI	DI	CO	FO	EI	WO				
Instruction 6						FI	DI	CO	FO	EI	WO			
Instruction 7							FI	DI	CO	FO	EI	WO		
Instruction 8								FI	DI	CO	FO	EI	WO	
Instruction 9									FI	DI	CO	FO	EI	WO

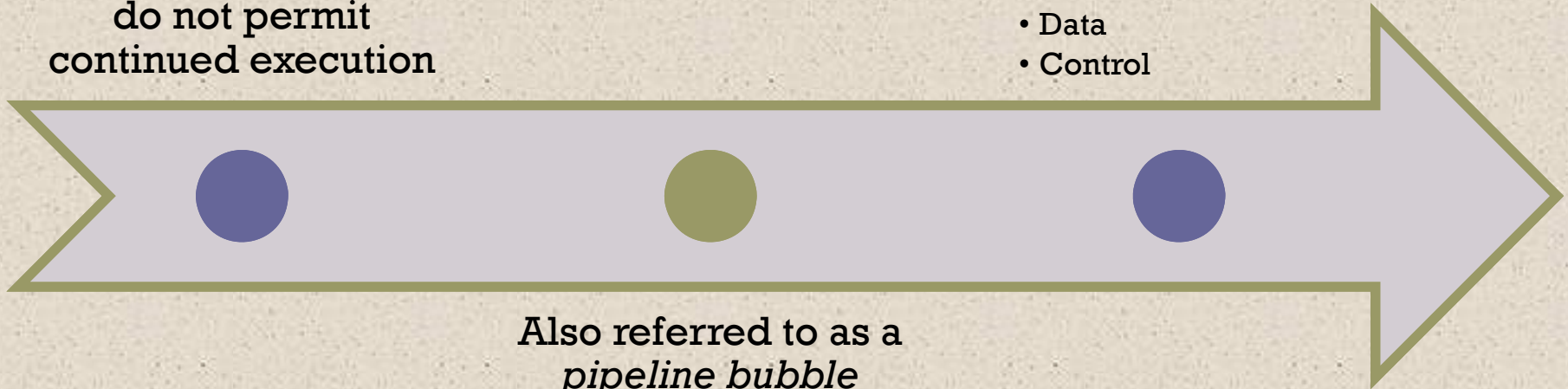
Figure 14.10 Timing Diagram for Instruction Pipeline Operation

Pipeline Hazards

Occur when the pipeline, or some portion of the pipeline, must stall because conditions do not permit continued execution

There are three types of hazards:

- Resource
- Data
- Control



Also referred to as a
pipeline bubble





Resource Hazards

A resource hazard occurs when two or more instructions that are already in the pipeline need the same resource

The result is that the instructions must be executed in serial rather than parallel for a portion of the pipeline

A resource hazard is sometimes referred to as a *structural hazard*

	Clock cycle								
	1	2	3	4	5	6	7	8	9
I1	FI	DI	FO	EI	WO				
I2		FI	DI	FO	EI	WO			
I3			FI	DI	FO	EI	WO		
I4				FI	DI	FO	EI	WO	

(a) Five-stage pipeline, ideal case

	Clock cycle								
	1	2	3	4	5	6	7	8	9
I1	FI	DI	FO	EI	WO				
I2		FI	DI	FO	EI	WO			
I3			Idle	FI	DI	FO	EI	WO	
I4					FI	DI	FO	EI	WO

(b) I1 source operand in memory

Figure 14.15 Example of Resource Hazard