Lecture #3
GPIO: General Purpose Input Output Module

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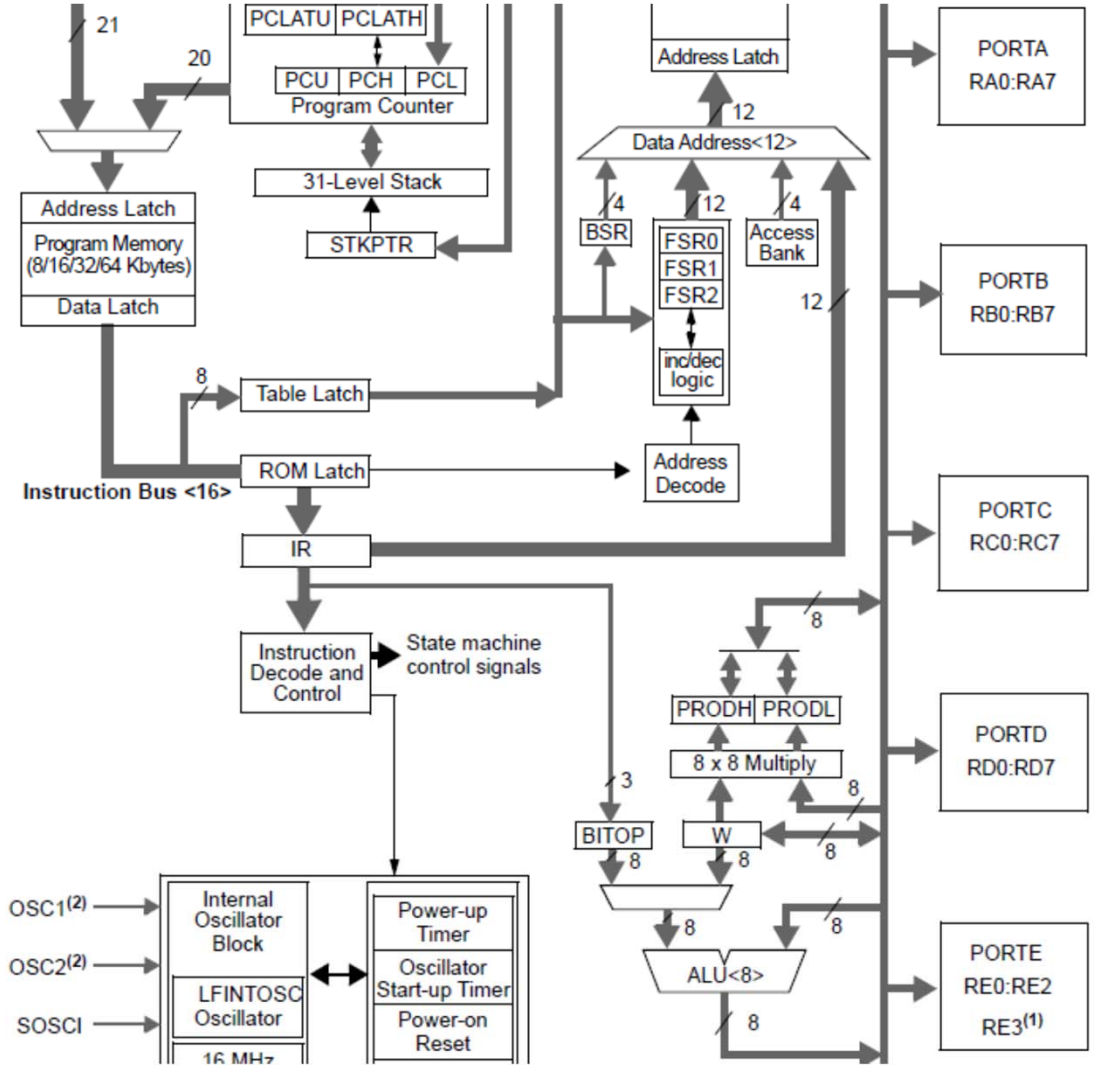
GPIO: General Purpose Input Output Module

- GPIO module provides interfaces for multiple peripherals or I/O devices.
- Generally, PIC18F45K22 provides five popular GPIO Ports, Ports A-E, to interface and access:
  - Most system peripherals
  - on-chip peripherals
  - External peripherals and I/O devices.
- Each GPIO Port can be mapped to an I/O block
  - Each block contains 8 bits or 8 pins.
  - Each bit or each pin can be configured as either input or output pin.
- Any GPIO can be an external edge or level triggered interrupt

GPIO in PIC18F45K22 Microcontroller



GPIO: General Purpose Input Output Module

- Memory Mapped General Purpose I/O (GPIO) Ports
  - 5 general purpose I/O ports: Port A, B, C, D, E
  - Processor communicates with them through memory mapped registers.
  - A set of data and control registers associated with each port.
  - Processor communicates with arbitrary attachments using ports
- Each port has five registers for its operation. These registers are:
  - TRIS register (data direction register)
  - PORT register (reads the levels on the pins of the device)
  - LAT register (output latch)
  - ANSEL register (analog input control)
  - SLRCON register (port slew rate control)

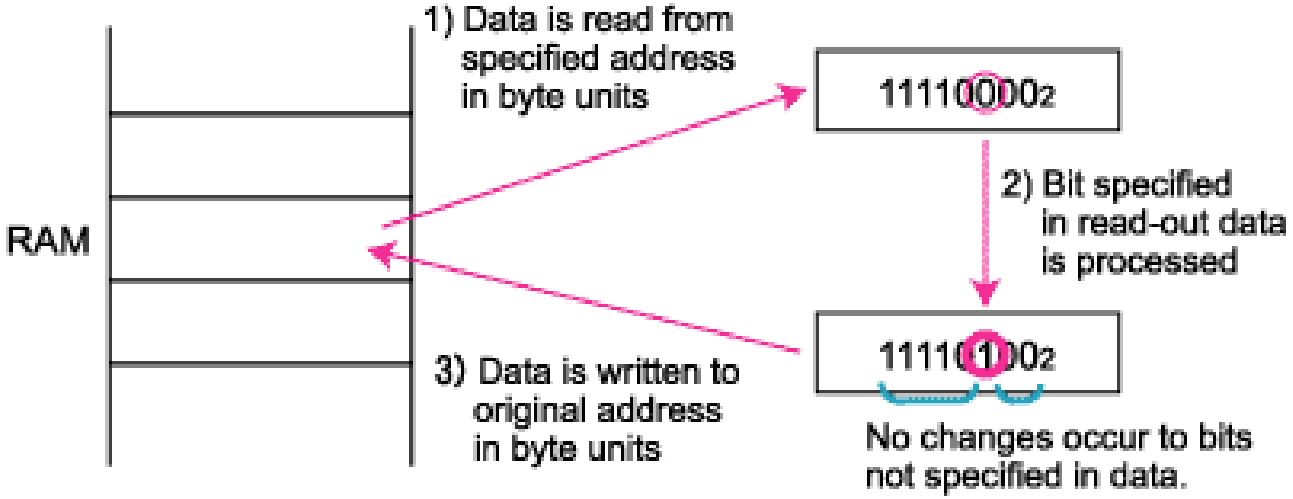
The Data Latch (LAT register) is useful for read-modify-write operations on the value that the I/O pins are driving.

GPIO: General Purpose Input Output Module

The READ-MODIFY-WRITE instruction performs the following operations:

1. Read data from a specified address.
2. Process the bits specified in the read-out data.
3. Write the data to the original address.

Data is written and read in byte units. When processing a bit or performing a logic operation, the data in the bits which are not specified in the data read out (in byte units) are not processed but are simply written to the original address.



GPIO: General Purpose Input Output Module

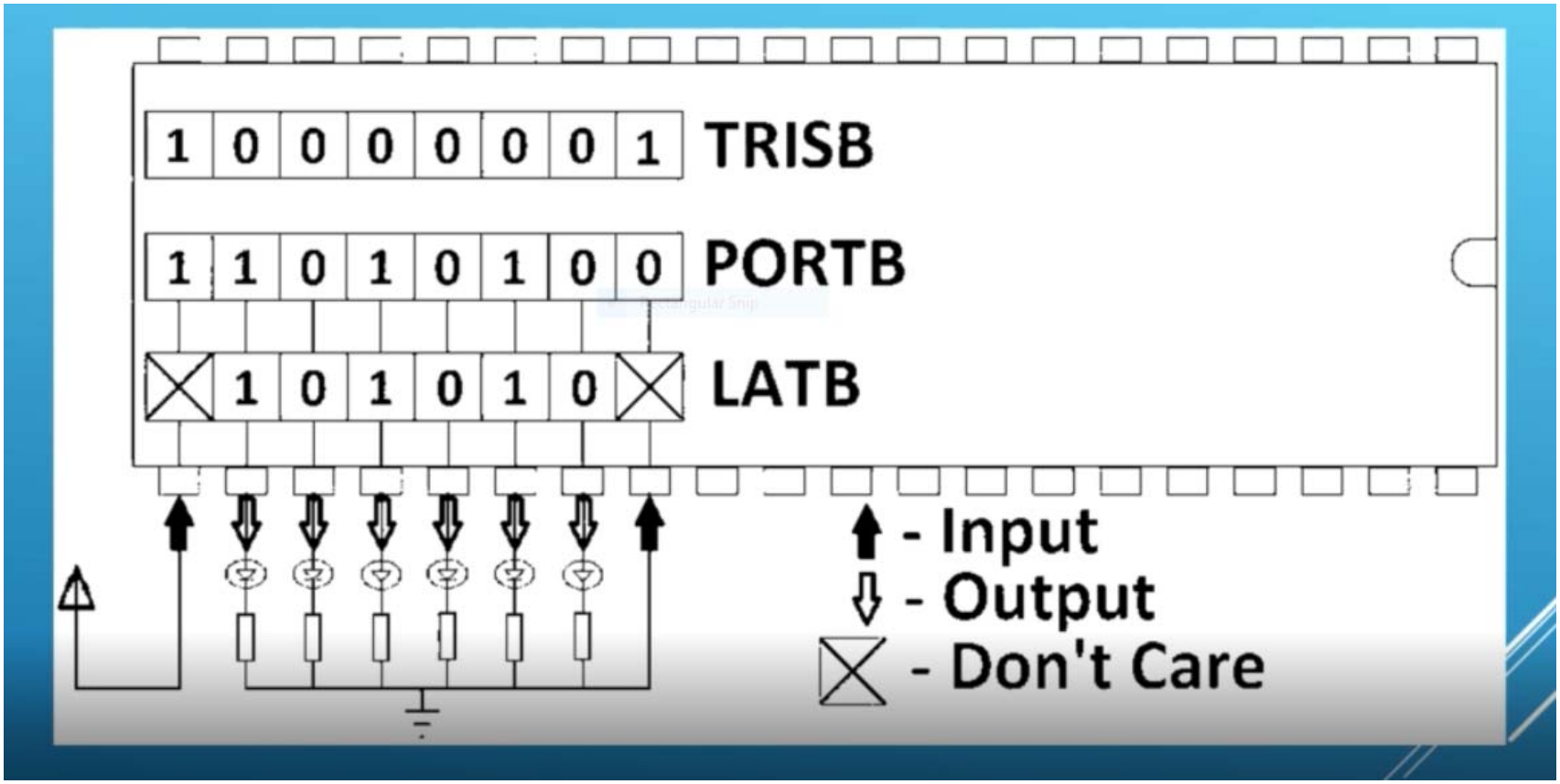
GPIO Registers

The basic and important feature of any microcontrollers is the number of gpio's available for connecting the peripherals. PIC18F45K22 has 36-gpio's grouped into five ports namely PORTA-PORTE as shown in the below table.

PORT	Direction Register	Number of Pins	Alternative Function
PORTA	TRISA	8 (RA0-RA7)	ADC
PORTB	TRISB	8 (RB0-RB7)	Interrupts
PORTC	TRISC	8 (RC0-RC7)	UART,I2C,PWM
PORTD	TRISD	8 (RD0-RD7)	Parallel Slave Port
PORTE	TRISE	4 (PE0-PB3)	ADC

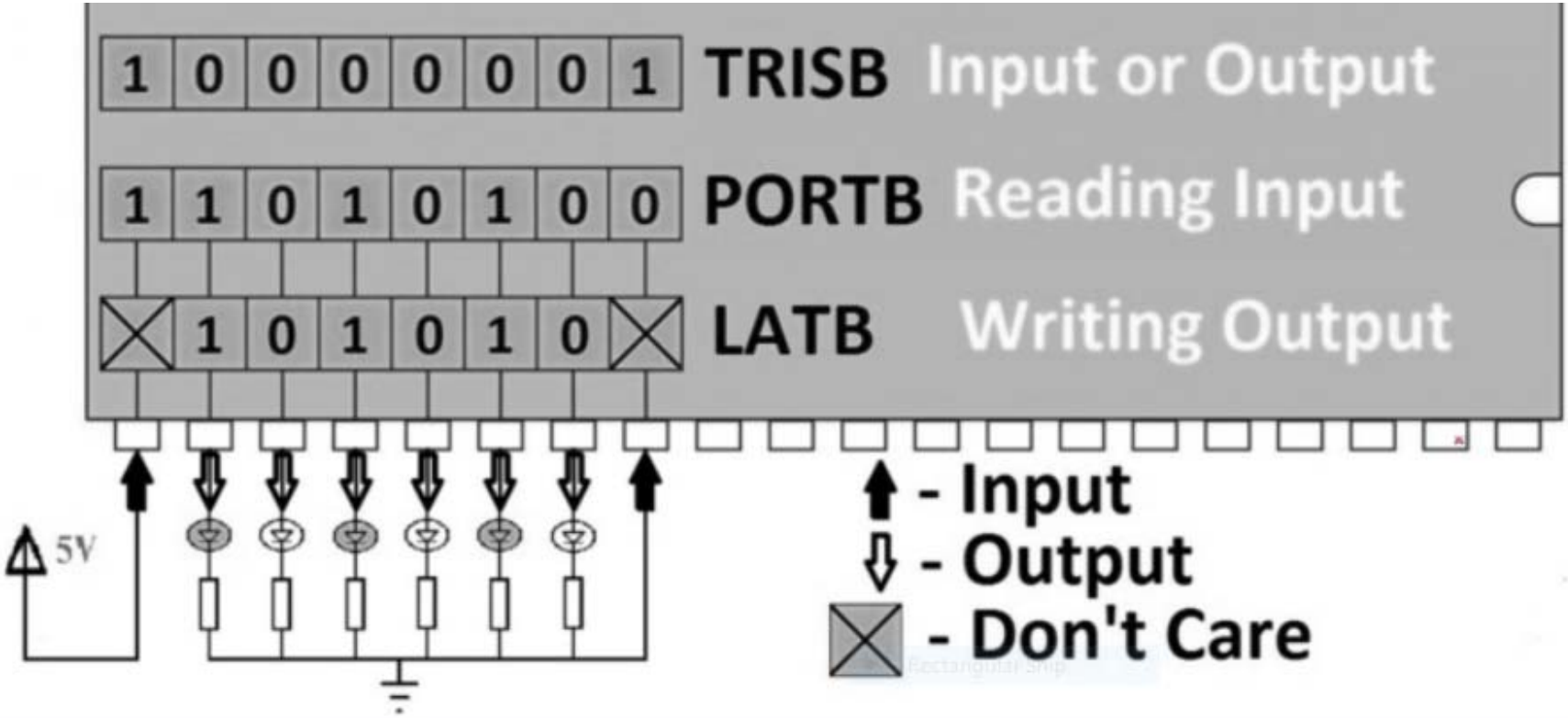
General Purpose Input Output Module

TRIS , PORT, and LAT Registers



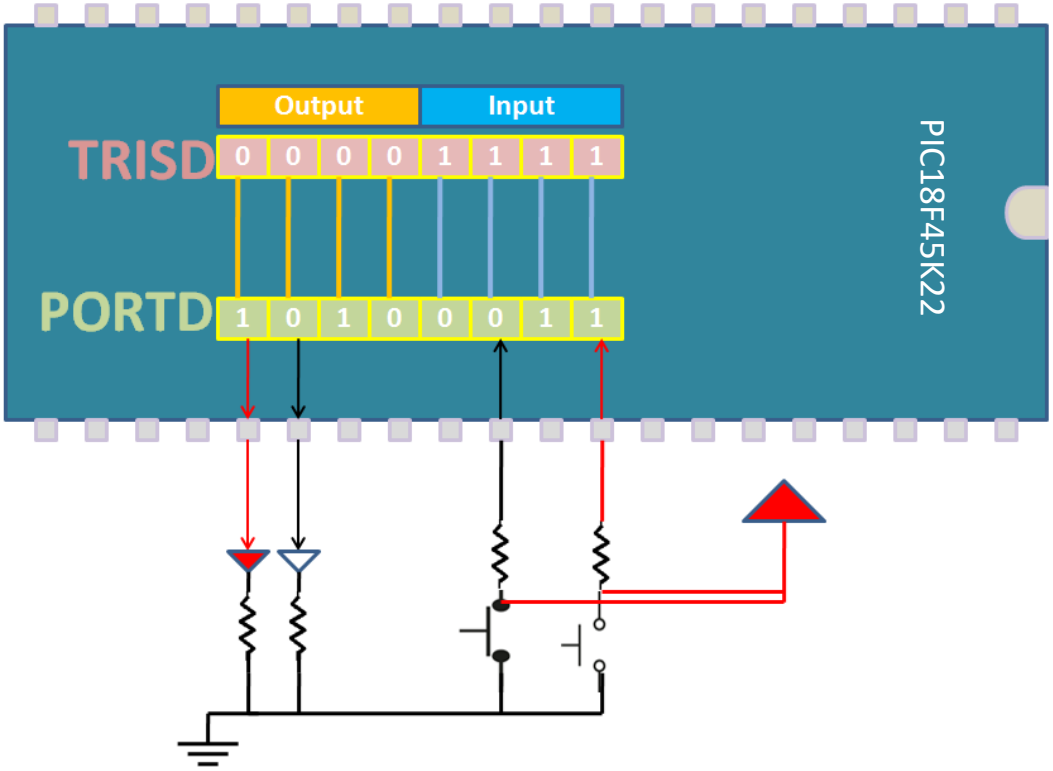
General Purpose Input Output Module

TRIS , PORT, and LAT Registers



General Purpose Input Output Module

TRIS , and PORT Registers



Register	Description
TRISx	Used to configure the respective PORT as output/input
PORTx	Used to Read/Write the data from/to the Port pin

General Purpose Input Output Module

TRISx:TRI-State Register/ Data Direction Register

Before reading or writing the data from the ports, their direction needs to be set. Unless the PORT is configured as output, the data from the registers will not go to controller pins.

This register is used to configure the PORT pins as Input or Output. Writing 1's to TRISx will make the corresponding PORTx pins as Input. Similarly writing 0's to TRISx will make the corresponding PORTx pins as Output.

```
1.TRISB = 0xff;  // Configure PORTB as Input.
2.
3.TRISC = 0x00;  // Configure PORTC as Output.
4.
5.TRISD = 0x0F;  // Configure lower nibble of PORTD as Input and higher nibble as Output
6.
7.TRISD = (1<<0) | (1<<3) | (1<<6); // Configure RD0,RD3,RD6 as Input and others as Output
8.
```

```
1.TRISA0_bit = 1;                    // set RA0 pin as input
2.TRISA0_bit = 0;                    // set RA0 pin as output
```

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PORTx:

This register is used to read/write the data from/to port pins. Writing 1's to PORTx will make the corresponding PORTx pins as HIGH. Similarly writing 0's to PORTx will make the corresponding PORTx pins as LOW.

Before reading/writing the data, the port pins should be configured as InputOutput.

```
1.PORTB = 0xff; // Make all PORTB pins HIGH.
2.
3.PORTC = 0x00; // Make all PORTC pins LOW..
4.
5.PORTD = 0x0F; // Make lower nibble of PORTD as HIGH and higher nibble as LOW
6.
7.PORTD = (1<<PD0) | (1<<PD3) | (1<<PD6); // Make PD0,PD3,PD6 HIGH,
8.
9.
10.TRISB = 0x00; // Configure PORTB as Output
11.TRISD = 0xff; // Configure PORTD as Input
12.PORTD = PORTB; // Read the data from PORTB and send it to PORTD.
```

General Purpose Input Output Module

LATx:

The LATx register associated with an I/O pin eliminates the problems that can occur with read-modify-write instructions. A read of the LATx register returns the values that are held in the port output latches instead of the values on the I/O pins. A read-modify-write operation on the LATx register associated with an I/O port avoids the possibility of writing the input pin values into the port latches. A write to the LATx register has the same effect as a write to the PORTx register.

The differences between the PORTx and LATx registers are summarized in the following table:

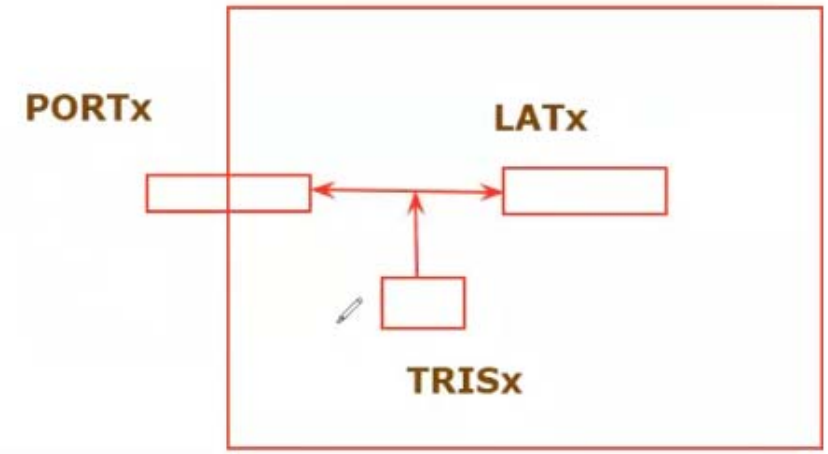
	PORTx	LATx
Read	Reads data value on the I/O pin	Reads data value held in the port latch
Write	Writes data value to the port latch	Writes data value to the port latch

General Purpose Input Output Module

Difference between PORTx and LATx || Role of TRIS

LATx vs PORTx

Some time we read the value from Input PORT, But its not actual value we have applied at input



General Purpose Input Output Module

ANSELx: Port Analog Control

Most port pins are multiplexed with analog functions such as the Analog-to-Digital Converter and comparators. When these I/O pins are to be used as analog inputs it is necessary to disable the digital input buffer to avoid excessive current caused by improper biasing of the digital input. Individual control of the digital input buffers on pins which share analog functions is provided by the ANSELA, ANSELB, ANSELC, ANSELD and ANSELE registers. Setting an ANSx bit high will disable the associated digital input buffer and cause all reads of that pin to return '0' while allowing analog functions of that pin to operate correctly.

ANSELx ➲ Configures the input pins as analog or digital. (1 ➲ Analog , 0 ➲ Digital)

General Purpose Input Output Module

ANSELx: Port Analog Control

REGISTER 10-3: ANSELA – PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ANSA5	—	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

REGISTER 10-4: ANSELB – PORTB ANALOG SELECT REGISTER

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0
bit 7							bit 0

REGISTER 10-5: ANSELC – PORTC ANALOG SELECT REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	U-0	U-0
ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—
bit 7							bit 0

REGISTER 10-6: ANSELD – PORTD ANALOG SELECT REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0
bit 7							bit 0

REGISTER 10-7: ANSELE – PORTE ANALOG SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1
—	—	—	—	—	ANSE2(1)	ANSE1(1)	ANSE0(1)
bit 7							bit 0

Pad Control Registers

- **GPIO Pull-Up and Pull-Down**

  are used to select either Pull-Up or Pull-Down resistor on the output of a pin (only work for input pins).