Pipelined Example

- Consider the following instruction sequence:
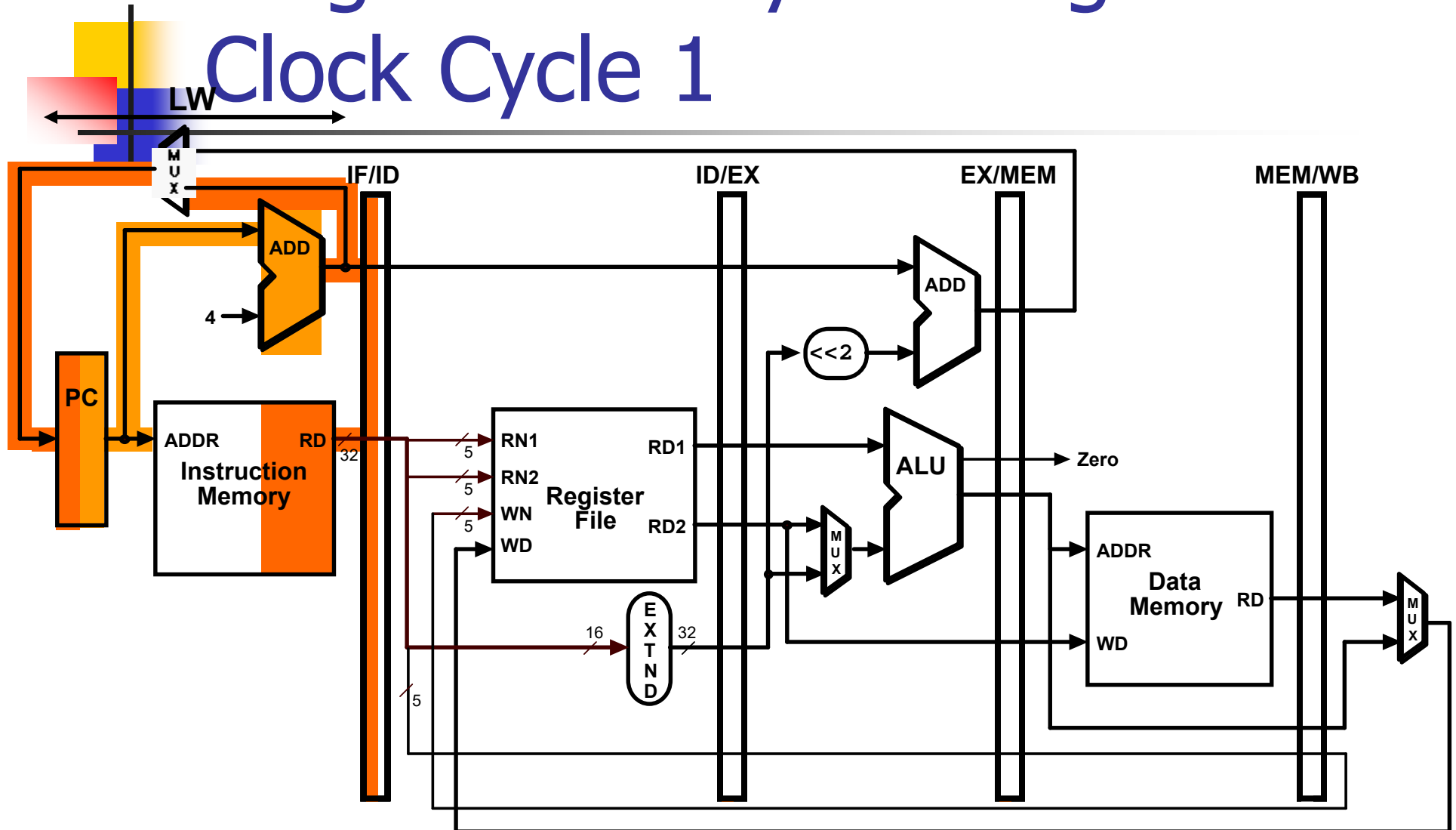
```
lw  $t0,  10($t1)
sw  $t3, 20($t4)
add $t5,  $t6,  $t7
sub $t8,  $t9,  $t10
```
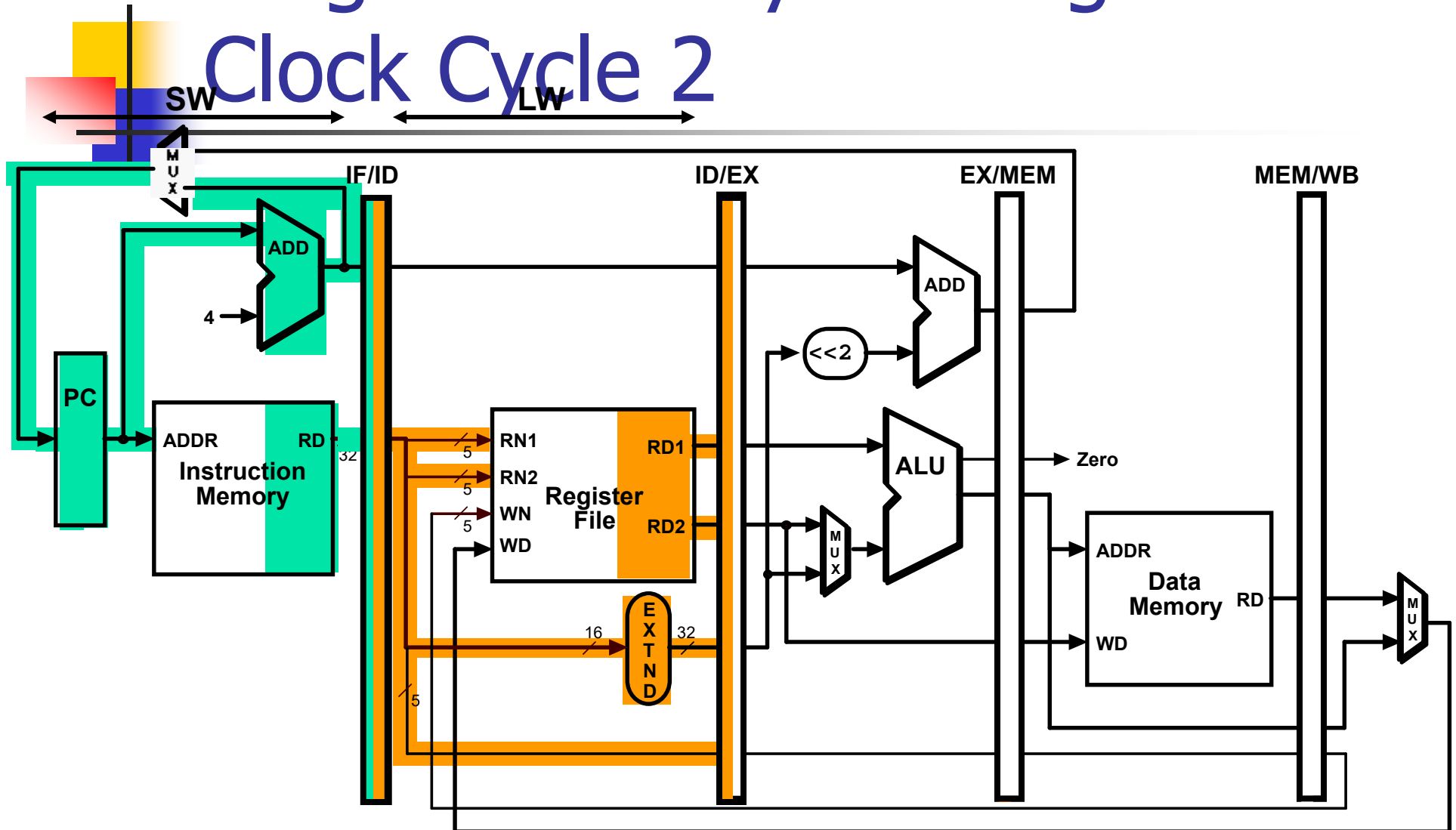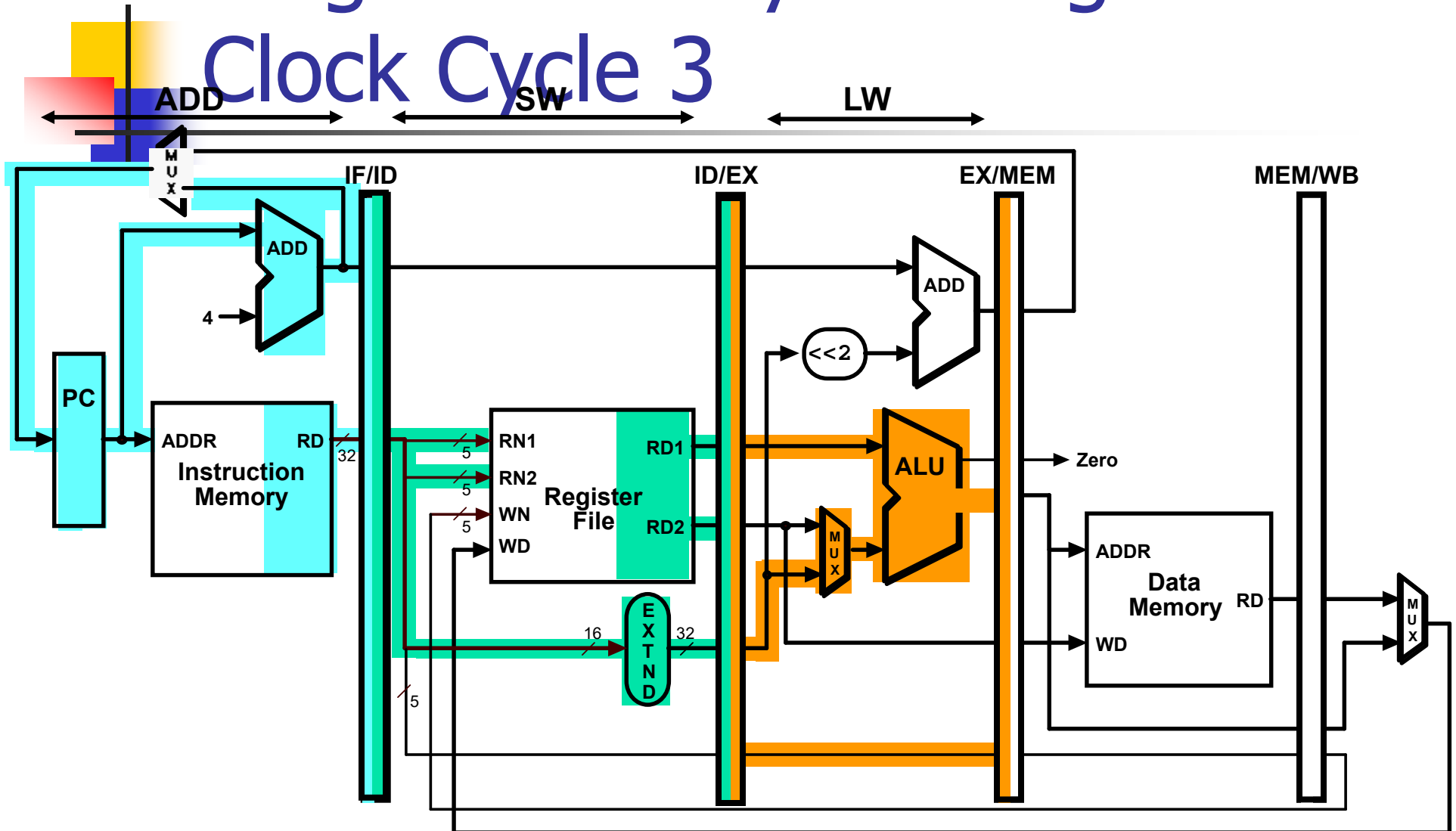
Single-Clock-Cycle Diagram: Clock Cycle 1

Single-Clock-Cycle Diagram: Clock Cycle 2

Single-Clock-Cycle Diagram: Clock Cycle 3

Single-Clock-Cycle Diagram: Clock Cycle 4

SUB   ADD   SW   LW

IF/ID   ID/EX   EX/MEM   MEM/WB

MUX

ADD

4

PC

ADDR   RD
Instruction
Memory
32

ADD

<<2

RN1   RD1
RN2
WN   RD2
WD
Register
File

5
5
5

ALU

Zero

MUX

ADDR
Data
Memory   RD
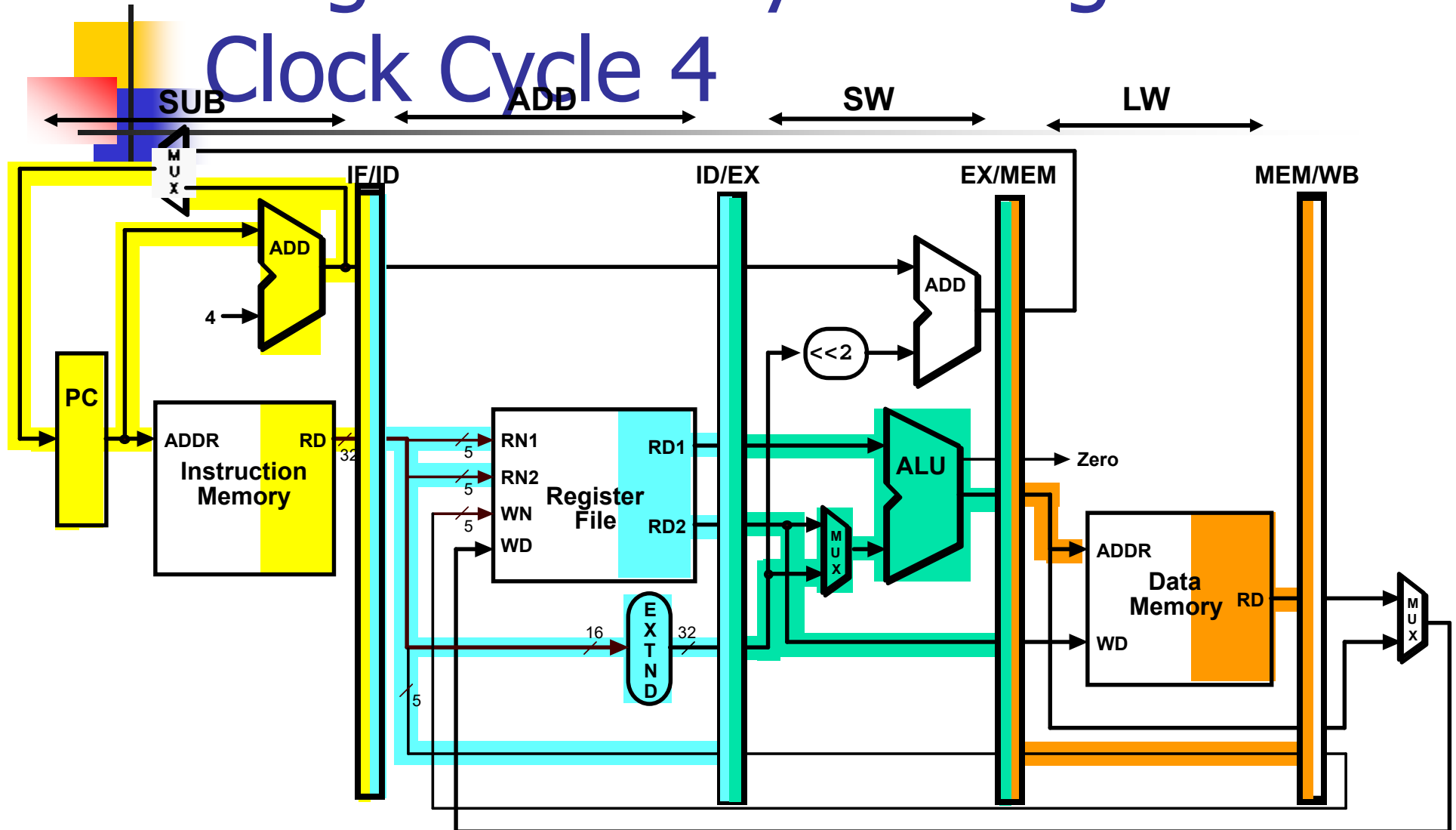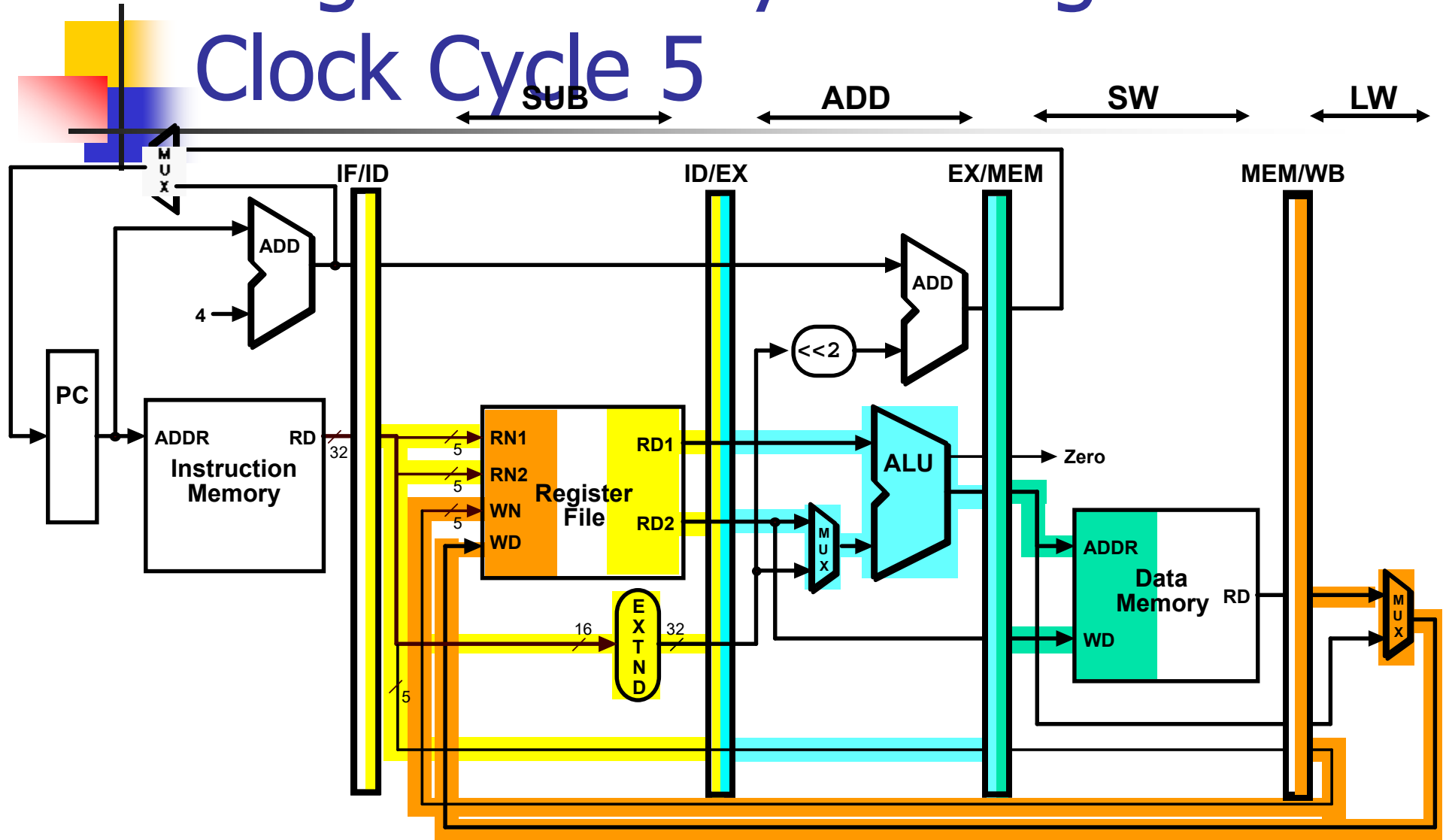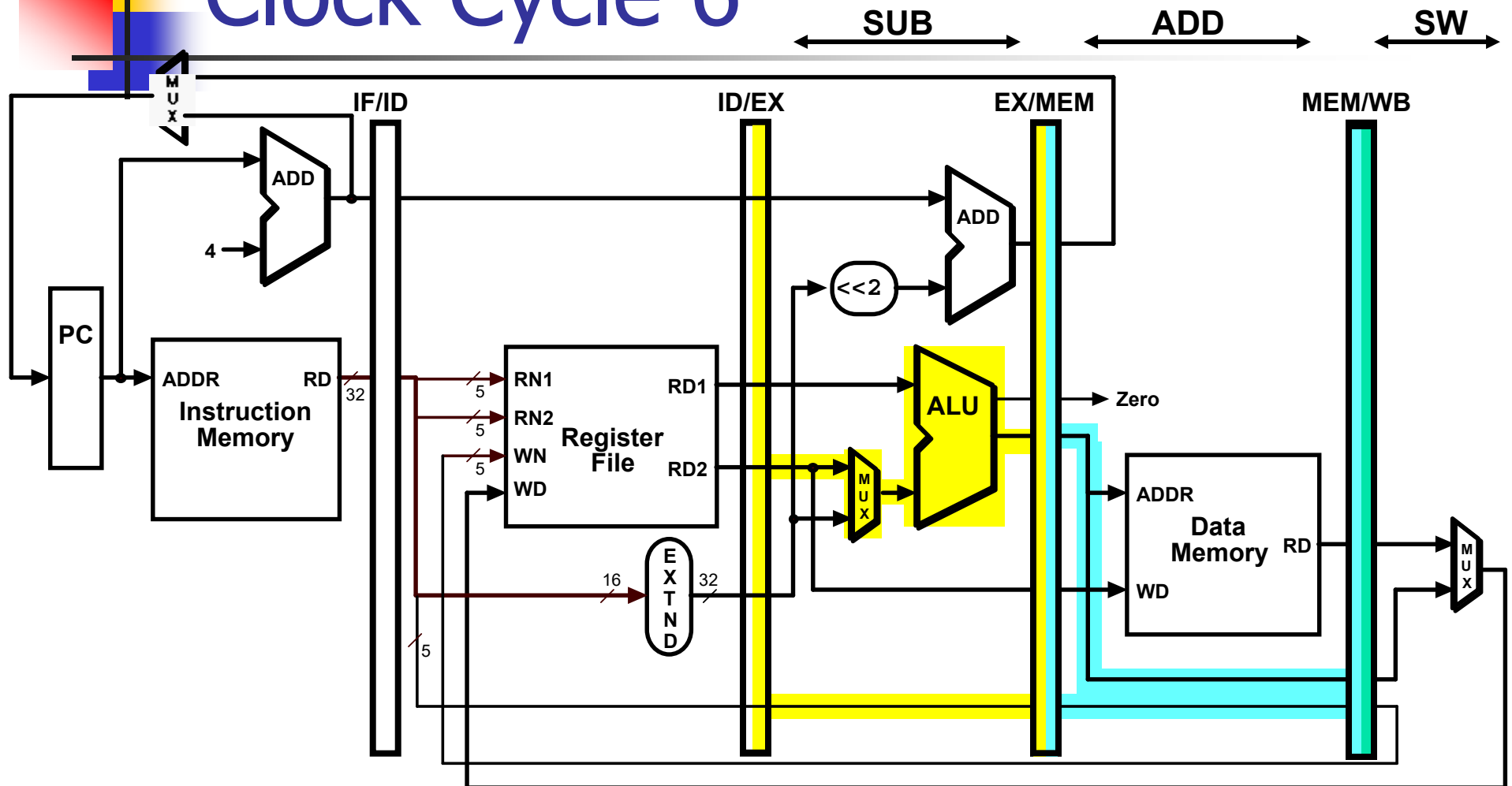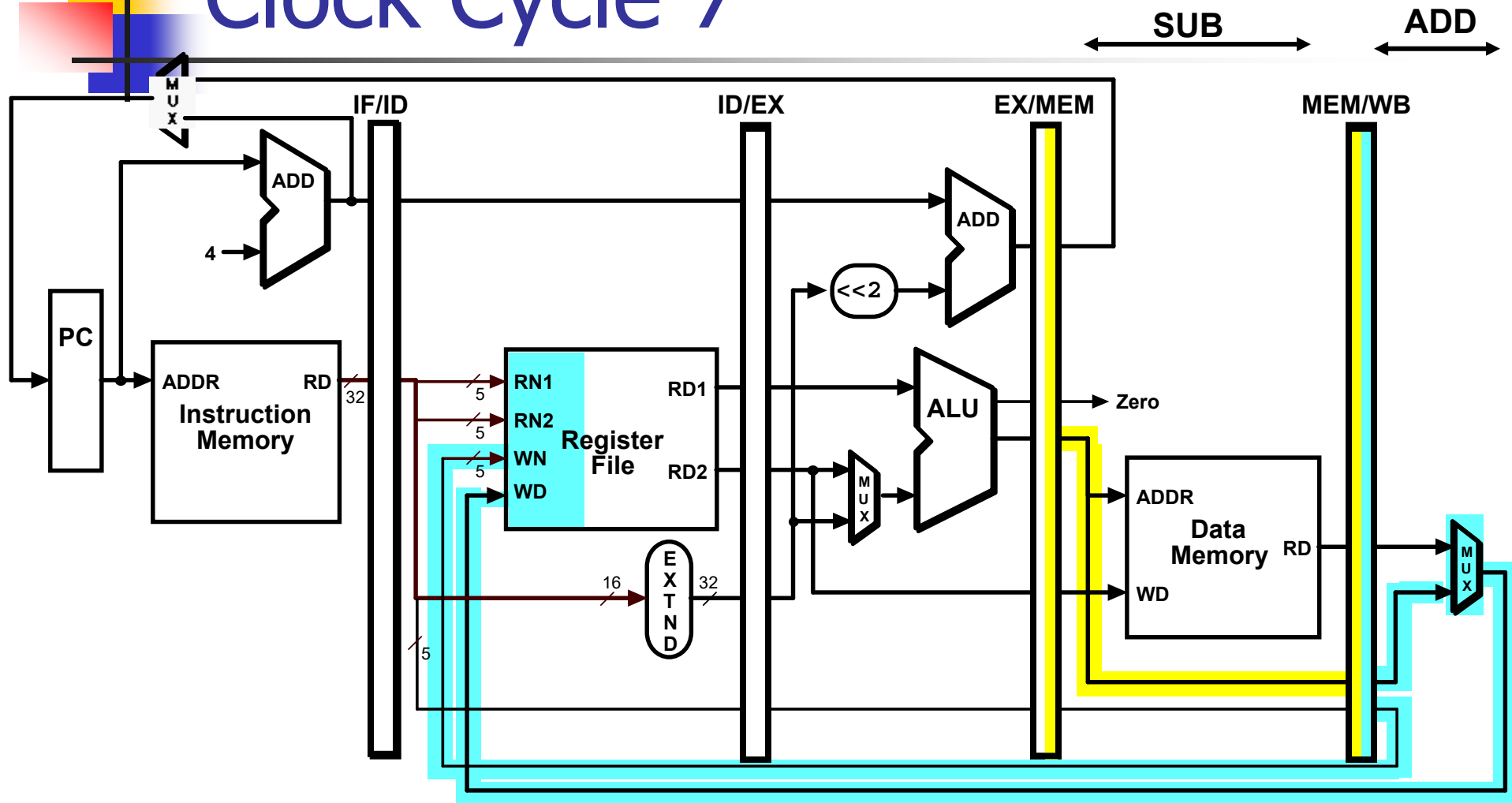
WD

16   E
X
T
N
D   32
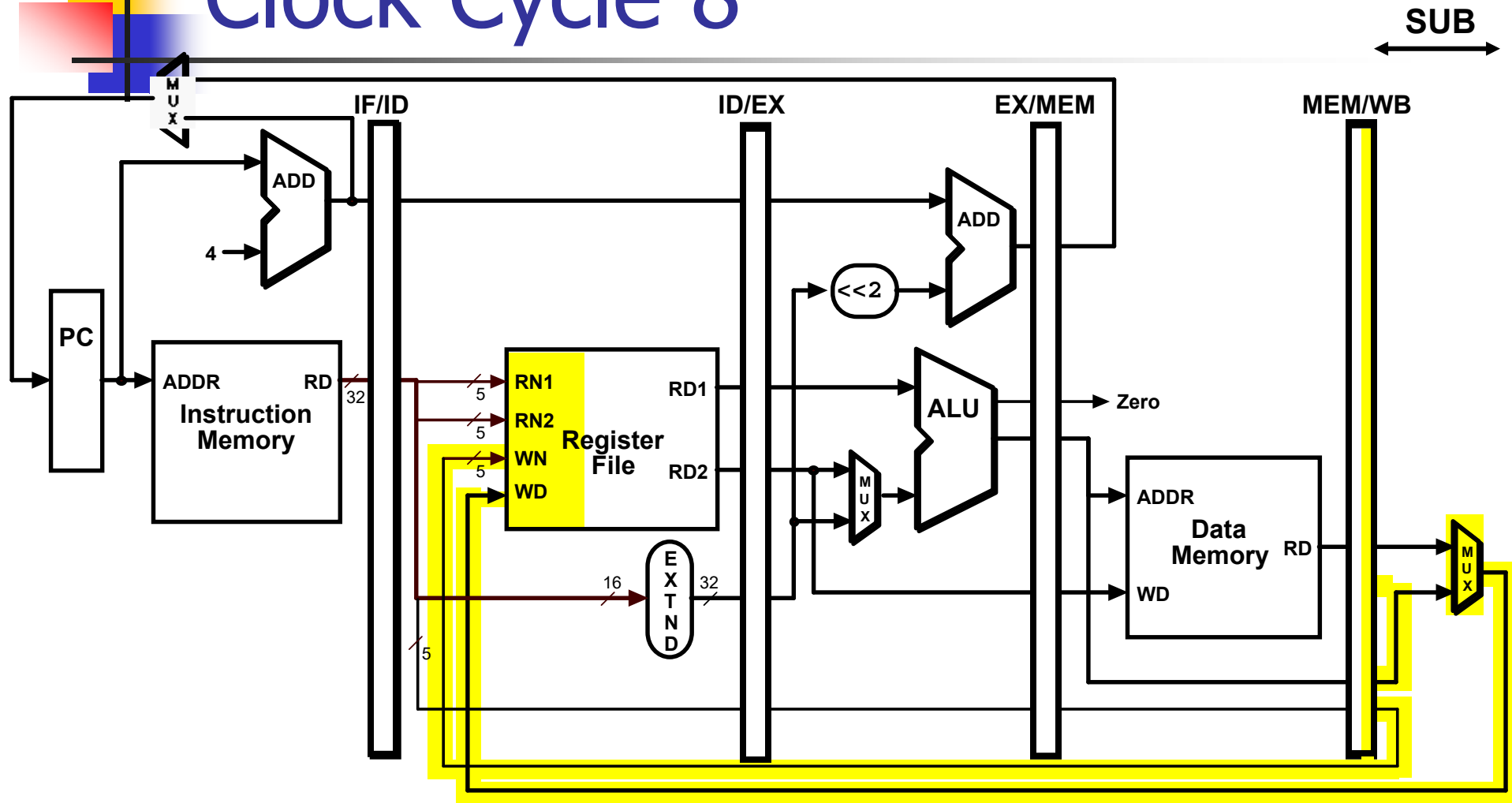
5

MUX

Single-Clock-Cycle Diagram: Clock Cycle 5

Single-Clock-Cycle Diagram: Clock Cycle 6

Single-Clock-Cycle Diagram: Clock Cycle 7

Single-Clock-Cycle Diagram: Clock Cycle 8

Alternative View – Multiple-Clock-Cycle Diagram

CC 1   CC 2   CC 3   CC 4   CC 5   CC 6   CC 7   CC 8

Time axis ⟶

lw $t0, 10($t1)   IM   REG   ALU   DM   REG

sw $t3, 20($t4)   IM   REG   ALU   DM   REG

add $t5, $t6, $t7   IM   REG   ALU   DM   REG

sub $t8, $t9, $t10   IM   REG   ALU   DM   REG