Open source software tools for FPGA developments

Brahim HAMADI CHAREF
Scientist, IHPC / A*STAR

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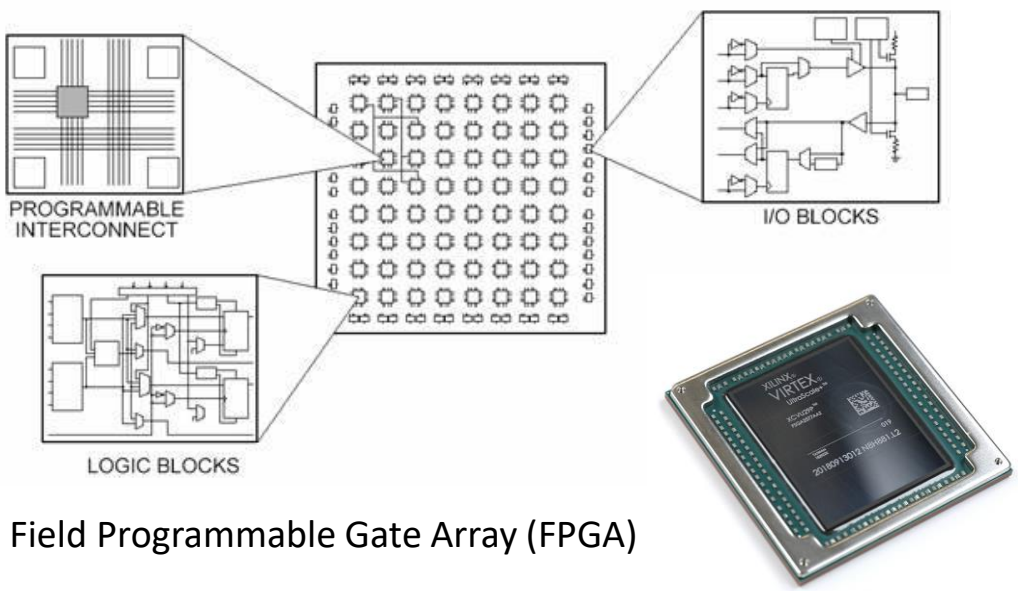
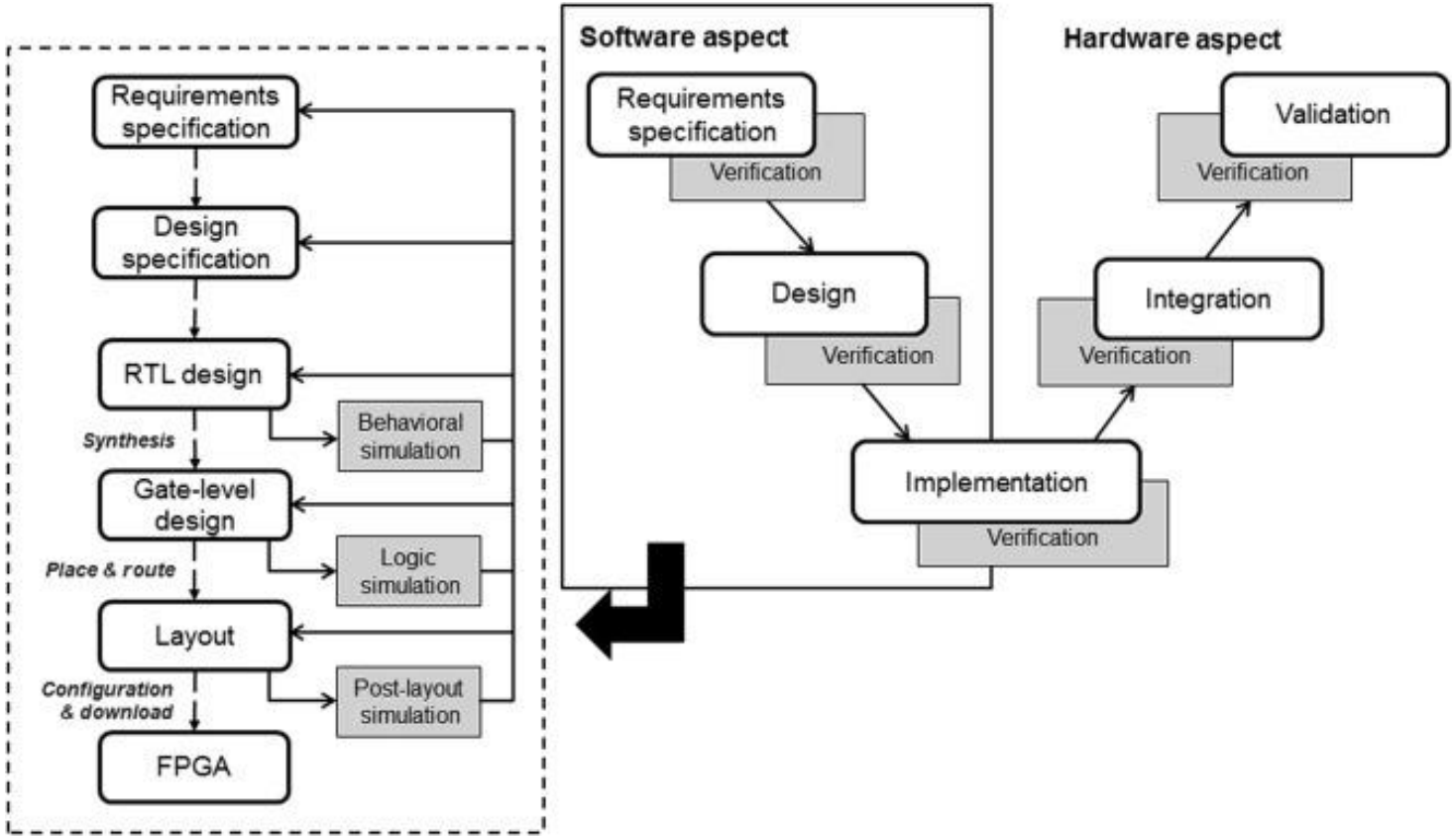
Brahim HAMADI CHAREF

B.Eng EE, M.Eng IE, PhD Audio DSP
Scientist, Computing and Intelligence (CI) Department
Institute of High Performance Computing (IHPC)
Agency for Science, Technology and Research (A*STAR)
https://www.linkedin.com/in/bhamadicharef/
https://twitter.com/BHamadicharef

FPGA Development Cycle



Field Programmable Gate Array (FPGA)



Register-transfer-level (RTL) design is about creating digital logic circuits using hardware description languages like Verilog HDL, VHDL

An Integrated Software Testing Framework for FPGA-Based Controllers in Nuclear Power Plants
Jaeyeob Kim, Eui-Sub Kim, Junbeom Yoo, Young Jun Lee, Jong-Gyun Choi
Nuclear Engineering and Technology Volume 48, Issue 2, April 2016, Pages 470-481
https://doi.org/10.1016/j.net.2015.12.008

FPGA Development Tool

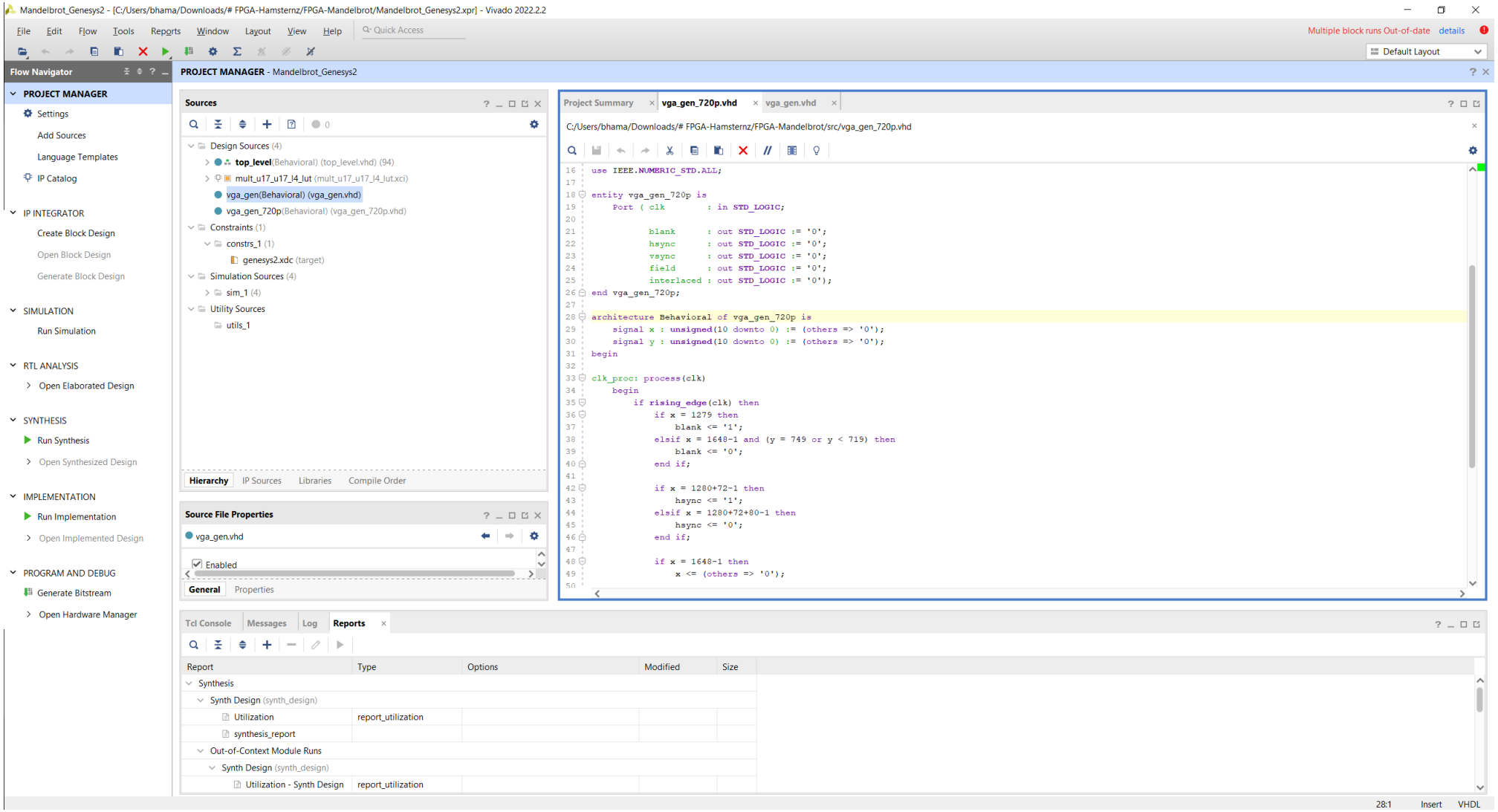
(ALL FREE)

Xilinx (AMD) Vivado

Altera (Intel) Quartus

Lattice Diamond

GoWin EDA



Yosys+nextpnr FCCM2019 Paper

Yosys+nextpnr: an Open Source Framework from Verilog to Bitstream for Commercial FPGAs
David Shah, Eddie Hung, Clifford Wolf, Serge Bazanski, Dan Gisselquist, Miodrag Milanović
Proceedings of the 2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM) April 28 2019 to May 1 2019 San Diego, CA, USA
DOI: https://doi.org/10.1109/FCCM.2019.00010
arXiv: https://arxiv.org/abs/1903.10407

Abstract: This paper introduces a fully free and open source software (FOSS) architecture-neutral FPGA framework comprising of **Yosys for Verilog synthesis, and nextpnr for placement, routing, and bitstream generation**. Currently, this flow supports two commercially available FPGA families, Lattice iCE40 (up to 8K logic elements) and Lattice ECP5 (up to 85K elements) and has been hardware-proven for custom-computing machines including a low-power neural-network accelerator and an OpenRISC system-on-chip capable of booting Linux. Both Yosys and nextpnr have been engineered in a highly flexible manner to support many of the features present in modern FPGAs by separating architecture-specific details from the common mapping algorithms. This framework is demonstrated on a longest-path case study to find an atypical single source-sink path occupying up to 45% of all on-chip wiring.

Yosys Open SYnthesis Suite

- Framework for RTL synthesis tools
  https://yosyshq.net/yosys/
- Can be fully built from source
- Verilog and SystemVerilog supported
  VHDL using GHDL https://github.com/ghdl/ghdl
- YosysHQ - yosys
  https://github.com/YosysHQ/yosys
- YosysHQ additional projects
  - SymbiYosys (SBY) is a front-end for Yosys-based formal verification flows
  - Many other projects like Trellis for ECP5 FPGAs
  - PicoRV32 implementing the RISC-V RV32IMC (Base Integer Instruction Set, M Standard Extension for Integer Multiplication and Division, and C Standard Extension for Compressed Instructions)

Project X-Ray

- Project X-Ray documents the Xilinx 7-Series FPGA architecture to enable the development of open-source tools
- Main goal is to provide sufficient information to develop a free and open Verilog to bitstream toolchain for these devices.
- Minitests, designs viewed by a human in Vivado to gain better understand on how to generate useful designs
- Experiments are like "minitests" except are only useful for a short period of time.
- Fuzzers are the scripts which generate the large number of bitstream
- F4PGA prjxray: https://github.com/f4pga/prjxray

nextpnr - A portable FPGA place and route tool

- **Portable FPGA place and route tool**
  Same as yosys, can be fully built from source
- YosysHQ - nextpnr
  https://github.com/YosysHQ/nextpnr

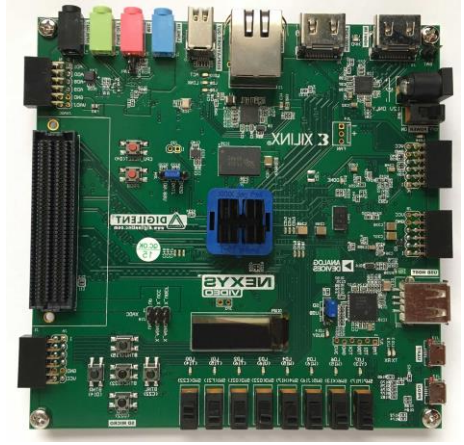
- Lattice iCE40 devices supported by Project IceStorm
  https://github.com/YosysHQ/icestorm
- Lattice ECP5 devices supported by Project Trellis
  Lattice MachXO2 devices supported by Project Trellis (experimental)
  https://github.com/YosysHQ/prjtrellis
- Lattice Nexus devices supported by Project Oxide
  https://github.com/gatecat/prjoxide
- Gowin LittleBee devices supported by Project Apicula
  https://github.com/YosysHQ/apicula
- Intel Cyclone V devices supported by Mistral (experimental)
  https://github.com/Ravenslofty/mistral

Supported FPGA Manufacturers

Lattice Semiconductors FPGAs
ECP5 General Purpose FPGAs
ICE40 Ultra Low Power FPGAs
Nexus Ultra Low Power FPGAs
https://www.latticesemi.com/Products/FPGAandCPLD/ECP5
https://www.latticesemi.com/Products/FPGAandCPLD/iCE40
https://www.latticesemi.com/solutions/solutions/solutionsdetails02/latticenexus

GOWIN FPGAs
LittleBee Flash Based FPGAs
https://www.gowinsemi.com/en/product/detail/46/

Altera (Intel) FPGAs
MAX10 and Cyclone IV
https://www.intel.com/content/www/us/en/products/details/fpga.html



Xilinx (AMD) Series 7 FPGAs
28nm Spartan, Artix, Kintex, Virtex
20nm UltraScale Artix, Kintex, Virtex
16nm UltraScale+ Artix, Kintex, Virtex
https://docs.xilinx.com/v/u/en-US/7-series-product-selection-guide

FPGA Community Singapore

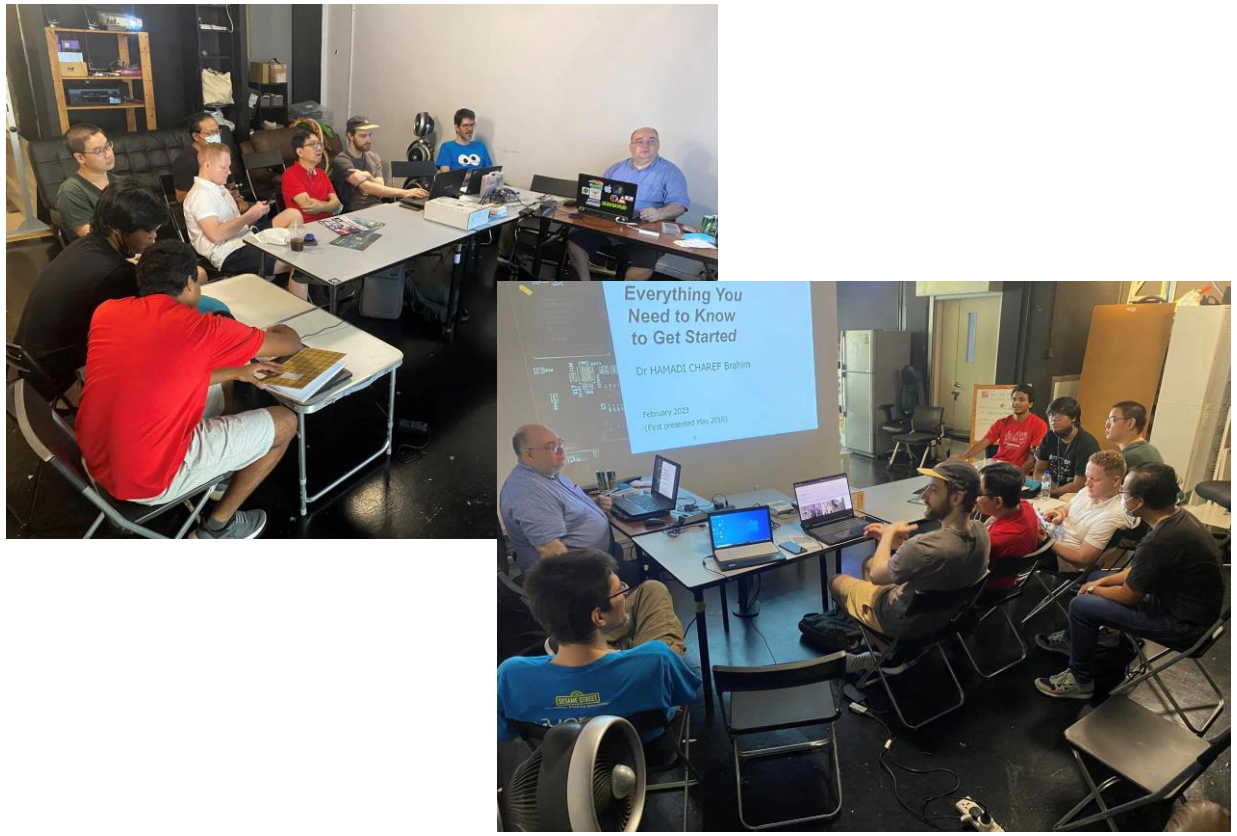
Facebook FPGA Community Singapore
https://www.facebook.com/groups/fpga.sg

"Hackware x FPGA Day"
early July 2023 at Hackerspace.SG

Presentations/talks

Live demonstrations

FPGA applications



Paper We Love - Singapore Chapter

Yosys+nextpnr: an Open Source Framework from Verilog to Bitstream for Commercial FPGAs
David Shah, Eddie Hung, Clifford Wolf, Serge Bazanski, Dan Gisselquist, Miodrag Milanović
Proceedings of the 2019 IEEE 27th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), San Diego, CA, USA, April 28 - May 1, 2019
DOI: https://doi.org/10.1109/FCCM.2019.00010

A Complete Open Source Design Flow for Gowin FPGAs
Pepijn de Vos, Michael Kirchhoff, Daniel Ziener
2020 International Conference on Field-Programmable Technology (ICFPT), Maui, HI, USA, December 9-11, 2020
https://doi.org/10.1109/ICFPT51103.2020.00033

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https://paperswelove.org/chapter/singapore/