Tools for FPGA Development

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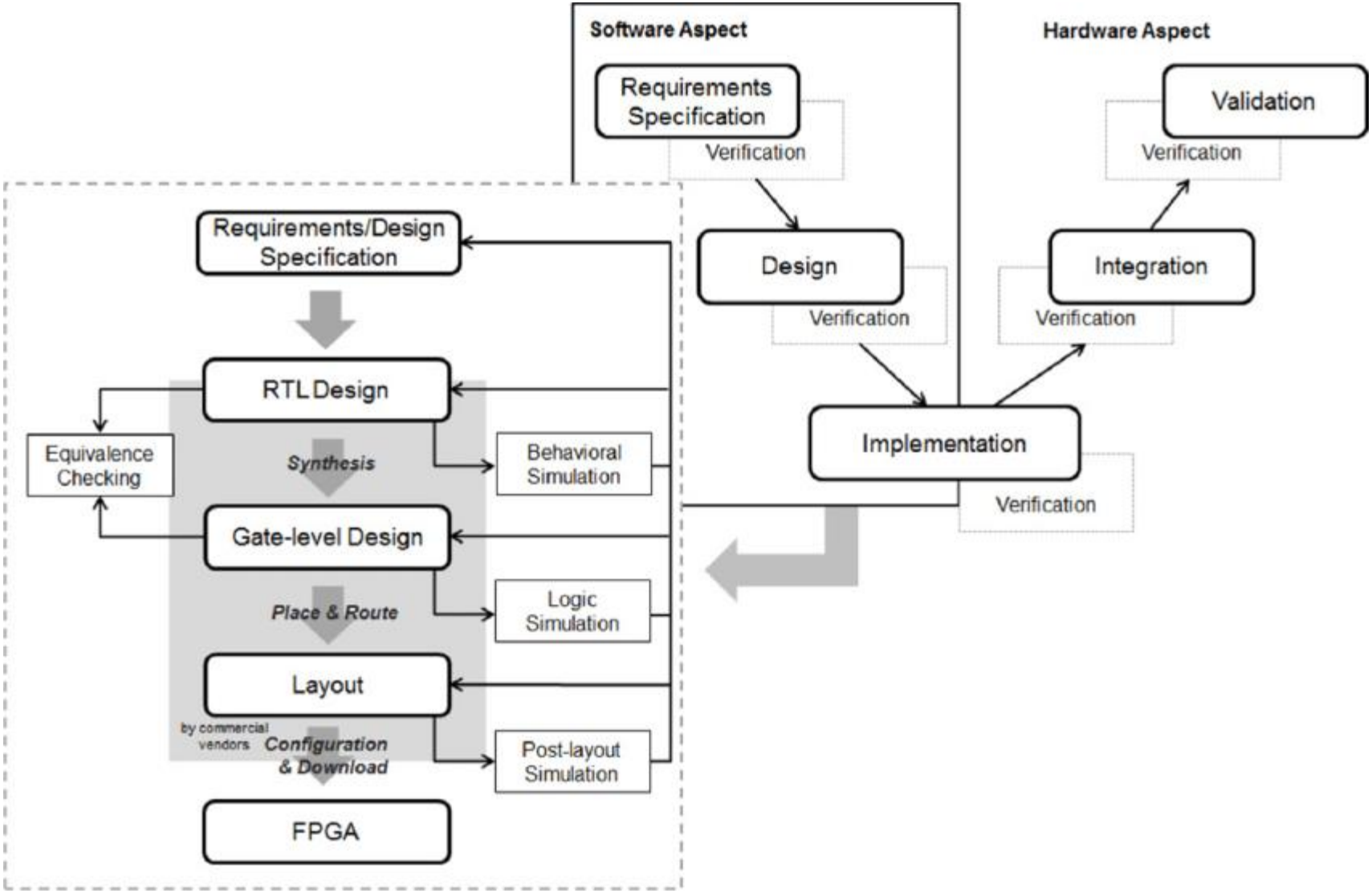
Hackware V5.0

FPGA Market 2016

	2015		2016		
Vendor	FPGA Total	Market share	FPGA Total	Market share	Growth CY15-CY16
Xilinx	$2,044	53%	$2,167	53%	6%
Intel (Altera)	$1,389	36%	$1,486	36%	7%
Microsemi	$301	8%	$297	7%	-1%
Lattice	$124	3%	$144	3%	16%
QuickLogic	$19	0%	$11	0%	-40%
Others	$2	0%	$2	0%	0%
TOTAL	**$3,879**	**100%**	**$4,112**	**100%**	**6%**

FPGA development life-cycle

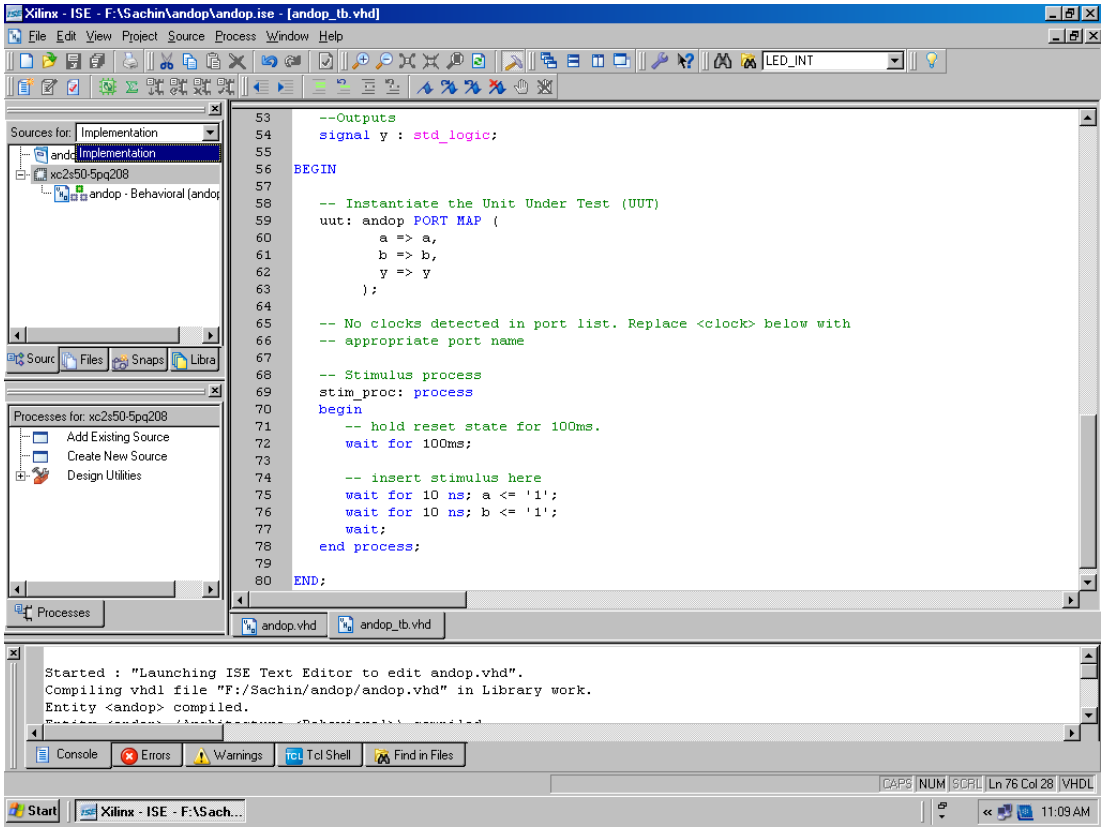


FPGA Tools

- **Xilinx ISE and Vivado**
  https://www.xilinx.com/products/design-tools/vivado.html
- **Altera / Intel Quartus**
  https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/download.html
- **Lattice Diamond Suite**
  https://www.latticesemi.com/Products/DesignSoftwareAndIP/FPGAandLDS/LatticeDiamond
- **Microsemi Libero**
- https://www.microsemi.com/product-directory/services/3711-fpga-soc-design
- **Verilator**
  https://www.veripool.org/wiki/verilator
- **Yosys Open SYnthesis Suite**
  http://www.clifford.at/yosys/

Xilinx ISE Design Suite

ISE Design Suite: WebPACK Edition delivers a complete, front-to-back design flow providing instant access to the ISE features and functionality at no cost.



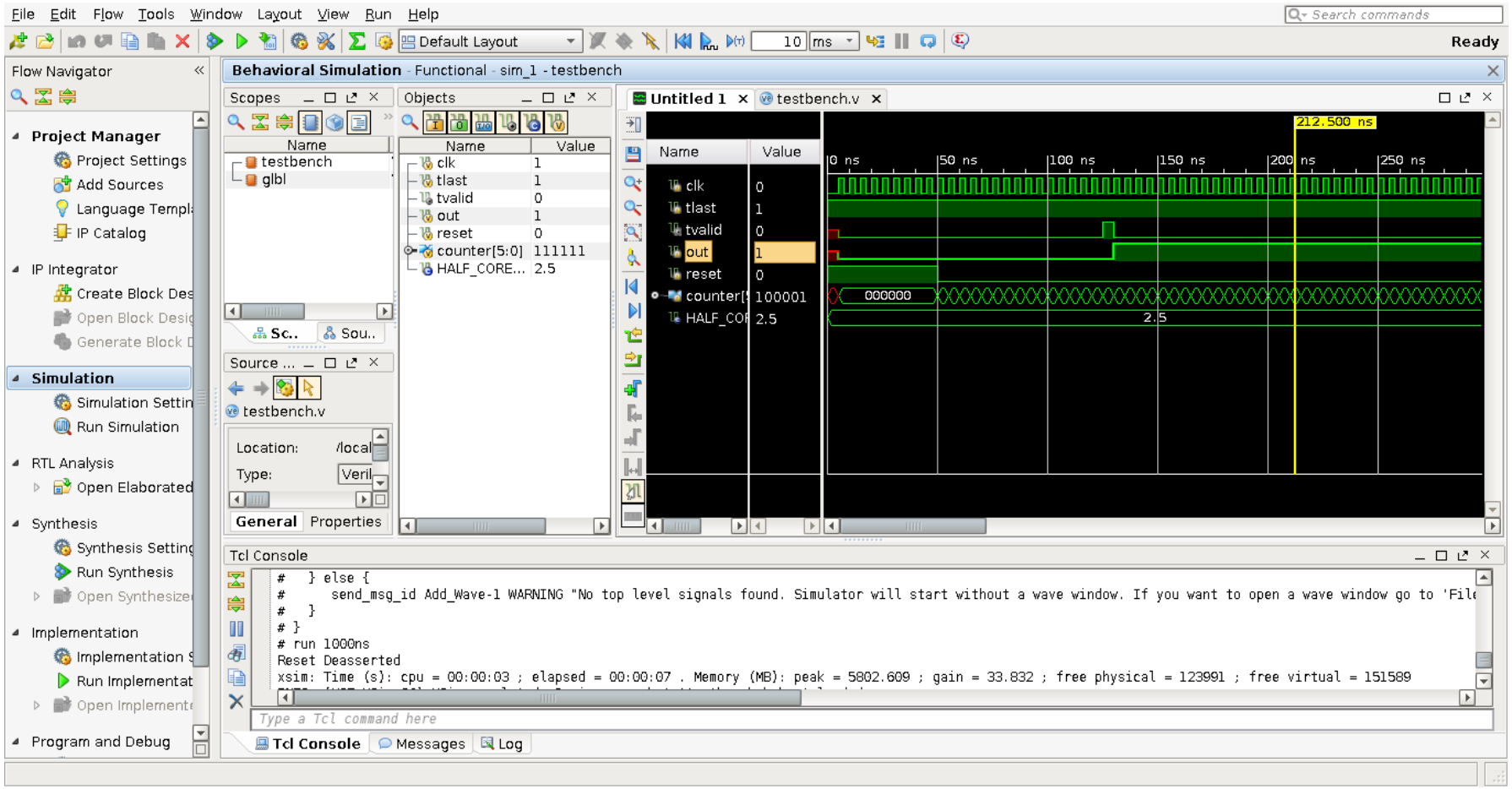
ISE Design Suite: WebPACK Edition

https://www.xilinx.com/products/design-tools/ise-design-suite.html

Xilinx ISE Features

Features	ISE WebPACK	Embedded Edition	System Edition
Device Support	Limited	All	All
ChipScope™ Pro and the ChipScope Pro Serial I/O Toolkit	✓	✓	✓
CORE Generator™	✓	✓	✓
Design Preservation	✓	✓	✓
Embedded IP Peripherals	✓	✓	✓
ISE Simulator (ISim)	Limited	✓	✓
MicroBlaze Soft Processor	✓	✓	✓
Partial Reconfiguration*	Option	Option	Option
PlanAhead™	✓		
Platform Studio	✓	✓	✓
Power Optimization	✓	✓	✓
Project Navigator	✓	✓	✓
Software Development Kit (SDK)	✓	✓	✓
System Generator for DSP			✓
Timing Driven Place & Route, SmartGuide, and SmartXplorer	✓	✓	✓
XST Synthesis	✓	✓	✓

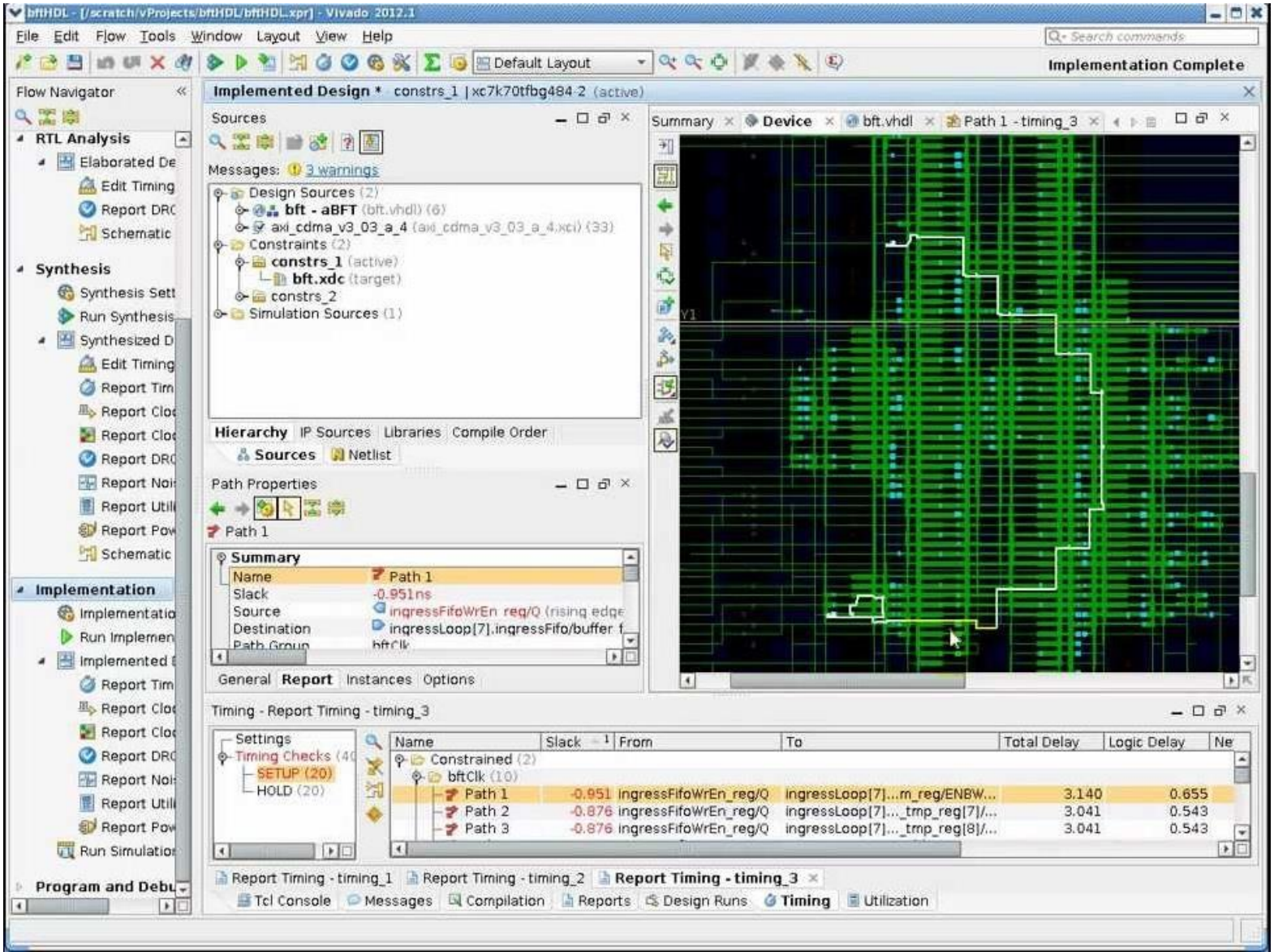
Xilinx Vivado Design Suite



Vivado Design Suite - HLx Editions

https://www.xilinx.com/products/design-tools/vivado.html

Xilinx Vivado Design Suite



Altera bought by Intel

Intel Completes Acquisition of Altera
SANTA CLARA, Calif., Dec. 28, 2015 – Intel Corporation (“Intel”) today announced that it has completed the acquisition of Altera Corporation (“Altera”), a leading provider of field-programmable gate array (FPGA) technology. The acquisition complements Intel’s leading-edge product portfolio and enables new classes of products in the high-growth data center and Internet of Things (IoT) market segments.
https://newsroom.intel.com/news-releases/intel-completes-acquisition-of-altera/

Why Intel will spend $16.7 billion on Altera
https://fortune.com/2015/08/27/why-intel-altera/

Altera / Intel Quartus

Intel Quartus Prime Design Software
Release date: September, 2018 / Latest Release: v18.1
https://www.intel.com/content/www/us/en/software/programmable/overview.html

Pro Edition The Intel® Quartus® Prime Pro Edition Software supports the advanced features in Intel's next-generation FPGAs and SoCs with the Intel® Stratix® 10, Intel® Arria® 10, and Intel® Cyclone® 10 GX device families.
http://fpgasoftware.intel.com/?edition=pro (paid license required)

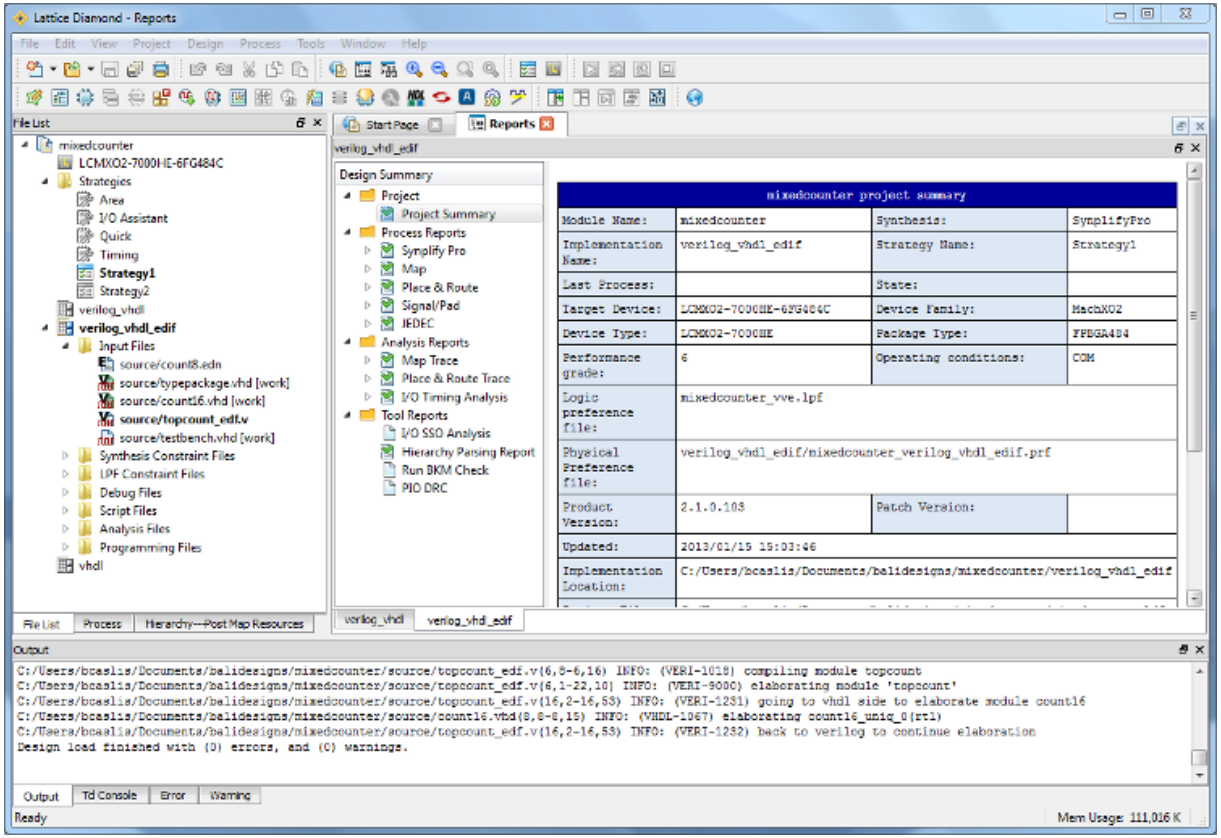
Standard Edition The Intel® Quartus® Prime Standard Edition software includes extensive support for earlier device families in addition to the Intel® Cyclone® 10 LP device family.
http://fpgasoftware.intel.com/?edition=standard (paid license required)

Lite Edition The Intel® Quartus® Prime Lite Edition software supports Intel's low-cost FPGA device families
http://fpgasoftware.intel.com/?edition=lite (free, no license required)

Lattice Diamond Suite

Support for
ECP5 / ECP5-5G
LatticeECP3
MachXO3
MachXO2
LatticeXP2

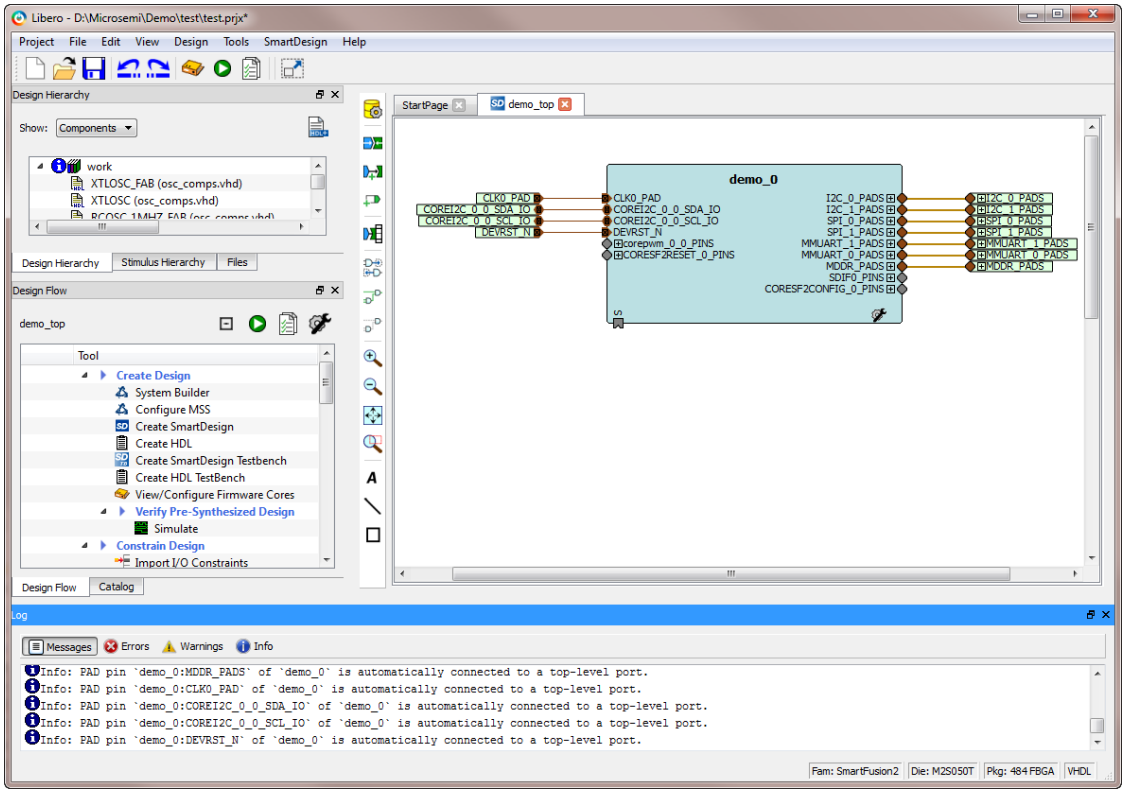
Features Complete
GUI based FPGA design and verification environment, Design exploration in a single project with multiple implementations and settings strategies, Graphical environment for managing and navigating timing and power results



Lattice Diamond Suite
https://www.latticesemi.com/Products/DesignSoftwareAndIP/FPGAandLDS/LatticeDiamond

Microsemi Libero

Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's PolarFire, IGLOO2, SmartFusion2, RTG4, SmartFusion, IGLOO, ProASIC3 and Fusion families. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation



Microsemi

https://www.microsemi.com/product-directory/fpga-soc/1637-design-resources

Verilator

Verilator is the fastest free Verilog HDL simulator, and outperforms most commercial simulators. Verilator compiles synthesizable SystemVerilog (generally not test-bench code), plus some SystemVerilog and Synthesis assertions into single- or multithreaded C++ or SystemC code. Verilator is designed for large projects where fast simulation performance is of primary concern, and is especially well suited to generate executable models of CPUs for embedded software design teams

https://www.veripool.org/wiki/verilator

Verilator Installation
Verilator Documentation
Verilator FAQ

Yosys Open SYnthesis Suite

Yosys is a framework for Verilog RTL synthesis. It currently has extensive Verilog-2005 support and provides a basic set of synthesis algorithms for various application domains. Selected features and typical applications:

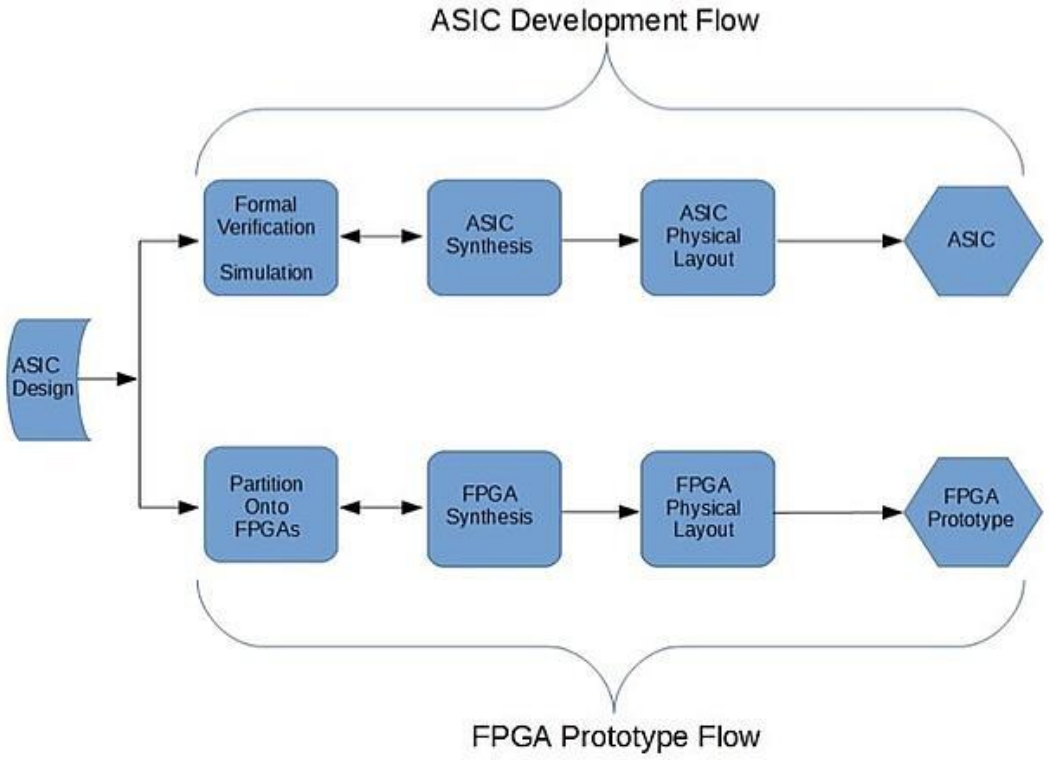
- Process almost any synthesizable Verilog-2005 design
- Converting Verilog to BLIF / EDIF/ BTOR / SMT-LIB / simple RTL Verilog / etc.
- Built-in formal methods for checking properties and equivalence
- Mapping to ASIC standard cell libraries (in Liberty File Format)
- Mapping to Xilinx 7-Series and Lattice iCE40 FPGAs
- Foundation and/or front-end for custom flows

Yosys can be adapted to perform any synthesis job by combining the existing passes (algorithms) using synthesis scripts and adding additional passes as needed by extending the Yosys C++ code base. Yosys is free software licensed under the ISC license (a GPL compatible license that is similar in terms to the MIT license or the 2-clause BSD license).
http://www.clifford.at/yosys/ - https://github.com/YosysHQ/yosys

FPGA Popularity

- FPGA-based ASIC prototype
- FPGA-based RISC-V
- FPGA-based Deep Learning
- FPGA-based Cryptocurrency Mining
- FPGA-based Internet of Things (IoT)

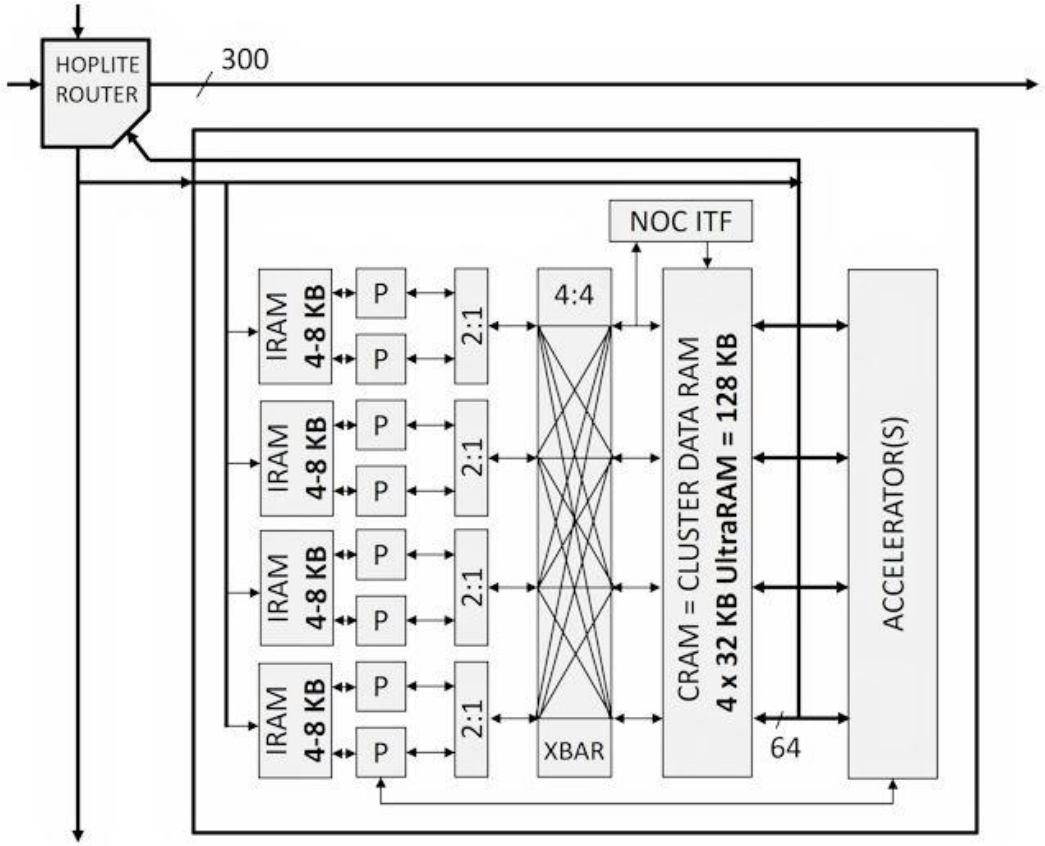
FPGA – ASIC Prototyping



Controlling the Complexity of FPGA Based ASIC Emulation
https://www.intrinsix.com/blog/controlling-the-complexity-of-fpga-based-asic-emulation

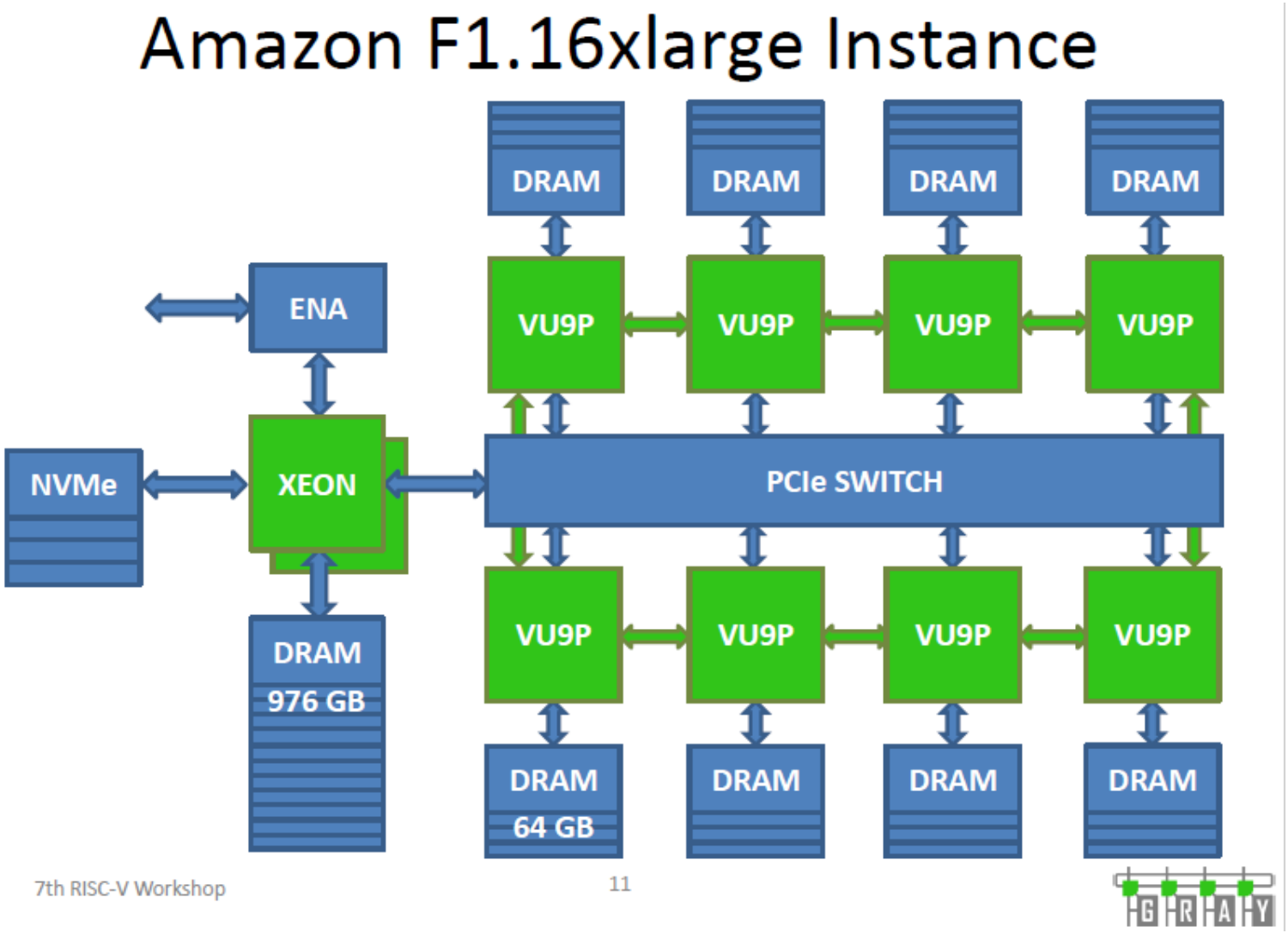
FPGA - RISC-V cluster

GRVI is an FPGA-efficient RISC-V RV32I soft processor. Phalanx is a parallel processor and accelerator array framework. Groups of processors and accelerators form shared memory clusters. Clusters are interconnected with each other and with extreme bandwidth I/O and memory devices by a 300- bit-wide Hoplite NOC. Example Kintex UltraScale KU040 system has 400 RISC-V cores, peak throughput of 100,000 MIPS, peak shared memory bandwidth of 600 GB/s, NOC bisection bandwidth of 700 Gbps, and uses 13 W.



GRVI Phalanx: A Massively Parallel RISC-V FPGA Accelerator Accelerator
Jan Gray, Gray Research LLC
https://arxiv.org/abs/1606.01037

FPGA - RISC-V cluster



RISC-V Cores and SoC Overview

Name	Links	Priv. spec	User spec	License	Supplier
rocket	GitHub	1.11-draft	2.3-draft	BSD	SiFive, UCB Bar
freedom	GitHub	1.11-draft	2.3-draft	BSD	SiFive
Berkeley Out-of-Order Machine (BOOM)	GitHub	1.11-draft	2.3-draft	BSD	Esperanto, UCB Bar
ORCA	GitHub		RV32IM	BSD	VectorBlox
RI5CY	GitHub		RV32IMC	Solderpad Hardware License v. 0.51	ETH Zurich, Università di Bologna
Zero-riscy	GitHub		RV32IMC	Solderpad Hardware License v. 0.51	ETH Zurich, Università di Bologna
Ariane	Website,GitHub		RV64IMC	Solderpad Hardware License v. 0.51	ETH Zurich, Università di Bologna
Riscy Processors	Website,GitHub			MIT	MIT CSAIL CSG
Minerva	GitHub	1.10	RV32I	BSD	LambdaConcept
OPenV/mriscv	GitHub		RV32I(?)	MIT	OnChipUIS
VexRiscv	GitHub		RV32I[M][C]	MIT	SpinalHDL
Roa Logic RV12	GitHub	1.9.1	2.1	Non-Commercial License	Roa Logic
SCR1	GitHub	1.10	2.2, RV32I/E[MC]	Solderpad Hardware License v. 0.51	Syntacore
Hummingbird E200	GitHub	1.10	2.2, RV32IMAC	Apache 2.0	Bob Hu
Shakti	Website,GitLab	1.11	2.2, RV64IMAFDC	BSD	IIT Madras
ReonV	GitHub			GPL v3	
PicoRV32	GitHub		RV32I/E[MC]	ISC	Clifford Wolf
MR1	GitHub		RV32I	Unlicense	Tom Verbeure

FPGA – Deep Learning

Compute Acceleration Products by BittWare

https://www.bittware.com/fpga/intel/boards/

FPGA – AI Inference

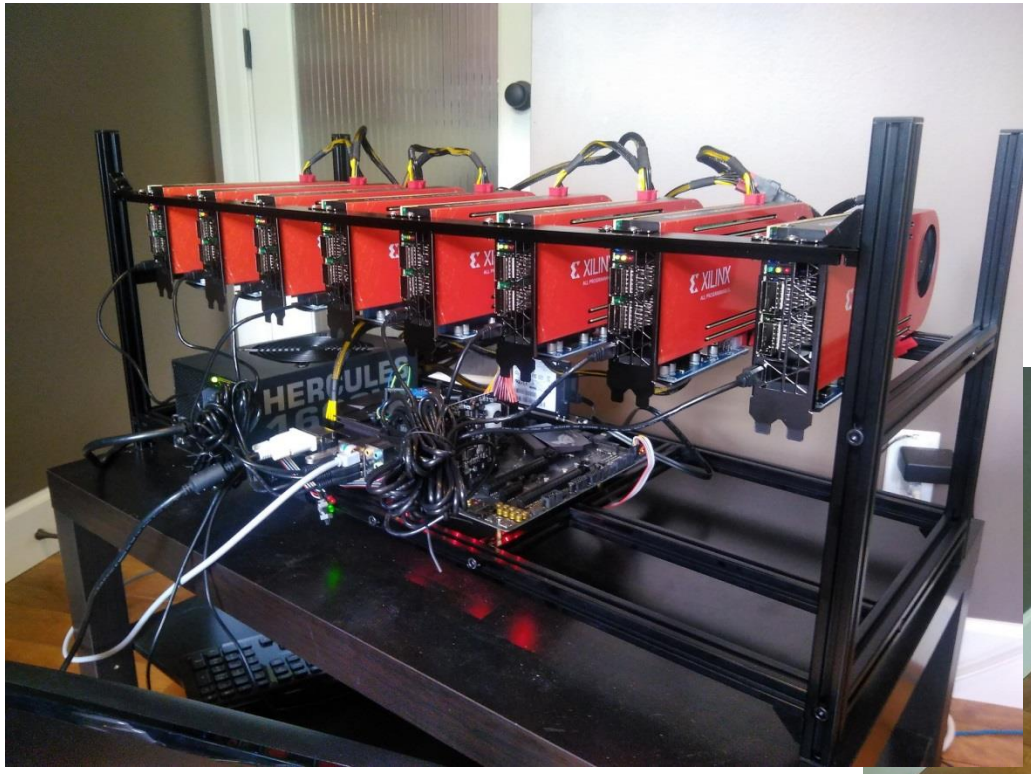
Virtex® UltraScale+™ VU9P FPGA

Virtex® UltraScale+™ FPGA VCU1525
Developer Board and Reference Design

- > 16nm TSMC FF+ FPGA
- > 2.5M System Logic Cells
- > 6840 DSP Blocks (18x27 MACs)
- > 382 Mbit On-Die SRAM
- > 4 DDR4-2400 x72 Channels
- > VU9P Virtex UltraScale+ FPGA
- > 21 TOPS (INT8)
- > 382 Mbit on-chip SRAM
- > 64 GByte on-board DRAM
- > 75W

XILINX UNVEILS XDNN FPGA ARCHITECTURE FOR AI INFERENCE
August 27, 2018 Nicole Hemsoth
https://www.nextplatform.com/2018/08/27/xilinx-unveils-xdnn-fpga-architecture-for-ai-inference/

FPGA – Crypto Mining



FPGA ultra-low-power IoT

An ultra-low-power FPGA for IoT applications
He Qi, Oluseyi Ayorinde, Benton H. Calhoun
Proceedings of the 2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S2017)
https://doi-org/10.1109/S3S.2017.8308753

Abstract: The rapid development of the Internet-of-Things requires hardware that is both energy-efficient and flexible, and an ultra-low-power Field-Programmable-Gate-Array (FPGA) is a very promising solution. This paper presents a near/sub-threshold FPGA with low-swing global interconnect, folded switch box (SB), per-path voltage scaling, and power-gating. A fully programmable 512-look-up-table FPGA chip is fabricated in 130nm CMOS. When implementing a 4bit-adder, the measured energy of the proposed FPGA is 15% less than the normalized energy of the state-of-the-art. When implementing fifteen selected low-power applications, the estimated energy of the proposed FPGA is on average 75x lower than Microsemi IGLOO.